Intel[®] HD Graphics OpenSource PRM

Volume 3 Part 2: Display Registers

For the all new 2010 Intel Core Processor Family Programmer's Reference Manual (PRM)

February 2010

Revision 1.0

IHD-OS-022810-V3PT2



You are free:

to Share -- to copy, distribute, display, and perform the work

Under the following conditions:

Attribution. You must attribute the work in the manner specified by the author or licensor (but not in any way that suggests that they endorse you or your use of the work).

No Derivative Works. You may not alter, transform, or build upon this work.

You are not obligated to provide Intel with comments or suggestions regarding this document. However, should you provide Intel with comments or suggestions for the modification, correction, improvement, or enhancement of: 9a) this document; or (b) Intel products, which may embody this document, you grant to Intel a non-exclusive, irrevocable, worldwide, royalty-free license, with the right to sublicense Intel's licensees and customers, under Recipient intellectual property rights, to use and disclose such comments and suggestions in any manner Intel chooses and to display, perform, copy, make, have made, use, sell, and otherwise dispose of Intel's and its sublicensee's products embodying such comments and suggestions in any manner and via any media Intel chooses, without reference to the source.

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL® PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER, AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT. Intel products are not intended for use in medical, life saving, or life sustaining applications.

Intel may make changes to specifications and product descriptions at any time, without notice.

Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them.

The Sandy Bridge chipset family, Havendale/Auburndale chipset family, Intel[®] 965 Express Chipset Family, Intel[®] G35 Express Chipset, and Intel[®] 965GMx Chipset Mobile Family Graphics Controller may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Intel and the Intel are trademarks of Intel Corporation in the U.S. and other countries.

*Other names and brands may be claimed as the property of others.

Copyright © 2010, Intel Corporation. All rights reserved.



Revision History

Document Number	Revision Number	Description	Revision Date
IHD-OS-022810-R1V3PT2	1.0	First Release.	February 2010

§§



	troduction and Register Summary	
1.1.1	Terminology	7
1.1.2	Register Protection for Panel Protection	7
1.1.3	Display Mode Set Sequence	8
	th Shared Functions (40000h–4FFFFh)	
	GA Control Registers	
	VGACNTRL—VGA Display Plane Control Register	
2.2 Si	ne ROM Registers	
2.2.1		
2.3 Po	ower Measurement Registers	
2.3.1	DE_POWER1 – Display Engine Power Register 1	
2.3.2	DE_POWER2 – Display Engine Power Register 2	
	PFC Control Registers (43200h–433FFh)	
2.4.1	DPFC_CB_BASE – DPFC Compressed Buffer Base Address	
2.4.2	DPFC_CONTROL— DPFC Control	20
2.4.3	DPFC_RECOMP_CTL — DPFC ReComp Control	
2.4.4	DPFC_CPU_Fence_Offset — Y Offset CPU Fence Base to Display Buffer Base	
	terrupt Control Registers	
2.5.1	Display Engine Interrupt Registers Bit Definition	
2.5.2	DEISR — Display Engine Interrupt Status Register	
2.5.3	DEIMR — Display Engine Interrupt Mask Register	
2.5.4	DEIIR — Display Engine Interrupt Identity Register	
2.5.5	DEIER — Display Engine Interrupt Enable Register	
2.5.6	GT Interrupt Registers Bit Definition	
2.5.7	GTISR — GT Interrupt Status Register	
2.5.8	GTIMR — GT Interrupt Mask Register	
2.5.9	GTIIR — GT Interrupt Identity Register	
2.5.10		
2.5.11		40
2.5.12		
2.5.13		
2.5.14	5 1 7 5	
2.5.15		
2.5.16		
2.5.17		
	splay Engine Render Response	
2.6.1		
2.6.2	DERRMR — Display Engine Render Response Mask Register splay Arbitration Control	
2.7 D	DISP_ARB_CTL—Display Arbiter Control	
2.7.1	DISP_ARB_CTL2—Display Arbiter Control 2 [DevSNB]	49 51
	splay Watermark Registers	ו ט בא
2.8 D	WM0_PIPE_A—Pipe A Main Watermarks	
2.8.1	WM0_PIPE_A—Pipe A Main Watermarks	
2.8.2	WM0_PIPE_B—Pipe B Main Watermarks	
2.8.3	WM1—Low Power 1 Display Watermarks WM2—Low Power 2 Display Watermarks	
2.8.4	WM2—Low Power 2 Display Watermarks WM3—Low Power 3 Display Watermarks	
2.8.5	WMIS—Low Power 3 Display Watermarks WM1S—Low Power 1 Sprite Watermark	
2.0.0		



2	2.9 Re	fresh Rate Hardware Control Register	
	2.9.1	RR_HW_CTL—Refresh Rate Hardware Control	
2	2.10 Ba	acklight Control and Modulation Histogram Registers	
	2.10.1	BLC_PWM_CTL2—Backlight PWM Control Register 2	
	2.10.2	BLC_PWM_CTL—Backlight PWM Control Register	
	2.10.3	BLM_HIST_CTL—Image Enhancement Histogram Control Register	
		IIST_CTL—Image Enhancement Histogram Control	
	2.10.4	Image Enhancement Bin Data Register	
	2.10.5	Histogram Threshold Guardband Register	
2		otion Blur Mitigation (MBM) Control	
	2.11.1	MBM_CTRL—MBM Control	
	2.11.2	MBM_TBL—MBM Overdrive Table	
2		blor Conversion & Control Registers	
	2.12.1	Pipe A Color Control	
	2.12.2	Pipe B Color Control	
4		splay Palette Registers (4A000h–4CFFFh)	
	2.13.1	LGC_PALETTE_A—Pipe A Legacy Display Palette	
	2.13.2	LGC_PALETTE_B—Pipe B Legacy Display Palette	
	2.13.3	PREC_PALETTE_A—Pipe A Precision Display Palette	
	2.13.4	PREC_PALETTE_B—Pipe B Precision Display Palette	
	2.13.5	PIPEAGCMAX—Pipe A Gamma Correction Max	
,	2.13.6	PIPEBGCMAX — Pipe B Gamma Correction Max oftware Flag Registers (4F000h–4F10Fh)	
4	2.14 30	Software Flag Registers	
	2.14.1	GT Scratchpad	
		•	
3.		n Pipe and Port Controls (60000h–6FFFh)	
	3.1.1	Pipe A Timing	
	3.1.2	Pipe A M/N Values	
	3.1.3	Pipe B M/N Values	
	3.1.4	Panel Fitter Control Registers	
	3.1.5	Panel Fitter Coefficient Registers	118
	3.1.6	Panel Fitter Horizontal Coefficients	120
	3.1.7	Panel Fitter Vertical Coefficients	
	3.1.8	FDI AFE Control (6C000h–6DFFFh)	124
4.	Plan	e Controls (70000h–7FFFFh)	
	4.1.1	Display Pipeline A	
	4.1.2	Display Pipeline A Counters and Timestamps	
	4.1.3	Display Timestamp	
	4.1.4	Display Pipeline B	
	4.1.5	Display Pipeline B Counters and Timestamps	
	4.1.6	Cursor A Plane Control Registers	
	4.1.7	Cursor B Plane Control Registers	
	4.1.8	Primary A Plane Control	
	4.1.9	Primary B Plane Control	
	4.1.10	Video Sprite A Control	
	4.1.11	Video Sprite B Control	



Display Registers [DevILK]

1.1 Introduction and Register Summary

This chapter contains the register descriptions for the display portion of a family of integrated graphics devices. These registers do vary by devices within the family of devices so special attention needs to be paid to which devices use which registers and register fields.

Different devices within the family may add, modify, or delete registers or register fields relative to another device in the same family based on the supported functions of that device. Additional information on the use and programming of these registers can be found in the display chapter.

The following table contains the sections break down where the register information is contained within this chapter:

Address Range	Description
40000h-4FFFFh	Shared Functions
50000h-5FFFFh	Messages
60000h-6FFFFh	Pipe and Port Controls
70000h–7FFFFh	Plane Controls



1.1.1 Terminology

Description	Software Use	Should be implemented as
Read/Write	This bit can be read or written.	
Reserved:	Don't assume a value for these bits. Writes have no effect.	Writes are ignored. Reads return zero.
Reserved: write as zero, must be zero, or MBZ	Software must always write a zero to these bits. This allows new features to be added using these bits that will be disabled when using old software and as the default case.	Writes are ignored. Reads return zero. Maybe be connected as Read/Write in future projects.
Reserved: software must preserve contents	Software must write the original value back to this bit. This allows new features to be added using these bits.	Read only Read/Write.
Read Only	This bit is read only. The read value is determined by hardware. Writes to this bit have no effect.	According to each specific bit. The bit value is determined by hardware and not affected by register writes to the actual bit.
Read/Clear	This bit can be read. Writes to it with a one cause the bit to clear.	Hardware events cause the bit to be set and the bit will be cleared on a write operation where the corresponding bit has a one for a value.
Double Buffered	Write when desired. Read gives the unbuffered value (written value) unless specified otherwise. Written values will update to take effect after a certain point. Some have a specific arming sequence where a write to another register is required before the update can take place. This is used to ensure atomic updates of several registers.	Two stages of registers used. First stage is written into and used for readback (unless specified otherwise). First stage value is transferred into second stage at the update point. Second stage value is used to control hardware. Arm/disarm flag needed for specific arming sequences.

1.1.2 Register Protection for Panel Protection

TBD



1.1.3 Display Mode Set Sequence

Enable sequence
[ILK]: CPU PLL warmup = 20uS
[ILK]: CPU FDI transmitter PLL warmup = 10us
[ILK]: DMI latency = 20uS
FDI training pattern 1 time = 0.5uS
FDI training pattern 2 time = 1.5uS
FDI idle pattern time = 31uS
Enable sequence



Enable panel power as needed to retrieve panel configuration

- 1. Enable PCH clock reference source and PCH SSC modulator, wait for warmup (Can be done anytime before enabling port)
- 2. If enabling port on PCH: (Must be done before enabling CPU pipe or FDI)
 - a. Enable PCH FDI Receiver PLL, wait for warmup plus DMI latency
 - b. Switch from Rawclk to PCDclk in FDI Receiver (FDI A OR FDI B)
 - c. [ILK] CPU FDI PLL is always on and does not need to be enabled
- 3. Enable CPU panel fitter if needed for hires, required for VGA (Can be done anytime before enabling CPU pipe)
- 4. Configure CPU pipe timings, M/N/TU, and other pipe settings (Can be done anytime before enabling CPU pipe)
- 5. Enable CPU pipe
- 6. Configure and enable CPU planes (VGA or hires)
- 7. If enabling port on PCH:
 - a. Train FDI
 - i. Set pre-emphasis and voltage (iterate if training steps fail)
 - ii. Enable CPU FDI Transmitter and PCH FDI Receiver with Training Pattern 1 enabled.
 - iii. Wait for FDI training pattern 1 time
 - iv. Read PCH FDI Receiver ISR
 - v. Enable training pattern 2 on CPU FDI Transmitter and PCH FDI Receiver
 - vi. Wait for FDI training pattern 2 time
 - vii. Read PCH FDI Receiver ISR
 - viii. Enable normal pixel output on CPU FDI Transmitter and PCH FDI Receiver
 - ix. Wait for FDI idle pattern time for link to become active
 - b. Configure and enable PCH DPLL, wait for PCH DPLL warmup (Can be done anytime before enabling PCH transcoder)
 - c. Configure PCH transcoder timings, M/N/TU, and other transcoder settings (should match CPU settings).
 - d. Enable PCH transcoder
- 8. Enable ports
- 9. Enable panel power through panel power sequencing
- 10. Wait for panel power sequencing to reach enabled steady state
- 11. Disable panel power override
- 12. Enable panel backlight



Disable sequence

- 1. Disable Panel backlight
- 2. Disable panel power through panel power sequencing
- 3. Disable CPU planes (VGA or hires)
- 4. [ILK] Disable CPU panel fitter
- 5. Disable CPU pipe
- 6. Wait for CPU pipe off status (CPU pipe config register pipe state)
- 7. [ILK] Disable CPU panel fitter (Can be done anytime after CPU pipe is off)
- 8. Else disabling port on PCH:
 - a. Disable CPU FDI Transmitter and PCH FDI Receiver
 - b. Disable port
 - c. Disable PCH transcoder
 - d. Wait for PCH transcoder off status (PCH transcoder config register transcoder state)
 - e. Disable PCH DPLL (Can be done anytime after PCH ports and transcoder are off)
 - f. If no other PCH transcoder is enabled
 - i. Switch from PCDclk to Rawclk in PCH FDI Receiver
 - ii. Disable PCH FDI Receiver PLL
- 9. If SSC is no longer needed, disable PCH SSC modulator
- 10. If clock reference no longer needed, disable PCH clock reference source



2. North Shared Functions (40000h– 4FFFFh)

2.1 VGA Control Registers

2.1.1 VGACNTRL—VGA Display Plane Control Register

	N N	/GACNTRL—	/GA Display Plane Control Register		
Register T	ype: MMIC)			
	ffset: 41000)h			
Project:	All				
Default Val	lue: 00002	2900h			
Access:	R/W				
Size (in bit	s): 32				
Bit			Description		
31	VGA_Displ	ay_Disable			
	Project:	All			
	Default Valu	ie: 0b	VGA Display Enabled		
This bit will disable the VGA compatible display mode. It has no effect on VGA register or A0000- BFFFF memory aperture accesses which are controlled by the PCI configuration and VGA register settings. VGA display should only be enabled if all display planes other than VGA are disabled. After enabling the VGA, most display planes need to stay disabled, only the VGA popup (cursor A) can be enabled.					
	Value	Name	Description	Project	
	0b	Enable	VGA Display Enabled	All	
	1b	Disable	VGA Display Disabled	All	
30	Reserved	Project: All	Format: PBC	, ,	



29	VGA_Pip	be_Select				
	Project:		All			
	Default Value: 0b					
	changed	only when t		etermines which pipe is to receive the VGA display play is in the disabled state via the VGA display d		
	Value	Name		Description	Project	
	0b	PipeA		Selects Assigns the VGA display to Pipe A	All	
	1b	PipeB		Selects Assigns the VGA display to Pipe B	All	
28:27	Reserved	d Proje	ect: All	Format	it: PBC	
26	VGA_Bo	rder_Enab	le			
	Project:		All			
			0b f the VGA b	order areas are included in the active display area	a and do o	r do not
	This bit o appear o The bord	determines i on the port o er if enabled	f the VGA b output. d will be sca	border areas are included in the active display area aled along with the pixel data. Setting this bit allow er area of the image.		
	This bit o appear o The bord	determines i on the port o er if enabled	f the VGA b output. d will be sca	aled along with the pixel data. Setting this bit allover area of the image.		
	This bit of appear o The bord positione	determines i on the port o er if enable d overlappir	f the VGA b utput. d will be sca ng the borde Descripti	aled along with the pixel data. Setting this bit allow er area of the image. Ion der areas are not included in the image size calcu	ws the pop	up to be
	This bit of appear of The bord positioned Value	determines i on the port o er if enable d overlappir Name	f the VGA b output. d will be sca ng the borde Descripti VGA Bord for active VGA Bord	aled along with the pixel data. Setting this bit allow er area of the image. Ion der areas are not included in the image size calcu	ws the pop	up to be Project
25	This bit of appear o The bord positioner Value 0b	determines i on the port o er if enabled d overlappin Name Disable Enable	f the VGA b output. d will be sca ng the borde Descripti VGA Bord for active VGA Bord display ar	aled along with the pixel data. Setting this bit allow er area of the image. Son der areas are not included in the image size calcu area. der areas are enabled and passed to the display p nd used in the image size calculations.	ws the pop	up to be Project All
25 24	This bit of appear of The bord positioned Value 0b 1b Reserved	determines i on the port o er if enable d overlappir Name Disable Enable d Proje	f the VGA b output. d will be sca ng the borde Descripti VGA Bord for active VGA Bord display ar	aled along with the pixel data. Setting this bit allow er area of the image. Ion der areas are not included in the image size calcu area. der areas are enabled and passed to the display p ind used in the image size calculations. Format	ws the pop lations pipe for	up to be Project All
-	This bit of appear of The bord positioned Value 0b 1b Reserved	determines i on the port o er if enable d overlappir Name Disable Enable d Proje	f the VGA b utput. d will be sca ng the borde Descripti VGA Bord for active VGA Bord display ar ect: All	aled along with the pixel data. Setting this bit allow er area of the image. Ion der areas are not included in the image size calcu area. der areas are enabled and passed to the display p ind used in the image size calculations. Format	ws the pop lations pipe for	up to be Project All
-	This bit of appear of The bord positioned of the bord position	determines i on the port o er if enabled d overlappin Name Disable Enable d Proje Ior_Space_	f the VGA b output. d will be sca bg the borde VGA Bord for active VGA Bord display ar ect: All Conversio	aled along with the pixel data. Setting this bit allow er area of the image. Ion der areas are not included in the image size calcu area. der areas are enabled and passed to the display p ind used in the image size calculations. Format	ws the pop lations pipe for	up to be Project All
-	This bit c appear o The bord positioned 0b 1b 1b Reserved Pipe_Col Project: Default V This bit e	determines i on the port o er if enabled d overlappir Name Disable Enable Enable d Proje Ior_Space_ 'alue: nables pipe	f the VGA b utput. d will be sca ing the border VGA Bord for active VGA Bord display ar ect: All Conversio All Ob color space	aled along with the pixel data. Setting this bit allow er area of the image. Ion der areas are not included in the image size calcu area. der areas are enabled and passed to the display p ind used in the image size calculations. Format	ulations pipe for t: PBC	up to be Project All All
-	This bit c appear o The bord positioned 0b 1b 1b Reserved Pipe_Col Project: Default V This bit e	determines i on the port o er if enabled d overlappir Name Disable Enable Enable d Proje Ior_Space_ 'alue: nables pipe	f the VGA b utput. d will be sca ing the border VGA Bord for active VGA Bord display ar ect: All Conversio All Ob color space	aled along with the pixel data. Setting this bit allow er area of the image.	ulations pipe for t: PBC	Project All All
-	This bit c appear o The bord positioned 0b 1b 1b Reserved Project: Default V This bit e registers	determines i on the port o er if enabled d overlappir Name Disable Enable Enable d Proje Ior_Space_ 'alue: mables pipe must be se	f the VGA b utput. d will be sca be borded VGA Bord for active VGA Bord display ar ect: All Conversio All Ob color space t to match th Descripti	aled along with the pixel data. Setting this bit allow er area of the image.	Ilations pipe for it: PBC	Project All All CSC



23	VGA Pal	ette_Read_Select					
	Project:	All					
	Default Value: 0b						
	This bit only applies to dual display pipe devices and determines which palette VGA palette read accesses will occur from.						
	VGA pale	tte reads are reads fror	n I/O address 0x3c9.				
	Value	Name	Description	Project			
	0b	Palette A	VGA palette reads will access Palette A	All			
	1b	Palette B	VGA palette reads will access Palette B	All			
22	VGA_Pal	ette_A_Write_Disable		1			
	Project:	All					
	Default Va	alue: Ob					
	can be the	e destination. If both a	e VGA palette writes will have as a destination. G e disabled, writes will not affect the palette conte				
	· .	tte writes are writes to	/O address 0x3C9h.	1			
	Value	Name	Description	Project			
	0b	Update Palette A	VGA palette writes will update Palette A	All			
	1b	Not Update Palette A	VGA palette writes will not update Palette A	All			
21		Not Update Palette A ette_B_Write_Disable		All			
21	VGA_Pal	ette_B_Write_Disable		All			
21	VGA_Pal Project: Default Va	ette_B_Write_Disable All alue: 0b		1			
21	VGA_Pal Project: Default Va This deter	ette_B_Write_Disable All alue: 0b mines which palette th		Dne or both palettes			
21	VGA_Pale Project: Default Va This deter can be the	ette_B_Write_Disable All alue: 0b mines which palette th	e VGA palette writes will have as a destination. C	Dne or both palettes			
21	VGA_Pale Project: Default Va This deter can be the	ette_B_Write_Disable All alue: 0b mines which palette the e destination. If both a	e VGA palette writes will have as a destination. C	Dne or both palettes			
21	VGA_Pale Project: Default Va This deter can be the VGA pale	ette_B_Write_Disable All alue: 0b rmines which palette the e destination. If both an tte writes are writes to	e VGA palette writes will have as a destination. Or e disabled, writes will not affect the palette conte //O address 0x3C9h.	One or both palettes nts.			
21	VGA_Pale Project: Default Va This deter can be the VGA pale	ette_B_Write_Disable All alue: 0b mines which palette the e destination. If both an tte writes are writes to Name	e VGA palette writes will have as a destination. Or re disabled, writes will not affect the palette conte /O address 0x3C9h. Description VGA palette writes will update Palette B	Dne or both palettes nts. Project			
	VGA_Pale Project: Default Va This deter can be the VGA pale Value Ob 1b	ette_B_Write_Disable All alue: 0b mines which palette the destination. If both an tte writes are writes to Name Update Palette B	e VGA palette writes will have as a destination. Or e disabled, writes will not affect the palette conte //O address 0x3C9h. Description VGA palette writes will update Palette B VGA palette writes will not update Palette B	Dne or both palettes nts. Project All			
	VGA_Pale Project: Default Va This deter can be the VGA pale Value Ob 1b	ette_B_Write_Disable All alue: 0b mines which palette the e destination. If both an tte writes are writes to Name Update Palette B Not Update Palette B	e VGA palette writes will have as a destination. Or e disabled, writes will not affect the palette conte //O address 0x3C9h. Description VGA palette writes will update Palette B VGA palette writes will not update Palette B	Dne or both palettes nts. Project All			
	VGA_Pale Project: Default Va This deter can be the VGA pale Value Ob 1b	ette_B_Write_Disable All alue: 0b mines which palette the e destination. If both an tte writes are writes to Name Update Palette B Not Update Palette B /GA_8-Bit_Palette_Er All	e VGA palette writes will have as a destination. Or e disabled, writes will not affect the palette conte //O address 0x3C9h. Description VGA palette writes will update Palette B VGA palette writes will not update Palette B	Dne or both palettes nts. Project All			
	VGA_Pale Project: Default Va This deter can be the VGA pale Value 0b 1b Legacy_V Project: Default Va This bit or 8-bits of d the read.	ette_B_Write_Disable All alue: 0b mines which palette the e destination. If both an tte writes are writes to Name Update Palette B Not Update Palette B /GA_8-Bit_Palette_En All alue: 0b hly affects reads and we lata are shifted up two b It provides backward c E support for 8-bit pale	e VGA palette writes will have as a destination. Or e disabled, writes will not affect the palette conte //O address 0x3C9h. Description VGA palette writes will update Palette B VGA palette writes will not update Palette B	Dne or both palettes nts. Project All All n the 6-bit mode, the ed two bits down on ault state) as well as			
	VGA_Pale Project: Default Va This deter can be the VGA pale Value 0b 1b Legacy_V Project: Default Va This bit or 8-bits of d the read. VESA VB	ette_B_Write_Disable All alue: 0b mines which palette the e destination. If both an tte writes are writes to Name Update Palette B Not Update Palette B /GA_8-Bit_Palette_En All alue: 0b hly affects reads and we lata are shifted up two b It provides backward c E support for 8-bit pale	e VGA palette writes will have as a destination. Or re disabled, writes will not affect the palette content /O address 0x3C9h. Description VGA palette writes will update Palette B VGA palette writes will not update Palette B vGA palette writes will not update Palette B rable	Dne or both palettes nts. Project All All n the 6-bit mode, the ed two bits down on ault state) as well as			
21	VGA_Pale Project: Default Va This deter can be the VGA pale Value 0b 1b Legacy_V Project: Default Va This bit or 8-bits of d the read. VESA VB	ette_B_Write_Disable All alue: 0b mines which palette the e destination. If both an tte writes are writes to Name Update Palette B Not Update Palette B /GA_8-Bit_Palette_En All alue: 0b hly affects reads and wi lata are shifted up two b It provides backward c E support for 8-bit pale th.	e VGA palette writes will have as a destination. Or re disabled, writes will not affect the palette content /O address 0x3C9h. Description VGA palette writes will update Palette B VGA palette writes will not update Palette B wable writes to the palette through VGA I/O addresses. In bits on the write (upper two bits are lost) and shift ompatibility for original VGA programs (in it's defatte. It does not affect palette accesses through the	Dne or both palettes nts. Project All All All n the 6-bit mode, the ed two bits down on ault state) as well as he palette register			



19	Reserved	I		
18	Reserved	I		
7:16	Reserved	Project:	All	Format: PBC
5:12	Reserved	I		
11:8	Reserved	1		
7:6	Blink Du	ty_Cycle		
-				
-	Project:		All	
-			All 00b	
-	Project: Default Va	alue:		link duty cycle.
-	Project: Default Va	alue:	00b	link duty cycle. Project
-	Project: Default Va Controls t	alue: he VGA text mod	00b de blink duty cycle <u>relative to the VGA cursor bl</u>	
-	Project: Default Va Controls the Value	alue: he VGA text moc	00b de blink duty cycle <u>relative to the VGA cursor bl</u> Description	Project
-	Project: Default Va Controls the Value	alue: he VGA text mod Name 100%	00b de blink duty cycle <u>relative to the VGA cursor bl</u> Description 100% Duty Cycle, Full Cursor Rate	Project All
-	Project: Default Va Controls the Value 00b 01b	alue: he VGA text mod Name 100% 25%	00b de blink duty cycle relative to the VGA cursor bl Description 100% Duty Cycle, Full Cursor Rate 25% Duty Cycle, ½ Cursor Rate	Project All All



2.2 Sine ROM Registers

2.2.1 SINE_ROM—Sine ROM

		SINE_ROM-	Sine ROM		
Register T	ype: MMIO				1
-	offset: 42200h				
Project:	All				
Default Va					
Access:	R/W Special				
Size (in bit	ts): 32				4
The angle is	s written to bits [16:6] as			of filter coefficients.	1
Bit			escription		1
31:17	Reserved Project	t: All	Fc	ormat:	1
16:6	Sine				
	Project:	All			L
	Default Value:	0b			Τ
	Write the angle, read	the sine			
					T
	Programming Notes				+
	Programming Notes Examples of values to				+
		o write:			
	Examples of values to	o write: or 360 degrees			
	Examples of values to 0000000000b = 0 or	o write: or 360 degrees degrees			
	Examples of values to 0000000000b = 0 of 0100000000b = 90 of	o write: or 360 degrees degrees 0 degrees			



2.3 **Power Measurement Registers**

These registers are read by the PMU to get information for use in device power estimation.

2.3.1 DE_POWER1 – Display Engine Power Register 1

	DE_POWER1 – Display Engine Power Register 1							
Register Ty	ype: 432	208hMMIO						
Project:Ad Offset:								
Default Value:Proje		000000hDevSNB						
Access:Default R/W0000000h Value:								
Size (in bits):Acces	32F ss:	Read Only						
		register can not be c	hang	ged, except bit 31, while compression is e	enabled			
Size (in bit	s): 32							
Bit				Description				
31:8	Reserved	d Project: All		Format: MB	Z			
Enable_Frame_Buffer_Compression								
	Project:	All						
	Default V	alue: 0b						
	This bit is	s used to globally enab	ole DF	PFC function at the next Vertical Blank start.				
	Value	Name		Description		Project		
	0b	Disable		Disable frame buffer compression		All		
	1b	Enable		Enable frame buffer compression		All		
307:4	Plane_Se	electTransmit_Lanes	Ena	bled				
	Project:	All						
	Range	012						
	The total	number of eDP & FDI	lanes	s enabled.				
	Default V	alue: 0b						
	Value	Name	De	scription	Projec	ct		
	0b	Plane A	Pla	ane A	All			
	1b	Plane B	Pla	ane B	All			



293:2	CPII For	nce_EnableEnabled	Panel Fitters		· · · · · · · · · · · · · · · · · · ·				
200.2	Project:								
	Range 02								
	-		umes an additional xx mW of power.						
	Default V								
	Value	Name	Description	F	Project				
	0b	No CPU Disp Buf	Display Buffer is not in a CPU fence. No modif are allowed from CPU to the Display Buffer	fications A	All				
	1b	CPU Disp Buf	Display Buffer exists in a CPU fence	A	AII				
291:0	Enabled	DPLLs							
	Project:	All							
	Range	02							
	Each DPI	LL enabled consumes	s xx mW of power.						
	Reserved	d							
	Reserved	d Project: A	ll Forma	at: MBZ					
28									
27	CS_SYN	C_FLIP_NUKE_Disa	ble						
	Project:	All							
	Default V								
	Default V	alue: 0b	command streamer SYNC Flips from resetting the	DPFC.					
	Default V	alue: 0b	command streamer SYNC Flips from resetting the Description	DPFC.					
	Default V Setting th	alue: 0b is bit will disable the o							
	Default V Setting th	alue: 0b his bit will disable the o Name	Description	Project					
26	Default V Setting th Value Ob 1b	alue: 0b iis bit will disable the o Name Enable	Description Enable the CS SYNC Flip Nuke Disable the CS SYNC Flip Nuke	Project All					
26	Default V Setting th Value Ob 1b	alue: 0b is bit will disable the o Name Enable Disable	Description Enable the CS SYNC Flip Nuke Disable the CS SYNC Flip Nuke	Project All					
26	Default V Setting th Ob 1b MMIO_S	alue: 0b is bit will disable the o Name Enable Disable YNC_FLIP_Nuke_Dis All	Description Enable the CS SYNC Flip Nuke Disable the CS SYNC Flip Nuke	Project All					
26	Default V Setting th Ob 1b MMIO_S Project: Default V	alue: 0b iis bit will disable the o Name Enable Disable YNC_FLIP_Nuke_Dis All alue: 0b	Description Enable the CS SYNC Flip Nuke Disable the CS SYNC Flip Nuke	Project All					
26	Default V Setting th Ob 1b MMIO_S Project: Default V	alue: 0b iis bit will disable the o Name Enable Disable YNC_FLIP_Nuke_Dis All alue: 0b	Description Enable the CS SYNC Flip Nuke Disable the CS SYNC Flip Nuke sable	Project All					
26	Default V Setting th Ob 1b MMIO_S Project: Default V Setting th	alue: 0b is bit will disable the of Name Enable Disable YNC_FLIP_Nuke_Dis All alue: 0b his bit will disable the	Description Enable the CS SYNC Flip Nuke Disable the CS SYNC Flip Nuke sable MMIO Sync Flip from resetting the DPFC.	Project All All					
26	Default V Setting th Ob 1b MMIO_S Project: Default V Setting th Value	alue: 0b is bit will disable the of Name Enable Disable YNC_FLIP_Nuke_Dis All alue: 0b his bit will disable the Name	Description Enable the CS SYNC Flip Nuke Disable the CS SYNC Flip Nuke sable MMIO Sync Flip from resetting the DPFC. Description	Project All All Project					
26	Default V Setting th Ob 1b MMIO_S Project: Default V Setting th Value Ob	alue: 0b is bit will disable the o Name Enable Disable YNC_FLIP_Nuke_Dis All alue: 0b nis bit will disable the Name Enable Disable	Description Enable the CS SYNC Flip Nuke Disable the CS SYNC Flip Nuke sable MMIO Sync Flip from resetting the DPFC. Description Enable the MMIO Sync Flip Nuke	Project All All Project All					
	Default V Setting th Ob 1b MMIO_S Project: Default V Setting th Ob 1b	alue: 0b is bit will disable the o Name Enable Disable YNC_FLIP_Nuke_Dis All alue: 0b nis bit will disable the Name Enable Disable	Description Enable the CS SYNC Flip Nuke Disable the CS SYNC Flip Nuke sable MMIO Sync Flip from resetting the DPFC. Description Enable the MMIO Sync Flip Nuke	Project All All Project All					
	Default V Setting th Ob 1b MMIO_S Project: Default V Setting th Value Ob 1b Persister	alue: 0b is bit will disable the of Name Enable Disable YNC_FLIP_Nuke_Dis All alue: 0b his bit will disable the Name Enable Disable Mame All All All All	Description Enable the CS SYNC Flip Nuke Disable the CS SYNC Flip Nuke sable MMIO Sync Flip from resetting the DPFC. Description Enable the MMIO Sync Flip Nuke	Project All All Project All					
	Default V Setting th Ob 1b MMIO_S Project: Default V Setting th Value Ob 1b Persister Project:	alue: 0b is bit will disable the of Name Enable Disable YNC_FLIP_Nuke_Dis All alue: 0b his bit will disable the Name Enable Disable Disable All All	Description Enable the CS SYNC Flip Nuke Disable the CS SYNC Flip Nuke sable MMIO Sync Flip from resetting the DPFC. Description Enable the MMIO Sync Flip Nuke	Project All All Project All All	Project				
	Default V Setting th Ob 1b MMIO_S Project: Default V Setting th Value Ob 1b Persister Project: Default V	alue: 0b is bit will disable the of Name Enable Disable YNC_FLIP_Nuke_Dis All alue: 0b is bit will disable the Disable Disable nt_Mode All alue: 0b	Description Enable the CS SYNC Flip Nuke Disable the CS SYNC Flip Nuke sable MMIO Sync Flip from resetting the DPFC. Description Enable the MMIO Sync Flip Nuke Disable the MMIO Sync Flip Nuke	Project All All Project All All All F	Project				



24:16	Reserved	ł						
15	Reserved	Reserved						
14:8	Reserved	Reserved Project: All Format: MBZ						
7:6	Compres	sion_Limit						
	Project:		All					
	Default Va	alue:	0b					
	This register sets a minimum limit on compression. It is also used to determine the size of the compressed buffer.							
		pression		Pixel F	Format			
	R	atio		16 bpp	32 bpp			
	1		Not Sup	ported	Supported (CFB=FB)			
	1/2		Supporte	Supported (CFB=FB) Supported (CFB=1/2 FB)				
	1/4 Support			d (CFB=1/2FB) Supported (CFB=1/4 FB)				
	FB = Frame Buffer Size							
	CFB = Co	mpressed F	rame Buff	er Size				
	Value Name Desc			cription				
	00b	1:1	1:1 compression, compressed buffer is the same size as the uncompressed buffer			All		
	01b	2:1	2:1 compression, compressed buffer is one half the size of the uncompressed buffer.			All		
	10b	4:1		ompression, compressed buffe mpressed buffer.	r is one quarter the size of the	All		
			Deer			All		
	11b	Reserved	Rese	erved		/ 11		
5:4		Reserved ck_Waterm		rved		7.01		
5:4				rved		7.41		
5:4	Write_Ba	ck_Waterma	ark	rved		7.0		
5:4	Write_Ba Project: Default Va Comprese	ck_Waterma alue: sed data writ	ark All Ob e back en	gine waits for this amount of da	ata (per segment) to be ready be be a 1, or SR disabled for this to	fore		
5:4	Write_Ba Project: Default Va Compress writing the	ck_Waterma alue: sed data writ	ark All Ob e back en	gine waits for this amount of da		fore		
5:4	Write_Ba Project: Default Va Compress writing the effect.	ck_Waterma alue: sed data writ e data out to	All Ob e back en memory.	gine waits for this amount of da Compression SR mode must b	be a 1, or SR disabled for this to	fore		
5:4	Write_Ba Project: Default Va Compress writing the effect. Value	ck_Waterma alue: sed data writ e data out to Name	All Ob e back en memory.	gine waits for this amount of da Compression SR mode must t Description	pe a 1, or SR disabled for this to Project	fore		



	DE_POWER1 – Display Engine Power Register 1					
3:0	CPU_Fence_Numb	ber				
	Project:	DevILK				
	Default Value:	Ob				
	This field specifies the CPU visible FENCE number corresponding to the placement of the uncompressed frame buffer					
3:0	Reserved					

2.3.2 DE_POWER2 – Display Engine Power Register 2

Register T	vne [.]	MMIO	
Address C		42404h	
Project:		DevSNB	
Default Value:		0000000h	
Access:		Read Only	
Size (in bi	ts):	32	
Bit		Description	
31:0	DE_I	pandwidth_counter	Project: All
		counter increments on every cache line put arriving at g the difference between two reads at a known interval	



2.4 DPFC Control Registers (43200h–433FFh)

2.4.1 DPFC_CB_BASE – DPFC Compressed Buffer Base Address

Register Ty	/pe: MMIO					
Address Of	fset: 43200h	۱				
Project:	All					
Default Valu	ue: 000000)00h				
Access:	R/W					
Size (in bits	s): 32					
The content	ts of this regi	ster can not	be changed wl	nile compression is ena	abled.	
Bit				Description		
31:28	Reserved	Project:	All		Format:	MBZ
27:12	Compressed	d_Frame_Buf	fer_Offset_Add	ress	Project:	All
	This register	specifies offs	et of the Compre	essed Frame Buffer from	the base of stole	n memory.
	The buffer m	nust be 4K byt	e aligned.			
		,				

2.4.2 DPFC_CONTROL— DPFC Control

DPFC_CONTROL— DPFC Control					
Register Type:	MMIO				
Address Offset:	43208h				
Project:	All				
Default Value:	0000000h				
Access:	R/W				
Size (in bits):	32				



Bit				Description				
31	Enable_F	rame_Buffer_Com	pressio	on				
	Project:	All						
	Default Va	lue: 0b						
	This bit is	used to globally en	able DF	PFC function at the next Vertical Blank start.				
	[ILK, Work	around to allow C	<sr afte<="" td=""><td>r Frame Buffer Compression is disabled:</td><td></td><td></td></sr>	r Frame Buffer Compression is disabled:				
	• F							
	• E	Enable primary plar	ne on the	e selected pipe if it is not already enabled				
		Program Pipe Main Is	Waterm	nark for the selected pipe (WM0_PIPE_A or V	VM0_Pip	be_B) to all		
	• V	Vait for vertical blar	nk on th	e selected pipe				
	• [Disable frame buffe	r compr	ession				
	Restore Pipe Main Watermark							
	Wait for vertical blank on the selected pipe							
	• F	Restore primary pla	ne					
	Value	Name		Description		Project		
	0b	Disable		Disable frame buffer compression				
	1b	Enable		Enable frame buffer compression		All		
30	Plane_Se	lect						
	Project:	All						
	Default Va	lue: 0b						
	Value	Name	De	scription	Projec	ct		
	0b	Plane A	Pla	Plane A All				
	1b	Plane B	Pla	ne B	All			
29	CPU_Fen	ce_Enable						
	Project:	All						
	Default Va	lue: 0b						
	Value	Name	De	scription		Project		
			D .			All		
	0b	No CPU Disp Buf		play Buffer is not in a CPU fence. No modifie allowed from CPU to the Display Buffer	cations	All		



		DPF	C_CONT	ROL— DPFC Control		
27	CS_SYN	C_FLIP_NUKE_Dis	sable			
	Project:	All				
	Default V	alue: 0b	1			
	Setting th	is bit will disable the	e command s	streamer SYNC Flips from resetting the	DPFC.	
	Value	Name		Description	Project	
	0b	Enable		Enable the CS SYNC Flip Nuke	All	
	1b	Disable		Disable the CS SYNC Flip Nuke	All	
26		YNC_FLIP_Nuke_D	Jisable			
26	Project:	YNC_FLIP_NUKE_L All				
26	_	All				
26	Project: Default V	All alue: 0b		c Flip from resetting the DPFC.		
26	Project: Default V	All alue: 0b		c Flip from resetting the DPFC.	Project	
26	Project: Default V Setting th	All alue: Ob his bit will disable the			Project	
26	Project: Default V Setting th	All alue: 0b nis bit will disable the Name		Description		
26	Project: Default V Setting th Value 0b	All alue: 0b his bit will disable the Name Enable Disable		Description Enable the MMIO Sync Flip Nuke	All	
	Project: Default V Setting th Value 0b 1b	All alue: 0b his bit will disable the Name Enable Disable	e MMIO Syn	Description Enable the MMIO Sync Flip Nuke	All	
	Project: Default V Setting th Value Ob 1b Persister	All alue: 0b his bit will disable the Name Enable Disable ht_Mode All	e MMIO Syn	Description Enable the MMIO Sync Flip Nuke	All	
	Project: Default V Setting the Value Ob 1b Persister Project:	All alue: 0b his bit will disable the Name Enable Disable ht_Mode All	e MMIO Syn	Description Enable the MMIO Sync Flip Nuke Disable the MMIO Sync Flip Nuke	All	Project
	Project: Default V Setting th Ob 1b Persister Project: Default V	All alue: 0b his bit will disable the bisable Disable ht_Mode All alue: 0b	e MMIO Syn	Description Enable the MMIO Sync Flip Nuke Disable the MMIO Sync Flip Nuke	All	Project All



			DPFC_	CO	NTROL— DPFC Control	
24:16	Compres	ssion_Co	ntrol(testmo	ode)		
	Project:		All			
	Security:		Test			
	Default V		0b			
	Setting th	ne bits in t	his register d	isable	es certain compression capabilities.	
	Value		Name	De	scription	Project
	1XXXX	XXXXb	Disable		n length without 1 nibble ([ILK] this setting not allowed)	All
	0XXXX	XXXXb	Enable	Ru	n length with 1 nibble	All
	X1XXX	XXXXb	Disable		n length without 2 nibble ILK] this setting is allowed)	All
	XOXXXX	XXXXb	Enable	Ru	n length with 2 nibble	All
	XX1XX	XXXXb	Disable	Мс	no Palette Disabled	All
	XX0XXX	XXXXb	Enable	Мс	no Palette Enabled	All
	XXX1XX	XXXXb	Disable	His	torical Palette Disabled	All
	XXX0XX	XXXXb	Enable	His	torical Palette Enabled	All
	XXXX1	XXXXb	Disable	De	Ita 6 Disabled	All
	XXXX0	XXXXb	Enable	De	Ita 6 Enabled	All
	XXXXX	1XXXb	Disable	De	Ita 5 Disabled	All
	XXXXX	0XXXb	Enable	De	Ita 5 Enabled	All
	XXXXX	X1XXb	Disable	De	lta 4 Disabled	All
	XXXXX	X0XXb	Enable	De	lta 4 Enabled	All
	XXXXXX	XX1Xb	Disable	De	Ita 3 Disabled	All
	XXXXX	XX0Xb	Enable	De	Ita 3 Enabled	All
	XXXXX	XXX1b	Disable	De	lta 2 Disabled	All
	XXXXX	XXX0b	Enable	De	lta 2 Enabled	All
15	SLB_Init	ialization	_Flush_Disa	able_	Control(testmode)	
	Project:		All			
	Security:		Test			
	Default V		0b			
	Setting th	nis bit will	disable the S	LB flu	ush mechanism for the first frame DPFC is o	on.
	Value	Name			Description	Project
	0b	Enable			Enable the SLB initialization flush	All
	1b	Disable	l		Disable SLB initialization flush	All
14:8	Reserved	d Pr	oject: All		Form	at: MBZ



7:6	Compres	ssion_Limit				
	Project:		All			
	Default Value: 0					
		ster sets a mir sed buffer.	nimum lin	it on compression. It is also use	ed to determine the size of the	
		pression		Pixel Fo	ormat	
	F	Ratio		16 bpp	32 bpp	
	1		Not Sup	ported	Supported (CFB=FB)	
	1/2		Supporte	ed (CFB=FB)	Supported (CFB=1/2 FB)	
	1⁄4		Supporte	ed (CFB=1/2FB)	Supported (CFB=1/4 FB)	
	FB = Fra	me Buffer Siz	е			
	CFB = Co	ompressed Fra	ame Buff	er Size		
	Value	Name	Desc	ription		Projec
	00b	1:1 1		:1 compression, compressed buffer is the same size as the ncompressed buffer		
	01b	2:1		ompression, compressed buffer is one half the size of the mpressed buffer.		
	10b 4:1		4:1 compression, compressed buffer is one quarter the size of the uncompressed buffer.			All
	11b	Reserved	Rese	rved		All
5:4	Write_Ba	ack_Waterma	rk			
	Project:		All			
	Default V	alue:	0b			
				gine waits for this amount of data Compression SR mode must be		
	Value	Name		Description	Project	
	00b	4 cache li	nes	4 cache lines	All	
	01b	8 cache li	nes	8 cache lines	All	
				Reserved	All	
	1Xb	Reserved				
3:0	1Xb	Reserved				
3:0	1Xb					
3:0	1Xb CPU_Fe	nce_Number				



2.4.3 DPFC_RECOMP_CTL — DPFC ReComp Control

		DPFC_RE	COMP_CTL — D	PFC ReComp	Control	
Register T Address C Project: Default Va Access: Size (in bit	All Iue: 000 R/W	0Ch 00000h				
Bit			Des	scription		
31:28	Reserved			Project:	All Format:	MBZ
	Project: Default Va	ReComp_Stall Al alue: 0b	-			Project
	0b	Disable	Disable			All
	1b	Enable	Enable			All
26:16	If this mar		ion_Watermark dations occur in one fran recomp timer.	Project: ne, stop compressi	All on until the numb	er falls below
15:6	Reserved	Project:	All		Format:	MBZ
5:0	After inva		Count ow watermark, wait this r ession on the following fra	-	All e restarting the co	ompressor.



2.4.4 DPFC_CPU_Fence_Offset — Y Offset CPU Fence Base to Display Buffer Base

Register Typ Address Offs Project: Default Value Access: Size (in bits)	set: 43218h All e: 00000000h R/W	
	of this register can not be changed while compression is enabled.	
Bit	Description	
31:22 F	Reserved Project: All	Format: MBZ
	Yfence_disp Y offset from the CPU fence to the Display Buffer base. DevSNB] The CPU fence is always programmed to match the Disp be programmed to 0 to match.	Project: All alay Buffer base, so this offset must



2.5 Interrupt Control Registers

2.5.1 Display Engine Interrupt Registers Bit Definition

	Display Engine Interrupt Re	egisters Bit Definition
Project: Size (in bit	All s): 32	
explicitly list the CPU in		GTIIR and PMIIR are ORed together to generate
Bit		cription
31	Master_Interrupt_Control	Project: All Format:
	This bit exists only in the DEIER Display Engine In	terrupt Enable Register.
	This is the master control for the Display to CPU in to propagate to the system.	terrupt. This bit must be set to 1 for any interrupts
30	Reserved Project: All	Format:
29	Sprite_Plane_B_flip_done	Project: All Format:
	This is an active high pulse when a sprite plane B f	ílip is done.
28	Sprite_Plane_A_flip_done	Project: All Format:
	This is an active high pulse when a sprite plane A f	ílip is done.
27	Primary_Plane_B_flip_done	Project: All Format:
	This is an active high pulse when a primary plane E	3 flip is done.
26	Primary_Plane_A_flip_done	Project: All Format:
	This is an active high pulse when a primary plane A	A flip is done.
25	PCU_event [DevILK]:	Project: DevILK Format:
	This is an active high pulse when a thermal or rend and status should be checked in RGVINTRSTS (M event comes display directly on a wire.	ler geyserville event has occured. Interrupt source ICHBAR+1184h) and TIS1 (MCHBAR+101Eh). This
25	Reserved Project: DevSNB	Format:
24	GTT_fault	Project: All Format:
	This is an active high level while either of the GTT	Fault Status register bits are set.
23	Poison	Project: All Format:
	This is an active high pulse on receiving the poison	n message.
22	Performance_counter	Project: All Format:
	This is an active high pulse when the performance the Performance Counter Source register.	counter reaches the threshold value programmed in



21	PCH_Display_interrupt_event	Project:	All	Format:	
	This is an active high level while there is an interrupt bein asserted until the interrupts in the PCH Display are all cle interrupt will cause the IIR to be set here, so all PCH Dis interrupts, must be cleared before a new PCH Display In	eared. Onl play Interru	ly the upts,	rising edge of the PCH Displain including back to back	
20	AUX_Channel_A	Project:	All	Format:	
	This is an active high pulse on the AUX A done event.				
18	GSE Project	ct: DevS	SNB	Format:	
	This is an active high pulse on the GSE system level even	ent.			
17	DPST_histogram_event	Project:	All	Format:	
	This is an active high pulse on the DPST histogram ever	nt.			
16	DPST_phase_in_event	Project:	All	Format:	
	This is an active high pulse on the DPST phase in event.				
15	Pipe_B_vblank	Project:	All	Format:	
	This is an active high level for the duration of the Pipe B	vertical bla	ank.		
14	Pipe_B_even_field	Project:	All	Format:	
	This is an active high level for the duration of the Pipe B		even	field.	
13	Pipe_B_odd_field	Project:	All	Format:	
	This is an active high level for the duration of the Pipe B interlaced odd field.				
12	Pipe_B_line_compare	Project:	All	Format:	
	This is an active high level for the duration of the selecte	d Pipe B s	can li	nes.	
11	Pipe_B_vsync	Project:	All	Format:	
	This is an active high level for the duration of the Pipe B vertical sync.				
10	Pipe_B_CRC_done	Project:	All	Format:	
	This is an active high pulse on the Pipe B CRC done.				
9	Pipe_B_CRC_error	Project:	All	Format:	
	This is an active high pulse on the Pipe B CRC error.				
8	Pipe_B_FIFO_underrun	Project:	All	Format:	
	This is an active high level for the duration of the Pipe B	FIFO unde	errun.		
7	Pipe_A_vblank	Project:	All	Format:	
	This is an active high level for the duration of the Pipe A	vertical bla	ank.		
6	Pipe_A_even_field	Project:	All	Format:	
	This is an active high level for the duration of the Pipe A				
5	Pipe_A_odd_field	Project:	All	Format:	
	This is an active high level for the duration of the Pipe A	-			
4	Pipe_A_line_compare	Project:		Format:	



	Display Engine Interrupt Regi	sters Bit	Def	finition
3	Pipe_A_vsync This is an active high level for the duration of the Pipe A	Project: A vertical sy		Format:
2	Pipe_A_CRC_done This is an active high pulse on the Pipe A CRC done.	Project:	All	Format:
1	Pipe_A_CRC_error This is an active high pulse on the Pipe A CRC error.	Project:	All	Format:
0	Pipe_A_FIFO_underrun This is an active high level for the duration of the Pipe A	Project: A FIFO unde		Format:

2.5.2 DEISR — Display Engine Interrupt Status Register

		DEISR — Display	Engine Interrupt Status Register		
Register Ty	ype: MN	110			
Address O	ffset: 44()00h			
Project:	All				
Default Val	ue: 000	00000h			
Access:	Re	ad Only			
Size (in bit	s): 32				
of these int	errupt cor	nditions are reported in th	value of all interrupt status bits. The IMR register ne persistent IIR (i.e., set bits must be cleared by s IIR bits to cause CPU interrupts.		
Bit		Description			
31:0	Display_	Engine_Interrupt_Status_	Bits		
	Project:	All			
	Format:	Display Engine Interrupt R	egisters Bit Definition See Description	on Above	
	This field	contains the non-persistent	t values of all interrupt status bits.		
	Value	Name	Description	Project	
	0b	Condition Doesn't exist	Interrupt Condition currently does not exist	All	
	1b	Condition Exists	Interrupt Condition currently exists	All	
	Programming Notes				
		nputs to this register are sho le these conditions.	ort pulses; therefore software should not expect to use t	his register	



2.5.3 DEIMR — Display Engine Interrupt Mask Register

DEIMR — Display Engine Interrupt Mask Register					
Register Ty	ype: MM	IIO			
Address Offset: 44004h					
Project:	All				
Default Val	lue: FFF	FFFFFh			
Access:	R/V	V			
Size (in bit	s): 32				
"unmasked in the IIR u generate C	l". "Unmas ntil cleare	sked" bits will be rep d by software. "Mas	control which Interrupt Status Register b ported in the IIR, possibly triggering a CF ked" bits will not be reported in the IIR a	PU interrupt, and will persist	
Bit		Description			
31:0	Display_	Engine_Interrupt_Ma	sk_Bits		
	Project:	All			
	Format:	Display Engine Interru	upt Registers Bit Definition	See Description Above	
	This field	contains a bit mask w	hich selects which interrupt bits from the ISR	are reported in the IIR.	
Value Name Description Project			Project		
	0b	Not Masked	Not Masked – will be reported in the IIR	All	
	1b	Masked	Masked – will not be reported in the IIR	All	



2.5.4 DEIIR — Display Engine Interrupt Identity Register

		DEIIR — Display B	Engine Interrupt Identity Register	
Register T	ype: MN	/IO		
Address C	Offset: 440	008h		
Project:	All			
Default Va	lue: 000	00000h		
Access:	R/\	N Clear		
Size (in bit	<u> </u>		at are "unmasked" by the IMR and thus can genera	
nterrogate	ed to deter		CPU interrupt is generated, this should be the first renterrupt. Writing a '1' into the appropriate bit po	
Bit			Description	
31:0	Display_	Engine_Interrupt_Identity	y_Bits	
51.0	Project:	All		
	Format:	Display Engine Inte	errupt Registers Bit Definition See Description	on Above
	Format: This field IMR. If e register v the appro	holds the persistent values enabled by the IER, bits set vill remain set (persist) unti opriate bit(s)	s of the interrupt bits from the ISR which are "unmasked" in this register will generate a CPU interrupt. Bits set in I the interrupt condition is "cleared" via software by writin	by the this g a '1' to
	Format: This field IMR. If e register v the appro	holds the persistent values enabled by the IER, bits set vill remain set (persist) unti opriate bit(s)	s of the interrupt bits from the ISR which are "unmasked" in this register will generate a CPU interrupt. Bits set in	by the this g a '1' to
	Format: This field IMR. If e register v the appro	holds the persistent values enabled by the IER, bits set vill remain set (persist) unti opriate bit(s) bit, the IIR can store a sec	s of the interrupt bits from the ISR which are "unmasked" in this register will generate a CPU interrupt. Bits set in I the interrupt condition is "cleared" via software by writin cond pending interrupt if two or more of the same interrup	by the this g a '1' to t



2.5.5 DEIER — Display Engine Interrupt Enable Register

DEIER — Display Engine Interrupt Enable Register				
Register Ty	ype: MMIC	C		
Address O	ffset: 4400	Ch		
Project:	All			
Default Val	ue: 0000	0000h		
Access:	R/W			
Size (in bit	s): 32			
	•		able bit for each interrupt bit in the IIR register. A disa gister to allow polling of interrupt sources.	bled interrupt
Bit			Description	
31:0	Display_E	ngine_Interrupt_Ena	ble_Bits	
	Project:	All		
	Format:	Display Engine	Interrupt Registers Bit Definition See Descripti	on Above
	Interrupt Id		CPU interrupt to be generated whenever the correspondin nes set. The DEIER master interrupt control bit must be set stem.	
	Value	Name	Description	Project
	0b	Disable	Disable	All
	1b	Enable	Enable	All



2.5.6 GT Interrupt Registers Bit Definition

	GT Interrupt Registers Bit Definition	
Project: Size (in bi	All (ts): 32	
GT interrup The DEIIR	pt bits come to display either directly on wires [DevILK] or through interrupt message 0x50200 [DevSN and GTIIR and PMIIR are ORed together to generate the CPU interrupt.	IB]
The GT Int	terrupt Control Registers all share the same bit definition from this table.	
Bit	Description	
31:10	Reserved Project: DevILK Format:	
9	Bit_Stream_Pipeline_Counter_Exceeded_Notify_Interrupt	
	Project: DevILK	
	The counter threshold for the execution of the Bit Stream Pipeline is exceeded. Driver needs to attempt hang recovery.	
7	Page_Fault	
	Project: DevILK	
	This bit is set whenever there is a pending PPGTT (page or directory) fault.	
6	Media_Decode_Pipeline_Counter_Exceeded_Notify_Interrupt	
	Project: DevILK	
	The counter threshold for the execution of the media pipeline is exceeded. Driver needs to attempt hang recovery.	
5	Video_Decode_Command_Parser_User_Interrupt	
	Project: DevILK	
	This status bit is set when an MI_USER_INTERRUPT instruction is executed on the Media Decode Command Parser. Note that instruction execution is not halted and proceeds normally. A mechanis such as an MI_STORE_DATA instruction is required to associate a particular meaning to a user interrupt.	
4	PIPE_CONTROL_Notify_Interrupt	
	Project: DevILK	
	The Pipe Control packet (Fences) specified in <i>3D pipeline</i> document may optionally generate an Interrupt. The Store QW associated with a fence is completed ahead of the MSI. This ordering is n guaranteed if PCI Line Intr# mechanism is used.	ot



	GT Interrupt Registers	Bit Definition
3	Render_Command_Parser_Master_Error	
	Project: DevILK	
	When this status bit is set, it indicates that the hardwa upon an error condition and cleared by a CPU write of Error ID register followed by a write of a one to this bit the error comes from the "Error Status Register" whic which error conditions will cause the error status bit to	If a one to the appropriate bit contained in the tin the IIR. Further information on the source of the along with the "Error Mask Register" determine
	Page Table Error: Indicates a page table error.	
	Instruction Parser Error: The Renderer Instruction F instruction.	Parser encounters an error while parsing an
2	Sync_Status	
	Project: DevILK	
	This bit is toggled when the Instruction Parser comple INSTPM register. The toggle event will happen after a Status DWord write resulting from this toggle will caus coherent as well (flush and invalidate the render cach	all the graphics engines are flushed. The HW se the CPU's view of graphics memory to be
0	Render_Command_Parser_User_Interrupt	
	Project: DevILK	
	This status bit is set when an MI_USER_INTERRUPT Parser. Note that instruction execution is not halted at MI_STORE_DATA instruction is required to associate	nd proceeds normally. A mechanism such as an
31:0	Reserved	
31	Reserved Project: DevSNB	Format:
29	Blitter_page_directory_faults	
	Project: DevSNB	
	This is a write of logic1 via interrupt message from GT	via 0x50200 bit29
28:27	Reserved Project: DevSNB	Format:
26	Blitter_MI_FLUSH_DW_notify	
	Project: DevSNB	
	This is a write of logic1 via interrupt message from GT	via 0x50200 bit26
25	Blitter_Command_Streamer_error_interrupt	
	Project: DevSNB	
	This is a write of logic1 via interrupt message from GT	via 0x50200 bit25
24	Billter_MMIO_sync_flush_status	
	Project: DevSNB	
	This is a write of logic1 via interrupt message from GT	via 0x50200 bit24
23	Reserved Project: DevSNB	Format:
22	Blitter_Command_Streamer_MI_USER_INTERRUPT Project: DevSNB	г
	This is a write of logic1 via interrupt message from GT	via 0x50200 hit22



	GT Interrupt Registers Bit Definition	1	
21	Reserved Project: DevSNB	Format:	
19	Video_page_directory_faultsProject:DevSNBThis is a write of logic1 via interrupt message from GT via 0x50200 bit19		
18	Video_Command_Streamer_Watchdog_counter_exceeded Project: DevSNB This is a write of logic1 via interrupt message from GT via 0x50200 bit18		
17	Reserved Project: DevSNB	Format: MBZ	
16	Video_MI_FLUSH_DW_notify Project: DevSNB This is a write of logic1 via interrupt message from GT via 0x50200 bit16 Video_Command_Streamer_error_interrupt		
15	Video_Command_Streamer_error_interrupt Project: DevSNB This is a write of logic1 via interrupt message from GT via 0x50200 bit15		
14	Video_MMIO_sync_flush_statusProject:DevSNBThis is a write of logic1 via interrupt message from GT via 0x50200 bit14		
13	Reserved Project: DevSNB	Format:	
12	Video_Command_Streamer_MI_USER_INTERRUPT Project: DevSNB This is a write of logic1 via interrupt message from GT via 0x50200 bit12		
1:9	Reserved Project: DevSNB	Format:	
7	Render_page_directory_faults Project: DevSNB This is a write of logic1 via interrupt message from GT via 0x50200 bit7		
6	Render_Command_Streamer_Watchdog_counter_exceeded Project: DevSNB This is a write of logic1 via interrupt message from GT via 0x50200 bit6		
5	Reserved Project: DevSNB	Format:	_
4	Render_PIPE_CONTROL_notify Project: DevSNB This is a write of logic1 via interrupt message from GT via 0x50200 bit4		
3	Render_Command_Streamer_error_interrupt Project: DevSNB This is a write of logic1 via interrupt message from GT via 0x50200 bit3.		
2	Render_MMIO_sync_flush_status Project: DevSNB		_



	GT Interrupt Registers Bit Definition
	This is a write of logic1 via interrupt message from GT via 0x50200 bit2
0	Render_Command_Streamer_MI_USER_INTERRUPT
	Project: DevSNB
	This is a write of logic1 via interrupt message from GT via 0x50200 bit0



2.5.7 GTISR — GT Interrupt Status Register

		GTISR — GT	Γ Interrupt Status Register				
Register Ty	ype: MN	110					
Address O	ffset: 440)10h					
Project:	All						
Default Val							
Access:	Read Only						
Size (in bit							
			value of all interrupt status bits. The IMR registe				
			e persistent IIR (i.e., set bits must be cleared by	software).			
Bits in the I	ER are us	sed to selectively enable	IIR bits to cause CPU interrupts.				
Bit		Description					
31:0	GT_Inter	_Interrupt_Status_Bits					
	Project:	All					
	Format:	GT Interru	pt Registers Bit Definition See Description	n Above			
	This field	contains the non-persistent	values of all interrupt status bits.				
	Value	Name	Description	Project			
	0b	Condition Doesn't Exist	Interrupt Condition currently does not exist	All			
	1b	Condition Exists	Interrupt Condition currently exists	All			
	Progra	mming Notes					
		nputs to this register are sho le these conditions.	ort pulses; therefore software should not expect to use	this register			

2.5.8 **GTIMR — GT Interrupt Mask Register**

	GTIMR — GT Interrupt Mask Register
Register Type:	MMIO
Address Offset:	44014h
Project:	All
Default Value:	FFFFFFh
Access:	R/W
Size (in bits):	32
•	is used by software to control which Interrupt Status Register bits are "masked" or
	nmasked" bits will be reported in the IIR, possibly triggering a CPU interrupt, and will persist eared by software. "Masked" bits will not be reported in the IIR and therefore cannot terrupts.
Eor command st	reamer interrupts DO NOT use this register to mask interrupt events. Instead use the

For command streamer interrupts DO NOT use this register to mask interrupt events. Instead use the individual command streamer MASK bits.



Bit			Description	
31:0	GT_Inter	rupt_Mask_Bits	5	
	Project:		All	
	Format:		GT Interrupt Registers Bit Definition	See Description Above
			Of interrupt registere bit benintion	Dee Description Above
	This field	contains a bit m	hask which selects which interrupt bits fi	1
	This field	contains a bit m		1
		1	hask which selects which interrupt bits fr	om the ISR are reported in the III Project

2.5.9 GTIIR — GT Interrupt Identity Register

		GTIIR — GT II	nterrupt Identity Register				
Register Ty	ype: MI	ЛЮ					
Address O	ffset: 44	018h					
Project:	All						
Default Val							
Access:	R/W Clear						
Size (in bit	/						
interrupts (interrogate	if enableo d to detei	I via the IER). When a CPI	are "unmasked" by the IMR and thus can generate U interrupt is generated, this should be the first re- rrupt. Writing a '1' into the appropriate bit pos	gister to be			
Bit		Description					
31:0	GT_Inte	rrupt_Identity_Bits					
	Project:	All					
	Format:	GT Interrupt	t Registers Bit Definition See Description Al	oove			
	IMR. If register	enabled by the IER, bits set in	of the interrupt bits from the ISR which are "unmasked" this register will generate a CPU interrupt. Bits set in t ne interrupt condition is "cleared" via software by writing	his			
	Value	Name	Description	Project			
	0b	Condition Not Detected	Interrupt Condition Not Detected	All			
	1b	Condition Detected	Interrupt Condition Detected (may or may not have actually generated a CPU interrupt)	All			



2.5.10 GTIER — GT Interrupt Enable Register

		GTIER —	GT Interrupt Enable Register	,			
Register Ty	pe: MMIC)					
Address Of	fset: 4401	Ch					
Project:	All						
Default Val	fault Value: 00000000h						
Access:	R/W						
Size (in bits	ts): 32						
	The IER register contains an interrupt enable bit for each interrupt bit in the IIR register. A disabled interrupt will still appear in the Interrupt Identity Register to allow polling of interrupt sources.						
Bit		Description					
31:0	GT_Interru	pt_Enable_Bits					
	Project:	All					
	Format:	GT Int	terrupt Registers Bit Definition	See Description	n Above		
	The bits in this register enable a CPU interrupt to be generated whenever the corresponding bit in the Interrupt Identity Register becomes set. The DEIER master interrupt control bit must be set to 1 for any interrupts to propagate to the system.						
	Value	Name	Description		Project		
	0b	Disable	Disable		All		
	1b	Enable	Enable		All		
		1					



2.5.11 Power Management Interrupt Registers Bit Definition [DevSNB]

	Power Management Interrupt Registers Bit I	efinition	[De\	/SNB]
Project: Size(in bits	DevSNB 32			
GTIIR and	agement interrupt bits come to display through interrupt me PMIIR are ORed together to generate the CPU interrupt. Management Interrupt Control Registers all share the same	0		
Bit	Description			
31:26	Reserved Project: All	Format:		
25	PCU_pcode2driver_mailbox_event This is a write of logic1 via interrupt message from PCU via 0x50	Project: 210 bit25	All	Format:
24	PCU_Thermal_Event This is a write of logic1 via interrupt message from PCU via 0x50	Project: 210 bit24	All	Format:
23:7	Reserved Project: All	For	mat:	
6	Render_Frequency_Downward_Timeout_During_RC6_interr This is a write of logic1 via interrupt message from GT via 0x502	• •		All Format:
5	RP_UP_threshold_interrupt This is a write of logic1 via interrupt message from GT via 0x502	Project: 10 bit5	All	Format:
4	RP_DOWN_threshold_interrupt This is a write of logic1 via interrupt message from GT via 0x502	Project: 10 bit4	All	Format:
3	Reserved Project: All	For	mat:	
2	Render_geyserville_UP_evaluation_interval_interrupt This is a write of logic1 via interrupt message from GT via 0x502	Project: 10 bit2	All	Format:
1	Render_geyserville_Down_evaluation_interval_interrupt BitFieldDesc	Project:	All	Format:
0	Reserved Project: All	For	mat:	MBZ



Register T	vpe: MMI	0					
-	ffset: 4402	20h					
Project:	Dev	SNB					
Default Va	lue: 0000	0000h					
Access:	Rea	d Only					
Size (in bit	s): 32						
Bits in the			I in the persistent IIR (i.e., set bits must be clear able IIR bits to cause CPU interrupts.	ed by software).			
Bit			Description				
31:0	Power_Ma	Power_Management_Interrupt_Status_Bits					
		Project: All					
	Project:	All					
	, ,			scription Above			
	Format:	Power Management I		scription Above			
	Format:	Power Management I	Interrupt Registers Bit Definition See Des	scription Above			
	Format: I This field o	Power Management I contains the non-pers	Interrupt Registers Bit Definition See Des sistent values of all interrupt status bits.				
	Format: I This field o	Power Management I contains the non-pers Name Condition Does	Interrupt Registers Bit Definition See Des sistent values of all interrupt status bits.	Project			
	Format: I This field o Value 0b 1b	Power Management I contains the non-pers Name Condition Does Not Exist	Interrupt Registers Bit Definition See Description See Description Interrupt status bits.	Project			

2.5.12 PMISR — PM Interrupt Status Register

2.5.13 PMIMR — Power Management Interrupt Mask Register

	PMIMR — Power Management Interrupt Mask Register
Register Type:	MMIO
Address Offset:	44024h
Project:	DevSNB
Default Value:	FFFFFFh
Access:	R/W
Size (in bits):	32

"unmasked". "Unmasked" bits will be reported in the IIR, possibly triggering a CPU interrupt, and will persist in the IIR until cleared by software. "Masked" bits will not be reported in the IIR and therefore cannot generate CPU interrupts. For power management interrupts DO NOT use this register to mask interrupt events. Instead use the

individual power management MASK bits in the corresponding PMunit register space.



Bit			Description					
1:0	Power_Ma	anagement_Interru	upt_Mask_Bits					
	Project: /	Project: All						
	Format: Power Management Interrupt Registers Bit Definition See Description Abc							
	Format:	Power Managemen	nt Interrupt Registers Bit Definition See De	escription Above				
			Interrupt Registers Bit Definition See Definition which selects which interrupt bits from the ISR are residued and the ISR are residued and the ISR and the ISR are residued and the ISR and the ISR are residued and t	•				
				•				
	This field o	contains a bit mask	which selects which interrupt bits from the ISR are re	ported in the IIR.				

2.5.14 PMIR — Power Management Interrupt Identity Register

	Р	MIIR — Powe	er Management Interrupt Identity Register				
Register T	ype: MN	110					
Address C) ffset: 440)28h					
Project:	Dev	vSNB					
Default Va	lue: 000)00000h					
Access:	R/V	R/W Clear					
Size (in bit	t s): 32						
nterrupts (nterrogate	(if enabled ed to deter	via the IER). W	t bits that are "unmasked" by the IMR and thus can gen /hen a CPU interrupt is generated, this should be the firs of the interrupt. Writing a '1' into the appropriate bit	st register to be			
Bit			Description				
31:0	Power_N	lanagement_Inte	rrupt_Identity_Bits				
	Project:	All					
	Format:	Power Managem	ent Interrupt Registers Bit Definition See Descript	ion Above			
	IMR. If e register v	This field holds the persistent values of the interrupt bits from the ISR which are "unmasked" by the IMR. If enabled by the IER, bits set in this register will generate a CPU interrupt. Bits set in this register will remain set (persist) until the interrupt condition is "cleared" via software by writing a '1' to the appropriate bit(s).					
	condition	s occur before the	ore a second pending interrupt if two or more of the same inte first condition is cleared. Upon clearing the interrupt, the IIR eturn high to indicate there is another interrupt pending.				
	Value	Name	Description	Project			
	0b	IC No Detect	Interrupt Condition Not Detected	All			
	1b	IC Detect	Interrupt Condition Detected (may or may not have actually generated a CPU interrupt)	All			



2.5.15 PMIER — Power Management Interrupt Enable Register

	Р	IIER — Pow	er Management Interrupt Ena	able Register			
Register T	ype: MM	0					
Address O	ffset: 440	2Ch					
Project:	Dev	SNB					
Default Va	lue: 000						
Access:	R/W	R/W					
Size (in bit	s): 32): 32					
	The IER register contains an interrupt enable bit for each interrupt bit in the IIR register. A disabled interrupt will still appear in the Interrupt Identity Register to allow polling of interrupt sources.						
Bit			Description				
31:0	Power Ma	nagement Interr	rupt Enable Bits				
	Project:	All					
	Format:	Power Manageme	ent Interrupt Registers Bit Definition	See Description Above			
	The bits in this register enable a CPU interrupt to be generated whenever the corresponding bit in the Interrupt Identity Register becomes set. The DEIER master interrupt control bit must be set to 1 for any interrupts to propagate to the system.						
	Value	Name	Description	Project			
	0b	Disable	Disable	All			

2.5.16 Port Hot Plug Control Register

			Digi	tal Por	Hot Plug Control Register
Register Ty	-	MMIO			
Address Of Project:	TSet:	44030h All	1		
Default Valu	ue:	000000	00h		
Access: Size (in bits	5):	R/W 32			
Bit					Description
31:5	Rese	rved	Project:	All	Format:



4	Digital_P	ort_A_Hot	_Plug_Det	ect_Input_E	Enable		
	Project:		All	-			
	Default V	alue:	0b				
		the state of abled or no		uffer for the o	digital port. The buffer st	ate is independent of whet	her the
	Value	Name	Descript	ion			Proje
	0b	Disable	Buffer dis	sabled			All
	1b	Enable	Buffer en	abled. Hot p	olugs bit reflect the elect	rical state of the HPD pin	All
	Project: Default V These bit		All 0b e duration o	f the pulse d	lefined as a short pulse.		
	Value	Name		Descrip	otion	Project	
	00b	2ms		2 ms		All	
	01b	4.5ms		4.5 ms	4.5 ms All		
	10b	6ms		6 ms		All	
	11b	100ms		100 ms		All	
1:0	Project: Access: Default V This refle or for noti set. Thes	alue: cts hot plug fication of a	All R/W 0b g detect stat a sink event DRed togetl	tus on the dig t. When eith	gital port. This bit is use er a long or short pulse	d for either monitor hotplu is detected, one of these b gister bit. These are sticky	its will
	Value	Name		Descrip	otion	P	roject
	00b	Not De	tected	Digital p	oort hot plug event not d	etected A	II
	1Xb	Long P	ulse	Digital p	oort long pulse hot plug	event detected A	II
				1			



2.5.17 GTT Fault Status Register

		GTT F	ault Status Register	
Register Address Project: Default V Access: Bize (in b	Offset: 4404 All alue: 0000 R/W	-		
Bit			Description	
31:8	Reserved	Project: All	Forma	t:
7	Project: Default Va This is a st the main IS	icky bit, cleared by writing	g 1 to it. All the GTT Fault Status bits are ORe ent comes to display either directly on a wire	
	Value	Name	Description	Project
	0b	Not Detected	Event not detected	All
	1b	Detected	Event detected	All
		ige_table_entry_data		
	Project: Default Va This is a st the main IS 0x50220.	All lue: 0b ticky bit, cleared by writing SR GTT Fault bit. This ev This event comes to displ	g 1 to it. All the GTT Fault Status bits are OR ent comes to display either directly on a wire ay either directly on a wire ILK] or through me	or through message
	Project: Default Va This is a st the main IS 0x50220. [DevSNB].	All lue: 0b ticky bit, cleared by writing SR GTT Fault bit. This ev This event comes to displ	ent comes to display either directly on a wire ay either directly on a wire ILK] or through me	or through message essage 0x50220 bit 0
	Project: Default Va This is a st the main IS 0x50220. [DevSNB]. Value	All lue: 0b licky bit, cleared by writing SR GTT Fault bit. This ev This event comes to displ Name	ent comes to display either directly on a wire ay either directly on a wire ILK] or through me Description	or through message essage 0x50220 bit 0 Project
	Project: Default Va This is a st the main IS 0x50220. [DevSNB].	All lue: 0b ticky bit, cleared by writing SR GTT Fault bit. This ev This event comes to displ	ent comes to display either directly on a wire ay either directly on a wire ILK] or through me	or through message essage 0x50220 bit 0
5	Project: Default Va This is a st the main IS 0x50220. [DevSNB]. Value 0b 1b Cursor_B Project: Default Va This reflec	All lue: 0b ticky bit, cleared by writing SR GTT Fault bit. This ev This event comes to displ Name Not Detected Detected GTT_Fault_Status All lue: 0b ts GTT fault status for this	ent comes to display either directly on a wire ay either directly on a wire ILK] or through me Description Event not detected	or through message essage 0x50220 bit 0 Project All All
5	Project: Default Va This is a st the main IS 0x50220. [DevSNB]. Value 0b 1b Cursor_B Project: Default Va This reflec	All lue: 0b ticky bit, cleared by writing SR GTT Fault bit. This ev This event comes to displ Name Not Detected Detected GTT_Fault_Status All lue: 0b ts GTT fault status for this	ent comes to display either directly on a wire ay either directly on a wire ILK] or through me Description Event not detected Event detected	or through message essage 0x50220 bit 0 Project All All
5	Project: Default Va This is a st the main IS 0x50220. [DevSNB]. Value 0b 1b Cursor_B Project: Default Va This reflec Fault Statu	All lue: 0b iticky bit, cleared by writing SR GTT Fault bit. This ev This event comes to displ Name Not Detected Detected GTT_Fault_Status All lue: 0b ts GTT fault status for this is bits are ORed together	ent comes to display either directly on a wire ay either directly on a wire ILK] or through me Description Event not detected Event detected a plane. This is a sticky bit, cleared by writing to go to the main ISR GTT Fault bit.	or through message essage 0x50220 bit 0 Project All All 1 to it. All the GTT



	Cursor A	_GTT_Fault_Status		
	Project:	All		
	Default Va			
	This reflec	ts GTT fault status for this pla	ane. This is a sticky bit, cleared by go to the main ISR GTT Fault bit.	writing 1 to it. All the GT
	Value	Name	Description	Project
	0b	Not Detected	Event not detected	All
	1b	Detected	Event detected	All
3	Sprite_B_	GTT_Fault_Status		
	Project:	All		
	Default Va	lue: 0b		
	This reflect Fault Statu	ts GTT fault status for this pla is bits are ORed together to g	ane. This is a sticky bit, cleared by go to the main ISR GTT Fault bit.	writing 1 to it. All the GT
	Value	Name	Description	Project
	0b	Not Detected	Event not detected	All
	1b	Detected	Event detected	All
2	Sprite_A_	GTT_Fault_Status		
2	Sprite_A_ Project:	GTT_Fault_Status		
2	-	All		
2	Project: Default Va This reflec	All lue: 0b ts GTT fault status for this pla	ane. This is a sticky bit, cleared by go to the main ISR GTT Fault bit.	I
2	Project: Default Va This reflec	All lue: 0b ts GTT fault status for this pla	ane. This is a sticky bit, cleared by go to the main ISR GTT Fault bit. Description	I
2	Project: Default Va This reflec Fault Statu	All lue: 0b ts GTT fault status for this pla is bits are ORed together to g	go to the main ISR GTT Fault bit.	writing 1 to it. All the GT
2	Project: Default Va This reflec Fault Statu	All lue: 0b ts GTT fault status for this pla is bits are ORed together to g	go to the main ISR GTT Fault bit. Description	writing 1 to it. All the GT
2	Project: Default Va This reflec Fault Statu Value 0b 1b	All lue: 0b ts GTT fault status for this pla is bits are ORed together to g Name Not Detected	go to the main ISR GTT Fault bit. Description Event not detected	writing 1 to it. All the GT Project All
	Project: Default Va This reflec Fault Statu Ob 1b Primary_E	All lue: 0b ts GTT fault status for this pla is bits are ORed together to g Name Not Detected Detected	go to the main ISR GTT Fault bit. Description Event not detected	writing 1 to it. All the GT Project All
	Project: Default Va This reflec Fault Statu Ob 1b Primary_E Project:	All lue: 0b ts GTT fault status for this pla ts bits are ORed together to g Name Not Detected Detected G_GTT_Fault_Status All	go to the main ISR GTT Fault bit. Description Event not detected	writing 1 to it. All the GT Project All
	Project: Default Va This reflec Fault Statu Ob 1b Primary_E Project: Default Va This reflec	All lue: 0b ts GTT fault status for this pla s bits are ORed together to g Name Not Detected Detected G-GTT_Fault_Status All lue: 0b ts GTT fault status for this pla	go to the main ISR GTT Fault bit. Description Event not detected	writing 1 to it. All the GT Project All All
	Project: Default Va This reflec Fault Statu Ob 1b Primary_E Project: Default Va This reflec	All lue: 0b ts GTT fault status for this pla s bits are ORed together to g Name Not Detected Detected G-GTT_Fault_Status All lue: 0b ts GTT fault status for this pla	go to the main ISR GTT Fault bit. Description Event not detected Event detected	writing 1 to it. All the GT Project All All
	Project: Default Va This reflect Fault Statu Ob 1b Primary_E Project: Default Va This reflect Fault Statu	All lue: 0b ts GTT fault status for this pla is bits are ORed together to g Name Not Detected Detected G_GTT_Fault_Status All lue: 0b ts GTT fault status for this pla is bits are ORed together to g	go to the main ISR GTT Fault bit.	writing 1 to it. All the GT Project All All writing 1 to it. All the GT



0	Primary_A	_GTT_Fau	Ilt_Status		
	Project:		All		
	Default Va	lue:	0b		
				ne. This is a sticky bit, cleared b o to the main ISR GTT Fault bit.	
	Fault Statu	is bits are C	DRed together to g	o to the main ISR GTT Fault bit.	

2.6 Display Engine Render Response

2.6.1 Display Engine Render Response Message Bit Definition

	Display Engine Render Response Mess	age Bit Def	initio	on	
Project:	DevSNB				
Size(in bits	;): 32				
	gine (DE) render response message bits come from event gine Render Response Message Registers all share the s				
Bit	Description				
31:14	Reserved Project: All			Format:	MBZ
13	Pipe_B_Start_of_Horizontal_Blank_Event	Project:	All	Format:	
	This even will be reported on the start of the Pipe B Horizontal	Blank.			
12	Reserved Project: All			Format:	MBZ
11	Pipe_B_Start_of_Vertical_Blank_Event	Project:	All	Format:	
	This even will be reported on the start of the Pipe B Vertical Bla	ank.			
10	Pipe_B_Sprite_Plane_Flip_Done_Event	Project:	All	Format:	
	This even will be reported on the completion of a flip for the Pip	e B Sprite Plan	e.		
9	Pipe_B_Primary_Plane_Flip_Done_Event	Project:	All	Format:	
	This even will be reported on the completion of a flip for the Pip	e B Primary Pla	ane.		
8	Pipe_B_Scanline_Event	Project:	All	Format:	
	This even will be reported on the start of the scan line specified Range Compare Register.	I in the Pipe B [Display	Scan Line	Count
7:6	Reserved Project: All			Format:	MBZ



	Display Engine Render Response Messa	ge Bit Def	finitio	on	
5	Pipe_A_Start_of_Horizontal_Blank_Event This even will be reported on the start of the Pipe A Horizontal B	Project: lank	All	Format:	
4	Reserved Project: All			Format:	MBZ
3	Pipe_A_Start_of_Vertical_Blank_Event This even will be reported on the start of the Pipe A Vertical Blan	Project: ik.	All	Format:	
2	Pipe_A_Sprite_Plane_Flip_Done_Event This even will be reported on the completion of a flip for the Pipe	Project: A Sprite Plar	All ne.	Format:	
1	Pipe_A_Primary_Plane_Flip_Done_Event This even will be reported on the completion of a flip for the Pipe	Project: A Primary Pl	All ane.	Format:	
0	Pipe_A_Scanline_Event This even will be reported on the start of the scan line specified i Range Compare Register.	Project: n the Pipe A I	All Display	Format: / Scan Line	Count

2.6.2 DERRMR — Display Engine Render Response Mask Register

Register Typ				gister
	pe: IVIIVI	10		
Address Off	i set: 440	50h		
Project:	Dev	SNB		
Default Valu	ie: FFF	FFFFFh		
Access:	R/W	1		
Size (in bits)): 32			
"unmasked".	. "Unmas	ked" bits will cause a	I which render response message bits are "n a render response message to be sent and w red and will not cause a render response mes	vill be reported in that
Bit			Description	
31:0	Display_I	Engine_Render_Resp	onse_Message_Mask_Bits	
	Project:	All		
	Format:	Display Engine Render	r Response Message Bit Definition See	Description Above
	This field response		ich selects which events cause and are reported i	n the render
	Value	Name	Description	Project
	0b	Not Masked	Not Masked – will be cause and be reported in the message	All
	1b	Masked	Masked – will not cause or be reported in the message	All



2.7 Display Arbitration Control

2.7.1 DISP_ARB_CTL—Display Arbiter Control

Register Type: MMIO Address Offset: 45000h Project: All Default Value: C2240622h Access: R/W Size (in bits): 32 Trusted Type: 1 Bit Description 31 FBC_Memory_Wake(testmode) Project: All Security: Test Default Value: 1b Setting this bit allows FBC compressed write requests to wake memory from SR (default: on) 30 KVMr_Memory_Wake(testmode) Project: All Security: Test Default Value: 1b Setting this bit allows KVMr display write back requests to wake memory from SR. (default: on) 29 Opportunistic_Fetch_Mode_Enable(testmode) Project: All Security: Test Default Value: 0b Setting this bit allows opportunistic data fetches (even when above watermark) when other clients wake the system from SelfRefresh. For any opportunistic fetch to happen, display should not be in process of waking the system. 28 Reserved Project: All			DISP_	ARB_C	FL—Display Arbiter Control
31 FBC_Memory_Wake(testmode) Project: All Security: Test Default Value: 1b Setting this bit allows FBC compressed write requests to wake memory from SR (default: on) 30 KVMr_Memory_Wake(testmode) Project: All Security: Test Default Value: 1b Setting this bit allows KVMr display write back requests to wake memory from SR. (default: on) 29 Opportunistic_Fetch_Mode_Enable(testmode) Project: All Security: Test Default Value: 1b Setting this bit allows KVMr display write back requests to wake memory from SR. (default: on) 29 Opportunistic_Fetch_Mode_Enable(testmode) Project: All Security: Test Default Value: 0b Setting this bit allows opportunistic data fetches (even when above watermark) when other clients wake the system from SelfRefresh. For any opportunistic fetch to happen, display should not be in process of waking the system.	Address Of Project: Default Val Access: Size (in bits	ffset: 45000h All ue: C22406 R/W s): 32	22h		
Project: All Security: Test Default Value: 1b Setting this bit allows FBC compressed write requests to wake memory from SR (default: on) 30 KVMr_Memory_Wake(testmode) Project: All Security: Test Default Value: 1b Setting this bit allows KVMr display write back requests to wake memory from SR. (default: on) 29 Opportunistic_Fetch_Mode_Enable(testmode) Project: All Security: Test Default Value: 0b Setting this bit allows opportunistic data fetches (even when above watermark) when other clients wake the system from SelfRefresh. For any opportunistic fetch to happen, display should not be in a process of waking the system.	Bit				Description
Security: Test Default Value: 1b Setting this bit allows FBC compressed write requests to wake memory from SR (default: on) 30 KVMr_Memory_Wake(testmode) Project: All Security: Test Default Value: 1b Setting this bit allows KVMr display write back requests to wake memory from SR. (default: on) 29 Opportunistic_Fetch_Mode_Enable(testmode) Project: All Security: Test Default Value: 0b Setting this bit allows opportunistic data fetches (even when above watermark) when other clients wake the system from SelfRefresh. For any opportunistic fetch to happen, display should not be in process of waking the system.	31	FBC_Memory	-Wake(tes	stmode)	
Default Value: 1b Setting this bit allows FBC compressed write requests to wake memory from SR (default: on) 30 KVMr_Memory_Wake(testmode) Project: All Security: Test Default Value: 1b Setting this bit allows KVMr display write back requests to wake memory from SR. (default: on) 29 Opportunistic_Fetch_Mode_Enable(testmode) Project: All Security: Test Default Value: 0b Setting this bit allows opportunistic data fetches (even when above watermark) when other clients wake the system from SelfRefresh. For any opportunistic fetch to happen, display should not be in process of waking the system.		Project:		All	
Setting this bit allows FBC compressed write requests to wake memory from SR (default: on) 30 KVMr_Memory_Wake(testmode) Project: All Security: Test Default Value: 1b Setting this bit allows KVMr display write back requests to wake memory from SR. (default: on) 29 Opportunistic_Fetch_Mode_Enable(testmode) Project: All Security: Test Default Value: 0b Setting this bit allows opportunistic data fetches (even when above watermark) when other clients wake the system from SelfRefresh. For any opportunistic fetch to happen, display should not be in process of waking the system.		Security:		Test	
30 KVMr_Memory_Wake(testmode) Project: All Security: Test Default Value: 1b Setting this bit allows KVMr display write back requests to wake memory from SR. (default: on) 29 Opportunistic_Fetch_Mode_Enable(testmode) Project: All Security: Test Default Value: 0b Setting this bit allows opportunistic data fetches (even when above watermark) when other clients wake the system from SelfRefresh. For any opportunistic fetch to happen, display should not be in process of waking the system.		Default Value:		1b	
Project: All Security: Test Default Value: 1b Setting this bit allows KVMr display write back requests to wake memory from SR. (default: on) 29 Opportunistic_Fetch_Mode_Enable(testmode) Project: All Security: Test Default Value: 0b Setting this bit allows opportunistic data fetches (even when above watermark) when other clients wake the system from SelfRefresh. For any opportunistic fetch to happen, display should not be in process of waking the system.		Setting this bit	allows FB0	C compress	ed write requests to wake memory from SR (default: on)
Security: Test Default Value: 1b Setting this bit allows KVMr display write back requests to wake memory from SR. (default: on) 29 Opportunistic_Fetch_Mode_Enable(testmode) Project: All Security: Test Default Value: 0b Setting this bit allows opportunistic data fetches (even when above watermark) when other clients wake the system from SelfRefresh. For any opportunistic fetch to happen, display should not be in process of waking the system.	30	KVMr_Memor	y_Wake(te	estmode)	
Default Value: 1b Setting this bit allows KVMr display write back requests to wake memory from SR. (default: on) 29 Opportunistic_Fetch_Mode_Enable(testmode) Project: All Security: Test Default Value: 0b Setting this bit allows opportunistic data fetches (even when above watermark) when other clients wake the system from SelfRefresh. For any opportunistic fetch to happen, display should not be in process of waking the system.		Project:		All	
Setting this bit allows KVMr display write back requests to wake memory from SR. (default: on) 29 Opportunistic_Fetch_Mode_Enable(testmode) Project: All Security: Test Default Value: Ob Setting this bit allows opportunistic data fetches (even when above watermark) when other clients wake the system from SelfRefresh. For any opportunistic fetch to happen, display should not be in process of waking the system.		Security:		Test	
29 Opportunistic_Fetch_Mode_Enable(testmode) Project: All Security: Test Default Value: 0b Setting this bit allows opportunistic data fetches (even when above watermark) when other clients wake the system from SelfRefresh. For any opportunistic fetch to happen, display should not be in process of waking the system.		Default Value:		1b	
Project: All Security: Test Default Value: 0b Setting this bit allows opportunistic data fetches (even when above watermark) when other clients wake the system from SelfRefresh. For any opportunistic fetch to happen, display should not be in process of waking the system.		Setting this bit	allows KVI	Mr display w	rite back requests to wake memory from SR. (default: on)
Security: Test Default Value: 0b Setting this bit allows opportunistic data fetches (even when above watermark) when other clients wake the system from SelfRefresh. For any opportunistic fetch to happen, display should not be in process of waking the system.	29	Opportunistic	_Fetch_M	ode_Enable	e(testmode)
Default Value: 0b Setting this bit allows opportunistic data fetches (even when above watermark) when other clients wake the system from SelfRefresh. For any opportunistic fetch to happen, display should not be in process of waking the system.		Project:		All	
Setting this bit allows opportunistic data fetches (even when above watermark) when other clients wake the system from SelfRefresh. For any opportunistic fetch to happen, display should not be in process of waking the system.		Security:		Test	
wake the system from SelfRefresh. For any opportunistic fetch to happen, display should not be in process of waking the system.		Default Value:		0b	
28 Reserved Project: All Format:		wake the syste	em from Se	lfRefresh. F	
	28	Reserved	Project:	All	Format:
27:26 HP_Queue_Watermark	27:26	HP_Queue_W	/atermark		
Project: All		Project:		All	
Default Value: 00b		Default Value:		00b	



25:24	LP_Write	_Request_Limit								
	Project:	ŀ	All							
	Default Va	Default Value: 10b 4								
		in this register in rom a single clier		e maximum number of back to back LP write require-arbitrating.	ests that will be					
	Value	Name	De	scription Pro	ject					
	00b	1	1	All						
	01b	2	2	All						
	10b	4	4 (0	default) All						
	11b	8	8	All						
23:20	TLB_Req	uest_Limit								
	Project:	ŀ	All							
	Default Va	lue: C	010b	2						
	Range:	1	15							
				e maximum number of TLB requests that can be m ult 2). Zero is not a valid programming.	ade in an					
19:16	TLB_Requ	uest_In-Flight_L	imit							
	Project:	A	All							
	Default Va	lue: C)100b	4						
	Range:		15							
				e maximum number of TLB (or VTd) requests that fault 4). Zero is not a valid programming.	can be in flight					
	EBC Wat	ermark_Disable	(testmode	e)						
15	FBC_Wall			-,						
15	Project:		All	-,						
15		ŀ	All Fest	-,						
15	Project:	<i>4</i> ۲		-,						
15	Project: Security: Default Va Setting this	ہ ٦ اue: C s bit disables the	⊺est)b FBC wate	ermarks.						
15	Project: Security: Default Va Setting this	ہ ٦ اue: C	⊺est)b FBC wate	ermarks.						
	Project: Security: Default Va Setting this [ILK, This]	ہ ٦ اue: C s bit disables the	Fest 0b FBC wate 1 for all s	ermarks. steppings.						
	Project: Security: Default Va Setting this [ILK, This]	/ lue: C s bit disables the bit must be set to Swizzling_for_T	Fest 0b FBC wate 1 for all s	ermarks. steppings.						
	Project: Security: Default Va Setting this [ILK, This] Address_	/ lue: () s bit disables the bit must be set to Swizzling_for_T	Fest Db FBC wate 1 for all s Tiled-Surf a	ermarks. steppings.						
	Project: Security: Default Va Setting this [ILK, This Address_ Project: Default Va	/ lue: 0 s bit disables the bit must be set to Swizzling_for_T / lue: 0	Fest bb FBC wate 1 for all s iled-Surf All	ermarks. steppings.						
	Project: Security: Default Va Setting this [ILK, This Address_ Project: Default Va	/ lue: 0 s bit disables the bit must be set to Swizzling_for_T / lue: 0	Fest bb FBC wate 1 for all s iled-Surf All	ermarks. steppings. aces	Project					
	Project: Security: Default Va Setting this [ILK, This] Address_ Project: Default Va DRAM cor	/ lue: () s bit disables the bit must be set to Swizzling_for_T / lue: () nfiguration registe	Fest bb FBC wate 1 for all s iled-Surf All	ermarks. steppings. aces f memory address swizzling is needed.	Project All					
15	Project: Security: Default Va Setting this [ILK, This] Address_ Project: Default Va DRAM cor Value	/ lue: () s bit disables the bit must be set to Swizzling_for_T / lue: () figuration registe	Fest bb FBC wate 1 for all s iled-Surf All	ermarks. steppings. aces f memory address swizzling is needed. Description						



12	Reserved	Project:	All	Format:
1:8	HP_Page_Brea	ak_Limit		
	Project:		All	
	Default Value:		0110b	6
	_		4 45	
	Range:		115	
	The value in this		represents the m	aximum number of page breaks allowed in a HP reques ot a valid programming.
7	The value in this chain. Range 1		represents the m	
7 6:0	The value in this chain. Range 1	– 15, (def Project:	represents the m fault 6). Zero is n All	ot a valid programming.
	The value in this chain. Range 1	– 15, (def Project:	represents the m fault 6). Zero is n All	ot a valid programming.
·	The value in this chain. Range 1 Reserved HP_Data_Requ	– 15, (def Project:	represents the m fault 6). Zero is n All	ot a valid programming.

2.7.2 DISP_ARB_CTL2—Display Arbiter Control 2 [DevSNB]

Register 1	Type: MN	/IO			
Address (Offset: 450)04h			
Project:	De	vSNB			
Default Va	alue: 000	00000h			
Access:	R/\	N			
Size (in bi	its): 32				
Bit			C	Description	
31:9	Reserve	d Project:	All	Fc	ormat:
8	Fetch_Ti	iming			
	Project:		All		
	Default V	alue:	0b		
	register is	s used to specify		ortunistic Fetches are enable c fetch can happen. For any o waking the system.	
	Value	Name	Description		Project
	0b	FE inSR	Fetch on falling edge	of inSR	All
	1b	Not inSR	Fetch when not inSR		All



7	Opportuni	istic_Fetch_Beha	vior	
	Project:	All		
	Default Va	lue: 0h		
	register rep	presents the fetch l	alid only when Opportunistic Fetches are enab behavior when an opportunistic fetch is trigger Ild not be in the process of waking the system.	red. For any opportunistic
	Value	Name	Description	Project
	0h	One Burst	One Burst Only	All
	1h	Fill FIFO	Fill FIFO to Top	All
6	Reserved	Project:	All	Format: MBZ
5:4	Inflight_H	P_Read_Request	_Limit	
	Project:	All		
	Default Va	lue: 00	b	
		in this register repr any given time.	resents the maximum number of HP read requ	lest transactions that can
	Value	Name	Description	Project
	Value 00b	Name 128 HP	Description 128 HP inflight transactions limit	Project All
			•	
	00b	128 HP	128 HP inflight transactions limit	All
	00b 01b	128 HP 64 HP	128 HP inflight transactions limit 64 HP inflight transactions limit	All
:2	00b 01b 10b	128 HP 64 HP 32 HP 16 HP	128 HP inflight transactions limit 64 HP inflight transactions limit 32 HP inflight transactions limit 16 HP inflight transactions limit	All All All
	00b 01b 10b 11b Reserved	128 HP 64 HP 32 HP 16 HP	128 HP inflight transactions limit 64 HP inflight transactions limit 32 HP inflight transactions limit 16 HP inflight transactions limit	All All All All All
	00b 01b 10b 11b Reserved	128 HP 64 HP 32 HP 16 HP Project:	128 HP inflight transactions limit 64 HP inflight transactions limit 32 HP inflight transactions limit 16 HP inflight transactions limit	All All All All All
	00b 01b 10b 11b Reserved RTID_FIF0	128 HP 64 HP 32 HP 16 HP Project: O_Watermark All	128 HP inflight transactions limit 64 HP inflight transactions limit 32 HP inflight transactions limit 16 HP inflight transactions limit	All All All All All
	00b 01b 10b 11b Reserved RTID_FIF0 Project: Default Va The value	128 HP 64 HP 32 HP 16 HP Project: D_Watermark All lue: 0b in this register repr	128 HP inflight transactions limit 64 HP inflight transactions limit 32 HP inflight transactions limit 16 HP inflight transactions limit	All All All All Format:
	00b 01b 10b 11b Reserved RTID_FIF0 Project: Default Va The value	128 HP 64 HP 32 HP 16 HP Project: D_Watermark All lue: 0b in this register repr	128 HP inflight transactions limit 64 HP inflight transactions limit 32 HP inflight transactions limit 16 HP inflight transactions limit	All All All All Format:
	00b 01b 10b 11b Reserved RTID_FIFO Project: Default Va The value only when	128 HP 64 HP 32 HP 16 HP Project: D_Watermark All lue: 0b in this register repr the FIFO level is a	128 HP inflight transactions limit 64 HP inflight transactions limit 32 HP inflight transactions limit 16 HP inflight transactions limit All resents the watermark value for the RTID FIFO above or equal the watermark	All All All All All All Commute Commut
	00b 01b 10b 11b Reserved RTID_FIFC Project: Default Va The value only when Value	128 HP 64 HP 32 HP 16 HP Project: O_Watermark All Ilue: 0b in this register repr the FIFO level is a Name	128 HP inflight transactions limit 64 HP inflight transactions limit 32 HP inflight transactions limit 16 HP inflight transactions limit All resents the watermark value for the RTID FIFO above or equal the watermark Description	All All All All All All All Commute Format: D. HP transactions will star Project
3:2 :0	00b 01b 10b 11b Reserved RTID_FIFC Project: Default Va The value only when Value 00b	128 HP 64 HP 32 HP 16 HP Project: O_Watermark All lue: 0b in this register repr the FIFO level is a Name 8 RTIDs	128 HP inflight transactions limit 64 HP inflight transactions limit 32 HP inflight transactions limit 16 HP inflight transactions limit All All Description 8 RTIDs available in FIFO	All All All All All All All All Commut: Pormat: Project All All



2.8 Display Watermark Registers

The watermark registers are used to control the display to memory request timing. The watermarks must be programmed according to the rules provided in the "Programming Watermarks" document. The default values of the watermarks should allow the display to operate in any mode supported by the memory configuration. However, the default watermarks are not optimized for power or memory bandwidth efficiency. Watermarks must enable from the bottom up, meaning if WM2 is disabled, WM3 must also be disabled, and if WM1 is disabled, both WM2 and WM3 must also be disabled. Watermark latency values must increase from the bottom up, meaning WM1 (if enabled) must have higher latency than WM0, and so on. [ILK] The low power 1 display watermark register latency value must be programmed to match the Memory Latency Timer Register (MLTR, MCHBAR BDF 0:0:0, Offset 0x1222) Self Refresh Latency Time microsecond value, and the low power 2 display watermark register latency value must be programmed to match the Memory Latency Timer Register (MPLL Shutdown Latency Time microsecond value.

2.8.1 WM0_PIPE_A—Pipe A Main Watermarks

		WM0_	PIPE_/	A—Pipe A Main Watermarks	
Register Ty	ype: MMIO				
Address O	ffset: 45100h	ו			
Project:	All				
Default Val	lue: 007838	318h			
Access:	R/W				
Size (in bit	s): 32				
Bit				Description	
31:23	Reserved	Project:	All	Format:	
22:16	Pipe_A_Prin	nary_Waterm	ark	Project:	All
	Number in 64 memory	IBs of data in	FIFO bel	low which the Pipe A Primary stream will generate requests to)
15:14	Reserved	Project:	All	Format:	
13:8	Pipe_A_Spri	ite_Waterma	rk	Project:	All
	Number in 64 memory	Bs of data in	FIFO bel	ow which the Pipe A Sprite stream will generate requests to	
7:5	Reserved	Project:	All	Format:	
4:0	Pipe_A_Cur	sor_Waterma	ark	Project:	All
	Number in 64 memory	IBs of data in	FIFO bel	low which the Pipe A Cursor stream will generate requests to	



2.8.2 WM0_PIPE_B—Pipe B Main Watermarks

	WM0_PIPE_B—Pipe B Main Watermarks					
Register T	pe: MMIO					
Address O	ffset: 45104h	า				
Project:	All					
Default Val	ue: 007838	318h				
Access:	R/W					
Size (in bit	s): 32					
Trusted Ty	pe: 1					
Bit				Description		
31:23	Reserved	Project:	All	Format:		
22:16	Pipe_B_Prin	nary_Waterma	ark	Project:	All	
	Number in 64 memory	4Bs of data in F	FIFO belo	w which the Pipe B Primary stream will generate requests to		
15:14	Reserved	Project:	All	Format:		
13:8	Pipe_B_Spr	ite_Watermar	k	Project:	All	
	Number in 64 memory	4Bs of data in F	FIFO belo	w which the Pipe B Sprite stream will generate requests to		
7:5	Reserved	Project:	All	Format:		
4:0	Pipe_B_Cur	sor_Waterma	rk	Project:	All	
	Number in 64 memory	4Bs of data in F	FIFO belo	w which the Pipe B Cursor stream will generate requests to		



2.8.3 WM1—Low Power 1 Display Watermarks

	WM1—Low Power 1 Display Water	marks
Register Ty	pe: MMIO	
Address Of	fset: 45108h	
Project:	All	
Default Val	Je: 0000000h	
Access:	R/W	
Size (in bits	•	
	rmark values will be used only when one pipe is enabled and or using the Low Power 1 Sprite Watermark are met) and the	
Bit	Description	
31	Enabled	Project: All
	Enables LP1 watermarks	
30:24	Latency	Project: All
	The latency associated with the LP1 watermarks in half usecs.	
23:20	FBC_LP1_Watermark	Project: All
	Number of equivalent lines of the primary display for this WM	
19:17	Reserved Project: All	Format:
16:8	LP1_Primary_Watermark	Project: All
	Number in 64Bs of data in FIFO below which the Primary stream w	ill generate requests to memory.
7:6	Reserved Project: All	Format:
5:0	LP1_Cursor_Watermark	Project: All
	Number in 64Bs of data in FIFO below which the Cursor stream wi	Il generate requests to memory.

2.8.4 WM2—Low Power 2 Display Watermarks

WM2—Low Power 2 Display Watermarks					
Register Type:	MMIO				
Address Offset:	4510Ch				
Project:	All				
Default Value:	0000000h				
Access:	R/W				
Size (in bits):	32				
These watermark values will be used only when one pipe is enabled and no sprites are enabled and the lisplay is in LP2 state.					



Bit				Description		
31	Enabled				Project:	All
	Enables LP2	watermarks				
30:24	Latency				Project:	All
	The latency a	ssociated wi	th the LP2	2 watermarks in half usecs.		
23:20	FBC_LP2_W	atermark			Project:	All
	Number of eq	uivalent lines	s of the pi	rimary display for this WM		
19:17	Reserved	Project:	All	Forma	t:	
16:8	LP2_Primary	_Watermarl	(Project:	All
	Number in 64	Bs of data in	FIFO bel	low which the Primary stream will generate red	quests to memo	ory.
7:6	Reserved	Project:	All	Forma	t:	
5:0	LP2_Cursor_	Watermark			Project:	All
	Number in 64	Bs of data in	FIFO bel	low which the Cursor stream will generate requ	uests to memo	rv.

2.8.5 WM3—Low Power 3 Display Watermarks

Register T	vpe: MMIO						
	ffset: 45110h						
Project:	All						
Default Va	lue: 0000000h						
Access:	R/W						
Size (in bit	s): 32						
	ermark values will be used only when one pipe is enabled and no n LP3 state.	o sprites are enabled an	d the				
Bit	Description						
31	Enabled	Project:	All				
	Enables LP3 watermarks						
30:24	Latency	Project:	All				
	The latency associated with the LP3 watermarks in half usecs.						
23:20	FBC_LP3_Watermark	Project:	All				
	Number of equivalent lines of the primary display for this WM						
19:17	Reserved Project: All	Format:					
16:8	LP3_Primary_Watermark	Project:	All				
	Number in 64Bs of data in FIFO below which the Primary stream will generate requests to memory.						



	WM3—Low Power 3 Display Watermarks	
5:0	LP3_Cursor_Watermark	Project: All
	Number in 64Bs of data in FIFO below which the Cursor stream will generate re	equests to memory.

2.8.6 WM1S—Low Power 1 Sprite Watermark

			WM1	S—L	ow Power 1 Sprite Watermark
Register Ty	ype: N	IMIO			
Address O	ffset: 4	5120h			
Project:	A	II			
Default Val	lue: 0	1000000	า		
Access:	R	/W			
Size (in bit	s): 3	2			
This waterr enabled an					ne pipe is enabled and a sprite is enabled and sprite scaling is not
Bit					Description
31	Enable	d			Project: All
	Enable: enable		rite water	mark.	This bit allows memory self refresh to be entered when sprite is
30:8	Reserv	ed l	Project:	All	Format:
7:0	LP1_S	orite_Wa	termark		
	Project			All	
	Default	Value:		0b	
	Numbe	r in 64Bs	of data ir	n FIFO	below which the Sprite stream will generate requests to memory.



2.9 Refresh Rate Hardware Control Register

2.9.1 RR_HW_CTL—Refresh Rate Hardware Control

	F	RR_HW_CT	Refresh Ra	ate Hardwa	re Control		
Register T	ype: MMIO						
Address C	offset: 45300h						
Project:	All						
Default Va	lue: 0000000	0h					
Access:	R/W						
Size (in bit	t s): 32						
ate mode.		hold a minimu	sition updates, to m number of fram				
		9.	Des	scription			
Bit				scription			107
	Reserved	e. Project: A		scription		Format:	MBZ
Bit	Reserved	Project: A		scription		Format: Project:	MBZ
Bit 31:16	Reserved Minimum_Nu This field spec mode before a	Project: A mber_Of_High_ ifies the minimu	Power_Frames n number of frames to the low power ret	s that must be s		Project: ower refresh	All
Bit 31:16	Reserved Minimum_Nu This field spec mode before a number of fram	Project: A mber_Of_High_ ifies the minimu llowing a switch nes desired mini	Power_Frames n number of frames to the low power ret	s that must be s		Project: ower refresh	All



2.10 Backlight Control and Modulation Histogram Registers

2.10.1 **BLC_PWM_CTL2—Backlight PWM Control Register 2**

	BL	C PWM CTL	2—Backlight PWM Control Register	2			
Register 1 Address (Project: Default Va Access: Size (in bi	Type: MMIO Offset: 48250 All alue: 00000 R/W))h					
Bit	it Description						
31	PWM_Enab Project: Default Valu This bit enal	All	ter logic				
	Value	Name	Description	Project			
	0b	Disable	PWM disabled (drives 0 always)	All			
	1b	Enable	PWM enabled	All			
30	Reserved	Project: All	Format	:			
29	Project: Default Valu This bit assi	gns PWM to a pipe	. The PWM counter will run off of this pipe's PLL.	The PWM function			
	Value	Name	Description	Project			
	0b	Pipe A	Pipe A	All			
	1b	Pipe B	Pipe B	All			
28:27	Reserved	Project: All	Format	:			
26	Project: Access: Default Valu This bit will I	ie: 0b be set by hardware	Clear when a Phase-In interrupt has occurred. Software interrupt generation.	e will clear this bit by			



	BLC	_PWM_CT	L2—Backlight PWM Contr	ol Register 2				
25	Phase_In_En	able		Project: All				
		Setting this bit enables a PWM phase in based on the programming of the Phase In registers below. This bit clears itself when the phase in is completed.						
24	Phase_In_Interrupt_Enable Project:							
	Setting this bit	enables an inte	errupt to be generated when the PWN	Λ phase in is completed.				
23:16	Phase_In_tim	ne_base						
	Project:	All						
	Default Value:	0b						
	This field determines the number of VBLANK events that pass before one increment occurs.							
	Value	Name	Description	Project				
	0b		Invalid	All				
	01h-FFh		VBlank Count	All				
15:8	Phase_In_Co	unt	·	Project: All				
	This field determines the number of increment events in this phase in. Writes to this ronly occur when hardware-phase-ins are disabled. Reads to this register can occur a the value in this field indicates the number of increment events remaining to fully applicate request as hardware automatically decrements this value. A value of 0 is invalid.							
7:0	Phase_In_Inc	Project: All						
	This field indi	cates the amou	nt to adjust the PWM duty cycle regis	ter on each increment event.				
	This is a two's	complement n	umber.					

2.10.2 **BLC_PWM_CTL—Backlight PWM Control Register**

	E	<mark>BLC</mark> _PWI	I_CTL—Backlight PW	M Control Register			
Register Ty	ype: MMIC						
Address O	ffset: 48254	h					
Project:	All						
Default Val	lue: 00000	000h					
Access:	R/W						
Size (in bit	s): 32						
Bit			Descript	tion			
31:16	Reserved	Project:	All	Format:			
15:0	Backlight_I	Duty_Cycle		Project:	All		
	Backlight_Duty_Cycle Project: All This field determines the number of time base events for the active portion of the PWM backlight control. This should never be larger than the frequency field. A value of zero will turn the backlight off. A value equal to the backlight modulation frequency field will be full on. This field gets updated when it is desired to change the intensity of the backlight, it will take affect at the end of the current PWM cycle. This value represents the active time of the PWM stream in PCH display raw clock periods multiplied by 128.						



2.10.3 BLM_HIST_CTL—Image Enhancement Histogram Control Register

BLN	I_HIST	_CTL-	-Image Enhancement Histogram Control R	egister						
Register T	ype: MN	110								
Address O	ffset: 482	260h								
Project:	All									
Default Va	lue: 000	00000h								
Access:	R/V	V								
Size (in bit	in bits): 32									
Bit		Description								
31	Image_Enhancement_Histogram_Enabled									
	Project:		All							
	Default Value:0bThis bit enables the Image Enhancement histogram logic to collect data.									
	Value	Name	Description	Project						
	0b	Disable	Image histogram is disabled	All						
	1b	Enable	The image histogram is enabled. When this bit is changed from a zero to a one, histogram calculations will begin after the next VBLANK of the assigned pipe.	All						
30	Image Enhancement Modification Table Enabled									
	Project:		All							
	Default V	alue	Ob							
	This bit e	nables the	Image Enhancement modification table.							
	Value	Name	Description	Project						
	0b	Disable	Disabled	All						
	1b	Enable	Enabled. When this bit is changed from a zero to a one, modifications begin after the next VBLANK of the assigned pipe.	All						



29	Project: Default Va This bit as	signs the IE function	to a pipe. IE events will be synchron disabled in order to change the value	
	Value	Name	Description	Project
	0b	Pipe A	Pipe A	All
	1b	Pipe B	Pipe B	All
28:25	Reserved	Project: Al		Format:
24	Project: Default Va	n Mode Select All lue: Ob		
	Value	Name	Description	Project
	0b	YUV	YUV Luma Mode	All
	1b	HSV	HSV Intensity Mode	All
23:16	This field in	Phase_In_Count ndicates the phase in p Phase in is enable	n count number on which the Image E d.	Project: All Enhancement table will be loaded if
15	Reserved	Project: All	F	ormat:
14:13	Enhancen Project: Default Va	nent_mode All lue: 00b		
	Value	Name	Description	Project
	00b	Direct	Direct look up mode	All
	01b	Additive	Additive mode	All
	10b	Multiplicative	Multiplicative mode	All
	11b	Reserved	Reserved	All
12	0		ble buffered registers to be loaded or	Project: All https://www.alue.com/allection/alue/alue/alue/alue/alue/alue/alue/alue



11	Bin_Reg	ister_Fund	ction_Select						
	Project:		All						
	Default V	alue:	Ob						
	This field indicates what data is being written to or read from the bin data register.								
	Value	Name	Description	Project					
	0b	BTC	Bin Threshold Count. A read from the bin data register returns that bin's threshold value from the most recent vblank load event (guardband threshold trip). Valid range for the Bin Index is 0 to 31.	All					
	1b	BIE	Bin Image Enhancement Value. Valid range for the Bin Index is 0 to 32	All					
			ct: All Format:						
10:7	Reserve	d Projec							

2.10.4 Image Enhancement Bin Data Register

Register 1	Гуре:	MMIO						
Address (Offset:	48264h	48264h					
Project:		All	All					
Exists If:		BLM_HIST_CTL:Bin Re	egister Function Select = 0					
Default Va	alue:	0000000h						
Access:		Read Only	Read Only					
Size (in bits): 32								
			ter by programming the Bin Register	Function	Selec			
and the Bi Function (in Register Ind		Read Only	Function	Selec			
nd the Bi	in Register Ind	ex.		Function	Selec			
and the Bi Function (in Register Ind	ex.	Read Only	Function Project:	Selec			
and the Bi Function (Bit	in Register Ind) usage (Thres Busy_Bit	ex. hold Count) this Function is I	Read Only	Project:	All			
nd the Bi function (Bit	in Register Ind) usage (Thres Busy_Bit	ex. hold Count) this Function is I	Read Only Description	Project:	All			
Ind the Bi Function (Bit 31	in Register Ind D usage (Thres Busy_Bit If set , the en	ex. hold Count) this Function is I gine is busy, the rest of the regis	Read Only Description ster is undefined. If clear, the register cor	Project:	All			



Image Enhancement Bin Data Register(F1 Image Enhancement Usage)									
Register Type:	:	MMIO							
Address Offse	et:	8264h							
Project:		All							
Exists If:		BLM_HIST_CTL:Bin Register Function Select = 1							
Default Value:		0000000h							
Access:		R/W							
Size (in bits):		32							
Double Buffer Update Point: Next vblank if in normal mode, or on phase in Sync event frame if it is enabled									
Writes to this a	address are steer	ed to the correct register by programming the Bi	n Register Function Select						
and the Bin Re									
Function 1 usa	age (Image Enhar	ncement) this Function is Read/Write							
Bit		Description							
31:10 Re	eserved Proje	ct: All	Format:						
9:0 Im	nage_Bin_Correcti	on_Factor	Project: All						
no	The correction value for this bin. Writes to this register are double buffered on the next vblank if in normal mode, or on the phase in Sync event frame if it is enabled. The value written here is the 10bit corrected channel value for the lowest point of the bin.								



2.10.5 Histogram Threshold Guardband Register

		His	stogram	Threshold Guardband Register	r				
Register 1	Гуре:		MMIO						
Address (48268h						
Project:			All						
Default Va	alue:		0000000h						
Access:			R/W						
Size (in bi	its):		32						
Double Bu	uffer Update	e Point:	Start of vertical blank						
Bit				Description					
31 Histogram_Interru			t_enable						
Project:			All						
Default Value:			0b						
	Value	Name	Descripti	on		Project			
Ob		Disable	Disabled						
	1b	Enable		rates a histogram interrupt once a Histograr must always program 1.	n event occurs.	All			
30	Histogra	m_Event_s	tatus						
	Project:		All						
	Access:		R/W Clear						
	Default V	alue:	0b						
	When a H	listogram e	vent has oc	curred, this will get set by the hardware. For eds to clear this bit by writing a '1'. The defa	r any more Histog ault state for this b	ıram bit is '0'			
	Value	Name		Description	Project				
	0b	Not Oc	curred	Histogram event has not occurred	All				
	1b	Occure	d	Histogram event has occurred	All				
29:22	Guardba	nd_Interru	pt_Delay		Proj	ect: All			
				after this many consecutive frames of the g buffered on start of vblank. A value of 0 is i		ld being			
21:0	Threshol	d_Guardba	and		Proj	ect: All			
				the guardband for the threshold interrupt ger is value is double buffered on start of vblank		gle value			



2.11 Motion Blur Mitigation (MBM) Control

These registers are use to control the MBM logic. (Sometimes called LOT, panel overdrive, or LRTC).

Before enabling MBM, software should have identically programmed both pipes source size and gamma tables. Additionally, before executing a flip on the selected pipe (which generates the MBM frame) software should have loaded the address of the reference frame into the second plane(s), this can be done by MMIO or by a flip command. The second pipe does not need to have it's panel fitter, link, or link PLL enabled (or anything else down the pipe from MBM).

2.11.1 MBM_CTRL—MBM Control

MBM_CTRL—MBM Control								
Register Type: MMIO Address Offset: 48800h Project: All Default Value: 0000000h Access: R/W Size (in bits): 32 Bit Description								
31								
	Project: All Default Value: 0b This bit enables MBM logic.							
	0b	Disable		MBM is Disabled	Project All			
	1b	Enable		MBM is Enabled	All			
30	Reserved		ect: All	Format:				
29	29 MBM Pipe Select Project: All Default Value: 0b This bit assigns MBM modification to the selected pipe.							
	Value	Name	Descripti	on	Project			
	Ob	Pipe A	PipeA (Pip previous b	peA will fetch the current buffer and PipeB will fetch the puffer)	All			
	1b	Pipe B	PipeB (Pip previous b	peB will fetch the current buffer and PipeA will fetch the puffer)	All			



	MBM_CTRL—MBM Control								
28:27	MBM_Surfa	ace_select							
	Project:	Project: All							
	Default Valu								
	Value	Name	Description	n		Project			
	00b	None	None			All			
	01b	Sprite	Sprite Only			All			
	10b Primary		Primary Only			All			
	11b	Both	Both sprite	and primary		All			
26:24	Reserved	Project:	All			Format:			
23:16	MBM_Delta	_Threshol	d						
	Project:		All						
	Default Valu	le:	0000000b						
				t and previous component therwise, the current value					
15:0	Reserved	Project	: All		Format	:			



2.11.2 MBM_TBL—MBM Overdrive Table

MBM TBL—MBM Overdrive Table										
Register	Type: MA	/IO					•			
Address		810h								
Project:	All	51011								
Default V		00000h								
Access: R/W										
Size (in bits): 63x32										
These will be the overdrive values to be used as the lookup table entries for MBM. Correction table factors are stored x-major, groups of input values go together, ascending from row entry zero. The first row is internally hard coded to 0, so the first address actually corresponds to the second row of the table. The last ow is internally hard coded to 256, so only 7 rows total are programmable.										
verdriv	e table ado 0	dress offse 31	ets: 63	95	127	159	191	223	255	
0	0	0	0	0	0	0	0	0	0	
31	48810h	48814h	48818h	4881Ch	48820h	48824h	48828h	4882Ch	48830h	
63	48834h	48838h	4883Ch	48840h	48844h	48848h	4884Ch	48850h	48854h	
95	48858h	4885Ch	48860h	48864h	48868h	4886Ch	48870h	48874h	48878h	
127	4887Ch	48880h	48884h	48888h	4888Ch	48890h	48894h	48898h	4889Ch	
159	488A0h	488A4h	488A8h	488ACh	488B0h	488B4h	488B8h	488BCh	488C0h	
191	488C4h	488C8h	488CCh	488D0h	488D4h	488D8h	488DCh	488E0h	488E4h	
223	488E8h	488ECh	488F0h	488F4h	488F8h	488FCh	48900h	48904h	48908h	
255	256	256	256	256	256	256	256	256	256	
Previous Pixel Value Range Current Pixel Value Range Address Offset Hard Coded Value										
DWord	Bit					ription				
062	31:24	Reserved	l Project	: All			For	mat:		
	23:16	Red_MB	M_overdriv	e_value				Project:	All	
	15:8	Green_M	BM_overdr	ive_value				Project:	All	

Project:

All

7:0

Blue_MBM_overdrive_value



2.12 Color Conversion & Control Registers

These registers contain the coefficients of the pipe color space converter. There are 12 values in 6 registers for each pipe. Or alternately a YUV frame buffer could be converted to RGB.

The high color channel is the most significant bits of the color. The low color channel is the least significant bits of the color. The medium color channel is the bits between high and low. For example: In RGB modes Red is in the High channel, Green in Medium, and Blue in Low. In YUV modes, U is in the High channel, Y in Medium, and V in Low.

The color space conversion registers are double buffered and are updated on the start of vertical blank following a write to the CSC Mode register for the respective pipe.

Ductor	A 11		030	Coefficient Description			
Project: Default Va	All alue: 0000	Ωh					
Size (in b		011					
Coefficien	its for the C			n-exponent-mantissa format. Two C ta packing in each dword.	SC coefficients	s are stored i	
Bit				Description			
15	Sign						
	Project:		All				
	Value	Name		Description		Project	
	0b	Positive		Positive		All	
	1b	Negative		Negative		All	
14:12	Exponent	bits					
	Project:		All				
	Represent	ted as 2 ⁻ⁿ					
	Value	Name	Desc	ription	Proje	ect	
	110b	4	4 or r	nantissa is bb.bbbbbbb All			
	111b	2	2 or r	mantissa is b.bbbbbbbb		All	
	000b	1	1 or r	mantissa is 0.bbbbbbbbbbbbbbbbbbbbbbbbbbbbbbbbbbbb		All	
	001b	0.5	0.5 o	r mantissa is 0.0bbbbbbbbb	All		
	010b	0.25	0.25	or mantissa is 0.00bbbbbbbbbb	All		
	011b	0.125	0.12	5 or mantissa is 0.000bbbbbbbbb	All		
	others	Reserved	Rese	rved	All		
11:3	Mantissa				Pr	oject: All	



The matrix equations are as follows:

Y	=	(RY	*	R)	+	(GY	*	G)	+	(BY	*	B)
U	=	(RU	*	R)	+	(GU	*	G)	+	(BU	*	B)
V	=	(RV	*	R)	+	(GV	*	G)	+	(BV	*	B)

The standard programming for RGB to YUV is in the following table.

	Bt	1.601	Bt.709		
	Value	Program	Value	Program	
RU	0.2990	0x1990	0.21260	0x2D98	
GU	0.5870	0x0968	0.71520	0x0B70	
BU	0.1140	0x3E98	0.07220	0x3940	
RV	-0.1687	0xAAC8	-0.11460	0xBEA8	
GV	-0.3313	0x9A98	-0.38540	0x9C58	
BV	0.5000	0x0800	0.50000	0x0800	
RY	0.5000	0x0800	0.50000	0x0800	
GY	-0.4187	0x9D68	-0.45420	0x9E88	
BY	-0.0813	0xBA68	-0.04580	0xB5E0	

The standard programming for YUV to sRGB without scaling is in the following table.

The input is VYU on high, medium, and low channels respectively.

The output is RGB on high, medium, and low channels respectively.

Program the pre-CSC offsets to -128, -16, and -128 for high, medium, and low channels respectively.

The coefficients can be scaled if desired.

	Bt.601	Reverse	Bt.709 Reverse	
	Value	Program	Value	Program
GY	1.000	0x7800	1.000	0x7800
BY	0.000	0x0000	0.000	0x0000
RY	1.371	0x7AF8	1.574	0x7C98
GU	1.000	0x7800	1.000	0x7800
BU	-0.336	0x9AC0	-0.187	0xABF8
RU	-0.698	0x8B28	-0.468	0x9EF8
GV	1.000	0x7800	1.000	0x7800
BV	1.732	0x7DD8	1.855	0x7ED8
RV	0.000	0x0000	0.000	0x0000



2.12.1 Pipe A Color Control

2.12.1.1 CSC_A_Coefficients 1

CSC_A_Coefficients 1					
Register Ty	/pe:	MMIO			
Address Offset:		49010h			
Project:		All			
Default Value:		0000000h			
Access:		R/W			
Size (in bits):		32			
Double Buffer Update Point:		Start of vertical blank after armed			
Double Buffer Armed By: Write to CSC_A		CSC_A_Mode			
Bit	Description				
31:16	RY Project	t: All	Format:	CSC COEFFICIENT DESCRIPTION	
	CSC coefficient. See format description above.				
15:0	GY Project	t: All	Format:	CSC COEFFICIENT DESCRIPTION	
	CSC coefficient. See format description above.				



2.12.1.2 CSC_A_Coefficients 2

CSC_A_Coefficients 2						
Register Type:	MMIC)				
Address Offset:	4901	49014h				
Project:	All	All				
Default Value:	0000	0000000h				
Access:	R/W	R/W				
Size (in bits):	32	32				
Double Buffer Update P	oint: Start	Start of vertical blank after armed				
Double Buffer Armed B	y: Write	to CSC_A_Mode)			
Bit	Description					
31:16 BY	BY Project: All Format: CSC COEFFICIENT DESCRIPTION					
CSC coeffici	CSC coefficient. See format description above.					
15:0 Reserved	Project:	All	Format:			

2.12.1.3 CSC_A_Coefficients 3

CSC_A_Coefficients 3						
Register Ty	ype:	MMIO				
Address Offset:		49018h	49018h			
Project:		All	All			
Default Value:		0000000	0000000h			
Access:		R/W	R/W			
Size (in bits):		32	32			
Double Buffer Update Point:		Start of vertical blank after armed				
Double Buffer Armed By:		Write to C	SC_A_Mode)		
Bit	Description					
31:16	RU Proje	ect: All	Format:	CSC COEFFICIENT DESCRIPTION		
	CSC coefficient. See format description above.					
15:0	GU Proje	ect: All	Format:	CSC COEFFICIENT DESCRIPTION		
	CSC coefficient. See format description above.					



2.12.1.4 CSC_A_Coefficients 4

CSC_A_Coefficients 4							
Register T	ype:	MMIO					
Address O	ffset:	4901Ch					
Project:		All					
Default Val	lue:	00000000h					
Access:		R/W					
Size (in bit	s):	32					
Double Bu	ffer Update Point:	Start of vertical blank after armed					
Double Bu	ffer Armed By:	Write to CSC_A	_Mode				
Bit	Bit Description						
31:16	BU Proje	ct: All For	mat: CSC COEFFICIENT DESCRIPTION				
	CSC coefficient. See format description above.						
15:0	Reserved Proj	ect: All	Format:				

2.12.1.5 CSC_A_Coefficients 5

CSC_A_Coefficients 5						
Register Ty	pe:	MMIO				
Address Of	fset:	49020h				
Project:		All				
Default Valu	ue:	00000000	h			
Access:		R/W				
Size (in bits	s):	32				
Double Buf	fer Update Point:	Start of ve	ertical blank a	ifter armed		
Double Buf	fer Armed By:	Write to C	SC_A_Mode			
Bit				Description		
31:16	1:16 RV Project: All Format:		Format:	CSC COEFFICIENT DESCRIPTION		
	CSC coefficient. See format description above.			ove.		
15:0	GV Proje	ct: All	Format:	CSC COEFFICIENT DESCRIPTION		
	CSC coefficient. S	ee format de	escription abo	ove.		



2.12.1.6 CSC_A_Coefficients 6

CSC_A_Coefficients 6							
Register Type:	MMIO						
Address Offset:	49024h						
Project:	All						
Default Value:	0000000h						
Access:	R/W						
Size (in bits):	32						
Double Buffer Update Point	: Start of vertical blank a	Start of vertical blank after armed					
Double Buffer Armed By:	Write to CSC_A_Mode						
Bit		Description					
31:16 BV Pr	oject: All Format:	CSC COEFFICIENT DESCRIPTION					
CSC coefficient.	ve.						
15:0 Reserved	· ·						

2.12.1.7 CSC_A_Mode

CSC_A_Mode						
Register Type:	MMIO					
Address Offset:	49028h					
Project:	All					
Default Value:	00000000h					
Access:	R/W					
Size (in bits):	32					
Double Buffer Update Point:	Start of vertical blank					
Writes to this register arm C	SC_A registers					
Bit		Description				
31:3 Reserved Pro	ject: All	Format:				



			CSC_A_Mode				
2	CSC_Bla	ck_Screen_Of	fset				
	Project:		All				
	Default V	ult Value: 0b					
	Adds an	offset to the dat	ta output from CSC				
	In sRGB	ouput mode: R	GB is defined as R`+ 1/16, G`+ 1/16, B`+ 1/16				
	In rcYUV	output mode: \	(UV is defined as Y'+ 1/16, U and V are output in excess 2048 form	nat			
	Value	Name	Description	Project			
	0b	Ob No Offset CSC output has no offset added (will be RGB or YUV, depending on bit 0) Al					
	1b		CSC output has offset added (will be sRGB or rcYUV depending on bit 0)	All			
1	CSC_Position						
	Project:		All				
	Default V	alue:	0b				
	Selects the	ne CSC positior	n in the pipe.				
	Value	Name	Description	Project			
	0b	CSC After	CSC is after gamma and DPST image enhancement	All			
	1b	CSC Before	CSC is before gamma and DPST image enhancement	All			
0	CSC_Mo	de					
	Project:		All				
	Default V	alue:	0b				
	Selects the	ne CSC directio	n.				
	Value	Name	Description	Project			
	0b	RGB to YUV	RGB to YUV conversion	All			
	1b	YUV to RGB	YUV to RGB conversion	All			



2.12.1.8 Pre-CSC_A High Color Channel Offset

	Pre-CSC_A High Color (Channel Offset				
Register Type:	ММІО					
Address Offset:	49030h					
Project:	All					
Default Value:	0000000h					
Access:	R/W	R/W				
Size (in bits):	32	32				
Double Buffer Update Poi	nt: Start of vertical blank after arme	Start of vertical blank after armed				
Double Buffer Armed By:	Write to CSC_A_Mode					
Bit	Descri	ption				
31:13 Reserved	Reserved Project: All Format:					
12:0 Pre-CSC_Hig	h_Color_Channel_Offset	Project: All				
This 13-bit 2's	complement value is used to give an o	ffset to the color channel as it enters CSC logic.				

2.12.1.9 Pre-CSC_A Medium Color Channel Offset

	Pre-CSC_A Medium Color Ch	nannel Offset				
Register Type:	MMIO					
Address Offset:	49034h					
Project:	All					
Default Value:	0000000h					
Access:	R/W	R/W				
Size (in bits):	32					
Double Buffer Update Point	Start of vertical blank after armed					
Double Buffer Armed By:	Write to CSC_A_Mode					
Bit	Description					
31:13 Reserved	Reserved Project: All Format:					
12:0 Pre-CSC_Mediu	Pre-CSC_Medium_Color_Channel_Offset Project:					
This 13-bit 2's co	omplement value is used to give an offset	to the color channel as it enters CSC logic.				



Register 1	Who	MMIO				
•	21					
Address C	Diffset:	49038h				
Project:		All				
Default Va	lue:	0000000h				
Access:		R/W	R/W			
Size (in bi	ts):	32				
Double Bu	Iffer Update Point:	Start of vertical blank after armed				
Double Bu	Iffer Armed By:	Write to CSC_A_Mode				
Bit		Des	scription			
31:13	Reserved Project: All Format:					
12:0	Pre-CSC_Low_Co	lor_Channel_Offset	Projec	ct: All		
	This 13-bit 2's com	plement value is used to give a	n offset to the color channel as it enters CS	SC logic.		

2.12.1.10 Pre-CSC_A Low Color Channel Offset

2.12.2 Pipe B Color Control

2.12.2.1 CSC_B_Coefficients 1

CSC_B_Coefficients 1							
Register T	ype:		MMIO				
Address O	ffset:		49110h				
Project:			411				
Default Va	lue:		000000	0h			
Access:			R/W				
Size (in bit	s):	:	32				
Double Bu	ffer Update P	oint:	Start of vertical blank after armed				
Double Bu	ffer Armed By	y :	Write to	CSC_B_Mode)		
Bit					Description		
31:16 RY Project: All		All	Format:	CSC COEFFICIENT DESCRIPTION			
CSC coefficient. See format description above.			ove.				
15:0	GY	GY Project: All Format:			CSC COEFFICIENT DESCRIPTION		
	CSC coeffici	CSC coefficient. See format description above.					



2.12.2.2 CSC_B_Coefficients 2

CSC_B_Coefficients 2						
Register Type:	MMIO					
Address Offset:	49114h					
Project:	All					
Default Value:	0000000h					
Access:	R/W	R/W				
Size (in bits):	32	32				
Double Buffer Update Poin	t: Start of vertical blank a	Start of vertical blank after armed				
Double Buffer Armed By:	Write to CSC_B_Mode	9				
Bit Description						
31:16 BY P	roject: All Format:	CSC COEFFICIENT DESCRIPTION				
CSC coefficient. See format description above.						
15:0 Reserved	Project: All	Format:				

2.12.2.3 CSC_B_Coefficients 3

CSC_B_Coefficients 3						
Register Ty	/pe:	MMIO				
Address O	ffset:	49118h				
Project:		All				
Default Val	ue:	00000000	h			
Access:		R/W				
Size (in bit	s):	32				
Double But	ffer Update Point:	Start of ve	ertical blank a	ifter armed		
Double But	ffer Armed By:	Write to C	SC_B_Mode			
Bit				Description		
31:16 RU Project		t: All	Format:	CSC COEFFICIENT DESCRIPTION		
CSC coefficient. See format description above.			ove.			
15:0	GU Project: All Format:			CSC COEFFICIENT DESCRIPTION		
	CSC coefficient. See format description above.					



2.12.2.4 CSC_B_Coefficients 4

CSC_B_Coefficients 4							
Register T	ype:	MMIO					
Address O	ffset:	4911Ch					
Project:		All					
Default Val	lue:	00000000h					
Access:		R/W					
Size (in bit	s):	32					
Double Bu	ffer Update Point:	Start of vertical blank	after armed				
Double Bu	ffer Armed By:	Write to CSC_B_Mod	e				
Bit	t Description						
31:16 BU Project: All Format: CSC COEFFICIENT DE			CSC COEFFICIENT DESCRIPTION				
CSC coefficient. See format description above.							
15:0	Reserved Project: All Format:						

2.12.2.5 CSC_B_Coefficients 5

CSC_B_Coefficients 5						
Register Typ	be:	MMIO				
Address Off	set:	49120h				
Project:		All				
Default Valu	e:	00000000	h			
Access:		R/W				
Size (in bits)):	32				
Double Buff	er Update Point:	Start of ve	ertical blank a	after armed		
Double Buff	er Armed By:	Write to C	SC_B_Mode	•		
Bit				Description		
31:16 RV Project		ect: All	Format:	CSC COEFFICIENT DESCRIPTION		
CSC coefficient. See for			escription abo	ove.		
15:0	GV Proje	ect: All	Format:	CSC COEFFICIENT DESCRIPTION		
	CSC coefficient. S	See format de	escription abo	ove.		



2.12.2.6 CSC_B_Coefficients 6

CSC_B_Coefficients 6						
Register Type:		MMIO				
Address O	ffset:	49124h				
Project:		All				
Default Val	lue:	00000000h				
Access:		R/W				
Size (in bit	s):	32				
Double Bu	ffer Update Point:	Start of vertical blank af	ter armed			
Double Bu	ffer Armed By:	Write to CSC_B_Mode				
Bit			Description			
31:16 BV Projec		t: All Format:	CSC COEFFICIENT DESCRIPTION			
	CSC coefficient. Se	e format description abo	ve.			
15:0	Reserved Project	et: All	Format:			

2.12.2.7 CSC_B_Mode

CSC_B_Mode						
Register Type:	MMIO					
Address Offset:	49128h					
Project:	All					
Default Value:	00000000h					
Access:	R/W					
Size (in bits):	32					
Double Buffer Update Point:	Start of vertical blank					
Writes to this register arm C	SC_B registers					
Bit		Description				
31:3 Reserved Pro	oject: All	Format:				



			CSC_B_Mode							
2	CSC_Bla	ck_Screen_Of	fset							
	Project:	Project: All								
	Default Value: 0b									
	Adds an offset to the data output from CSC									
	In sRGB	ouput mode: R	GB is defined as R`+ 1/16, G`+ 1/16, B`+ 1/16							
	In rcYUV	output mode:	(UV is defined as Y'+ 1/16, U and V are output in excess 2048 form	nat						
	Value	Name	Description	Project						
	Ob		CSC output has no offset added (will be RGB or YUV, depending on bit 0)	All						
	1b		CSC output has offset added (will be sRGB or rcYUV depending on bit 0)	All						
1	CSC_Pos Project:		NI							
1	Project: Default V	Ą	b							
1	Project: Default V	A alue: 0	b	Project						
1	Project: Default V Selects tl	A alue: 0 he CSC positior	b n in the pipe.	Project All						
1	Project: Default V Selects th	۵ alue: 0 he CSC positior Name	b n in the pipe. Description	Project All All						
0	Project: Default V Selects the Value Ob	A alue: 0 he CSC position Name CSC After CSC Before	b n in the pipe. Description CSC is after gamma and DPST image enhancement	All						
	Project: Default V Selects the Ob 1b CSC_Mo Project:	A alue: 0 he CSC position Name CSC After CSC Before de	b n in the pipe. Description CSC is after gamma and DPST image enhancement CSC is before gamma and DPST image enhancement	All						
	Project: Default V Selects th Ob 1b CSC_Mo Project: Default V	A alue: 0 he CSC position Name CSC After CSC Before de A alue: 0	b n in the pipe. Description CSC is after gamma and DPST image enhancement CSC is before gamma and DPST image enhancement	All						
	Project: Default V Selects th Ob 1b CSC_Mo Project: Default V	A alue: 0 he CSC position Name CSC After CSC Before de A alue: 0	b n in the pipe. Description CSC is after gamma and DPST image enhancement CSC is before gamma and DPST image enhancement	All						
	Project: Default V Selects th Ob 1b CSC_Mo Project: Default V	A alue: 0 he CSC position Name CSC After CSC Before de A alue: 0	b n in the pipe. Description CSC is after gamma and DPST image enhancement CSC is before gamma and DPST image enhancement	All						
	Project: Default V Selects th Ob 1b CSC_Mo Project: Default V Selects th	A alue: 0 he CSC position Name CSC After CSC Before de A alue: 0 he CSC direction	b n in the pipe. Description CSC is after gamma and DPST image enhancement CSC is before gamma and DPST image enhancement CSC is before gamma and DPST image enhancement	All						



2.12.2.8 Pre-CSC_B High Color Channel Offset

	Pre-CSC_B High Color C	hannel Offset				
Register Type:	MMIO					
Address Offset:	49130h					
Project:	All					
Default Value:	0000000h					
Access:	R/W	R/W				
Size (in bits):	32					
Double Buffer Update Po	int: Start of vertical blank after armed	l				
Double Buffer Armed By	Write to CSC_B_Mode					
Bit	Descrip	tion				
31:13 Reserved	Reserved Project: All Format:					
12:0 Pre-CSC_B_	High_Color_Channel_Offset	Project: All				
This 13-bit 2's	complement value is used to give an offs	set to the color channel as it enters CSC logic.				

2.12.2.9 Pre-CSC_B Medium Color Channel Offset

		e-CSC_B Medium Col						
Register Typ	be:	MMIO						
Address Off	set:	49134h						
Project:		All						
Default Valu	e:	0000000h						
Access:		R/W	R/W					
Size (in bits)):	32						
Double Buff	er Update Point:	Start of vertical blank after ar	med					
Double Buff	er Armed By:	Write to CSC_B_Mode						
Bit	Description							
31:13	Reserved Project: All Format:							
12:0	Pre-CSC_B_Medium_Color_Channel_Offset				All			
	This 13-bit 2's com	plement value is used to give ar	n offset to the color channel as it ente	ers CSC le	oaic.			



Register T	vpe:	MMIO				
Address C	21 C	49138h				
Project:		All				
Default Va	lue:	00000000h				
Access:		R/W				
Size (in bits):		32				
Double Bu	uffer Update Point:	Start of vertical blank after armed				
Double Bu	uffer Armed By:	Write to CSC_B_Mode				
Bit		Descr	iption			
31:13	Reserved Project: All Format:					
12:0	Pre-CSC_B_Low_	Color_Channel_Offset	Project: All			
	This 13-bit 2's com	plement value is used to give an o	ffset to the color channel as it enters CSC logic.			

2.12.2.10 Pre-CSC_B Low Color Channel Offset

2.13 Display Palette Registers (4A000h–4CFFFh)

The display palette provides a means to correct the gamma of an image stored in a frame buffer to match the gamma of the monitor or presentation device. Additionally, the display palette provide a method for converting indexed data values to color values for VGA and 8-bpp indexed display modes. The display palette is located after the plane blender. Using the individual plane gamma enables, the blended pixels can go through or bypass the palette on a pixel by pixel basis.

The display palette can be accessed through multiple methods and operate in one of three different modes.

8 bit legacy palette mode (for indexed VGA and 8 bpp formats and for legacy gamma): 256 entries of 24 bits each (8 bits per color).

For indexed formats, an 8 bit per pixel value is used to lookup a 24 bit per pixel value from the palette which then is padded to 36 bits. This permits a compact data format to choose from 256 colors out of a larger palette of colors. The legacy palette is accessible through both MMIO and VGA palette register I/O addresses. Through VGA palette register I/O addresses, the palette can look as though there are only 6 bits per color component (this mapping is handled inside the VGA engine).

For legacy gamma, the 36 bits per pixel gamma input is chopped to 24 bits and used to lookup a 24 bit pixel value from the palette which then is padded to 36 bits. This permits a color to be re-mapped to a different brightness for gamma correction. This provides the lowest quality gamma and should only be used for legacy requirements.



10 bit precision palette mode (for 10 bit gamma):

1024 entries of 30 bits each (10 bits per color).

For 10 bit gamma, the 36 bits per pixel gamma input is chopped to 30 bits and used to lookup a 30 bit pixel value from the palette which then is padded to 36 bits. This permits a color to be re-mapped to a different brightness for gamma correction. This provides the highest quality gamma for non-indexed pixel data formats of 30 bits per pixel or less.

12 bit interpolated gamma mode:

512 entries of 16 bits each (format described in 12 bit interpolated gamma programming notes).

For 12 bit interpolated gamma, the 36 bits per pixel gamma input is used to lookup reference points (16 bits per color in 12.4 format) along a gamma curve and interpolate a 36 bit pixel result. This permits a color to be re-mapped to a different brightness for gamma correction. This provides the highest quality gamma for pixel data formats greater than 30 bits per pixel.

Pixel chopping refers to removing the LSBs of each color component to reduce bits per pixel. Pixel padding refers to adding LSBs to each color component to increase bits per pixel.

Accesses to the palette entries require that the core display clock is running at the time of the update. All write accesses to the palette must be in dwords. Byte or word writes to the palettes are not allowed.

2.13.1 LGC_PALETTE_A—Pipe A Legacy Display Palette

	LGC_PALETTE_A—Pipe A Legacy Display Palette							
Register Type: MMIO Address Offset: 4A000h Project: All Default Value: UUUUUUUUh Access: R/W (DWORD access only, no byte access) Size (in bits): 256x32								
DWord	Bit				I	Description		
0255	31:24	Reserved	Project:	All			Format:	
	23:16	Red_Palette	_Entry	Project:	All	Format:		
	15:8	Green_Pale	tte_Entry	Project:	All	Format:		
	7:0	Blue_Palett	e_Entry	Project:	All	Format:		



2.13.2 LGC_PALETTE_B—Pipe B Legacy Display Palette

	LGC_PALETTE_B—Pipe B Legacy Display Palette						
Register Ty	/pe: MM	10					
Address Of	f <mark>fset:</mark> 4A8	00h					
Project:	All						
Default Val	ue: UU	JUUUUUh					
Access:	R/W	/ (DWORD ac	cess only, r	no byte acce	ess)		
Size (in bits	s): 256	x32					
DWord	Bit				I	Description	
0255	31:24	Reserved	Project:	All			Format:
	23:16	Red_Palette	_Entry	Project:	All	Format:	
	15:8	Green_Pale	tte_Entry	Project:	All	Format:	
	7:0	Blue_Palette	e_Entry	Project:	All	Format:	

2.13.3 PREC_PALETTE_A—Pipe A Precision Display Palette

10 bit Precision Palette Mode Format					
Project:	All				
Format for	10 bit precision palette mode.				
Bit	Description				
31:30	Reserved Project: All	Format:			
29:20	Red_Palette_Entry	Project: All			
19:10	Green_Palette_Entry	Project: All			
9:0	Blue_Palette_Entry	Project: All			

12-bit Interpolated Precision Palette Mode (odd Dword) Format					
Project:	All				
Format for	12 bit interpolated gamma mode, odd dwords.				
Bit	Description				
31:30	Reserved Project: All	Format:			
29:20	Red_ Base[11:2]	Project: All			
19:10	Green_ Base[11:2]	Project: All			



9:0

Blue_ Base[11:2]

Project: All

	12-bit In	terpolated	d Precisio	on Palette Mode (even I	Dword) Format	
Project:	All					
Format for	12 bit interpo	lated gamm	a mode, odo	d dwords		
Bit				Description		
31:30	Reserved	Project:	All		Format:	MBZ
29:28	Red_Base[1	:0]			Project:	All
27:24	Red_Fractio	n			Project:	All
23:20	Reserved	Project:	All		Format:	
19:18	Green_Base	e[1:0]			Project:	All
17:14	Green_Fract	tion			Project:	All
13:10	Reserved	Project:	All		Format:	
9:8	Blue_Base[1	1:0]			Project:	All
7:4	Blue_Fraction	on			Project:	All
3:0	Reserved	Project:	All		Format:	

PREC_PALETTE_A—Pipe A Precision Display Palette(10 bit)								
Register Typ	De: MMIO							
Address Offs	set: 4B0	00h						
Project:	All							
Exists If:	PIP	EACONF:Pipe_A_P	alette/Gamma	_Unit_	mode = 01b			
Default Value	e: UUl	JUUUUUh						
Access:	R/W	(DWORD access of	only, no byte ad	ccess)				
Size (in bits)	: 102	4x32						
DWord	Bit				Description			
01023	31:0	10bit_mode	Project:	All	Format:	10 bit Precision Palette Mode Format		
		See format descrip	otion above					



	PRE	C_PALETTE_A—Pipe A Precision Display Palette(12 bit)
Register Ty	vpe: MM	10
Address Of	fset: 4B0)00h
Project:	All	
Exists If:	PIP	EACONF:Pipe_A_Palette/Gamma_Unit_mode = 10b
Default Value	ue: UUI	JUUUUUh
Access:	R/W	/ (DWORD access only, no byte access)
Size (in bits	s): 102	4x32
DWord	Bit	Description
0,2,4,102 2	31:0	12bit_even Project: All Format: 12-bit Interpolated Precision Palette Mode (even Dword) Format
		See format description above
1,3,5,102 3	31:0	12bit_odd Project: All Format: 12-bit Interpolated Precision Palette Mode (odd Dword) Format
		See format description above

2.13.4 PREC_PALETTE_B—Pipe B Precision Display Palette

	PREC_PALETTE_B—Pipe B Precision Display Palette(10 bit)								
Register Ty	ype: MMIO								
Address Of	fset: 4C	000h							
Project:	All								
Exists If:	PIP	EBCONF:Pipe_B_P	alette/Gamma	_Unit_	mode = 01b				
Default Valu	le: UU	UUUUUUh							
Access:	R/V	V (DWORD access o	only, no byte ad	cess)					
Size (in bits): 102	4x32							
DWord	Bit				Description				
01023	31:0	10bit_mode	Project:	All	Format:	10 bit Precision Palette Mode Format			
		See format descrip	otion above						



	PRE	C_PALETTE_B—Pipe B Precision Display Palette(12 bit)							
Register Ty	/pe: MMIO								
Address Of	fset: 4C0	000h							
Project:	All								
Exists If:	PIP	EBCONF:Pipe_B_Palette/Gamma_Unit_mode = 10b							
Default Val	ue: UU	UUUUUh							
Access:	R/V	V (DWORD access only, no byte access)							
Size (in bits	s): 102	24x32							
DWord	Bit	Description							
01023	63:32	12bit_odd Project: All Format: 12-bit Interpolated Precision Palette Mode (odd Dword) Format							
		See format description above							
	31:0 12bit_even Project: All Format: 12-bit Interpolated Precision Palette Mode (Format								
		See format description above							

12-bit Interpolated Gamma Programming Notes:

The 12-bit gamma correction curve is represented by specifying a set of reference points spaced equally along the desired curve. Red, Green, and Blue each have 513 reference points. The first 512 reference points are stored in the precision palette RAM, and the final value is stored in the GCMAX register. The first 512 reference points are 16 bits represented in a 12.4 format with 12 integer and 4 fractional bits. The final reference points are 17 bits represented in a 13.4 format with 13 integer and 4 fractional bits.

During operation the appropriate reference point pairs (adjacent) are selected for each color, and the output is interpolated between these two reference point values.

To program the gamma correction reference points, calculate the desired gamma curve for inputs from 0 to 4096. Every 8th point on the curve (0, 8, 16 ... 4088, 4096) becomes a reference point. Convert the gamma value to the 13.4 format. The first 512 reference points are saved to the precision palette RAM, where the even DWords contain the lower 6 bits of the reference point value, and the odd DWords contain the upper 10 bits of the reference point is saved in the GCMAX registers in 13.4 format.

Example equation for gamma curve of 2.2:

For (X = 0..4096) { gamma = $[(X / 4096) ^ 2.2] * 4096$ }

The curve must be flat or increasing, never decreasing.



2.13.5 PIPEAGCMAX—Pipe A Gamma Correction Max

	Pipe Max Gamma Correction Format							
Project: All Default Value: 00010000h								
Bit	D	escription						
31:17	Reserved Project: All	Format:						
16:0Max_Color_Gamma_Correction_PointProject:All513 th reference point for the color channel of the 12-bit pipe piecewise linear gamma correction. The value should always be programmed to be less than or equal to 4096.0.Project:All								

		PIPEAG	CMAX—Pipe	A Ga	mma Corr	ection Max	
Register Ty	egister Type: MMIO						
Address Of	fset: 4D0)00h					
Project:	All						
Default Val	ue: 000	10000h					
Access:	R/W	V					
Size (in bits	s): 3x3	2					
DWord	Bit				Description		
0	31:0	Red	Project:	All	Format:	Pipe Max Gamma Correction Format	
1	31:0	Green	Project:	All	Format:	Pipe Max Gamma Correction Format	
2	31:0	Blue	Project:	All	Format:	Pipe Max Gamma Correction Format	



2.13.6 PIPEBGCMAX — Pipe B Gamma Correction Max

		PIPEBG	CMAX—Pipe I	B Ga	mma Corr	ection Max
Register Ty	ype: MM	lio				
Address O	ffset: 4D0	010h				
Project:	All					
Default Val	lue: 000	10000h				
Access:	R/V	V				
Size (in bit	<mark>s):</mark> 3x3	2				
DWord	Bit				Description	
0	31:0	Red	Project:	All	Format:	Pipe Max Gamma Correction Format
1	31:0	Green	Project:	All	Format:	Pipe Max Gamma Correction Format
2	31:0	Blue	Project:	All	Format:	Pipe Max Gamma Correction Format

2.14 Software Flag Registers (4F000h-4F10Fh)

2.14.1 Software Flag Registers

Software Flag Registers								
Register Ty	r <mark>pe:</mark> M	MIO						
Address Of	fset: 4	=000h						
Project:	A	I						
Default Val	ue: 00	000000h						
Access:	R	/W						
Size (in bits	s): 36	6x32						
					e space and have no direct effect on hardware he software architecture.			
DWord	Bit		Description					
035	31:0	Reserved	Project:	All	Format: PBC			



2.14.2 GT Scratchpad

GT Scratchpad									
Register Ty	/pe: MN	AIO							
Address Of	ffset: 4F	100h							
Project:	All								
Default Val	ue: 00	0000000h							
Access:	R/\	N							
Size (in bits	s): 8x3	32							
					e space and have no direct effect on hardware the software architecture.				
DWord	Bit	Description							
07	31:0	Reserved	Project:	All	Format: PBC				



3. North Pipe and Port Controls (60000h–6FFFh)

3.1.1 Pipe A Timing

3.1.1.1 HTOTAL_A—Pipe A Horizontal Total Register

		HTOTAL	_A—Pipe	A Horizontal Total	Register		
Register Ty	ype: MMIO						
Address O	ffset: 60000h	า					
Project:	All						
Default Val	lue: 000000)00h					
Access:	R/W						
Size (in bit	s): 32						
Bit				Description			
31:29	Reserved	Project:	All		Format:	MBZ	
28:16	Pipe_A_Hor	izontal_Total	_Display_Clo	cks		Project:	All
		d, front/back		l up to 8192 pixels encomp race period. This field is pro			clocks
	This value sh		e equal or gre	tiple of two when driving the ater to the sum of the horiz			
15:12	Reserved	Project:	All		Format:	MBZ	
11:0	Pipe_A_Hor	izontal_Activ	e_Display_Pi	xels		Project:	All
		tive display pi		ve Display resolutions up to red pixel number 0. The va			
				d to multiples of two pixels horizontal active display si			VDS



3.1.1.2 HBLANK_A—Pipe A Horizontal Blank Register

		HBLANK	_A—Pip	e A Horizontal Blank Register			
Register T Address C Project: Default Va Access: Size (in bi	Offset: 60004 All alue: 000000 R/W						
Bit				Description			
31:29	Reserved	Project:	All	Format:			
28:16	Pipe_A_Hor	izontal_Blan	k_End	Project: All			
	number relat End pixel po considered p that there is	tive to the hor sition, where cosition 1, etc no left hand b of clocks with	izontal activ the first act Horizonta order area.	of Horizontal Blank End expressed in terms of the absolute pixel ve display start. The value programmed should be the HBLANK ive pixel is considered position 0; the second active pixel is I blank ending at the same point as the horizontal total indicates HBLANK size has a minimum value of 32 clocks. eds to be a multiple of two when driving the LVDS port in two			
	The value lo	aded in the re	gister woul	d be equal to RightBorder+Active+HBlank-1.			
		nust be 0, so t	•	must always be programmed to the same value as the			
15:13	Reserved	Project:	All	Format:			
12:0	Pipe_A_Hor	izontal_Blan	k_Start	Project: All			
	This 13-bit field specifies the Horizontal Blank Start position expressed in terms of the absolute pinumber relative to the horizontal active display start. The value programmed should be the HBLA Start pixel position, where the first active pixel is considered position 0; the second active pixel is considered position 1, etc.						
		n two channel		d right borders need to be a multiple of two when driving the izontal blank should only start after the end of the horizontal			
	The value lo	aded in the re	gister woul	d be equal to RightBorder+Active-1.			
	The border n Horizontal A		his register	must always be programmed to the same value as the			



3.1.1.3 HSYNC_A—Pipe A Horizontal Sync Register

		HSYNC	_A—Pipe A	Horizontal Sync Register				
Register T Address C Project: Default Va Size (in bi	Offset: 60008h All alue: 000000	-						
Bit	Description							
31:29	Reserved	Project:	All	Format	MBZ			
	number relat End pixel por considered p The number two channel	eld specifies tive to the hor sition, where position 1, etc of clocks in the mode. This v	rizontal active dis the first active pi : ne sync period ne	nc End position expressed in terms of the play start. The value programmed shou xel is considered position 0; the second eeds to be a multiple of two when driving reater than the horizontal sync start pos Porch+Sync-1.	Id be the HSYNC active pixel is g the LVDS port in			
15:13	Reserved	Project:	All	Format	MBZ			
12:0	number relat Start pixel po considered p HSYNC and than HBLAN	e: eld specifies ive to the hor osition, where osition 1, etc HBLANK will K start.	All 0b the horizontal Sy rizontal active dis a the first active p b. Note that when I be asserted on t	nc Start position expressed in terms of t play start. The value programmed shou ixel is considered position 0; the second h HSYNC Start is programmed equal to the same pixel clock. It should never be of the line needs to be a multiple of two v	uld be the HSYNC d active pixel is HBLANK Start, both programmed to less			



3.1.1.4 VTOTAL_A—Pipe A Vertical Total Register

		ντοτα	L_A—Pipe	A Vertical Total Register	
	MMIO				
Address C	Offset: 6000C	h			
Project:	All				
Default Va	alue: 00000	000h			
Access:	R/W				
Size (in bi	ts): 32				
Bit				Description	
31:29	Reserved	Project:	All	Format:	
28:16	Pipe_A_Ver	tical_Total_D	isplay_Lines	Project:	All
	Lines, top/bc required min active, vertic leading edge lines in both	ottom border a us one. Vertio al border, and of the horizo	nd retrace perio cal total needs to the vertical blar ntal sync. For in rlaced modes, h	to 8192 lines encompassing the Vertical Active Display d. The value programmed should be the number of lines be large enough to be greater than the sum of the vertic k regions. The vertical counter is incremented on the terlaced display modes, this indicates the total number of ardware automatically divides this number by 2 to get the	cal f
15:12	Reserved	Project:	All	Format:	
11:0	Pipe_A_Ver	tical_Active_	Display_Lines	Project:	All
	with the desi vertical activ of lines in bo	red number of e area must b	f lines minus one e seven lines. F iterlaced modes	play resolutions up to 4096 lines. It should be programme by When using the internal panel fitting logic, the minimum for interlaced display modes, this indicates the total numb hardware automatically divides this number by 2 to get the	im Der

3.1.1.5 VBLANK_A—Pipe A Vertical Blank Register

	VBLANK_A—Pipe A Vertical Blank Register									
	MMIO									
Address Off	set: 60010	h								
Project:	All									
Default Value	e: 00000	000h								
Access:	R/W									
Size (in bits)	32									
Bit				Description						
31:29	Reserved	Project:	All	Format:						



	VBLANK_A—Pipe	A Vertical Blank Register	
28:16	Pipe_A_Vertical_Blank_End	Project:	All
	number relative to the vertical active displayed line position, where the first active line is etc. The end of vertical blank should be vertical total. This register should be load interlaced display modes, hardware autor	nk End position expressed in terms of the absolute Line olay start. The value programmed should be the VBLANK E considered line 0, the second active line is considered line after the start of vertical blank and before or equal to the ded with the Vactive+BottomBorder+VBlank-1. For matically divides this number by 2 to get the vertical blank e alf lines that get added when operating in modes with half	1,
	The border must be 0, so this register mo Total.	ust always be programmed to the same value as the Vertica	I
15:13	Reserved Project: All	Format:	
12:0	Pipe_A_Vertical_Blank_Start	Project:	All
	relative to the vertical active display star position, where the first active line is con Minimum vertical blank size is required t active. This register is loaded with the V	Ink Start expressed in terms of the absolute line number The value programmed should be the VBLANK Start line sidered line 0, the second active line is considered line 1, et be at least three lines. Blank should start after the end of active+BottomBorder-1. For interlaced display modes, ber by 2 to get the vertical blank start in each field. It does r hen operating in modes with half lines.	
	The border must be 0, so this register me Active.	ust always be programmed to the same value as the Vertica	I

3.1.1.6 VSYNC_A—Pipe A Vertical Sync Register

	MMIC)		
Address O	offset: 60014	-		
Project:	All			
Default Va	lue: 00000	0000h		
Access:	R/W			
Size (in bit	s): 32			
Bit				Description
31:29	Reserved	Project:	All	Format:
28:16	Pipe_A_Ve	ertical_Sync_E	nd	Project: All
	number rela	ative to the vert	ical active of active of active line	ync End position expressed in terms of the absolute Line play start. The value programmed should be the VSYNC End s considered line 0, the second active line is considered line 1, n Vactive+BottomBorder+FrontPorch+Sync-1. For interlaced



	VSYNC_A—Pip	e A Vertical Sync Register
15:13	Reserved Project: All	Format:
12:0		Project: All nc Start position expressed in terms of the absolute line play start. The value programmed should be the VSYNC Start
	line position, where the first active line i etc. This register would be loaded with modes, hardware automatically divides	Vactive+BottomBorder+FrontPorch-1. For interlaced display this number by 2 to get the vertical sync start in each field. It added when operating in modes with half lines.

3.1.1.7 PIPEASRC—Pipe A Source Image Size

			C—Pipe A Source Image	Size		
		MMIO	- -			
Address C	offset:	6001Ch				
Project:		All				
Default Va	lue:	00000000h	1			
Access:		R/W				
Size (in bit	(s):	32				
Double Bu	Iffer Update Point:	Start of ver	tical blank			
Bit			Description			
31:28	Reserved Pro	ject: All		Format:	MBZ	
27:16	Pipe_A_Horizontal	Source_Im	age_Size		Project:	All
	image created by th image size minus o It must represent a	ne display pla ne. size that is a	ntal source image size up to 4096. nes sent to the blender. The value multiple of two (even numbers) wh for this mode, the value programm	programmed sho en driving the LV	ould be the so DS port in tw	ource
	programmed to a va	alue identical	g internal or in an external device, t to the horizontal active. This is the d while the pipe is enabled.			jisters
15:12	Reserved Pro	ject: All		Format:	MBZ	
11:0	Pipe_A_Vertical_S	ource_Image	e_Size		Project:	All
11:0	This 12-bit field spe	ecifies the vert	e_Size tical source image size up to 4096 planes sent to the blender. The va		nines the size	e of
11:0	This 12-bit field spe the image created b source image size r Except in the case	ecifies the vert by the display minus one. of panel fitting	tical source image size up to 4096	alue programmec	nines the size I should be th	e of



3.1.1.8 VSYNCSHIFT_A— Vertical Sync Shift Register

		VSYNCSI	HIFT_A— \	Pertical Sync Shift Register	er	
	MMIO					
Address O	ffset: 60028h	n				
Project:	All					
Default Va	lue: 000000	000h				
Access:	R/W					
Size (in bit	s): 32					
Trusted Ty	v pe: 1					
Bit				Description		
31:13	Reserved	Project:	All	Fo	rmat:	
12:0	Pipe_A_Sec	ond_Field_V	ertical_Sync_	Shift	Project:	All
				nment for the start of the interlaced s the to the horizontal active display sta		sed in
	This value wi	ill only be use	d if the PIPEAC	CONF is programmed to an interlace	ed mode.	
				cal sync should start one pixel after the value of this register should be p		
	(horizontal sy	/nc start - floo	or[horizontal tota	al / 2]).		
	· ·	al horizontal s into the regis		norizontal total values and not the m	inus one values	
			v occurs during ed with horizont	the interlaced second field. In all ot al sync start.	her cases the vertic	al



3.1.2 Pipe A M/N Values

Calculation of TU is as follows: For modes that divide into the link frequency evenly, Active/TU = payload/capacity Please note that this is the same ratio as data m/n: Payload/capacity = dot clk * bytes per pixel / ls_clk * # of lanes

3.1.2.1 PipeADataN1— Pipe A Data N value 1

			Pipe	AData	M1— Pipe A Data M value 1			
Register Ty	<mark>/pe:</mark> M	ЛЮ						
Address Of	f set: 60	030h						
Project:	A							
Default Val	ue: 00	000000h						
Access:	R	N						
Size (in bits	s): 32							
					en two refresh rates, both the M1/N1 o Data M value 1 is used for the higher p Description			
31	Reserve	d F	roject:	All	F	ormat:	MBZ	
24	Reserve	d F	roject:	All	F	ormat:	MBZ	
23:0	Pipe_A	Data_M	value				Project:	All
	This fie	d is the m	n value fo	or intern	al use of the DDA. Calculation of this valu	e is as fo	ollows:	
	Data m	n = dot c	lock * by	/tes pe	pixel / ls_clk * # of lanes			



3.1.2.2 PipeADataM2— Pipe A Data M value 2

		Pipe	ADataM2—	- Pipe A Data	M value 2		
Register T	ype: MMI)					
Address O	ffset: 6003	8h					
Project:	All						
Default Val	ue: 0000	0000h					
Access:	R/W						
Size (in bit	s): 32						
	st be progra	mmed. This v			a and link values and t of vblank. Data M valu		
Dit				Description			
31	Reserved	Project:	All		Format:	MBZ	
24	Reserved	Project:	All		Format:	MBZ	
23:0	Pipe_A_Da	ata_M_value				Project:	All
	This field is	s the m value fo	r internal use c	of the DDA. Calcul	ation of this value is as fo	llows:	
	Data m/n :	= dot clock * b	ytes per pixel	/ ls_clk * # of lane	S		



3.1.2.3 PipeADataN2— Pipe A Data N value 2

		Pipe	ADataN2— Pipe A	A Data N value 2			
Register Ty	pe: MMIO						
Address Off	fset: 6003C	h					
Project:	All						
Default Valu	ue: 00000	000h					
Access:	R/W						
Size (in bits	s): 32						
				ed in conjunction with the and link values and the M			
switching be be programi N value sett	etween two i med. This va	efresh rates	s, both the M1/N1 data s at the beginning of vb	and link values and the M lank. Data N value 2 is u	12/N2	2 link values	s must
switching be	etween two i med. This va	efresh rates	s, both the M1/N1 data s at the beginning of vb	and link values and the M	12/N2	2 link values	s must
switching be be program N value sett Bit	etween two i med. This va	efresh rates	s, both the M1/N1 data s at the beginning of vb	and link values and the M lank. Data N value 2 is u	12/N2 Ised 1	2 link values	s must
switching be be program N value sett Bit 31:24	etween two r med. This va ting.	efresh rates alue updates Project:	s, both the M1/N1 data s at the beginning of vb	and link values and the M lank. Data N value 2 is u	12/N2 Ised 1	2 link values for the lowe	s must
switching be be program N value sett Bit 31:24	etween two i med. This va ting. Reserved Pipe_A_Dat	efresh rates alue updates Project: a_N_value	s, both the M1/N1 data s at the beginning of vb Desc All	and link values and the M lank. Data N value 2 is u	12/N2 ised 1 nat:	2 link values for the lowe MBZ Project:	s must r powe

3.1.2.4 PipeADPLinkM1— Pipe A Link M value 1

	PipeA	DPLinkM1— Pipe A	Link M value 1				
Register Type:	MMIO						
Address Offset:	ffset: 60040h						
Project:	roject: All						
Default Value:	00000000h						
Access:	R/W						
Size (in bits):	32						
1. When switch	ng between two refr programmed. This v	esh rates, both the M1/N	. It is used in conjunction wit I1 data and link values and th nning of vblank. Link M valu	he M2/N2 link			
Bit		Descri	ption				
31:24 Res	erved Project:	All	Format:	MBZ			



PipeADPLinkM1— Pipe A Link M value 1		
Pipe_A_Link_M_value	Project:	All
This field is the m value for external transmission in the Main Stream Attributes. value is as follows:	Calculation of this	
Link m/n = pixel clk / ls_clk		
	This field is the m value for external transmission in the Main Stream Attributes. value is as follows:	This field is the m value for external transmission in the Main Stream Attributes. Calculation of this value is as follows:

3.1.2.5 PipeADPLinkN1— Pipe A Link N value 1

	PipeADPLinkN1— Pipe A Link N value 1		
Register Type:	MMIO		
Address Offset:	60044h		
Project:	All		
Default Value:	0000000h		
Access:	R/W		
Size (in bits):	32		
	ary link data N value used for embedded FDI. It is used in conjunction wit ing between two refresh rates, both the M1/N1 data and link values and the programmed. This value updates at the beginning of vblank. Link N value	he M2/N2 I	ink
alues must be	ing between two refresh rates, both the M1/N1 data and link values and the programmed. This value updates at the beginning of vblank. Link N value	he M2/N2 I	ink
values must be higher power N Bit	ing between two refresh rates, both the M1/N1 data and link values and the programmed. This value updates at the beginning of vblank. Link N value value setting.	he M2/N2 I	ink
values must be higher power N Bit 31:24 Res	ing between two refresh rates, both the M1/N1 data and link values and the programmed. This value updates at the beginning of vblank. Link N value value setting. Description	he M2/N2 I e 1 is used	ink
Alues must be higher power N Bit 31:24 Res 23:0 Pipe This	ing between two refresh rates, both the M1/N1 data and link values and the programmed. This value updates at the beginning of vblank. Link N value value setting. Description served Project: All Format:	he M2/N2 I e 1 is used MBZ Project:	ink for the All



3.1.2.6 PipeADPLinkM2— Pipe A Link M value 2

		PipeA	DPLinkM2—	Pipe A Link M va	alue 2		
Register Ty	pe: MMIO						
Address Off	fset: 60048h	n					
Project:	All						
Default Valu	le: 000000)00h					
Access:	R/W						
Size (in bits)): 32						
				both the M1/N1 data the beginning of vbla			
	r M value set			Description			a for the
ower power Bit			All		Format:	MBZ	
Bit 31:24	r M value set	ting. Project:					All
Bit 31:24	M value set Reserved Pipe_A_Link	tting. Project: t_ M_value he m value fo	All		Format:	MBZ Project:	All
Bit 31:24	M value set Reserved Pipe_A_Link This field is th	tting. Project: x_M_value he m value fo bllows:	All r external transmis	Description	Format:	MBZ Project:	All

3.1.2.7 PipeADPLinkN2— Pipe A Link N value 2

	PipeA	DPLinkN2	2— Pipe A Link	N value 2	
Register Type:	MMIO				
Address Offset	6004Ch				
Project:	All				
Default Value:	00000000h				
Access:	R/W				
Size (in bits):	32				
value 1. When	switching between tw programmed. This va	/o refresh ra	tes, both the M1/N	is used in conjunction 1 data and link values of vblank. Link N value	and the M2/N2 link
Bit			Description		
31:24 Re	served Project:	All		Format:	MBZ



	PipeADPLinkN2— Pipe A Link N value 2		
23:0	Pipe_A_Link_N_value	Project:	Al
	This field is the n value for external transmission in the Main Stream Attributes of this value is as follows (to be filled in):	s and VB-ID. Calcu	lation
	Link m/n = pixel clk / ls_clk		

3.1.3 Pipe B M/N Values

3.1.3.1 PipeBDataM1— Pipe B Data M value 1

			Pipe	BDataM	1— Pipe B	Data M value 1		
Register T	ype: M	/IO						
Address O	offset: 61	030h						
Project:	All							
Default Va	lue: 00	00000h						
Access:	R/	N						
Size (in bit	t s): 32							
See pipe A	descripti	on						
Bit					Descr	iption		
31	Reserve	d Pr	oject:	All			Format:	MBZ
30:25	TU_Size					F	Project:	All
	See pipe	A descrip	otion					
24	Reserve	d Pr	oject:	All			Format:	MBZ
23:0	Pipe_B_	Data_M_v	value			F	Project:	All
	See pipe	A descrip	otion					



3.1.3.2 PipeBDataN1— Pipe B Data N value 1

			Pipe	BDataN1	— Pipe	B Data	N value 1		
Register T	ype:	MMIO							
Address O	ffset:	61034h	n						
Project:		All							
Default Val	lue:	000000)00h						
Access:		R/W							
Size (in bit	s):	32							
See pipe A	descri	iption							
Bit					D	escription			
31:24	Rese	rved	Project:	All			F	ormat:	MBZ
23:0	Pipe_	B_Data	a_N_value				Pr	oject:	All
	See p	ipe A d	escription						

3.1.3.3 PipeBDataM2— Pipe B Data M value 2

		Pipe	BDataM2-	– Pipe B Data M valu	ue 2	
Register T	ype: MMIO					
Address O	ffset: 61038h	ו				
Project:	All					
Default Va	lue: 000000)00h				
Access:	R/W					
Size (in bit	s): 32					
See pipe A	description					
Bit				Description		
31	Reserved	Project:	All		Format:	MBZ
30:25	TU_Size				Project:	All
	See pipe A d	escription				
24	Reserved	Project:	All		Format:	MBZ
23:0	Pipe_B_Data	a_M_value			Project:	All
	See pipe A d	escription				



3.1.3.4 PipeBDataN2— Pipe B Data N value 2

			Pipe	BDataN2-	– Pipe B	Data N v	alue 2	
Register T	ype:	MMIO						
Address O	Offset:	6103C	h					
Project:		All						
Default Va	lue:	00000	000h					
Access:		R/W						
Size (in bit	ts):	32						
See pipe A	desci	ription						
Bit					Descr	iption		
31:24	Rese	erved	Project:	All			Format:	MBZ
23:0	Pipe	_B_Dat	a_N_value				Project:	All
	See	pipe A d	lescription					

3.1.3.5 PipeBDPLinkM1— Pipe B Link M value 1

			PipeB	DPLinkM	1— Pipe B L	ink M value 1		
Register T	ype:	MMIO						
Address O	ffset:	61040ł	า					
Project:		All						
Default Va	lue:	000000)00h					
Access:		R/W						
Size (in bit	ts):	32						
See pipe A	descrip	otion						
Bit					Description	on		
31:24	Rese	rved	Project:	All		Forma	at:	MBZ
23:0	Pipe_	B_Linl	_M_value			Project	:	All
	See p	ipe A d	escription					



3.1.3.6 PipeBDPLinkN1— Pipe B Link N value 1

			PipeB	DPLinkN	11— P	ipe B Linl	k N value 1		
Register T	ype:	MMIO							
Address O	ffset:	61044	n						
Project:		All							
Default Va	lue:	00000	000h						
Access:		R/W							
Size (in bit	s):	32							
See pipe A	desci	ription.							
Bit						Description			
31:24	Rese	erved	Project:	All			F	ormat:	MBZ
23:0	Pipe	_B_Lin	k_N_value				Pr	oject:	All
	See	oipe A d	lescription						

3.1.3.7 PipeBDPLinkM2— Pipe B Link M value 2

			PipeB	DPLinkM	2— Pipe B Li	ink M value 2	
Register Ty	ype: N	IMIO					
Address Of	ffset: 6	1048h	ı				
Project:	A	11					
Default Val	ue: 0	00000)00h				
Access:	R	/W					
Size (in bits	s): 3	2					
See pipe A	descrip	tion					
Bit					Descriptio	on	
31:24	Reserv	ed	Project:	All		Format:	MBZ
23:0	Pipe_B	_Link	_M_value			Project:	All
	See pip	e A d	escription				



3.1.3.8 PipeBDPLinkN2— Pipe B Link N value 2

			PipeB	DPLinkN	12— P	ipe B Link	k N value 2		
Register Type:		MMIO							
Address Offset:		6104C	h						
Project: Default Value:		All							
		00000	000h						
Access:		R/W							
Size (in bit	s):	32							
See pipe A	desci	ription							
Bit						Description			
31:24	Rese	erved	Project:	All			Fo	rmat:	MBZ
23:0	Pipe	_B_Lin	k_N_value				Proj	ect:	All
	See	oipe A d	escription						

3.1.4 Panel Fitter Control Registers

3.1.4.1 **PF_PWR_GATE_CTRL**—Panel Fitter Power Gate Control

ddress Off Project:	set:	68060h				
-						
		DevSNB				
Default Valu	le:	00006453h				
ccess:		R/W				
ize (in bits)):	32				
ouble Buff	er Update Point:	Start of vertical blank after armed				
Double Buffer Armed By:		Write to PFA_WIN_SZ				
Bit		Description				



	PFA	_PWR_GATE_CTR	L—Panel Fitter A Power Gate Control	
15:13	LATE_SI	GNAL_SEQUENCE_STAR	RT Project: All	
			M bank in number of cdclks after the start of power gati er gating on and off conditions.	ing
	Value	Name	Description	Project
	000b	Start time 0	Start time 0	All
	001b	Start time 256	Start time 256	All
	010b	Start time 512	Start time 512	All
	011b	Start time 768	Start time 768	All
	100b	Start time 1024	Start time 1024	All
	101b	Start time 1280	Start time 1280	All
	110b	Start time 1536	Start time 1536	All
	111b	Start time 1792	Start time 1792	All
12	Reserved	Project: All	Format: MB2	Z
11:9	MID_SIG	NAL_SEQUENCE_START	r Project: All	
			M bank in number of cdclks after the start of power gati er gating on and off conditions.	ing
	Value	Name	Description	Project
	000b	Start time 0	Start time 0	All
	001b	Start time 256	Start time 256	All
	010b	Start time 512	Start time 512	All
	011b	Start time 768	Start time 768	All
	100b	Start time 1024	Start time 1024	All
	101b	Start time 1280	Start time 1280	All
	110b	Start time 1536	Start time 1536	All
	111b	Start time 1792	Start time 1792	All
8	Reserved	Project: All	Format: MB2	Z
7:6	Delay bet	GNAL_DELAY ween late signals going int ting on and off conditions.	Project: All to successive RAM banks in number of cdclks. Applical	ble for both
	Value	Name	Description	Project
	00b	Start time 0	Start time 0	All
	01b	Start time 256	Start time 256	All
	10b	Start time 512	Start time 512	All
	1			
	11b	Start time 768	Start time 768	All



4:3	MID_SIG	NAL_DELAY	Project: All	
		tween mid signals going i ting on and off conditions	nto successive RAM banks in number of cdclks. Applicat 3.	ble for both
	Value	Name	Description	Projec
	00b	Start time 0	Start time 0	All
	01b	Start time 256	Start time 256	All
	10b	Start time 512	Start time 512	All
	11b	Start time 768	Start time 768	All
2	Reserved	d Project: All	Format: MB2	7
		•		
1:0	EARLY_	SIGNAL_DELAY	Project: All	
1:0	Delay bet		into successive RAM banks in number of cdclks. Applica	able for
1:0	Delay bet	tween early signals going	into successive RAM banks in number of cdclks. Applica	
1:0	Delay bet both pow	tween early signals going er gating on and off cond	into successive RAM banks in number of cdclks. Applications.	
1:0	Delay bet both pow	tween early signals going er gating on and off cond Name	into successive RAM banks in number of cdclks. Applications.	Projec
1:0	Delay bet both pow Value 00b	tween early signals going er gating on and off cond Name Start time 0	into successive RAM banks in number of cdclks. Applications.	Projec All

PF	B_PWR_G	ATE_C	CTRL—Pa	nel Fitter	B Power G	ate Con	trol
Register Type:		1MIO					
Address Offset:		8860h					
Project:		evSNB					
Default Value:		0006453	3h				
Access:		R/W					
Size (in bits):		2					
Double Buffer Upda	ate Point:	start of v	vertical blank af	ter armed			
Double Buffer Arm	ed By:	Vrite to F	PFA_WIN_SZ				
Bit				Description	n		
31:16 Reserv	ed Proje	t: All				Format:	MBZ



	PFB	_PWR_GATE_CTR	L—Panel Fitter B Power Gate Control	
15:13	LATE_SI	GNAL_SEQUENCE_STAF	RT Project: All	
			M bank in number of cdclks after the start of power gati r gating on and off conditions.	ng
	Value	Name	Description	Project
	000b	Start time 0	Start time 0	All
	001b	Start time 256	Start time 256	All
	010b	Start time 512	Start time 512	All
	011b	Start time 768	Start time 768	All
	100b	Start time 1024	Start time 1024	All
	101b	Start time 1280	Start time 1280	All
	110b	Start time 1536	Start time 1536	All
	111b	Start time 1792	Start time 1792	All
12	Reserved	Project: All	Format: MB2	<u> </u>
11:9	MID_SIG	NAL_SEQUENCE_START	Project: All	
			M bank in number of cdclks after the start of power gation of and off conditions.	ng
	Value	Name	Description	Project
	000b	Start time 0	Start time 0	All
	001b	Start time 256	Start time 256	All
	010b	Start time 512	Start time 512	All
	011b	Start time 768	Start time 768	All
	100b	Start time 1024	Start time 1024	All
	101b	Start time 1280	Start time 1280	All
	110b	Start time 1536	Start time 1536	All
	111b	Start time 1792	Start time 1792	All
8	Reserved	Project: All	Format: MB2	<u> </u>
7:6	Delay bet	GNAL_DELAY ween late signals going intentions on and off conditions.	Project: All o successive RAM banks in number of cdclks. Applicat	ble for both
	Value	Name	Description	Project
	00b	Start time 0	Start time 0	All
	01b	Start time 256	Start time 256	All
	10b	Start time 512	Start time 512	All
		a		1
	11b	Start time 768	Start time 768	All



4:3	MID_SIG	NAL_DELAY	Project: All			
		tween mid signals going i ting on and off conditions	nto successive RAM banks in number of cdclks. Applicat 3.	le for both		
	Value	Name	Description	Project		
	00b	Start time 0	Start time 0	All		
	01b	Start time 256	Start time 256	All		
	10b	Start time 512	Start time 512	All		
	11b	Start time 768	Start time 768	All		
2	Reserve	d Project: All	Format: MB2	2		
1:0	EARLY_SIGNAL_DELAY Project: All					
1.0	Delay between early signals going into successive RAM banks in number of cdclks. Applicable for both power gating on and off conditions.					
			itions.			
			Description	Project		
	both pow	er gating on and off cond		Project All		
	both pow	er gating on and off cond	Description	-		
	both pow Value 00b	er gating on and off cond Name Start time 0	Description Start time 0			

3.1.4.2 **PF_WIN_POS—**Panel Fitter Window Position

	I	PFA_WIN	POS-	-Panel Fitter A Window Position
Register 1	Гуре:	MMI	0	
Address (Offset:	6807	70h	
Project:		All		
Default Va	alue:	0000	0000h	
Access:		R/W		
Size (in bi	ts):	32		
Double Bu	uffer Update Po	oint: Star	t of verti	cal blank after armed
Double Bu	uffer Armed By	: Write	e to PFA	A_WIN_SZ
Bit				Description
31:29	Reserved	Project:	All	Format:
28:16	XPOS	Project:	All	
	The X coordi of horizontal		s) of the	upper left most pixel of the display window. Measured from the end
15:12	Reserved	Project:	All	Format:



		PFA_WIN_POS—Panel Fitter A Window Position
11:0	YPOS	Project: All
		ordinate (in lines) of the upper left most pixel of the display window. Measured from the end to find the Non-Blanked Region (or end of the vertical interval, whatever).

Register Ty	/pe:	MM	10				
Address Of	ffset:	688	68870h				
Project:		All					
Default Val	ue:	000	00000h				
Access:		R/V	/				
Size (in bits):							
Double Buf	fer Update Poi	nt: Sta	t of verti	al blank after armed			
Double Buf	fer Armed By:	Wri	e to PFB	_WIN_SZ			
Bit				Description			
31:29	Reserved	Project:	All	Format:			
28:16	XPOS	Project:	All				
	The X coordina of horizontal b		s) of the	upper left most pixel of the display window. Measured from the end			
15:12	Reserved	Project:	All	Format:			
11:0	YPOS	Project:	All				

]]



3.1.4.3 **PF_WIN_SZ**—Panel Fitter Window Size

Coordinates are determined with a value of (0,0) being the upper left corner of the display device (rotation does not affect this). Writes to the window size arm PF registers for the pipe.

		PFA_W	IN_S	SZ—Panel Fitter A Window Size
Register Ty	ype:	MMI	C	
Address O	ffset:	6807	4h	
Project:		All		
Default Val	lue:	0000	0000	h
Access:		R/W		
Size (in bit	s):	32		
Double Bu	ffer Update P	oint: Start	of ve	rtical blank
Bit				Description
31:29	Reserved	Project:	All	Format:
28:16	XSIZE	Project:	All	
	The horizont	al size in pixel	s of th	ne desired video window.
15:12	Reserved	Project:	All	Format:
11:0	YSIZE	Project:	All	
	The vertical	size in pixels c	f the	desired video window. LSB must be zero for interlaced modes

		PFB_WI	N_SZ	—Panel Fitter B Window Size
Register T	ype:	MMIC)	
Address O		68874	łh	
Project:		All		
Default Val	lue:	00000	0000h	
Access:		R/W		
Size (in bit	s):	32		
Double Bu	ffer Update Po	oint: Start	of vertic	al blank
Bit				Description
31:29	Reserved	Project:	All	Format:
28:16	XSIZE	Project:	All	
	The horizonta	al size in pixels	of the o	desired video window.
15:12	Reserved	Project:	All	Format:
11:0	YSIZE	Project:	All	
	The vertical s	size in pixels of	the des	ired video window. LSB must be zero for interlaced modes



3.1.4.4 **PF_CTRL_1—Panel Fitter Control 1**

		PF	A_CTRI	_1—Panel Fitter A Control	1			
Register 1	Гуре:	Ν	/MIO					
Address (6	8080h					
Project:		ŀ	All					
Default Va	alue:		0000000h					
Access:			R/W					
Size (in bi			32 Start of vort	ical blank after armed				
	uffer Update uffer Armed			A_WIN_SZ				
Bit		.		Description				
31	Enable_F	Pipe_Scaler						
	Project:	-	All					
	Default Value: 0b							
	Value	Value Name		Description	Project			
	0b	Disable		Data bypasses the scaler	All			
	1b	1b Enable T		The scaler is enabled	All			
30	Reserved	1						
29	Reserved	1						
28	Reserved	ł						
27	VADAPT Project: All							
	Puts the adaptive vertical filter into adaptive mode, intended for use in interlace output modes only.							
	Value	Name	Descript	tion	Project			
	0b	Disable	Adaptive	filtering disabled	All			
	1b	Enable	Adaptive	filtering enabled	All			
26:25	-	VADAPT_MODE Project: All						
	Puts the a	adaptive verti	cal filter into	o adaptive mode, intended for use in int	erlace output modes only.			
	Value	Name		Description	Project			
	00b	Least Adap	tive	Least Adaptive (Recommended)	All			
	01b	Moderately	Adaptive	Moderately Adaptive	All			
	10b	Reserved		Reserved	All			
	11b	Most Adapt	ive	Most Adaptive	All			



24:23	FILTER_	FILTER_SELECT Project: All							
	Filter coe	Filter coefficient selection							
	Value	Name		Description	Project				
	00b			Programmed Coefficients (Recommended)	All All All				
	01b			Hardcoded Coefficients for Medium 3x3 Filtering					
	10b			Hardcoded Coefficients for Edge Enhancing 3x3 Filtering					
	11b	Edge Softe	n	Hardcoded Coefficients for Edge Softening 3x3 Filtering	All				
22	CHR_PREF Project: All Chroma Pre-filter enable. Can be used to further reduce chroma bandwidth in TV modes.								
	Chroma I	Pre-filter enab	ole. Car	n be used to further reduce chroma bandwidth in TV modes.					
	Chroma I	Pre-filter enat		n be used to further reduce chroma bandwidth in TV modes. cription	Project				
		1	Desc		Project				
	Value	Name	Desc Pre-f	ription					
21	Value 0b	Name Disable Enable	Desc Pre-f	cription ilter disabled	All				
21	Value Ob 1b	Name Disable Enable	Desc Pre-f	cription ilter disabled	All				



		PF	B_CTR	L_1	—Panel Fitter B Control 1				
Register 1	Гуре:	Ν	/MIO						
Address (6	8880h						
Project:	All								
Default Va	alue: 00000000h								
Access:			R/W						
Size (in bi		-	2						
	uffer Update uffer Armed		Start of ver Vrite to PF		blank after armed				
Bit		by. v		-D_VV	Description				
31	Enable F	Pipe_Scaler							
01	Project:		All						
	Default Va	alue.	0b						
	Value	Name	00	Dos	scription	D	oject		
					•		-		
	0b	Disable		Data	a bypasses the scaler	AI			
	1b	Enable		The	scaler is enabled	AI	I		
30	Reserved	ł							
29	Reserved	1							
28	Reserved	1							
27	VADAPT		Projec	ct:	All				
	Puts the a	adaptive vertion	cal filter in	to ad	aptive mode, intended for use in interlace output	ut modes	only.		
	Value	Name	Descrip	otion			Project		
	0b	Disable	Adaptive	e filte	ring disabled		All		
	1b	Enable	Adaptive	e filte	ring enabled		All		
26:25	VADAPT	MODE	Projec	ct:	All		• •		
	Puts the a	adaptive vertion	cal filter in	to ad	aptive mode, intended for use in interlace output	ut modes	only.		
	Value Name Description Project								
	00b	Least Adap	tive	T	Least Adaptive (Recommended)		All		
	01b	Moderately	Adaptive		Moderately Adaptive		All		
	10b	Reserved			Reserved		All		
	11b	Most Adapt	ive		Most Adaptive		All		



24:23		SELECT		ject: All				
	Value	Name		Description	Project			
	00b	Programm	ed	Programmed Coefficients (Recommended)	All			
	01b	Hardcodec	Med	Hardcoded Coefficients for Medium 3x3 Filtering	All			
	10b	Edge Enha	ance	Hardcoded Coefficients for Edge Enhancing 3x3 Filtering	All			
	11b	11b Edge Soften Hardcoded Coefficients for Edge Softening 3x3 Filtering						
22	CHR_PR Chroma I			ject: All n be used to further reduce chroma bandwidth in TV modes.				
	Value	Name	Desc	cription	Project			
	0b	Disable	Pre-f	ilter disabled	All			
	1b	Enable	Pre-f	ilter enabled	All			
21	Reserve	d						
		d						

3.1.5 Panel Fitter Coefficient Registers

Coefficients for the panel fitter filters are stored in sign-exponent-mantissa format. The number of mantissa bit varies based on the filter. There are three exponent bits but not all values are allowed, ranges are specified per filter. Two filter coefficients are stored in each dword, the tables below show the data packing in each of the words. Unused bits are considered reserved and should be written zero. The default value of all coefficient registers is 00000000h. Coefficients greater than 1.0 are only allowed in the center tap of the filter, center coeffs can not use the "100" exponent.

	Panel Fitter Coefficient Definition										
Project:	All										
Bit		Description									
15	Sign_bit Project:	A	Ι								
	Value	Name	Description	Project							
	0b	Positive	Positive	All							
	1b	Negative	Negative	All							
	-			i							

For RGB modes the Luma and Chroma filter coeffs are programmed with the same values.



		Pa	nel F	itter Coefficient Definition	
14	Reserved	Project:	All	Form	nat: MBZ
13:12	Exponent_	bits			
	Project:		All		
	The meanir	ng of the expon	ent bits	varies for center tap or non-center tap coeffic	ients.
	Value	Name		Description	Project
	00b	2 or 0.125		Center taps: 2 or mantissa is b.bbbbbb	All
				Non-center taps: 0.125 or mantissa is 0.000bbbbbbb	
	01b	1		1 or mantissa is 0.bbbbbbbb	All
	10b	0.5		0.5 or mantissa is 0.0bbbbbbbb	All
	11b	0.25		0.25 or mantissa is 0.00bbbbbbbb	All
	others	Reserved		Reserved	All
11:3	Center tap	mantissa varies coefficients u	use all s	All on the filter, but the MSB of the mantissa is a 9 bits of mantissa. Ily the upper 7 bits of mantissa and the lower a	
2:0	Reserved	Project:	All	Form	nat: MBZ



3.1.6 Panel Fitter Horizontal Coefficients

Coefficients are packed in the horizontal coefficient registers as follows (with the letter representing the tap and the number representing the coefficient set):

Address	bits [31:16]	bits[15:0]	
68x00	BO	A0	
68x04	D0	CO	
68x08	F0	E0	
68x0C	A1	GO	
68x10	C1	B1	

etc....

3.1.6.1 **PF_HFILTL_COEF**—Panel Fitter Horizontal Luma/Red Coefficients

Р	FA_HF		anel Fitter	AH	orizontal L	uma/Red Coefficients
Register Ty	pe: MN	/IO				
Address Of	fset: 68	100h				
Project:	All					
Default Val	ue: 000	00000h				
Access:	R/\	N				
Size (in bits	s): 602	k 32				
17 phases of Center coef Other coeff	fficient is	-				
DWord	Bit				Description	
059	31:16	Coefficient2	Project:	All	Format:	Panel Fitter Coefficient Definition
	15:0	Coefficient1	Project:	All	Format:	Panel Fitter Coefficient Definition



Р	FB_HF	FILTL_COEF—P	anel Fitter	BH	orizontal L	uma/Red Coefficients
Register Ty	v <mark>pe:</mark> N	IMIO				
Address Of	fset: 6	8900h				
Project:	A	II				
Default Val	ue: 0	000000h				
Access:	R	/W				
Size (in bits	s): 6	0x32				
17 phases of	of 7 taps	s require 60 dwords				
Center coef	fficient is	s 1.2.9				
Other coeff	icients a	re 1.2.7				
DWord	Bit				Description	
059	31:16	Coefficient2	Project:	All	Format:	Panel Fitter Coefficient Definition
	15:0	Coefficient1	Project:	All	Format:	Panel Fitter Coefficient Definition

3.1.6.2 **PF_HFILTC_COEF—Panel Fitter Horizontal Chroma/Green and Blue** Coefficients

PFA_HFI		OEF—Panel	Fitter .	A Hor	izonta	al Chroma	/Green and Blue Coefficients
Register Ty	/pe: M	OIN					
Address Of	f set: 68	200h					
Project:	Al						
Default Val	ue: 00	000000h					
Access:	R/	W					
Size (in bits	s): 60	x32					
17 phases	of 7 taps	require 60 dword	ds				
Center coef	fficient is	1.2.9					
Other coeff	icients a	e 1.2.7					
DWord	Bit					Description	
059	31:16	Coefficient2	F	Project:	All	Format:	Panel Fitter Coefficient Definition
	15:0	Coefficient1	F	Project:	All	Format:	Panel Fitter Coefficient Definition



PFB_HF		OEF—Panel Fi	tter B Hori	zont	al Chroma	/Green and Blue Coefficients
Register Ty	/pe: M	MIO				
Address Of	f set: 68	BA00h				
Project:	AI	I				
Default Val	ue: 00)000000h				
Access:	R/	W				
Size (in bits	s): 60)x32				
17 phases	of 7 taps	require 60 dwords				
Center coet	fficient is	s 1.2.9				
Other coeff	icients a	re 1.2.7				
DWord	Bit				Description	
059	31:16	Coefficient2	Project:	All	Format:	Panel Fitter Coefficient Definition
	15:0	Coefficient1	Project:	All	Format:	Panel Fitter Coefficient Definition

3.1.7 Panel Fitter Vertical Coefficients

Coefficients are packed in the vertical coefficient registers as follows (with the letter representing the tap and the number representing the coefficient set). When the vertical filter is in 3 line mode the three taps used are A, C & E, B & C must be programmed to zero in three line mode.

Address	bits [31:16]	bits[15:0]
68x00	B0	A0
68x04	D0	CO
68x08	A1	E0
68x0C	C1	B1
68x10	E1	D1

etc....



3.1.7.1 **PF_VFILTL_COEF**—Panel Fitter Vertical Luma/Red Coefficients

	PFA_	VFILTL_COEF	-Panel Fitte	er A	Vertical Lu	Ima/Red Coefficients
Register Ty	vpe: N	MMIO				
Address Of	fset: 6	68300h				
Project:	ŀ	All				
Default Val	ue: ()0000000h				
Access:	F	R/W				
Size (in bits	s): 4	13x32				
17 phases of Center coef Other coeff	ficient		ls			
DWord	Bit				Description	
042	31:16	6 Coefficient2	Project:	All	Format:	Panel Fitter Coefficient Definition
	15:0	Coefficient1	Project:	All	Format:	Panel Fitter Coefficient Definition

PFB_VF	FILTC_	COEF—Panel F	itter B Ve	rtica	I Chroma/	Green and Blue Coefficients			
Register Ty	pe: MN	/IO							
Address Of	fset: 680	C00h							
Project:	All								
Default Valu	Je: 000	00000h							
Access:	R/\	W							
Size (in bits): 43)	k 32							
17 phases of Center coef Other coeffi	ficient is	-							
DWord	Bit		Description						
042	31:16	Coefficient2	Project:	All	Format:	Panel Fitter Coefficient Definition			
	15:0	Coefficient1	Project:	All	Format:	Panel Fitter Coefficient Definition			



3.1.7.2 **PF_VFILTC_COEF**—Panel Fitter Vertical Chroma/Green and Blue Coefficients

PFA_VF	ILTC_O	COEF—Panel F	itter A Ve	rtica	I Chroma/	Green and Blue Coefficients
Register Ty	pe: MM	IIO				
Address Of	f <mark>set:</mark> 684	00h				
Project:	All					
Default Valu	le: 000	00000h				
Access:	R/V	V				
Size (in bits): 43x	32				
17 phases c	of 5 taps r	equire 43 dwords				
Center coef	ficient is '	1.2.9				
Other coefficient	cients are	e 1.2.7				
DWord	Bit				Description	
042	31:16	Coefficient2	Project:	All	Format:	Panel Fitter Coefficient Definition
	15:0	Coefficient1	Project:	All	Format:	Panel Fitter Coefficient Definition

PFB_VF	ILTC_	COEF—Panel F	itter B Ve	rtica	I Chroma/	Green and Blue Coefficients
Register Ty	pe: Mi	OIN				
Address Of	fset: 68	C00h				
Project:	All					
Default Valu	le: 00	000000h				
Access:	R/	W				
Size (in bits): 43	x32				
17 phases c	of 5 taps	require 43 dwords				
Center coef	ficient is	1.2.9				
Other coeffi	cients ar	e 1.2.7				
DWord	Bit				Description	
042	31:16	Coefficient2	Project:	All	Format:	Panel Fitter Coefficient Definition
	15:0	Coefficient1	Project:	All	Format:	Panel Fitter Coefficient Definition

3.1.8 FDI AFE Control (6C000h–6DFFFh)

Documented separately



4. Plane Controls (70000h–7FFFFh)

4.1.1 Display Pipeline A

4.1.1.1 PIPEA_DSL—Pipe A Display Scan Line

		P	IPEA_DSL—Pipe A Display Scan Line	
Register T	ype: MN	110		
Address O	ffset: 700	00h		
Project:	All			
Default Val	lue: 000	00000h		
Access:	Rea	ad Only		
Size (in bit	s): 32			
leading ed of the displ	ge of HSY ay. In inte ve a total	NC and ca erlaced dis number of	back of the display pipe vertical "line counter". The value increan be safely read any time. The value resets to line zero at the play timings, the scan line counter provides the current line in a lines that is one greater than the other field. Content locked c displayed.	first active line he field. One
Bit			Description	
31	Current_	Field		
	Project:		All	
	Default V	alue:	0	
	Provides	read back o	of the current field being displayed on display pipe A.	
	Value	Name	Description	Project
	0b	Odd	First field (odd field)	All
	1b	Even	Second field (even field)	All
30:13	Reserved	d Proj	ect: All Format:	
12:0	Line_Co	unter_for_	Display Pro	ject: All
			of the display pipe A vertical line counter. This is an indication of the used by software to synchronize with the display.	current



4.1.1.2 PIPEA_SLC—Pipe A Display Scan Line Count Range Compare

PI	PEA_SLC—Pipe A Display Scan Line Count Range Compare
Register Type:	MMIO
Address Offset:	70004h
Project:	All
Default Value:	0000000h
Access:	R/W
Size (in bits):	32
DaveNP1 The a	can line number register is compared with the display line value from the pipe timing

[DevSNB] The scan line number register is compared with the display line value from the pipe timing generator. The result of this comparison is used to generate interrupts and render responses. The value programmed should be desired value – 1, so for line 0, the value programmed is VTOTAL, and for line 1, the value programmed is 0. Content locked display will adjust the total number of lines displayed.

[ILK] The Top and Bottom Line Count Compare registers are compared with the display line values from pipe A timing generator. The Top compare register operator is a less than or equal, while the Bottom compare register operator is a greater than or equal. The results of these 2 comparisons are used to generate interrupts. For range check, the value programmed should be the (desired value – 1), so for line 0, the value programmed is 0. Content locked display will adjust the total number of lines displayed.

Bit				Description		
31	Inclusive	/Exclusive				
	Project:		_K			
	Default Va	alue: 0	b			
	Value	Name	Description			Project
	0b	Exclusive	Exclusive: outsid	e of the range		All
	1b	Inclusive	Inclusive: within t	he range		All
30:29	Reserved	l	Project:	ILK	Forma	t: MBZ
28:16	Start_Sca	an_Line_Number	Project:	ILK	Forma	t:
	Range:		0Vertica	I Total		
	This field	specifies the start	ing scan line numb	er of the Scan Line Window.		
	Scan line	0 is the first line c	f the display frame			
15:13	Reserved	l	Project:	ILK	Forma	t: MBZ
12:0	End_Sca	n_Line_Number	Project:	ILK	Forma	t:
	Range:		0Vertical Tota	l		
	This field	specifies the endi	ng scan line numbe	er of the Scan Line Window.		
	Scan line	0 is the first line c	f the display frame			
31:13	Reserved	l	Project:	DevSNB	Forma	t: MBZ



	PIPEA_SL	C—Pipe A Display Scan Line Count Range Compare
12:0	Scan_Line_Nun	nber
	Project:	DevSNB
	Range	0Vertical Total
	This field specifie	es the scan line number on which to generate scan line interrupt and render response.



4.1.1.3 **PIPEACONF**—Pipe A Configuration Register

		PIPEACON		ister
Register 1	Гуре:	MMIO		
Address (70008h		
Project:		All		
Default Va	alue:	0000000	h	
Access:		R/W		
Size (in bi	its):	32		
Double B	uffer Update	Point: Start of ve	ertical blank OR pipe disabled	
Bit			Description	
31	Pipe_A_Er	nable		
	Project:	All		
	Default Val	ue: Ob		
	have been Synchroniz	disabled. Turning th ation pulses to the d	ero should only be done when all planes e pipe enable bit off disables the timing isplay are not maintained if the timing ge lid values before this bit is enabled.	generator in this pipe.
	Value	Name	Description	Project
	0b	Disable	Disable	All
	1b	Enable	Enable	All
30		All ue: 0b icates the actual stat	e of the pipe. Since there can be some	
			ng off, this bit indicates the true current	
	Value	Name	Description	Project
	0b	Disable	Disable State	All
	1b	Enable	Enable State	All
29	Reserved	Project: All		Format:
28:27	Reserved			
26	Reserved			
26	Reserved	Project: De	vILK	Format:
20	Itesel veu			i onnat:



25:24	Pipe A	Palette/Gamn	na_Unit_Mode	
	Project:		All	
	Default V	alue:	Ob	
	Registers	s select which for informatio unaffected by	mode the pipe gamma correction logic works in. See the Display Pa n on the different palette/gamma modes. Other gamma units such a this bit.	alette s in the
	Value	Name	Description	Project
	00b	8 bit	8-bit Legacy Palette Mode	All
	01b	10 bt	10-bit Precision Palette Mode	All
	10b	12 bit	12-bit Interpolated Gamma Mode	All
	11b	Reserved	Reserved	All
23:21	Interlace	d Mada		
-	Internace	a_inioae		
-	Project:	a_mode	All	
-			All Ob	
-	Project: Default V These bit	alue: s are used for		ely if the
-	Project: Default V These bit pipe is of	alue: s are used for f, or in the ver	0b software control of interlaced behavior. They are updated immediate	ely if the
-	Project: Default V These bit pipe is of	alue: s are used for f, or in the ver	0b software control of interlaced behavior. They are updated immediate tical blank after programming if pipe is enabled.	-
-	Project: Default V These bit pipe is of Note: VG	alue: s are used for f, or in the vert A display mo	0b software control of interlaced behavior. They are updated immediate tical blank after programming if pipe is enabled. odes do not work while in interlaced fetch modes	-
-	Project: Default V These bit pipe is off Note: VG Value	alue: s are used for f, or in the vert A display mo Name	0b software control of interlaced behavior. They are updated immediate tical blank after programming if pipe is enabled. odes do not work while in interlaced fetch modes Description	Project
	Project: Default V These bit pipe is off Note: VG Value 000b	alue: s are used for f, or in the ver 5A display mo Name PF-PD	Ob software control of interlaced behavior. They are updated immediate tical blank after programming if pipe is enabled. odes do not work while in interlaced fetch modes Description Progressive Fetch / Progressive display Progressive Fetch / Interlaced display (TV) Requires panel	Project All
	Project: Default V These bit pipe is of Note: VG Value 000b 001b	alue: s are used for f, or in the vert A display mo Name PF-PD PF-ID	Ob software control of interlaced behavior. They are updated immediate tical blank after programming if pipe is enabled. odes do not work while in interlaced fetch modes Description Progressive Fetch / Progressive display Progressive Fetch / Interlaced display (TV) Requires panel fitting to be enabled	Project All All
	Project: Default V These bit pipe is off Note: VG Value 000b 001b 010b	alue: s are used for f, or in the vert 5A display mo Name PF-PD PF-ID Reserved	Ob software control of interlaced behavior. They are updated immediate tical blank after programming if pipe is enabled. odes do not work while in interlaced fetch modes Description Progressive Fetch / Progressive display Progressive Fetch / Interlaced display (TV) Requires panel fitting to be enabled Reserved Interlaced Fetch / Interlaced display (programmable sync,	Project All All All All
	Project: Default V These bit pipe is of Note: VG Value 000b 001b 010b 011b	alue: s are used for f, or in the vert A display mo Name PF-PD PF-ID Reserved IF-ID	Ob software control of interlaced behavior. They are updated immediate tical blank after programming if pipe is enabled. odes do not work while in interlaced fetch modes Description Progressive Fetch / Progressive display Progressive Fetch / Interlaced display (TV) Requires panel fitting to be enabled Reserved Interlaced Fetch / Interlaced display (programmable sync, normal interlaced) Interlaced embedded panel with interlaced fetch (pixel	Project All All All All All



20	Display_	Power_Mo	ode_Switch				
	Project: All						
	Default V	alue:	Ob				
	power sa	vings mode	oftware to set the power saving progressive mode. The pipe enters or exe on the vblank after this bit is written. Please note that bits 17:16 of this order for this bit to take effect.				
	Value	Name	Description	Projec			
	0b	Progress	ive Pipe is in progressive mode	All			
	1b	Power sa	Ave Pipe is in power savings progressive mode	All			
19	Reserve	d: Must be	e zero				
18	Reserve	d: Must be	e zero				
7:16	Refresh	Rate_CxS	R_Mode_Association				
7:16	Refresh_ Project:	_Rate_CxS	R_Mode_Association				
7:16	Project: Default V These bit anything	alue: s select ho other than	All 0b w refresh rates are tied to big FIFO mode on pipe A. When they are set 00, bits 23:21 of this register must be programmed to 000. Switching bel	ween 01			
7:16	Project: Default V These bit anything and 10 se Software correspon	alue: s select ho other than ettings direc is responsi nding mode	All Ob w refresh rates are tied to big FIFO mode on pipe A. When they are set 00, bits 23:21 of this register must be programmed to 000. Switching bet ctly is not allowed. Software must program this field to 00 before switchin ible for enabling this mode only for integrated display panels that support a.	ween 01 g.			
7:16	Project: Default V These bit anything and 10 se Software correspon	alue: s select ho other than ettings direct is responsion nding mode Name	All Ob w refresh rates are tied to big FIFO mode on pipe A. When they are set 00, bits 23:21 of this register must be programmed to 000. Switching bet ctly is not allowed. Software must program this field to 00 before switchin ible for enabling this mode only for integrated display panels that support e. Description	ween 01 g. Projec			
7:16	Project: Default V These bit anything and 10 se Software correspon	alue: s select ho other than ettings direc is responsi nding mode	All Ob w refresh rates are tied to big FIFO mode on pipe A. When they are set 00, bits 23:21 of this register must be programmed to 000. Switching bet ctly is not allowed. Software must program this field to 00 before switchin ible for enabling this mode only for integrated display panels that support a.	ween 01 g.			
7:16	Project: Default V These bit anything and 10 se Software correspon	alue: s select ho other than ettings direct is responsion nding mode Name	All Ob w refresh rates are tied to big FIFO mode on pipe A. When they are set 00, bits 23:21 of this register must be programmed to 000. Switching bet ctly is not allowed. Software must program this field to 00 before switchin ible for enabling this mode only for integrated display panels that support be Description No dynamic refresh rate change enabled. Software control through	ween 01 g. Projec			



		PIPE	ACONF—Pipe A Configuration	on Register	
15:14	Display_	Rotation_In	fo		
	Project:		All		
	Default V	alue:	0b		
			bits set by software to indicate this pipe re and software rotation cases. Hardwar		
	Value	Name	Description		Project
	00b	None	No rotation on this pipe		All
	01b	90	90° rotation on this pipe		All
	10b	180	180° rotation on this pipe		All
	11b	270	270° rotation on this pipe		All
13	Color_R	ange_Select			
	Project:		All		
	Default V	alue:	Ob		
	This bit is	s used to sele	ct the color range of outputs.		
	Value	Name	Description		Project
	0b	Full	Apply full 0-2 ⁿ - 1 color range to the outp	out	All
	1b	CE	Apply CE color range to the output		All
12:11	Pipe out	tout color s	pace_select		
	Project:	-h	All		
	Default V	alue:	0b		
		he ports of th what is seled	e pipe output color space. Plane data fo ted here.	rmats and CSC need to be pro	grammed
	Value	Name	Description		Project
	00b	RGB	RGB		All
	01b	YUV 601	YUV 601		All
	10b	YUV 709	YUV 709		All
	11b	Reserved	Reserved		All
10:9	Reserve	d			•
10:9	Reserve	d Projec	ct: DevILK	Format:	
8	Reserve	d Proje	xt: All	Format: MBZ	



		PIPE	ACONF—Pipe A Configuration Register	
7:5	Bits_Per	Color		
	Project:		All	
	Default V	alue:	0b	
	format ta a pixel cl Software	kes place or ock change. should enat	number of bits per color sent to a receiver device connected to this the Vblank after being written. Color format change can be done ole dithering in the pipe/port if selecting a pixel color depth higher o of the frame buffer.	independent of
	Value	Name	Description	Project
	000b	8 bits	8 bits per color	All
	001b	10 bits	10 bits per color	All
	010b	6 bits	6 bits per color	All
	011b	12 bits	12 bits per color	All
	1XXb	Reserved	Reserved	All
	Project: Default V This bit e	alue: nables dithe	All Ob ring	
	Value	Name	Description	Project
	0b	Disable	Dithering disabled	All
	1b	Enable	Dithering enabled	All
3:2	Dithering Project: Default V These bit		All Ob ering type.	
	Value	Name	Description	Project
	00b	Spatial	Spatial only	All
	01b	ST1	Spatio-Temporal 1	All
	10b	Reserved	Reserved	All
	11b	Reserved	Reserved	All
1	Reserve	d		
	1			



4.1.2 Display Pipeline A Counters and Timestamps

4.1.2.1 **PIPEA_FRMCOUNT—Pipe A Frame Counter**

Register Type:		MMIO			
Address Offset: Project:		70040h			
		All			
Default Va	alue:	00000000h			
Access:		Read Only			
Size (in bi	its):	32			
Bit					Description
31:0	Pipe	_Frame_Counter	Project:	All	Format:
		ides read back of th cal blank and rolls o			counter. This counter increments on every start of \32 frames.

4.1.2.2 PIPEA_FLIPCOUNT—Pipe A Flip Counter

PIPEA_FLIPCOUNT—Pipe A Flip Counter							
Register Type:		MMIO					
Address O	ffset:	70044h					
Project:		All					
Default Val	lue:	0000000h					
Access:		Read Only					
Size (in bit	s):	32					
Bit		Description					
31:0	Pipe	_Flip_Counter Project: All Format:					
	of the	des read back of the display pipe flip counter. This counter increments on each flip of the surface primary plane on this pipe. This includes command streamer asynchronous and synchronous and any MMIO writes to the primary plane surface address. It rolls over back to 0 after 2^32 flips.					



4.1.2.3 **PIPEA_FRMTIMESTAMP—Pipe A Frame Time Stamp**

		PIPEA_FRMTIMESTAMP—Pi	i <mark>pe A Frame T</mark> i	ime St	amp	
Register T	уре:	MMIO				
Address Offset:		70048h				
Project:		All				
Default Value:		0000000h				
Access:		Read Only				
Size (in bi	ts):	32				
Bit		De	scription			
31:0	Pipe	_Frame_Time_Stamp	F	Project:	All	Format:
		ides read back of the display pipe frame time of vertical blank. The TIMESTAMP register I				

4.1.2.4 **PIPEA_FLIPTIMESTAMP—Pipe A Flip Time Stamp**

		PIPEA_FLIPTIMESTAMP—Pipe	A Flip Time Stamp
Register Type:		MMIO	
Address Offset:		7004Ch	
Project:		All	
Default Value:		0000000h	
Access:		Read Only	
Size (in bit	s):	32	
Bit		Descripti	ion
31:0	Pipe	_Flip_Time_Stamp	Project: All Format:
	of the sync	des read back of the display pipe flip time stamp. e surface of the primary plane on this pipe. This inc hronous flips and any MMIO writes to the primary pl ter has information on the time stamp value.	cludes command streamer asynchronous and



4.1.3 Display Timestamp

This register provides an elapsed real-time value that can be used as a timestamp for GPU events over short periods of time.

The register counts at a constant frequency by adjusting the increment amount according to the actual core display clock frequency. SW therefore does not need to know the reference clock frequency.

4.1.3.1 TIMESTAMP_HI—Time Stamp High Value

		ТІМ	ESTAMP_	HI—Ti	me Stamp High Value
Register 1	Гуре:	MMIO			
Address Offset:		70070h			
Project:		All			
Default Value:		00000000h			
Access:		R/W Clear			
Size (in bi	its):	32			
Bit					Description
31:0	TIME	STAMP_High	Project:	All	Format:
	regist	ers when flips oc	cur, and in the	Pipe Fra	e value in this field is latched in the Pipe Flip TIMESTAMP ame TIMESTAMP registers at start of vertical blank. The to it. The register is not reset by a graphics software



4.1.4 Display Pipeline B

4.1.4.1 PIPEB_DSL—Pipe B Display Scan Line

		PIPEB	_DSL—Pipe B D	isplay Scan I	Line	
Register T	ype: MM	0				
-	Offset: 710	00h				
Project:	All					
Default Va	alue: 000	00000h				
Access:	Rea	d Only				
Size (in bi	-					
See Pipe /	A descriptio	n				
Bit			Des	cription		
31	Current_I	Field				
	Project:	A	All			
	Default Va	alue: C	b			
	Provides	read back of the o	current field being displa	yed on display pip	e B.	
	Value	Name	Description			Project
	0b	First	First field (odd fie	ld)		All
	1b	Second	Second field (eve	en field)		All
30:13	Reserved			Project:	All Format:	MBZ
12:0	Line_Cou	nter_for_Display	y	Project:	All Format:	
	See pipe	A description.				



4.1.4.2 **PIPEB_SLC**—Pipe B Display Scan Line Count Range Compare

	PIPEB	SLC-P	ipe B C	Display Scan Line Count Range Compare		
Register T Address O Project: Default Va	ype: MMI offset: 7100 All	0				
Access:	R/W					
Size (in bit	s): 32					
See Pipe A	A description	n				
Bit				Description		
31	Inclusive/	Exclusive				
	Project:		All			
	Default Va	lue:	0b			
	Value	Name	Descrip	tion	Project	
	0b	Exclusive	Exclusive: outside of the range All			
	1b	Inclusive	Inclusive	e: within the range	All	
30:29	Reserved	Project:	All	Format:		
28:16	Start_Sca	n_Line_Num	ber			
	Project:		All			
	Default Va	lue:	0b			
	Format:		U13	Scan lines, where scan line 0 is the first line of the display	frame.	
	Range		0Disp	lay Buffer height in lines-1		
	See pipe A	A description				
15:13	Reserved	Project:	All	Format:		
12:0	End_Scan	_Line_Numb	ber			
	Project:		All			
	Default Va	lue:	0b			
	Format:		U13	Scan lines, where scan line 0 is the first line of the display	frame.	
	Range		0Disp	lay Buffer height in lines-1		
	See pipe A	A description				



4.1.4.3 **PIPEBCONF**—Pipe B Configuration Register

		PIPEBCONF	-Pipe B Configuration Regist	ter				
Register T	ype:	MMIO						
Address O	ffset:	71008h						
Project:		All	All					
Default Val	lue:	0000000	h					
Access:		R/W						
Size (in bit	s):	32						
Double Bu	ffer Update	Point: Start of ve	rtical blank OR pipe disabled					
Bit			Description					
31	Pipe_B_Er	able						
	Project:	All						
	Default Val	ue: Ob						
	on this pipe. Changing it to a zero should only be done when all planes that are assigned to this pipe have been disabled. Turning the pipe enable bit off disables the timing generator in this pipe. Synchronization pulses to the display are not maintained if the timing generator is disabled. Pipe timing registers must contain valid values before this bit is enabled.							
	Value	Name	Description	Project				
	0b	Disable	Disable	All				
	1b	Enable	Enable	All				
30		All ue: 0b cates the actual state	e of the pipe. Since there can be some delang off, this bit indicates the true current sta					
	Value	Name	Description	Project				
	0b	Disable	Disable	All				
	1b	Enable	Enable	All				
29	Reserved	Project: All		Format:				
29 28:27	Reserved Reserved	Project: All		Format:				
		Project: All		Format:				



25:24	Pipe B	Palette/Gamn	na Unit Mode						
20.21	Pipe_B_Palette/Gamma_Unit_Mode Project: All								
	Default Value: 0b								
	These bits select which mode the pipe gamma correction logic works in. See the Display Palette Registers for information on the different palette/gamma modes. Other gamma units such as in the sprite are unaffected by this bit.								
	Value	Name	Description	Project					
	00b	8 bit	8-bit Legacy Palette Mode	All					
	01b	10 bit	10-bit Precision Palette Mode	All					
	10b	12 bit	12-bit Interpolated Gamma Mode	All					
	11b	Reserved	Reserved	All					
23:21	Interlaced_Mode								
20.21	internace	a_woae							
20.21	Project:	a_wode	All						
20.21			All Ob						
20.21	Project: Default V These bit	alue: s are used for	0b software control of interlaced behavior. They are updated immediate	ely if the					
20.21	Project: Default V These bit pipe is of	alue: s are used for f, or in the ver	Ob	ely if the					
20.21	Project: Default V These bit pipe is of	alue: s are used for f, or in the ver	0b software control of interlaced behavior. They are updated immediate ical blank after programming if pipe is enabled.	-					
20.21	Project: Default V These bit pipe is of Note: VG	alue: s are used for f, or in the ver A display mo	0b software control of interlaced behavior. They are updated immediate ical blank after programming if pipe is enabled. odes do not work while in interlaced fetch modes	-					
20.21	Project: Default V These bit pipe is of Note: VG Value	alue: s are used for f, or in the ver A display mo Name	0b software control of interlaced behavior. They are updated immediate ical blank after programming if pipe is enabled. odes do not work while in interlaced fetch modes Description	Project					
20.21	Project: Default V These bit pipe is off Note: VG Value	alue: s are used for f, or in the ver 5A display mo Name PF-PD	Ob software control of interlaced behavior. They are updated immediate tical blank after programming if pipe is enabled. odes do not work while in interlaced fetch modes Description Progressive Fetch / Progressive display Progressive Fetch / Interlaced display (TV) Requires panel	Project					
20.21	Project: Default V These bit pipe is of Note: VG Value 000b 001b	alue: s are used for f, or in the vert A display mo Name PF-PD PF-ID	Ob software control of interlaced behavior. They are updated immediate interlaced behavior. Description Progressive Fetch / Progressive display Progressive Fetch / Interlaced display (TV) Requires panel fitting to be enabled	Project All All					
20.21	Project: Default V These bit pipe is off Note: VG Value 000b 001b 010b	alue: s are used for f, or in the vert A display mo Name PF-PD PF-ID Reserved	Ob software control of interlaced behavior. They are updated immediate tical blank after programming if pipe is enabled. odes do not work while in interlaced fetch modes Description Progressive Fetch / Progressive display Progressive Fetch / Interlaced display (TV) Requires panel fitting to be enabled Reserved Interlaced Fetch / Interlaced display (programmable sync,	Project All All All					
20.21	Project: Default V These bit pipe is off Note: VG Value 000b 001b 010b 011b	alue: s are used for f, or in the veri A display mo Name PF-PD PF-ID Reserved IF-ID	Ob software control of interlaced behavior. They are updated immediated interlaced fetch modes Description Progressive Fetch / Progressive display Progressive Fetch / Interlaced display (TV) Requires panel fitting to be enabled Reserved Interlaced Fetch / Interlaced display (programmable sync, normal interlaced) Interlaced embedded panel with interlaced fetch (pixel	Project All All All All All					



20	Display_	Power_Mod	le_Switch						
	Project: All								
	Default Value: 0b								
	This bit is used for software to set the power saving progressive mode. The pipe enters or exits the power savings mode on the vblank after this bit is written. Please note that bits 17:16 of this register must be set to 00 in order for this bit to take effect.								
	Value Name		Description	Project					
	0b	Progressiv	ressive Pipe is in progressive mode						
	1b	Power Sav	Pipe is in power savings progressive mode	All					
19	Reserved	d: Must be a	zero						
18	Reserved	d: Must be a	zero						
7:16	Refresh	Rate_CxSR	Refresh_Rate_CxSR_Mode_Association						
-	Project: All								
	Project:		All						
	Default V These bit	s select how	0b / refresh rates are tied to big FIFO mode on pipe B. When they are set t						
	Default V These bit anything and 10 se Software	s select how other than 00 ettings directl	0b refresh rates are tied to big FIFO mode on pipe B. When they are set to 0, bits 23:21 of this register must be programmed to 000. Switching betw ly is not allowed. Software must program this field to 00 before switching le for enabling this mode only for integrated display panels that support	ween 01					
	Default V These bit anything and 10 se Software	s select how other than 00 ettings directl is responsibl	0b refresh rates are tied to big FIFO mode on pipe B. When they are set to 0, bits 23:21 of this register must be programmed to 000. Switching betw ly is not allowed. Software must program this field to 00 before switching le for enabling this mode only for integrated display panels that support	ween 01 J.					
	Default V These bit anything and 10 se Software correspor	s select how other than 00 ettings directl is responsible nding mode.	0b or refresh rates are tied to big FIFO mode on pipe B. When they are set to 0, bits 23:21 of this register must be programmed to 000. Switching betw ly is not allowed. Software must program this field to 00 before switching le for enabling this mode only for integrated display panels that support	ween 01					
	Default V These bit anything and 10 se Software correspon	s select how other than 00 ettings directl is responsible nding mode.	0b refresh rates are tied to big FIFO mode on pipe B. When they are set to 0, bits 23:21 of this register must be programmed to 000. Switching betw ly is not allowed. Software must program this field to 00 before switching le for enabling this mode only for integrated display panels that support Description No dynamic refresh rate change enabled. Software control through	ween 01 g. Project					
	Default V These bit anything and 10 se Software correspon Value 00b	s select how other than 00 ettings directl is responsibl nding mode. Name None	Ob Ob Verefresh rates are tied to big FIFO mode on pipe B. When they are set to 0, bits 23:21 of this register must be programmed to 000. Switching between the set of the set o	ween 01 g. Projec All					



		PIPE	BCONF—Pipe B Configuration Register					
15:14	Display_	Rotation_In	fo					
	Project:		All					
	Default V	alue:	Ob					
	These are informative bits set by software to indicate this pipe is being rotated. Software should set these for both hardware and software rotation cases. Hardware rotation is <u>not</u> enabled through these bits.							
	Value	Name	Description	Project				
	00b	None	No rotation on this pipe	All				
	01b	90	90° rotation on this pipe	All				
	10b	180	180° rotation on this pipe	All				
	11b	270	270° rotation on this pipe	All				
13	Color_R	ange_Select						
	Project: All							
	Default Value: 0b							
	This bit is used to select the color range of outputs.							
	Value Name		Description	Project				
	0b	Full	Apply full 0-2 ⁿ - 1 color range to the output	All				
	1b	CE	Apply CE color range to the output	All				
12:11	Pine out	tout color s	snace select					
12.11	Project:	Pipe_output_color_space_select Project: All						
	Default V	alue:	Ob					
	Informs the ports of the pipe output color space. Plane data formats and CSC need to be programmed to match what is selected here.							
	Value	Name	Description	Project				
	00b	RGB	RGB	All				
	01b	YUV 601	YUV 601	All				
	10b YUV 709		YUV 709	All				
	11b	Reserved	Reserved	All				
10:9	Reserve	d						
10:9	Reserve	d Project	DevILK	Format:				
8	Reserve	d Proje	ct: All Format:	MBZ				



		PIPE	BCONF—Pipe B Configuration	n Register				
7:5	Bits_Per	_Color						
	Project:		All					
	Default Value: 0b							
	This field selects the number of bits per color sent to a receiver device connected to this pipe. Color format takes place on the Vblank after being written. Color format change can be done independent of a pixel clock change.							
			ble dithering in the pipe/port if selecting a pi of the frame buffer.	xel color depth highe	er or lower than			
	Value	Name	Description		Project			
	000b	8 bits	8 bits per color		All			
	001b	10 bits	10 bits per color	10 bits per color				
	010b	6 bits	6 bits per color	All				
	011b	12 bits	12 bits per color	All				
	1XXb	Reserved	Reserved		All			
4	Dithering	g_enable						
	Project:		All					
	Default V	alue:	0b					
	This bit e	nables dithe	ring					
	Value	Name	Description		Project			
	0b	Disable	Dithering disabled		All			
	1b	Enable	Dithering enabled		All			
3:2	Reserve	d						
1	Reserve	d						



4.1.5 Display Pipeline B Counters and Timestamps

4.1.5.1 **PIPEB_FRMCOUNT—Pipe B Frame Counter**

	PIPEB_FRMCOUNT—Pipe B Frame Counter							
Register Type:		MMIO						
Address Of	ffset:	71040h						
Project:		All						
Default Val	ue:	00000000h						
Access:		Read Only						
Size (in bits	s):	32						
Bit					Description			
31:0	Pipe	Frame_Counter	Project:	All	Format:			
	See	Pipe A description						

4.1.5.2 **PIPEB_FLIPCOUNT**—Pipe B Flip Counter

		PIPE	B_FLIF		NT—Pipe B Flip Counter
Register Type:		MMIO			
Address O	ffset:	71044h			
Project:		All			
Default Va	lue:	00000000h			
Access:		Read Only			
Size (in bit	s):	32			
Bit					Description
31:0	Pipe	_Flip_Counter P	roject:	All	Format:
	See	Pipe A description			



4.1.5.3 **PIPEB_FRMTIMESTAMP—Pipe B Frame Time Stamp**

		PIPEB_FRMTIMESTAMI	P—Pipe B Fran	me Time Star	np
Register Type:		MMIO			
Address	Offset:	71048h			
Project:		All			
Default Value:		0000000h			
Access:		Read Only			
Size (in bits):		32			
Bit			Description		
31:0	Pipe	_Frame_Time_Stamp		Project:	All Format:
	See	Pipe A description			

4.1.5.4 **PIPEB_FLIPTIMESTAMP—Pipe B Flip Time Stamp**

		PIPEB_FLIPTIMES	STAMP-	–Pipe B	Flip Tin	ne Stam	p	
Register Type:		MMIO						
Address O	ffset:	7104Ch						
Project:		All						
Default Va	lue:	00000000h						
Access:		Read Only						
Size (in bit	s):	32						
Bit			l	Description	n			
31:0	Pipe	_Flip_Time_Stamp				Project:	All	Format:
	See	Pipe A description						

4.1.6 Cursor A Plane Control Registers

The CURACNTR active register will be updated on the vertical blank or when pipe is disabled, after the CURABASE or CURAPOPUPBASE trigger register is written, or when cursor A is not yet enabled – thus providing an atomic update of the cursor A control and base address registers.



4.1.6.1 CURACNTR—Cursor A Control Register

		CI		R—Cursor A Control R	enister			
Register T Address C Project:	Offset:		MMIO 70080h All					
Double Bu	its): uffer Update uffer Armed	By:	Write to Cl	rtical blank or pipe disabled or cur JRABASE or CURAVGAPOPUPE	BASE			
For Hi-res Bit	o it follows the VGA pipe	select.						
31:28	Reserved	Description Reserved Project: All Format:						
	interprets	nould be turn the cursor b		n using Cursor A as a popup curs ss as a <u>physical</u> address instead o	of a graphics address.	hardware		
	Value	ue Name		Description	Project			
	0b 1b	Hi-Res VGA		Cursor A is hi-res Cursor A is popup	All			
26	Project: Default Va This bit or	Cursor_Gamma_Enabled Project: All Default Value: 0b This bit only has an effect when using the cursor in a non-VGA mode. In VGA pop-up operation, the cursor data will always bypass the gamma (palette) unit.						
	Value	Name	Description	on		Project		
		Purpage	Cursor pix	All				
	0b	Bypass						
	0b 1b	Gamma	-	el data is gamma to be corrected	•	All		



		C	URACNTR—Cursor A Control Register						
24	Pipe_Co	Pipe_Color_Space_Conversion_Enable							
	Project: All								
	Default V	alue:	Ob						
	This bit e registers	nables pip must be se	e color space conversion for the cursor pixel data. CSC mode in the pipe et to match the format of the cursor pixel data.	CSC					
	Value	Name	Description	Project					
	0b	Bypass	Cursor pixel data bypasses the pipe color space conversion logic	All					
	1b	Pass	Cursor pixel data passes through the pipe color space conversion logic	: All					
23:16	Reserved Project: All Format:								
	180°_Rotation Project: All Default Value: 0b This mode causes the cursor to be rotated 180°. Only 32 bits per pixel cursors can be rotated. This field must be zero when the cursor format is 2 bits per pixel.								
	Value	Name	Description	Project					
	0b	None	No rotation	All					
	1b	180	180° Rotation of 32 bit per pixel cursors	All					
14	Trickle_Feed_Enable Project: DevSNB Default Value: 0b								
	Value	Name	Description	Project					
	0b	Enable	Trickle Feed Enabled - Data requests are sent whenever there is space in the Display Data Buffer	All					
		1	Trickle Food Dischlad Data regulate are cont in hursts	1					
	1b	Disable	Trickle Feed Disabled - Data requests are sent in bursts	All					
14	1b Reserve		ject: DevILK Format:	All					



5	Cursor M	ode Sel	ect
	Bit 5	Bits 2:0	Mode
	0	000	Cursor is disabled. This is the default after reset. When the cursor register value changes from enabled to disabled, the cursor will stop fetching data at the following VBLANK event. The cursor enable can be overridden by the pipe cursor disable bit. The value of these bits do not change when disabled by the pipe cursor disable bit.
	0	001	Reserved
	0	010	128 x 128 32bpp AND/INVERT (not available for VGA use) See description off 64 x 64 32bpp AND/INVERT format for byte usage
	0	011	256 x 256 32bpp AND/INVERT (not available for VGA use) See description off 64 x 64 32bpp AND/INVERT format for byte usage
	0	100	64 x 64 2bpp Indexed 3-color and transparency mode
	0	100	64 x 64 2bpp Indexed AND/XOR 2-plane mode
	0	110	64 x 64 2bpp Indexed 4-color mode
	0	111	64 x 64 32bpp AND/INVERT (not available for VGA use) For each pixel:
			Least significant three bytes provides cursor RGB 888 color information Most Significant Byte:
			All Ones: Opaque, show the cursor color All Zeros: Transparent (color must also equal zero)
	1	000	Other: Invert the underlying display pixel data (ignore the color)
	1	000	Reserved
	1	001	Reserved
	1	010 011	128 x 128 32bpp ARGB (8:8:8:8 MSB-A:R:G:B) (not available for VGA use)256 x 256 32bpp ARGB (8:8:8:8 MSB-A:R:G:B) (not available for VGA use)
	1	100	64 x 64 32bpp AND/XOR (not available for VGA use)
		100	For each pixel: Least significant three bytes provides cursor RGB 888 color information Most Significant Byte: All Ones: Opaque, show the cursor color All Zeros: Transparent (color must also equal zero) Other: XOR the cursor color with the underlying display pixel data
	1	101	128 x 128 32bpp AND/XOR (not available for VGA use) See description off 64 x 64 32bpp AND/XOR format for byte usage
	1	110	256 x 256 32bpp AND/XOR (not available for VGA use) See description off 64 x 64 32bpp AND/XOR format for byte usage
	1	111	64 x 64 32bpp ARGB (8:8:8 MSB-A:R:G:B) (not available for VGA use)
4:3	Reserved	d F	Project: All Format:
2:0		Mode_S	elect[2:0]
	Project:		All
	Default V	alue:	Ob
	1		



4.1.6.2 CURABASE—Cursor A Base Address Register

	CUR	ABASE—Cur	sor A Base Address Register
Register Ty	/pe:	MMIO	
Address Of	ifset:	70084h	
Project:		All	
Default Val	ue:	00000000h	
Access:		R/W	
Size (in bits	s):	32	
Double But	fer Update Point:	Start of vertical b	lank or pipe disabled
This registe CURAVGA	POPUPBASE is us	n cursor A is in th ed instead and th	e hi-res mode. In VGA popup mode his register <u>must not be written.</u> This register specifies the mage data is located.
Bit			Description
31:12	Cursor_Base_Add	ress[31:12]	
	Project:	All	
	Address:	GraphicsAd	dress[31:12]
			aphics address of the base of the cursor for hi-res mode. The cursor is in the CURAVGAPOPUPBASE register.
	The cursor surface a be tiled. When perfort to start from the last	orming 180° rotatic	K byte aligned. The cursor must be in linear memory, it cannot on, this address does not change, hardware will internally offset e of the cursor.
11:0	Reserved Proj	ect: All	Format:



4.1.6.3 CURAPOS—Cursor A Position Register

	CURAPOS—Cursor A Position Regis	ster							
Register Ty	mpe: MMIO								
Address O									
Project:	All								
Default Val	ue: 00000000h								
Access:	R/W								
Size (in bit	32								
Double But	fer Update Point: Start of vertical blank or pipe disabled								
0	r specifies the screen position of the cursor. The origin of the cur of the active image for the display pipe that the cursor is assigned		is always th	ne upper					
Bit	Description								
31	Cursor_Y-Position_Sign_Bit		Project:	All					
	This bit provides the sign bit of a signed 13-bit value that specifies the For normal high resolution display modes, the cursor must have at least the active screen. For use as a VGA Popup, the entire cursor must be of the VGA image.	st a single pixe	l positioned	over					
30:28	Reserved Project: All	Format:	MBZ						
27:16	Cursor_Y-Position_Magnitude_Bits		Project:	All					
	This register provides the magnitude bits of a signed 12-bit value that cursor. The sign bit of this value is provided by bit 31of this register. If entire cursor must be positioned over the active area of the VGA imag (VGA Border Enable bit in the VGA Config register) includes the border "active area".	For use as a V e. Enabling th	GA Popup, t e border in V	he /GA					
	When performing 180° rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation								
15	Cursor_X-Position_Sign_Bit		Project:	All					
	This bit provides the sign bit of a signed 13-bit value that specifies the For normal high resolution display modes, the cursor must have at least the active screen. For use as a VGA Popup, the entire cursor must be of the VGA image. Enabling the border in VGA (VGA Border Enable b includes the border in what is considered the "active area".	st a single pixe	I positioned er the active	over area					
14:12	Reserved Project: All	Format:	MBZ						
11:0	Cursor_X-Position_Magnitude_Bits		Project:	All					
	These 12 bits provide the signed 13-bit value that specifies the horizon bit is provided by bit 15 of this register.	ntal position of	cursor. The	e sign					
	When performing 180° rotation, this field specifies the horizontal positive relative to the end of the active video area in the unrotated orientation.		right corner						



4.1.6.4 CURAVGAPOPUPBASE—Cursor A VGA Popup Base Address Register

CI	JRAVGAPOPU	BASE—Cur	sor A VGA Popup Base Address Register					
Register Ty		MMIO						
Address Of	•	7008Ch						
Project:		All						
Default Val	ue:	00000000h						
Access:		R/W						
Size (in bits	s):	32						
Double But	fer Update Point:	Start of vertical b	lank or pipe disabled					
	his register arm Cl							
instead and		not be written. T	e VGA popup mode. In hi-res mode CURABASE is used his register specifies the physical memory address at which					
Bit		Description						
31:12	Cursor_VGA_Popu	p_Base_Address	[31:12]					
	Project:	All						
	Address:	PhysicalAddres	ss[31:12]					
			<u>ysical</u> address of the base of the cursor for VGA popup mode. ursor is in the CURABASE register.					
	The cursor surface a be tiled.	ddress must be 4l	K byte aligned. The cursor must be in linear memory, it cannot					
11:7	Reserved Proje	ect: All	Format:					
6:0	Cursor_VGA_Popu	p_Base_Address	_MSBs[38:32]					
	Project:	All						
	Address:	PhysicalAddres	ss[38:32]					
	This field specifies b See restrictions in C		vsical address of the base of the cursor for VGA popup mode. Base Address field.					



4.1.6.5 CURAPALET—Cursor A Palette registers

	Cursor Palette Format										
Project:	All										
Bit	Description										
31:24	Reserved Pro	oject: All			Format:	MBZ					
23:16	Red_or_Y_Value	Project:	All	Format:							
	These registers specify the cursor palette. RGB data is full range unsigned numbers. YUV data will be unsigned for the Y and excess 128 notation for the UV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.										
15:8	Green_or_U_Valu	e Project:	All	Format:							
7:0	Blue_or_V_Value	Project:	All	Format:							

C	CURAPALET—Cursor A Palette registers				
Register Type:	MMIO				
Address Offset:	70090h				
Project:	All				
Default Value:	0000000h				
Access:	R/W				
Size (in bits):	4x32				
Double Buffer Update Point:	Start of vertical blank or pipe disabled				

The cursor palette provides color information when using one of the indexed modes. The two-bit index selects one of the four colors or two of the colors when in the AND/XOR cursor mode. The cursor palette provides color information when using one of the indexed modes. The two-bit index selects one of the four colors or two of the colors when in the AND/XOR cursor mode for two of the colors when in the AND/XOR cursor mode.

The table below describes the palette usage for different cursor modes and indexes.

		Ind	ex	2 color	3color	4	color
		00)	palette 0	palette 0	pa	lette 0
		01	l	palette 1	palette 1	ра	lette 1
		10)	transparent	transparent	ра	lette 2
		11	I	invert destination	palette 3	pa	lette 3
					(palette 3 all 1s)		
		Palett	e 3 m	ust be programmed w	vith all 1s for inver	t destinat	ion.
DWord		Bit			De	scription	
0	3	1:0	CUR	APALETO Pro	oject: All	Format:	Cursor Palet



	CURAPALET—Cursor A Palette registers							
1	31:0	CURAPALET1	Project:	All	Format:	Cursor Palette Format		
2	31:0	CURAPALET2	Project:	All	Format:	Cursor Palette Format		
3	31:0	CURAPALET3	Project:	All	Format:	Cursor Palette Format		

4.1.6.6 CURASURFLIVE—Cursor A Live Surface Base Address

		CURASURFLIVE—Cursor A Live S	urface Base Address				
Register 1	Гуре:	MMIO					
Address C	Offset:	700ACh					
Project:		All					
Default Va	alue:	0000000h					
Access:		Read Only					
Size (in bi	ts):	32					
Bit		Descripti	on				
31:0	Curs	or_A_Live_Surface_Base_Address	Project: All Format:				
	This	gives the live value of the surface base address as being currently used for the plane.					



4.1.7 Cursor B Plane Control Registers

The CURBCNTR active register will be updated on the vertical blank or when pipe is disabled, after the CURBBASE trigger register is written, or when cursor B is not yet enabled – thus providing an atomic update of the cursor B control and base address registers.

4.1.7.1 CURBCNTR—Cursor B Control Register

		Cl	JRBCNTR—Cursor B Control Register				
Register T	vpe:		MMIO				
Address O			700C0h				
Project:			All				
Default Val	ue:		0000000h				
Access:			R/W				
Size (in bit	s):		32				
Double Bu	ffer Update	e Point:	Start of vertical blank or pipe disabled or cursor disabled, after armed				
Double Bu	ffer Armed	l By:	Write to CURBBASE				
Cursor B is	connected	to pipe B or	nly.				
Bit			Description				
31:27	Reserved Project: All Format: MBZ						
26	Cursor_Gamma_Enable						
	Project: All						
	Default Value: 0b						
	Value	Name	Description Pr	Project			
	0b	Bypass	Cursor pixel data bypasses gamma correction All				
	1b	Corrected	Cursor pixel data is gamma to be corrected All				
25	Reserved	d Proje	ect: All Format:				
24	Pipe Co	or Space	Conversion_Enable				
	Project:	- • -	All				
	Default Value: 0b						
			color space conversion for the cursor pixel data. CSC mode in the pipe C to match the format of the cursor pixel data	SC			
	Value	Name	Description	Project			
	0b	Bypass	Cursor pixel data bypasses the pipe color space conversion logic	All			
	1b	pass	Cursor pixel data passes through the pipe color space conversion logic.	All			



		CI	JRBCN	TR—Cur	sor B Control	Register		
15	180°_Rota	ation						
	Project:		All					
	Default Va	alue:	0b					
					180°. Only 32 bits p s 2 bits per pixel.	per pixel cursors ca	n be rotate	d. This
	Value	Value Name		Descript	Description			
	0b	None		No rotatio	on		All	
	1b	180		180° Rota	ation of 32 bit per pi	kel cursors	All	
14	Trickle_F Project: Default Va	eed_Enab alue:	le DevS 0b	SNB				
	Value	Name	Descript	ion				Projec
	0b	Enable			d - Data requests ar Data Buffer.	e sent whenever th	ere is	All
	1b	Disable	Trickle F	eed Disable	d - Data requests a	e sent in bursts.		All
14	Reserved	Proje	ect: De	evILK		Format	:	
13:6	Reserved	Proje	ect: All			Format	MBZ	
5	Cursor_N	lode_Sele	ct Proje	ct: All	Format:			
	Cursor M	ode Select	t					
	Defined in	CURACN	TR—Curso	or A Control	Register Bit 5.			
4:3	Reserved	Proje	ect: All			Format:	:	
2:0	Cursor_N	lode_Sele	ct Proje	ct: All	Format:			
	These three	ee bits toge	ether with b	oit 5 select th	ne mode for cursor a	as shown in CURAC	NTR—Cu	rsor A



4.1.7.2 CURBBASE—Cursor B Base Address Register

	CUR	BBASE—Cursor	B Base Address Regist	er					
Register Type: MMIO									
Address O	ffset:	700C4h	700C4h						
Project:		All	All						
Default Val	ue:	00000000h							
Access:		R/W							
Size (in bit	s):	32							
Double Bu	ffer Update Point:	Start of vertical blank	or pipe disabled						
	his register arm C er specifies the grap	-	at which the cursor image da	ıta is loc	cated.				
Bit			Description						
31:12	Cursor_Base_Add	ress[31:12]							
	Project:	All							
	Address:	GraphicsAddress[31:12]							
		es the graphics address gisters on the next displa	of the cursor. It also acts as a tri y event.	igger eve	ent to force the				
	The cursor surface address must be 4K byte aligned. The cursor must be in linear memory, it cannot be tiled. When performing 180° rotation, this address does not change, hardware will internally offset to start from the last pixel of the last line of the cursor.								
11:0	Reserved Pro	ject: All	Fo	ormat:	MBZ				



4.1.7.3 CURBPOS—Cursor B Position Register

		CURB	POS—Cu	rsor B P	osition R	egister		
Register T	ype:	MMIC)					
Address C	offset:	700C	8h					
Project:		All						
Default Va	lue:	00000	0000h					
Access:		R/W						
Size (in bit	ts):	32						
Double Bu	Iffer Update Point:	Start	of vertical bla	ank or pipe d	isabled			
	er specifies the so						on is always	s the upper
left corner	of the active imag	ge for the	display pipe	e that the c	ursor is assi	gned.		
Bit				Desci	ription			
31	Cursor_Y-Positio	on_Sign_	Bit				Project	: All
	This bit provides t For normal high re the active screen.	esolution of						
30:28	Reserved P	Project:	All			Format	: MBZ	
27:16	Cursor_Y-Position	on_Magni	itude_Bits				Project	: All
	This register prov cursor. The sign						e vertical pos	sition of
	When performing to the end of the a					ition of the lower	right corner	relative
15	Cursor_X-Position	on_Sign_	Bit				Project	: All
	This bit provides t For normal high re the active screen.	esolution of						
14:12	Reserved P	Project:	All			Format	: MBZ	
11:0	Cursor_X-Position	on_Magni	itude_Bits				Project	: All
	These 12 bits pro bit is provided by			value that sp	pecifies the ho	prizontal position	of cursor. T	The sign
	When performing to the end of the a					ition of the lower	right corner	relative



4.1.7.4 CURBPALET—Cursor B Palette registers

	CURBPALET—Cursor B Palette registers										
Register Ty	Register Type:										
Address Of	Address Offset:		700D0h								
Project:	Project:			All							
Default Val	Default Value:		0000000h								
Access:		F	R/W								
Size (in bits	s):	4	4x32								
Double Buf	fer Update	Point:	Start of ve	ertical blank o	or pipe	disabled					
selects one provides co	of the fou	ir colors or t ation when	two of the using on	e colors wh	en in exed	the AND/XOF modes. The	lexed modes. The two-bit index R cursor mode. The cursor palette two-bit index selects one of the four ursor A palette usage table.				
DWord	Bit					Description					
0	31:0	CURBPAL	ET0	Project:	All	Format:	Cursor Palette Format				
1	31:0	CURBPAL	ET1	Project:	All	Format:	Cursor Palette Format				
2	31:0	CURBPAL	ET2	Project:	All	Format:	Cursor Palette Format				
3	31:0	CURBPAL	ET3	Project:	All	Format:	Cursor Palette Format				

4.1.7.5 CURBSURFLIVE—Cursor B Live Surface Base Address Register

	CU	RBSURFLIVE—Cursor B Live Surfa	ace Base Address Register
Register T	ype:	MMIO	
Address Offset:		700ECh	
Project:		All	
Default Value:		0000000h	
Access:		Read Only	
Size (in bit	ts):	32	
Bit		Descript	tion
31:0	Curs	or_Live_Surface_Base_Address	Project: All Format:
	This	gives the live value of the surface base address as	s being currently used for the plane.



4.1.8 Primary A Plane Control

The DSPACNTR and DSPASTRIDE active registers will be updated on the vertical blank or when pipe is disabled, after the DSPASURF trigger register is written, or when the primary A is not yet enabled – thus providing an atomic update of the primary A control, stride, and base address registers.

4.1.8.1 DSPACNTR—Primary A Control Register

		DS	PACNTR—Primary A Control Register			
Register Ty	ype:		MMIO			
Address O	ffset:		70180h			
Project:			All			
Default Val	ue:		0000000h			
Access:			R/W			
Size (in bit	s):		32			
Double But	ffer Update		Start of vertical blank or pipe disabled or primary disabled, after armed			
	ffer Armed I		Write to DSPASURF			
Primary A P	Plane is conn	nected to pi	pe A only.			
Bit			Description			
31	Primary_	Plane_Ena	able Project: All Format:	Enable		
	When this bit is set, the primary plane will generate pixels for display. When set to zero, primary pl memory fetches cease and plane output is transparent. The display pipe must be enabled to enab the plane. There is an override for the enable of the plane in the Pipe Configuration register. When					
			O mode, write to this register to enable the plane will be internally buffe FO mode is exiting.	red and		
30	Gamma_	Enable				
	Project:		All			
	Default V	/alue:	0b			
			be changed after the plane has been disabled. It controls the bypassing unit for the plane pixel data. For 8-bit indexed display data, this bit sho			
	Value	Name	Description	Project		
	0b	Bypass	Plane pixel data bypasses the display pipe gamma correction logic	All		
		Correct	Plane pixel data is gamma corrected in the display pipe gamma	All		



29:26	Source_Pixel_Format Project: All								
	Default V	alue:	0b						
	These bir uses the pixel.	ts should only pipe palette.	be changed after the plane has been disable Before entering the blender, each source for	ed. Pixel format of 8-bit indemat is converted to 12 bits p	exed ber				
	Value	Name		Description	Projec				
	0010b	8bpp	8-bpp Indexed	All					
	0101b	16-bit BGR>	((5:6:5 MSB-R:G:B)	pixel format (XGA compatible).	All				
	0110b	32-bit BGR>	(8:8:8:8 MSB-X:R:G:B)	pixel format. Ignore alpha	All				
	1000b	32-bit RGB>	((2:10:10:10 MSB-X:B:G:R)	pixel format. Ignore alpha	All				
	1010b	32-bit BGR>	((2:10:10:10 MSB-X:R:G:B)	pixel format. Ignore alpha	All				
	1100b	64-bit RGB>	K Floating Point(16:16:16:16 MSB-X:B:G:R)	pixel format. Ignore alpha	All				
	1110b	32-bit RGB>	(8:8:8:8 MSB-X:B:G:R)	pixel format. Ignore alpha	All				
		Use of 64bp 80% of cdcl							
	others	Reserved		Reserved	All				
25	Plane Ex	stended Ran	ge_Source_Select						
	Project:		DevSNB						
	Default V	alue:	0b						
	extended plane ext	range. This i	ate when the plane source pixel format shou s only valid with certain source pixel formats source is not selected, the plane will fit the so range.	. If the pipe is extended ran					
	Value	Name	Description	I	Project				
	0b	Normal	Normal range source selected		All				
	1b	Extended	Extended range source selected.		All				



24	Pipe Co	lor Space	Conversion_Enable					
	Project: All							
	Default V	alue:	Ob					
	This bit enables pipe color space conversion for the plane pixel data. CSC mode in the pipe CSC registers must be set to match the format of the plane pixel data.							
	Value	Name	Description	Project				
	0b	Bypass	Plane pixel data bypasses the pipe color space conversion logic	All				
	1b	Pass	Plane pixel data passes through the pipe color space conversion logic.	All				
23:16	Reserve	d Proje	ect: All Format:					
15	180°_Dis	play_Rota	tion					
	Project: All							
	Default Value: 0b							
	This mode causes the plane to be rotated 180°. In addition to setting this bit, software must also set the surface address offset to the lower right corner of the unrotated image.							
	Value Name Description							
	0b	None	No rotation	All				
	1b	180	180° rotation	All				
14	Trickle_	Feed_Enab	le					
	Project: All							
	Project:		All					
	Project: Default V	alue:	All Ob					
	Default V							
	Default V		Ob	Projec t				
	Default V [ILK]: Thi	s bit must a	0b Iways be programmed to '1'.	-				
	Default V [ILK]: This Value	s bit must a	Ob Iways be programmed to '1'. Description Trickle Feed Enabled - Plane data requests are sent whenever there	-				
13	Default V [ILK]: Thi Value 0b 1b	s bit must a Name Enable Disable	Ob Iways be programmed to '1'. Description Trickle Feed Enabled - Plane data requests are sent whenever there is space in the Display Data Buffer.	t All				
13	Default V [ILK]: Thi Value 0b 1b	s bit must a Name Enable Disable	Ob Iways be programmed to '1'. Description Trickle Feed Enabled - Plane data requests are sent whenever there is space in the Display Data Buffer. Trickle Feed Disabled - Plane data requests are sent in bursts	t All				
13	Default V [ILK]: Thi Value 0b 1b Data_Bu	s bit must a Name Enable Disable	Ob Iways be programmed to '1'. Description Trickle Feed Enabled - Plane data requests are sent whenever there is space in the Display Data Buffer. Trickle Feed Disabled - Plane data requests are sent in bursts Trickle Feed Disabled - Plane data requests are sent in bursts	t All				
13	Default V [ILK]: Thi: Value Ob 1b Data_Bu Project:	s bit must a Name Enable Disable	Ob Iways be programmed to '1'. Description Trickle Feed Enabled - Plane data requests are sent whenever there is space in the Display Data Buffer. Trickle Feed Disabled - Plane data requests are sent in bursts toning_Control(testmode) All	t All				
13	Default V [ILK]: Thi Value 0b 1b Data_Bu Project: Security: Default V	s bit must a Name Enable Disable ffer_Partiti	Ob Iways be programmed to '1'. Description Trickle Feed Enabled - Plane data requests are sent whenever there is space in the Display Data Buffer. Trickle Feed Disabled - Plane data requests are sent in bursts Trickle Feed Disabled - Plane data requests are sent in bursts ioning_Control(testmode) All Test	t All				
13	Default V [ILK]: Thi Value 0b 1b Data_Bu Project: Security: Default V	s bit must a Name Enable Disable ffer_Partiti	Ob Iways be programmed to '1'. Description Trickle Feed Enabled - Plane data requests are sent whenever there is space in the Display Data Buffer. Trickle Feed Disabled - Plane data requests are sent in bursts toring_Control(testmode) All Test Ob	t All				
13	Default V [ILK]: Thi Value 0b 1b Data_Bu Project: Security: Default V Note: Wh	s bit must a Name Enable Disable ffer_Partiti alue: en in CxSR	Ob Iways be programmed to '1'. Description Trickle Feed Enabled - Plane data requests are sent whenever there is space in the Display Data Buffer. Trickle Feed Disabled - Plane data requests are sent in bursts toning_Control(testmode) All Test Ob Max FIFO mode, this bit will be ignored.	t All All				
13	Default V [ILK]: This Value 0b 1b Data_Bu Project: Security: Default V Note: Wh	s bit must a Name Enable Disable ffer_Partiti falue: hen in CxSR Name Use	Ob Iways be programmed to '1'. Description Trickle Feed Enabled - Plane data requests are sent whenever there is space in the Display Data Buffer. Trickle Feed Disabled - Plane data requests are sent in bursts ioning_Control(testmode) All Test Ob RMax FIFO mode, this bit will be ignored. Description Primary A Data Buffer will use Sprite A buffer space when Sprite A is	t All All Project				



10	Tiled Su	rfaco							
10									
	Project: All Default Value: 0b								
		ndicates that	at the plane surface data is in tiled memory. Only X tiling is supported fo	r display					
		s bit is set, IRF registe	it affects the hardware interpretation of the DSPATILEOFF, DSPALINOI rs.	FF, and					
	Value Name Description								
	0b	Linear	Plane uses linear memory	All					
	1b	X-tiled	Plane uses X-tiled memory	All					
	address	will change ertical blank	synchronous updates of the surface address when written by MMIO. The with the next TLB request or when start of vertical blank is reached. Up may not complete until after the first few active lines are displayed.						
	is - W	enabled.	d streamer initiated surface address updates to this plane are allowed who done indication in pipe status register before writing the surface address is bit set						
		-	1	-					
	Value	Ob Sync Surface Address MMIO writes will update synchronous to state							
	Value Ob		Description Surface Address MMIO writes will update synchronous to start of vertical blank	Projec All					



Primary Plane Source Pixel Format Mapping of Bits to Colors:

Note: For 64-bit Floating Point format, each of the 16 bit color components is 1:5:10 MSBsign:exponent:fraction

PRIMARY RGB	Ignored	Red	Green	Blue
16-bit BGRX 5:6:5	N/A	15:11	10:5	4:0
32-bit BGRX 8:8:8	31:24	23:16	15:8	7:0
32-bit RGBX 10:10:10	31:30	9:0	19:10	29:20
32-bit BGRX 10:10:10	31:30	29:20	19:10	9:0
64-bit RGBX Float 16:16:16	63:48	15:0	31:16	47:32
32-bit RGBX 8:8:8	31:24	7:0	15:8	23:16

4.1.8.2 DSPALINOFF—Primary A Linear Offset Register

Register Type:		MMIO					
Address Offset:		70184h					
Project:		All					
Default Value:		0000000h					
Access:		R/W					
Size (in bits):		32					
Double Bu	ffer Update Point:	Start of vertical blank or pipe disabled					
Bit		Description					
31:0	Primary_Linear_O	ffset Proje	ct: All	Format:			
	surface address to aligned. When perf pixel of the last line	es the linear panning byte offset into the primary plane. get the address of the first pixel to be displayed. This off orming 180° rotation, the unpanned offset must be the d of the display data in its unrotated orientation and the dis s tiled, the contents of this register are ignored.	set must ifference	be at least pixel between the last			



4.1.8.3 DSPASTRIDE—Primary A Stride Register

	D	SPASTRIDE	E—Prima	ary A Stride Register			
Register Ty	/pe:	MMIO					
Address Offset:		70188h					
Project:		All					
Default Val	ue:	00000000h					
Access:		R/W					
Size (in bit	s):	32					
Double But	ffer Update Point:	Start of vertical blank or pipe disabled or primary disabled, after armed					
Double But	ffer Armed By:	Write to DSPASURF					
Bit			I	Description			
31:16	Reserved Pro	ject: All		Format:			
15:6	Primary_Stride	Project:	All	Format:			
	aligned. When usin line to line incremer	g tiled memory, It for the display Ind stream or wr	this must b . This regis	When using linear memory, this must be 64 byte e 512 byte aligned. This value is used to determine the ter is updated through either a command packet passed egister. The stride is limited to a maximum of 32K bytes			
5:0	Reserved Pro	ject: All		Format:			

4.1.8.4 DSPASURF—Primary A Surface Base Address Register

DSPASURF—Primary A Surface Base Address Register				
Register Type:	MMIO			
Address Offset:	7019Ch			
Project:	All			
Default Value:	0000000h			
Access:	R/W			
Size (in bits):	32			
Double Buffer Update Point:	Start of vertical blank or pipe disabled			
Writes to this register arm D	SPA registers			



	DSP	ASURF—	Primary A	Surface Base A	ddress Registe	r
Bit	Description					
31:12	Primary_Surface_Base_Address					
	Project:	All				
	Address:	Gr	aphicsAddres	s[31:12]		
This address specifies the surface base address. (x, y) offsets in the DSPATILEOFF register. When specified using a linear offset in the DSPALINOFF			ster. When the surface is			
	This address must be 4K aligned. When performing asynchronous flips and the display surface is in tiled memory, this address must be 256K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT.					
11:3	Reserved	Project:	All		Format:	
2	Reserved	Project:	ILK		Format:	MBZ
0	Reserved	Project:	All		Format:	MBZ



4.1.8.5 DSPATILEOFF—Primary A Tiled Offset Register

DSPATILEOFF—Primary A Tiled Offset Register						
Register Type:	ype: MMIO					
Address Offse	et:	701A4h				
Project:		All				
Default Value:		00000000h				
Access:		R/W				
Size (in bits):		32				
Double Buffer	Update Point:	Start of vertical	l blank or pipe disabled			
DSPASURF re surface is in lir register are igr	er specifies the panning for the display surface. The surface base address is specified in the F register, and this register is used to describe an offset from that base address. When the in linear memory, the offset is specified in the DSPALINOFF register and the contents of this e ignored. When the surface is tiled, the start position is specified in this register as an (x, y) offse eginning of the surface.					
Bit	Description					
31:28 Re	eserved Proje	ct: All	Format: MBZ			
27:16 Pr	imary_Start_Y-Po	sition	Project: All Format:			
Th Th	These 12 hits specify the vertical position in lines of the beginning of the active display plane relative to					

	the display surface. When performing 180° rotation right corner relative to the start of the active display	, this field specifies the vertical position of the lower
15:12	Reserved Project: All	Format: MBZ
11:0	Primary_Start_X-Position	Project: All Format:
	These 12 bits specify the horizontal offset in pixels of to the display surface. When performing 180° rotation lower right corner relative to the start of the active di	on, this field specifies the horizontal position of the



4.1.8.6 DSPASURFLIVE—Primary A Live Surface Base Address

	0	SPASURFLIVE—Primary A Live Surface Base Address
Register 1	Гуре: М	MIO
Address Offset:		J1ACh
Project:	A	I
Default Va	alue: 0)000000h
Access:	R	ead Only
Size (in bi	i ts): 3	
Trusted T	ype: 1	
Bit		Description
31:0	Primar	_Live_Surface_Base_Address
	Project:	All
	Address	:: GraphicsAddress[31:0]
	This giv	es the live value of the surface base address as being currently used for the plane.

4.1.9 Primary B Plane Control

The DSPBCNTR and DSPBSTRIDE active registers will be updated on the vertical blank or when pipe is disabled, after the DSPBSURF trigger register is written, or when the primary B is not yet enabled – thus providing an atomic update of the primary B control, stride, and base address registers.

4.1.9.1 DSPBCNTR—Primary B Control Register

DSPBCNTR—Primary B Control Register				
Register Type:	MMIO			
Address Offset:	71180h			
Project:	All			
Default Value:	0000000h			
Access:	R/W			
Size (in bits):	32			
Double Buffer Update Point:	Start of vertical blank or pipe disabled or primary disabled, after armed			
Double Buffer Armed By:	Write to DSPBSURF			
Primary B Plane is connected	to pipe B only			



Bit			Description				
31	Primary_	Plane_Ena	ble Project: All Format	:: Enable			
	memory f the plane Self Refre	etches ceas . There is a esh Big FIF	it is set, the primary plane will generate pixels for display. When set to zero, primar ches cease and plane output is transparent. The display pipe must be enabled to er here is an override for the enable of the plane in the Pipe Configuration register. When Big FIFO mode, write to this register to enable the plane will be internally buffered ile Big FIFO mode is exiting.				
30	Gamma	Enable					
	Project:		All				
	Default V	/alue:	Ob				
			be changed after the plane has been disabled. It controls the bypass unit for the plane pixel data. For 8-bit indexed display data, this bit s				
	Value	Name	Description	Project			
	0b	Bypass	Plane pixel data bypasses the display pipe gamma correction logic	All			
	1b	Correct Plane pixel data is gamma corrected in the display pipe gamma correction logic.		All			
9:26	Project:	Pixel_Form	nat All				
9:26	Project: Default V These bit	alue: ts should or	lat				
9:26	Project: Default V These bit uses the	alue: ts should or	All Ob Ny be changed after the plane has been disabled. Pixel format of 8-	2 bits per			
9:26	Project: Default V These bit uses the pixel.	alue: ts should or pipe palette	All Ob Ny be changed after the plane has been disabled. Pixel format of 8- e. Before entering the blender, each source format is converted to 12	2 bits per			
9:26	Project: Default V These bit uses the pixel. Value	alue: is should or pipe palette Name 8bpp	All Ob Ny be changed after the plane has been disabled. Pixel format of 8- be. Before entering the blender, each source format is converted to 12 Description	2 bits per Projec			
9:26	Project: Default V These bit uses the pixel. Value 0010b	alue: ts should or pipe palette Name 8bpp 16-bit BG	All Ob	2 bits per Projec All All			
9:26	Project: Default V These bit uses the pixel. Value 0010b 0101b	alue: is should or pipe palette Name 8bpp 16-bit BG 32-bit BG	All Ob Ny be changed after the plane has been disabled. Pixel format of 8- be. Before entering the blender, each source format is converted to 12 Description 8-bpp Indexed RX (5:6:5 MSB-R:G:B) pixel format (XGA compatible).	2 bits per Projec All All alpha All			
9:26	Project: Default V These bit uses the pixel. Value 0010b 0101b 0110b	alue: ts should or pipe palette Name 8bpp 16-bit BG 32-bit BG 32-bit RG	All Ob ob ob ob ob ob ob ob ob ob o	2 bits per Projec All All alpha All alpha All			
9:26	Project: Default V These bit uses the pixel. Value 0010b 0101b 0110b 1000b	alue: ts should or pipe palette 8bpp 16-bit BG 32-bit BG 32-bit RG 32-bit BG	All Ob Ob Ob Ob Ob Ob Ob Ob Ob Ob	2 bits per Projec All All All alpha All alpha All alpha All			
9:26	Project: Default V These bit uses the pixel. Value 0010b 0101b 0110b 1000b 1010b	alue: ts should or pipe palette 8bpp 16-bit BG 32-bit BG 32-bit RG 32-bit RG 64-bit RG	All Ob block all block block block block block	2 bits per Projec All All All alpha All alpha All alpha All			
9:26	Project: Default V These bit uses the pixel. Value 0010b 0101b 0110b 1000b 1010b	alue: ts should or pipe palette 8bpp 16-bit BG 32-bit BG 32-bit RG 32-bit RG 32-bit RG Use of 64 80% of cc	All Ob block all block block block block block	2 bits per Projec All All All alpha All alpha All alpha All alpha All			



25		DS				
20	Plane_Extended_Range_Source_Select					
	Project: DevSNB					
	Default Value: 0b					
	extended plane exte	range. Th	dicate when the plane source pixel format should be processed as having is is only valid with certain source pixel formats. If the pipe is extended ra- ie source is not selected, the plane will fit the source pixel data into the 0 ed range.	ange and		
	Value	Name	Description	Project		
	0b	Normal	Normal range source selected	All		
	1b	Extended	Extended range source selected.	All		
25	Reserved	l Proj	ect: DevILK Format:			
24	Pipe_Col	or_Space_	_Conversion_Enable			
	Project:		All			
	Default Va	Default Value: 0b				
			e color space conversion for the plane pixel data. CSC mode in the pipe t to match the format of the plane pixel data.	CSC		
	Value	Name	Description	Project		
	0b	Bypass	Plane pixel data bypasses the pipe color space conversion logic	All		
	1b	Pass	Plane pixel data passes through the pipe color space conversion logic.	All		
3:16	Reserved	l Proj	ect: All Format:			
15	180°_Dis	play_Rota	tion			
	Project: All					
	Default Value: 0b					
			ne plane to be rotated 180°. In addition to setting this bit, software must a offset to the lower right corner of the unrotated image.	lso set		
	Value	Name	Description	Project		
		1	No rotation	All		
	0b	None	No rotation	All		
	0b 1b	None 180	180° rotation	All		
14	1b		180° rotation			
14	1b	180	180° rotation			
14	1b Trickle_F	180 Feed_Enak	180° rotation			
14	1b Trickle_f Project: Default Va	180 Feed_Enat	180° rotation			
14	1b Trickle_f Project: Default Va	180 Feed_Enat	180° rotation DIE All Ob	All		
14	1b Trickle_F Project: Default Va [DevILK]	180 Feed_Enat alue: This bit mu	180° rotation DIE All Ob st always be programmed to '1'.			



		DS	PBCNTR—Primary B Control Register	
13	Data_Bu	ffer_Partiti	oning_Control(testmode)	
	Project: Security: Default Va		All Test 0b Max FIFO mode, this bit will be ignored.	
	Value	Name	Description	Project
	Ob	Use Sprite	Primary B Data Buffer will use Sprite B buffer space when Sprite B is disabled.	All
	1b	Not Use Sprite	Primary B Data Buffer will not use Sprite B buffer space when Sprite B is disabled	All
12:11	Reserved	l Proje	ect: All Format:	11
10	Tiled_Surface Project: All Default Value: 0b This bit indicates that the plane surface data is in tiled memory. Only X tiling is support surfaces. When this bit is set, it affects the hardware interpretation of the DSPBTILEOFF, DSI			
		RF register		Project
	Value	Name	Description	Project
	0	Linear		A 11
	0b	Linear	Plane uses linear memory	All
	1b	X-tiled	Plane uses X-tiled memory	All All
9	1b Asynchro Project: Default Va This bit w address v	X-tiled onous_Sur alue: <i>i</i> III enable a <i>w</i> ill change		All
9	1b Asynchro Project: Default Va This bit w address v	X-tiled DNOUS_Sur alue: <i>i</i> II enable a <i>w</i> ill change rrtical blank	Plane uses X-tiled memory face_Address_Update_Enable All Ob synchronous updates of the surface address when written by MMIO. Th with the next TLB request or when start of vertical blank is reached. Upd	All
9	1b Asynchro Project: Default Va This bit w address w during ve Restricti	X-tiled DNOUS_Sur alue: <i>i</i> III enable a will change rtical blank ONS:	Plane uses X-tiled memory face_Address_Update_Enable All Ob synchronous updates of the surface address when written by MMIO. Th with the next TLB request or when start of vertical blank is reached. Upd	All e surface dates
9	1b Asynchro Project: Default Va This bit w address w during ve Restricti - Na is - W	X-tiled DNOUS_Sur alue: vill enable a will change vill change vill change ortical blank ons: o command enabled.	Plane uses X-tiled memory face_Address_Update_Enable All Ob synchronous updates of the surface address when written by MMIO. Th with the next TLB request or when start of vertical blank is reached. Upp may not complete until after the first few active lines are displayed. I streamer initiated surface address updates to this plane are allowed wh one indication in pipe status register before writing the surface address r	All e surface dates en this bit
9	1b Asynchro Project: Default Va This bit w address w during ve Restricti - Na is - W	X-tiled DNOUS_SUR alue: vill enable a will change vill change vill change vill change ortical blank ONS: o command enabled. vait for flip d	Plane uses X-tiled memory face_Address_Update_Enable All Ob synchronous updates of the surface address when written by MMIO. Th with the next TLB request or when start of vertical blank is reached. Upp may not complete until after the first few active lines are displayed. I streamer initiated surface address updates to this plane are allowed wh one indication in pipe status register before writing the surface address r	All e surface dates en this bit
9	1b Asynchro Project: Default Va This bit w address v during ve Restricti - No is - W ag	X-tiled X-tiled alue: vill enable a will change vill change vill change ortical blank ons: o command enabled. vait for flip d gain with thi	Plane uses X-tiled memory face_Address_Update_Enable All Ob synchronous updates of the surface address when written by MMIO. Th with the next TLB request or when start of vertical blank is reached. Upo may not complete until after the first few active lines are displayed. I streamer initiated surface address updates to this plane are allowed wh one indication in pipe status register before writing the surface address r s bit set.	All e surface dates en this bit egister
9	1b Asynchro Project: Default Va This bit w address v during ve Restricti - No is - W ag	X-tiled Drous_Sur alue: <i>i</i> II enable a will change will change ortical blank ons: o command enabled. 'ait for flip d gain with thi Name	Plane uses X-tiled memory face_Address_Update_Enable All Ob synchronous updates of the surface address when written by MMIO. Th with the next TLB request or when start of vertical blank is reached. Upd may not complete until after the first few active lines are displayed. I streamer initiated surface address updates to this plane are allowed wh one indication in pipe status register before writing the surface address r s bit set. Description Surface Address MMIO writes will update synchronous to start of	All e surface dates en this bit egister Project



See DSPACNTR - Primary Plane Source Pixel Format Mapping of Bits to Colors

4.1.9.2 DSPBLINOFF—Primary B Linear Offset Register

	DSPE	3LINOFF—Primary B Linear Offset Register		
Register Type:		MMIO		
Address Offset:		71184h		
Project:		All		
Default Va	lue:	0000000h		
Access:		R/W		
Size (in bit	ts):	32		
Double Bu	Iffer Update Point:	Start of vertical blank or pipe disabled		
Bit		Description		
31:0	Primary_Linear_Offset			All
	Primary_Linear_Offset Project: All This register provides the linear panning byte offset into the primary plane. This value is added to the surface address to get the address of the first pixel to be displayed. This offset must be at least pixel aligned. When performing 180° rotation, the unpanned offset must be the difference between the last pixel of the last line of the display data in its unrotated orientation and the display surface address. When the surface is tiled, the contents of this register are ignored.			el

4.1.9.3 DSPBSTRIDE—Primary B Stride Register

	DSPBSTRIDE—Primary B Stride Register						
Register Ty	/pe:	MMIO					
Address O	ffset:	71188h					
Project:		All					
Default Val	ue:	0000000h					
Access:		R/W					
Size (in bit	s):	32					
	ffer Update Point: ffer Armed By:	Start of vertical blar Write to DSPBSU	nk or pipe disabled or primary disabled, afte IRF	r armed			
Bit	Description						
31:16	Reserved Pro	ect: All	Format:	MBZ			



	DSPBSTRIDE—Primary B Stride Register							
15:6	Primary_Stride	Project: All						
	aligned. When using tiled memory, line to line increment for the display.	the in bytes. When using linear memory, this must be 64 byte this must be 512 byte aligned. This value is used to determine the This register is updated through either a command packet passed es to this register. The stride is limited to a maximum of 32K bytes						
5:0	Reserved Project: All	Format: MBZ						

4.1.9.4 DSPBSURF—Primary B Surface Base Address Register

	DSPBS	SURF—	Primary B Su	Irface Base	Address Reg	giste	er
Register T	ype:	MMI	0				
Address O	ffset:	7119	9Ch				
Project:		All					
Default Val	ue:	0000	0000h				
Access:							
Size (in bit	s):	32					
Double Bu	ffer Update Point	t: Star	t of vertical blank o	r pipe disabled			
Writes to t	his register arr	n DSPB I	registers				
Bit				Description			
31:12	Primary_Surfac	e_Base_	Address				
	Project:	All					
	Address:	Gr	aphicsAddress[31:	12]			
	(x, y) offsets in t	the DSPB		When the surfa	e surface is tiled, pa ace is in linear mem		
	tiled memory, th software or by c	is address ommand p	must be 256K alig backets in the comr	ned. This regis	ronous flips and the ster can be written o t represents an offs ough the global GT	directl set fro	y through
11:3	Reserved	Project:	All		Forn	nat:	
2	Reserved	Project:	ILK		Forn	nat:	MBZ
0	Reserved	Project:	All		Forn	nat:	MBZ



4.1.9.5 DSPBTILEOFF—Primary B Tiled Offset Register

Address Offset:
Default:
Normal Access:
Double Buffer Update Point:
Size:

711A4h 00000000h Read/Write Start of vertical blank or pipe disabled 32 bits

This register specifies the panning for the display surface. The surface base address is specified in the DSPBSURF register, and this register is used to describe an offset from that base address. When the surface is in linear memory, the offset is specified in the DSPBLINOFF register and the contents of this register are ignored. When the surface is tiled, the start position is specified in this register as an (x, y) offset from the beginning of the surface.

Bit	Descriptions
31:28	Reserved: Write as zero
27:16	Primary Start Y-Position: These 12 bits specify the vertical position in lines of the beginning of the active display plane relative to the display surface. When performing 180° rotation, this field specifies the vertical position of the lower right corner relative to the start of the active display plane in the unrotated orientation.
15:12	Reserved: Write as zero
11:0	Primary Start X-Position: These 12 bits specify the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. When performing 180° rotation, this field specifies the horizontal position of the lower right corner relative to the start of the active display plane in the unrotated orientation.

4.1.9.6 DSPBSURFLIVE—Primary B Live Surface Base Address

	DSPE	SURFLIVE—Primary B Live Surface Base Address
Register Ty	pe: MMIO	
Address O	ffset: 711ACh	
Project:	All	
Default Val	ue: 0000000)0h
Access:	Read O	nly
Size (in bit	s): 32	
Bit		Description
31:0	Primary_Live	_Surface_Base_Address
	Project:	All
	Address:	GraphicsAddress[31:0]
	This gives the	live value of the surface base address as being currently used for the plane.



4.1.10 Video Sprite A Control

Two video sprites are provided for the display of video content. These sprite planes provide windowing and keying functions as well as gamma and color space conversion from YUV to RGB. Each sprite plane is attached to only one of the pipes, Video Sprite A to pipe A and Video Sprite B to pipe B. Apart from the pipe assignments, the functionality is identical.

The DVSACNTR, DVSASTRIDE, DVSAPOS, DVSASIZE, and DVSASCALE active registers will be updated on the vertical blank or when pipe is disabled, after the DVSASURF trigger register is written, or when the sprite A is not yet enabled – thus providing an atomic update of the video sprite A control, stride, position, size, scale, and base address registers.

		DVS	ACNTR—Video Sprite A Control Register	
Register ⁻	Туре:		MMIO	
Address (Offset:		72180h	
Project:			All	
Default Va	alue:		0000000h	
Access:			R/W	
Size (in b	its):		32	
Double B	uffer Update	e Point:	Start of vertical blank or pipe disabled or sprite disabled, after armed	
Double B	uffer Armed	By:	Write to DVSASURF	
∕ideo Spr	rite A Plane	is connec	ted to pipe A only.	
Bit			Description	
31	Sprite_E	nable	Project: All Format: Enable	
	When this memory f	s bit is set, t etches ceas	the sprite plane will generate pixels for display. When set to zero, sprite se and plane output is transparent. The display pipe must be enabled to	enable
	When this memory f the plane internally	s bit is set, t etches ceas . When in S buffered an	the sprite plane will generate pixels for display. When set to zero, sprite	enable
30	When this memory f the plane internally Gamma	s bit is set, t etches ceas . When in S buffered an	the sprite plane will generate pixels for display. When set to zero, sprite se and plane output is transparent. The display pipe must be enabled to Self Refresh Big FIFO mode, write to this register to enable the plane will ad delayed while Big FIFO mode is exiting.	enable
	When this memory f the plane internally Gamma_ Project:	s bit is set, t etches ceas . When in S buffered an Enable	the sprite plane will generate pixels for display. When set to zero, sprite se and plane output is transparent. The display pipe must be enabled to Self Refresh Big FIFO mode, write to this register to enable the plane will ad delayed while Big FIFO mode is exiting.	enable
	When this memory f the plane internally Gamma	s bit is set, t etches ceas . When in S buffered an Enable	the sprite plane will generate pixels for display. When set to zero, sprite se and plane output is transparent. The display pipe must be enabled to Self Refresh Big FIFO mode, write to this register to enable the plane will ad delayed while Big FIFO mode is exiting.	enable
	When this memory f the plane internally Gamma_ Project: Default V There are correction display pl	s bit is set, t etches ceas . When in S buffered an Enable alue: e two gamm in the disp ane. Gamr	the sprite plane will generate pixels for display. When set to zero, sprite se and plane output is transparent. The display pipe must be enabled to Self Refresh Big FIFO mode, write to this register to enable the plane will ad delayed while Big FIFO mode is exiting.	o enable I be ne gamma ta from this
	When this memory f the plane internally Gamma_ Project: Default V There are correction display pl	s bit is set, t etches ceas . When in S buffered an Enable alue: e two gamm in the disp ane. Gamr	the sprite plane will generate pixels for display. When set to zero, sprite se and plane output is transparent. The display pipe must be enabled to Self Refresh Big FIFO mode, write to this register to enable the plane will ad delayed while Big FIFO mode is exiting. All Ob na adjustments possible in the video sprite data path. This bit controls the play pipe not the gamma control in this plane. It affects only the pixel data ma correction logic that is contained in the video sprite is disabled by load	o enable I be ne gamma ta from this
	When this memory f the plane internally Project: Default V There are correction display pl default va	s bit is set, t etches ceas . When in S buffered an Enable alue: e two gamm in the disp ane. Gamr lues into th	the sprite plane will generate pixels for display. When set to zero, sprite se and plane output is transparent. The display pipe must be enabled to Self Refresh Big FIFO mode, write to this register to enable the plane will ad delayed while Big FIFO mode is exiting. All Ob na adjustments possible in the video sprite data path. This bit controls the play pipe not the gamma control in this plane. It affects only the pixel da ma correction logic that is contained in the video sprite is disabled by loa nose registers.	b enable I be ne gamma ta from this ading the

4.1.10.1 DVSACNTR—Video Sprite A Control Register



29	Reserve	d Proj	ect: All	Format	: MBZ		
28	YUV_By	pass_Exce	ss-512_Format_	Conversion			
	Project:		All				
	Default V	alue:	0b				
	Value	Name	Description		Project		
	0b	Disable	Disable excess	s-512 conversion	All		
	1b	Enable	Enable excess	-512 conversion	All		
27	Range_C	Correction_	Disable				
	Project:		All				
	Default V	alue:	0b				
	expanded	d to full rang	ge RGB, setting t	e correction logic. Normally the range comp his bit will generate range compressed RGB. erial is used. This bit has no effect on RGB s	This bit shou	uld also	
	Value	Name	Description		Project		
	0b	Frahla	Denge correcti				
	00	Enable	Range correcti	All			
	00 1b	Disable	No range correction		All		
26:25	1b		No range corre				
26:25	1b	Disable	No range corre				
26:25	1b Source_	Disable Pixel_Form	No range corre				
6:25	1b Source_ Project: Default V This field	Disable Pixel_Form alue:	No range corre nat DevSNB 0b pixel format for t		All	t is	
6:25	1b Source_ Project: Default V This field	Disable Pixel_Form alue: selects the	No range corre nat DevSNB 0b pixel format for t	ection	All	t is Projec	
6:25	1b Source_ Project: Default V This field converted	Disable Pixel_Form alue: selects the d to 12 bits	No range corre nat DevSNB 0b pixel format for t per pixel.	ection the sprite. Before entering the blender, each	All source forma	<u>г</u>	
6:25	1b Source_ Project: Default V This field converted Value	Disable Pixel_Form alue: selects the to 12 bits Name YUV 4:2::	No range corre nat DevSNB 0b pixel format for t per pixel.	the sprite. Before entering the blender, each Description YUV 4:2:2 packed pixel format (byte order	All source forma	Projec	
6:25	1b Source_ Project: Default V This field converted Value 00b	Disable Pixel_Form alue: selects the to 12 bits Name YUV 4:2:: RGB 32-b	No range corre nat DevSNB Ob pixel format for t per pixel.	the sprite. Before entering the blender, each Description YUV 4:2:2 packed pixel format (byte order programmed separately) RGB 32-bit 2:10:10:10 pixel format (color of the second s	All source forma	Projec All	



26:25	Source_	Pixel_Form	nat				
	Project:		ILK				
	Default Value: 0b						
	This field selects the pixel format for the sprite. Before entering the blender, each source format is converted to 12 bits per pixel.						
	Value	Name	Description	Project			
	00b	YUV 4:2:2	2 YUV 4:2:2 packed pixel format (byte order programmed separately)	All			
	01b	Reserved	Reserved	All			
	10b	32-bit BG	RX 32-bit BGRX (8:8:8:8 MSB-X:R:G:B) pixel format. Ignore alpha.	All			
	11b	Reserved	Reserved	All			
24	Bino Col	lor Space	_Conversion_Enable				
24	Fibe_co	ioi Space					
	Project	- • -					
		alue: nables pipe	All 0b e color space conversion for the plane pixel data. This is separate from the				
	Default V This bit e conversion the formation	alue: mables pipe on logic with at of the plan	All Ob e color space conversion for the plane pixel data. This is separate from the nin the sprite plane. CSC mode in the pipe CSC registers must be set to ma ne pixel data after the color conversion logic within the sprite plane.	atch			
	Default V This bit e conversio	alue: nables pipe on logic with	All Ob e color space conversion for the plane pixel data. This is separate from the nin the sprite plane. CSC mode in the pipe CSC registers must be set to ma ne pixel data after the color conversion logic within the sprite plane. Description				
	Default V This bit e conversio the forma	alue: mables pipe on logic with at of the plan	All Ob e color space conversion for the plane pixel data. This is separate from the nin the sprite plane. CSC mode in the pipe CSC registers must be set to ma ne pixel data after the color conversion logic within the sprite plane. Description F Plane pixel data bypasses the pipe color space conversion logic A	atch Project			
23	Default V This bit e conversio the forma Value 0b	alue: enables pipe on logic with at of the plan Name Disable Enable	All Ob e color space conversion for the plane pixel data. This is separate from the nin the sprite plane. CSC mode in the pipe CSC registers must be set to man ne pixel data after the color conversion logic within the sprite plane. Description F Plane pixel data bypasses the pipe color space conversion logic A Plane pixel data passes through the pipe color space conversion logic	atch Project			
23 22	Default V This bit e conversio the forma Value 0b 1b Reserved	alue: enables pipe on logic with at of the plan Name Disable Enable	All Ob e color space conversion for the plane pixel data. This is separate from the in the sprite plane. CSC mode in the pipe CSC registers must be set to man ne pixel data after the color conversion logic within the sprite plane. Description F Plane pixel data bypasses the pipe color space conversion logic A Plane pixel data passes through the pipe color space conversion A logic Format: MBZ	atch Project			
	Default V This bit e conversio the forma Value 0b 1b Reserved	alue: alue: on logic with at of the plan Name Disable Enable	All Ob e color space conversion for the plane pixel data. This is separate from the in the sprite plane. CSC mode in the pipe CSC registers must be set to man ne pixel data after the color conversion logic within the sprite plane. Description F Plane pixel data bypasses the pipe color space conversion logic A Plane pixel data passes through the pipe color space conversion A logic Format: MBZ	atch Project			
	Default V This bit e conversio the forma Value 0b 1b Reserved Sprite_S	alue: inables pipe on logic with at of the plan Name Disable Enable d Proje ource_Key	All Ob e color space conversion for the plane pixel data. This is separate from the nin the sprite plane. CSC mode in the pipe CSC registers must be set to man ne pixel data after the color conversion logic within the sprite plane. Description F Plane pixel data bypasses the pipe color space conversion logic A Plane pixel data passes through the pipe color space conversion logic A Plane pixel data passes through the pipe color space conversion logic A Plane pixel data passes through the pipe color space conversion logic A Enable	atch Project			
	Default V This bit e conversion the formation Ob 1b Reserved Sprite_S Project: Default V This bit e	alue: nables pipe on logic with at of the plan Name Disable Enable d Proje ource_Key alue: nables sour	All Ob e color space conversion for the plane pixel data. This is separate from the in the sprite plane. CSC mode in the pipe CSC registers must be set to man ne pixel data after the color conversion logic within the sprite plane. Description f Plane pixel data bypasses the pipe color space conversion logic f Plane pixel data passes through the pipe color space conversion logic f Plane pixel data passes through the pipe color space conversion for f ect: All Format: MBZ -Enable All	Project All			
	Default V This bit e conversion the formation Ob 1b Reserved Sprite_S Project: Default V This bit e	alue: nables pipe on logic with at of the plan Name Disable Enable d Proje ource_Key alue: nables sour	All Ob e color space conversion for the plane pixel data. This is separate from the in the sprite plane. CSC mode in the pipe CSC registers must be set to ma ne pixel data after the color conversion logic within the sprite plane. Description F Plane pixel data bypasses the pipe color space conversion logic A Plane pixel data passes through the pipe color space conversion logic A Plane pixel data passes through the pipe color space conversion logic A Plane pixel data passes through the pipe color space conversion logic A Enable All Ob rce color keying. Sprite pixel values that match (within range) the key will b	Project All			
	Default V This bit e conversion the format Ob 1b Reserved Sprite_S Project: Default V This bit e transpare	alue: alue: alue: at of the plan Name Disable Enable Disable Control Con	All Ob e color space conversion for the plane pixel data. This is separate from the nin the sprite plane. CSC mode in the pipe CSC registers must be set to man ne pixel data after the color conversion logic within the sprite plane. Description F Plane pixel data bypasses the pipe color space conversion logic F Plane pixel data passes through the pipe color space conversion logic F Plane pixel data passes through the pipe color space conversion for the logic F ect: All Format: MBZ -Enable All Ob rce color keying. Sprite pixel values that match (within range) the key will be key can not be enabled if destination key is enabled.	Project All			



21	Plane_Ex	xtended_Ra	nge_Source_Select						
	Project:		DevSNB						
	Default Value: 0b								
	extended plane ext	range. This	licate when the plane source pixel format should be processed as has is only valid with certain source pixel formats. If the pipe is extend a source is not selected, the plane will fit the source pixel data into the drange.	ed range and					
	Value	Name	Description Proje	ct					
	0b	Normal	Normal range source selected All						
	1b	Extended	Extended range source selected All						
21	Reserved	d Proje	ct: ILK Format:						
20	RGB_Co	lor_Order							
	Project [.]		DouCNID	RGB_Color_Order					
	Project: DevSNB								
	Default V	alue:	0b						
	Default V	is used to s		ts, this field					
	Default V This field	is used to s	Ob						
	Default V This field is ignored	l is used to s d.	0b elect the color order when using RGB data formats. For other formation						
	Default V This field is ignored Value	l is used to s d. Name	Ob elect the color order when using RGB data formats. For other formation Description						
20	Default V This field is ignored Value 0b	l is used to s d. BGRX RGBX	Ob elect the color order when using RGB data formats. For other formation Description Projection BGRX (MSB-X:R:G:B) All RGBX (MSB-X:B:G:R) All						
20	Default V This field is ignored Value 0b 1b Reserved	l is used to s d. BGRX RGBX	Ob elect the color order when using RGB data formats. For other format Description Projet BGRX (MSB-X:R:G:B) All RGBX (MSB-X:B:G:R) All ct: ILK						
-	Default V This field is ignored Value 0b 1b Reserved	l is used to s d. Name BGRX RGBX d Proje	Ob elect the color order when using RGB data formats. For other format Description Projet BGRX (MSB-X:R:G:B) All RGBX (MSB-X:B:G:R) All ct: ILK						
-	Default V This field is ignored 0b 1b Reserved Color_Co	l is used to s d. Name BGRX RGBX d Proje onversion_I	Ob elect the color order when using RGB data formats. For other format Description Projet BGRX (MSB-X:R:G:B) All RGBX (MSB-X:B:G:R) All ct: ILK Disabled Format:						
-	Default V This field is ignored 0b 1b Reserved Project: Default V This bit e	l is used to s d. Name BGRX RGBX d Proje onversion_f alue: enables or dis to be used v	Ob elect the color order when using RGB data formats. For other format Description Projet BGRX (MSB-X:R:G:B) All RGBX (MSB-X:B:G:R) All ct: ILK Format: Disabled All All	ct 					
-	Default V This field is ignored 0b 1b Reserved Project: Default V This bit e intended	l is used to s d. Name BGRX RGBX d Proje onversion_f alue: enables or dis to be used v	Ob elect the color order when using RGB data formats. For other format Description Projet BGRX (MSB-X:R:G:B) All RGBX (MSB-X:B:G:R) All ct: ILK Format: Disabled All Ob sables the color conversion logic internal to the sprite. Color conversion	ct 					
-	Default V This field is ignored 0b 1b Reserved Color_Co Project: Default V This bit e intended source fo	l is used to s d. Name BGRX RGBX d Proje onversion_f alue: enables or dis to be used v ormats.	Ob elect the color order when using RGB data formats. For other format Description Projet BGRX (MSB-X:R:G:B) All RGBX (MSB-X:B:G:R) All ct: ILK Format: Disabled All Ob sables the color conversion logic internal to the sprite. Color conversion the formats that support YUV format. This bit is ignored when used with the formats that support YUV format. This bit is ignored when used with the formatic that support YUV format. This bit is ignored when used with the formatic that support YUV format. This bit is ignored when used with the formatic that support YUV format. This bit is ignored when used with the formatic that support YUV format. This bit is ignored when used with the formatic that support YUV format. This bit is ignored when used with the formatic that support YUV format. This bit is ignored when used with the formatic that support YUV format. This bit is ignored when used with the formatic that support YUV format.	ct sion is sing RGB					



18	YUV_For	mat		
10	Project:		All	
	Default V	alue:	Ob	
			e source YUV format for the YUV to RGB color co e data is RGB.	nversion operation. This field is
	Value	Name	Description	Project
	0b	BT.601	ITU-R Recommendation BT.601	All
	1b	BT.709	ITU-R Recommendation BT.709	All
7:16		- Ordor		
/:10	YUV_Byt	e_Order		
	Droject		A II	
	Project: Default V	alue:	All Ob	
	Default V	is used to		formats. For other formats, this
	Default V This field	is used to	Ob	formats. For other formats, this Project
	Default V This field field is ig	l is used to nored.	0b select the byte order when using YUV 4:2:2 data	
	Default V This field field is ig Value	is used to nored.	0b select the byte order when using YUV 4:2:2 data Description	Project
	Default V This field field is ig Value 00b	l is used to nored. Name YUYV	0b select the byte order when using YUV 4:2:2 data Description YUYV (8:8:8:8 MSB-V:Y ₂ :U:Y ₁)	Project All
	Default V This field field is ig Value 00b 01b	I is used to nored. Name YUYV UYVY	Ob select the byte order when using YUV 4:2:2 data Description YUYV (8:8:8:8 MSB-V:Y ₂ :U:Y ₁) UYVY (8:8:8:8 MSB-Y ₂ :V:Y ₁ :U)	Project All All
15	Default V This field field is ig 00b 01b 10b 11b	NameYUYVYUYVYVYUYVYUYVYU	Ob select the byte order when using YUV 4:2:2 data Description YUYV (8:8:8:8 MSB-V:Y_2:U:Y_1) UYVY (8:8:8:8 MSB-Y_2:V:Y_1:U) YVYU (8:8:8:8 MSB-U:Y_2:V:Y_1) VYUY (8:8:8:8 MSB-U:Y_2:U:Y_1) VYUY (8:8:8:8 MSB-U:Y_2:U:Y_1)	Project All All All
15	Default V This field field is ig 00b 01b 10b 11b 180°_Dis	is used to nored. Name YUYV UYVY YVYU	Ob select the byte order when using YUV 4:2:2 data Description YUYV (8:8:8:8 MSB-V:Y_2:U:Y_1) UYVY (8:8:8:8 MSB-Y_2:V:Y_1:U) YVYU (8:8:8:8 MSB-U:Y_2:V:Y_1) VYUY (8:8:8:8 MSB-U:Y_2:U:Y_1) VYUY (8:8:8:8 MSB-U:Y_2:U:Y_1)	Project All All All
15	Default V This field field is ig 00b 01b 10b 11b	I is used to nored. Name YUYV UYVY VYVU VYUY VYUY Splay_Rota	Ob select the byte order when using YUV 4:2:2 data Description YUYV (8:8:8:8 MSB-V:Y_2:U:Y_1) UYVY (8:8:8:8 MSB-Y_2:V:Y_1:U) YVYU (8:8:8:8 MSB-U:Y_2:V:Y_1) VYUY (8:8:8:8 MSB-U:Y_2:V:Y_1) VYUY (8:8:8:8 MSB-Y_2:U:Y_1:V)	Project All All All
15	Default V This field field is ig 00b 01b 10b 11b 180°_Dis Project: Default V This moo the surfa	I is used to nored. Name YUYV YUYV YVYU YVYU YVYU YUYV Splay_Rota alue: de causes t ce address	Ob select the byte order when using YUV 4:2:2 data Description YUYV (8:8:8:8 MSB-V:Y_2:U:Y_1) UYVY (8:8:8:8 MSB-Y_2:V:Y_1:U) YVYU (8:8:8:8 MSB-U:Y_2:V:Y_1) VYUY (8:8:8:8 MSB-U:Y_2:V:Y_1) VYUY (8:8:8:8 MSB-U:Y_2:V:Y_1) VYUY (8:8:8:8 MSB-U:Y_2:U:Y_1) All	Project All All All All All HI All State All All All All All All All All All
15	Default V This field field is ig 00b 01b 10b 11b 180°_Dis Project: Default V This moo the surfa	I is used to nored. Name YUYV YUYV YVYU YVYU YVYU YUYV Splay_Rota alue: de causes t ce address	Ob select the byte order when using YUV 4:2:2 data Description YUYV (8:8:8:8 MSB-V:Y_2:U:Y_1) UYVY (8:8:8:8 MSB-Y_2:V:Y_1:U) YVYU (8:8:8:8 MSB-Y_2:V:Y_1) VYUY (8:8:8:8 MSB-Y_2:U:Y_1) VYUY (8:8:8:8 MSB-Y_2:U:Y_1) VYUY (8:8:8:8 MSB-Y_2:U:Y_1) VYUY (8:8:8:8 MSB-Y_2:U:Y_1:V)	Project All All All All All HI All State All All All All All All All All All
15	Default V This field field is ig 00b 01b 10b 11b 180°_Dis Project: Default V This moo the surfa as relativ	is used to nored. Name YUYV YUYV YVYU YVYU YVYU YVYU YUYV eplay_Rota alue: de causes t ce address ve to the low	Ob select the byte order when using YUV 4:2:2 data Description YUYV (8:8:8:8 MSB-V:Y_2:U:Y_1) UYVY (8:8:8:8 MSB-Y_2:V:Y_1:U) YVYU (8:8:8:8 MSB-U:Y_2:V:Y_1) VYUY (8:8:8:8 MSB-Y_2:U:Y_1:V) VYUY (8:8:8:8 MSB-Y_2:U:Y_1:V)	Project All All All All All All It is bit, software must also set nage and calculate the x, y offset



14	Trickle-F	eed_Enab	le			
	Project:		DevSNB			
	Default V	alue:	Ob			
	Value	Name	Description	ription		
	0b	Enable	Trickle Feed Enabled - Data requests a space in the Display Data Buffer	re sent whenever ther	re is All	
	1b	Disable	Trickle Feed Disabled - Data requests a	are sent in bursts.	All	
14	Reserved	I Proj	ect: ILK	Format:		
13:11	Reserved	l Proj	ect: All	Format:		
10	Tiled_Su	rface				
	Project:		All			
	Default V	alue:	Ob			
	This bit indicates that the surface data is in tiled memory. The tile pitch is specified in bytes in the					
			at the surface data is in tiled memory. The ter. Only X tiling is supported for display s		in bytes in the	
	DVSAST	RIDE regis s bit is set,		surfaces.	-	
	DVSAST When this	RIDE regis s bit is set,	ter. Only X tiling is supported for display s	surfaces. e DVSASTART and D	-	
	DVSAST When this registers.	RIDE regis s bit is set,	ter. Only X tiling is supported for display s it affects the hardware interpretation of th	surfaces. e DVSASTART and D	VSASURFADDR	
	DVSAST When this registers.	RIDE regis s bit is set, Name	ter. Only X tiling is supported for display s it affects the hardware interpretation of th Description	surfaces. e DVSASTART and D	PVSASURFADDR	
9:3	DVSAST When thi registers.	RIDE regis s bit is set, Name Linear Tiled	ter. Only X tiling is supported for display s it affects the hardware interpretation of th Description Linear memory Tiled memory	surfaces. e DVSASTART and D	Project	
9:3	DVSAST When this registers. Value 0b 1b Reserved	RIDE regis s bit is set, Name Linear Tiled	ter. Only X tiling is supported for display s it affects the hardware interpretation of the Description Linear memory Tiled memory ect: All	surfaces. e DVSASTART and D	Project All	
	DVSAST When this registers. Value 0b 1b Reserved	RIDE regis s bit is set, Name Linear Tiled Proj	ter. Only X tiling is supported for display s it affects the hardware interpretation of the Description Linear memory Tiled memory ect: All	surfaces. e DVSASTART and D	Project All	
	DVSAST When this registers. 0b 1b Reserved Sprite_D	RIDE regis s bit is set, Name Linear Tiled Tiled Proj estination	ter. Only X tiling is supported for display s it affects the hardware interpretation of th Description Linear memory Tiled memory ect: All _Key	surfaces. e DVSASTART and D	Project All	
	DVSAST When this registers. 0b 1b Reserved Sprite_D Project: Default V This bit e key value	RIDE regis s bit is set, Name Linear Tiled Proj estination alue: nables the in DVSAK	ter. Only X tiling is supported for display s it affects the hardware interpretation of the Description Linear memory Tiled memory ect: All _Key All	surfaces. e DVSASTART and D Format:	DVSASURFADDR Project All All MBZ is pipe matches the	
	DVSAST When this registers. 0b 1b Reserved Sprite_D Project: Default V This bit e key value through t	RIDE regis s bit is set, Name Linear Tiled Tiled Proj estination alue: nables the in DVSAK	ter. Only X tiling is supported for display s it affects the hardware interpretation of the Description Linear memory Tiled memory ect: All _Key All _Ob destination key function. If the pixel for th CEYVAL the sprite pixel is used, otherwise	surfaces. e DVSASTART and D Format: Format: he primary plane on this the primary plane pixe enabled if source key i	DVSASURFADDR Project All All MBZ is pipe matches the	
	DVSAST When this registers. 0b 1b Reserved Sprite_D Project: Default V This bit e key value through t	RIDE regis s bit is set, Name Linear Tiled Proj estination alue: nables the in DVSAK	ter. Only X tiling is supported for display s it affects the hardware interpretation of the Description Linear memory Tiled memory ect: All _Key All 0b destination key function. If the pixel for th CEYVAL the sprite pixel is used, otherwise unmodified. Destination Key can not be e	surfaces. e DVSASTART and D Format: Format:	oVSASURFADDR Project All All MBZ is pipe matches the set is passed is enabled.	

Sprite Source Pixel Format Mapping of Bits to Colors: Note: For RGB formats, see the primary source pixel format mapping



SPRITE YUV	Y1	U	Y2	V
YUV 4:2:2 YUYV	7:0	15:8	23:16	31:24
YUV 4:2:2 UYVY	15:8	7:0	31:24	23:16
YUV 4:2:2 YVYU	7:0	31:24	23:16	15:8
YUV 4:2:2 VYUY	15:8	23:16	31:24	7:0



4.1.10.2 DVSALINOFF—Video Sprite A Linear Offset Register

	DVSAL	INOFF—Video Sprite A Linear Offset Register
Register T		
Address O		72184h
Project:		All
Default Val	lue:	0000000h
Access:		R/W
Size (in bit	s):	32
	ffer Update Point:	Start of vertical blank or pipe disabled
Bit		Description
31:0	Sprite_Linear_Offs	set Project: All Format:
	surface address to g aligned for RGB for unpanned offset mu	es the linear panning byte offset into the sprite plane. This value is added to the get the address of the first pixel to be displayed. This offset must be at least pixel mats and even pixel aligned for YUV formats. When performing 180° rotation, the ust be the difference between the last pixel of the last line of the display data in its n and the display surface address. When the surface is tiled, the contents of this .

4.1.10.3 DVSASTRIDE—Video Sprite A Stride Register

DVSASTRIDE—Video Sprite A Stride Register				
Register Type:		MMIO		
Address Offset:		72188h		
Project:		All		
Default Value:		0000000h		
Access:		R/W		
Size (in bits):		32		
Double Buffer Update Point:		Start of vertical blank or pipe disabled or sprite disabled, after armed		
Double Buffer Armed By:		Write to DVSASURF		
Bit	Description			
31:15	Reserved Pro	ject: All		Format:
14:6	Sprite_Stride	Project:	All	Format:
This is the stride for the sprite in bytes. When using linear memory, this must be 64 byte aligned. When using tiled memory, this must be 512 byte aligned. This register is updated through either a command packet passed through the command stream or writes to this register. The stride is limited to a maximum of 16K bytes when sprite scaling is not enabled, 4K bytes when sprite scaling is enabled, for both linear and tiled memory.				
5:0	Reserved Pro	ject: All		Format:



4.1.10.4 DVSAPOS—Video Sprite A Position Register

	DVS	SAPOS—Vie	deo Sp	orite A Positi	ion Register		
Register Ty	/pe:	MMIO					
Address O		7218Ch					
Project:		All					
Default Val	ue:	00000000h					
Access:		R/W					
Size (in bit	s):	32					
	ffer Update Point: ffer Armed By:	Start of vertication Start of VSA		r pipe disabled o	r sprite disabled, after a	armed	
This registe	is register specifies the position of the sprite. Software must take care that the sprite does not extend out the display active area. ie. Xposition + Xsize =< Xsrcsize						
Bit		Description					
31:28	Reserved Pro	ject: All			Format:	MBZ	
27:16	Sprite_Y-Position	Project:	All	Format:			
	These 12 bits specify the vertical position in lines of the sprite (upper left corner) relative to the beginning of the active video area. When performing 180° rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.						
15:12	Reserved Pro	ject: All			Format:	MBZ	
11:0	Sprite_X-Position	Project:	All	Format:			
	beginning of the act position of the origin	ive video area. N al lower right co n. The defined s	When per orner relat sprite rect	forming 180° rota tive to the origina	rite (upper left corner) ation, this field specifies I end of the active vide ys be completely conta	s the horizontal o area in the	



4.1.10.5 DVSASIZE—Video Sprite A Size Register

	D		Vic	leo Sprite A Siz	ve Register		
Double Bu	ype: ffset: ue: s): ffer Update Point: ffer Armed By:	All 00000000h R/W 32 Jpdate Point: Start of vertical blank or pipe disabled or sprite disabled, after armed					
the display	active area. ie. Xp			Xsrcsize			
Bit				Description			
31:28	Reserved Pro	ect: All			Format:	MBZ	
27:16		he defined s	sprite re		lines. The value in the r be completely contained		
15:12	Reserved Pro	ect: All			Format:	MBZ	
11:0	same as the stride l the width minus one displayable area of The sprite width (ac	but should b . The define the screen i rual width, n	e less t ed sprite mage. ot the w	han or equal to the stu e rectangle must alwa vidth minus one value	pixels. This does not ha ride in pixels. The value ys be completely contain) is limited to even values (el doubling or Pixel dout	in the register is ed within the s when YUV	



4.1.10.6 DVSAKEYVAL—Video Sprite A Color Key Value Register

	DVSAKEY	VAL—Video Sprite	A Color Key Va	alue Reg	ister	
Register Ty	/pe:	MMIO				
Address Of	ffset:	72194h				
Project:		All				
Default Val	ue:	00000000h				
Access:		R/W				
Size (in bits	s):	32				
Double But	fer Update Point:	Start of vertical blank or pi	be disabled			
matches th	e key. This register alue is the minimur	color to be used with the will only have an effect w n value for the range com	hen the sprite cold	or key is en	ablec	I. In source key
Bit		D	escription			
31:24	Reserved Proj	ect: All		Forma	ıt:	MBZ
23:16	V_Source_Key_Mir	n_Value/R_Source/Dest_Ke	ey_Value	Project:	All	Format:
	Specifies the color k or destination key co	ey (minimum) value for the s ompare value.	prite V channel sour	ce key or the	e Red	channel source
15:8	Y_Source_Key_Mir	n_Value/G_Source/Dest_K	ey_Value	Project:	All	Format:
		ey (minimum) value for the s n key compare value.	prite Y channel sour	ce key or the	e Gree	en channel
7:0	U_Source_Key_Mir	n_Value/B_Source/Dest_K	ey_Value	Project:	All	Format:
		ey (minimum) value for the s n key compare value.	prite U channel sour	ce key or th	e Blue	e channel



4.1.10.7 DVSAKEYMSK—Video Sprite A Color Key Mask Register

VSAKEYMSK—Video Sprite A Color Key Mask Register
MMIO
72198h
All
0000000h
R/W
32
e Point: Start of vertical blank or pipe disabled

For source key this register specifies which channels to perform range checking on.

For destination key this register specifies the key mask to be used with the color value bits to determine if the display source data matches the key when enabled. A zero bit in the mask indicates that the corresponding bit match failure should be ignored when determining if the pixel matches.

Note that source key and destination key are mutually exclusive modes of operation, they can not be used simultaneously. For the function that is not enabled, the associated bits in this register should be programmed to zeroes.

Bit	Description							
31:27	Reserved Project: All	Forma	at:	MBZ				
26	V/R_Channel_Source_Key_Enable	Project:	All	Format:				
	Specifies the source color key enable for the V/Red channel							
25	Y/G_Channel_Source_Key_Enable	Project:	All	Format:				
	Specifies the source color key enable for the Y/Green channel							
24	U/B_Channel_Source_Key_Enable	Project:	All	Format:				
	Specifies the source color key enable for the U/Blue channel							
23:16	R_mask_Dest_Key_Value	Project:	All	Format:				
	Specifies the destination color key mask for the sprite R channel							
15:8	G_mask_Dest_Key_Value	Project:	All	Format:				
	Specifies the destination color key mask for the sprite G channel							
7:0	B_mask_Dest_Key_Value	Project:	All	Format:				
	Specifies the destination color key mask for the sprite B channel							



	DVSAS	URF—Video Sj	orite A Surface Address Register				
Register T	Register Type: MMIO						
Address O	ffset:	7219Ch	7219Ch				
Project:		All					
Default Va	lue:	00000000h					
Access:		R/W					
Size (in bit	s):	32					
Double Bu	ffer Update Point:	Start of vertical b	ank or pipe disabled				
Writes to t	his register arm DV	'SA registers					
Bit	Description						
31:12	Sprite_Surface_B	ase_Address					
	Project:	All					
	Address:	Graphicsdress[31:12]				
	This address specifies the surface base address. When the surface is tiled, panning is specified using (x, y) offsets in the DVSATILEOFF register. When the surface is in linear memory, panning is specified using a linear offset in the DVSALINOFF register.						
	This address must be 4K aligned. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. The value in this register is updated through the command streamer with synchronous flips.						
11:0	Reserved Pr	oject: All	Format:				

4.1.10.8 DVSASURF—Video Sprite A Surface Address Register



4.1.10.9 DVSAKEYMAXVAL—Video Sprite A Color Key Max Value Register

	DVSAKEYMAX	VAL—Video Sprite A Colo	or Key Max Value R	egister
Register T	ype:	MMIO		
Address O	ffset:	721A0h		
Project:		All		
Default Val	lue:	0000000h		
Access:		R/W		
Size (in bit	s):	32		
Double Bu	ffer Update Point:	Start of vertical blank or pipe disable	led	
matches th		color to be used with the mask bi r will only have an effect when the	•	
Bit		Descriptio	on	
31:24	Reserved Proj	iect: All	Format:	MBZ
23:16	V_Key_Max_Value		Project: Al	I Format:
	Specifies the color k	ey value for the sprite V channel		
15:8	Y_Key_Max_Value		Project: Al	I Format:
	Specifies the color k	ey value for the sprite Y channel		
7:0	U_Key_Max_Value		Project: Al	I Format:
	Specifies the color k	ey value for the sprite U channel		

4.1.10.10 DVSATILEOFF—Video Sprite A Tiled Offset Register

DVSATILEOFF—Video Sprite A Tiled Offset Register							
Register Type:	ter Type: MMIO						
Address Offset:	Iress Offset: 721A4h						
Project:	roject: All						
Default Value:	ault Value: 00000000h						
Access:	Access: R/W						
Size (in bits): 32							
Double Buffer Update	Double Buffer Update Point: Start of vertical blank or pipe disabled						
This register specifies the panning for the sprite surface in tiled memory. The surface base address is specified in the DVSASURFADDR register, and this register is used to describe an offset from that base address. When the surface is in linear memory, the offset is specified in the DVSALINOFF register and the contents of this register are ignored. When the surface is tiled, the start position is specified in this register							
as an (x, y) offset from the beginning of the surface.							
Bit	Description						
31:28 Reserved	Project:	4II		Format:	MBZ		



27:16	Sprite_Start_Y-Position	Project: All Format:					
	These 12 bits specify the vertical position in lines of the beginning of the active display plane relative to the display surface. When performing 180° rotation, this field specifies the vertical position of the lower right corner relative to the start of the active display plane in the unrotated orientation.						
15:12	Reserved Project: All	Format: MBZ					
11:0	Sprite_Start_X-Position	Project: All Format:					
	Sprite_Start_X-Position Project: All Format: These 12 bits specify the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. The offset must be even pixel aligned for YUV formats. When performing 180° rotation, this field specifies the horizontal position of the lower right corner relative to the start of the active display plane in the unrotated orientation.						

4.1.10.11 DVSASURFLIVE—Video Sprite A Live Surface Base Address Register

D	VSASUR	FLIVE—Video Sprite A Live Surface Base Address Register
Register T	ype: MMIC	
Address O	ffset: 721A	Ch
Project:	All	
Default Va	lue: 00000	1000h
Access:	Read	Only
Size (in bit	s): 32	
Bit		Description
31:0	Sprite_Sur	ace_Base_Address
	Project:	All
	Address:	GraphicsAddress[31:0]
	This gives t	ne live value of the surface base address as being currently used for the plane.



4.1.10.12 DVSASCALE—Video Sprite A Scaler Control

DV	DVSASCALE—Video Sprite A Scaler Control				
Register Type:	MMIO				
Address Offset:	72204h				
Project:	All				
Default Value:	0000000h				
Access:	R/W				
Size (in bits):	32				
Double Buffer Update Point:	Start of vertical blank or pipe disabled or sprite disabled, after armed				
Double Buffer Armed By:	Write to DVSASURF				

This register controls the sprite scaling. The DVSASIZE register gives the destination (output to pipe) size of the sprite. This register gives the source (input to sprite) size of the sprite. When scaling is enabled, the source size will be scaled up or down to the destination size.

Upscaling of any amount is allowed. Downscaling up to 16X (source/destination) is allowed. Downscaling greater than 2X will involve decimation. Downscaling increases memory bandwidth requirements. Scaling can not be used with the sprite 64bpp source pixel format. Source and destination sizes must be 3x3 (3x6 when interlacing) or greater when scaling is enabled.

Horizontal downscaling limits the maximum dot clock allowed as percent of cdclk. Rules to calculate the allowed dot clock:

Start with maximum dot clock 90% of cdclk. (There is a separate requirement that planes using 64bpp formats can not be enabled with dot clock >80% of cdclk when sprite is enabled on the same pipe) Subtract 10% more per horizontal decimation step (decimation steps at 2x, 4x, 8x, and 16x downscale). Subtract 10% more if sprite is using the RGB data format.

Subtract 10% more if sprite scaling is enabled on the other pipe.

Then divide that by horizontal downscale amount within each decimation step.

The result is the maximum allowed dot clock as percent of cdclk frequency.

Example:

Scale factor	Decimation amount	YUV single pipe dot clock %	YUV dual pipe dot clock %	RGB single pipe dot clock %	RGB dual pipe dot clock %	Comment
1	1	90	80	80	70	No scaling
1.5	1	60	53	53	46	
1.99	1	45	40	40	35	Max downscale before decimation starts
2	2	80	70	70	60	
3	2	53	46	46	40	
3.99	2	40	35	35	30	
4	4	70	60	60	50	
6	4	46	40	40	33	
7.99	4	35	30	30	25	
8	8	60	50	50	40	
12	8	40	33	33	26	
15.99	8	30	25	25	20	Worst case dot clock
16	16	50	40	40	30	Max downscaling allowed



DH			ASCALE—Video Sprite A Scaler Control			
Bit			Description			
31	Scaling_EnableProject:AllFormat:EnableEnables the scaling function.Source width can be no more than 4k bytes. For best picture quality, disable when scaling is not required.					
30:29	Filter_Co	ontrol				
	Project:		All			
	Default V Filter sele		Ob			
	Value	Name	Description	Project		
	00b	Medium	Medium Filtering	All		
	01b	Enhancing	g Edge Enhancing Filtering	All		
	10b	Softening	Edge Softening Filtering	All		
	11b	Reserved	Reserved	All		
	Default V Select the surface d	e vertical off	0b set of the filtered data. Software is responsible for updating this to matc	h the		
	Value	Name	Description	Project		
	0b	0	Vertical initial phase of 0			
	1b					
		0.5	Vertical initial phase of 0.5	All All		
27	Project: Default V	d_Field_En		All		
27	Project: Default V	d_Field_En	able All Ob	All		
27	Project: Default V Enable ad	d_Field_En alue: djustment of	able All 0b the vertical offset of the filtered data.	All		
27	Project: Default V Enable ac Value	d_Field_En	able All Ob the vertical offset of the filtered data. Description	All All Project		
27 26:16	Project: Default V Enable ad Value Ob	d_Field_En alue: djustment of Name Disable Enable	able All Ob the vertical offset of the filtered data. Description Off (Vertical initial phase is 1/2 the scale factor)	All All Project All		
	Project: Default V Enable ad Ob 1b Source_V The horiz is 3. The 4k bytes,	d_Field_En d_Field_En djustment of Disable Enable Width contal size of value progr counting frc	able All 0b the vertical offset of the filtered data. Description Off (Vertical initial phase is 1/2 the scale factor) On (Vertical initial phase is selected by the Even/Off Field Offset bit)	All All Project All All minimum nore than		



F

DVSASCALE—Video Sprite A Scaler Control					
10:0	Source_Height	Project:	All	Format:	
		x number of line	es is 204	8; minimum is 3 (the source is a field, this is the number of (6 when interlacing). The value
	The height must be e That means the prog				he pipe has set planes to interlaced fetch

4.1.10.13 DVSAGAMC—Video Sprite A Gamma Correction Registers

		DVSGAMC	Reference Point				
Project:		All					
Bit			Description				
31:30	Rese	erved	Project: A	II Format:			
29:20	Red	Gamma Reference Point	Project: A	ll Format:			
19:10	Gree	en Gamma Reference Point	Project: A	ll Format:			
9:0	Blue	Gamma Reference Point	Project: A	ll Format:			
	DVSGAMC Max Reference Point						
Project:	-	All					
Bit			Description				
31:11	Rese	erved Project: All	Forma	at:			
10:0	Fina	I Gamma Max Reference Point	Project: A	II Format:			
		DVSAGAMC—Video Sprite	A Gamma Correctio	n Registers			
Register T Address C		MMIO 72300h					
Project:		All					
Default Va	lue:	00000000h; 04010040h; 08020080h 1C0701C0h; 20080200h; 24090240h 380E0380h; 3C0F03C0h; 00000400	i; 280A0280h; 2C0B02C0h; 3				
Access:		R/W					
Size (in bit	ts):	19x32					



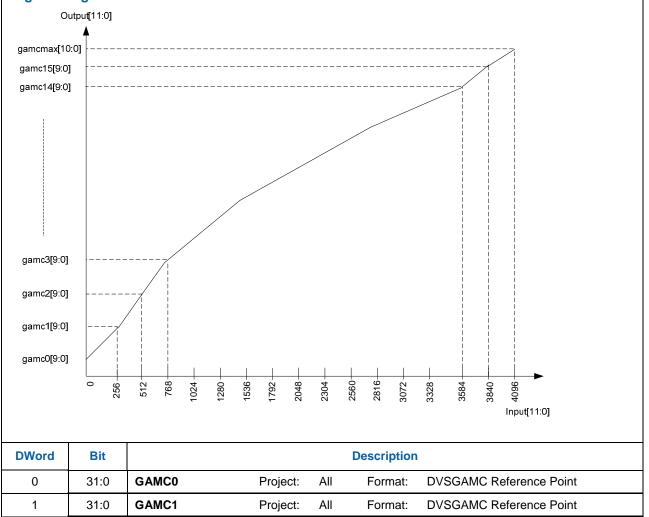
These registers are used to determine the characteristics of the gamma correction for the sprite pixel data *pre-blending*. Additional gamma correction can be done in the display pipe gamma if desired.

The gamma correction curve is represented by specifying a set of reference points spaced equally along the desired curve. Red, Green, and Blue each have 17 reference points. The first 16 reference points are 10 bit values with Red, Green, and Blue sharing a single register for each point. The final max reference point is an 11 bit value with separate registers for Red, Green, and Blue. The curve must be flat or increasing, never decreasing.

During operation the appropriate reference point pairs (adjacent) are selected for each color, and the output is interpolated between these two reference point values.

The gamma correction registers are not double-buffered. They should only be updated when the sprite is off, otherwise, screen artifacts may show.

To pass sprite pixel data through gamma correction unchanged, program the gamma reference points to the default linear ramp values. When the output from sprite is set in YUV format by programming CSC bypass, or the sprite source pixel format is RGB, the sprite gamma correction will be bypassed.



Programming of the Piecewise-linear Estimation of Gamma Correction Curve



2	31:0	GAMC2	Project:	All	Format:	DVSGAMC Reference Point
3	31:0	GAMC3	Project:	All	Format:	DVSGAMC Reference Point
4	31:0	GAMC4	Project:	All	Format:	DVSGAMC Reference Point
5	31:0	GAMC5	Project:	All	Format:	DVSGAMC Reference Point
6	31:0	GAMC6	Project:	All	Format:	DVSGAMC Reference Point
7	31:0	GAMC7	Project:	All	Format:	DVSGAMC Reference Point
8	31:0	GAMC8	Project:	All	Format:	DVSGAMC Reference Point
9	31:0	GAMC9	Project:	All	Format:	DVSGAMC Reference Point
10	31:0	GAMC10	Project:	All	Format:	DVSGAMC Reference Point
11	31:0	GAMC11	Project:	All	Format:	DVSGAMC Reference Point
12	31:0	GAMC12	Project:	All	Format:	DVSGAMC Reference Point
13	31:0	GAMC13	Project:	All	Format:	DVSGAMC Reference Point
14	31:0	GAMC14	Project:	All	Format:	DVSGAMC Reference Point
15	31:0	GAMC15	Project:	All	Format:	DVSGAMC Reference Point
16	31:0	GAMCmaxR	Project:	All	Format:	DVSGAMC Max Reference Point
17	31:0	GAMCmaxG	Project:	All	Format:	DVSGAMC Max Reference Point
18	31:0	GAMCmaxB	Project:	All	Format:	DVSGAMC Max Reference Point

4.1.11 Video Sprite B Control

The DVSBCNTR, DVSBSTRIDE, DVSBPOS, DVSBSIZE, and DVSBSCALE active registers will be updated on the vertical blank or when pipe is disabled, after the DVSBSURF trigger register is written, or when the sprite B is not yet enabled – thus providing an atomic update of the video sprite B control, stride, position, size, scale, and base address registers.



4.1.11.1 DVSBCNTR—Video Sprite B Control Register

		DVS	BCNTR—Video Sprite B Control Register			
Register Ty Address O Project: Default Val Access: Size (in bit Double But	ess Offset: ct: It Value: cs: in bits): le Buffer Update Point:		MMIO 73180h All 00000000h R/W 32 Start of vertical blank or pipe disabled or sprite disabled, afte	er armed		
Double Buffer Armed By:			Write to DVSBSURF			
Video Sprit Bit	ideo Sprite B Plane is connected to pipe B only. Bit Description					
			· · · · · · · · · · · · · · · · · · ·			
31	Sprite_EnableProject:AllFormat:EnableWhen this bit is set, the sprite plane will generate pixels for display.When set to zero, sprite planememory fetches cease and plane output is transparent.The display pipe must be enabled to enablethe plane.When in Self Refresh Big FIFO mode, write to this register to enable the plane will beinternally buffered and delayed while Big FIFO mode is exiting.					
30	Gamma_Enable					
	Project: All					
	Default V	alue:	Ob			
	correction this displa	n in the disp ay plane. G	na adjustments possible in the video sprite data path. This bit play pipe not the gamma control in this plane. It affects only t Gamma correction logic that is contained in the video sprite is to those registers.	he pixel dat	a from	
	Value	Name	Description		Project	
	0b	Disable	Plane pixel data bypasses the display pipe gamma correction	on logic	All	
	1b	Enable	Plane pixel data is gamma corrected in the pipe gamma co logic	rrection	All	
29	Reserved	d Proje	ect: All Format	:: MBZ		
28	YUV Byr	bass Exce	ss-512_Format_Conversion			
	Project:		All			
	Default V	alue:	Ob			
	Value	Name	Description	Project		
	0b	Disable	Disable excess-512 conversion	All		
	1b	Enable	Enable excess-512 conversion	All		
	•	*	•			



27	Range_C	Correction_D	lisable				
	Project:		All				
	Default Value: 0b						
	expanded	d to full range	RGB, setting this	correction logic. Normally the range compressed YUV is so bit will generate range compressed RGB. This bit shout all is used. This bit has no effect on RGB source formate	uld also		
	Value	Name	Description	Project			
	0b	Enable	Range correctior	n enabled All			
	1b	Disable	No range correct	ange correction All			
26:25	Source I	Pixel_Forma	t				
	Project:		DevSNB				
	Default V	alue:	0b				
		selects the p d to 12 bits pe		e sprite. Before entering the blender, each source forma	t is		
	Value	Name		Description			
	00b	YUV 4:2:2		YUV 4:2:2 packed pixel format (byte order programmed separately)			
	01b	RGB 32-bit 2:10:10:10		RGB 32-bit 2:10:10:10 pixel format (color order programmed separately). Ignore alpha.			
		1					
	10b	RGB 32-bit	t 8:8:8:8	RGB 32-bit 8:8:8:8 pixel format (color order programmed separately). Ignore alpha.	All		
	10b 11b		t 8:8:8:8 t 16:16:16:16	programmed separately). Ignore alpha. RGB 64-bit 16:16:16:16 floating point pixel format	All		
		RGB 64-bit Use of 64b	t 16:16:16:16 pp format will aximum dot	programmed separately). Ignore alpha.			
26:25	11b	RGB 64-bit Use of 64b limit the ma	t 16:16:16:16 pp format will aximum dot % of cdclk.	programmed separately). Ignore alpha. RGB 64-bit 16:16:16:16 floating point pixel format			
26:25	11b	RGB 64-bit Use of 64b limit the ma clock to 80 ⁶	t 16:16:16:16 pp format will aximum dot % of cdclk.	programmed separately). Ignore alpha. RGB 64-bit 16:16:16:16 floating point pixel format			
26:25	11b Source_I	RGB 64-bit Use of 64bj limit the ma clock to 80° Pixel_Forma	t 16:16:16:16 pp format will aximum dot % of cdclk.	programmed separately). Ignore alpha. RGB 64-bit 16:16:16:16 floating point pixel format			
26:25	11b Source_I Project: Default V This field	RGB 64-bit Use of 64b limit the ma clock to 80° Pixel_Forma	t 16:16:16:16 pp format will aximum dot % of cdclk. It DevILK Ob Dixel format for the	programmed separately). Ignore alpha. RGB 64-bit 16:16:16:16 floating point pixel format	All		
26:25	11b Source_I Project: Default V This field	RGB 64-bit Use of 64b limit the ma clock to 80° Pixel_Forma alue: selects the p	t 16:16:16:16 pp format will aximum dot % of cdclk. It DevILK Ob Dixel format for the	programmed separately). Ignore alpha. RGB 64-bit 16:16:16:16 floating point pixel format (color order programmed separately). Ignore alpha. e sprite. Before entering the blender, each source formation	All		
26:25	11b Source_I Project: Default V This field converted	RGB 64-bit Use of 64b limit the ma clock to 80° Pixel_Forma alue: selects the p d to 12 bits pe	t 16:16:16:16 pp format will aximum dot % of cdclk. tt DevILK 0b bixel format for the er pixel. Description	programmed separately). Ignore alpha. RGB 64-bit 16:16:16:16 floating point pixel format (color order programmed separately). Ignore alpha. e sprite. Before entering the blender, each source formation	All		
26:25	11b Source_I Project: Default V This field converted Value	RGB 64-bit Use of 64bj limit the ma clock to 80° Pixel_Forma alue: selects the p d to 12 bits pe	t 16:16:16:16 pp format will aximum dot % of cdclk. tt DevILK 0b bixel format for the er pixel. Description	programmed separately). Ignore alpha. RGB 64-bit 16:16:16:16 floating point pixel format (color order programmed separately). Ignore alpha. e sprite. Before entering the blender, each source forma	All at is Project		
26:25	11b Source_I Project: Default V This field converted Value 00b	RGB 64-bit Use of 64bj limit the ma clock to 80° Pixel_Forma alue: selects the p d to 12 bits pe Name YUV 4:2:2	t 16:16:16:16 pp format will aximum dot % of cdclk. tt DevILK 0b bixel format for the er pixel. Description YUV 4:2:2 p Reserved	programmed separately). Ignore alpha. RGB 64-bit 16:16:16:16 floating point pixel format (color order programmed separately). Ignore alpha. e sprite. Before entering the blender, each source forma	All All All All All All All All		



24	Pipe Co	lor Space	_Conversion_Enable				
- ·	Project:	opuoo_	All				
	Default Value: 0b						
	conversio	on logic with	e color space conversion for the plane pixel data. This hin the sprite plane. CSC mode in the pipe CSC regist one pixel data after the color conversion logic within the	ters must be set			
	Value	Name	Description		Project		
	0b	Disable	Plane pixel data bypasses the pipe color space conv	version logic	All		
	1b	Enable	Plane pixel data passes through the pipe color spac logic	e conversion	All		
23	Reserved	d Proj	ect: All	Format: MB2	2		
22	Sprite_S						
	Project:	ource_key					
	-	-					
	Project: Default V This bit e	alue: enables sou	All		vill become		
	Project: Default V This bit e	alue: enables sou	All 0b irce color keying. Sprite pixel values that match (withir				
	Project: Default V This bit e transpare	alue: enables sou ent. Source	All Ob arce color keying. Sprite pixel values that match (withir e key can not be enabled if destination key is enabled.				
	Project: Default V This bit e transpare	alue: enables sou ent. Source Name	All Ob Ince color keying. Sprite pixel values that match (within e key can not be enabled if destination key is enabled. Description	Project			
22	Project: Default V This bit e transpare Value 0b 1b	alue: enables sou ent. Source Name Disable	All Ob arce color keying. Sprite pixel values that match (within e key can not be enabled if destination key is enabled. Description Sprite source key is disabled Sprite source key is enabled	Project All			
22	Project: Default V This bit e transpare Value 0b 1b	alue: enables sou ent. Source Name Disable Enable	All Ob arce color keying. Sprite pixel values that match (within e key can not be enabled if destination key is enabled. Description Sprite source key is disabled Sprite source key is enabled	Project All			
22	Project: Default V This bit e transpare 0b 1b Sprite_S	alue: enables sou ent. Source Name Disable Enable ource_Key	All Ob arce color keying. Sprite pixel values that match (within key can not be enabled if destination key is enabled. Description Sprite source key is disabled Sprite source key is enabled P_Enable	Project All			
22	Project: Default V This bit e transpare 0b 1b Sprite_S Project: Default V This bit e	alue: enables sou ent. Source Name Disable Enable ource_Key alue: nables sou	All Ob arce color keying. Sprite pixel values that match (within the key can not be enabled if destination key is enabled. Description Sprite source key is disabled Sprite source key is enabled y_Enable All	Project All All			
22	Project: Default V This bit e transpare 0b 1b Sprite_S Project: Default V This bit e	alue: enables sou ent. Source Name Disable Enable ource_Key alue: nables sou	All Ob arce color keying. Sprite pixel values that match (within e key can not be enabled if destination key is enabled. Description Sprite source key is disabled Sprite source key is enabled y_Enable All Ob rce color keying. Sprite pixel values that match (within	Project All All	vill become		
22	Project: Default V This bit e transpare 0b 1b Sprite_S Project: Default V This bit e transpare	alue: mables sou ent. Source Name Disable Enable ource_Key alue: nables source	All Ob arce color keying. Sprite pixel values that match (within the key can not be enabled if destination key is enabled. Description Sprite source key is disabled Sprite source key is enabled r_Enable All Ob rce color keying. Sprite pixel values that match (within key can not be enabled if destination key is enabled.	Project All All			



21	Plana E	vtondod D	ango Souroo Soloot			
	Project:	klenueu_Ka	ange_Source_Select DevSNB			
	Default Value: 0b					
	extendec plane ext	range. Thi	dicate when the plane source pixel format should be processed as have is is only valid with certain source pixel formats. If the pipe is extende e source is not selected, the plane will fit the source pixel data into the ed range.	d range and		
	Value	Name	Description Project	t		
	0b	Normal	Normal range source selected All			
	1b	Extended	Extended range source selected All			
21	Reserved	d Proje	ect: DevILK Format:			
	Project:		DevSNB			
	Default V	is used to s	DevSNB 0b select the color order when using RGB data formats. For other format	s, this field		
	Default V This field	is used to s	Ob			
	Default V This field is ignored	l is used to s d.	0b select the color order when using RGB data formats. For other format			
	Default V This field is ignored Value	l is used to s d. Name	Ob select the color order when using RGB data formats. For other format Description Project			
20	Default V This field is ignored Value 0b	l is used to s d. BGRX RGBX	Ob Project Select the color order when using RGB data formats. For other format Project BGRX (MSB-X:R:G:B) All RGBX (MSB-X:B:G:R) All			
20 19	Default V This field is ignored Value 0b 1b Reserved	l is used to s d. BGRX RGBX d Proje	Ob Select the color order when using RGB data formats. For other format Description Project BGRX (MSB-X:R:G:B) All RGBX (MSB-X:B:G:R) All ect: DevILK			
	Default V This field is ignored 0b 1b Reserved Color_Co	l is used to s d. BGRX RGBX	Ob Select the color order when using RGB data formats. For other format Description Project BGRX (MSB-X:R:G:B) All RGBX (MSB-X:B:G:R) All ect: DevILK			
	Default V This field is ignored Value 0b 1b Reserved	l is used to s d. Name BGRX RGBX d Proje	Ob select the color order when using RGB data formats. For other format Description Project BGRX (MSB-X:R:G:B) All RGBX (MSB-X:B:G:R) All ect: DevILK Format: Disabled			
	Default V This field is ignored 0b 1b Reserved Project: Default V This bit e	A subset to s d. BGRX RGBX d Proje onversion_ alue: enables or d to be used	Ob select the color order when using RGB data formats. For other format Description Project BGRX (MSB-X:R:G:B) All RGBX (MSB-X:B:G:R) All ect: DevILK Format: Disabled All	t on is		
	Default V This field is ignored 0b 1b Reserved Color_Co Project: Default V This bit e intended	A subset to s d. BGRX RGBX d Proje onversion_ alue: enables or d to be used	Ob select the color order when using RGB data formats. For other format Description Project BGRX (MSB-X:R:G:B) All RGBX (MSB-X:B:G:R) All ect: DevILK Format: Disabled All Ob isables the color conversion logic internal to the sprite. Color conversion	t on is ing RGB		
	Default V This field is ignored 0b 1b Reserved Color_Co Project: Default V This bit e intended source fo	A subset to s d. Name BGRX RGBX d Proje Driversion_ alue: enables or d to be used primats.	Ob select the color order when using RGB data formats. For other format Description Project BGRX (MSB-X:R:G:B) All RGBX (MSB-X:B:G:R) All ect: DevILK Format: Disabled All Ob isables the color conversion logic internal to the sprite. Color converse with the formats that support YUV format. This bit is ignored when us	t on is		



		DVS	BCNTR—Video Sprite B Control Register			
18	YUV_For	mat				
	Project:		All			
	Default Value: 0b					
			e source YUV format for the YUV to RGB color conversion operati e data is RGB.	on. This field is		
	Value	Name	Description Pr	oject		
	0b	BT.601	ITU-R Recommendation BT.601 AI			
	1b	BT.709	ITU-R Recommendation BT.709 AI			
17:16	YUV_Byt	e_Order				
	Project:		All			
	Default V	alue:	Ob			
	This field field is ig		select the byte order when using YUV 4:2:2 data formats. For oth	er formats, this		
	Value	Name	Description Pr	oject		
	00b	YUYV	YUYV (8:8:8:8 MSB-V:Y ₂ :U:Y ₁) AI			
	01b	UYVY	UYVY (8:8:8:8 MSB-Y ₂ :V:Y ₁ :U) AI			
	10b	YVYU	YVYU (8:8:8:8 MSB-U:Y ₂ :V:Y ₁) AI			
	11b	VYUY	VYUY (8:8:8:8 MSB-Y ₂ :U:Y ₁ :V) AI			
15	180°_Dis	play_Rota	tion			
	Project:		All			
	Default V	alue:	0b			
	the surfa	ce address	ne plane to be rotated 180°. In addition to setting this bit, software offset to the lower right corner of the unrotated image and calculater right corner.			
	Value	Name	Description Pr	oject		
			No rotation Al			
	0b	None				
	0b 1b	None 180	180° rotation Al			
14	1b	180				
14	1b Trickle-F		le			
14	1b Trickle-F Project:	180	le DevSNB			
14	1b Trickle-F Project: Default V	180 reed_Enab	le DevSNB 0b			
14	1b Trickle-F Project:	180	le DevSNB	Project		
14	1b Trickle-F Project: Default V Value	180 eed_Enab alue: Name	le DevSNB Ob Description Trickle Feed Enabled - Data requests are sent whenever there	Project		



13:11	Reserved	d Proj	ect: All	Format:			
10	Tiled_Su	rface					
	Project:		All				
	Default V	alue:	Ob				
			t the surface data is in tiled mem ter. Only X tiling is supported for	ory. The tile pitch is specified in bytes in the display surfaces.			
	When this bit is set, it affects the hardware interpretation of the DVSBSTART and DVSBSURFADDR registers.						
	Value	Name	Description	Project			
	0b	Linear	Linear memory	All			
	1b	Tiled	Tiled memory	All			
		<u>.</u>					
9:3	Reserved	d Proje	ect: All	Format: MBZ			
	Oranita D	estination_	Кеу				
2	Sprite_D		All				
2	Project:						
2	• -	alue:	Ob				
2	Project: Default V This bit e key value	enables the e in DVSBK	0b destination key function. If the pi EYVAL the sprite pixel is used, o	ixel for the primary plane on this pipe matches the therwise the primary plane pixel is passed not be enabled if source key is enabled.			
2	Project: Default V This bit e key value	enables the e in DVSBK	0b destination key function. If the pi EYVAL the sprite pixel is used, o	therwise the primary plane pixel is passed			
2	Project: Default V This bit e key value through t	enables the e in DVSBK he blender	0b destination key function. If the pi EYVAL the sprite pixel is used, o unmodified. Destination Key can	not be enabled if source key is enabled.			

See DVSACNTR - Sprite Source Pixel Format Mapping of Bits to Colors



4.1.11.2 DVSBLINOFF—Video Sprite B Linear Offset Register

Register Type:		MMIO	
Address Offset:		73184h	
Project:		All	
Default Va	alue:	0000000h	
Access:		R/W	
Size (in bi	ts):	32	
Double B	uffer Update Point:	Start of vertical blank or pipe disabled	
Bit		Description	
31:0	Sprite_Linear_Offs	set Project: All Format:	
	•		



4.1.11.3 DVSBSTRIDE—Video Sprite B Stride Register

DVSBSTRIDE—Video Sprite B Stride Register						
Register Type:	MMIO					
Address Offset:	offset: 73188h					
Project:	All					
Default Value:	0000000h					
Access:	R/W					
Size (in bits):	32					
Double Buffer Update Poin	t: Start of vertic	cal blank or	pipe disabled or sprite disabled, after armed			
Double Buffer Armed By:	Write to DVS	BSURF				
Bit			Description			
31:15 Reserved	Project: All		Format:			
14:6 Sprite_Stride	Project:	All	Format:			
When using tile command pack to a maximum of	d memory, this mus et passed through t	st be 512 by the commai sprite scalir	n using linear memory, this must be 64 byte aligned. yte aligned. This register is updated through either a nd stream or writes to this register. The stride is limited ng is not enabled, 4K bytes when sprite scaling is			
5:0 Reserved	Project: All		Format:			



4.1.11.4 DVSBPOS—Video Sprite B Position Register

	DVS	BPOS—Vic	deo S	prite B Positi	on Register			
Register Ty	/pe:	MMIO						
Address O	ffset:	7318Ch						
Project:		All						
Default Val	ue:	00000000h						
Access:		R/W						
Size (in bits	s):	32						
	ffer Update Point:			or pipe disabled or	sprite disabled, after	armed		
	ffer Armed By:	Write to DVSE						
	er specifies the posi ay active area. ie. 2				care that the sprite	does not extend out		
Bit				Description				
31:28	Reserved Proj	ect: All			Format:	MBZ		
27:16	Sprite_Y-Position	Project:	All	Format:				
	These 12 bits specify the vertical position in lines of the sprite (upper left corner) relative to the beginning of the active video area. When performing 180° rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.							
15:12	Reserved Proj	ect: All			Format:	MBZ		
11:0	Sprite_X-Position	Project:	All	Format:				
	These 12 bits specify the horizontal position in pixels of the sprite (upper left corner) relative the beginning of the active video area. When performing 180° rotation, this field specifies the horizontal position of the original lower right corner relative to the original end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.							



4.1.11.5 DVSBSIZE—Video Sprite B Size Register

	מ	/SBSIZE	—Vid	leo Sprite B Si	ze Register	
Double But	ype: ffset: ue: s): ffer Update Point: ffer Armed By:	MMIO 73190h All 000000000 R/W 32 Start of ve Write to D	n rtical bla /SBSU	RF	or sprite disabled, after a	
	er specifies the size active area. ie. Xp				are that the sprite does	not extend out of
Bit				Description		
31:28	Reserved Proj	ect: All			Format:	MBZ
27:16		ne defined s	prite red		n lines. The value in the r be completely contained	
15:12	Reserved Proj	ect: All	-		Format:	MBZ
11:0	same as the stride the width minus one displayable area of The sprite width (act	out should be . The define he screen ir ual width, no	e less th d sprite nage. ot the w	nan or equal to the so rectangle must alwa	pixels. This does not ha tride in pixels. The value ays be completely contair e) is limited to even value xel doubling or Pixel doul	in the register is led within the s when YUV



4.1.11.6 DVSBKEYVAL—Video Sprite B Color Key Value Register

	DVSBKEY	VAL—Video Sprite B (olor Key Val	ue Reg	ister	r	
Register Ty	/pe:	MMIO					
Address O	ffset:	73194h					
Project:		All					
Default Val	ue:	0000000h					
Access:		R/W					
Size (in bit	s):	32					
Double But	ffer Update Point:	Start of vertical blank or pipe d	isabled				
matches th	e key. This register value is the minimur	color to be used with the mas will only have an effect when n value for the range compar	the sprite color	key is en	ablec	l. In source key	
Bit		Desc	iption				
31:24	Reserved Proj	ect: All		Forma	t:	MBZ	
23:16	V_Source_Key_Mir	n_Value/R_Source/Dest_Key_\	/alue	Project:	All	Format:	
	Specifies the color k or destination key co	ey (minimum) value for the sprite	e V channel source	e key or the	e Red	channel source	
15:8	Y_Source_Key_Mir	n_Value/G_Source/Dest_Key_V	/alue	Project:	All	Format:	
	Specifies the color key (minimum) value for the sprite Y channel source key or the Green channel source or destination key compare value.						
7:0	U_Source_Key_Mii	n_Value/B_Source/Dest_Key_V	/alue	Project:	All	Format:	
		ey (minimum) value for the sprite a key compare value.	e U channel source	e key or the	e Blue	e channel	



4.1.11.7 DVSBKEYMSK—Video Sprite B Color Key Mask Register

DVSBKEYMSK—Video Sprite B Color Key Mask Register						
Register Type:	ММІО					
Address Offset:	73198h					
Project:	All					
Default Value:	0000000h					
Access:	R/W					
Size (in bits):	32					
Double Buffer Update Point:	Start of vertical blank or pipe disabled					

For source key this register specifies which channels to perform range checking on. For destination key this register specifies the key mask to be used with the color value bits to determine if the display source data matches the key when enabled. A zero bit in the mask indicates that the corresponding bit match failure should be ignored when determining if the pixel matches.

Note that source key and destination key are mutually exclusive modes of operation, they can not be used simultaneously. For the function that is not enabled, the associated bits in this register should be programmed to zeroes.

Bit	Description			
31:27	Reserved Project: All	Forma	at:	MBZ
26	V/R_Channel_Source_Key_Enable	Project:	All	Format:
	Specifies the source color key enable for the V/Red channel			
25	Y/G_Channel_Source_Key_Enable	Project:	All	Format:
	Specifies the source color key enable for the Y/Green channel			
24	U/B_Channel_Source_Key_Enable	Project:	All	Format:
	Specifies the source color key enable for the U/Blue channel			
23:16	R_mask_Dest_Key_Value	Project:	All	Format:
	Specifies the destination color key mask for the sprite R channel			
15:8	G_mask_Dest_Key_Value	Project:	All	Format:
	Specifies the destination color key mask for the sprite G channel			
7:0	B_mask_Dest_Key_Value	Project:	All	Format:
	Specifies the destination color key mask for the sprite B channel			



	DVSBS	URF—Video S	prite B Surface Address Register		
Register T	ype:	MMIO			
Address O	ffset:	7319Ch			
Project:		All			
Default Va	lue:	00000000h			
Access:		R/W			
Size (in bit	s):	32			
Double Bu	ffer Update Point:	Start of vertical	plank or pipe disabled		
Writes to t	his register arm D	VSB registers			
Bit			Description		
31:12	Sprite_Surface_E	Base_Address			
	Project:	All			
	Address:	GraphicsAddre	ess[31:12]		
	This address specifies the surface base address. When the surface is tiled, panning is specified using (x, y) offsets in the DVSBTILEOFF register. When the surface is in linear memory, panning is specified using a linear offset in the DVSBLINOFF register.				
	is mapped to phys		epresents an offset from the graphics memory aperture base and he global GTT. The value in this register is updated through the flips.		
11:0	Reserved P	roject: All	Format:		

4.1.11.8 DVSBSURF—Video Sprite B Surface Address Register



4.1.11.9 DVSBKEYMAXVAL—Video Sprite B Color Key Max Value Register

Register T	уре:	MMIO			
Address C	Offset:	731A0h			
Project:		All			
Default Va	lue:	0000000h			
Access:		R/W			
Size (in bi	ts):	32			
Double Bu	Iffer Update Point:	Start of vertical blank or pipe disabled			
•		color to be used with the mask bits to er will only have an effect when the spi Description		•	
31:24	Reserved Pro	oject: All	Forma	at:	MBZ
00.40	V_Key_Max_Value	9	Project:	All	Format:
23:16	Specifies the color	key value for the sprite V channel	-		
23:16			Project:	All	Format:
15:8	Y_Key_Max_Value	9	110,000.		
	Y_Key_Max_Value	e key value for the sprite Y channel	1 10,000.		
	Y_Key_Max_Value	key value for the sprite Y channel	Project:	All	Format:



4.1.11.10 DVSBTILEOFF—Video Sprite B Tiled Offset Register

	DV	SBTILEO	FF—Video	Sprite B	Tiled Offse	et Regist	ter	
Register Ty	ype:	MMIC)					
Address O	ffset:	731A	4h					
Project:		All						
Default Val	ue:	0000	0000h					
Access:		R/W						
Size (in bit	s):	32						
Trusted Ty	pe:	1						
Double But	ffer Update Po	oint: Start	of vertical bla	nk or pipe dis	abled			
specified in address. V contents of	Vhen the surfa	JRFADDR re ace is in line are ignored.	egister, and t ar memory, t When the s	his register i he offset is s urface is tile	s used to des	cribe an of e DVSBLII	ffset f NOFF	e address is from that base Fregister and the ed in this register
Bit				Descrip	otion			
31:28	Reserved	Project:	All			Forma	at:	MBZ
27:16	Sprite_Start	Y-Position				Project:	All	Format:
	the display su	irface. When	performing 18	30° rotation, th		s the vertic	al pos	plane relative to ition of the lower
15:12	Reserved	Project:	All			Forma	at:	MBZ
11:0	Sprite_Start	X-Position				Project:	All	Format:
	to the display	surface. The ield specifies	offset must b the horizontal	e even pixel a position of th		formats. V	Vhen j	y plane relative performing 180° le start of the



4.1.11.11 DVSBSURFLIVE—Video Sprite B Live Surface Base Address Register

D	VSB	SURFLIVE—	Video Sprite B Live Surface Base Address Register			
Register Ty	/pe:	MMIO				
Address Of	ffset:	731ACh				
Project: All						
Default Val	ue:	00000000h				
Access:		Read Only				
Size (in bits	s):	32				
Bit			Description			
31:0	Sprite	e_Surface_Base	_Address			
	Proje	ot:	All			
	Addre	SS:	GraphicsAddress[31:0]			
	This gives the live value of the surface base address as being currently used for the plane.					

4.1.11.12 DVSBSCALE—Video Sprite B Scaler Control

DVSBSCALE—Video Sprite B Scaler Control										
Register Ty	/pe:	e: MMIO								
Address O	ffset:	73204h								
Project:		All								
Default Val	ue:	0000000h								
Access:		R/W								
Size (in bit	s):	32								
Double But	fer Update Point:	Start of vertical blank or pipe disabled or sprite disabled, after armed								
	fer Armed By:	Write to DVSBSURF								
source size Upscaling o greater that can not be when interla Horizontal o	the sprite. This register gives the source (input to sprite) size of the sprite. When scaling is enabled, the source size will be scaled up or down to the destination size. Upscaling of any amount is allowed. Downscaling up to 16X (source/destination) is allowed. Downscaling greater than 2X will involve decimation. Downscaling increases memory bandwidth requirements. Scaling can not be used with the sprite 64bpp source pixel format. Source and destination sizes must be 3x3 (3x6 when interlacing) or greater when scaling is enabled. Horizontal downscaling limits the maximum dot clock allowed as percent of cdclk. See DVSASCALE for the rules to calculate the allowed dot clock.									
Bit		Description								
31	Scaling_Enable	Project: All Format: Enable								
	Enables the scaling function. Source width can be no more than 4k bytes. For best picture quality, disable when scaling is not required. When in Self Refresh Big FIFO mode, scaling enable will be masked off while Big FIFO mode is exiting.									



30:29	Filter_Co	ontrol					
	Project:		All				
	Default V	alue:	Ob				
	Filter sele	ection					
	Value	Name	Description	Project			
	00b	Medium	Medium Filtering	All			
	01b	Enhancin	g Edge Enhancing Filtering	All			
	10b	Softening	Edge Softening Filtering	All			
	11b	Reserved	Reserved	All			
28	Even/Od	d_Field_Of	fset				
	Project:		All				
	Default V	alue:	Ob				
	Select the surface d		fset of the filtered data. Software is responsible for updating this to mate	h the			
	Value	Name	Description				
	0b	0	Vertical initial phase of 0	All			
	1b	0.5	Vertical initial phase of 0.5	All			
27	Even/Od	d_Field_Er	nable				
	Project:		All				
	Default V	alue:	Ob				
	Enable ad	djustment o	f the vertical offset of the filtered data.				
	Value	Name	Description				
	0b	Disable	Off (Vertical initial phase is 1/2 the scale factor)	All			
	1b	Enable	On (Vertical initial phase is selected by the Even/Off Field Offset bit)	All			
26:16	Source_	Width	Project: All Format:	-			
	is 3. The 4k bytes,	value progr	f the source image to be scaled in pixels. Max number of pixels is 2048 rammed is one less than the number of pixels. Source width can be no om a 64 byte alignment. The sprite width (actual width, not the width min ven values when YUV source pixel format is used.	more than			
15:11	Reserved	d Proje	ect: All Format: MBZ				
	Source_	Height	Project: All Format:				
10:0	The vertical size of the source image to be scaled in lines. If the source is a field, this is the number of lines in the field. Max number of lines is 2048; minimum is 3 (6 when interlacing). The value programmed is one less than the number of lines.						



4.1.11.13 DVSBGAMC—Video Sprite B Gamma Correction Registers

	DVS	SBGAMC—Vid	leo Sprite I	B Ga	mma Corr	ection Registers				
DVSBGAMC—Video Sprite B Gamma Correction Registers Register Type: MMIO Address Offset: 73300h										
Project: All										
Default Value: 0000000h; 04010040h; 08020080h; 0C0300C0h; 10040100h; 14050140h; 18060180h; 1C0701C0h; 20080200h; 24090240h; 280A0280h; 2C0B02C0h; 300C0300h; 340D0340h; 380E0380h; 3C0F03C0h; 00000400h; 00000400h; 00000400h;										
Access: R/W										
Size (in bits): 19x32										
DWord	Dword Bit Description									
0	31:0	GAMC0	Project:	All	Format:	DVSGAMC Reference Point				
1	31:0	GAMC1	Project:	All	Format:	DVSGAMC Reference Point				
2	31:0	GAMC2	Project:	All	Format:	DVSGAMC Reference Point				
3	31:0	GAMC3	Project:	All	Format:	DVSGAMC Reference Point				
4	31:0	GAMC4	Project:	All	Format:	DVSGAMC Reference Point				
5	31:0	GAMC5	Project:	All	Format:	DVSGAMC Reference Point				
6	31:0	GAMC6	Project:	All	Format:	DVSGAMC Reference Point				
7	31:0	GAMC7	Project:	All	Format:	DVSGAMC Reference Point				
8	31:0	GAMC8	Project:	All	Format:	DVSGAMC Reference Point				
9	31:0	GAMC9	Project:	All	Format:	DVSGAMC Reference Point				
10	31:0	GAMC10	Project:	All	Format:	DVSGAMC Reference Point				
11	31:0	GAMC11	Project:	All	Format:	DVSGAMC Reference Point				
12	31:0	GAMC12	Project:	All	Format:	DVSGAMC Reference Point				
13	31:0	GAMC13	Project:	All	Format:	DVSGAMC Reference Point				
14	31:0	GAMC14	Project:	All	Format:	DVSGAMC Reference Point				
15	31:0	GAMC15	Project:	All	Format:	DVSGAMC Reference Point				
16	31:0	GAMCmaxR	Project:	All	Format:	DVSGAMC Max Reference Point				
17	31:0	GAMCmaxG	Project:	All	Format:	DVSGAMC Max Reference Point				
18	31:0	GAMCmaxB	Project:	All	Format:	DVSGAMC Max Reference Point				

