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Volume 3 Part 4: PCH Display Registers [DevIBX]

For the all new 2010 Intel Core Processor Family Programmer's Reference Manual (PRM)

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1. PCH Display Registers [DevIBX]

1.1 Introduction and Register Summary

This chapter contains the register descriptions for the display portion of a family of integrated graphics devices. These registers do vary by devices within the family of devices so special attention needs to be paid to which devices use which registers and register fields.

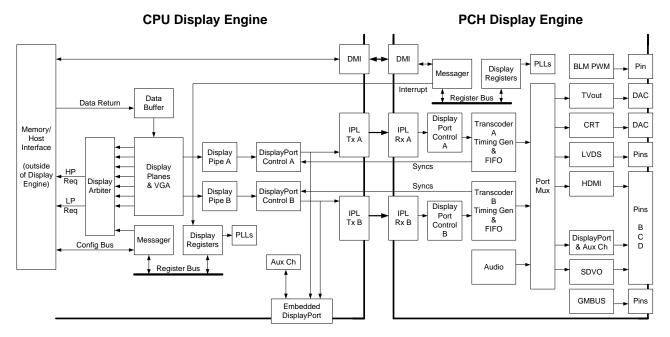
Different devices within the family may add, modify, or delete registers or register fields relative to another device in the same family based on the supported functions of that device. Additional information on the use and programming of these registers can be found in the display chapter.

The following table contains the sections break down where the register information is contained within this chapter:

| Address Range | Description |
|---------------|--------------------------------|
| C0000h-CFFFFh | Shared Functions |
| D0000h-DFFFFh | Messages |
| E0000h-EFFFFh | Transcoder and Port Controls |
| F0000h-FBFFFh | Transcoder and FDI Rx Controls |
| FC000h-FFFFFh | AFE Registers |



1.1.1 Display Diagram



The display engine plane and pipe functions are in the CPU and most of the port functions are in the PCH.

FDI transfers pixel data from the CPU Display Engine (Tx - transmit side) to the PCH Display Engine (Rx - receive side). Sync signals control the pixel flow over FDI.

A pipe in the CPU Display Engine connects to a transcoder in the PCH Display Engine through the FDI interface.

The CPU Display Engine is also called the "North Display".

The PCH Display Engine is also called the "South Display".



1.1.2 Terminology

| Description | Software Use | Should be implemented as |
|--|---|---|
| Read/Write | This bit can be read or written. | |
| Reserved: | Don't assume a value for these bits. Writes have no effect. | Writes are ignored. Reads return zero. |
| Reserved: write as zero, must be zero, or MBZ | Software must always write a zero to these bits. This allows new features to be added using these bits that will be disabled when using old software and as the default case. | Writes are ignored. Reads return zero. Maybe be connected as Read/Write in future projects. |
| Reserved: software must preserve contents | Software must write the original value back to this bit. This allows new features to be added using these bits. | Read only Read/Write. |
| Read Only | This bit is read only. The read value is determined by hardware. Writes to this bit have no effect. | According to each specific bit. The bit value is determined by hardware and not affected by register writes to the actual bit. |
| Read/Clear | This bit can be read and writes to it with a one cause the bit to clear. | Hardware events cause the bit to be set and the bit will be cleared on a write operation where the corresponding bit has a one for a value. |
| Double Buffered | Write when desired. Read gives the unbuffered value (written value) unless specified otherwise. Written values will update to take effect after a certain point. Some have a specific arming sequence where a write to another register is required before the update can take place. This is used to ensure atomic updates of several registers. | Two stages of registers used. First stage is written into and used for readback (unless specified otherwise). First stage value is transferred into second stage at the update point. Second stage value is used to control hardware. Arm/disarm flag needed for specific arming sequences. |

1.1.3 Display Mode Set Sequence

See the CPU Display Registers Bspec.



1.1.4 Simultaneous Display Capabilities on a Single Display Pipe/Transcoder

| | Embedded DP (on CPU) | Inte- grated LVDS | DP | Inte- grated TV | CRT |
|----------------------|----------------------------|-------------------------|-------------|-----------------------|-----------|
| Embedded DP (CPU) | | No (6) | No (6) | No (6) | No (6) |
| Integrated LVDS | | | No (2, 7) | No (1, 7) | No (3, 7) |
| DP | | | No(3, 5, 7) | No (1, 7) | No (4, 7) |
| Integrated TV | | | | | No (1, 7) |
| CRT | | | | | |

Shading: Rose = Does not work, Yellow = Some cases work, Green = works

) TV Timings don't match.

2) No internal LVDS, HDMI or TV. DP optionally has SSC.

4) Only works if DP/HDMI is in 24bpp mode.

6) Digital ports are multiplexed on the same pins, only works if ports are different.

7) Embedded DP is on the CPU; can not share the link.

8) Dithering, range correction, and gamma are done in the CPU; the display with lower bpp can truncate or the display with higher bpp can lose bits. One of the displays dictates range and gamma.

9) No DisplayPort allowed with other port on the same pipe/transcoder.

10) No HDMI allowed with another HDMI on the same transcoder.



2. South Shared Functions (C0000h– CFFFFh)

2.1 Interrupt Control Registers

2.1.1 South Display Engine Interrupt Registers Bit Definition

| | South Display Engine Interrupt Control R | egisters Bit | Defir | nition |
|---|--|--|-------------------|--|
| Project: | All | | | |
| South Disp together to Registers. | lay Engine (SDE) interrupt bits come from events within the so generate the South/PCH Display Interrupt Event which will app | outh display engine pear in the Display | e. The y Engir | SDEIIR is ORed ne Interrupt Control |
| The South | Display Engine Interrupt Control Registers all share the same I | bit definitions from | n this ta | able. |
| Bit | Description | | | |
| 31:25 | Reserved Project: All | For | mat: | |
| 24 | Gmbus(combined) | Project: | All | Format: |
| | No IMR | | | |
| 23 | Reserved | Project: | All | Format: |
| 22 | Reserved | Project: | All | Format: |
| 21 | Audio_Transcoder_B | Project: | All | Format: |
| | Pulse? | | | |
| 20 | Audio_Transcoder_A | Project: | All | Format: |
| | Pulse? | | | |
| 19 | Poison | Project: | All | Format: |
| | This is an active high pulse on receiving the poison message | Э. | | |
| 18 | Performance_counter | Project: | All | Format: |
| | This is an active high pulse when the performance counter return the Performance Counter Source register | eaches the thresh | old val | ue programmed in |
| 17 | FDI_RXB(combined) | Project: | All | Format: |
| | This is an active high level while any of the FDI_RXB_ISR bi | its are set | | |
| 16 | FDI_RXA(combined) | Project: | All | Format: |
| | This is an active high level while any of the FDI_RXA_ISR bi | its are set | | |
| 15 | AUX_Channel_D | Project: | All | Format: |
| | This is an active high pulse on the AUX D done event | | | |



| | South Display Engine Interrupt Control Reg | jisters Bit | Defir | nition |
|----|---|-----------------|----------|---------|
| 14 | AUX_Channel_C | Project: | All | Format: |
| | This is an active high pulse on the AUX C done event | | | |
| 13 | AUX_Channel_B | Project: | All | Format: |
| | This is an active high pulse on the AUX B done event | | | |
| 12 | Reserved Project: All | For | mat: | |
| 11 | CRT_Hotplug | Project: | All | Format: |
| | This is an active high level while either of the CRT Hot Plug Det | ection Status b | oits are | e set. |
| 10 | Reserved | Project: | All | Format: |
| 9 | Reserved | Project: | All | Format: |
| 8 | Reserved | Project: | All | Format: |
| 7 | Reserved Project: All | For | mat: | |
| 6 | Reserved | Project: | All | Format: |
| 5 | Transcoder_B_CRC_done | Project: | All | Format: |
| | This is an active high pulse on the Transcoder B CRC done. | | | |
| 4 | Transcoder_B_CRC_error | Project: | All | Format: |
| | This is an active high pulse on the Transcoder B CRC error. | | | |
| 3 | Transcoder_B_FIFO_underrun | Project: | All | Format: |
| | This is an active high level for the duration of the Transcoder B | FIFO underrun | n | |
| 2 | Transcoder_A_CRC_done | Project: | All | Format: |
| | This is an active high pulse on the Transcoder A CRC done. | | | |
| 1 | Transcoder_A_CRC_error | Project: | All | Format: |
| | This is an active high pulse on the Transcoder A CRC error. | | | |
| 0 | Transcoder_A_FIFO_underrun | Project: | All | Format: |
| | This is an active high level for the duration of the Transcoder A | FIFO underrun | n | |



2.1.1.1 SDEISR — South Display Engine Interrupt Status Register

| | SD | EISR — South Disp | lay Engine Interrupt Status R | egister | | | |
|--------------------|---------------|---|--|----------------------------|--|--|--|
| Register Ty | ype: MN | ЛЮ | | | | | |
| | | set: C4000h | | | | | |
| Project: | All | | | | | | |
| Default Val | lue: 000 | 00000h | | | | | |
| Access: | Re | ad Only | | | | | |
| Size (in bit | s): 32 | | | | | | |
| of these int | errupt co | nditions are reported in th | value of all interrupt status bits. The II te persistent IIR (i.e., set bits must be IIR bits to cause CPU interrupts. | | | | |
| Bit | | | Description | | | | |
| 31:0 | South_D | isplay_Engine_Interrupt_S | Status_Bits | | | | |
| | Project: | All | | | | | |
| | Format: | South Display Engine Ir | nterrupt Control Registers Bit Definition | See description above | | | |
| | This field | contains the non-persistent | values of all interrupt status bits. | | | | |
| | Value | Name | Description | Project | | | |
| | 0b | Condition Doesn't Exist | Interrupt Condition currently does not e | exist All | | | |
| 1 | 1b | Condition Exists | Interrupt Condition currently exists | All | | | |
| | Progra | mming Notes | | | | | |
| | | nputs to this register are sho ble these conditions. | rt pulses; therefore software should not ex | xpect to use this register | | | |



2.1.1.2 DEIMR — South Display Engine Interrupt Mask Register

| | S | DEIMR — So | outh Display Engine Interrupt Mask Register | |
|--------------------|---------------------|--------------------|--|---------|
| Register Ty | <mark>ype:</mark> M | MIO | | |
| Address O | ffset: C4 | 4004h | | |
| Project: | AI | I | | |
| Default Val | ue: Ff | FEDFFFh | | |
| Access: | R | /W | | |
| Size (in bit | <mark>s):</mark> 32 | 2 | | |
| | ntil clear | ed by software. | be reported in the IIR, possibly triggering a CPU interrupt, and w "Masked" bits will not be reported in the IIR and therefore cannot | |
| Bit | | | Description | |
| 31:0 | South_ | Display_Engine | _Interrupt_Mask_Bits | |
| | Project: | All | | |
| | Format: | South Displ | ay Engine Interrupt Control Registers Bit Definition See description a | bove |
| | This fiel | d contains a bit m | nask which selects which interrupt bits from the ISR are reported in the I | IR. |
| | Value | Name | Description | Project |
| | 0b | Not Masked | Will be reported in the IIR | All |
| | 1b | Masked | Will not be reported in the IIR | All |



2.1.1.3 SDEIIR — South Display Engine Interrupt Identity Register

| | SD | EIIR — South Displa | ay Engine Interrupt Identity Register | | | |
|-----------------------------|--------------------------|--------------------------------|---|--------------|--|--|
| Register Type: MMIO | | | | | | |
| . . | ffset: C4008h | | | | | |
| Project: | All | | | | | |
| Default Va | ue: 00 | 00000h | | | | |
| Access: | R/\ | N Clear | | | | |
| Size (in bit | s): 32 | | | | | |
| interrupts (interrogate | if enablec d to deter | I via the IER). When a CF | are "unmasked" by the IMR and thus can generat PU interrupt is generated, this should be the first re errupt. Writing a '1' into the appropriate bit pos | gister to be | | |
| Bit | | - | Description | | | |
| 31:0 | South_D |) isplay_Engine_Interrupt_I | dentity_Bits | | | |
| | Project: | All | | | | |
| | Format: | South Display Engine In | terrupt Control Registers Bit Definition See description | on above | | |
| | IMR. If e register v | nabled by the IER, bits set in | of the interrupt bits from the ISR which are "unmasked" n this register will generate a CPU interrupt. Bits set in t the interrupt condition is "cleared" via software by writing | his | | |
| | Value | Name | Description | Project | | |
| | 0b | Condition Not Detected | Interrupt Condition Not Detected | All | | |
| | 1b | Condition Detected | Interrupt Condition Detected (may or may not have actually generated a CPU interrupt) | All | | |



2.1.1.4 SDEIER — South Display Engine Interrupt Enable Register

| | SD | EIER — | South Display Engine Interrupt Enable Register | |
|--------------------|----------------|-------------|--|------------------|
| Register Ty | /pe: MI | NIO | | |
| Address O | ffset: C4 | 00Ch | | |
| Project: | All | | | |
| Default Val | ue: 00 | 000000h | | |
| Access: | R/ | W | | |
| Size (in bit | s): 32 | | | |
| | • | | terrupt enable bit for each interrupt bit in the IIR register. A di Identity Register to allow polling of interrupt sources. | sabled interrupt |
| Bit | | | Description | |
| 31:0 | South_[| Display_Eng | gine_Interrupt_Enable_Bits | |
| | Project: | All | | |
| | Format: | South I | Display Engine Interrupt Control Registers Bit Definition See descr | iption above |
| | | | ter enable a CPU interrupt to be generated whenever the correspond gister becomes set. | ing bit in the |
| | Value | Name | Description | Project |
| | 0b | Disable | Disable | All |
| | 1b | Enable | Enable | All |



2.1.1.5 Digital Port Hot Plug Control Register

| | | | Digital Port Hot Plug Control Register | | | | |
|---|---|-----------------------------|---|------------|--|--|--|
| Register T Address C Project: Default Va Access: Size (in bi | Offset: C4 All Ilue: 000 R/\ | /IO 030h 000000h N | | | | | |
| Bit | | | Description | | | | |
| 31:21 | Reserve | d Proj | ject: All Format: | | | | |
| 20 | Digital_F | ort_D_Ho | t_Plug_Detect_Input_Enable | | | | |
| | Project: | | All | | | | |
| | Default V | /alue: | 0b | | | | |
| | Controls the state of the HPD buffer for the digital port. The buffer state is independent of whether the port is enabled or not. | | | | | | |
| | Value | Name | Description | Project | | | |
| | 0b | Disable | Buffer disabled | All | | | |
| | 1b | Enable | Buffer enabled. Hot plugs bit reflect the electrical state of the HPD pin | All | | | |
| 19:18 | Digital_Port_D_Hot_Plug_Short_Pulse_Duration | | | | | | |
| | Project: | | All | | | | |
| | Default V | /alue: | 0b | | | | |
| | These bit | ts define the | e duration of the pulse defined as a short pulse. | | | | |
| | Malara | Name | Description | Project | | | |
| | Value | | | | | | |
| | 00b | 2ms | 2mS | All | | | |
| | | | 2mS 4.5mS | All All | | | |
| | 00b | 2ms | - | | | | |



| | | I | Digital Po | rt Hot Plug Control Register | |
|-------|--------------------------|------------------------------|------------------|---|----------|
| 17:16 | Digital_P | ort_D_Hot | _Plug_Interr | upt_Detect_Status | |
| | Project: | | All | | |
| | Default Va | alue: | 0b | | |
| | to clear th When eith | ne status. T ner a long c | This bit is used | o on the digital port. Graphics software must write a one to t d for either monitor hotplug/unplug or for notification of a sin is detected, one of these bits will set. These bits are ORed ster bit. | k event. |
| | Value | Name | | Description | Project |
| | 00b | No Detec | t | Digital port hot plug event not detected | All |
| | X1b | Short Det | ect | Digital port short pulse hot plug event detected | All |
| | 1Xb | Long Det | ect | Digital port long pulse hot plug event detected | All |
| 15:13 | Reserved | l Proje | ect: All | Format: | |
| 12 | Digital_P | ort_C_Hot | _Plug_Detec | t_Input_Enable | |
| | Project: | | All | | |
| | Default Va | alue: | 0b | | |
| | | he state of abled or no | | er for the digital port. The buffer state is independent of whe | ther the |
| | Value | Name | Description | 1 | Project |
| | 0b | Disable | Buffer disat | bled | All |
| | 1b | Enable | Buffer enab | led. Hot plugs bit reflect the electrical state of the HPD pin | All |
| 11:10 | Digital_P | ort_C_Hot | _Plug_Short | _Pulse_Duration | |
| | Project: | | All | | |
| | Default Va | alue: | 0b | | |
| | These bits | s define the | e duration of th | ne pulse defined as a short pulse. | |
| | Value | Name | Description | ı | Project |
| | 00b | 2ms | 2mS | | All |
| | 01b | 4.5ms | 4.5mS | | All |
| | 10b | 6ms | 6mS | | All |
| | 11b | 100ms | 100mS | | All |
| | | | | | |



| 9:8 | Digital F | ort C Hot Plu | Ig_Interrupt_Detect_Status | | | | | | |
|-----|---|---|---|----------------------------|--|--|--|--|--|
| | Project: | | All | | | | | | |
| | Default Value: 0b | | | | | | | | |
| | This reflects hot plug detect status on the digital port. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of a sink event. When either a long or short pulse is detected, one of these bits will set. These bits are ORed together to go to the main ISR hotplug register bit. | | | | | | | | |
| | Value | Name | Description | Project | | | | | |
| | 00b | No Detect | Digital port hot plug event not detected | All | | | | | |
| | X1b | Short Detect | Digital port short pulse hot plug event detected | All | | | | | |
| | 1Xb | Long Detect | Digital port long pulse hot plug event detected | All | | | | | |
| 7:5 | Reserve | d Project: | All Format: | | | | | | |
| 4 | - | ort_B_Hot_Plu | Ig_Detect_Input_Enable | | | | | | |
| | Project: | | All | | | | | | |
| | Default V | | 0b | | | | | | |
| | Controls the state of the HPD buffer for the digital port. The buffer state is independent of whether the port is enabled or not. | | | | | | | | |
| | Value | Name De | escription | Project | | | | | |
| | 0b | Disable Bu | iffer disabled | All | | | | | |
| | 1b | Enable Bu | ffer enabled. Hot plugs bit reflect the electrical state of the HPD pin | All | | | | | |
| 3:2 | Digital_Port_B_Hot_Plug_Short_Pulse_Duration | | | | | | | | |
| | | These bits define the duration of the pulse defined as a short pulse. | | | | | | | |
| | | 00 = 2mS (Default) | | | | | | | |
| | 01 = 4.5r | - | | | | | | | |
| | 10 = 6mS | | | | | | | | |
| | 11 = 100 | mS | | | | | | | |
| 1:0 | Digital_F | ort_B_Hot_Plu | ɪg_Interrupt_Detect_Status | | | | | | |
| | Project: | | All | | | | | | |
| | Default V | alue: | Ob | | | | | | |
| | This reflects hot plug detect status on the digital port. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of a sink event. When either a long or short pulse is detected, one of these bits will set. These bits are ORed together to go to the main ISR hotplug register bit. | | | | | | | | |
| | to clear the When eit | he status. This the her a long or sho | ort pulse is detected, one of these bits will set. These bits are ORed | together | | | | | |
| | to clear the When eit | he status. This the her a long or sho | ort pulse is detected, one of these bits will set. These bits are ORed | together Project | | | | | |
| | to clear th When eit to go to th | he status. This k her a long or sho he main ISR hot | ort pulse is detected, one of these bits will set. These bits are ORed plug register bit. | together | | | | | |
| | to clear th When eit to go to th Value | he status. This k her a long or sho he main ISR hot Name | ort pulse is detected, one of these bits will set. These bits are ORed plug register bit. Description | together Project | | | | | |



2.2 GMBUS and I/O Control Registers (C5000h–C5FFFh)

2.2.1 GPIO Pin Usage (By Functions)

GPIO pins allow the support of simple query and control functions such as DDC and I^2C interface protocols. GPIO pins exist in pairs (for the most part) and provide a mechanism to control external devices through a register programming interface. GPIO pins can be set to a level or the value of the pin can be read. This allows for a "bit banging" version of an I2C interface to be implemented. An additional function of using the GMBUS engine to run the I2C protocols is also allowed. Refer to the *CSpec* for GPIO signal descriptions. Refer to the *Philips I2C-BUS SPECIFICATION version 2.1* for a description of the I2C bus and protocol.

The number and names of the GPIO pins vary from device type to device type. Some of the GPIO pins will be muxed with other functions and are only available when the other function is not being used. The following subsections describe the GPIO pin to register mapping for the various devices. OEMs have the ability to remap these functions onto other pins as long as the hardware limitations are observed.

| Port | Pin Use (Name) | GMBUS Use | Internal Pullup | I ² C | Device | Description |
|------|--------------------------------|--------------|--------------------|------------------|--------|--|
| 7 | Reserved | No | No | | | |
| | Reserved | | | | | |
| 6 | Reserved | No | No | | | |
| | Reserved | | | | | |
| 5 | Reserved | | | | | |
| | Reserved | | | | | |
| 4 | Reserved | | | | | |
| | Reserved | | | | | |
| 3 | Reserved | | | | | |
| | Reserved | | | | | |
| 2 | LVDS DDC Data (DDCLDATA) | Yes | No | Yes | All | DDC for Digital Display connection via the integrated LVDS |
| | LVDS DDC Clock (DDCLCLK) | | | Yes | | |
| 1 | I2C Data (LCLKCTRLB) | Yes | No | Yes | All | For control of SSC clock generator devices on motherboard. Support can be optionally i2c or control level. |

2.2.2 GPIO Pin Usage (By Device)



| Port | Pin Use (Name) | GMBUS Use | Internal Pullup | I ² C | Device | Description |
|------|----------------------------|--------------|--------------------|------------------|--------|---|
| | I2C Clock (LCLKCTRLA) | | | Yes | | |
| 0 | DAC DDC Data (DDCADATA) | Yes | No | Yes | All | DDC for Analog monitor (VGA) connection. This cannot be shared with other DDC or I2C pairs due to legacy monitor issues. |
| | DAC DDC Clock | | | Yes | | |
| | (DDCACLK) | | | | | |



2.2.2.1 GPIO Control Registers

The number of registers and their usage may change with each product.

| - | | | | | Register I | | | | | |
|----------|--|--|--|---|---|---|---|--|--|--|
| Project: | All | | | | | | | | | |
| Bit | | Description | | | | | | | | |
| 31:13 | Reserved | Project: | All | | | | Format: | MBZ | | |
| 12 | GPIO_Dat | ta_In | Project: | All | Access: | Read Only | y | | | |
| | This is the | e value that is | sampled on | the GPIC | D_Data pin as | an input. | | | | |
| | | is synchronize bit is undefine | | ore Clock | domain. Beca | use the defa | ult setting is t | his buffer is an | | |
| 11 | GPIO_Dat | ta_Value | Project: | All | Access: | R/W | | | | |
| | Default Va | alue: | 1b | | | | | | | |
| | the registe actually w configure | er if GPIO DA ritten to this re the pin as an o | FA MASK is egister and to output. | s also ass the GPIO | erted. The val Data DIRECT | ue will appea ION VALUE | ar on the pin if contains a va | | | |
| | | Default = 1. The GPIO default clock data value is programmed to '1' in hardware. The hardware drives a default of '1' since the I2C interface defaults to a '1'. (this mimics the I2C external pull-ups on the bus) | | | | | | | | |
| 10 | GPIO_Dat | ta_Mask | | | | | | | | |
| | Project: | | All | | | | | | | |
| | Access: | | Write On | hy. | | | | | | |
| | ALLESS. | | | iy | | | | | | |
| | Default Va | alue: | 0b | ıy | | | | | | |
| | Default Va This is a n | | 0b ermine whe | ther the G | | ALUE bit shc | uld be writter | n into the register. | | |
| | Default Va This is a n | nask bit to dete | 0b ermine whe and when re | ther the G | is 0. | ALUE bit sho | | n into the register. roject | | |
| | Default Va This is a n This value | hask bit to dete is not stored a | 0b ermine whe and when re D | ther the G ead returr escriptio | is 0. | | | roject | | |
| | Default Va This is a n This value Value | hask bit to dete is not stored a Name | 0b ermine whe and when ro D D | ther the G ead returr escriptio o NOT wr | ns 0. n | Value bit | Р | roject | | |
| 9 | Default Va This is a n This value Value 0b 1b | nask bit to dete is not stored a Name No Write | 0b ermine whe and when ro D D | ther the G ead returr escriptio o NOT wr | ns 0. n ite GPIO Data | Value bit | P A | roject | | |
| 9 | Default Va This is a n This value Value 0b 1b | nask bit to dete is not stored a Name No Write Write | 0b ermine whe and when ro D D | ther the G ead returr escriptio o NOT wr | ns 0. n ite GPIO Data | Value bit | P A | roject | | |
| 9 | Default Va This is a n This value Value 0b 1b GPIO_Dat | nask bit to dete is not stored a Name No Write Write | 0b ermine whe and when re D W Value | ther the G ead returr escriptio o NOT wr | ns 0. n ite GPIO Data | Value bit | P A | roject | | |
| 9 | Default Va This is a n This value Value 0b 1b GPIO_Dat Project: | nask bit to dete is not stored a Name No Write Write ta_Direction_ | 0b ermine whe and when ro D W Value All | ther the G ead returr escriptio o NOT wr | ns 0. n ite GPIO Data | Value bit | P A | roject | | |
| 9 | Default Va This is a n This value Ob 1b GPIO_Dat Project: Access: Default Va This is the only writte | nask bit to dete is not stored a No Write Write ta_Direction_ | 0b ermine whe and when ro D W W Value All R/W 0b Duld be use ster if GPIO | ther the G ead return escriptio o NOT wr /rite GPIC | ns 0. n ite GPIO Data Data Value b Data Value b Rection MA | Value bit it. nable of the (SK is also as | P A A SPIO Data pir serted. The v | roject II II n. This value is alue that will | | |
| 9 | Default Va This is a n This value Ob 1b GPIO_Dat Project: Access: Default Va This is the only writte | nask bit to dete is not stored a No Write Write ta_Direction_ alue: value that sho n into the regis | 0b ermine whe and when re D D W Value All R/W 0b Ster if GPIO ned by wha | ther the G ead return escriptio o NOT wr /rite GPIC | ns 0. n ite GPIO Data Data Value b Data Value b e the output e RECTION MA register for th | Value bit it. nable of the (SK is also as | P A A SPIO Data pir serted. The v A VALUE bit. | roject II II n. This value is alue that will | | |
| 9 | Default Va This is a n This value Ob 1b GPIO_Dat Project: Access: Default Va This is the only writte appear on | Name No Write Write ta_Direction_ value: value that sho n into the regis the pin is defi | 0b ermine whe and when re D W W Value All R/W 0b Valud be use ster if GPIO ned by wha | ther the G ead return escriptio o NOT wr /rite GPIC d to defini Data DIF tt is in the escriptio | ns 0. n ite GPIO Data Data Value b Data Value b e the output e RECTION MA register for th | Nalue bit it. nable of the (SK is also as e GPIO DAT | P A A SPIO Data pir serted. The v A VALUE bit. | roject II II n. This value is alue that will | | |



| | | GF | PIO Control Register Format | | | | |
|-----|--|--|--|-------------------------|--|--|--|
| 8 | GPIO_Data | a_Direction_Mas | k | | | | |
| | Project: | All | l | | | | |
| | Access: | W | rite Only | | | | |
| | Default Val | lue: 0b | | | | | |
| | | | ne whether the GPIO DIRECTION VALUE bit shoul red and when read always returns 0. | d be written into the | | | |
| | Value | Name | Description | Project | | | |
| | 0b | No Write | Do NOT write GPIO Data Direction Value bit | All | | | |
| | 1b | Write | Write GPIO Data Direction Value bit | All | | | |
| 7:5 | Reserved | Project: | All Form | at: MBZ | | | |
| 4 | GPIO_Clo | ck_Data_In Pro | oject: All Access: Read Only | | | | |
| | This is the value that is sampled on the GPIO Clock pin as an input. | | | | | | |
| | | s synchronized to bit is undefined at | the Core Clock domain. Because the default settin reset. | ng is this buffer is an | | | |
| 3 | GPIO_Clo | ck_Data_Value | Project: All Access: R/W | | | | |
| | Default Val | ue: | 1b | | | | |
| | This is the value that should be place on the GPIO Clk pin as an output. This value is only written into the register if GPIO Clock DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Clock DIRECTION VALUE contains a value that will configure the pin as an output. | | | | | | |
| | | | ult clock data value is programmed to '1' in hardwar ne I2C interface defaults to a '1'. (this mimics the I2C | | | | |
| 2 | GPIO_Clo | ck_Data_Mask | | | | | |
| | Project: | All | l | | | | |
| | Access: | W | rite Only | | | | |
| | Default Val | lue: 0b |) | | | | |
| | | | ne whether the GPIO Clock DATA VALUE bit shou red and when read always returns 0. | ld be written into the | | | |
| | 1 | Name | Description | Project | | | |
| | Value | Name | | , , | | | |
| | Value 0b | No Write | Do NOT write GPIO Clock Data Value bit | All | | | |



| 1 | GPIO_CI | ock _Direc | tion_Value | | | | |
|---|---------------------------|-------------|--|--------------|--|--|--|
| | Project: | | All | | | | |
| | Access: | | R/W | | | | |
| | Default V | alue: | Ob | | | | |
| | only writte | en into the | t should be used to define the output enable of the GPIO Clock pin. This register if GPIO Clock DIRECTION MASK is also asserted. The value the defined by what is in the register for the GPIO Clock DATA VALUE bit. | nat will | | | |
| | Value | Name | Description | Project | | | |
| | 0b | Input | Pin is configured as an input and the output driver is set to tri-state | All | | | |
| | 1b | Output | Pin is configured as an output | All | | | |
| 0 | GPIO_Clock_Direction_Mask | | | | | | |
| | Project: | | All | | | | |
| | Access: | | Write Only | | | | |
| | Default V | alue: | Ob | | | | |
| | | | determine whether the GPIO Clock DIRECTION VALUE bit should be v lue is not stored and when read returns 0. | vritten into | | | |
| | Value | Name | Description | Project | | | |
| | 0b | No Upda | te Do NOT update the GPIO Clock Direction Value bit on a write | All | | | |
| | 1b | Update | Update the GPIO Clock Direction Value bit. on a write operation | All | | | |



| Register Type: | MMIO |
|--------------------|--|
| Address Offset: | C5010h |
| Project: | All |
| Default Value: | 000U1000b |
| Access: | R/W |
| Size (in bits): | 8x32 |
| These registers of | define the control of sets of the "general purpose" I/O pins. Each register controls a pair of |
| • | used for general purpose control, but most are designated for specific functions according nts of the device and the system that the device is in. Each pin of the two pin pair is |

pins that can be used for general purpose control, but most are designated for specific functions according to the requirements of the device and the system that the device is in. Each pin of the two pin pair is designated as a clock or data for descriptive purposes. See the table at the beginning of this section to determine for each product which pins/registers are supported and their intended functions. **Board design variations are possible and would affect the usage of these pins.**

| DWord | Bit | | | | Description | |
|-------|------|-----------|----------|-----|-------------|------------------------------|
| 0 | 31:0 | GPIOCTL_0 | Project: | All | Format: | GPIO Control Register Format |
| 1 | 31:0 | GPIOCTL_1 | Project: | All | Format: | GPIO Control Register Format |
| 2 | 31:0 | GPIOCTL_2 | Project: | All | Format: | GPIO Control Register Format |
| 3 | 31:0 | GPIOCTL_3 | Project: | All | Format: | GPIO Control Register Format |
| 4 | 31:0 | GPIOCTL_4 | Project: | All | Format: | GPIO Control Register Format |
| 5 | 31:0 | GPIOCTL_5 | Project: | All | Format: | GPIO Control Register Format |
| 6 | 31:0 | GPIOCTL_6 | Project: | All | Format: | GPIO Control Register Format |
| 7 | 31:0 | GPIOCTL_7 | Project: | All | Format: | GPIO Control Register Format |



2.2.3 GMBUS Controller Programming Interface

The GMBUS (Graphic Management Bus) can be used to indirectly access/control devices connected to a GMBUS bus as an alternate to bit-wise programming via software.

The GMBUS interface is I²C compatible. The basic features are listed as follow:

- 1. Works as the master of a single master bus.
- 2. The bus clock frequency is selectable by software to be 50KHz, 100KHz, 400KHz , and 1MHz
- 3. The GMBUS controller can be attached to the selected GPIO pin pairs.
- 4. 7 or 10-Bit Slave Address and 8- or 16-bit index.
- 5. Hardware byte counter to track the data transmissions/reception
- 6. Timing source from core display clock.
- 7. There is a double buffered data register and a 9 bit counter to support 0 byte to 256 byte transfers.
- 8. The slave device can cause a stall by pulling down the clock line (Slave Stall), or delay the slave acknowledge response.
- 9. The master controller detects and reports time out conditions for a stall from a slave device or delayed or missing slave acknowledge.
- 10. Interrupt may optionally be generated.
- 11. There is no support for ring buffer based operation of GMBUS. The GMBUS is controlled by a set of memory mapped IO registers. Status is reported through the GMBUS status register.

The byte counter register is a read/write register, and in receiving mode, is used to track the data bytes received. There is a status register to indicate the error condition, data buffer busy, time out, and data complete acknowledgement.



2.2.3.1 GMBUS0—GMBUS Clock/Port Select

| | | GMBU | S0—GMBUS Clock/ | Port Select |
|---|--|--|---|---|
| Project: Default Val Access: Size (in bit The GMBU The clock r data valid b | ffset: C5100 All lue: 000000 R/W s): 32 ISO register w ate options a bit is set, beca | /ill set the clock re 50 KHz, 100 ause it will be re | KHz, 400 KHz, and 1MH | d the device the controller is connected to. Iz. This register should be set before the firs lata valid bit, and not read during the period |
| Bit | | | Descriptio | |
| 31:11 | Reserved | Project: A | | Format: |
| 10:8 | GMBUS_Rat Project: Default Value These two bir used. It shou | All e: 0b ts select the rate | that the GMBUS will run at. ed when between transfers | It also defines the AC timing parameters when the GMBUS is idle. |
| | Value | Name | Description | Project |
| | 000b | 100KHz | 100 KHz | All |
| | 001b | 50KHz | 50 KHz | All |
| | 010b | 400KHz | 400 KHz | All |
| | 011b | 1MHz | Reserved | All |
| | 1XXb | RESERVED | Reserved | All |
| 7 | Value Na Ob Or | All e: 0b ets the hold time of ame Descript ns Hold time | on the data line driven from otion ne of 0ns ne of 300ns | the GMBUS. Project All All |
| | | | | |
| 6:3 | Reserved | Project: A | | Format: |



| | | GM | BUS0—GMBUS Clock/Port Select | |
|-----|----------------------|------------------------------|--|-------------------|
| 2:0 | Pin_Pair | Select | | |
| | Project: | | All | |
| | Default V | alue: | 0b | |
| | determine | e which pin pairs | JS pin pair for use in the GMBUS communication. Use the table ab s are available for a particular device and the intended function of the ht forward mapping of port numbers to pair select numbers. | |
| | Value | Name | Description | Project |
| | 000b | None | None (disabled) | All |
| | | | | |
| | 001b | LCTRCLK | LCTRCLKA, LCTRLCLKB SSC Clock Device | All |
| | 001b 010b | LCTRCLK Analog Mon | LCTRCLKA, LCTRLCLKB SSC Clock Device Dedicated Analog Monitor DDC Pins (DDC1DATA, DDC1CLK) | All All |
| | | | , | |
| | 010b | Analog Mon | Dedicated Analog Monitor DDC Pins (DDC1DATA, DDC1CLK) | All |
| | 010b 011b | Analog Mon LVDS | Dedicated Analog Monitor DDC Pins (DDC1DATA, DDC1CLK) Integrated Digital Panel DDC Pins, LVDS | All All |
| | 010b 011b 100b | Analog Mon LVDS Port C | Dedicated Analog Monitor DDC Pins (DDC1DATA, DDC1CLK) Integrated Digital Panel DDC Pins, LVDS Reserved | All All All |

2.2.3.2 GMBUS1—GMBUS Command/Status

| | GMBUS1—GMBUS Command/Status |
|--------------------|---|
| Register Type: | MMIO |
| Address Offset: | C5104h |
| Project: | All |
| Default Value: | 0000000h |
| Access: | R/W Protect |
| Size (in bits): | 32 |
| This register lets | the software indicate to the GMBUS controller the slave device address, register index, and |
| indicate when the | e data write is complete. |
| When the SW_C | LR_INT bit is asserted, all writes to the GMBUS2, GMBUS3, and GMBUS4 registers are |
| diagordad Tha (| MPLIS1 register writes to any other bit execut the SW/ CLP. INT are also lost. Boada to |

discarded. The GMBUS1 register writes to any other bit except the SW_CLR_INT are also lost. Reads to these registers always work normally regardless of the state of the SW_CLR_INT bit.



| Bit | | | Description | | | |
|-----|---|------------------|---|---------|--|--|
| 31 | Software | e_Clear_Interr | upt(SW_CLR_INT) | | | |
| | Project: | | All | | | |
| | Access: | | R/W | | | |
| | Default V | alue: | Ob | | | |
| | GMBUS | | or normal operation. Setting the bit then clearing it acts as local reset to s bit is commonly used by software to clear a BUS_ERROR when a sla | | | |
| | Value | Name | Description | Project | | |
| | 0b | Clear HW_RDY | If this bit is written as a zero when its current state is a one, will clear the HW_RDY bit and allows register writes to be accepted to the GMBUS registers (Write Protect Off). This bit is cleared to zero when an event causes the HW_RDY bit transition to occur. | All | | |
| | 1b | Assert HW_RDY | Asserted by software after servicing the GMBUS interrupt. Setting this bit causes the INT status bit to be cleared. Setting (1) this bit also asserts the HW_RDY bit (until this bit is written with a 0). When this bit is set, no writes to GMBUS registers will cause the contents to change with the exception of this bit which can be written. | All | | |
| 30 | Software | e_Ready(SW_ | RDY) | | | |
| | Project: | | All | | | |
| | Default V | 'alue: | Ob | | | |
| | Data han | dshake bit use | ed in conjunction with HW_RDY bit. | | | |
| | Value | Name | Description | Proje | | |
| | 0b | De-Assert | De-asserted via the assertion event for HW_RDY bit | All | | |
| | 1b | SW Assert | When asserted by software, results in de-assertion of HW_RDY bit | All | | |
| 29 | Enable | Timeout(ENT) | · · · · · · · · · · · · · · · · · · · | | | |
| | Project: | | All | | | |
| | Default V | alue: | Ob | | | |
| | Enables timeout for slave response. When this bit is enabled and the slave device response has exceeded the timeout period, the GMBUS Slave Stall Timeout Error interrupt bit is set. | | | | | |
| | Value | Name | Description | Proje | | |
| | 0b | Disable | Disable timeout counter | All | | |
| | 1b | Enable | Enable timeout counter | All | | |



| | | GMB | US1—GMBUS Command/Status | | | | | | | |
|-------|---|----------------------------|---|---------------------|--|--|--|--|--|--|
| 27:25 | Bus_Cyc | cle_Select | | | | | | | | |
| | Project: | All | | | | | | | | |
| | Default V | alue: 0b | | | | | | | | |
| | GMBUS cycle will always consist of a START followed by Slave Address, followed by an optional read or write data phase. A read cycle with an index will consist of a START followed by a Slave Address a WRITE indication and the INDEX and then a RESTART with a Slave Address and an optional read data phase. The GMBUS cycle will terminate either with a STOP or by entering a wait state. The WAIT state is exited by generating a STOP or by starting another GMBUS cycle. | | | | | | | | | |
| | | | OP to be generated if a GMBUS cycle is generated, the GMBUS , or it is in a WAIT phase: | is | | | | | | |
| | Note that | t the three bits can | be decoded as follows: | | | | | | | |
| | 27 = ST0 | OP generated | | | | | | | | |
| | 26 = IND | EX used | | | | | | | | |
| | 25 = Cyc | le ends in a WAIT | | | | | | | | |
| | Value | Name | Description | Project | | | | | | |
| | 000b | No cycle | No GMBUS cycle is generated | All | | | | | | |
| | 001b | No Index, No Stop, Wait | GMBUS cycle is generated without an INDEX, with no STOP, and ends with a WAIT | All | | | | | | |
| | 010b | Reserved | Reserved | All | | | | | | |
| | 011b | Index, No Stop, Wait | GMBUS cycle is generated with an INDEX, with no STOP, and ends with a WAIT | All | | | | | | |
| | 100b | Gen Stop | Generates a STOP if currently in a WAIT or after the completion of the current byte if active | All | | | | | | |
| | 101b | No Index, Stop | GMBUS cycle is generated without an INDEX and with a STOP | All | | | | | | |
| | 110b | Reserved | Reserved | All | | | | | | |
| | 111b | Index, Stop | GMBUS cycle is generated with an INDEX and with a STOP | All | | | | | | |
| 24:16 | Total_By | /te_Count | Project: All Format: | | | | | | | |
| | cycle. Th | ne DATA phase ca | total number of bytes to be transferred during the DATA phase of a n be prematurely terminated by generating a STOP while in the DAT ct). Do not change the value of this field during GMBUS cycles trans | ΓA | | | | | | |
| 15:8 | | - | ister_Index(INDEX) Project: All Format: | | | | | | | |
| | used for | the WRITE portion | s of index to be used for the generated bus write transaction or the i of the WRITE/READ pair. It only has an effect if the enable Index b ing a GMBUS transaction. | ndex vit is set. | | | | | | |



| | GMBUS1—GMBUS Command/Status | | | | | | | | | | |
|-----|---|--|----------------------|---------|--|--|--|--|--|--|--|
| 7:0 | GMBUS_Slave_Address_And_Direction Project: All | | | | | | | | | | |
| | | Bits 7:1 = 7-bit GMBUS Slave Address (SADDR): When a GMBUS cycle is to be generated using the Bus Cycle Select field, this field specifies the value of the slave address that is to be sent out. | | | | | | | | | |
| | For use with 10-bit slave address devices, set this value to 11110XXb (where the last two bits (xx) are the two MSBs of the 10-bit address) and the slave direction bit to a write. This is followed by the first data byte being the 8 LSBs of the 10-bit slave address. | | | | | | | | | | |
| | Bit 0 = Slave Direction Bit: When a GMBUS cycle is to be generated based on the Bus Cycle Select, this bit determines if the operation will be a read or a write. A read operation with the index enabled will perform a write with just the index followed by a re-start and a read. A 1 indicates that a Read from the slave device operation is to be performed. A 0 indicates that a Write to the slave device operation is to be performed. | | | | | | | | | | |
| | Value | Name | Description | Project | | | | | | | |
| | 0000001b | General | General Call Address | All | | | | | | | |
| | 0000000b | Start | Start Bye | All | | | | | | | |
| | 0000001Xb | CBUS | CBUS Address | All | | | | | | | |
| | 11110XXXb | 10-bit | 10-Bit addressing | All | | | | | | | |
| | Others | Reserved | Reserved | All | | | | | | | |

2.2.3.3 GMBUS2—GMBUS Status Register

| | | GM | BUS2— | GMBUS Status Register |
|--------------------------|-----------|----------|-------|-----------------------|
| Register Type | : MMIO | | | |
| Address Offs | et: C5108 | h | | |
| Project: | All | | | |
| Default Value: 00000800h | | 800h | | |
| Access: R/W Protect | | rotect | | |
| Size (in bits): | 32 | | | |
| Bit | | | | Description |
| 31:16 F | eserved | Project: | All | Format: |



| 15 | INUSE | | | | | | | | |
|----|------------------------------------|---|------------------------------------|---|----------------------|--|--|--|--|
| | Project: | | All | | | | | | |
| | Default V | alue: | 0b | | | | | | |
| | own usag semapho of this res | e of the GM re among v source that | IBUS con arious ind may need | or the GMBUS resource can poll this bit until it reads a zero and troller. This bit has no effect on the hardware, and is only used ependent software threads that don't know how to synchronize to use the GMBUS logic. Writing a one to this bit is software's e of this resource is now terminated and it is available for other | as their use s | | | | |
| | Value | Value Name | | scription | Project | | | | |
| | Ob | GMBUS i Acquired | that read | ad operation that contains a zero in this bit position indicates t the GMBUS engine is now acquired and the subsequent ds of this register will now have this bit set. Writing a 0 to this has no effect. | All | | | | |
| | 1b | GMBUS i Use | GM Ono relir | ad operation that contains a one for this bit indicates that the IBUS is currently allocated to someone else and "In use". ce set, a write of a 1 to this bit indicates that the software has inquished the GMBUS resource and will reset the value of this to a 0. | All | | | | |
| 14 | Hardwar | e_Wait_Pha | ase(HW_\ | WAIT_PHASE) | | | | | |
| | Project: | | All | | | | | | |
| | Access: | | Read C | Dnly | | | | | |
| | Default V | alue: | 0b | | | | | | |
| | | | | software can now choose to generate a STOP cycle or a repea another GMBUS transaction on the GMBUS. | ted start | | | | |
| | Value | Name | Descrip | tion | Project | | | | |
| | 0b | No Wait | The GM | BUS engine is not in a wait phase. | All | | | | |
| | 1b | Wait | the end | on GMBUS engine is in wait phase. Wait phase is entered at of the current transaction when that transaction is selected orminate with a STOP. | All | | | | |
| 13 | Slave_St | all_Timeou | It_Error | | | | | | |
| | Project: | | All | | | | | | |
| | Access: | | Read C | Dnly | | | | | |
| | Defaulty | alue: | 0b | | | | | | |
| | Default V | This bit indicates that a slave stall timeout has occurred. It is tied to the Enable Timeout (ENT) bit. | | | | | | | |
| | | dicates that | t a slave s | | / | | | | |
| | | idicates that Name | t a slave s | Description | , | | | | |
| | This bit in | | | · · | Project All | | | | |



| | GMRIIS | _Interrupt_Sta | MBUS2—GMBUS Status Register | | |
|----|-----------------|-----------------|--|----------|--|
| 12 | Project: | - | All | | |
| | Access: | | Read Only | | |
| | Default V | | Ob | | |
| | This bit ir | ndicates that a | n event that causes a GMBUS interrupt has occurred. | | |
| | Value | Name | Description | Project | |
| | 0b No Interrupt | | The conditions that could cause a GMBUS interrupt have not occurred or this bit has been cleared by software assertion of the SW_CLR_INT bit. | All | |
| | 1b | Interrupt | GMBUS interrupt event occurred. This interrupt must have been one of the types enabled in the GMBUS4 register | All | |
| 11 | Hardwar | e_Ready(HW | _RDY) | | |
| | Project: | | All | | |
| | Access: | | Read Only | | |
| | Default V | /alue: | 1b See Description Below | | |
| | SW_RDY | / bit. | s bit is asserted by the GMBUS controller, it results in the de-assertior mal operation when the SW_CLR_INT bit is written to a 0. | i of the | |
| | Value | Name | Description | Project | |
| | 01- | | Condition required for assertion has not occurred or when this bit | A 11 | |
| | Ob | | is a one and: | All | |
| | dU | | is a one and: SW_RDY bit has been asserted | All | |
| | 00 | | | All | |
| | UB | | SW_RDY bit has been asserted During a GMBUS read transaction, after the each read of the | All | |
| | UB | | SW_RDY bit has been asserted During a GMBUS read transaction, after the each read of the data register During a GMBUS write transaction, after each write of the | All | |
| | 05 1b | | SW_RDY bit has been asserted During a GMBUS read transaction, after the each read of the data register During a GMBUS write transaction, after each write of the data register | All | |
| | | | SW_RDY bit has been asserted During a GMBUS read transaction, after the each read of the data register During a GMBUS write transaction, after each write of the data register SW_CLR_INT bit has been cleared | | |
| | | | SW_RDY bit has been asserted During a GMBUS read transaction, after the each read of the data register During a GMBUS write transaction, after each write of the data register SW_CLR_INT bit has been cleared This bit is asserted under the following conditions: After a reset or when the transaction is aborted by the setting | | |
| | | | SW_RDY bit has been asserted During a GMBUS read transaction, after the each read of the data register During a GMBUS write transaction, after each write of the data register SW_CLR_INT bit has been cleared This bit is asserted under the following conditions: After a reset or when the transaction is aborted by the setting of the SW_CLR_INT bit | | |



| | | | GM | BUS2—GMBUS Status Register | | | | |
|-----|-----------------------|---------------------------|---------------------|--|----------------------|--|--|--|
| 10 | NAK_Inc | licator | | | | | | |
| | Project: | | All | All | | | | |
| | Access: | ess: F | | Read Only | | | | |
| | Default V | 'alue: | 0b | | | | | |
| | Value | Name | | Description | Project | | | |
| | 0b | No bus | error | No bus error has been detected or SW_CLR_INT has been written as a zero since the last bus error | All | | | |
| | 1b | No Ack | | Set by hardware if any expected device acknowledge is not received from the slave within the timeout | All | | | |
| 9 | GMBUS | _Active(G | A) | | | | | |
| | Project: | | All | | | | | |
| | Access: | | Re | ad Only | | | | |
| | Default V | alue: | 0b | | | | | |
| | This is a | status bit | that ind | icates whether the GMBUS controller is in an IDLE state or not. | | | | |
| | Value | Name | Descr | iption | Project | | | |
| | 0b | Idle | The G | MBUS controller is currently IDLE | All | | | |
| | 1b | Active | | ndicates that the bus is in START, ADDRESS, INDEX, DATA, , or STOP Phase. Set when GMBUS hardware is not IDLE. | All | | | |
| 8:0 | Current | Byte_Co | unt | | | | | |
| | Project: | | | All | | | | |
| | Access: | | | Read Only | | | | |
| | hardware completio | e. Set to z on of each | ero at t byte of | the number of bytes currently transmitted/received by the GMBUS he start of a GMBUS transaction data transfer and incremented at f the data phase. Note that because reads have internal storage, may be ahead of the data that has been accepted from the data r | fter the the byte | | | |



2.2.3.4 GMBUS3—GMBUS Data Buffer

| GMBUS3—GMBUS Data Buffer | | | | | | | | |
|---|---|--------|-------------|--|--|--|--|--|
| Register Type: | MMIO | MMIO | | | | | | |
| Address Offset: | C510Ch | C510Ch | | | | | | |
| Project: | All | | | | | | | |
| Default Value: | 00000000h | | | | | | | |
| Access: | R/W Protect | | | | | | | |
| Size (in bits): | 32 | | | | | | | |
| Double Buffer Update Point: | Start of next Vt | olank | | | | | | |
| Double Buffer Armed By: | HW_RDY | | | | | | | |
| or read, all the way through bit 3 count, this register should be wri greater than four bytes, this regist indicating that the register is now | This is data read/write register. This register is double buffered. Bit 0 is the first bit sent or read, bit 7 is the 8 th bit sent or read, all the way through bit 31 being the 32 nd bit sent or read. For GMBUS write operations with a non-zero byte count, this register should be written with the data before the GMBUS cycle is initiated. For byte counts that are greater than four bytes, this register will be written with subsequent data only after the HW_RDY status bit is set indicating that the register is now ready for additional data. For GMBUS read operations, software should wait until the HW_RDY bit indicates that the register contains the next set of valid read data before reading this register. | | | | | | | |
| Bit | | | Description | | | | | |
| 31:24 Data Byte 3 | Project: | All | Format: | | | | | |
| 23:16 Data Byte 2 | Project: | All | Format: | | | | | |
| 15:8 Data Byte 1 | Project: | All | Format: | | | | | |
| 7:0 Data Byte 0 | Project: | All | Format: | | | | | |



2.2.3.5 GMBUS4—GMBUS Interrupt Mask

| | | GMBUS4—GMB | US Interrupt Mask | |
|---|---|---|---|------------|
| Register ⁻ Address (Project: Default Va Access: Size (in b | Offset: C511 All alue: 00000 R/W | | | |
| Bit | | | Description | |
| 31:5 | Reserved | Project: All | Format: | |
| | | | vents may contribute to the setting of GMBUS inter. | nterrupt |
| | Value | Name | Description | Project |
| | 0XXXXb | GMBUS Slave stall TO Disable | Disable GMBUS Slave stall timeout interrupt | All |
| | 1XXXXb | GMBUS Slave stall TO Enable | Enable GMBUS Slave stall timeout interrupt | All |
| | X0XXXb | GMBUS NAK Disable | Disable GMBUS NAK interrupt | All |
| | X1XXXb | GMBUS NAK Enable | Enable GMBUS NAK interrupt | All |
| | | | | |
| | XX0XXb | GMBUS Idle Disable | Disable GMBUS Idle interrupt | All |
| | XX0XXb XX1XXb | GMBUS Idle Disable GMBUS Idle Enable | Disable GMBUS Idle interrupt Enable GMBUS Idle interrupt | All All |
| | | | • | |
| | XX1XXb | GMBUS Idle Enable | Enable GMBUS Idle interrupt Disable Hardware wait (GMBUS cycle | All |
| | XX1XXb XXX0Xb | GMBUS Idle Enable HW Wait Disable | Enable GMBUS Idle interrupt Disable Hardware wait (GMBUS cycle without a stop has completed) Interrupt Enable Hardware wait (GMBUS cycle | All |



2.2.3.6 GMBUS5—2 Byte Index Register

| | GMBUS5—2 Byte Index Register | | | | | | | | |
|--------------------|--|--------------|--------------|----------|---|--|--|--|--|
| Register Ty | gister Type: MMIO | | | | | | | | |
| Address Of | s Offset: C5120h | | | | | | | | |
| Project: | All | | | | | | | | |
| Default Val | ue: 000000 |)00h | | | | | | | |
| Access: | R/W | | | | | | | | |
| Size (in bits | s): 32 | | | | | | | | |
| This registe | er provides a | method for | the softw | are indi | dicate to the GMBUS controller the 2 byte device index. | | | | |
| Bit | | | | | Description | | | | |
| 31 | 2_Byte_Inde | ex_Enable | Project: | All | Format: | | | | |
| | When this bit is asserted (1), then bits 15:0 are used as the index. Bits 15:8 are used in the first byte which is the most significant index bits. The slave index in the GMBUS1<15:8> are ignored. Bits 7:0 are used in the second byte which is the least significant index bits. | | | | | | | | |
| 30:16 | Reserved | Project: | All | | Format: | | | | |
| 15:0 | 2_Byte_Slav | ve_Index | Project: | All | Format: | | | | |
| | This is the 2 | byte index u | sed in all G | SMBUS a | accesses when bit 31 is asserted (1). | | | | |



2.3 Display Clock Control Registers (C6000h–C6FFFH)

| Pixel Data Rate | Dot Clock | Dual Channel? | External Clock | Data Clock Rate | Multiplier |
|--------------------|-----------|---------------|----------------|--------------------|------------|
| 25-112MHz | 25-112MHz | NO | 25-112MHz | 175-784MHz | 1x |
| 80-224MHz | 80-224MHz | YES | 80-224MHz | 280-784MHz | 1x |

| Display Modes | Display Clock Frequency Range (MHz) |
|-----------------------|-------------------------------------|
| CRT DAC | 25-350 |
| LVDS (Single Channel) | 25-112 |
| LVDS (Dual Channel) | 80-224 |

The PLL frequency selection must be done such that the internal VCO frequency is within its limits. The PLL Frequency is based on the selected register and the following formula.

Reference Frequency: 120MHz for CRT and LVDS. 100MHz for the FDI.

$DotClk_Frequency = (ReferenceFrequency * (5* (M1+2)+(M2+2)) / (N+2)) / (P1* P2)$

| Item | Units | Range | Notes |
|-------------|-----------|-----------|----------------------------------|
| Dot Clock | Frequency | 20-350 | MHz (Combining ALL modes) |
| VCO | Frequency | 1760-3510 | MHz |
| N – Counter | Value | 3-8 | |
| M – Counter | Value | 79-127 | M=5*(M1+2)+(M2+2) |
| M1 and M2 | | M1 > M2 | |
| M1 | Value | 12-22 | |
| M2 | Value | 5-9 | |
| P-Div | Value | 5-80 | Reserved |
| P-Div | Value | 28-112 | Combined P1 and P2 for LVDS mode |
| P1-Div | Value | 1-8 | All modes |



2.3.1.1 DPLLA_CTRL—DPLL A Control Register

| | | DP | LLA_CTRL—DPLL A Control Registe | er | | | |
|-------------|---|--|---|---------|-----------------------|--|--|
| Register T | Гуре: | | MMIO | | | | |
| Address (| | | C6014h | | | | |
| Project: | | | All | | | | |
| Default Va | alue: | | 04800080h | | | | |
| Access: | | | R/W Protect | | | | |
| Size (in bi | • | | 32 | | | | |
| Double Bu | uffer Updat | e Point: | Transcoder A vertical blank, except as stated | | | | |
| | | | Description | | | | |
| 31 | DPLL_V | CO_Enable | | | | | |
| | Project: | | All | | | | |
| | Access: | | R/W | | | | |
| | Default V | alue: | Ob | | | | |
| | This bit w | This bit will enable or disable the PLL VCO. Disabling the PLL will cause the display clock to stop. | | | | | |
| | Value | Name | Description | | Project | | |
| | 0b | Disable | DPLL is disabled in its lowest power state | | All | | |
| | | | | | All | | |
| | 1b | Enable | DPLL is enabled and operational | | All | | |
| 30 | 1b Reserved | | DPLL is enabled and operational | | All | | |
| 30 29:28 | | d | · | Format: | MBZ | | |
| | Reserved | d | ct: All | Format: | | | |
| 29:28 | Reserved | d d Proje | ct: All | Format: | | | |
| 29:28 | Reserved Reserved DPLLA_I Project: | d Proje Mode_Selec | ct: All | | | | |
| 29:28 | Reserved Reserved DPLLA_I Project: Default V | d Proje Mode_Selec All alue: 01b | ct: All | | | | |
| 29:28 | Reserved Reserved DPLLA_I Project: Default V | d Proje Mode_Selec All alue: 01b | ct: All ct: DPLLA in DAC /Integrated TV mode | | | | |
| 29:28 | Reserved Reserved DPLLA_I Project: Default V Configure | d Proje Mode_Selec All alue: 01b e the DPLLA | ct: All ct: DPLLA in DAC /Integrated TV mode for various supported Display Modes | | MBZ | | |
| 29:28 | Reserved Reserved DPLLA_I Project: Default V Configure Value | d Proje Mode_Selec All alue: 01b e the DPLLA Name | ct: All DPLLA in DAC /Integrated TV mode for various supported Display Modes Description Reserved | | MBZ Project | | |
| 29:28 | Reserved Reserved DPLLA_I Project: Default V Configure Value 00b | d Proje Mode_Selec All alue: 01b the DPLLA Name Reserved | ct: All DPLLA in DAC /Integrated TV mode for various supported Display Modes Description Reserved | | MBZ Project All | | |



| 25:24 | FPA0/FPA1 _P2_Clock_Divide_LVDS_Mode | | | | | | |
|-------|--------------------------------------|--------------|---|------------|--|--|--|
| | Project: | | All | | | | |
| | Exists If: | | DPLLA_CTRL: DPLLA_Mode_Select = 10b | | | | |
| | Default Va | lue: | 00b | | | | |
| | Value | Name | Description | Project | | | |
| | 00b | Div 14 | Divide by 14. This is used in Single-Channel LVDS | All | | | |
| | 01b | Div 7 | Divide by 7. This is used in Dual-Channel LVDS | All | | | |
| | Others | Reserved | Reserved | All | | | |
| 25:24 | FPA0/FPA | 1 _P2_Clock | _Divide_NonLVDS_Mode | | | | |
| | Project: | | All | | | | |
| | Exists If: | | DPLLA_CTRL: DPLLA_Mode_Select != 10b | | | | |
| | Default Va | lue: | 00b | | | | |
| | Value | Name | Description | Project | | | |
| | 00b Div 10 | | Divide by 10. This is used when Dot Clock =< 270MHz DVI, DP, or DAC modes | All | | | |
| | Others | Reserved | Reserved | All | | | |
| 23:16 | FPA0_P1 | Post_Divisor | | | | | |
| | Project: | | All | | | | |
| | Default Va | | 80h Divide by eight | | | | |
| | | FPA1 when FF | e the write of m, n and p values into the PLL when the F PAO is in use (or vice versa) is also allowed. Writes to the formation of the second se | | | | |
| | Value | Name | Description | Project | | | |
| | 0000000 | 1b 1 | Divide by one | All | | | |
| | 0000001 | 0b 2 | Divide by two | All | | | |
| | 0000010 | 0b 3 | Divide by three | All | | | |
| | 0000100 | 0b 4 | Divide by four | All | | | |
| | 0001000 | 0b 5 | Divide by five | All | | | |
| | | | Divide by six | All | | | |
| | 0010000 | 0b 6 | | | | | |
| | | | | All | | | |
| | 0010000 | 0b 7 | Divide by seven Divide by eight (default) | All All | | | |



| 15:13 | PLL Refe | PLL_Reference_Input_Select(NOT_DOUBLE_BUFFERED) | | | | | | |
|-------|------------|---|---|-------------|--|--|--|--|
| | Project: | - • - | All | | | | | |
| | Default Va | lue: | 000b | | | | | |
| | | | d be selected based on the display device that is beir or CRT modes using the LCD panels for the integrate | | | | | |
| | Value | Name | Description | Project | | | | |
| | 000b | DREFCLK | DREFCLK (default is 120 MHz) for DAC/DVI/DP/T | / All | | | | |
| | 001b | Super SSC | 120MHz super-spread clock | All | | | | |
| | 010b | Reserved | Reserved | All | | | | |
| | 011b | SSC | Spread spectrum input clock (120MHz default) for I | _VDS/DP All | | | | |
| | 101b | Reserved | Reserved | All | | | | |
| | others | Not Allowed | Not allowed | All | | | | |
| 12 | Reserved | Project: | All For | mat: | | | | |
| 11:9 | Reserved | | | | | | | |
| 8 | Reserved | Project: | All For | mat: MBZ | | | | |
| 7:0 | FPA1_P1 | _Post_Divisor | | | | | | |
| | Project: | | All | | | | | |
| | Default Va | lue: | 80h Divide by eight | | | | | |
| | | FPA1 when FP | e the write of m, n and p values into the PLL when the PAO is in use (or vice versa) is also allowed. Writes to | | | | | |
| | Value | Name | Description | Project | | | | |
| | 0000000 | 1b 1 | Divide by one | All | | | | |
| | 0000001 | 0b 2 | Divide by two | All | | | | |
| | 0000010 | 0b 3 | Divide by three | All | | | | |
| | 0000100 | 0b 4 | Divide by four | All | | | | |
| | 0001000 | 0b 5 | Divide by five | All | | | | |
| | 0010000 | 0b 6 | Divide by six | All | | | | |
| | 0100000 | 0b 7 | Divide by seven | All | | | | |
| | 400000 | 0b 8 | Divide by eight (Default) | All | | | | |
| | 1000000 | 00 0 | Divide by eight (Deradit) | 7 40 | | | | |



2.3.1.2 DPLLB_CTRL—DPLL B Control Registers

| | | DPLL | .B_CTRL—DPLL B Control Register | S | |
|-----------------|--|-----------------|--|---------|---------|
| Register Ty | /pe: | М | MIO | | |
| Address Offset: | | | 6018h | | |
| Project: | | AI | I | | |
| Security: | | N | one | | |
| Default Val | ue: | 04 | 1800080h | | |
| Access: | | | W . | | |
| Size (in bit | - | 32 | | | |
| Double Bu | ffer Updat | te Point: Tr | anscoder B vertical blank, except as stated | | |
| Bit | | | Description | | |
| 31 | DPLLB_ | VCO_Enable | | | |
| | Project: | | All | | |
| | Default V | /alue: | Ob | | |
| | See DPL | LA description. | | | |
| | Value | Name Des | scription | | Project |
| | 0b Disable DPLL is disabled in it's lowest power state | | | | All |
| | 1b | Enable DPI | L is enabled and operational | | All |
| 30 | Reserve | d | | | |
| 29:28 | Reserve | d Project: | All | Format: | MBZ |
| 27:26 | DPLLB | Mode_Select | | | |
| | Project: | All | | | |
| | Default V | /alue: 01b | DPLLB in DAC/Integrated TV mode | | |
| | See DPL | LA description | | | |
| | Value | Name | Description | | Project |
| | 00b | Reserved | Reserved | | All |
| | 01b | Non-LVDS | DPLLB in DAC/DP/Integrated TV mode (default) | | All |
| | 10b | LVDS | DPLLB in LVDS mode | | All |
| | 11b | Reserved | Reserved | | All |



| 25:24 | FPB0/FPB1 | _P2_Clock | _Divide_LVDS_Mode | | |
|-------|----------------|--------------|--|---------|--|
| | Project: | | All | | |
| | Exists If: | | DPLLB_CTRL: DPLLB_Mode_Select = 10b | | |
| | Default Value | e: | 00b | | |
| | Value | Name | Description | Project | |
| | 00b | Div 14 | Divide by 14. This is used in Single-Channel LVDS | All | |
| | 01b | Div 7 | Divide by 7. This is used in Dual-Channel LVDS | All | |
| | Others | Reserved | Reserved | All | |
| 25:24 | FPB0/FPB1 | _P2_Clock | _Divide_NonLVDS_Mode | | |
| | Project: | | All | | |
| | Exists If: | | DPLLB_CTRL: DPLLB_Mode_Select != 01b | | |
| | Default Value: | | 00b | | |
| | Value | Name | Description | Project | |
| | 00b | Div 10 | Divide by 10. This is used when Dot Clock =< 270MHz in DAC modes | All | |
| | Others | Reserved | Reserved | All | |
| 23:16 | FPB0_P1_P | ost_Divisor | | | |
| | Project: | | All | | |
| | Default Value | | 80h Divide by eight | | |
| | See DPLLA | description. | | | |
| | Value | Name | Description | Project | |
| | 0000001b | 1 | Divide by one | All | |
| | 00000010b | 2 | Divide by two | All | |
| | 00000100b | 3 | Divide by three | All | |
| | 00001000b | 4 | Divide by four | All | |
| | 00010000b | 5 | Divide by five | All | |
| | 0010000b | 6 | Divide by six | All | |
| | 0100000b | 7 | Divide by seven | All | |
| | 1000000b | 8 | Divide by eight (Default) | All | |
| | Others | Illegal | Values are illegal and should not be used | All | |



| | | DPLLE | B_CTRL—DPLL B Control Register | rs |
|-------|--------------|---------------------|--|-------------|
| 15:13 | PLL_Refer | ence_Input_S | elect(NOT_DOUBLE_BUFFERED) All | |
| | Default Valu | ue: | 000b | |
| | See DPLLA | description. | | |
| | Value | Name | Description | Project |
| | 000b | DREFCLK | DREFCLK (default is 120 MHz) for DAC/DVI/ | /DP/TV All |
| | 001b | Super SSC | 120MHz super-spread clock | All |
| | 010b | Reserved | Reserved | All |
| | 011b | SSC | Spread spectrum input clock (120MHz defaul LVDS/DP | It) for All |
| | 101b | Reserved | Reserved | All |
| | others | Not Allowed | Not allowed | All |
| 12 | Reserved | Project: | All | Format: |
| 11:9 | Reserved | | | |
| 8 | Reserved | Project: | All | Format: MBZ |
| 7:0 | FPB1_P1_ | Post_Divisor | | |
| | Project: | | All | |
| | Default Valu | ue: description. | 80h Divide by eight | |
| | Value | Name | Description | Project |
| | 00000001 | b 1 | Divide by one | All |
| | 00000010 | b 2 | Divide by two | All |
| | 00000100 | b 3 | Divide by three | All |
| | 00001000 | b 4 | Divide by four | All |
| | 00010000 | b 5 | Divide by five | All |
| | 00100000 | b 6 | Divide by six | All |
| | 0100000 | b 7 | Divide by seven | All |
| | 1000000 | b 8 | Divide by eight (default) | All |
| | Others | Illegal | Values are illegal and should not be used | All |



2.3.1.3 FPA0—DPLL A Divisor Register 0

| | | FP | A0—I | DPLL A Divisor Register 0 | | | | |
|--------------|---------------|---------------|--------|--|----------------|--------------------|--|--|
| Register T | уре: | MMI | C | | | | | |
| Address O | ffset: | | | | | | | |
| Project: | | All | | | | | | |
| Default Va | lue: | 0003 | 0D07h | | | | | |
| Access: | | R/W | | | | | | |
| Size (in bit | :s): | 32 | | | | | | |
| Double Bu | ffer Update F | Point: Tran | scoder | A vertical blank | | | | |
| Bit | | | | Description | | | | |
| 31:28 | Reserved | Project: | All | | Format: | MBZ | | |
| 27 | Frequency | _doubler_cloc | k_enak | ble | | | | |
| | Project: | All | | | | | | |
| | Default Valu | ue: Ob | | | | | | |
| | | | | lency doubler clock. When the VCO cl er and its output clock is not available | lock to the do | ubler is disabled, | | |
| | Value | Name | | Description | F | Project | | |
| | 0h | Disable | | Disables clock of frequency doubler | A | di . | | |
| | 1h | Enable | | Enables clock of frequency doubler | Д | .II | | |
| 26:25 | Reserved | Project: | All | | Format: | MBZ | | |



| | | FPA | 0—DPLL | A Divisor Reg | gister 0 | | |
|-------|-----------------------------------|--------------------|-------------------|--|--------------|---------------|----------------|
| 24:22 | CB_Tuning | | | | | | |
| | Project: | All | | | | | |
| | Default Value | : 000b | | | | | |
| | | tter performanc | | lay PLL Analog co adroom of the Dis | | | |
| | | | - | If M/N Ratio is I | | | |
| | DAC | 2520.00 | | 21.00 | | 011 | |
| | LVDS 1ch | 2520.00 | | 21.00 | | 011 | |
| | LVDS 2ch | 2500.00 | | 25.00 | | 011 | |
| | Value N | ame | Description | | | Project | |
| | 000b O | Off | CB Tune Off | (Functional) | | All | |
| | 001b R | eserved | Reserved | | | All | |
| | 010b R | eserved | Reserved | | | All | |
| | 011b 10 | 00% | CB Tune 10 | 0% On (Functiona | I) | All | |
| 21:16 | FPA0_N-Divi | sor Proje | ct: All | Format: | | | |
| | N-Divisor valu less than the a | | r the desired o | output frequency. | The register | value is proo | grammed two |
| 15:14 | Reserved | Project: | All | | | Format: | MBZ |
| 13:8 | FPA0_M1-Div | visor Proje | ct: All | Format: | | | |
| | M-Divisor valu | | or the desired of | output frequency. | The register | value is pro | grammed to two |
| 7:6 | Reserved | Project: | All | | | Format: | MBZ |
| 5:0 | FPA0_M2-Div | visor Pr | oject: All | Format: | | | |
| | M-Divisor values than the a | | or the desired of | output frequency. | The register | value is prog | grammed two |



2.3.1.4 FPA1—DPLL A Divisor Register 1

| | | FF | PA1—DPLL A Diviso | r Register 1 | |
|--------------|--------------------|------------------------------------|------------------------------|---------------------------------|-----------------|
| Register T | | MM | • | | |
| Address O | ffset: | C60 | 44h | | |
| Project: | _ | All | | | |
| Default Val | lue: | | 30D07h | | |
| Access: | | R/W | | | |
| Size (in bit | s): ffer Update | 32 Boint: Tra | scoder A vertical blank | | |
| Bit | | | Descrip | otion | |
| 31:25 | Reserved | d Project: | All | Format: | MBZ |
| 24:22 | CB_Tuni | | | i offiat. | WIDZ |
| 27.22 | Project: | Al | | | |
| | Default V | | 0b | | |
| | | 0 CB_Tuning de | | | |
| | | Ū. | | | |
| | Value | Name | Description | Project | |
| | 000b | Off | CB Tune Off (Functiona | I) All | |
| | 001b | Reserved | Reserved | All | |
| | 010b | Reserved | Reserved | All | |
| | 011b | 100% | CB Tune 100% On (Fun | nctional) All | |
| 21:16 | FPA1_N- | Divisor Pr | oject: All Format: | | |
| | | value calculated the actual diviso | | ency. The register value is pro | grammed two |
| 15:14 | Reserved | d Project: | All | Format: | MBZ |
| 13:8 | FPA1_M1 | 1-Divisor Pr | oject: All Format: | | |
| | | value calculated the actual diviso | | ency. The register value is pro | ogrammed to two |
| 7:6 | Reserved | d Project: | All | Format: | MBZ |
| 5:0 | FPA1_M2 | 2-Divisor | Project: All Form | at: | |
| | M-Divisor | | for the desired output frequ | ency. The register value is pro | ogrammed two |



| Register 1 | vpe: | MM | 110 | | |
|--------------------------|-------------------------|------------------------------------|---|----------------|---------------------|
| Address (| | | D48h | | |
| Project: | | All | | | |
| Default Va | lue: | |)30D07h | | |
| Access: | (a). | R/V | V | | |
| Size (in bi Double Bi | ts): Iffer Update | 32 Point: Tra | nscoder B vertical blank | | |
| Bit | | | Description | | |
| 31:28 | Reserved | Project: | All | Format: | MBZ |
| 27 | Frequenc | y_doubler_clo | ock_enable | | |
| | Project: | A | | | |
| | Default Va | alue: Ol | b | | |
| | This bit er the circuit | nables/disables does not dissip | the frequency doubler clock. When the VCO clate power and its output clock is not available | lock to the do | oubler is disabled, |
| | Value | Name | Description | F | Project |
| | 0b | Disable | Disables clock of frequency doubler | Α | All |
| | 1b | Enable | Enables clock of frequency doubler | A | All |
| 26:25 | Reserved | Project: | All | Format: | MBZ |
| 24:22 | CB_Tuni | ng | | | |
| | Project: | A | II | | |
| | Default Va | alue: 00 | 00b | | |
| | See FPA |) CB_Tuning de | escription | | |
| | Value | Name | Description | Project | |
| | 000b | Off | CB Tune Off (Functional) | All | |
| | 001b | Reserved | Reserved | All | |
| | 010b | Reserved | Reserved | All | |
| | 011b | 100% | CB Tune 100% On (Functional) | All | |
| 21:16 | FPB0_N- | Divisor P | roject: All Format: | | |
| | See FPA | description. | | | |
| 15:14 | Reserved | Project: | All | Format: | MBZ |
| 13:8 | FPB0_M1 | I-Divisor P | roject: All Format: | | |
| | See FPA | description. | | | |
| 7:6 | Reserved | Project: | All | Format: | MBZ |
| 5:0 | FPB0 M2 | 2-Divisor | Project: All Format: | | |

2.3.1.5 FPB0—DPLL B Divisor Register 0



2.3.1.6 FPB1—DPLL B Divisor Register 1

| | | | FPB1—DPLL B Divisor Registe | er 1 | |
|--------------|-------------|--------------|------------------------------|---------|-----|
| Register T | vpe: | Ν | ИМЮ | | |
| Address O | | (| C604Ch | | |
| Project: | | A | All | | |
| Default Va | lue: | C | 00030D07h | | |
| Access: | | - | R/W | | |
| Size (in bit | | | 32 | | |
| Double Bu | ffer Update | e Point: | ranscoder B vertical blank | | |
| Bit | | | Description | | |
| 31:25 | Reserved | l Projec | t: All | Format: | MBZ |
| 24:22 | CB_Tuni | ng | | | |
| | Project: | | All | | |
| | Default Va | alue: | 000b | | |
| | See FPA |) CB_Tuning | description | | |
| | Value | Name | Description | Project | |
| | 000b | Off | CB Tune Off (Functional) | All | |
| | 001b | Reserved | Reserved | All | |
| | 010b | Reserved | Reserved | All | |
| | 011b | 100% | CB Tune 100% On (Functional) | All | |
| 21:16 | FPB1_N- | | Project: All Format: | | |
| | See FPA | description. | | | |
| 15:14 | Reserved | l Projec | t: All | Format: | MBZ |
| 13:8 | FPB1_M1 | | Project: All Format: | | |
| | See FPA | description. | | | |
| 7:6 | Reserved | l Projec | t: All | Format: | MBZ |
| 5:0 | FPB1_M2 | 2-Divisor | Project: All Format: | | |
| | See FPA | description. | | | |



2.3.1.7 DREF_CONTROL – Display Reference Clock Control Register

| Register T | | ЛЮ | | | | | |
|------------------------|---------------------------------|------------------|--|---------|--|--|--|
| Address C | | 200h | | | | | |
| Project: Default Va | All | 00000h | | | | | |
| Access: | R/N | | | | | | |
| Size (in bi | ts): 32 | | | | | | |
| Bit | | | Description | | | | |
| 31:15 | Reserve | d Project: | All Format: MBZ | | | | |
| 14:13 | 120MHz_CPU_source_output_enable | | | | | | |
| | Project: | | All | | | | |
| | Default V | alue: | 00b | | | | |
| | Value | Name | Description | Project | | | |
| | 00b | Disabled | Source output to CPU disabled | All | | | |
| | 01b | Reserved | Rerserved | All | | | |
| | 10b | Downspread | -0.5% SSC downspread source output to CPU enabled. Both the 120MHz SSC source and the SSC1 modulator must be enabled prior to enabling this output | All | | | |
| | 11b | Non-spread | Non-spread source output to CPU enabled. The 120MHz non- SSC source must be enabled prior to enabling this output | All | | | |
| 12:11 | 120MHz | _SSC_source_e | nable | | | | |
| | Project: | | All | | | | |
| | Default V | alue: | 00b | | | | |
| | This bit e | enables the 120M | /Hz SSC source used as a reference for CPU | | | | |
| | Value | Name | Description | Project | | | |
| | 00b | Disabled | Source disabled | All | | | |
| | 01b | Reserved | Reserved for CK505 buffered source enabled | All | | | |
| | 10b | Enabled | Integrated source enabled | All | | | |
| | 11b | Reserved | Reserved | All | | | |



| 10:9 | 120MHz_r | non-spread_ | sourc | e_enable | | |
|------|--|---------------|-------|--|---------|--|
| | Project: | | All | | | |
| | Default Value: 00b | | |) | | |
| | This field e | enables the 1 | 20MH | z non-SSC source for display | | |
| | Value | Name | Desc | ription | Project | |
| | 00b | Disabled | Sour | ce disabled | All | |
| | 01b | CK505 | CK50 | 05 buffered source enabled. This setting enables the 96MHz | All | |
| | 10b | Integrated | Integ | rated source enabled | All | |
| | 11b | Reserved | Rese | erved | All | |
| 8:7 | 120MHz_s | super-spread | l_sou | rce_enable | | |
| | Project: | | All | | | |
| | Default Value: 00b | | 00b |) | | |
| | This field enables the 120MHz super-SSC source for display | | | | | |
| | Value | Name | De | scription | Project | |
| | 00b | Disabled | So | urce disabled | All | |
| | 01b | Reserved | Re | served | All | |
| | 10b | Enabled | Int | egrated source enabled | All | |
| | 11b | Reserved | Re | served | All | |
| 6:2 | 120MHz_S | SSC4(variabl | e%)so | ource_programming | | |
| | Project: | | All | | | |
| | Default Va | lue: | 000 | 000b | | |
| | | | | ed for super-spread on LVDS. Please note that this reference is ATA it must not be used for LVDS | shared | |
| | Value | Name | | Description | Projec | |
| | 0XXXXb | Downspre | ad | Center vs downspread: this bit sets center vs downspread on the SSC4 modulator used for superspread. | All | |
| | 1XXXXb | Centerspr | ead | Center vs downspread: this bit sets center vs downspread on the SSC4 modulator used for superspread. | All | |
| | X0001b | 0% | | 0% SSC | All | |
| | X0010b | 0.5% | | 0.5% SSC (center or downspread) | All | |
| | X0011b | 1% | | 1.0% (center spread only) | All | |
| | X0100b | 1.5% | | 1.5% (center spread only) | All | |
| | | | | 2% (center spread only) | | |
| | X0101b | 2% | | 2 % (Center Spread Only) | All | |
| | X0101b X0110b | 2% 2.5% | | 2.5% (center spread only) | All | |



| 1 | 120MHz | _SSC1(-0.5%) | modulation_enable | | | |
|---|---|--------------|-------------------|---------|--|--|
| | Project: | | All | | | |
| | Default V | /alue: | Ob | | | |
| | PLL's using this clock as an input must be enabled not more than yyuS after this bit is enabled to ensure a stable input. | | | | | |
| | Value | Name | Description | Project | | |
| | 0b | Disabled | SSC1 disabled | All | | |
| | 1b | Enabled | SSC1 enabled | All | | |
| 0 | 120MHz | _SSC4_modu | lation_enable | | | |
| | Project: | | All | | | |
| | Default Value: | | 0b | | | |
| | This bit enables the variable % modulator used for the 120MHz SSC source used for LVDS. It must be set xxuS after the 120MHz SSC output is enabled. PLL's using this clock as an input must be enabled not more than yyuS after this bit is enabled to ensure a stable input. | | | | | |
| | Value | Name | Description | Project | | |
| | 0b | Disabled | SSC4 disabled | All | | |
| | 1 | | | | | |



2.3.1.8 RAWCLK_FREQ—Rawclk frequency

| Register 1 Address (Default Va Access: Bize (in bi | Dffset: C620 All alue: 00000 R/W | | | | | |
|---|---|------------------|-----------------------------------|----------------------------------|--|--|
| Bit | | | Descriptior | 1 | | |
| 31:14 | Reserved | Project: | All | Format: | | |
| 13:12 | FDL_TP1_ | Timer | Project: | All | | |
| | This field se | elects the minin | num time TP1 is to be sent durin | g training of the FDL interface. | | |
| | Value | Name | Description | Project | | |
| | 00b | 0.5us | 0.5us | All | | |
| | 01b | 1us | 1.0us | All | | |
| | 10b | 2us | 2.0us | All | | |
| | 11b | 4us | 4.0us | All | | |
| 11:10 | FDL_TP2_ | Timer | Project: | All | | |
| | This field selects the minimum time TP2 is to be sent during training of the FDL interface. | | | | | |
| | Value | Name | Description | Project | | |
| | 00b | 1.5us | 1.5us | All | | |
| | 01b | 3us | 3.0us | All | | |
| | 10b | 6us | 6.0us | All | | |
| | 11b | 12us | 12.0us | All | | |
| 9:0 | Rawclk fre | quency | Project: All Format: | | | |
| | Program thi | | clk frequency. This is used to ge | enerate a divided down clock for | | |



2.4 Panel Power Sequencing Registers

2.4.1.1 **PP_STATUS**—Panel Power Status Register

| | | F | PP_STATUS—Panel Power Status Register | |
|-------------------------|----------|--------------|---|---------|
| Register Ty | | 1MIO | | |
| Address O | A | | | |
| Project: Default Val | | 8000000ł | | |
| Access: | | lead Only | | |
| Size (in bit | | 2 | | |
| Bit | | | Description | |
| 31 | Panel_ | Power_C | n_Status | |
| | Project | : | All | |
| | Default | Value: | 0b | |
| | LCD di | splay by v | is selected as the target for the panel control, Software is responsible for enab writing a "1" to the port enable bit only after all transcoder timing and DPLL reg grammed and the PLL has locked to the reference signal. | |
| | This bit | is cleared | d (set to "0") only after the panel power down sequencing is completed. | |
| | Value | Name | Description | Project |
| | Ob | Off | Indicates that the panel power down sequencing has completed. A power cycle delay may be currently active. It is safe and allowed to program timing, port, and DPLL registers. If this bit is not a zero, it activates the register write protect and writes to those registers will be ignored unless the write protect key value is set in the panel sequencing control register. | All |
| | 1b | On | In conjunction with bits Power Sequence Progress field and Power Cycle Delay Active, this bit set to a one indicates that the panel is currently powered up or is currently in the power down sequence and it is unsafe to change the timing, port, and DPLL registers for the pipe or transcoder that is assigned to the panel output. | All |



| 30 | Require_Asset_Sta | tus | | | | | | |
|-------|---|--|----------|--|--|--|--|--|
| | Project: | All | | | | | | |
| | Default Value: | Ob | | | | | | |
| | This bit indicates the status of programming of the display PLL and the selected port. A power on cycle will not be allowed unless this status indicates that the required assets are programmed and ready for use. | | | | | | | |
| | The following condit | ons determine that the assets are ready: | | | | | | |
| | 1) Display pipe or transcoder PLL enabled and frequency locked. | | | | | | | |
| | 2) Display pipe or transcoder enabled. | | | | | | | |
| | 3) Port attached to the panel is enabled. | | | | | | | |
| | Value Name | Description | Project | | | | | |
| | 0b Not Ready | All required assets are not properly programmed | All | | | | | |
| | 1b Ready | All required assets are ready for the driving of a panel | All | | | | | |
| 29:28 | Power_Sequence_Progress | | | | | | | |
| | Project: | All | All | | | | | |
| | Default Value: | 0b | | | | | | |
| | Value Name | Description | Projec | | | | | |
| | 00b None | Indicates that the panel is not in a power sequence | All | | | | | |
| | 01b Power Up | Indicates that the panel is in a power up sequence (may include power cycle delay) | All | | | | | |
| | 10b Power Dow | n Indicates that the panel is in a power down sequence | All | | | | | |
| | 11b Reserved | Reserved | All | | | | | |
| 27 | Power_Cycle_Delay | /_Active | | | | | | |
| | Project: | All | | | | | | |
| | Default Value: | 1bA power cycle delay (T4) is currently active | | | | | | |
| | | occur after a panel power down sequence or after a hardware reset. On II occur using the default value for the timing. | reset, a | | | | | |
| | Value Name | Description | Projec | | | | | |
| | 0b Not Active | A power cycle delay is not currently active | All | | | | | |
| | 1b Active | A power cycle delay (T4) is currently active | All | | | | | |
| | December 1 Deci | ect: All Format: | | | | | | |
| 26:4 | Reserved Proje | Format. | | | | | | |



2.4.1.2 **PP_CONTROL**—Panel Power Control Register

| | | PP_CO | NTROL— | -Panel Power Contro | l Register | |
|-------------|--|---|---|--|--|--|
| Register 1 | ype: MM | 10 | | | | |
| Address C | Offset: C72 | 04h | | | | |
| Project: | All | | | | | |
| Default Va | | 00000h | | | | |
| Access: | R/W | / | | | | |
| Size (in bi | ts): 32 | | | | | |
| Bit | | | | Description | | |
| 31:16 | Reserved | | | | | |
| 15:3 | Reserved | Project: | All | | Format: | |
| 2 | Backlight | _Enable | | | | |
| | Project: | | All | | | |
| | Default Va | alue: | 0b | | | |
| | Software r target. | must enable th | nis bit after tra | aining the link, and disable it v | when disabling the p | panel power state |
| | 0 | | | | | |
| | Value | Name | De | scription | Pi | roject |
| | - | Name Disable | | scription cklight disabled | Pı Al | - |
| | Value | | Ba | - | | II |
| 1 | Value Ob 1b | Disable | Ba Ba | cklight disabled | AI | II |
| 1 | Value Ob 1b Power_Do | Disable Enable | Ba Ba | cklight disabled | AI | II |
| 1 | Value Ob 1b | Disable Enable | Ba Ba | cklight disabled | AI | II |
| 1 | Value 0b 1b Power_Do Project: Default Va Enabling t | Disable Enable own_on_Res alue: his bit causes | Bar Bar et All Ob the panel to | cklight disabled | Al Al g. When system res | II II set is initiated, th |
| 1 | Value 0b 1b Power_Do Project: Default Va Enabling t panel pow | Disable Enable own_on_Res alue: his bit causes | Bar Bar et All Ob the panel to | cklight disabled cklight enabled power down on reset warning automatically. If the panel is | Al Al g. When system res | II II set is initiated, th |
| 1 | Value 0b 1b Power_Do Project: Default Va Enabling t panel pow ignored. | Disable Enable own_on_Res alue: his bit causes ver down sequ | Bar Bar et All 0b the panel to ence begins Description | cklight disabled cklight enabled power down on reset warning automatically. If the panel is | Al Al g. When system res not on during a rese | II II set is initiated, the et event, this bit i Projec |



| 0 | Power_S | State_Tar | get | |
|---|------------|-------------|--|---------|
| | Project: | | All | |
| | Default V | alue: | 0b | |
| | Writing th | nis bit can | occur any time, it will only be used at the completion of any current power | cycle. |
| | Value | Name | Description | Project |
| | Ob | Off | The panel power state target is off, if the panel is either on or in a power on sequence, a power off sequence is started as soon as the panel reaches the power on state. This may include a power cycle delay. If the panel is currently off, there is no change of the power state or sequencing done. | All |
| | 1b | On | The panel power state target is on, if the panel is in either the off state or a power off sequence, if all pre-conditions are met, a power on sequence is started as soon as the panel reaches the power off state. This may include a power cycle delay. If the panel is currently off, there is no change of the power state or sequencing done. While the panel is on or in a power on sequence, the register write lock will be enabled. | |

2.4.1.3 **PP_ON_DELAYS**—Panel Power on Sequencing Delays

| | PP_ON_DELAYS—Panel | Power on S | equei | ncing Delays | |
|--------------|--|-------------|-------|--------------|----|
| Register T | ype: MMIO | | | | |
| Address O | ffset: C7208h | | | | |
| Project: | All | | | | |
| Default Val | lue: 00000000h | | | | |
| Access: | R/W Protect | | | | |
| Size (in bit | s): 32 | | | | |
| Nrite Prote | ect by Panel Power Sequencer | | | | |
| Bit | | Description | | | |
| 29 | Reserved Project: All | | | Format: | |
| 28:16 | Power_up_delay Project: All | Format: | | | |
| | Programmable value of panel power seque delay for the T1+T2 time sequence. The ti | | | | ıe |
| 15:13 | Reserved | Project: | All | Format: | |
| 12:0 | Power_on_to_Backlight_enable_delay | Project: | All | Format: | |
| | Programmable value of panel power seque delay for the T5 time sequence. The time | | | | е |



2.4.1.4 **PP_OFF_DELAYS**—Panel Power off Sequencing Delays

| | PP_OFF_DELAYS—Panel Power off Sequencing Delays |
|--------------|---|
| Register Ty | /pe: MMIO |
| Address O | ffset: C720Ch |
| Project: | All |
| Default Val | ue: 0000000h |
| Access: | R/W Protect |
| Size (in bit | s): 32 |
| Nrite Prote | ct by Panel Power Sequencer |
| Bit | Description |
| 31:29 | Reserved Project: All Format: |
| 28:16 | Power_Down_delay Project: All Format: |
| | Programmable value of panel power sequencing delay during power up. This provides the time delay for the T3 time sequence. The time unit used is the 100us timer. |
| 15:13 | Reserved Project: All Format: |
| 12:0 | Power_Backlight_off_to_power_down_delay Project: All Format: U32 |
| | Programmable value of panel power sequencing delay during power down. This provides the time delay for the Tx time sequence. The time unit used is the 100us timer. |



2.4.1.5 **PP_DIVISOR—Panel Power Cycle Delay and Reference Divisor**

| | PP_DIV | ISOR—Pane | el Power | Cycle Delay and Reference Divisor | | | | | | | |
|--|--|--|---|--|--|--|--|--|--|--|--|
| Register Ty | ype: MMIO | | | | | | | | | | |
| Address O | ffset: C7210 | h | | | | | | | | | |
| Project: | All | | | | | | | | | | |
| Default Val | lue: 00186 | 00186904h | | | | | | | | | |
| Access: | R/W P | R/W Protect | | | | | | | | | |
| Size (in bit | s): 32 | 32 | | | | | | | | | |
| This registe condition o reset. If th seconds, b programme | er selects the nce powered ne panel limit ut limited to 4 | down. This ha s how fast we n 400ms in the SI Special care is | sor and cont as a default nay sequence PWG specifi | trols how long the panel must remain in a power off value that allows a timer to initiate directly after device ce from up to down to up again. Typically this is 0.5-1.5 ication. This register forces the panel to stay off for a und reset and D3 cold situations to conform to power | | | | | | | |
| Bit | | | | Description | | | | | | | |
| 31:8 | Reference_divider | | | | | | | | | | |
| | Project: | All | | | | | | | | | |
| | Default Valu | e: 00 ⁻ | 1869h | 125MHz raw clock. | | | | | | | |
| | This field provides the value of the divider used for the creation of the panel timer reference clock. The output of the divider is used as the fastest of the three time bases (100us) for all other timers. The other time bases are divided from this frequency. The value of zero should not be used. When it is desired to divide by N, the actual value to be programmed is (N/2)-1. | | | | | | | | | | |
| | The value sl raw clock. | nould be (100 * R | ef clock frequ | uency in MHz / 2) - 1. The default value is for the 125MHz | | | | | | | |
| | Example: | | | | | | | | | | |
| | Reference C 233MHz 200MHz 125MHz | Clock Frequency | Value of F 2D81h 270Fh 1869h | ield | | | | | | | |
| 7:5 | Reserved | Project: | 411 | Format: | | | | | | | |



| 4:0 | Power_Cycle_Delay Project: All Form | nat: |
|-----|---|---|
| | Programmable value of time panel must remain in a po devices coming out of reset, the default values will def sequence can be started. This field uses the 0.1 S tim on sequence is attempted during this delay, the power cycle delay is complete. Writing a value of 0 selects r active. | fine how much time must pass before a power of ne base unit from the divider. If the panel power r on sequence will commence once the power |
| | During the initial power up reset, a D3 cold power cycle will be set to the default value and the count down will this field to a zero while the count is active will abort the the T4 of the SPWG specification. Note: Even if the p reset. | begin after the de-assertion of reset. Writing his portion of the sequence. This corresponds to |
| | This register needs to be programmed to a "+1" value. specification of 400mS, program 5 to achieve at least 4 | |

2.5 Backlight Control Registers

2.5.1.1 Backlight PWM PCH Control Register

| | | Bacl | klight PWM PCH Control Register | |
|-------------------|---------------|---------------|------------------------------------|---------|
| Register T | ype: MMI | 0 | | |
| Address O | ffset: C82 | 50h | | |
| Project: | All | | | |
| Default Va | lue: 0000 | 0000h | | |
| Access: | R/W | | | |
| Size (in bit | s): 32 | | | |
| Bit | | | Description | |
| 31 | PWM_PC | H_Enable | | |
| | Project: | | All | |
| | Default Va | lue: | Ob | |
| | This bit en | ables the PWM | counter logic in the PCH. | |
| | Value | Name | Description | Project |
| | 0b | Disable | PCH PWM disabled (drives 0 always) | All |
| | 1b | Enable | PCH PWM enabled | All |
| 30 | Reserved | | | |



| 29 | Backligh | t_Polarity | | |
|----|------------|-------------|-------------------------------|---------|
| | Project: | | All | |
| | Default V | alue: | Ob | |
| | This field | controls th | e polarity of the PWM signal. | |
| | Value | Name | Description | Project |
| | 0b | High | Active High | All |
| | 1b | Low | Active Low | All |



2.5.1.2 Backlight PWM PCH Control Register

| Backlight PWM PCH Control Register | | | | | | | | | |
|------------------------------------|---------------|---|--|--|--|--|--|--|--|
| Register T | ype: | MMIO | | | | | | | |
| Address Offset: | | C8254h | | | | | | | |
| Project: | | All | | | | | | | |
| Default Va | lue: | 0000000h | | | | | | | |
| Access: | | R/W | | | | | | | |
| Size (in bit | :s): | 32 | | | | | | | |
| Bit | | Descri | otion | | | | | | |
| 31:16 | Back | klight_Modulation_Frequency | Project: All Format: | | | | | | |
| | back clock | field determines the number of time base events light control. This field is normally set once during that is being used and the desired PWM frequent stream in PCH display raw clocks multiplied by | g initialization based on the frequency of the cy. This value represents the period of the | | | | | | |
| 15:0 | Rese | erved | Project: All | | | | | | |



3. South Transcoder and Port Controls (E0000h–EFFFFh)

3.1 Transcoder A Timing

3.1.1.1 TRANS_HTOTAL_A—Transcoder A Horizontal Total Register

| | TRANS | _HTOTA | L_A—Tı | anscoder A Horizontal Total Register |
|--|--|---|--|---|
| Register T Address C Project: Default Va Access: | All | - | | |
| Size (in bi | | | | |
| Bit | | | | Description |
| 31:29 | Reserved | Project: | All | Format: MBZ |
| 28:16 | Project: Default Value This 13-bit fie Display perio desired minu This number | e: eld provides od, front/back is one. of clocks ne nould always | All Ob Horizontal ⁻ border and eds to be a be equal of | Total up to 8192 pixels encompassing the Horizontal Active d retrace period. This field is programmed to the number of clocks multiple of two when driving the LVDS port in two channel mode. r greater to the sum of the horizontal active and the horizontal |
| 15:12 | Reserved | Project: | All | Format: MBZ |
| 11:0 | Project: Default Value This 12-bit fie horizontal ac (active pixels | e: eld provides tive display p s/line – 1). | All Ob Horizontal <i>J</i> bixel is cons | Display_Pixels Active Display resolutions up to 4096 pixels. Note that the first sidered pixel number 0. The value programmed should be the nited to multiples of two pixels when driving the LVDS port in two |
| | The number | of active pixe | | nited to multiples of two pixels when driving the LVDS port in tv ntal active display size allowed will be 64 pixels. |



3.1.1.2 TRANS_HBLANK_A—Transcoder A Horizontal Blank Register

| | TRANS | _HBLANK | _A—Tra | anscoder A Horizontal Blank Register | | | | |
|--------------|---|----------------|-------------|--|--|--|--|--|
| Register T | ype: MMIO | | | | | | | |
| - | offset: E0004h | า | | | | | | |
| Project: | All | | | | | | | |
| Default Va | lue: 000000 |)00h | | | | | | |
| Access: | R/W | | | | | | | |
| Size (in bit | t s): 32 | | | | | | | |
| Bit | | | | Description | | | | |
| 31:29 | Reserved | Project: | All | Format: MBZ | | | | |
| 28:16 | Transcoder_ | _A_Horizonta | I_Blank_E | nd | | | | |
| | Project: | | All | | | | | |
| | Default Value: 0b | | | | | | | |
| | This 13-bit field specifies the position of Horizontal Blank End expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HBLANK End pixel position, where the first active pixel is considered position 0; the second active pixel is considered position 1, etc. Horizontal blank ending at the same point as the horizontal total indicates that there is no left hand border area. HBLANK size has a minimum value of 32 clocks. | | | | | | | |
| | The number of clocks within blank needs to be a multiple of two when driving the LVDS port in two channel mode. | | | | | | | |
| | The value loaded in the register would be equal to RightBorder+Active+HBlank-1. | | | | | | | |
| | | | | Vout port the border must be zero. In that case this register is HTOTAL register. | | | | |
| 15:13 | Reserved | Project: | All | Format: MBZ | | | | |
| 12:0 | Transcoder | _A_Horizonta | I_Blank_S | tart | | | | |
| | Project: | | All | | | | | |
| | Default Value | 9: | 0b | | | | | |
| | This 13-bit field specifies the Horizontal Blank Start position expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HBLANK Start pixel position, where the first active pixel is considered position 0; the second active pixel is considered position 1, etc. | | | | | | | |
| | | n two channel | | d right borders need to be a multiple of two when driving the rizontal blank should only start after the end of the horizontal | | | | |
| | The value loa | aded in the re | gister woul | d be equal to RightBorder+Active-1. | | | | |
| | | | | Vout port the border must be zero. In that case this register is HACTIVE register. | | | | |



3.1.1.3 TRANS_HSYNC_A—Transcoder A Horizontal Sync Register

| | | | • • T | enceder Allerizentel Cure Derieter | | | | |
|-------------|--|--|--------------|---|--|--|--|--|
| Register T | | S_HSYNC | ∠A—Ir | anscoder A Horizontal Sync Register | | | | |
| Address C | | า | | | | | | |
| Project: | All | | | | | | | |
| Default Va | lue: 000000 |)00h | | | | | | |
| Access: | R/W | | | | | | | |
| Size (in bi | ts): 32 | | | | | | | |
| Bit | | | | Description | | | | |
| 31:29 | Reserved | Project: | All | Format: MBZ | | | | |
| 28:16 | Transcoder | _A_Horizont | al_Sync_E | Ind | | | | |
| | Project: | | All | | | | | |
| | Default Value | e: | 0b | | | | | |
| | End pixel pos considered p | sition, where position 1, etc | the first ac | ive display start. The value programmed should be the HSYNC tive pixel is considered position 0; the second active pixel is | | | | |
| | two channel i | mode. This v | alue shoul | riod needs to be a multiple of two when driving the LVDS port in d be greater than the horizontal sync start position and would be FrontPorch+Sync-1. | | | | |
| 15:13 | Reserved | Project: | All | Format: MBZ | | | | |
| 12:0 | Transcoder_A_Horizontal_Sync_Start | | | | | | | |
| | Project: | | All | | | | | |
| | Default Value | e: | 0b | | | | | |
| | number relat Start pixel po considered p | This 13-bit field specifies the horizontal Sync Start position expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HSYNC Start pixel position, where the first active pixel is considered position 0; the second active pixel is considered position 1, etc. Note that when HSYNC Start is programmed equal to HBLANK Start, both HSYNC and HBLANK will be asserted on the same pixel clock. It should never be programmed to less | | | | | | |
| | LVDS port in | two channel | mode. Th | ning of the line needs to be a multiple of two when driving the is register should not be less than the horizontal active end. This ctive+RightBorder+FrontPorch-1. | | | | |



3.1.1.4 TRANS_VTOTAL_A—Transcoder A Vertical Total Register

| | TRAN | IS VTOT | ΔΙ Δ—Τ | ranscoder A Vertical Total Register |
|--|---|---|--|---|
| Register T Address O Project: Default Va Access: Size (in bit | ype: MMIO iffset: E000C All lue: 000000 R/W | h | <u></u> | |
| Bit | | | | Description |
| 31:29 | Reserved | Project: | All | Format: MBZ |
| 28:16 | Lines, top/bo required mine active, vertica leading edge | e: ttom border a us one. Vert al border, and of the horizo fields. In inte | All Ob /ertical Total and retrace p cal total nee d the vertical ontal sync. F erlaced mode | I up to 8192 lines encompassing the Vertical Active Display beriod. The value programmed should be the number of lines eds to be large enough to be greater than the sum of the vertical I blank regions. The vertical counter is incremented on the For interlaced display modes, this indicates the total number of es, hardware automatically divides this number by 2 to get the |
| 15:12 | Reserved | Project: | All | Format: MBZ |
| 11:0 | with the desir vertical active | e: eld provides v red number c e area must b th fields. In i | All Ob vertical active of lines minus be seven line nterlaced mo | play_Pixels e display resolutions up to 4096 lines. It should be programmed s one. When using the internal panel fitting logic, the minimum es. For interlaced display modes, this indicates the total number odes, hardware automatically divides this number by 2 to get the |



3.1.1.5 TRANS_VBLANK_A—Transcoder A Vertical Blank Register

| | TRANS_VBLANK_A—Transcoder A Vertical Blank Register |
|--|---|
| Register T Address O Project: Default Va Access: Size (in bit | ype: MMIO bffset: E0010h All lue: 00000000h R/W |
| Bit | Description |
| 31:29 | Reserved Project: All Format: MBZ |
| 28:16 | Transcoder_A_Vertical_Blank_End Project: All Default Value: Ob This 13-bit field specifies the Vertical Blank End position expressed in terms of the absolute Line number relative to the vertical active display start. The value programmed should be the VBLANK End line position, where the first active line is considered line 0, the second active line is considered line 1, etc. The end of vertical blank should be after the start of vertical blank and before or equal to the vertical total. This register should be loaded with the Vactive+BottomBorder+VBlank-1. For interlaced display modes, hardware automatically divides this number by 2 to get the vertical blank end in each field. It does not count the two half lines that get added when operating in modes with half lines. If this transcoder is connected to the TVout port the border must be zero. In that case this register is programmed to the same value as the VTOTAL register. |
| 15:13 | Reserved Project: All Format: MBZ |
| 12:0 | Transcoder_A_Vertical_Blank_Start Project: All Default Value: Ob This 13-bit field specifies the Vertical Blank Start expressed in terms of the absolute line number relative to the vertical active display start. The value programmed should be the VBLANK Start line position, where the first active line is considered line 0, the second active line is considered line 1, etc. Minimum vertical blank size is required to be at least three lines. Blank should start after the end of active. This register is loaded with the Vactive+BottomBorder-1. For interlaced display modes, hardware automatically divides this number by 2 to get the vertical blank start in each field. It does not count the two half lines that get added when operating in modes with half lines. If this transcoder is connected to the TVout port the border must be zero. In that case this register is programmed to the same value as the VACTIVE register. |



3.1.1.6 TRANS_VSYNC_A—Transcoder A Vertical Sync Register

| | TRA | NS_VSYN | IC_A—Tran | scoder A Vertical Sync Register |
|--|---|--|---|---|
| Register T Address C Project: Default Va Access: | Offset: E0014 All | | | |
| Size (in bi | | | | |
| Bit | | | | Description |
| 31:29 | Reserved | Project: | All | Format: MBZ |
| 28:16 | Project: Default Value This 13-bit fir number relat line position, etc. This reg display mode | eld specifies tive to the ver where the fir gister should es, hardware | All Ob the Vertical Syn tical active disp st active line is be loaded with V automatically di | c End position expressed in terms of the absolute Line lay start. The value programmed should be the VSYNC End considered line 0, the second active line is considered line 1, /active+BottomBorder+FrontPorch+Sync-1. For interlaced ivides this number by 2 to get the vertical sync end in each that get added when operating in modes with half lines. |
| 15:13 | Reserved | Project: | All | Format: MBZ |
| 12:0 | Project: Default Value This 13-bit fie number relat line position, | eld specifies tive to the ver where the fir gister would b | All 0b the Vertical Syn tical active disp st active line is e loaded with V | c Start position expressed in terms of the absolute line lay start. The value programmed should be the VSYNC Start considered line 0, the second active line is considered line 1, active+BottomBorder+FrontPorch-1. For interlaced display his number by 2 to get the vertical sync start in each field. It |



3.1.1.7 TRANS_BCLRPAT_A— Transcoder A Border Color Pattern Register

| | | B | CLRPAT_ | A— Tr | anscoder A | Border Col | or Patter | n Re | gister | |
|---------------------|-------------------------|---------------|--------------------------------|----------|----------------|------------|--------------|---------|------------------------------------|--|
| Register Type: MMIO | | | | | | | | | | |
| Address Of | Address Offset: E0020h | | | | | | | | | |
| Project: | All | | | | | | | | | |
| Default Val | Default Value: 0000000h | | | | | | | | | |
| Access: | R/ | V | | | | | | | | |
| Size (in bits | s): 32 | | | | | | | | | |
| between th | e end of a rogramme | activ ed w | ve and the b vith 8 bits pe | eginning | g of blank and | | k and the be | əginniı | ng of active. The he transcoder is | |
| Bit | | | | | Des | cription | | | | |
| 31:24 | Reserve | b | Project: | All | | | Forma | at: | | |
| 23:16 | Border_ | Red | _Channel_V | alue | | | Project: | All | Format: | |
| 15:8 | Border_ | Gree | en_Channel_ | Value | | | Project: | All | Format: | |
| 7:0 | Border_ | Blue | e_Channel_V | /alue | | | Project: | All | Format: | |



3.1.1.8 TRANS_VSYNCSHIFT_A— Transcoder A Vertical Sync Shift Register

| Т | RANS_VS | YNCSHIF | T_A— Tra | nscoder A Vertical Syr | nc Shift F | Register | | |
|--------------|--|---|----------------|------------------------------|------------|--------------|--|--|
| Register Ty | /pe: MMIO | | | | | | | |
| Address O | ffset: E0028h | า | | | | | | |
| Project: | All | | | | | | | |
| Default Val | ue: 000000 | 00h | | | | | | |
| Access: | R/W Pr | oject | | | | | | |
| Size (in bit | | | | | | | | |
| Write Prote | ct by Panel Pov | wer Sequence | r when panel i | s connected to transcoder A. | | | | |
| Bit | Description | | | | | | | |
| 31:13 | Reserved | Project: | All | | Format: | MBZ | | |
| 120 | Transcoder_ | A_Second_F | ield_Vertical_ | _Sync_Shift | | Project: All | | |
| | This value specifies the vertical sync alignment for the start of the interlaced second field expressed in terms of the absolute pixel number relative to the horizontal active display start. | | | | | | | |
| | This value will only be used if the transcoder is in an interlaced mode. | | | | | | | |
| | Typically, the interlaced second field vertical sync should start one pixel after the point halfway between successive horizontal syncs, so the value of this register should be programmed to: (horizontal sync start - floor[horizontal total / 2]). | | | | | | | |
| | | (For calculation, use the actual horizontal sync start and horizontal total values and not the minus one values programmed into the registers) | | | | | | |
| | | This vertical sync shift only occurs during the interlaced second field. In all other cases the vertical sync start position is aligned with horizontal sync start. | | | | | | |

3.2 Transcoder A M/N Values

Calculation of TU, Data M, and Data N is as follows: For modes that divide into the link frequency evenly, Active/TU = Payload/Capacity = Data M/N = dot clock * bytes per pixel / ls_clk * number of lanes Default value to program TU size is "111111" for TU size of 64

Calculation of Link M and Link N is as follows: Link M/N = dot clock / ls_clk

When switching between two refresh rates, both the M1/N1 data and link values and the M2/N2 link values must be programmed. For dynamic refresh rate control, M1/N1 values are used for higher power, and M2/N2 values are used for lower power. Selection of M1/N1 or M2/N2 is indicated via MSA from the CPU display.



3.2.1.1 TransADataM1— Transcoder A Data M value 1

| | Tra | nsADataM1- | — Transcoder A Da | ata M value 1 | |
|-------------------|-----------------------|-------------------|-------------------------|---------------|--------------|
| Register T | уре: | MMIO | | | |
| Address C | Offset: | E0030h | | | |
| Project: | | All | | | |
| Default Va | lue: | 00000000h | | | |
| Access: | | R/W | | | |
| Size (in bi | ts): | 32 | | | |
| Double Bu | Iffer Update Point: | Start of Vblank | | | |
| Double Bu | uffer Armed By: | Writing the Tran | nsADPLinkN1 | | |
| | | | | | |
| Bit | | | Description | | |
| 31 | Reserved Pr | oject: All | | Format: | MBZ |
| 30:25 | TU1_Size | Project: | All | | |
| | This field is the siz | e of the transfer | unit for DP, minus one. | | |
| 24 | Reserved Pr | oject: All | | Format: | MBZ |
| 23:0 | Transcoder_A_Da | ata_M1_value | | | Project: All |
| | This field is the M1 | value for interna | al use of the DDA. | | |

3.2.1.2 TransADataN1— Transcoder A Data N value 1

| Register Type: Address Offset: | | MMIO | | | | | |
|--|----------|-------------|--------------|---------------------|-----|---------|--------------|
| | | E0034h | | | | | |
| Project: | | All | | | | | |
| Default Value: | | 0000000 |)0h | | | | |
| Access: | | R/W | | | | | |
| Size (in bits): Double Buffer Update Point: | | 32 | | | | | |
| | | Start of \ | Vblank | | | | |
| Double Buffer Arme | l By: | Writing th | he TransADF | ² LinkN1 | | | |
| Bit | | | | Descript | ion | | |
| 31:24 Reserve | d P | roject: | All | | | Format: | MBZ |
| 23:0 Transco | der_A_D | ata_N1_va | alue | | | | Project: All |
| This fiel | is the N | 1 value for | internal use | of the DDA. | | | |



3.2.1.3 TransADataM2— Transcoder A Data M value 2

| Register 1 | Type: | MMIO | | | |
|-------------------|-----------------------|------------------------------|----------------|---------|--------------|
| Address (| | E0038h | | | |
| Project: | | All | | | |
| - Default Va | alue: | 00000000h | | | |
| Access: | | R/W | | | |
| Size (in bi | its): | 32 | | | |
| Double B | uffer Update Point: | Start of Vblank | | | |
| Double B | uffer Armed By: | Writing the TransADPLi | nkN2 | | |
| | - | | | | |
| Bit | | | Description | | |
| 31 | Reserved Pr | oject: All | Form | nat: MB | Z |
| 30:25 | TU2_Size | Project: All | | | |
| | This field is the siz | e of the transfer unit for D | DP, minus one. | | |
| 24 | Reserved Pr | oject: All | Form | nat: MB | Z |
| | | | | · | |
| 23:0 | Transcoder_A_D | ata_M2_value | | | Project: All |

3.2.1.4 TransADataN2— Transcoder A Data N value 2

| Default Value: Access: Size (in bits): | | MMIO | | | | | |
|--|----------------------|--------------------------|---------------|---------|--------------|--|--|
| | | E003Ch | | | | | |
| | | All | | | | | |
| | | 00000000h | | | | | |
| | | R/W | | | | | |
| | | 32 | | | | | |
| | | Start of Vblank | | | | | |
| Double Bu | Iffer Armed By: | Writing the TransAD | PLinkN2 | | | | |
| Bit | | | Description | | | | |
| 31:24 | Reserved Pr | roject: All | | Format: | MBZ | | |
| 23:0 | Transcoder_A_D | ata_N2_value | | | Project: All | | |
| | This field is the N2 | 2 value for internal use | e of the DDA. | | | | |



3.2.1.5 TransADPLinkM1— Transcoder A Link M value 1

| | Tran | sADPLink | / 1— Transco | der A Link | M value 1 | |
|--------------------|---------------------|-----------------|---------------------|---------------|----------------|--------------|
| Register Ty | ype: | MMIO | | | | |
| Address Of | ffset: | E0040h | | | | |
| Project: | | All | | | | |
| Default Val | ue: | 00000000h | | | | |
| Access: | | R/W | | | | |
| Size (in bits | s): | 32 | | | | |
| Double But | ffer Update Point: | Start of Vblank | k | | | |
| Double Buf | ffer Armed By: | Writing the Tra | ansADPLinkN1 | | | |
| Bit | | | Desci | ription | | |
| 31:24 | Reserved P | oject: All | | | Format: | MBZ |
| 23:0 | Transcoder_A_L | nk_M1_value | | | | Project: All |
| | This field is the M | value for exter | nal transmission in | the Main Stre | am Attributes. | |

3.2.1.6 TransADPLinkN1— Transcoder A Link N value 1

| Deviator T | | SADPLinkN1— Trai | | | |
|-------------------------|----------------------|-----------------------------|------------------------|------------------|--------------|
| Register T | | | | | |
| Address C | itset: | E0044h | | | |
| Project: | | All | | | |
| Default Va | lue: | 00000000h | | | |
| Access: | | R/W | | | |
| Size (in bits): | | 32 | | | |
| Double Bu | Iffer Update Point: | Start of Vblank | | | |
| Double Buffer Armed By: | | Writing the TransADPLink | N1 | | |
| Bit | | | Description | | |
| 31:24 | Reserved P | oject: All | | Format: | MBZ |
| 23:0 | Transcoder_A_L | ink_N1_value | | | Project: All |
| | This field is the N1 | value for external transmis | sion in the Main Strea | m Attributes and | VB-ID. |



3.2.1.7 TransADPLinkM2— Transcoder A Link M value 2

| Tra | nsADPLinkM2— Transcode | er A Link M value 2 | |
|-----------------------------------|---|---------------------------|--------------|
| Register Type: | MMIO | | |
| Address Offset: | E0048 | | |
| Project: | All | | |
| Default Value: | 0000000h | | |
| Access: | R/W | | |
| Size (in bits): | 32 | | |
| Double Buffer Update Point | Start of Vblank | | |
| Double Buffer Armed By: | Writing the TransADPLinkN2 | | |
| Bit | Descrip | tion | |
| 31:24 Reserved F | Project: All | Format: | MBZ |
| 23:0 Transcoder_A_ | _ink_M2_value | | Project: All |
| This field is the M | 2 value for external transmission in th | e Main Stream Attributes. | |

3.2.1.8 TransADPLinkN2— Transcoder A Link N value 2

| Tra | ansADPLinkN2— Transcode | r A Link N value 2 | |
|----------------------------------|---|------------------------------|--------------|
| Register Type: | MMIO | | |
| Address Offset: | E004Ch | | |
| Project: | All | | |
| Default Value: | 0000000h | | |
| Access: | R/W | | |
| Size (in bits): | 32 | | |
| Double Buffer Update Poin | t: Start of Vblank | | |
| Double Buffer Armed By: | Writing the TransADPLinkN2 | | |
| Bit | Descripti | on | |
| 31:24 Reserved | Project: All | Format: | MBZ |
| 23:0 Transcoder_A | Link_N2_value | | Project: All |
| This field is the | N2 value for external transmission in the | Main Stream Attributes and V | ′B-ID. |



3.3 Transcoder A Video DIP

3.3.1.1 VIDEO_DIP_CTL_A—Video DIP Control for Transcoder A

| | VIDEO_DIP_CTL_A—Video DIP Control for Transcoder A | | | | | |
|-----------------------|---|--|--|--|--|--|
| Register Type: | MMIO | | | | | |
| Address Offset: | E0200h | | | | | |
| Project: | All | | | | | |
| Default Value: | 2000000h | | | | | |
| Access: | R/W | | | | | |
| Size (in bits): | 32 | | | | | |
| | Please note that writes to this register take effect immediately. Therefore, it is critical for software to follow he write and read sequences as described in the bit 31 text. | | | | | |



| | VI | DEO_DIP_C | TL_A—Video DIP Control for T | ranscoder A |
|-----|---|--|--|---|
| Bit | | | Description | |
| 31 | Project: Default V Data Isla VBLANK sent onc transcod transcod Please n are prog register, 1) 2) 3) 4) 5) | Yalue: And Packet (DIP) i This includes he e per vsync, once er, through any di er. Note that the audio rammed by the audio address E20B4h. Write sequence: Write sequence: Write for 1 VSync Disable the DIP ty Set the DIP data 1 DWORD write, with been reached. Ple Enable the DIP ty Reading sequence Set the DIP buffer Set the DIP accession Set the DIP accession Se | Island_Packet All Ob is a mechanism that allows up to 36 bytes to eader, payload, checksum and ECC informa- every other vsync, or once. This data can igital port (digital port B, C or D), but not two o subsystem is also capable of sending Data udio driver and can be read by in MMIO spa to ensure completion of any pending DIP tra- ype (bits 24:21) and set the DIP buffer index ss address (bits 3:0) to 0, or to the desired I DWORD at a time. The IF access address a rapping around to address 0 when the max lease note that software must write an entire ype and transmission frequency. | ation. Each type of DIP can be be transmitted on either o simultaneously on one a Island Packets. These packets ice via the audio control state ansmissions. ((bits 20:19) for the DIP being DWORD to be written. autoincrements with each buffer address size of 0xF has e DWORD at a time. |
| | wrapping Value | around to addres | ss 0 when the max buffer address size of 0x | |
| | 0b | Disable | Description Video DIP is disabled | Project All |
| | 1b | Enable | Video DIP is enabled | All |
| | Progra | mming Notes | | |
| | + | | e never sent out while the port is enabled. D transferred will result in the DIP being comp | |
| | + | | port on which DIP is being transmitted will r no need to switch off the DIP enable bit if the | |
| | + | When disabling disable DIP. | both the DIP port and DIP transmission, first | st disable the port and then |
| | + | | function at the same time that the DIP woul nabled) will result in the DIP being sent on the | |
| | + | Enabling should | d only be done after the buffer contents have | e been written. |



| 30:29 | Port_Sele | ct | | | | | | |
|-------|--|---|---|---|--|--|--|--|
| | Project: | All | | | | | | |
| | Default Va | Default Value: 01b Digital Port B | | | | | | |
| | | ts which port is to tr on is enabled. | ransmit the data island. This field must not be changed while date | ata island | | | | |
| | Value | Name | Description Project | | | | | |
| | 00b | Reserved | Reserved All | | | | | |
| | 01b | Digital Port B | Digital Port B (Default) All | | | | | |
| | 10b | Digital Port C | Digital Port C All | | | | | |
| | 11b | Digital Port D | Digital Port D All | | | | | |
| 28:26 | Reserved | Project: A | All Format: | | | | | |
| 25 | GCP_DIP | _enable | | | | | | |
| | Project: | All | | | | | | |
| | Default Va | lue: 0b | | | | | | |
| | This hit en | ables the output of | the General Control Packet GCP is different from other DIPs i | n that | | | | |
| | much of th | e payload is autom Please refer to the G | the General Control Packet. GCP is different from other DIPs i natically reflected in the packet, and therefore a DIP buffer for G GCP payload register for payload details. Writes to this bit take | CP is not | | | | |
| | much of th needed. F immediate | le payload is autom Please refer to the G Iy. | atically reflected in the packet, and therefore a DIP buffer for G | CP is not effect | | | | |
| | much of th needed. F immediate This bit sh | le payload is autom Please refer to the G Iy. | natically reflected in the packet, and therefore a DIP buffer for G GCP payload register for payload details. Writes to this bit take | CP is not effect | | | | |
| | much of th needed. F immediate This bit sh mode. | le payload is autom Please refer to the C ly. oud not be enabled | natically reflected in the packet, and therefore a DIP buffer for G GCP payload register for payload details. Writes to this bit take I for 8bpc mode if at least one of the other HDMI ports is enable | CP is not effect | | | | |
| | much of th needed. F immediate This bit sh mode. Value | e payload is autom Please refer to the G ly. oud not be enabled Name | Description Project | CP is not effect | | | | |
| 24:21 | much of th needed. F immediate This bit sh mode. Value 0b 1b | le payload is autom Please refer to the G ly. oud not be enabled Name Disable | batically reflected in the packet, and therefore a DIP buffer for G GCP payload register for payload details. Writes to this bit take If for 8bpc mode if at least one of the other HDMI ports is enable Description Project GCP DIP disabled All GCP DIP enabled All | CP is not effect | | | | |
| 24:21 | much of th needed. F immediate This bit sh mode. Value 0b 1b | e payload is autom Please refer to the G ly. oud not be enabled Name Disable Enable | Description Project GCP DIP disabled All GCP DIP enabled All | CP is not effect | | | | |
| 24:21 | much of th needed. F immediate This bit sh mode. Value Ob 1b Data_Islar | ne payload is autom Please refer to the G ly. oud not be enabled Name Disable Enable nd_Packet_type_e All | Description Project GCP DIP disabled All GCP DIP enabled All | CP is not effect | | | | |
| 24:21 | much of th needed. F immediate This bit sh mode. Value Ob 1b Data_Islan Project: Default Va These bits is enabled | e payload is autom Please refer to the G ly. oud not be enabled Name Disable Enable nd_Packet_type_e All ilue: 000 | natically reflected in the packet, and therefore a DIP buffer for G GCP payload register for payload details. Writes to this bit take If for 8bpc mode if at least one of the other HDMI ports is enable Description Project GCP DIP disabled All GCP DIP enabled All enable Enable AVI DIP of a given data island packet (DIP) type. It can be updated whil v updated (not double-buffered). Within 2 vblank periods, the D | CP is not effect d in 12bpc | | | | |
| 24:21 | much of th needed. F immediate This bit sh mode. Value Ob 1b Data_Islan Project: Default Va These bits is enabled | e payload is autom Please refer to the G ly. oud not be enabled Name Disable Enable nd_Packet_type_e All lue: 000 enable the output of and is immediately | natically reflected in the packet, and therefore a DIP buffer for G GCP payload register for payload details. Writes to this bit take If for 8bpc mode if at least one of the other HDMI ports is enable Description Project GCP DIP disabled All GCP DIP enabled All enable Enable AVI DIP of a given data island packet (DIP) type. It can be updated whil v updated (not double-buffered). Within 2 vblank periods, the D | CP is not effect d in 12bpc | | | | |
| 24:21 | much of th needed. F immediate This bit sh mode. Value 0b 1b Data_Islan Project: Default Va These bits is enabled guarantee | e payload is autom Please refer to the G ly. oud not be enabled Name Disable Enable nd_Packet_type_e All Ilue: 000 enable the output o and is immediately d to have been tran | natically reflected in the packet, and therefore a DIP buffer for G GCP payload register for payload details. Writes to this bit take a for 8bpc mode if at least one of the other HDMI ports is enable Description Project GCP DIP disabled All GCP DIP enabled All enable Enable AVI DIP of a given data island packet (DIP) type. It can be updated while updated (not double-buffered). Within 2 vblank periods, the D hsmitted. | CP is not effect d in 12bpc | | | | |
| 24:21 | much of th needed. F immediate This bit sh mode. Value Ob 1b Data_Islan Project: Default Va These bits is enabled guarantee Value | e payload is autom Please refer to the G ly. oud not be enabled Name Disable Enable md_Packet_type_e All ilue: 000 e enable the output of and is immediately d to have been tran Name | natically reflected in the packet, and therefore a DIP buffer for G GCP payload register for payload details. Writes to this bit take a for 8bpc mode if at least one of the other HDMI ports is enable Description Project GCP DIP disabled All GCP DIP enabled All enable Enable AVI DIP of a given data island packet (DIP) type. It can be updated whill v updated (not double-buffered). Within 2 vblank periods, the D ismitted. Description | CP is not effect d in 12bpc e the port P is Projec | | | | |
| 24:21 | much of th needed. F immediate This bit sh mode. Value 0b 1b Data_Islan Project: Default Va These bits is enabled guarantee Value XXX1b | e payload is autom Please refer to the G ly. oud not be enabled Name Disable Enable nd_Packet_type_e All slue: 000 enable the output of and is immediately d to have been tran Name Enable AVI | natically reflected in the packet, and therefore a DIP buffer for G GCP payload register for payload details. Writes to this bit take If for 8bpc mode if at least one of the other HDMI ports is enable Description Project GCP DIP disabled All GCP DIP enabled All enable Enable AVI DIP of a given data island packet (DIP) type. It can be updated whil / updated (not double-buffered). Within 2 vblank periods, the D ismitted. Description Enable AVI DIP (Default = enabled) | CP is not effect d in 12bpc e the port P is Projec All | | | | |



| | VID | EO_DIP_CTL_# | A—Video DIP Control for Transco | oder A |
|---------------|--|---|---|--|
| 20:19 | DIP_buffer | index | | |
| | Project: | All | | |
| | Default Valu | ue: 00b | | |
| | | | nming of different DIPs. These bits are used as smission frequency must also be written when | |
| | Value | Name | Description | Project |
| | 00b | AVI | AVI DIP (31 bytes of space available) | All |
| | 01b | Vendor-specific | Vendor-specific DIP | All |
| | 10b | Gamut Metadata | Gamut Metadata Packet | All |
| | 11b | Source Product | Source Product Description DIP | All |
| 18 | Reserved | Project: All | Forr | nat: |
| 17:16 | Video_DIP | _transmission_freq | uency | |
| | Project: | All | | |
| | Default Valu | ue: 00b | | |
| | | | of Video DIP transmission for the DIP buffer in data, this value is also latched when the first D | |
| | | , this value reflects th in bits 20:19. | ne Video DIP transmission frequency for the Vi | deo DIP buffer |
| | Value | Name | Description | Project |
| | 00b | Send Once | Send Once | All |
| | 01b | Every VSync | Send Every VSync (Default for AVI) | |
| | | , | Send Every VSync (Delault for AVI) | All |
| 1 | 10b | Every Other Vsync | | All All |
| | 10b 11b | | | |
| 15:12 | | Every Other Vsync Reserved | Send at least every other VSync | All All |
| - | 11b Reserved | Every Other Vsync Reserved Project: All | Send at least every other VSync Reserved | All All |
| 15:12 11:8 | 11b Reserved Video_DIP | Every Other Vsync Reserved | Send at least every other VSync Reserved | All All |
| - | 11b Reserved | Every Other Vsync Reserved Project: All _buffer_size | Send at least every other VSync Reserved Forr | All All |
| - | 11b Reserved Video_DIP Project: | Every Other Vsync Reserved Project: All buffer_size All Read | Send at least every other VSync Reserved Forr | All All |
| | 11b Reserved Video_DIP Project: Access: Default Valu This reflects this register Please note | Every Other Vsync Reserved Project: All buffer_size All Read ue: 0000b s the buffer size in dw r, including the heade | Send at least every other VSync Reserved Forr Only ovords available for the type of Video DIP being er. It is hardwired to the maximum size of a Vid des ECC bytes, which are not writable by softw | AII AII mat: MBZ indexed by bits 20:19 of leo DIP, 36 bytes. |



| | VIDEO_DIP_CTL_A—Video DIP Control for Transcoder A | | |
|-----|--|-------------|-----|
| 3:0 | Video_DIP_RAM_access_address | Project: | All |
| | Selects the DWORD address for access to the Video DIP buffers. This value is automa incremented after each read or write of the Video DIP Data Register. The value wraps when it autoincrements past the max address value of 0xF. This field change takes effer after being written. The read value indicates the current access address. | back to zer | |

3.3.1.2 VIDEO_DIP_DATA_A–Video Data Island Packet Data for Transcoder A

| V | IDEO_DIP_DATA_A-Video Data Island Packet Data for Transcoder A |
|--------------------|--|
| Register Ty | ype: MMIO |
| Address Of | ffset: E0208h |
| Project: | All |
| Default Val | ue: 0000000h |
| Access: | R/W |
| Size (in bits | s): 32 |
| Bit | Description |
| 31:0 | Video_DIP_DATA Project: All |
| | When read, this returns the current value at the location specified in the Video DIP buffer index select and Video DIP RAM access address fields. The index used to address the RAM is incremented after each read or write of this register. DIP data can be read at any time. Data should be loaded into the RAM before enabling the transmission through the DIP type enable bit. Accesses to this register are on a per-DWORD basis. |

Construction of DIP write:

MSB

LSB



| DW0 | ECC for header (read only, calculated by HW) | Header byte 2 | Header byte 1 | Header byte 0 |
|---|---|------------------|-------------------------------------|--|
| DW1 | Data byte 3 | Data byte 2 | Data byte 1: start of payload | Data byte 0: Checksu m for payload |
| DW8 (read only, calculated by HW) | ECC | | ECC for data bytes 7-13 | ECC for data bytes 0-6 |

3.3.1.3 VIDEO_DIP_GDCP_PAYLOAD_A–Video Data Island Payload for Transcoder A

| VIDE | O_DIP_0 | GDCP_PAYL | OAD_A-Video | Data Island Paylo | oad for T | ransco | oder A |
|--------------|---------------|----------------|--|---|---------------|-----------|-------------|
| Register T | ype: MM | 110 | | | | | |
| Address O | ffset: E02 | 210h | | | | | |
| Project: | All | | | | | | |
| Default Va | lue: 000 |)00000h | | | | | |
| Access: | R/V | V | | | | | |
| Size (in bit | s): 32 | | | | | | |
| Bit | | | I | Description | | | |
| 31:3 | Reserve | d Project: | All | | Format: | MBZ | |
| 2 | Reserve | d_for_GCP_colo | r_indication | | | | |
| | Project: | | All | | | | |
| | Default V | alue: | 0b | | | | |
| | | | in deep color mode. I coder A can receive (| It may optionally be set for GCP data. | r 24-bit mode | e. It mus | t be set if |
| | Value | Name | Description | | | | Project |
| | 0b | Don't Indicate | Don't indicate colo | or depth. CD and PP bits i | n GCP set to | zero | All |
| | 1b | Indicate | | th using CD bits in GCP. I grammed pixel depth in po | | gister | All |



| 1 | | ault_phas | PAYLOAD_A–Video Data Island Payload for Transc | | | | |
|---|---|------------------------------|--|--------------|--|--|--|
| • | Project: | uun_phuo | All | | | | |
| | , | Default Value: 0b | | | | | |
| | Indicates the video timings meet alignment requirements such that the following conditions are met: | | | | | | |
| | | 1) Htotal is an even number | | | | | |
| | | 2) Hactive is an even number | | | | | |
| | | , | | | | | |
| | | | is an even number | | | | |
| | 4 | 4) Front a | and back porches for Hsync are even numbers | | | | |
| | | | always starts on an even-numbered pixel within a line in interlaced mode ng with 0) | es (starting | | | |
| | Value | Name | Description | Project | | | |
| | 0b | Clear | Default phase bit in GCP is cleared | All | | | |
| | 1b | Require I | Met Default phase bit in GCP is set. All requirements must be met before setting this bit | All | | | |
| 0 | GCP_AV | mute | | | | | |
| | Project: | | All | | | | |
| | Default V | alue: | 0b | Ob | | | |
| | Set AV m | ute bit in G | CP | | | | |
| | Value | Name | Description | Project | | | |
| | 0b | Clear | AV mute bit in GCP is cleared. When this bit transitions to 0, the AV mute clear flag is sent in the next GCP packet | All | | | |
| | 1b | Set | AV mute bit in GCP is set. When this bit transitions to 1, the AV mute set flag is sent in the next GCP packet | All | | | |



3.4 Transcoder B Timing

3.4.1.1 TRANS_HTOTAL_B—Transcoder B Horizontal Total Register

| | TRAN | S_HTOTA | L_ B —' | Transcoder B Horizonta | al Total Regi | ister | | | |
|------------------------|--------------------------|----------------|----------------|------------------------|---------------|----------|-----|--|--|
| Register Ty | Register Type: MMIO | | | | | | | | |
| Address Offset: E1000h | | | | | | | | | |
| Project: All | | | | | | | | | |
| Default Val | Default Value: 00000000h | | | | | | | | |
| Access: | R/W | | | | | | | | |
| Size (in bit | s): 32 | | | | | | | | |
| Bit | | | | Description | | | | | |
| 31:29 | Reserved | Project: | All | | Format: | MBZ | | | |
| 28:16 | Transcode | r_B_Horizonta | al_Total | _Display_Clocks | | Project: | All | | |
| | See Transo | oder A descrip | tion. | | | | | | |
| 15:12 | Reserved | Project: | All | | Format: | MBZ | | | |
| 11:0 | Transcode | r_B_Horizonta | al_Active | e_Display_Pixels | | Project: | All | | |
| | See Transo | oder A descrip | tion. | | | | | | |



3.4.1.2 TRANS_HBLANK_B—Transcoder B Horizontal Blank Register

| | TRANS | _HBLANK | E_B —Trans | coder B Horizont | al Blank Reg | jister | |
|-------------|---------------|---------------|-------------------|------------------|--------------|----------|-----|
| Register T | Type: MMIO | | | | | | |
| Address C | Offset: E1004 | h | | | | | |
| Project: | All | | | | | | |
| Default Va | alue: 000000 | 000h | | | | | |
| Access: | R/W | | | | | | |
| Size (in bi | ts): 32 | | | | | | |
| Bit | | | | Description | | | |
| 31:29 | Reserved | Project: | All | | Format: | MBZ | |
| 28:16 | Transcoder | _B_Horizonta | al_Blank_End | | | Project: | All |
| | See Transco | der A descrip | tion. | | | | |
| 15:13 | Reserved | Project: | All | | Format: | MBZ | |
| 12:0 | Transcoder | _B_Horizonta | al_Blank_Start | | | Project: | All |
| | See Transco | der A descrip | tion. | | | | |

3.4.1.3 TRANS_HSYNC_B—Transcoder B Horizontal Sync Register

| | TRAN | S_HSYNC | _B—Transc | oder B Horizonta | al Sync Regi | ster | |
|-------------|---------------|---------------|---------------|------------------|--------------|----------|-----|
| Register T | ype: MMIO | | | | | | |
| Address C | Offset: E1008 | h | | | | | |
| Project: | All | | | | | | |
| Default Va | alue: 00000 | 000h | | | | | |
| Access: | R/W | | | | | | |
| Size (in bi | ts): 32 | | | | | | |
| Bit | | | | Description | | | |
| 31:29 | Reserved | Project: | All | | Format: | MBZ | |
| 28:16 | Transcoder | _B_Horizonta | al_Sync_End | | | Project: | All |
| | See Transco | der A descrip | tion. | | | | |
| 15:13 | Reserved | Project: | All | | Format: | MBZ | |
| 12:0 | Transcoder | B_Horizonta | al_Sync_Start | | | Project: | All |
| | See Transco | der A descrip | tion. | | | | |



3.4.1.4 TRANS_VTOTAL_B—Transcoder B Vertical Total Register

| Register 1 | vpe: MMIO | | | | |
|-------------------|-----------------------|-------------------------|---------|----------|-----|
| Address (| | | | | |
| Project: | All | | | | |
| Default Va | lue: 00000000h | | | | |
| Access: | R/W | | | | |
| Size (in bi | ts): 32 | | | | |
| Bit | | Description | n | | |
| 31:29 | Reserved Project: | All | Format: | MBZ | |
| 28:16 | Transcoder_B_Vertica | al_Total_Display_Lines | | Project: | All |
| | See Transcoder A desc | ription. | | | |
| 15:12 | Reserved Project: | All | Format: | MBZ | |
| 11:0 | Transcoder_B_Vertica | al_Active_Display_Lines | | Project: | All |
| | See Transcoder A desc | ription. | | | |

3.4.1.5 TRANS_VBLANK_B—Transcoder B Vertical Blank Register

| Register 1 | vpe: MMIO | | | |
|-------------------|-------------------------------|-------------|----------|-----|
| Address (| | | | |
| Project: | All | | | |
| Default Va | lue: 0000000h | | | |
| Access: | R/W | | | |
| Size (in bi | ts): 32 | | | |
| Bit | | Description | | |
| 31:29 | Reserved Project: All | Forma | t: MBZ | |
| 28:16 | Transcoder_B_Vertical_Blank | _End | Project: | All |
| | See Transcoder A description. | | | |
| 15:13 | Reserved Project: All | Forma | t: MBZ | |
| 12:0 | Transcoder_B_Vertical_Blank | Start | Project: | All |
| | See Transcoder A description. | | | |



3.4.1.6 TRANS_VSYNC_B—Transcoder B Vertical Sync Register

| | | TRAN | NS_VSYN | C_B—Trar | nscoder B Vertica | I Sync Regist | er | |
|-----------------|------------------|---------|---------------|------------|-------------------|---------------|----------|-----|
| Register T | Гуре: | MMIO | | | | | | |
| Address Offset: | | E1014 | า | | | | | |
| Project: | | All | | | | | | |
| Default Value: | | 000000 |)00h | | | | | |
| Access: | | R/W | | | | | | |
| Size (in bi | ts): | 32 | | | | | | |
| Bit | | | | | Description | | | |
| 31:29 | Rese | erved | Project: | All | | Format: | MBZ | |
| 28:16 | Tran | scoder_ | B_Vertical_ | Sync_End | | | Project: | All |
| | See | Transco | der A descrip | tion. | | | | |
| 15:13 | Rese | erved | Project: | All | | Format: | MBZ | |
| 12:0 | Tran | scoder_ | B_Vertical_ | Sync_Start | | | Project: | All |
| | See ⁻ | Transco | der A descrip | tion. | | | | |

3.4.1.7 TRANS_BCLRPAT_B— Transcoder B Border Color Pattern Register

| Т | RANS_BCLRPAT_B— Transcoder B Border Color | Pattern Register |
|---------------|---|------------------|
| Register Ty | pe: MMIO | |
| Address Of | fset: E1020h | |
| Project: | All | |
| Default Valu | ie: 00000000h | |
| Access: | R/W | |
| Size (in bits |): 32 | |
| See Transco | oder A description. | |
| Bit | Description | |
| 31:24 | Reserved Project: All | Format: |
| 23:16 | Border_Red_Channel_Value | Project: All |
| 15:8 | Border_Green_Channel_Value | Project: All |
| 7:0 | Border_Blue_Channel_Value | Project: All |



3.4.1.8 TRANS_VSYNCSHIFT_B— Transcoder B Vertical Sync Shift Register

| | IRAN5_V5 | INCOHIE | T_B— Transcoder B \ | vertical Sync Shift | Register |
|-------------------|-----------------------|--------------|---------------------------|---------------------|----------|
| Register T | ype: MMIO | | | | |
| Address C | Offset: E1028h | | | | |
| Project: | All | | | | |
| Default Va | lue: 0000000 |)0h | | | |
| Access: | R/W | | | | |
| Size (in bit | t <mark>s):</mark> 32 | | | | |
| Bit | | | Descriptio | n | |
| 31:13 | Reserved | Project: | All | Format: | MBZ |
| 12:0 | Transcoder_E | B_Second_ | Field_Vertical_Sync_Shift | Project: | All |
| | See Transcod | er A descrip | tion. | | |

3.5 Transcoder B M/N Values

3.5.1.1 TransBDataM1— Transcoder B Data M value 1

| | Tra | nsBDa | ataM1— Tran | scoder B Da | ta M value 1 | | |
|--------------------|--------------------|----------|------------------|-------------|--------------|----------|-----|
| Register T | ype: | MMIO | | | | | |
| Address O | ffset: | E1030 | า | | | | |
| Project: | ct: | | | | | | |
| Default Val | lue: | 000000 |)00h | | | | |
| Access: | | R/W | | | | | |
| Size (in bit | s): | 32 | | | | | |
| Double Bu | ffer Update Point: | Start of | f Vblank | | | | |
| Double Bu | ffer Armed By: | Writing | the TransBDPLink | N1 | | | |
| See Transo | coder A descriptio | n | | | | | |
| Bit | | | | Description | | | |
| 31 | Reserved Pr | oject: | All | | Format: | MBZ | |
| 30:25 | TU1_Size | | | | | Project: | All |
| | See Transcoder A | descript | tion. | | | | |
| 24 | Reserved Pr | oject: | All | | Format: | MBZ | |
| 23:0 | Transcoder_B_D | ata_M1_ | value | | | Project: | All |
| | See Transcoder A | descript | tion. | | | | |



3.5.1.2 TransBDataN1— Transcoder B Data N value 1

| Register Type: | MMIO | | | |
|----------------------------------|----------------------------|---------|----------|-----|
| Address Offset: | E1034h | | | |
| Project: | All | | | |
| Default Value: | 0000000h | | | |
| Access: | R/W | | | |
| Size (in bits): | 32 | | | |
| Double Buffer Update Poir | t: Start of Vblank | | | |
| Double Buffer Armed By: | Writing the TransBDPLinkN1 | | | |
| See Transcoder A descrip | ion | | | |
| Bit | Description | | | |
| 31:24 Reserved | Project: All | Format: | MBZ | |
| 23:0 Transcoder_B | _Data_N1_value | | Project: | All |
| See Transcode | A description. | | | |

3.5.1.3 TransBDataM2— Transcoder B Data M value 2

| Register Ty | /pe: | MMIO | | | |
|-----------------------------|--------------------|----------------------------|---------|----------|-----|
| Address Offset: | | E1038h | | | |
| Project: | | All | | | |
| Default Valu | ue: | 00000000h | | | |
| Access: | | R/W | | | |
| Size (in bits | s): | 32 | | | |
| Double Buffer Update Point: | | Start of Vblank | | | |
| Double Buf | fer Armed By: | Writing the TransBDPLinkN2 | | | |
| See Transc | oder A description | | | | |
| Bit | | Descri | ption | | |
| 31 | Reserved Pro | iect: All | Format: | MBZ | |
| 30:25 | TU2_Size | | | Project: | All |
| | See Transcoder A d | lescription. | | | |
| 24 | Reserved Pro | iect: All | Format: | MBZ | |
| 23:0 | Transcoder_B_Dat | a_M2_value | | Project: | All |
| | See Transcoder A d | lescription. | | | |



3.5.1.4 TransBDataN2— Transcoder B Data N value 2

| Register Type: | MMIO | | | |
|-----------------------|--------------------------------|----------|----------|-----|
| Address Offset: | E103Ch | | | |
| Project: | All | | | |
| Default Value: | 0000000h | | | |
| Access: | R/W | | | |
| Size (in bits): | 32 | | | |
| Double Buffer Update | Point: Start of Vblank | | | |
| Double Buffer Armed I | By: Writing the TransBDPLinkN2 | | | |
| See Transcoder A des | cription | | | |
| Bit | Des | cription | | |
| 31:24 Reserved | Project: All | Format: | MBZ | |
| 23:0 Transcode | r_B_Data_N2_value | | Project: | All |
| See Transo | oder A description. | | | |

3.5.1.5 TransBDPLinkM1— Transcoder B Link M value 1

| Tra | nsBDPLinkM1— Tr | anscoder B Link | M value 1 | | |
|-----------------------------------|----------------------|-----------------|-----------|----------|-----|
| Register Type: | MMIO | | | | |
| Address Offset: | E1040h | | | | |
| Project: | All | | | | |
| Default Value: | 0000000h | | | | |
| Access: | R/W | | | | |
| Size (in bits): | 32 | | | | |
| Double Buffer Update Point | Start of Vblank | | | | |
| Double Buffer Armed By: | Writing the TransBDF | PLinkN1 | | | |
| See Transcoder A descript | on | | | | |
| Bit | | Description | | | |
| 31:24 Reserved | Project: All | | Format: | MBZ | |
| 23:0 Transcoder_B_ | Link_M1_value | | | Project: | All |
| See Transcoder | A description. | | | | |



3.5.1.6 TransBDPLinkN1— Transcoder B Link N value 1

| | ransBDPLinkN1— Transcod | | | |
|-----------------------------------|----------------------------|---------|----------|-----|
| Register Type: Address Offset: | E1044h | | | |
| | All | | | |
| Project: Default Value: | 00000000h | | | |
| Access: | R/W | | | |
| Size (in bits): | 32 | | | |
| Double Buffer Update Po | nt: Start of Vblank | | | |
| Double Buffer Armed By: | Writing the TransBDPLinkN1 | | | |
| See Transcoder A descri | otion | | | |
| Bit | Descri | otion | | |
| 31:24 Reserved | Project: All | Format: | MBZ | |
| 23:0 Transcoder_l | 3_Link_N1_value | | Project: | All |
| See Transcod | er A description. | | | |

3.5.1.7 TransBDPLinkM2— Transcoder B Link M value 2

| Register Type: | MMIO | | | |
|------------------------------|--------------------------|------------|----------|-----|
| Address Offset: | E1048h | | | |
| Project: | All | | | |
| Default Value: | 0000000h | | | |
| Access: | R/W | | | |
| Size (in bits): | 32 | | | |
| Double Buffer Update Point: | Start of Vblank | | | |
| Double Buffer Armed By: | Writing the TransBDPLink | N2 | | |
| See Transcoder A description | n | | | |
| Bit | De | escription | | |
| 31:24 Reserved F | roject: All | Format | MBZ | |
| 23:0 Transcoder_B_I | .ink_M2_value | | Project: | All |
| See Transcoder | A description. | | | |



3.5.1.8 TransBDPLinkN2— Transcoder B Link N value 2

| Register Type: | MMIO | | | |
|--------------------------|----------------------------|---------|----------|-----|
| Address Offset: | E104Ch | | | |
| Project: | All | | | |
| Default Value: | 0000000h | | | |
| Access: | R/W | | | |
| Size (in bits): | 32 | | | |
| Double Buffer Update Poi | t: Star of Vblank | | | |
| Double Buffer Armed By: | Writing the TransBDPLinkN2 | | | |
| See Transcoder A descri | tion | | | |
| Bit | Descrip | tion | | |
| 31:24 Reserved | Project: All | Format: | MBZ | |
| 23:0 Transcoder_E | _Link_N2_value | | Project: | All |
| See Transcod | r A description. | | | |



3.6 Transcoder B Video DIP

3.6.1.1 VIDEO_DIP_CTL_B—Video DIP Control for Transcoder B

| | See Transcoder A description. | | | | | | | |
|-------------------------|---|---------------|----------|-------|--|--|--|--|
| 3:0 | Video_DIP_RAM_access_address | | Project: | All | | | | |
| 7:4 | Reserved Project: All | Format: | MBZ | | | | | |
| | See Transcoder A description. | | | | | | | |
| | Default Value: 0b | | | | | | | |
| | Access: Read Only | | | | | | | |
| | Project: All | | | | | | | |
| 11:8 | Video_DIP_buffer_size | | | | | | | |
| 15:12 | | Format: | MBZ | | | | | |
| 45.40 | See Transcoder A description. | F | MD7 | | | | | |
| 17:16 | Video_DIP_transmission_frequency | | Project: | All | | | | |
| 18 | ······································ | Format: | | • · · | | | | |
| 10 | See Transcoder A description. | | | | | | | |
| 20:19 | DIP_buffer_index | | Project: | All | | | | |
| | See Transcoder A description. | | | | | | | |
| 24:21 | Data_Island_Packet_type_enable | | Project: | All | | | | |
| | This bit shoud not be enabled for 8bpc mode if at least one of the other HD mode. | ivii ports is | | | | | | |
| | See Transcoder A description. | | | | | | | |
| 25 | GCP_DIP_enable | | Project: | All | | | | |
| 28:26 | | Format: | | | | | | |
| | See Transcoder A description. | | | | | | | |
| 30:29 | Port_Select | | Project: | All | | | | |
| | See Transcoder A description. | | | | | | | |
| 31 | Enable_Graphics_Data_Island_Packet | | Project: | All | | | | |
| Bit | Description | | | | | | | |
| | coder A description. | | | | | | | |
| Size (in bit | | | | | | | | |
| Access: | R/W | | | | | | | |
| Project: Default Val | | | | | | | | |
| Address O | ffset: E1200h All | | | | | | | |
| Register T | | | | | | | | |
| | VIDEO_DIP_CTL_B—Video DIP Control for Trans | 00000 | _ | | | | | |



3.6.1.2 VIDEO_DIP_DATA_B-Video Data Island Packet Data for Transcoder B

| V | IDEO | _DIP_DATA | _B-Video | Data | Island Packet Data for Transcoder B |
|--------------------|------------------|-------------------|-----------|------|-------------------------------------|
| Register Ty | /pe: | MMIO | | | |
| Address Of | ffset: | E1208h | | | |
| Project: | | All | | | |
| Default Val | ue: | 0000000h | | | |
| Access: | | R/W | | | |
| Size (in bits | s): | 32 | | | |
| Bit | | | | | Description |
| 31:0 | Vide | DIP_DATA | Project: | All | Format: |
| | See ⁻ | Franscoder A dese | cription. | | |

3.6.1.3 VIDEO_DIP_GDCP_PAYLOAD_B-Video Data Island Payload for Transcoder B

| VIDE | D_DIP_GDCP_PAYLOAD_B-Video Data Island Payload for | Transcoo | der B |
|--------------------|--|----------|-------|
| Register Ty | ype: MMIO | | |
| Address O | ffset: E1210h | | |
| Project: | All | | |
| Default Val | ue: 0000000h | | |
| Access: | R/W | | |
| Size (in bit | s): 32 | | |
| Bit | Description | | |
| 31:3 | Reserved Project: All Format: | MBZ | |
| 2 | Reserved_for_GCP_color_indication | Project: | All |
| | See Transcoder A description. | | |
| 1 | GCP_default_phase_enable | Project: | All |
| | See Transcoder A description. | | |
| 0 | GCP_AV_mute | Project: | All |
| | See Transcoder A description. | | |



3.7 **CRT DAC**

3.7.1.1 ADP—Analog Display Port Control Register (CRT DAC)

| | A | P-Analog | Display Port Control Register (CRT DAC) | | |
|--|--|--|---|---------|--|
| Register T Address C Project: Default Va Access: Size (in bi Bit 31 | ype: MMI Dffset: E110 All Nue: 0004 R/W ts): 32 Analog_D Project: Default Va | O D0h 40000h isplay-Port_Enal A lue: 0l | Description ble | | |
| | | | ne analog port CRT DAC and syncs outputs. escription Project | | |
| | 0b | | Description Disable the analog port DAC and disable output of syncs | All | |
| | 1b | | Enable the analog port DAC and enable output of syncs | All | |
| 30 | Transcode Project: Default Va Determine: | A lue: 0l | | | |
| | Value | Name | Description | Project | |
| | 0b | Transcoder A | Transcoder A | All | |
| | 1b | Transcoder B | Transcoder B | All | |
| 29:26 | Reserved | Project: | All Format: | | |



| | AL | OP—Analog I | Display Port Control Register (CRT DA | AC) | | | |
|------|---|--|--|---|--|--|--|
| 5:24 | | Plug_Detection_ | | | | | |
| | Project: | AI | | | | | |
| | Access: Read Only | | | | | | |
| | Default Value: 00b These bits are set when a CRT hot plug or unplug event has been detected and indicate which color | | | | | | |
| | channels v | were attached. Wi | RT not plug of unplug event has been detected and in rite a one to these bits to clear the status. The rising o r to go to the main ISR CRT hot plug register bit. | dicate which color or falling edges of | | | |
| | Value | Name | Description | Project | | | |
| | 00b | None | No channels attached | All | | | |
| | 01b | Blue | Blue channel only is attached | All | | | |
| | 10b | Green | Green channel only is attached | All | | | |
| | 11b | Both | Both blue and green channel attached | All | | | |
| 23 | CRT_Hot_ | Plug_Detection_ | Enable | | | | |
| | Project: | AI | 1 | | | | |
| | Default Va | ilue: Ot |) | | | | |
| | Hot plug detection is used to set status bits or an interrupt on the connection or disconnection of a CRT to the analog display port. | | | | | | |
| | | | | | | | |
| | Value | Name | Description | Project | | | |
| | Value Ob | Name Disable | Description CRT hot plug detection is disabled | Project All | | | |
| | | | - | - | | | |
| 22 | 0b 1b | Disable | CRT hot plug detection is disabled CRT hot plug detection is enabled | All | | | |
| 22 | 0b 1b | Disable Enable | CRT hot plug detection is disabled CRT hot plug detection is enabled tivation_Period | All | | | |
| 22 | 0b 1b CRT_Hot_ | Disable Enable Plug_Circuit_Ac | CRT hot plug detection is disabled CRT hot plug detection is enabled tivation_Period | All | | | |
| 22 | 0b 1b CRT_Hot Project: Default Va | Disable Enable Plug_Circuit_Ac Al Ilue: 0t | CRT hot plug detection is disabled CRT hot plug detection is enabled tivation_Period | All | | | |
| 22 | 0b 1b CRT_Hot Project: Default Va | Disable Enable Plug_Circuit_Ac Al Ilue: 0t | CRT hot plug detection is disabled CRT hot plug detection is enabled tivation_Period | All | | | |
| 22 | 0b 1b CRT_Hot_ Project: Default Va This bit se | Disable Enable Plug_Circuit_Ac Al Ilue: Ob ts the activation pe | CRT hot plug detection is disabled CRT hot plug detection is enabled tivation_Period | All | | | |
| 22 | 0b 1b CRT_Hot_ Project: Default Va This bit se Value | Disable Enable Plug_Circuit_Ac Al Ilue: 0t ts the activation per | CRT hot plug detection is disabled CRT hot plug detection is enabled tivation_Period | All All Project | | | |
| | 0b1bCRT_HotProject:Default VaThis bit seValue0b1b | Disable Enable Plug_Circuit_Ac Alulue: Ot ts the activation per Name 64 cdclk | CRT hot plug detection is disabled CRT hot plug detection is enabled tivation_Period I o eriod for the CRT hot plug circuit. Description 64 cdclk periods 128 cdclk periods | All | | | |
| | 0b1bCRT_HotProject:Default VaThis bit seValue0b1b | Disable Enable Plug_Circuit_Ac Al Ilue: 0k ts the activation pe 64 cdclk 128 cdclk | CRT hot plug detection is disabled CRT hot plug detection is enabled tivation_Period b eriod for the CRT hot plug circuit. Description 64 cdclk periods 128 cdclk periods trmup_Time | All | | | |
| | 0b1bCRT_HotProject:Default VaThis bit seValue0b1bCRT_Hot | Disable Disable Enable Enable IPlug_Circuit_Ac Al Iue: 0t ts the activation pe 64 cdclk 128 cdclk Plug_Detect_Wa Al | CRT hot plug detection is disabled CRT hot plug detection is enabled tivation_Period I o eriod for the CRT hot plug circuit. Description 64 cdclk periods 128 cdclk periods irmup_Time | All | | | |
| | 0b1bCRT_Hot_Project:Default VaThis bit seValue0b1bCRT_Hot_Project:Default Va | Disable Enable Enable Plug_Circuit_Ac Al Iue: 0t ts the activation pe 64 cdclk 128 cdclk 128 cdclk Plug_Detect_Wa Al Iue: 0t | CRT hot plug detection is disabled CRT hot plug detection is enabled tivation_Period I o eriod for the CRT hot plug circuit. Description 64 cdclk periods 128 cdclk periods irmup_Time | All | | | |
| | 0b1bCRT_Hot_Project:Default VaThis bit seValue0b1bCRT_Hot_Project:Default Va | Disable Enable Enable Plug_Circuit_Ac Al Iue: 0t ts the activation pe 64 cdclk 128 cdclk 128 cdclk Plug_Detect_Wa Al Iue: 0t | CRT hot plug detection is disabled CRT hot plug detection is enabled tivation_Period I Description 64 cdclk periods 128 cdclk periods | All | | | |
| 22 | 0b1bCRT_Hot_Project:Default VaThis bit seValue0b1bCRT_Hot_Project:Default VaThis bit se | Disable Enable Plug_Circuit_Ac Al Ilue: 0t ts the activation per 64 cdclk 128 cdclk 128 cdclk Plug_Detect_Wa Al Ilue: 0t ts the warmup tim | CRT hot plug detection is disabled CRT hot plug detection is enabled tivation_Period b criod for the CRT hot plug circuit. Description 64 cdclk periods 128 cdclk periods trmup_Time c e for the CRT hot plug circuit. | All All Project All All | | | |



| 20 | - | DP—Analog [_Plug_Detect_Sar | nnling Period | - | | |
|-------|--|---------------------------------|---|-------------------|--|--|
| 20 | Project: | _i lug_betect_oai All | | | | |
| | Default Va | | | | | |
| | This bit de | etermines the length | n of time between sampling periods when the transc | oder is disabled. | | |
| | Value | Name | Description | Project | | |
| | 0b | 1G pcdclks | 1G pcdclks (approximately 2 seconds) | All | | |
| | 1b | 2G pcdclks | 2G pcdclks (approximately 4 seconds) | All | | |
| 19:18 | CRT_Hot | _Plug_Voltage_Co | ompare_Value | | | |
| | Project: | All | | | | |
| | Default Va | alue: 01 | b 50 | | | |
| | Compare | value for Vref to de | termine whether the analog port is connected to a C | CRT. | | |
| | Value | Name | Description | Project | | |
| | 00b | 40 | 40 | All | | |
| | 01b | 50 | 50 (Default) | All | | |
| | 10b | 60 | 60 | All | | |
| | 11b | 70 | 70 (bit 17 must be = 1) | All | | |
| 17 | CPT Hot | _Plug_Reference_ | Voltago | | | |
| 17 | Project: | | - | | | |
| | Default Va | | | | | |
| | Value | Name | Description | Project | | |
| | 0b | 325mv | 325mv | All | | |
| | 1b | 475mv | 475mv (bits 19:18 must be = 11) | All | | |
| 16 | Force CR | RT_Hot_Plug_Dete | ect Trigger | | | |
| | Project: | All | | | | |
| | Default Value: 0b | | | | | |
| | Triggers a CRT hotplug/unplug detection cycle independent of the hot plug detection enable bit. This bit is automatically cleared after the detection is completed. The result of this trigger is reflected in the CRT Hot Plug Detection Status. Software must reset status after a force CRT detect trigger. | | | | | |
| | Value | Name | Description | Project | | |
| | 0b | No Trigger | No Trigger | All | | |
| | 1b | Force Trigger | Force Trigger | All | | |
| 45.5 | | | | | | |
| 15:5 | Reserved | Project: | All Forma | al. | | |



| 4 | VSYNC P | olarity_Control | | | |
|---|--|--|--|------------|--|
| | Project: | - | All | | |
| | Default Val | lue: | ОЬ | | |
| | The output VSYNC polarity is controlled by this bit. This is used to implement display modes that require inverted polarity syncs and to set the disabled state of the VSYNC signal. | | | | |
| | Value | Name | Description | Project | |
| | 0b | Low | Active Low | All | |
| | 1b | High | Active High | All | |
| | | | All | | |
| | Project: Default Val | | ОЬ | | |
| | Default Val | lue: HSYNC polarit | 0b y is controlled by this bit. This is used to imp ncs and to set the disabled state of the HSY | | |
| | Default Val | lue: HSYNC polarit | y is controlled by this bit. This is used to imp | | |
| | Default Val The output require inv | lue: HSYNC polarit erted polarity sy | y is controlled by this bit. This is used to imp ncs and to set the disabled state of the HSY | NC signal. | |



3.8 HDMI port C

3.8.1.1 HDMIC—Digital Display Port C Register

| | | н | IDMIC—Digital Display Port C Register | | | | |
|--|---|---------------|---|-----------|--|--|--|
| Register Ty | /pe: | | MMIO | | | | |
| Address O | ffset: | | E1150h | | | | |
| Project: | | | All | | | | |
| Default Val | ue: | | 0000018h | | | | |
| Access: | Access: | | R/W | | | | |
| Size (in bits): | | | 32 | | | | |
| Double But | Double Buffer Update Point: | | Depends on bit | | | | |
| Bit | | | Description | | | | |
| 31 | HDMIC_ | Enable(Dig | jital_Display_Port_C_Enable) | | | | |
| | Project: | | All | | | | |
| | Default Value: 0b | | | | | | |
| being written. Bo | | | vill put it in its lowest power state. Port enable takes place on the Vblank this bit and bit 6 of this register must be enabled to send audio over this p ort must not be enabled simultaneously with DisplayPort C. | | | | |
| | #30) clea | ared to '0' a | abling the port, software must temporarily enable the port with transcoder fter disabling the port. This is workaround for hardware issue where the porevent DPC from being enabled on transcoder A. | | | | |
| | [DevIBX] Software must write this bit twice when enabling the port (setting to '1') as a workaround for hardware issue that may result in first write getting masked. | | | | | | |
| [DevIBX] Toggle thi color with pixel repe | | | s bit off then on at the end of mode set sequence when enabling HDMI 12 at. | 2-bit per | | | |
| | Value | Name | Description | Project | | | |
| | 0b | Disable | Disable and tristates the Digital Display Port C interface for HDMI or DVI modes. | All | | | |
| | 1b | Enable | Enable. This bit enables the Digital Display Port C interface for HDMI or DVI modes. | All | | | |



| | | HDMIC- | -Digital Display Port C Register | | | | |
|-------|------------------------|----------------------------------|--|---------|--|--|--|
| 30 | Transcoo | der_Select | | | | | |
| | Project: | All | | | | | |
| | Default V | alue: 0b | | | | | |
| | See HDMIB Description. | | | | | | |
| | that this b | | ly takes effect when port is enabled. Due to hardware issu port is disabled. To clear this bit software must temporarily | | | | |
| | Value | Name | Description | Project | | | |
| | 0b | Transcoder A | Transcoder A | All | | | |
| | 1b | Transcoder B | Transcoder B | All | | | |
| 29 | Reserved | d Project: A | All Format: | MBZ | | | |
| 28:26 | Color_Fo | ormat | | | | | |
| | Project: All | | | | | | |
| | Default Value: 0b | | | | | | |
| | See HDMIB Description. | | | | | | |
| | Value | Name | Description | Project | | | |
| | 000b | 8 bpc | 8 bits per color | All | | | |
| | 011b | 12 bpc | 12 bits per color | All | | | |
| | others | Reserved | Reserved | All | | | |
| 25:19 | Reserved | d Project: A | All Format: | | | | |
| 18 | Clock_O | Clock_Output_Inversion(testmode) | | | | | |
| | Project: | All | | | | | |
| | Security: | Tes | st | | | | |
| | Default Value: 0b | | | | | | |
| | See HDMIB Description. | | | | | | |
| | Value | Name | Description | Project | | | |
| | 0b | Not Inverted | Clock output is NOT inverted | All | | | |
| | 1b | Inverted | Clock output is inverted | All | | | |
| | | | | | | | |



| 15 | Port_Lar | ne_Reversa | ıl | | | | | |
|-------|------------------------|-------------------|---|-----------------------------|---------|--|--|--|
| | Project: All | | | | | | | |
| | Default V | alue: | 0b | | | | | |
| | See HDMIB Description. | | | | | | | |
| | Value Name | | | Description | Project | | | |
| | 0b | Not revers | sed | Not reversed | All | | | |
| | 1b | Reversed | | Reversed | All | | | |
| 14:10 | Reserved | d Proje | ect: A | II Format: MBZ | | | | |
| 9 | Null_pac | kets_enab | led_durir | ng_Vsync | | | | |
| | Project: | | All | | | | | |
| | Default V | Default Value: 0b | | | | | | |
| | See HDMIB Description. | | | | | | | |
| | Value | Name | Descri | ption | Project | | | |
| | 0b | Disable | able Disable null infoframe packets when Vsync=1 on this port. | | All | | | |
| | 1b | Enable | Enable Enable null infoframe packets when Vsync=1 on this port. | | | | | |
| 8:7 | Reserved | d Proje | ect: A | II Format: MBZ | | | | |
| 6 | Audio_Output_Enable | | | | | | | |
| | Project: All | | | | | | | |
| | Default Value: 0b | | | | | | | |
| | See HDMIB Description. | | | | | | | |
| | Value | Name | Desc | ription | Projec | | | |
| | 0b | Disable | No a | udio output on this port | All | | | |
| | 1b | Enable | Enab | le audio on this port | All | | | |
| 5 | HDCP_Port_Select | | | | | | | |
| | Project: | | All | | | | | |
| | Default Value: 0b | | | | | | | |
| | See HDM | 1IB Descript | ion. | | | | | |
| | | | | ription | Projec | | | |
| | Value | Name | Desc | | FIUJEC | | | |
| | Value 0b | Name Disable | | DCP encryption on this port | All | | | |



| 4:3 | Sync_Pol | | | gital Display Port C Register | | | | | |
|-----|-------------------------|---|--------|--|---------|--|--|--|--|
| 4.5 | Project: | • | Л | | | | | | |
| | Default Va | - | 1b | VS and HS are active high | | | | | |
| | See HDMIB Description. | | | | | | | | |
| | Value | Name | | Description | Project | | | | |
| | 00b | VS-HS Low | | VS and HS are active low (inverted) | All | | | | |
| | 01b | VS Low, HS H | ligh | VS is active low (inverted), HS is active high | All | | | | |
| | 10b | Vs High, HS L | .ow | VS is active high, HS is active low (inverted) | All | | | | |
| | 11b | High | | VS and HS are active high (Default) | All | | | | |
| 2 | Digital_Port_C_Detected | | | | | | | | |
| | Project: | All | | | | | | | |
| | Access: Read Only | | | | | | | | |
| | Default Value: 0b | | | | | | | | |
| | | Read-only bit indicating whether a digital port C was detected during initialization. It signifies the level of the GMBUS port 3 (port C) data line at boot. This bit is valid regardless of whether the port is enabled. | | | | | | | |
| | Value | Name | Desc | ription | Proje | | | | |
| | 0b | Not Detected | Digita | I Port C not detected during initialization | All | | | | |
| | | | Digita | I Port C detected during initialization | All | | | | |
| | 1b | Detected | Digita | | All | | | | |



3.9 HDMI port D

3.9.1 HDMID—Digital Display Port D Register

| | | Н | IDMID—Digital Display Port D Register | | | | | |
|-----------------------------|---|------------|--|---------|--|--|--|--|
| Register Ty | ype: | | MMIO | | | | | |
| Address O | ffset: | | E1160h | | | | | |
| Project: | | | All | | | | | |
| Default Val | ue: | | 0000018h | | | | | |
| Access: | | | R/W | | | | | |
| Size (in bit | s): | | 32 | | | | | |
| Double Buffer Update Point: | | | Depends on bit | | | | | |
| Bit | | | Description | | | | | |
| 31 | HDMID_ | Enable(Dig | jital_Display_Port_D_Enable) | | | | | |
| | Project: | | All | All | | | | |
| | Default Value: 0b | | | | | | | |
| | being written. Both this bit and bit 6 of this register must be enabled to send audio over this port in HDMI mode. This port must not be enabled simultaneously with DisplayPort D. [DevIBX] When disabling the port, software must temporarily enable the port with transcoder select (bit #30) cleared to '0' after disabling the port. This is workaround for hardware issue where the transcoder | | | | | | | |
| | select set to '1' will prevent DPD from being enabled on transcoder A. | | | | | | | |
| | [DevIBX] Software must write this bit twice when enabling the port (setting to '1') as a workaround for hardware issue that may result in first write getting masked. | | | | | | | |
| | [DevIBX] Toggle this bit off then on at the end of mode set sequence when enabling HDMI 12-bit per color with pixel repeat. | | | | | | | |
| | Value | Name | Description | Project | | | | |
| | 0b | Disable | Disable and tristates the Digital Display Port D interface for HDMI or DVI modes. | All | | | | |
| | 1b | Enable | Enable. This bit enables the Digital Display Port D interface for HDMI or DVI modes. | All | | | | |



| | | HDMID | —Digital Display Port D Regis | ter | | | |
|-------|----------------------------------|------------------|---|-------------|-----|--|--|
| 30 | Transcoder_Select | | | | | | |
| | Project: | А | II | | | | |
| | Default V | alue: 01 | b | | | | |
| | See HDM | IC Description. | | | | | |
| | that this b | | only takes effect when port is enabled. Due n port is disabled. To clear this bit software | | | | |
| | Value | Name | Description | Proje | ect | | |
| | 0b | Transcoder A | Transcoder A | All | | | |
| | 1b | Transcoder B | Transcoder B | All | | | |
| 29 | Reserved | d Project: | All | Format: MBZ | | | |
| 28:26 | Color_Format | | | | | | |
| | Project: All | | | | | | |
| | Default Value: 0b | | | | | | |
| | See HDMIC Description. | | | | | | |
| | Value | Name | Description | Proje | ect | | |
| | 000b | 8 bpc | 8 bits per color | All | | | |
| | 011b | 12 bpc | 12 bits per color | All | | | |
| | others | Reserved | Reserved | All | | | |
| 25:19 | Reserved | d Project: | All | Format: | | | |
| 18 | Clock_Output_Inversion(testmode) | | | | | | |
| | Project: | A | II | | | | |
| | Security: | T | est | | | | |
| | Default V | alue: 01 | b | | | | |
| | See HDN | AIC Description. | | | | | |
| | Value | Name | Description | Proje | ect | | |
| | 0b | Not Inverted | Clock output is NOT inverted | All | | | |
| | 1b | Inverted | Clock output is inverted | All | | | |
| | 10 | | | | | | |



| 15 | Port Lar | | | -Digital Display Port D Register | | | |
|-------|---------------------------------|---|------------------|---|---------|--|--|
| 15 | Port_Lane_Reversal Project: All | | | | | | |
| | Project: Default V | alue. | Ob | | | | |
| | | /IC Descrip | | | | | |
| | Value | Name | | Description | Project | | |
| | 0b | Not revers | sed | Not reversed | All | | |
| | 1b | Reversed | | Reversed | All | | |
| 14:10 | Reserved | | | I VII Format: MBZ | | | |
| | | | | | | | |
| 9 | Project: | kets_enab | ied_durir All | lg_vsync | | | |
| | Default V | alue. | 0b | | | | |
| | See HDMIC Description. | | | | | | |
| | Value | Name | Descrip | otion | Project | | |
| | 0b | Disable | - | null infoframe packets when Vsync=1 on this port. | All | | |
| | 1b | Enable Enable null infoframe packets when Vsync=1 on this port. | | | | | |
| 8:7 | Reserved | d Proje | ect: A | II Format: MBZ | • | | |
| 6 | Audio_Output_Enable | | | | | | |
| | Project: All | | | | | | |
| | Default Value: 0b | | | | | | |
| | See HDMIC Description. | | | | | | |
| | Value | Name | Desc | ription | Projec | | |
| | 0b | Disable | No au | udio output on this port | All | | |
| | 1b | Enable | Enab | le audio on this port | All | | |
| 5 | HDCP_P | ort_Select | | | | | |
| | Project: | | All | | | | |
| | Default Value: 0b | | | | | | |
| | See HDM | IIC Descript | tion. | | | | |
| | Value | Name | Desc | ription | Projec | | |
| | Value | | 1 | | | | |
| | 0b | Disable | No H | DCP encryption on this port | All | | |



| | | HDMID |)—Di | gital Display Port D Register | | | | | |
|-----|---|---------------|--------|--|---------|--|--|--|--|
| 4:3 | Sync_Polarity | | | | | | | | |
| | Project: | A | JI | | | | | | |
| | Default Va | ilue: 1 | 1b | VS and HS are active high | | | | | |
| | See HDMIC Description. | | | | | | | | |
| | Value | Name | | Description | Project | | | | |
| | 00b | VS-HS Low | | VS and HS are active low (inverted) | All | | | | |
| | 01b | VS Low, HS H | ligh | VS is active low (inverted), HS is active high | All | | | | |
| | 10b | Vs High, HS L | .ow | VS is active high, HS is active low (inverted) | All | | | | |
| | 11b | High | | VS and HS are active high (Default) | All | | | | |
| 2 | Digital_Port_D_Detected | | | | | | | | |
| | Project: | All | | | | | | | |
| | Access: Read Only | | | | | | | | |
| | Default Value: 0b | | | | | | | | |
| | Read-only bit indicating whether a digital port D was detected during initialization. It signifies the level of the GMBUS port 5 (port D) data line at boot. This bit is valid regardless of whether the port is enabled. | | | | | | | | |
| | Value | Name | Desc | ription | Project | | | | |
| | 0b | Not Detected | Digita | al Port D not detected during initialization | All | | | | |
| | 1b | Detected | Digita | al Port D detected during initialization | All | | | | |
| 1:0 | Reserved | Project: | All | Format: MB | Z | | | | |



3.10 LVDS

3.10.1.1 LVDS—LVDS Port Control Register

| | | | LVDS- | -LVDS Port Control Register | | | | |
|--------------------|-----------------------------|---|---|--|---------|--|--|--|
| Register Ty | pe: MN | /IO | | | | | | |
| Address Of | - | 180h | | | | | | |
| Project: | All | | | | | | | |
| Default Val | ue: 400 | 00000h | | | | | | |
| Access: | R/V | V Protect | | | | | | |
| Size (in bits | s): 32 | | | | | | | |
| Write Prote | ct by Pan | el Power | Sequence | er | | | | |
| Bit | | | | Description | | | | |
| 31 | LVDS_P | LVDS_Port_Enable | | | | | | |
| | Project: | | | | | | | |
| | Default V | Default Value: 0b | | | | | | |
| | the way t | When disabled the LVDS port is inactive and in it's low power state. Enabling the LVDS port changes the way that the PLL for this transcoder is programmed. This bit must be set before the display PLL is enabled and the port is power sequenced on using the panel power sequencing logic. | | | | | | |
| | Value | Name | Descript | Project | | | | |
| | 0b | Disable | The port | is disabled and all LVDS pairs are powered down. | All | | | |
| | 1b | Enable | The port is enabled (port must be enabled before powering up a All connected panel) | | | | | |
| 30 | LVDS_Port_Transcoder_Select | | | | | | | |
| | Project: | | All | | | | | |
| | Default V | alue: | 1b | Transcoder B | | | | |
| | Value | Name | | Description | Project | | | |
| | 0b | Transco | der A | The port gets data from Transcoder A | All | | | |
| | 1b | Transco | der B | The port gets data from Transcoder B | All | | | |
| 29:25 | Reserve | d Pro | ject: A | II Format: | | | | |



| | | L | VDS—LVDS Port | Control Register | | | | | |
|----|---|----------------|-----------------------------|----------------------------------|----------------|--|--|--|--|
| 24 | Data_Format_Select | | | | | | | | |
| | Project: | | All | | | | | | |
| | Default Va | alue: | 0b | | | | | | |
| | Combined with the other control bits it selects the LVDS data format. Other control bits in this register determine if two channel is enabled and 18 or 24 bit color is enabled. | | | | | | | | |
| | Value | Name | | Description | Project | | | | |
| | 0b | 1x18.0, 2x1 | 8.0, 1x24.0 or 2x24.0 | 1x18.0, 2x18.0, 1x24.0 or 2x24.0 | All | | | | |
| | 1b | 1x24.1 or 2x | (24.1 | 1x24.1 or 2x24.1 | All | | | | |
| 23 | LE_Cont | rol_Enable | | | | | | | |
| | Project: | | All | | | | | | |
| | Default Va | alue: | 0b | | | | | | |
| | This bit is used when the second channel control signal field indicates that we are using the LE instead of HS and the two channel mode is enabled. In single channel mode, this bit has no effect. | | | | | | | | |
| | Value | Name | Description | Project | | | | | |
| | 0b | Send 0 | Send 0 on second cha | All | | | | | |
| | 1b | Send 1 | Send 1 on second cha | nnel HS | All | | | | |
| 22 | LF_Control_Enable | | | | | | | | |
| | Project: All | | | | | | | | |
| | Default Value: 0b | | | | | | | | |
| | This bit is used when the second channel control signal field indicates that we are using the LF instead of VS and two channel mode is enabled. In single channel mode, this bit has no effect. | | | | | | | | |
| | Value | Name | Description | | Project | | | | |
| | 0b | Send 0 | Send 0 on second cha | annel VS (B2<3>) | All | | | | |
| | 1b | Send 1 | Send 1 on second cha | nnel VS | All | | | | |
| 21 | VSYNC_I | Polarity | | | | | | | |
| | Project: | | All | | | | | | |
| | Default Va | alue: | 0b | | | | | | |
| | This controls the polarity of the VSYNC indicator that is sent over the LVDS connection. Panels may require one or the other polarity or work with either polarity. | | | | | | | | |
| | | | | her polarity. | | | | | |
| | | | | her polarity. | Project | | | | |
| | require or | ne or the othe | r polarity or work with eit | · · · | Project All | | | | |



| 20 | HEVNC | LVDS—LVDS Port Control Register HSYNC_Polarity(LP_Invert) | | | | | | |
|-------|--|---|--|---|-------------------------------------|--|--|--|
| 20 | | | | | | | | |
| | - | Project: All Default Value: 0b | | | | | | |
| | This controls the polarity of the HSYNC indicator that is sent over the LVDS connection. Panels may require one or the other polarity or work with either polarity. | | | | | | | |
| | Value | Name | Des | scription | Project | | | |
| | 0b | No Invert | No | inversion (1=active) | All | | | |
| | 1b | Invert | Inve | ert the sense (0=active) | All | | | |
| 19 | DE_Invert Project: All Default Value: 0b This controls the polarity of the DE indicator that is sent over the LVDS connection. | | | | | | | |
| | Value | Name | Des | Description | | | | |
| | 0b | No Invert No | | inversion of DE (1=active) | All | | | |
| | 1b | Invert Inver | | ert the sense of DE (0=active) | All | | | |
| 18:17 | Second_Channel_Control_Signals Project: All Default Value: 00b This bit only applies to the two channel modes of operation it has no effect in single channel modes. | | | | | | | |
| | Default V | | | | nodes. | | | |
| | Default V | | | vo channel modes of operation it has no effect in single channel n | 1 | | | |
| | Default V This bit o | nly applies to | | | nodes. Project All | | | |
| | Default V This bit o Value | nly applies to | | vo channel modes of operation it has no effect in single channel n Description | Project | | | |
| | Default V This bit o Value 00b | nly applies to | | vo channel modes of operation it has no effect in single channel n Description Send DE, HS, VS on second channel if enabled | Project | | | |
| | Default V This bit o Value 00b 01b | nly applies to | | vo channel modes of operation it has no effect in single channel n Description Send DE, HS, VS on second channel if enabled Reserved | Project All All | | | |
| 16 | Default V This bit o Value 00b 01b 10b 11b | Name Reserved Reserved | the tw | vo channel modes of operation it has no effect in single channel n Description Send DE, HS, VS on second channel if enabled Reserved Do not send DE, HS, VS on second channel use zero instead Use DE=0, HS=LE, VS=LF on second channel I | Project All All All | | | |
| 16 | Default V This bit o Value 00b 01b 10b 11b Channel Project: | Name Reserved Reserved | the two second s | vo channel modes of operation it has no effect in single channel n Description Send DE, HS, VS on second channel if enabled Reserved Do not send DE, HS, VS on second channel use zero instead Use DE=0, HS=LE, VS=LF on second channel I | Project All All All | | | |
| 16 | Default V This bit o Value 00b 01b 10b 11b Channel Project: Default V | Name Reserved Reserved_E alue: | the two second s | vo channel modes of operation it has no effect in single channel n Description Send DE, HS, VS on second channel if enabled Reserved Do not send DE, HS, VS on second channel use zero instead Use DE=0, HS=LE, VS=LF on second channel | Project All All All All | | | |



| | | | LV | DS—LVDS Port Control Register | | | | | |
|-------|--|--------------|-----------|---|---------|--|--|--|--|
| 15 | LVDS_Border_Enable | | | | | | | | |
| | Project: All | | | | | | | | |
| | Default Value: 0b | | | | | | | | |
| | This selects whether the border data should be included in the active display data sent to the pa | | | | | | | | |
| | Value Name Description | | | | Project | | | | |
| | 0b | Disable | Border to | o the LVDS transmitter is disabled. DE (Display Enable) is used | All | | | | |
| | 1b | Enable | Border to | o the LVDS transmitter is enabled. Blank# is used as DE for the pane | I All | | | | |
| 14:11 | Reserve | ed l | Project: | All Format: | | | | | |
| 10 | Buffer_I | Power_[| Down_S | tate | | | | | |
| | Project: | | | All | | | | | |
| | Default \ | | | Ob | | | | | |
| | This bit selects the state of the LVDS buffers during a powered down state caused by the power sequence logic power down. This selection will be made based on the connected panel requirements. | | | | | | | | |
| | Value | Nam | e | Description P | oject | | | | |
| | 0b | Zero | | Zero Volts (Driven on both lines of the pairs) | .11 | | | | |
| | 1b | Tri-St | ate | Tri-State (High impedance state) Al | | | | | |
| 9:8 | ClkA,A0 | ,A1,A2_ | Control | | | | | | |
| | Project: All | | | | | | | | |
| | Default Value: 00b | | | | | | | | |
| | these lin | es when | the pan | -A2 data pairs and CLKA. It sets the highest level of activity that is all el is powered on. Power sequencing for LVDS connected panels over wer sequencer is in the power down mode all signals are in the power | errides | | | | |
| | Value | Nam | e | Description | Project | | | | |
| | 00b | Powe | er Down | Power Down all A channel signals including A3 (0V) | All | | | | |
| | 01b | Powe Data | | Power up – A0, A1, A2 Data bits forced to 0,Timing active, Clock Active | All | | | | |
| | 10b | Rese | rved | Reserved | All | | | | |
| | | | | | | | | | |



| 7:6 | Eight_bit_color_channel_A3,(B3)_Control | | | | | | | |
|-----|--|---|--|-------------------------|--|--|--|--|
| | Project: All | | | | | | | |
| | Default Value: 00b | | | | | | | |
| | This field can control both the A3 and B3 data pairs. Enabling those pairs indicates the selection of 8- bit per color channel mode. It sets the highest level of activity that is allowed on these lines when the panel is powered on. The A3 pair will only be powered up if both this field and the A0, A1, A2, CLKA field indicates that the pair should be powered up and will only be active if both indicate that it should be active. The B3 pair will only be powered up if both this field and the B0, B1, B2, (B3) field indicates that the pair should be powered up and will only be active if both indicate that it should be active. Power sequencing for LVDS connected panels overrides the control. When the power sequencer is in the power down mode all signals are in the power down state. | | | | | | | |
| | Value Name Description | | | | | | | |
| | 00b | Power Down | Power Down all signals A3, B3 (common mode) | All | | | | |
| | 01b | Power Up Data 0 | Power up – A3, (B3) Data (pixel data not control) lines forced to 0 output | All | | | | |
| | 10b | Reserved | Reserved | All | | | | |
| | 11b | 11bPower Up Data ActivePower up – A3, (B3) Data lines active | | | | | | |
| 5:4 | Two_channel_mode_ClkB_Control | | | | | | | |
| | Project: | | All | | | | | |
| | Default V | alue: | 00b | | | | | |
| | allowed o B0, B1, B | n these lines wh 2, (B3) field indi | de, this field controls the CLKB pair. It sets the highest level of active then the panel is powered on. The CLKB pair should only be powere cates that the second channel should be powered up and will only be d be active. Power sequencing for LVDS connected panels override | d up if the e active if | | | | |
| | | | | | | | | |
| | Value | Name | Description F | Project | | | | |
| | Value 00b | Name Power Down | · · | Project All | | | | |
| | | | Power Down CLKB (common mode) | - | | | | |
| | 00b | Power Down Power Up | Power Down CLKB (common mode) Power up – CLKB Forced to 0 | All | | | | |



| | | LVI | DS—LVDS Port Control Register | | | | |
|-----|---------------------------------------|--|---|------------------------|--|--|--|
| 3:2 | Two_cha | nnel_mode_B0 | ,B1,B2_Control | | | | |
| | Project: | | All | | | | |
| | Default Value: 00b | | | | | | |
| | these line the contro operation | es when the pane ol. During single is selected by se | e set B0-B2 data pairs. It sets the highest level of activity that is a el is powered on. Power sequencing for LVDS connected panels channel operation (1x18.0), these bits need to be both zero. Two etting them to ones. Note that the second clock can be optionally el mode ClkB control field. | overrides o channel | | | |
| | Value | Name | Description | Project | | | |
| | 00b | Power Down | Power Down all signals including B3 and CLKB | All | | | |
| | 01b | Power Up Data 0 | Power up – B0, B1, B2, Data lines forced to 0, timing is active | All | | | |
| | 10b | Reserves | Reserved | All | | | |
| | 11b | Power Up Data Active | Power up – Data lines active (color and timing) | All | | | |
| 1 | LVDS_de | etected | | | | | |
| | Project: | | All | | | | |
| | Access: | | Read Only | | | | |
| | Default V | alue: | Ob | | | | |
| | Read-onl GMBUS | y bit indicating w port 2 (LVDS) da | hether LVDS was detected during initialization. It signifies the levent ta line at boot. This bit is valid regardless of whether the port is e | vel of the enabled. | | | |
| | Value | Name | Description | Project | | | |
| | 0b | Not Detected | LVDS not detected during initialization | All | | | |
| | 1b | Detected | LVDS detected during initialization | All | | | |
| 0 | Reserved | d Project: | All Format: | | | | |



4. South FDI Rx and Transcoder Control (F0000h–FBFFFh)

4.1.1 Display Transcoder A Control

4.1.1.1 TRANSACONF—Transcoder A Configuration Register

| | ٦ | RANSAG | CONF—Tra | nscoder A Configuration Register | |
|---|---------------------------------|---|--|---|---------------------------------------|
| Register Ty Address Of Project: Default Val Access: Size (in bits Double But Bit | /pe: ffset: ue: s): | | MMIO F0008h All 00000000h R/W 32 | blank OR transcoder disabled | |
| 31 | Transco | der A Enab | le Project: | All | |
| | Changing enable bi VBLANK | g it to a zero t off disables event after t g generator is | should only be the timing gen he FDI is disabl | rns on transcoder A. This must be done before FDI done when FDI A has been disabled. Turning the t erator in this transcoder. FDI disable occurs after th led. Synchronization pulses to the display are not n nscoder timing registers must contain valid values b | ranscoder ne next naintained if |
| | 0b | Disable | Disabled | | All |
| | 1b | Enable | Enabled | | All |
| 30 | This read | disabling the | | All al state of the transcoder. Since there can be some d the transcoder actually shutting off, this bit indicate | |
| | Value | Name | Description | 1 | Project |
| | 0b | Disable | Disabled | | All |
| | 1b | Enable | Enabled | | All |
| 29 | Reserve | d Proje | ct: All | Format: | |
| 28:27 | Reserve | d | | | |



| | TR | ANSACON | IF—Transcoder A C | Configuration Register | |
|-------|------------------------------|--------------------------------------|--|--|--------------------------------|
| 26 | Reserved | Project: | All | Format: | |
| 25 | Reserved | | | | |
| 24 | Reserved | Project: | All | Format: | |
| 23:21 | Interlaced_ | Mode | | | |
| | Project: | | All | | |
| | Default Valu | ie: (| 000b | | |
| | software du in the vertic | iring transcodei al blank after p | setup (mode set). They a rogramming if transcoder is | is being set in the pipe, and mus re updated immediately if the tra enabled. The default behavior IF and transmitted over FDI VB- | inscoder is off, or is to have |
| | Value | Name | Description | | Project |
| | 000b | Progressive | Progressive display | | All |
| | 010b | Reserved | Reserved | | All |
| | 011b | Interlace | Interlaced display, progra | ammable Vsync for CRT, DP | All |
| | Others | Reserved | Reserved | | All |
| 20:8 | Reserved | Project: | All | Format: | |
| 4:2 | Reserved | Project: | All | Format: | |
| 1 | Reserved | | | | |
| 0 | Reserved | Project: | All | Format: | MBZ |



4.1.2 Display Transcoder B Control

4.1.2.1 TRANSBCONF—Transcoder B Configuration Register

| | TRANSE | BCONF | —Tra | nscoc | ler B Configura | ation I | Register | | |
|--------------|--------------------|-------------|----------|---------|----------------------|---------|----------|-----|--|
| Register Ty | | MMIO | | | | | | | |
| Address O | ffset: | F1008h | า | | | | | | |
| Project: | | All | | | | | | | |
| Default Val | ue: | 000000 | 00h | | | | | | |
| Access: | | R/W | | | | | | | |
| Size (in bit | · · | 32 | | | | | | | |
| Double But | ffer Update Point: | Start of | vertical | blank C | R transcoder disable | d | | | |
| Bit | | | | | Description | | | | |
| 31 | Transcoder_B_Ena | able Pro | oject: | All | Format: | | | | |
| | See Transcoder A d | lescriptior | ۱ | | | | | | |
| 30 | Transcoder_State | Pro | oject: | All | Format: | | | | |
| | See Transcoder A d | lescriptior | า | | | | | | |
| 29 | Reserved Pro | ject: | All | | | | Format: | | |
| 28:27 | Frame_Start_Delay | / Pro | oject: | All | Format: | | | | |
| | See Transcoder A d | lescriptior | r | | | | | | |
| 26 | Reserved Pro | ject: | All | | | | Format: | | |
| 25 | Reserved | | | | Project: | All | | | |
| 24 | Reserved Pro | ject: | All | | | | Format: | | |
| 23:21 | Reserved | | | | Project: | All | | | |
| 20:8 | Reserved Pro | ject: | All | | | | Format: | | |
| 7:5 | Display_Port_Bits_ | Per_Col | or | | Project: | All | Format: | | |
| | See Transcoder A d | lescriptior | <u>ו</u> | | | | | | |
| 4:2 | Reserved Pro | ject: | All | | | | Format: | | |
| 1 | Reserved | | | | Project: | All | | | |
| 0 | Reserved Pro | ject: | All | | | | Format: | MBZ | |



4.1.3 FDI A Receiver Control

4.1.3.1 FDI_RXA_CTL- FDI A Rx Control Register

| | | FDI_F | XA_CTL- FDI A Rx Control Register | |
|--------------|--------------|--------------|--|-----------|
| Register Ty | /pe: | MN | | |
| Address O | | | 00Ch | |
| Project: | | All | | |
| Default Val | ue: | 000 | 000040h | |
| Access: | | R/V | N | |
| Size (in bit | s): | 32 | | |
| Double But | fer Update F | Point: De | pends on bit | |
| Bit | | | Description | |
| 31 | FDI_Rx_A_ | Enable | | |
| | Project: | | All | |
| | Default Valu | le: | 0b | |
| | | | t it in its lowest power state. Port enable takes place on the Vbla te that link A is hardwired to transcoder A. | ank after |
| | Value | Name | Description | Project |
| | 0b | Disable | Disables and tristates the FDI Rx A interface | All |
| | 1b | Enable | Enable. This bit enables the FDI Rx A interface. | All |
| 30 | Reserved | Project: | All Format: MI | 3Z |
| 29:28 | Link_traini | ng_pattern_e | enable | |
| | Project: | | All | |
| | Default Valu | le: | 0b | |
| | Value | Name | Description | Project |
| | 00b | Pattern 1 | Pattern 1 enabled: Repetition of D10.2 characters. | All |
| | 01b | Pattern 2 | Pattern 2 enabled: Repetition of K28.5, D11.6, K28.5, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2. Please note that the entire pattern must complete before another pattern is sent. Scrambling initialization and disparity init commence at the end of the last iteration of pattern 2. | All |
| | 10b | Idle | Idle Pattern enabled: Transmit single-context scheduling followed by VB-ID with NoVideoStream_flag set to 1, five times | All |
| | 11b | Normal | Link not in training: Send normal pixels | All |
| | | | | |



| 21:19 | Port_Widt | th_Selection | | |
|-------|---|---|---|---|
| | Project: | All | | |
| | Default Va | lue: 0b | | |
| | Value | Name | Description | Project |
| | 000b | x1 Mode | x1 Mode | All |
| | 001b | x2 Mode | x2 Mode | All |
| | 010b | x3 Mode | x3 Mode | All |
| | 011b | x4 Mode | x4 Mode | All |
| | 111b | x8 Mode | x8 Mode | All |
| | Others | Reserved | Reserved | All |
| 18:16 | Bits_Per_ | Color | | |
| | Project: Default Va | All lue: 0b | | |
| | This field | selects the number (| of bits per color sent over the link Color form | nat takes place on the |
| | | | of bits per color sent over the link. Color forn olor format change can be done independent | |
| | Vblank aft | | | |
| | Vblank aft the link. | er being written. Co | olor format change can be done independent | t of a pixel clock change in |
| | Vblank aft the link. Value | er being written. Co Name | blor format change can be done independent Description | t of a pixel clock change in Project |
| | Vblank aft the link. Value 000b | er being written. Co Name 8 bpc | blor format change can be done independent Description 8 bits per color | t of a pixel clock change in Project All |
| | Vblank aft the link. Value 000b 001b | er being written. Co Name 8 bpc 10 bpc | blor format change can be done independent Description 8 bits per color 10 bits per color | t of a pixel clock change in Project All All |
| | Vblank aft the link. Value 000b 001b 010b | er being written. Co Name 8 bpc 10 bpc 6 bpc | blor format change can be done independent Description 8 bits per color 10 bits per color 6 bits per color | t of a pixel clock change in Project All All All |
| 15 | Vblank aft the link. Value 000b 001b 010b 011b 1XXb Link_reve | er being written. Co Name 8 bpc 10 bpc 6 bpc 12 bpc | Description 8 bits per color 10 bits per color 6 bits per color 12 bits per color Reserved | t of a pixel clock change in Project All All All All |
| 15 | Vblank aft the link. Value 000b 001b 010b 011b 1XXb Link_reve Project: | er being written. Co Name 8 bpc 10 bpc 6 bpc 12 bpc Reserved ersal_strap_overrid All | Description 8 bits per color 10 bits per color 6 bits per color 12 bits per color Reserved | t of a pixel clock change in Project All All All All |
| 15 | Vblank aft the link. Value 000b 001b 010b 011b 1XXb Project: Default Va Link is revu is strapped | Name 8 bpc 10 bpc 6 bpc 12 bpc Reserved rsal_strap_overrid All lue: 0b ersed if DMI is rever | Description 8 bits per color 10 bits per color 6 bits per color 12 bits per color Reserved | t of a pixel clock change in Project All All All All All All All Versal to the reverse of what Writing to this bit when the |
| 15 | Vblank aft the link. Value 000b 001b 010b 011b 1XXb Project: Default Va Link is revu is strapped | Name 8 bpc 10 bpc 6 bpc 12 bpc Reserved rsal_strap_overrid All lue: 0b ersed if DMI is rever | Description 8 bits per color 10 bits per color 6 bits per color 12 bits per color Reserved le | t of a pixel clock change in Project All All All All All All All Versal to the reverse of what Writing to this bit when the |
| 15 | Vblank aft the link. Value 000b 001b 010b 011b 1XXb Project: Default Va Link is revu is strapped link is enal | Name 8 bpc 10 bpc 6 bpc 12 bpc Reserved rsal_strap_overrid All lue: 0b ersed if DMI is rever 1. It must be set bef bled has no effect. | Description 8 bits per color 10 bits per color 6 bits per color 12 bits per color 12 bits per color Reserved le rsed. This bit overrides the status of DMI revelopment to take effect Both link A and link B must be off in order for | t of a pixel clock change in Project All All All All All All All All Versal to the reverse of what This bit to take effect. |



| | | FDI_RX | A_CTL- FDI A Rx Contro | ol Register |
|------|---------------------------|--------------------------------------|---|---|
| 14 | DMI_Link_ | reversal_status | 6 | |
| | Project: | ŀ | All | |
| | Access: | F | Read Only | |
| | Default Val | ue: C | b | |
| | This bit refl | ects the DMI link | k reversal strap. | |
| | Value | Name | Description | Project |
| | 0b | Not Reversed | Link not reversed | All |
| | 1b | Reversed | Link reversed. | All |
| 13 | FDI_PLL_e | enable F | Project: All Format: | Enable |
| | This bit ena | ables the FDI PL in either FDI RX | L. Software must enable this bit 1 A or FDI RXB Control registers. | 0uS prior to enabling the link. This bit |
| 12:9 | Reserved | Project: | All | |
| 8 | Reserved | | | |
| 7 | Reserved | Р | roject: All | |
| 6 | Reserved | | Project: All | |
| 5 | Reserved | | | |
| 4 | Rawclk_to | _PCDCLK_sele | ction | |
| | Project: | All | | |
| | Default Val | ue: Ob | | |
| | be program disregarded | imed as part of e d and Rawclk wi | enabling and disabling the link. If I | clock to PCDCLK (or vice versa). It must FDI PLL is disabled, this register will be set / boot flow for more detail. This bit can |
| | Value | Name | Description | Project |
| | 0b | Rawclk | Rawclk used | All |
| | 1b | PCDCLK | PCDCLK used | All |
| 3:0 | Reserved | Project: | All | Format: MBZ |



4.1.3.2 FDI_RXA_MISC— FDI A Rx Miscellaneous

| | | | FDI_R | XA_MIS | C— F | DI A Rx Miscell | aneous | | |
|--------------|--------|-----------|--|--------------|-----------------------|---|------------------------------|-------------------|----------------------------------|
| Register T | ype: | MMIO | | | | | | | |
| Address O | ffset: | F0010h | 1 | | | | | | |
| Project: | All | | | | | | | | |
| Default Val | lue: | 000000 | 80h | | | | | | |
| Access: | | R/W | | | | | | | |
| Size (in bit | s): | 32 | | | | | | | |
| Bit | | | | | | Description | | | |
| 31:13 | Rese | rved | Project: | All | | | For | mat: | MBZ |
| 12:0 | FDI_ | Delay | | Project: | All | Default Value: | 80h | | |
| | over | the FDI i | This field spe interface to e provided I | reach the ti | ncy as re ming ger | ative delay w.r.t. the herator FIFO in the tra | dot clock ree anscoder. S | quired pecific | for active data calculations (if |

4.1.3.3 FDI_RXA_ISR — FDI A Rx Interrupt Status Register

| | FDI_RXA_ISR — FDI A Rx Interrupt Status Register | | | | | | | | | |
|--------------------|--|--------------------|--------------|---|---------|--|--|--|--|--|
| Register Ty | pe: MMI | C | | | | | | | | |
| Address O | ffset: F001 | 4h | | | | | | | | |
| Project: | oject: All | | | | | | | | | |
| Default Val | Default Value: 0000000h | | | | | | | | | |
| Access: | Read | l Only | | | | | | | | |
| Size (in bit | s): 32 | | | | | | | | | |
| | | | | alue of FDI Receiver A interrupt sta reported on the combined FDI_RX | | | | | | |
| Bit | | | | Description | | | | | | |
| 31:11 | Reserved | Project: | All | F | Format: | | | | | |
| 10 | FDI_RX_In | ter-lane_Align | ment | | | | | | | |
| | Project: | | All | | | | | | | |
| | This bit ind | icates all the lar | nes are prop | erly inter-lane aligned | | | | | | |
| | Value | Name | Des | cription | Project | | | | | |
| | 0b | Not Aligned | Inter | -lane symbols are not aligned | All | | | | | |
| | 1b | Aligned | Inter | -lane symbols are properly aligned | All | | | | | |



| 9 | FDI RX | Symbol_Lock | | | | | | | | |
|---|---|------------------------------------|--|---------------------------|--|--|--|--|--|--|
| | Project: | - | All | | | | | | | |
| | This bit in lanes | dicates receiver | logic consecutively received training pattern 2 succe | ssfully on all the enable | | | | | | |
| | Value | Name | Description | Project | | | | | | |
| | 0b | Not Locked | Symbol is not locked | All | | | | | | |
| | 1b | Locked | Symbol lock is achieved | All | | | | | | |
| 8 | FDI_RX_I | FDI_RX_Bit_Lock | | | | | | | | |
| | Project: All | | | | | | | | | |
| | | dicates receiver enabled lanes. | logic consecutively received D10.2 pattern in training | g pattern 1 successfully | | | | | | |
| | Value | Name | Description | Project | | | | | | |
| | 0b | Not Locked | Bit is not locked | All | | | | | | |
| | 1b | Locked | Bit lock is achieved | All | | | | | | |
| 7 | FDI_RX_ | FDI_RX_Training_Pattern_2_Fail | | | | | | | | |
| | Project: All | | | | | | | | | |
| | This bit indicates that the training pattern 2 has failed | | | | | | | | | |
| | Value | Name | Description | Project | | | | | | |
| | 0b | No Error | Pattern 2 training did not report an error | All | | | | | | |
| | 1b | Failed | Pattern 2 has failed | All | | | | | | |
| 6 | Reserved | Project: | All For | mat: | | | | | | |
| 5 | | AFE_BIT_Unloc | | | | | | | | |
| | Project: | | All | a <u> </u> | | | | | | |
| | This bit in | dicates DRC circ | cuit detects that the recovered clock has drifted from | | | | | | | |
| | Value | Name | Description | Project | | | | | | |
| | 0b | No Drift | Recovered clock does not drift from the received da | ita All | | | | | | |
| | 1b | Drift | Recovered clock has drifted from the received data | All | | | | | | |
| 4 | FDI_RX_ | Symbol_Error_F | Rate_above_10^-9 | | | | | | | |
| | Project: | | All | | | | | | | |
| | This bit in | dicates the receipt | ived symbol error rate is more than 10^-9. | | | | | | | |
| | Value | Name | Description | Project | | | | | | |
| | 0b | Less than | The received symbol error rate is not greater than 1 | 0^-9 All | | | | | | |
| | 1 | | The received symbol error rate is greater than 10^- | | | | | | | |



| 3 | Reserved | | | |
|---|---|---|---|--|
| 2 | | Pixel_FIFO_Overflo | | |
| 2 | Project: | All | 54 | |
| | - | | Pixel FIFO overflowed or not. | |
| | Value | Name | Description | Project |
| | 0b | No Overflow | Pixel FIFO did not overflow | All |
| | 1b | Overflow | Pixel FIFO overflowed | All |
| 1 | FDI_RX_0 | Cross_Clock_FIFO | _Overflow | |
| | | | | |
| | Project: | All | | |
| | - | | Cross Clock symbol clock to display clock FIF | O overflowed or not. |
| | - | | Cross Clock symbol clock to display clock FIF Description | O overflowed or not. Project |
| | This bit in | dicates weather the | | |
| | This bit inc Value | dicates weather the Name | Description | Project |
| 0 | This bit in Value Ob 1b | dicates weather the Name No Overflow | Description Cross Clock FIFO did not overflow Cross Clock FIFO overflowed | Project All |
| 0 | This bit in Value Ob 1b | dicates weather the Name No Overflow Overflow | Description Cross Clock FIFO did not overflow Cross Clock FIFO overflowed | Project All |
| 0 | This bit ind Value 0b 1b FDI_RX_S Project: | dicates weather the Name No Overflow Overflow Symbol_Queue_ov All | Description Cross Clock FIFO did not overflow Cross Clock FIFO overflowed | Project All |
| 0 | This bit ind Value 0b 1b FDI_RX_S Project: | dicates weather the Name No Overflow Overflow Symbol_Queue_ov All | Description Cross Clock FIFO did not overflow Cross Clock FIFO overflowed | Project All |
| 0 | This bit ind Value 0b 1b FDI_RX_S Project: This bit ind | dicates weather the Name No Overflow Overflow Symbol_Queue_ov All dicates weather the | Description Cross Clock FIFO did not overflow Cross Clock FIFO overflowed | Project All All |



4.1.3.4 FDI_RXA_IMR — FDI A Rx Interrupt Mask Register

| | | FDI_RXA_ | IMR — I | F DI A I | Rx Interrup | ot Mask Register | r | |
|--------------------|---------------|-------------------------------------|----------|-----------------|------------------------------|--|-------|-------------------|
| Register T | ype: MM | lio | | | | | | |
| Address O | ffset: F00 |)18h | | | | | | |
| Project: | All | | | | | | | |
| Default Val | lue: 000 | 007FFh | | | | | | |
| Access: | R/V | V | | | | | | |
| Size (in bit | s): 32 | | | | | | | |
| | d" bits will | | | | | SR bits are "masked' upt in the SDEISR. | | |
| Bit | | | | | Description | | | |
| 31:11 | Reserved | d Project: | All | | | Format | | MBZ |
| 10:0 | Interrupt | _Mask_Bits | Project: | All | Format: | Interrupt Control Reg | giste | ers |
| | | contains a bit m ined FDI_RXA ii | | | | bits from the FDI_RXA | _ISR | R are reported on |
| | Value | Name | Descript | ion | | | | Project |
| | 0b | Not Masked | | | be reported or ain SDEISR | the combined FDI_R | XA | All |
| | 1b | Masked | Masked - | - will not | be reported | | | All |



4.1.4 FDI B Receiver Control

4.1.4.1 FDI_RXB_ISR — FDI B Rx Interrupt Status Register

| | F | DI_RXB_ISR - | - FDI B Rx Interrupt Status Regis | ster | | | | | | |
|--------------|-----------------------------|-----------------|---|---------|--|--|--|--|--|--|
| Register Ty | ype: MMIC |) | | | | | | | | |
| Address O | ffset: F1014 | 4h | | | | | | | | |
| Project: | All | | | | | | | | | |
| Default Val | | | | | | | | | | |
| Access: | Read | Only | | | | | | | | |
| Size (in bit | | | | | | | | | | |
| See FDI_R | XA descript | ion. | | | | | | | | |
| Bit | | | Description | | | | | | | |
| 31:11 | Reserved | Project: All | For | mat: | | | | | | |
| 10 | FDI_RX_Inter-lane_Alignment | | | | | | | | | |
| | Project: | All | | | | | | | | |
| | See FDI_RXA description | | | | | | | | | |
| | Value | Name | Description | Project | | | | | | |
| | 0b | Not Aligned | Inter-lane symbols are not aligned | All | | | | | | |
| | 1b | Aligned | Inter-lane symbols are properly aligned | All | | | | | | |
| 9 | FDI_RX_Sy | /mbol_Lock | | | | | | | | |
| | Project: | All | | | | | | | | |
| | - | XA description | | | | | | | | |
| | Value | Name | Description | Project | | | | | | |
| | 0b | Not Locked | Symbol is not locked | All | | | | | | |
| | 1b | Locked | Symbol lock is achieved | All | | | | | | |
| 8 | FDI_RX_Bi | t Lock | | | | | | | | |
| | Project: | All | | | | | | | | |
| | - | XA description. | | | | | | | | |
| | | | | | | | | | | |
| | Value | Name | Description | Project | | | | | | |
| | 0b | Not Locked | Bit is not locked | All | | | | | | |
| | 1b | Locked | Bit lock is achieved | All | | | | | | |
| | | | | | | | | | | |



| 7 | FDI RX T | raining_Patter | n 2 Fail | | | | | | |
|---|---|--------------------------------------|--|---------|---------|--|--|--|--|
| - | Project: | | All | | | | | | |
| | - | RXA description | | | | | | | |
| | Value | Name | Description | Project | | | | | |
| | 0b | No Error | Pattern 2 training did not report an error | All | | | | | |
| | 1b | Failed | Pattern 2 has failed | All | | | | | |
| 6 | Reserved | Project: | All For | mat: | | | | | |
| 5 | FDI_RX_A | FE_BIT_Unloc | cked | | | | | | |
| | Project: | | All | | | | | | |
| | See FDI_RXA description | | | | | | | | |
| | Value | Name | Description | | Project | | | | |
| | 0b No Drift Recovered clock does not drift from the received data | | | | | | | | |
| | 1b | Drift | Recovered clock has drifted from the received data | | All | | | | |
| 4 | FDI_RX_S | FDI_RX_Symbol_Error_Rate_above_10^-9 | | | | | | | |
| | Project: | - | | | | | | | |
| | See FDI_I | RXA description |). | | | | | | |
| | Value | Name | Description | | Project | | | | |
| | 0b | Less than | The received symbol error rate is not greater than 1 | 10^-9 | All | | | | |
| | 1b | Greater than | The received symbol error rate is greater than 10^- | 9 | All | | | | |
| 3 | Reserved | | | | | | | | |
| 2 | FDI RX P | FDI_RX_Pixel_FIFO_Overflow | | | | | | | |
| | Project: | | All | | | | | | |
| | See FDI_F | RXA description | | | | | | | |
| | Value | Name | Description | Project | | | | | |
| | 0b | No Overflow | Pixel FIFO did not overflow | All | | | | | |
| | 1b | Overflow | Pixel FIFO overflowed | All | | | | | |
| 1 | FDI_RX_C | cross_Clock_F | IFO_Overflow | | | | | | |
| | Project: | | All | | | | | | |
| | See FDI_F | RXA description | | | | | | | |
| | Value | Name | Description | Project | | | | | |
| | | No Overflow | Cross Clock FIFO did not overflow | All | | | | | |
| | 0b | NO Overnow | | , | | | | | |



| | FDI_RXB_ISR — FDI B Rx Interrupt Status Register | | | | | | | |
|---|--|------------------|-------------------------------|---------|--|--|--|--|
| 0 | FDI_RX_S | Symbol_Queue_ov | erflow | | | | | |
| | Project: | All | | | | | | |
| | See FDI_F | RXA description. | | | | | | |
| | Value | Name | Description | Project | | | | |
| | 0b | No Overflow | Symbol Queue did not overflow | All | | | | |
| | 1b | Overflow | Symbol Queue overflowed | All | | | | |
| | | | | | | | | |

4.1.4.2 FDI_RXB_IMR — FDI B Rx Interrupt Mask Register

| | | FDI_RXB_ | | FDI B I | Rx Interrup | ot Mask Register | |
|--------------|---------------|-----------------|-----------------------|----------|-------------|---------------------------|---------|
| Register T | ype: MM | 10 | | | | | |
| Address O | ffset: F10 | 18h | | | | | |
| Project: | All | | | | | | |
| Default Va | lue: 000 | 007FFh | | | | | |
| Access: | R/W | / | | | | | |
| Size (in bit | s): 32 | | | | | | |
| See FDI_R | XA descri | ption. | | | | | |
| Bit | | | | | Description | | |
| 31:11 | Reserved | Project: | All | | | Format: | MBZ |
| 10:0 | Interrupt | _Mask_Bits | Project: | All | Format: | Interrupt Control Registe | ers |
| | See FDI_ | RXA description | n. | | | | |
| | Value | Name | Descript | ion | | | Project |
| | 0b | Not Masked | Not Mask interrupt | | | the combined FDI_RXB | All |
| | 1b | Masked | Maskad | will not | be reported | | All |



| | | FDI_R | RXB_CTL- FDI B Rx Control Register | |
|-------------|----------------|----------------|--|---------|
| Register T | Type: | MN | AIO | |
| Address C | | F1(| 00Ch | |
| Project: | | All | | |
| Default Va | alue: | 000 | 000040h | |
| Access: | | R/V | N | |
| Size (in bi | | 32 | | |
| Double Bu | uffer Update F | Point: De | pends on bit | |
| Bit | | | Description | |
| 31 | FDI_Rx_B_ | Enable | | |
| | Project: | | All | |
| | Default Valu | le: | Ob | |
| | See FDI_R | XA description | n. | |
| | Value | Name | Description | Project |
| | 0b | Disable | Disables and tristates the FDI Rx A interface | All |
| | 1b | Enable | Enable. This bit enables the FDI Rx A interface. | All |
| 30 | Reserved | Project: | All Format: ME | 3Z |
| 29:28 | Link_traini | ng_pattern_e | enable | |
| | Project: | | All | |
| | Default Valu | ne: | Ob | |
| | See FDI_R | XA descriptio | n. | |
| | Value | Name | Description | Project |
| | 00b | Pattern 1 | Pattern 1 enabled: Repetition of D10.2 characters. | All |
| | 01b | Pattern 2 | Pattern 2 enabled: Repetition of K28.5, D11.6, K28.5, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2. Please note that the entire pattern must complete before another pattern is sent. Scrambling initialization and disparity init commence at the end of the last iteration of pattern 2. | All |
| | 10b | Idle | Idle Pattern enabled: Transmit single-context scheduling followed by VB-ID with NoVideoStream_flag set to 1, five times | All |
| | 11b | Normal | Link not in training: Send normal pixels | All |
| 27:22 | Reserved | Project: | All Format: | |

4.1.4.3 FDI_RXB_CTL- FDI B Rx Control Register



| | | FDI_R | XB_C | CTL- FDI B | Rx Cont | trol Regis | ster | |
|-------|-------------|----------------|---------|-----------------|---------|------------|---------|---------|
| 21:19 | | n_Selection | | | | | | |
| | Project: | | All | | | | | |
| | Default Val | | 0b | | | | | |
| | See FDI_R | XA descriptior | ٦. | | | | | |
| | Value | Name | | Description | | | F | Project |
| | 000b | x1 Mode | | x1 Mode | | | ŀ | All |
| | 001b | x2 Mode | | x2 Mode | | | A | All |
| | 010b | x3 Mode | | x3 Mode | | | A | All |
| | 011b | x4 Mode | | x4 Mode | | | A | All |
| | 111b | x8 Mode | | x8 Mode | | | A | All |
| | others | Reserved | | Reserved | | | P | All |
| 18:16 | Bits_Per_C | Color | | | | | | |
| | Project: | | All | | | | | |
| | Default Val | ue: | 0b | | | | | |
| | See FDI_R | XA descriptio | n. | | | | | |
| | Value | Name | | Description | | | F | Project |
| | 000b | 8 bpc | | 8 bits per colo | or | | A | All |
| | 001b | 10 bpc | | 10 bits per co | olor | | A | All |
| | 010b | 6 bpc | | 6 bits per colo | or | | A | All |
| | 011b | 12 bpc | | 12 bits per co | olor | | A | All |
| | 1XXb | Reserved | | Reserved | | | A | All |
| 15 | Reserved | Project: | All | | | | Format: | MBZ |
| 14 | DMI_Link_ | reversal_stat | us | | | | | |
| | Project: | | All | | | | | |
| | Access: | | Read | Only | | | | |
| | Default Val | ue: | 0b | | | | | |
| | See FDI_R | XA descriptior | ٦. | | | | | |
| | Value | Name | | Description | | | | Project |
| | 0b | Not Reverse | ed | Link not rever | rsed | | | All |
| | 1b | Reversed | | Link reversed | I. | | | All |
| 13 | FDI_PLL_e | enable | Projec | t: All | Format: | Enable | | |
| | | XA descriptior | | | | | | |
| 12:9 | Reserved | Project: | All | | | | Format: | |
| 8 | Reserved | | | | | | | |
| 7 | Reserved | | Project | t: All | | | | |



| 6 | Reserved | | Project: All | |
|---|--------------|-----------------|--------------|---------|
| 5 | Reserved | | | |
| 4 | Rawclk_to | _PCDCLK_sele | ction | |
| | Project: | All | | |
| | Default Valu | ue: 0b | | |
| | See FDI_R | XA description. | | |
| | Value | Name | Description | Project |
| | 0b | Rawclk | Rawclk used | All |
| | 1b | PCDCLK | PCDCLK used | All |

4.1.4.4 FDI_RXB_MISC— FDI B Rx Miscellaneous

| | | | FDI_R | XB_MIS | C—F | DI B Rx Miscell | laneo | us | |
|-----------------------|--------|--------|---------------|----------|-----|-----------------|-------|---------|-----|
| Register T | ype: | MMIO | | | | | | | |
| Address O | ffset: | F1010h | า | | | | | | |
| Project: | | All | | | | | | | |
| Default Value: | | 000000 |)80h | | | | | | |
| Access: | | R/W | | | | | | | |
| Size (in bit | s): | 32 | | | | | | | |
| Bit | | | | | | Description | | | |
| 31:13 | Rese | rved | Project: | All | | | | Format: | MBZ |
| 12:0 | FDI_D | Delay | | Project: | All | Default Value: | 80h | | |
| | See F | DI_RX | A description | n. | | | | | |



4.2 HD Audio Registers (E2000h–E2FFFh)

These registers are memory mapped and accessible through normal 32 bit, 16 bit, or 8 bit accesses.

4.2.1 Audio Configuration

The video driver configures the audio operation through the following procedure.

- 1. Read the Capabilities Written bit in the Audio Configuration register at address offset 0xE2000. If this bit is a 1, the video driver does not need to write the audio configuration. If this bit is a 0, continue this procedure to write the audio configuration.
- Read the EDID and directly write the EDID data into the audio EDID register region at address offset 0xE2080
- 3. Parse the EDID information to determine the monitor's audio capabilities. Then configure the hardware for those capabilities by setting the capability registers.
 - Write the audio capabilities to the Audio PCM Sizes and Rates register at address offset 0xE2044
 - Write the compressed audio supported formats to the Audio Stream Formats register at address offset 0xE2048
 - Set the presence detect bit to 1 in the Audio Pin Sense register at address offset 0xE2074
- 4. Set the Capabilities Written bit in the Audio Configuration register to 1. This indicates that the hardware can begin processing audio data using the current settings.

4.2.2 AUD_CONFIG_A—Audio Configuration – Transcoder A

| | | AUC | CONFIC | G_A—Au | dio Configuration – Transcoder A | |
|----------------|--------|---------|-------------|--------|----------------------------------|--|
| Register Ty | /pe: | MMIO | | | | |
| Address Of | fset: | E2000ł | า | | | |
| Project: | | All | | | | |
| Default Value: | | 000000 |)00h | | | |
| Access: | | R/W | | | | |
| Size (in bits | s): | 32 | | | | |
| This registe | er con | figures | the audio o | utput. | | |
| Bit | | | | | Description | |
| 31:30 | Rese | erved | Project: | All | Format: | |



| 29 | N_value_Index | | | | | | | | |
|-------|--|------------|---|----------|--------|---------------|---------|--|--|
| | Project: | | All | | | | | | |
| | Default V | alue: | Ob | | | | | | |
| | Value | Name | Description | | | | Project | | |
| | 0b | HDMI | N value read on bits 27:20 and 15:4 reflects HDMI N value. Bits 27:20 and 15:4 are is programmable to any N value - default h7FA6. | | | | | | |
| | 1b | DP | N value read on bits 27:20 and 15:4 reflects DP N value. Set this bit to 1 before programming N value register. When this is set to 1, 27:20 and 15:4 will reflect the current N value – default h8000. | | | | All | | |
| 28 | N_progra | amming_e | nable(testmode) | Project: | All | Security: | Test | | |
| | | | gramming of N values for non-CEA mod ned must be disabled when changing th | | ote th | at the Transc | oder to | | |
| 27:20 | Upper_N | _value(tes | stmode) | Project: | All | Security: | Test | | |
| | These are bits [19:12] of programmable N values for non-CEA modes. Bit 25 of this rube written in order to enable programming. Please note that the Transcoder to which must be disabled when changing this field. | | | | | | | | |



| 9:16 | Pixel_Clo | ck(HDMI) | | | | | | | |
|------|--------------------------|--|---|-------------|--|--|--|--|--|
| | Project: All | | | | | | | | |
| | Default Value: 0b | | | | | | | | |
| | | target frequency of the (sed for generating N_CT) | CEA/HDMI video mdoe to which the audio stream is ado S packets. | led. This | | | | | |
| | not requir | e this programming. | ock and does not refer to DP Link clock. DP Link cloud | | | | | | |
| | Value | Name | Description | Project | | | | | |
| | 0000b | 25.2 / 1.001 MHz | 25.2 / 1.001 MHz | All | | | | | |
| | 0001b | 25.2 MHz | 25.2 MHz Program this value for pixel clocks not listed in this field | All | | | | | |
| | 0010b 27 MHz 27 MHz | | | | | | | | |
| | 0011b | 27 * 1.001 MHz | 27 * 1.001 MHz | All | | | | | |
| | 0100b | 54 MHz | 54 MHz | | | | | | |
| | 0101b | 54 * 1.001 MHz | 54 * 1.001 MHz | All | | | | | |
| | 0110b | 74.25 / 1.001 MHz | 74.25 / 1.001 MHz | All | | | | | |
| | 0111b | 74.25 MHz | 74.25 MHz | All | | | | | |
| | 1000b | 148.5 / 1.001 MHz | 148.5 / 1.001 MHz | All All | | | | | |
| | 1001b | 148.5 MHz | 148.5 MHz | | | | | | |
| | Others | Reserved | Reserved | All | | | | | |
| 15:4 | Lower_N_ | value(testmode) | Project: All Security: | Test | | | | | |
| | be written | These are bits [11:0] of programmable N values for non-CEA modes. Bit 25 of this register must also be written in order to enable programming. Please note that the Transcoder to which audio is attached must be disabled when changing this field. | | | | | | | |
| | | ter can also be used to er when bit 29 is set to | program N value for DP for a specific Port. Default 1 is h7FA6 | value on | | | | | |
| 3 | Disable_N | стѕ | Project: All | | | | | | |
| | Set this bit CTM mode | | I generation for CTM modes. This is to enable prediction | n of CRC in | | | | | |
| | | | | | | | | | |



4.2.3 AUD_CONFIG_B—Audio Configuration – Transcoder B

| [| | | | | | | | | | |
|--------------|------------------|-----------------------------------|---------------------------|---|---------|--|--|--|--|--|
| | Α | UD_CO | NFIG_B—Audio Conf | figuration – Transcoder B | | | | | | |
| Register T | ype: MN | 110 | | | | | | | | |
| Address O | ffset: E2 | 100h | | | | | | | | |
| Project: | All | | | | | | | | | |
| Default Val | l ue: 000 | 00000h | | | | | | | | |
| Access: | R/V | V | | | | | | | | |
| Size (in bit | s): 32 | | | | | | | | | |
| This registe | er configu | res the au | dio output. | | | | | | | |
| Bit | | Description | | | | | | | | |
| 31:30 | Reserve | Reserved Project: All Format: | | | | | | | | |
| 29 | N_value | N_value_Index | | | | | | | | |
| | Project: | Project: All | | | | | | | | |
| | Default V | alue: | 0b | | | | | | | |
| | Value | Name | Description | | Project | | | | | |
| | 0b | HDMI | | and 15:4 reflects HDMI N value. Bits ammable to any N value - default h7FA6. | All | | | | | |
| | 1b | DP | to 1 before programming N | and 15:4 reflects DP N value. Set this bit value register. When this is set to 1, ne current N value – default h8000. | All | | | | | |
| 28 | N_progra | amming_e | nable(testmode) | Project: All Security: | Test | | | | | |
| | See Tran | scoder A d | escription. | | | | | | | |
| 27:20 | | l_ value(tes scoder A d | • | Project: All Security: | Test | | | | | |



| 19:16 | Pixel_Clo | ck(HDMI) | | | | |
|-------|------------------------|----------------------|---|------------|--|--|
| | Project: | All | | | | |
| | Default Va | lue: 0b | | | | |
| | See Trans | coder A description. | | | | |
| | Value Name Description | | | | | |
| | 0000b | 25.2 / 1.001 MHz | 25.2 / 1.001 MHz | | | |
| | 0001b | 25.2 MHz | 25.2 MHz Program this value for pixel clocks not listed in this field | All | | |
| | 0010b | 27 MHz | 27 MHz | | | |
| | 0011b | 27 * 1.001 MHz | 27 * 1.001 MHz | All | | |
| | 0100b | 54 MHz | 54 MHz | All All | | |
| | 0101b | 54 * 1.001 MHz | 54 * 1.001 MHz | | | |
| | 0110b | 74.25 / 1.001 MHz | 74.25 / 1.001 MHz 74.25 MHz | | | |
| | 0111b | 74.25 MHz | | | | |
| | 1000b | 148.5 / 1.001 MHz | 148.5 / 1.001 MHz | All | | |
| | 1001b | 148.5 MHz | 148.5 MHz | All | | |
| | others | Reserved | Reserved | All | | |
| 15:4 | Lower_N_ | value(testmode) | Project: All Security: | Test | | |
| | See Trans | coder A description | | | | |
| 3 | Disable_N | ICTS | Project: All | | | |
| | See Trans | coder A description | | | | |
| 2:0 | Reserved | Project: All | Format: | | | |



4.2.4 AUD_MISC_CTRL_A—Audio MISC Control for Transcoder

| | AUD | MISC_CTRI | A—Audio N | ISC Control for Transcoder A | | |
|------------------------|---|------------------------------------|---------------------|---|--|--|
| Register T | Type: MMIC |) | _ | | | |
| | Offset: E2010 |)h | | | | |
| Project: Default Va | All alue: 00000 | 0040h | | | | |
| Access: | Read | | | | | |
| Size (in bit | | Only | | | | |
| Bit | | | | Description | | |
| 31:8 | Reserved | Project: | All | Format: MBZ | | |
| 8 | | esent_Disable sed to Disable sa | ample present for H | Project: All Security: Debug IDMI or DP (Chicken Bit) | | |
| 7:4 | | • | | Default Value: 0100b nple is received from the HD Audio link and when it | | |
| 3 | Reserved | Project: | All | Format: MBZ | | |
| 2 | Sample_Fa | brication_EN_b | oit | | | |
| | Project: | A | II | | | |
| | Access: | R | /W | | | |
| | Default Valu | ue: Ot | b | | | |
| | This bit indicates whether internal fabrication of audio samples is enabled during a link underrun. | | | | | |
| | Value | Name | Description | Project | | |
| | 0b | Disable | Audio fabrica | ation disabled All | | |
| | 0.5 | | | | | |



| Droject | | | |
|-----------------------------|-------------------|---|----------|
| Project: | All | | |
| Access: | R/\ | N | |
| Default Val | ue: Ob | | |
| bit, the HD Note: Settir | Audio codec allov | le by an HD Audio verb. When Pro is allow vs a verb to set the device into professiona on bit does not change the default Pro bit v ess, using a verb. | al mode. |
| Value | Name | Description | Project |
| 0b | Consumer | Consumer use only | All |
| 1b | Professional | Professional use allowed | All |

4.2.5 AUD_MISC_CTRL_B—Audio MISC Control for Transcoder B

| | AUD_MISC_CTRL_B—Audio MISC Control for Transcoder B |
|--------------|---|
| Register Ty | ype: MMIO |
| Address O | ffset: E2110h |
| Project: | All |
| Default Val | ue: 00000040h |
| Access: | Read Only |
| Size (in bit | s): 32 |
| Bit | Description |
| 31:8 | Reserved Project: All Format: MBZ |
| 8 | Sample_present_Disable Project: All Security: Debug |
| | See Transcoder A description |
| 7:4 | Output_Delay Project: All Default Value: 0100b |
| | See Transcoder A description. |
| 3 | ReservedProject:AllFormat:MBZ |



| | 1 | | B—Audio MISC Control for | Transcoder B | | | |
|---|-------------------------------|-------------------|----------------------------|--------------|--|--|--|
| 2 | Sample_F | abrication_EN_bit | | | | | |
| | Project: | All | | | | | |
| | Access: | R/W | 1 | | | | |
| | Default Va | lue: 0b | | | | | |
| | See Transcoder A description. | | | | | | |
| | Value | Name | Description | Project | | | |
| | 0b | Disable | Audio fabrication disabled | All | | | |
| | 1b | Enable | Audio fabrication enabled | All | | | |
| 1 | Pro_Allow | ved | | | | | |
| | Project: | All | | | | | |
| | Access: | R/W | I | | | | |
| | Default Va | lue: 0b | | | | | |
| | See Transcoder A description. | | | | | | |
| | Value | Name | Description | Project | | | |
| | 0b | Consumer | Consumer use only | All | | | |
| | 1b | Professional | Professional use allowed | All | | | |
| 0 | Reserved | Project: A | 11 | Format: MBZ | | | |



4.2.6 AUD_VID_DID—Audio Vendor ID / Device ID

| | | AUE | D_VID_DID- | –Audi | o Vendor | ID / Device ID | | | | |
|---|---------|---|---|------------|---------------|------------------------------------|--|--|--|--|
| Register T | ype: | MMIO | | | | | | | | |
| Address Offset: Project: Default Value: | | E2020h | | | | | | | | |
| | | All | | | | | | | | |
| | | 80862804h | | | | | | | | |
| Access: | | Read Only | | | | | | | | |
| Size (in bit | ts): | 32 | | | | | | | | |
| hese valu | les are | returned from | the device as | s the Ve | ndor ID/ Devi | ice ID response to a Get Root Node | | | | |
| ommand. | | | | | | - | | | | |
| Bit | | Description | | | | | | | | |
| 31:16 | Vend | or_ID | Project: | All | Format: | U16 | | | | |
| | Used | Used to identify the codec within the PnP system. | | | | | | | | |
| | This f | This field is hardwired within the device. Value = $0x8086$ | | | | | | | | |
| 15:0 | Devic | e_ID | Project: | All | Format: | U16 | | | | |
| | Cons | tant used to ide | entify the codec | within the | e PnP svstem. | | | | | |
| | | Constant used to identify the codec within the PnP system. | | | | | | | | |
| | Th:- 6 | | This field is set by the device hardware. Value = 0x2804 [Ibexpeak] | | | | | | | |

4.2.7 AUD_RID—Audio Revision ID

| | | | | AUD_R | ID—Au | dio Revision | ID |
|--------------|---------|---------------------|--------------|----------------|-------------|--------------------|----------------------------------|
| Register T | ype: | MMIO | | | | | |
| Address O | ffset: | E2024h | ı | | | | |
| Project: | | All | | | | | |
| Default Va | lue: | 001000 | 00h | | | | |
| Access: | | Read C | Inly | | | | |
| Size (in bit | s): | 32 | | | | | |
| These valu | ies are | e returne | ed from the | device as | s the Rev | vision ID response | e to a Get Root Node command. |
| Bit | | | | | | Description | |
| 31:24 | Rese | erved | Project: | All | | | Format: |
| 23:20 | Majo | r_Revis | ion | Project: | All | Default Value: | 0001b |
| | | major re oliant. | vision numb | er (left of th | ne decima | I) of the HD Audio | Spec to which the codec is fully |
| | This | field is h | ardwired wit | hin the dev | vice. Value | e = 0x1 | |



| | | AUD_RID—Audio Revision ID | | | | | |
|-------|---|---|--|--|--|--|--|
| 19:16 | Minor_Revision | Project: All | | | | | |
| | The minor revision number (rights of the decimal) or "dot number" of the HD Audio Spec to which the codec is fully compliant. | | | | | | |
| | This field is hardwired within the device. Value = $0x0$ | | | | | | |
| 15:8 | Revision_ID | Project: All | | | | | |
| | The vendor's revision | number for this given Device ID. | | | | | |
| | This field is hardwired within the device. Value = $0x0$ | | | | | | |
| 7:0 | Stepping_ID | Project: All | | | | | |
| | An optional vendor s | epping number within the given Revision ID. | | | | | |
| | This field is hardwire | within the device. Value = $0x0$ | | | | | |



4.2.8 AUD_PWRST—Audio Power State (Function Group, Convertor, Pin Widget)

| | | AL | Idio Power State Format | | |
|----------|--------------|-------------|-------------------------|---------|--|
| Project: | All | | | | |
| Bit | Description | | | | |
| 1:0 | Power_Sta | te | | | |
| | Project: | All | | | |
| | Default Valu | ue: 11b | D3 | | |
| | Value | Name | Description | Project | |
| | 00b | D0 | D0 | All | |
| | 01b,10b | Unsupported | Unsupported | All | |
| | 11b | D3 | D3 | All | |

| AUD | D_PW | RST—Audio Power State (Function | on Grou | р, С | onverto | or, Pin Widget) |
|------------------------|--------|---|-------------|-------------|-----------|-----------------------------|
| Register Type: | | MMIO | | | | |
| Address Of | ffset: | E204Ch | | | | |
| Project: | | All | | | | |
| Default Val | ue: | 00FFFFFh | | | | |
| Access: | | Read Only | | | | |
| Size (in bit | s): | 32 | | | | |
| These valu command. | es are | returned from the device as the Power Sta | ate respons | se to | a Get Aud | dio Function Group |
| Bit | | Descr | iption | | | |
| 31:24 | Rese | rved | Project: | All | Format: | |
| 23:22 | Func | tion_Group_Device_Power_State_Current | Project: | All | Format: | Audio Power State Format |
| | Curre | ent power state | | | | |
| 21:20 | Func | tion_Group_Device_Power_State_Set | Project: | All | Format: | Audio Power State Format |
| | Powe | er state that was set | | | | |
| 19:18 | Conv | rertorB_Widget_Power_State_Current | Project: | All | Format: | Audio Power State Format |
| | Curre | ent power state | | | | |



| 17:16 | ConvertorB_Widget_Power_State_Requested | Project: | All | Format: | Audio Power State Format |
|-------|--|----------|-----|---------|-----------------------------|
| | Power state that was requested by audio software | | | | |
| 15:14 | ConvertorA_Widget_Power_State_Current | Project: | All | Format: | Audio Power State Format |
| | Current power state | | | | |
| 13:12 | ConvertorA_Widget_Power_State_Requsted | Project: | All | Format: | Audio Power State Format |
| | Power state that was requested by audio software | | | | |
| 11:10 | PinD_Widget_Power_State_Current | Project: | All | Format: | Audio Power State Format |
| | Current power state | | | | |
| 9:8 | PinD_Widget_Power_State_Set | Project: | All | Format: | Audio Power State Format |
| | Power state that was set | | | | |
| 7:6 | PinC_Widget_Power_State_Current | Project: | All | Format: | Audio Power State Format |
| | Current power state | | | | |
| 5:4 | PinC_Widget_Power_State_Set | Project: | All | Format: | Audio Power State Format |
| | Power state that was set | | | | |
| 3:2 | PinB_Widget_Power_State_Current | Project: | All | Format: | Audio Power State |
| | Current power state | | | | |
| 1:0 | PinB_Widget_Power_State_Set | Project: | All | Format: | Audio Power State Format |
| | Power state that was set | | | | |

4.2.9 AUD_PORT_EN_HD_CFG — Audio Port Enable HDAudio Config

AUD_PORT_EN_HD_CFG — Audio Port Enable HDAudio Config



| | AUD_P | ORT_EN_HD_(| CFG — Audio Port Enable | HDAudio Config | | |
|-------|--|--|--|--------------------------|--|--|
| | ffset: E2070 All Debu ue: 00077 Read s): 32 | Ch g 7003h Only ned from the devic | e as the Digital Converter respon Description | se to a Get Audio Output | | |
| 31:19 | Reserved | Project: All | | Format: | | |
| 18 | Port_D_Amp_Mute_Status Project: All Default Value: 1b Amp muted This read-only bit reflects the mute status of the amplifier | | | | | |
| | Value | Name | Description | Project | | |
| | 0b | Amp not muted | Amp not muted | All | | |
| | 1b | Amp muted | Amp muted | All | | |
| 17 | Project: Default Valu | | Amp muted ute status of the amplifier | | | |
| | Value | Name | Description | Project | | |
| | 0b | Amp not muted | Amp not muted | All | | |
| | 1b | Amp muted | Amp muted | All | | |
| 16 | Port_B_Amp_Mute_Status Project: All Default Value: 1b Amp muted This read-only bit reflects the mute status of the amplifier | | | | | |
| | Value | Name | Description | Project | | |
| | 0b | Amp not muted | Amp not muted | All | | |
| | 1b | Amp muted | Amp muted | All | | |
| 15 | Reserved | Project: All | | Format: | | |



| 4 | Port_D_O | out_Enable | | | | | | |
|----|---|---|--|---|--|--|--|--|
| | Project: All | | | | | | | |
| | Default Va | alue: 1 | b Audio is Enabled | | | | | |
| | This bit reflects the state of the output path of the Pin Widget. | | | | | | | |
| | Value Name | | Description | Project | | | | |
| | 0b | Disable | Audio is Disabled | All | | | | |
| | 1b | Enable | Audio is Enabled | All | | | | |
| 3 | Port_C_O | out_Enable | | | | | | |
| | Project: | A | All | | | | | |
| | Default Va | alue: 1 | b Audio is Enabled | | | | | |
| | This bit reflects the state of the output path of the Pin Widget. | | | | | | | |
| | Value Name | | Description | Project | | | | |
| | 0b Disable | | Audio is Disabled | All | | | | |
| | 1b | Enable | Audio is Enabled | All | | | | |
| 2 | Port_B_O | out_Enable | | | | | | |
| | Project: | A | All | | | | | |
| | Default Value: 1b Audio is Enabled | | | | | | | |
| | Default Va | alue: 1 | | | | | | |
| | | | the output path of the Pin Widget. | | | | | |
| | | | the output path of the Pin Widget. Description | Project | | | | |
| | This bit ref | flects the state of | | Project All | | | | |
| | This bit ref | flects the state of Name | Description | | | | | |
| .8 | This bit ref Value 0b 1b | flects the state of Name Disable Enable | Description Audio is Disabled | All | | | | |
| :8 | This bit ref Value 0b 1b Convertor Represent | Image: state of state of state of Disable Disable Enable rB_Stream_ID ts the link stream ID D and Stream ID | Description Audio is Disabled Audio is Enabled | All All Put. This value is set in the | | | | |
| | This bit ref Value 0b 1b Convertor Represent Channel II (stream 0) | Image: state of state of state of Disable Disable Enable rB_Stream_ID ts the link stream ID D and Stream ID | Description Audio is Disabled Audio is Enabled Project: All Format: used by the converter for data input or out | All All Put. This value is set in the | | | | |
| :8 | This bit ref Value 0b 1b Convertor Represent Channel II (stream 0) Convertor Represent | Image: state of of state of state of state of of state of stat | Description Audio is Disabled Audio is Enabled Project: All Format: used by the converter for data input or out through the Set Audio Output Converter W | All All All All Vidget command. Default = 0 | | | | |



| 1 | Converte | or_B_Dige | n | | | | | | |
|---|---|-----------|---|---|----------|--|--|--|--|
| | Project: | | All | | | | | | |
| | Default V | alue: | 1b | Digital Transmission Enabled | | | | | |
| | Enables digital transmission through this node. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. | | | | | | | | |
| | Value | Name | Description | | Project | | | | |
| | Ob | Block | Digital data is bl the state | locked from passing through the node, regardless of | All | | | | |
| | 1b | Pass | Digital data can | pass through the node (Default) | All | | | | |
| 0 | Converte | or_A_Dige | n | | | | | | |
| | Project: | | All | | | | | | |
| | Default V | alue: | 1b | Digital Transmission Enabled | | | | | |
| | | | smission through th onverter Widget co | nis node. This value is set in the Digital Converter 2 thrommand. | ough the | | | | |
| | Value | Name | Description | | Project | | | | |
| | Ob Block Digital data is blocked from passing through the node, regardless of the state | | locked from passing through the node, regardless of | All | | | | | |
| | 1b | Pass | | pass through the node (Default) | All | | | | |

4.2.10 AUD_OUT_DIG_CNVT_A—Audio Digital Converter – Conv A

| AUD_OUT_DIG_CNVT_A—Audio Digital Converter – Conv A | | | | | | | |
|---|-------|-------------|--------|-----|-----|---------|--|
| Register Type: | | /MIO | | | | | |
| Address Of | fset: | 2080 | h | | | | |
| Project: | | dl | | | | | |
| Security: | I | ebug | | | | | |
| Default Valu | le: (| 0000 | 001h | | | | |
| Access: | I | Read (| Only | | | | |
| Size (in bits | s): : | 2 | | | | | |
| These values are returned from the device as the Digital Converter response to a Get Audio Output Converter Widget command. | | | | | | | |
| Bit | | Description | | | | | |
| 31:24 | Reser | /ed | Projec | ct: | All | Format: | |



| | AUD | _001_010_011 | IVT_A—Audio Digital Converter – C | | | | | |
|-------|--|--|---|-------------------------------------|--|--|--|--|
| 23:20 | Stream_ID | | Project | | | | | |
| | Represents the link stream used by the converter for data input or output. This value is set in Channel ID and Stream ID through the Set Audio Output Converter Widget command. Default (stream 0) | | | | | | | |
| 19:16 | Lowest_C | hannel_Number | Project | All Format: | | | | |
| | Represents the lowest channel used by the converter. This value is set in the Channel ID and Stream ID through the Set Audio Output Converter Widget command. Default = 0 | | | | | | | |
| 15 | Reserved | ved Project: All Format: | | | | | | |
| 14:8 | Category_ | Code | Project | All Format: | | | | |
| | | C Category Code. Th Widget command. D | nis value is set in the Digital Converter 1 through the fault = 0 | ne Set Audio Output | | | | |
| 7 | Level | | Project | All Format: | | | | |
| | | C Generation Level. Widget command. D | This value is set in the Digital Converter 2 through befault = 0 | the Set Audio Output | | | | |
| 6 | PRO | | | | | | | |
| | Project: | All | | | | | | |
| | Default Val | lue: 0b | | | | | | |
| | This bit indicates professional or consumer use of channel. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. This value can only be set to 1 if the Pro Allowed bit is set in the audio configuration register. | | | | | | | |
| | Value | Name | Description | Project | | | | |
| | 0b | Consumer | Consumer use | All | | | | |
| | 1b | Professional | Professional use | All | | | | |
| 5 | Non-Audio | | | | | | | |
| | Project: | All | | | | | | |
| | Default Value: 0b | | | | | | | |
| | Data is non PCM format. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. | | | | | | | |
| | | | Description | Project | | | | |
| | Value | Name | Description | | | | | |
| | Value 0b | PCM | Data is PCM | All | | | | |
| | | | | | | | | |
| 4 | 0b | PCM | Data is PCM | All | | | | |
| 4 | 0b 1b | PCM | Data is PCM | All | | | | |
| 4 | 0b 1b Copy | PCM Non PCM All | Data is PCM | All | | | | |
| 4 | 0b 1b Copy Project: Default Val | PCM Non PCM All lue: 0b asserted. This value | Data is PCM | All | | | | |
| 4 | 0b 1b Copy Project: Default Val Copyright a | PCM Non PCM All lue: 0b asserted. This value | Data is PCM Data is non PCM format | All | | | | |
| 4 | 0b 1b Project: Default Val Copyright a Widget cor | PCM Non PCM All lue: 0b asserted. This value nmand. | Data is PCM Data is non PCM format is set in the Digital Converter 2 through the Set And International Converter 2 through the Set And Internation Converter 2 through the Set And Internation Converte | All All udio Output Converter | | | | |



| 3 | PRE | | | | | | |
|---|--|----------|-------------------------------|---------|--|--|--|
| | Project: | All | | | | | |
| | Default Va | lue: 0b | | | | | |
| | Filter preemphasis. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. | | | | | | |
| | Value | Name | Description | Project | | | |
| | 0b | Disabled | Preemphasis is disabled | All | | | |
| | 1b | Enabled | Filter preemphasis is enabled | All | | | |
| 2 | VCFG Project: All Format: | | | | | | |
| | Validity Configuration. Determines S/PDIF transmitter behavior when data is not being transmitted. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Default = 0 | | | | | | |
| 1 | V Project: All Format: | | | | | | |
| | Affects the validity flag transmitted in each subframe, and enables the S/PDIF transmitter to maintain connection during error or mute conditions. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Default = 0 | | | | | | |
| | | | et command. Default = 0 | | | | |

4.2.11 AUD_OUT_DIG_CNVT_B—Audio Digital Converter – Conv B

| | A | UD_C | DUT_DIG_ | | T_B—Audi | o Digita | l Conver | ter – Co | nv l | В |
|-----------------|-------|----------|--------------|--------|----------------|------------|------------|------------|-------|---------|
| Register T | ype: | MMIO | | | | | | | | |
| Address Offset: | | E2180h | ı | | | | | | | |
| Project: | | All | | | | | | | | |
| Security: | | Debug | | | | | | | | |
| Default Value: | | 000000 | 01h | | | | | | | |
| Access: | | Read O | Only | | | | | | | |
| Size (in bits): | | 32 | | | | | | | | |
| | | | | device | as the Digital | Converte | r response | to a Get A | Audic | Output |
| Converter | Widge | t comm | and. | | | | | | | |
| Bit | | | | | De | escription | | | | |
| 31:24 | Rese | erved | Project: | All | | | | Format: | | |
| 23:20 | Strea | am_ID | | | | | | Project: | All | Format: |
| | See | Conv A c | description. | | | | | | | |
| 19:16 | Lowe | est_Cha | nnel_Numbe | er | | | | Project: | All | Format: |
| | See | Conv A c | description | | | | | | | |



| 15 | Reserved | Project: A | .11 | Format | : | |
|------|--|----------------------------------|-------------------------------|----------|-------------|--|
| 14:8 | Category See Conv | _ Code A description | | Project: | All Format: | |
| 7 | Level See Conv | A description | | Project: | All Format: | |
| 6 | PRO Project: Default Va See Conv | All Ilue: 0b A description | | | | |
| | Value | Name | Description | iption | | |
| | 0b | Consumer | Consumer use | | All | |
| | 1b | Professional | Professional use | | All | |
| | | A description. | | | Γ | |
| | Value | Name | Description | | Project | |
| | 0b | PCM | Data is PCM | | All | |
| | 1b | Non PCM | Data is non PCM format | | All | |
| 4 | Copy Project: Default Va See Conv | All Iue: 0b A description | | | | |
| | Value | Name | Description | | Project | |
| | 0b | Not Asserted | Copyright is not asserted | | All | |
| | 1b | Asserted | Copyright is asserted | | All | |
| 3 | PRE Project: Default Va See Conv | All Ilue: 0b A description | | | | |
| | Value | Name | Description | | Project | |
| | 0b | Disabled | Preemphasis is disabled | | All | |
| | 1b | Enabled | Filter preemphasis is enabled | | All | |
| | | | | | | |



| | AUD_OUT_DIG_CNVT_B—Audio Digital Converter – Conv B | | | | | | | | |
|---|---|----------------------|--|--|--|--|--|--|--|
| 1 | V See Conv A description | Project: All Format: | | | | | | | |
| 0 | Reserved Project: All | Format: MBZ | | | | | | | |



4.2.12 AUD_OUT_CH_STR—Audio Channel ID and Stream ID

| | AUD_OUT_CH_STR—Audio Channel ID and Stream II |) | |
|--------------|--|-----------------|--------|
| Register Ty | /pe: MMIO | | |
| Address O | - | | |
| Project: | All | | |
| Security: | Debug | | |
| Default Val | ue: 0000000h | | |
| Access: | Read Only | | |
| Size (in bit | · · · · · · · · · · · · · · · · · · · | | |
| | es are returned from the device as the Channel ID and Stream ID response to overter Widget command. | a Get Audic |) |
| Bit | Description | | |
| 31:24 | Reserved Project: All Format: | | |
| 23:20 | Converter_Channel_MAP_PORTD | Project: | All |
| | The number in this field reflects the HD audio channel to which the Digital Display Au 19:16 is mapped. This field is read only | idio channel in |) bits |
| 19:16 | Digital_Display_Audio_Index_PORTD | Project: | All |
| | This field is the Digital Display Audio channel number. When these bits are written, to number assigned to the Digital Display Audio channel number are reflected in bits 20 register. | | inel |
| 15:12 | Converter_Channel_MAP_PORTC | Project: | All |
| | The number in this field reflects the HD audio channel to which the Digital Display Au 11:8 is mapped. This field is read only | udio channel in | ı bits |
| 11:8 | HDMI_Index_PORTC | Project: | All |
| | This field is the Digital Display Audio channel number. When these bits are written, to number assigned to the Digital Display Audio channel number are reflected in bits 12 register. | | inel |
| 7:4 | Converter_Channel_MAP_PORTB | Project: | All |
| | The number in this field reflects the HD audio channel to which the Digital Display Au 3:0 is mapped. This field is read only | udio channel in | ı bits |
| 3:0 | HDMI_Index_PORTB | Project: | All |
| | This field is the Digital Display Audio channel number. When these bits are written, a number assigned to the Digital Display Audio channel number are reflected in bits 4: | | |



4.2.13 AUD_OUT_STR_DESC_A—Audio Stream Descriptor Format – Conv A

| A | UD_OUT | _STR_DESC_A | A-Audio Stream I | Descript | or F | ormat | t – Conv A |
|--------------|--------------|------------------------|----------------------------|------------|--------|--------|-----------------------|
| Register Ty | /pe: MMIC |) | | | | | |
| Address O | ffset: E208 | 4h | | | | | |
| Project: | All | | | | | | |
| Security: | Debu | g | | | | | |
| Default Val | | 0032h | | | | | |
| Access: | | Only | | | | | |
| Size (in bit | | | | | | | |
| | | | e as the Stream Descr | iptor Form | at res | sponse | to a Get Audio Output |
| Converter | Nidget com | mand. | | | | | |
| Bit | | | Descriptio | on | | | |
| 31:29 | Reserved | | | Project: | All | Forma | t: |
| 28:27 | HBR_enab | le | | Project: | All | Forma | t: |
| | This reflect | s the current HBR se | ttings. | | | | |
| 26:21 | Reserved | | | Project: | All | Forma | t: |
| 20:16 | Convertor | Channel_Count | | Project: | All | Forma | t: |
| | This reflect | s the Convertor Char | nnel Count programmed t | hrough HDA | Audio. | | |
| 15 | Reserved | | | Project: | All | Forma | t: |
| 14 | Sample_B | ase_Rate | | | | | |
| | Project: | All | | | | | |
| | Default Val | ue: Ob | 48 kHz | | | | |
| | Sampling b | ase rate of audio stre | eam. This bit is hardwired | d to 0. | | | |
| | Value | Name | Description | | | | Project |
| | 0b | 48 kHz | 48 kHz | | | | All |
| | 1b | 44.1 kHz | 44.1 kHz | | | | All |



| 13:11 | AUD_OU1 | Base_Rate_Mult | | | | |
|-------|---|--|--|---|--|--|
| | Project: | AI | П | | | |
| | Default Value: 000b 48 kHz | | | | | |
| | Audio strea | am sample base r | ate multiple. This field is hardwired to 000. | | | |
| | Value | Name | Description | Project | | |
| | 000b | x1 | x1 (48 kHz/44.1 kHz or less) | All | | |
| | 001b | x2 | x2 (96 kHz, 88.2 kHz, 32 kHz) | All | | |
| | 010b | x3 | x3 (144 kHz) | All | | |
| | 011b | x4 | x4 (192 kHz, 176.4 kHz) | All | | |
| | 1XXb | Reserved | Reserved | All | | |
| 10:8 | Sample_E Project: Default Va | Base_Rate_Diviso Al lue: 00 | | | | |
| 10:8 | Project: Default Va Audio stre | Al lue: 00 am sample base r | II D0b 48 kHz ate divisor. This field is hardwired to 000. | | | |
| 10:8 | Project: Default Va | Al lue: 00 | II D0b 48 kHz ate divisor. This field is hardwired to 000. Description | Project | | |
| 10:8 | Project: Default Va Audio stre | Al lue: 00 am sample base r | II D0b 48 kHz ate divisor. This field is hardwired to 000. | Project All | | |
| 10:8 | Project: Default Va Audio stre | Al lue: 00 am sample base r Name | II D0b 48 kHz ate divisor. This field is hardwired to 000. Description | | | |
| 10:8 | Project: Default Va Audio strea Value 000b | Al lue: 00 am sample base ra Name Div 1 | II D0b 48 kHz ate divisor. This field is hardwired to 000. Description Divide by 1 (48 kHz, 44.1 kHz) | All | | |
| 10:8 | Project: Default Va Audio stree Value 000b 001b | Al lue: 00 am sample base r Name Div 1 Div 2 | II 48 kHz 00b 48 kHz ate divisor. This field is hardwired to 000. Description Divide by 1 (48 kHz, 44.1 kHz) Divide by 2 (24 kHz, 22.05 kHz) | All | | |
| 10:8 | Project: Default Va Audio stree Value 000b 001b 010b | Al lue: 00 am sample base r Name Div 1 Div 2 Div 2 Div 3 | II 48 kHz 00b 48 kHz ate divisor. This field is hardwired to 000. Description Divide by 1 (48 kHz, 44.1 kHz) Divide by 2 (24 kHz, 22.05 kHz) Divide by 3 (16 kHz, 32 kHz) | All All All | | |
| 10:8 | Project: Default Va Audio stree 000b 001b 010b 011b | Al lue: 00 am sample base ra Name Div 1 Div 2 Div 2 Div 3 Div 4 | II 48 kHz 00b 48 kHz ate divisor. This field is hardwired to 000. Description I Divide by 1 (48 kHz, 44.1 kHz) Divide by 2 (24 kHz, 22.05 kHz) Divide by 3 (16 kHz, 32 kHz) Divide by 4 (11.025 kHz) | All All All All All All | | |
| 10:8 | Project: Default Va Audio stree 000b 001b 010b 011b 100b | Al lue: 00 am sample base r Name Div 1 Div 2 Div 2 Div 3 Div 4 Div 5 | II 48 kHz 00b 48 kHz ate divisor. This field is hardwired to 000. Description Divide by 1 (48 kHz, 44.1 kHz) Divide by 2 (24 kHz, 22.05 kHz) Divide by 3 (16 kHz, 32 kHz) Divide by 4 (11.025 kHz) Divide by 5 (9.6 kHz) | All | | |
| 10:8 | Project: Default Va Audio strea 000b 001b 010b 011b 100b 101b | Al lue: 00 am sample base ra Div 1 Div 2 Div 3 Div 4 Div 5 Div 6 | II 48 kHz Dob 48 kHz ate divisor. This field is hardwired to 000. Description Divide by 1 (48 kHz, 44.1 kHz) Divide by 2 (24 kHz, 22.05 kHz) Divide by 3 (16 kHz, 32 kHz) Divide by 4 (11.025 kHz) Divide by 5 (9.6 kHz) Divide by 6 (8 kHz) | All | | |



| 6:4 | Bits_per_ | Sample | | | | |
|--------------|--------------|-------------|---|---------|--|--|
| | Project: All | | | | | |
| | Default Va | lue: | 011b 32 bits | | | |
| | Value | Name | Description | Project | | |
| | 000b | 8 bit | The data will be packed in memory in 8 bit containers on 16 bit boundaries | All | | |
| | 001b | 16 bits | The data will be packed in memory in 16 bit containers on 16 bit boundaries | All | | |
| 100b 20 bits | | 20 bits | The data will be packed in memory in 20 bit containers on 32 bit boundaries | | | |
| | 010b | 24 bits | The data will be packed in memory in 32 bit containers on 32 bit boundaries | All | | |
| | 011b | 32 bits | The data will be packed in memory in 32 bit containers on 32 bit boundaries | All | | |
| | Others | Reserved | Reserved | All | | |
| 3:0 | Number_o | of_Channels | _in_a_Stream | | | |
| | Project: | | All | | | |
| | Default Va | lue: | 0010b 3 channels in each frame | | | |
| | Format: | | U4+1 Binary value plus 1. 0000 = 1, 1111 = 16 | | | |

4.2.14 AUD_OUT_STR_DESC_B—Audio Stream Descriptor Format – Conv B

| A | UD_ | OUT_STR_DESC_B—Audio Stream Descriptor Format – Conv B |
|---------------|--------|--|
| Register Ty | /pe: | MMIO |
| Address Of | ffset: | E2184h |
| Project: | | All |
| Security: | | Debug |
| Default Val | ue: | 0000032h |
| Access: | | Read Only |
| Size (in bits | s): | 32 |
| See Conv A | A desc | cription. |
| Bit | | Description |
| 31:29 | Rese | rved Project: All Format: |



| 8:27 | HBR_enat | ble A description. | | Project: | All | Format | | | |
|-------|-------------------------|------------------------------|------|-------------------------------|------|---------|---------|--|--|
| 26:21 | Reserved | | | Project: | All | Format | | | |
| 20:16 | | Channel Co | unt | Project: | | Format | - | | |
| 20.10 | | A description. | unt | | 7.01 | i onnat | | | |
| 15 | Reserved | | | Project: | All | Format | | | |
| 14 | Sample_B | aca Bata | | 10,000 | 7.01 | 1 onna | | | |
| 14 | Project: | ase_nale | All | | | | | | |
| | Default Va | | 0b | 48 kHz | | | | | |
| | See Conv A description. | | | | | | | | |
| | Value | Name | | Description | | | Project | | |
| | 0b | 48 kHz | | 48 kHz | | | All | | |
| | 1b | 44.1 kHz | | 44.1 kHz | | | All | | |
| 13:11 | Sample_B | Sample_Base_Rate_Mult | | | | | | | |
| | Project: | | All | | | | | | |
| | Default Va | ue: | 000b | 48 kHz | | | | | |
| | See Conv | A description. | | | | | | | |
| | Value | Name | | Description | | | Project | | |
| | 000b | x1 | | x1 (48 kHz/44.1 kHz or less) | | | All | | |
| | 001b | x2 | | x2 (96 kHz, 88.2 kHz, 32 kHz) | | | All | | |
| | 010b | x3 | | x3 (144 kHz) | | | All | | |
| | 011b | x4 | | x4 (192 kHz, 176.4 kHz) | | | All | | |
| | 1XXb | Reserved | | Reserved | | | All | | |



| 10:8 | Sample_ | Base_Ra | te_Divisor | | | | | | |
|------|---------------------------|----------------------------|---|---|------------------|--------|--|--|--|
| | Project: All | | | | | | | | |
| | | Default Value: 000b 48 kHz | | | | | | | |
| | See Conv A description. | | | | | | | | |
| | Value | Name | 9 | Description | Project | | | | |
| | 000b | Div 1 | | Divide by 1 (48 kHz, 44.1 kHz) | All | | | | |
| | 001b | Div 2 | | Divide by 2 (24 kHz, 22.05 kHz) | All | | | | |
| | 010b | Div 3 | | Divide by 3 (16 kHz, 32 kHz) | All | | | | |
| | 011b | Div 4 | | Divide by 4 (11.025 kHz) | All | | | | |
| | 100b | Div 5 | | Divide by 5 (9.6 kHz) | All | | | | |
| | 101b | Div 6 | | Divide by 6 (8 kHz) | All | | | | |
| | 110b | Div 7 | | Divide by 7 | All | | | | |
| | 111b | Div 8 | | Divide by 8 (6 kHz) | All | | | | |
| | | | | L | | | | | |
| 7 | Reserved | l Pro | oject: All | | Format: MBZ | | | | |
| 6:4 | Bits_per_ | _Sample | | | | | | | |
| | Project: | | All | | | | | | |
| | Default V | alue: | 011b | 32 bits | | 1 | | | |
| | Value | Name | Description | 1 | | Projec | | | |
| | 000b | 8 bit | The data wi boundaries | Il be packed in memory in 8 bit contai | ners on 16 bit | All | | | |
| | 001b | 16 bits | The data wi boundaries | The data will be packed in memory in 16 bit containers on 16 bit poundaries | | | | | |
| | 100b | 20 bits | | he data will be packed in memory in 20 bit containers on 32 bit oundaries | | | | | |
| | | | boundaries | | | | | | |
| | 010b | 24 bits | | Il be packed in memory in 24 bit conta | | All | | | |
| | 010b 011b | 24 bits 32 bits | The data wi boundaries | | iners on 32 bit | All | | | |
| | | | The data wi boundaries The data wi | Il be packed in memory in 24 bit conta | iners on 32 bit | | | | |
| 3:0 | 011b others | 32 bits Res. | The data wi boundaries The data wi boundaries | II be packed in memory in 24 bit conta II be packed in memory in 32 bit conta | iners on 32 bit | All | | | |
| 3:0 | 011b others | 32 bits Res. | The data wi boundaries The data wi boundaries Reserved | II be packed in memory in 24 bit conta II be packed in memory in 32 bit conta | iners on 32 bit | All | | | |
| 3:0 | 011b others Number_ | 32 bits Res. | The data wi boundaries The data wi boundaries Reserved nels_in_a_S | II be packed in memory in 24 bit conta II be packed in memory in 32 bit conta Itream | ainers on 32 bit | All | | | |



4.2.14.1 AUD_PINW_CONNLNG_LIST—Audio Connection List

| | | AUI | D_PINW_ | | .NG_L | IST—Audio C | onnection List |
|------------------------|--------|------------|---------------|-------------|-----------|------------------------|--|
| Register T | ype: | MMIO | | | | | |
| Address O | ffset: | E20A8ł | ı | | | | |
| Project: | | All | | | | | |
| Default Val | ue: | 000003 | 02h | | | | |
| Access: | | Read C | Inly | | | | |
| Size (in bit | s): | 32 | | | | | |
| These valu command. | es are | ereturne | ed from the | device as | the Co | nnection List Leng | gth response to a Get Pin Widget |
| Bit | | | | | | Description | |
| 31:16 | Rese | erved | Project: | All | | | Format: |
| 15:8 | Conr | nection_ | List_Entry | Project: | All | Default Value: | 03h |
| | Conn | ection to | Convertor V | Vidget Noc | de 0x03 | | |
| 7 | Long | _Form | | Project: | All | Default Value: | Ob |
| | This | bit indica | ites whether | the items i | n the cor | nnection list are 'lon | g form' or 'short form'. |
| | This | bit is har | dwired to 0 (| items in co | onnection | list are short form) | |
| 6:0 | Conr | nection_ | List_Length | 1 | | Project: | All Default Value: 02h |
| | | wired inp | | | | | his field is 2, there is only one and there is no Connection Select |

4.2.15 AUD_PINW_CONNLNG_SEL—Audio Connection Select

| | | AUD_PINW_CONNLNG_SEL—Audio Co | nnection Se | elec | t |
|------------------------|---------|---|-----------------|-------|----------------|
| Register T | ype: | MMIO | | | |
| Address O | ffset: | E20ACh | | | |
| Project: | | All | | | |
| Default Val | lue: | 0000000h | | | |
| Access: | | Read Only | | | |
| Size (in bit | s): | 32 | | | |
| These valu command. | ies are | returned from the device as the Connection List Len | gth response to | o a G | Bet Pin Widget |
| Bit | | Description | | | |
| 31:24 | Rese | rved | Project: | All | Format: |
| 23:16 | Coni | ection_select_Control_D | Project: | All | Format: |
| | Conr | ection Index Currently Set [Default 0x00], Port D Widget is | set to 0x00 | | |



| | AUD_PINW_CONNLNG_SEL—Audio Connection S | elec | t |
|------|--|------|---------|
| 15:8 | Connection_select_Control_C Project: Connection Index Currently Set [Default 0x00], Port C Widget is set to 0x00 | All | Format: |
| 7:0 | Connection_select_Control_B Project: Connection Index Currently Set [Default 0x00], Port B Widget is set to 0x00 | All | Format: |

4.2.16 AUD_CNTL_ST_A—Audio Control State Register – Transcoder A

| | AUD_C | NTL_ST_A- | -Audio Control Sta | te Register – Transcoder A |
|---|---------------------------------------|---|--------------------|--|
| Register Ty Address O Project: Default Val Access: Size (in bits | ffset: E206 All ue: 0000 R/W | 34h 95400h | | |
| Bit | | | Descrip | otion |
| 31 | Reserved | Project: | All | Format: MBZ |
| 30:29 | is disabled | All Read lue: 00b only bit reflects wh . If one or more a | | it the DIP data. This can only change when DIP is enabled and audio is enabled on a digital port, irected. |
| | Value | Name | Description | Project |
| | 00b | Reserved | Reserved | All |
| | 01b | Digital Port B | Digital Port B | All |
| | 10b | Digital Port C | Digital Port C | All |
| | 11b | Digital Port D | Digital Port D | All |
| 28:25 | Reserved | Project: | All | Format: MBZ |



| 4:21 | DIP_type_ | enable_status | 5 | | | | |
|------|--------------------------------------|------------------------------------|--|-----------------------------|--|--|--|
| | Project: | | All | | | | |
| | Access: | | Read Only | | | | |
| | Default Val | ue: | 0000b | | | | |
| | periods, the DIP is guarant | | types enabled. It can be updated while the port is enabled. Within 2 vblan iteed to have been transmitted. Disabling a DIP type results in setting the r to zero. A reserved setting reflects a disabled DIP. | | | | |
| | Value | Name | Description | Project | | | |
| | XXX0b | Disable | Audio DIP disabled | All | | | |
| | XXX1b | Enable | Audio DIP enabled | All | | | |
| | XX0Xb | Disable | Generic 1 (ACP) DIP disabled | All | | | |
| | XX1Xb | Enable | Generic 1 (ACP) DIP enabled | All | | | |
| | X0XXb | Disable | Generic 2 DIP disabled | All | | | |
| | X1XXb | Enable | Generic 2 DIP enabled, can be used by ISRC1 or ISRC2 | All | | | |
| | 1XXXb | Reserved | Reserved | All | | | |
| 0:18 | DIP_buffer | r_index | | | | | |
| | Project: | | All | | | | |
| | Default Val | ue: | 0000b | | | | |
| | | | ead of different DIPs, and during read or write of ELD data. The respective DIP or ELD buffers. When the index is not valid, the or | | | | |
| | | l return all 0's. | | | | | |
| | | | Description | Project | | | |
| | the DIP wil | l return all 0's. | 1 | | | | |
| | the DIP wil | l return all 0's. | Description | Project | | | |
| | the DIP wil Value 000b | l return all 0's. Name Audio | Description Audio DIP (31 bytes of address space, 31 bytes of data) Generic 1 (ACP) Data Island Packet (31 bytes of address | All | | | |
| | the DIP wil Value 000b 001b | I return all 0's. Name Audio Gen 1 | Description Audio DIP (31 bytes of address space, 31 bytes of data) Generic 1 (ACP) Data Island Packet (31 bytes of address space, 31 bytes of data) Generic 2 (ISRC1) Data Island Packet (31 bytes of address | Project All All | | | |



| 17:16 | DIP_transmission_frequency | | | | | | |
|-------|------------------------------|---------------------|--|-----------------------|------------------------------|---------------|--|
| | Project: | | All | | | | |
| | Access: Read Only | | | | | | |
| | Default Value: 00b | | | | | | |
| | | | ency of DIP transmission for the value is also latched when the | | | | |
| | When rea 20:18. | d, this value refle | cts the DIP transmission frequ | ency for the | DIP buffer desig | nated in bits | |
| | Value | Name | Description | | | Project | |
| | 00b | Disable | Disabled | | | All | |
| | 01b | Reserved | Reserved | | | All | |
| | 10b Send Once Send Once | | | | | All | |
| | 11b | Best Effort | Best effort (Send at least ev | ery other vs | ync) | All | |
| 15 | Reserved | | | Project: | All Format: | MBZ | |
| 14:10 | ELD_buff 10101 = T | — | he size of the ELD buffer in DV | Project: NORDs (84 | All Access: Bytes of ELD) | Read Only | |
| 9:5 | ELD_acce | ess_address | | Project: | | All | |
| | when incre | emented past the | ss for access to the ELD buffe max addressing value 0x1F. Id value indicates the current a | This field ch | nange takes effect | | |
| 4 | ELD_ACK | K | | Project: | | All | |
| | Acknowled | dgement from the | audio driver that ELD read ha | is been com | pleted | | |
| 3:0 | DIP_RAM | _access_addres | S | Project: | | All | |
| | increment | ed past the max | ss for access to the DIP buffer addressing value of 0xF. This ue indicates the current acces | field change | | | |



4.2.17 AUD_CNTL_ST_B—Audio Control State Register – Transcoder B

| Register T Address C Project: Default Va Access: Size (in bi | Offset: E21E All Iue: 0000 R/W | | | | | | |
|---|---|----------------|--|---------|--|--|--|
| Bit | | | Description | | | | |
| 31 | Reserved Project: All Format: M | | | | | | |
| 30:29 | DIP_Port_ | Select | | | | | |
| | Project: | AI | I | | | | |
| | Access: | Re | ead Only | | | | |
| | Default Val | | | | | | |
| | See Transcoder A description. | | | | | | |
| | Value | Name | Description | Project | | | |
| | 00b | Reserved | Reserved | All | | | |
| | 01b | Digital Port B | Digital Port B | All | | | |
| | 10b | Digital Port C | Digital Port C | All | | | |
| | 11b | Digital Port D | Digital Port D | All | | | |
| 28:25 | Reserved | Project: | All Format: | MBZ | | | |
| 24:21 | DIP_type_ | enable_status | 3 | | | | |
| | Project: | | All | | | | |
| | Access: | | Read Only | | | | |
| | Default Val | | 0000b | | | | |
| | See Transcoder A description. | | | | | | |
| | Value | Name | Description | Project | | | |
| | XXX0b | Disable | Audio DIP disabled (Default) | All | | | |
| | XXX1b | Enable | Audio DIP enabled | All | | | |
| | XX0Xb | Disable | Generic 1 (ACP) DIP disabled | All | | | |
| | XX1Xb | Enable | Generic 1 (ACP) DIP enabled | All | | | |
| | X0XXb | Disable | Generic 2 DIP disabled | All | | | |
| | X1XXb | Enable | Generic 2 DIP enabled, can be used by ISRC1 or ISRC2 | All | | | |
| | 1XXXb | Reserved | Reserved | All | | | |



| 20:18 | DIP_buffer_index | | | | | | |
|------------------------|---|--|---|---|--|--|--|
| | Project: All | | | | | | |
| | Default Value: 000b | | | | | | |
| | See Trans | coder A descrip | tion. | | | | |
| | Value | Name | Description | Project | | | |
| | 000b | Audio | Audio DIP (31 bytes of address space, 31 bytes of data) | All | | | |
| | 001b | Gen 1 | Generic 1 (ACP) Data Island Packet (31 bytes of address space, 11 bytes of data) | All | | | |
| | 010b | Gen 2 | Generic 2 (ISRC1) Data Island Packet (31 bytes of address space, 31 bytes of data) Generic 3 (ISRC2) Data Island Packet (31 bytes of address space, 31 bytes of data) | | | | |
| | 011b | Gen 3 | | | | | |
| | 1XXb | 1XXb Reserved Reserved | | | | | |
| | Project: Access: Default Va | | All Read Only 00b | | | | |
| | Access: Default Va See Trans | lue: scoder A descrip | Read Only 00b otion | Burling | | | |
| | Access: Default Va See Trans Value | lue: scoder A descrip Name | Read Only 00b otion Description | Project | | | |
| | Access: Default Va See Trans Value 00b | lue: scoder A descrip Name Disable | Read Only 00b otion Description Disabled | All | | | |
| | Access: Default Va See Trans Value 00b 01b | lue: scoder A descrip Name Disable Reserved | Read Only 00b otton Description Disabled Reserved | All | | | |
| | Access: Default Va See Trans Value 00b 01b 10b | lue: scoder A descrip Name Disable | Read Only 00b otion Description Disabled Reserved Send Once | All All All | | | |
| | Access: Default Va See Trans Value 00b 01b | lue: scoder A descrip Name Disable Reserved | Read Only 00b otton Description Disabled Reserved | All | | | |
| 15 | Access: Default Va See Trans Value 00b 01b 10b | lue: scoder A descrip Name Disable Reserved Send Once | Read Only 00b otion Description Disabled Reserved Send Once Best effort (Send at least every other vsync) | All All All | | | |
| - | Access: Default Va See Trans Value 00b 01b 10b 11b Reserved ELD_buffe | lue: scoder A descrip Disable Reserved Send Once Best Effort | Read Only 00b ottion Description Disabled Reserved Send Once Best effort (Send at least every other vsync) Project: All Format: | All All All All All | | | |
| 4:10 | Access: Default Va See Trans Value 00b 01b 10b 11b Reserved ELD_buffe 10101 = T | lue: scoder A descrip Disable Reserved Send Once Best Effort | Read Only OUb Disabled Description Disabled Reserved Send Once Best effort (Send at least every other vsync) Project: All Format: Project: All Access: the size of the ELD buffer in DWORDs (84 Bytes of ELD) Project: | AII AII AII AII MBZ | | | |
| 15 4:10 9:5 4 | Access: Default Va See Trans Value 00b 01b 10b 11b Reserved ELD_buffe 10101 = T ELD_acce See Trans ELD_ACK | lue: Scoder A descrip Name Disable Reserved Send Once Best Effort er_size his field reflects ess_address coder A descrip | Read Only 00b otion | All All All All All MBZ Read Only | | | |



4.2.18 AUD_CNTL_ST2— Audio Control State 2

| | | AU | D_CNTL_ST2— Audio Control State 2 | |
|---|-------------------------------------|--|---|------------|
| Register Ty Address O Project: Default Val | ffset: E20 All | | | |
| Access: Size (in bit | R/V | | | |
| This registe each port, l when the E | er is used ELD readi LD or CP | ness is sen | aking between the audio and video drivers for interrupt managen t by the display software to the audio software via an unsolicited set. Display software sets these bits as part of enabling the res rt. | response |
| Bit | | | Description | |
| 31:10 | Reserved | Project: | All Format: | |
| 9 | | alue: bit reflects ti | All 0b he state of CP request from the audio unit. When an audio CP request set to 1 by the video software to indicate that the CP request has been | |
| | Value | Name | Description | Project |
| | 0b | Pending or Not Ready | CP request pending or not ready to receive requests | All |
| | 1b | Ready | CP request ready | All |
| 8 | video soft or on a ho | alue: bit reflects th ware must s otplug event, | All Ob he state of the ELD data written to the ELD RAM. After writing the ELD et this bit to 1 to indicate that the ELD data is valid. At audio codec initi this bit is set to 0 by the video software. This bit is reflected in the audio e ELD valid status bit. | alization, |
| | Value | Name | Description | Project |
| | 0b | Invalid | ELD data invalid (default, when writing ELD data, set 0 by software) | All |
| | 1b | Valid | ELD data valid (Set by video software only) | All |
| | | | | |



| 5 | CP_Read | lyC | | | | | |
|-----|--|--|--|-----------------------|--|--|--|
| | Project: All | | | | | | |
| | Default Value: 0b | | | | | | |
| | See CP_ | ReadyD de | scription. | | | | |
| | Value | Name | Description | Project | | | |
| | 0b | Not Read | ly CP request pending or not ready to receive requests | All | | | |
| | 1b | Ready | CP request ready | All | | | |
| 4 | ELD_vali | idC | | | | | |
| | Project: | | All | | | | |
| | Default V | alue: | Ob | | | | |
| | See ELD | _validD des | scripion. | | | | |
| | Value | Name | Description | Project | | | |
| | 0b | Invalid | ELD data invalid (default, when writing ELD data, set 0 by software) | All | | | |
| | 1b | 1b Valid ELD data valid (Set by video software only) | | | | | |
| 3:2 | Reserved | d Proje | ect: All Format: | | | | |
| 1 | CP_Read | łуВ | | | | | |
| | Project: All | | | | | | |
| | Default V | alue: | Ob | | | | |
| | See CP_ReadyD description. | | | | | | |
| | Value | Name | Description | Project | | | |
| | 0b | Not Read | ly CP request pending or not ready to receive requests | All | | | |
| | 1b | Ready | CP request ready | All | | | |
| | | | | | | | |
| 0 | ELD_vali | idB | | | | | |
| 0 | | dB | All | | | | |
| 0 | ELD_vali | | All Ob | | | | |
| 0 | ELD_vali Project: Default V | | Ob | | | | |
| 0 | ELD_vali Project: Default V | alue: | Ob | Project | | | |
| 0 | ELD_vali Project: Default V See ELD | alue: _validD des | Ob scripion. | Project All | | | |



| | AUD_HDMIW_STATUS—Audio HDMI Status |
|--|---|
| Register T Address C Project: Security: Default Va Access: Size (in bi | iffset: E20D4h All Debug Iue: 0000000h R/W Clear R/W Clear |
| Bit | Description |
| 31 | Conv_B_CDCLK/DOTCLK_FIFO_Underrun Project: All This bit indicates an underrun in the FIFO inside the clock crossing logic between CDCLK and DOTCLK. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO. |
| 30 | Conv_B_CDCLK/DOTCLK_FIFO_Overrun Project: All This bit indicates an overrun in the FIFO inside the clock crossing logic between CDCLK and DOTCLK. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO. |
| 29 | Conv_A_CDCLK/DOTCLK_FIFO_Underrun Project: All This bit indicates an underrun in the FIFO inside the clock crossing logic between CDCLK and DOTCLK. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO. |
| 28 | Conv_A_CDCLK/DOTCLK_FIFO_Overrun Project: All This bit indicates an overrun in the FIFO inside the clock crossing logic between CDCLK and DOTCLK. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO. |
| 27:26 | Reserved Project: All Format: |
| 25 | BCLK/CDCLK_FIFO_Overrun Project: All This bit indicates an overrun in the FIFO inside the clock crossing logic between BCLK and CDCLK. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO. |
| 24 | Function_Reset Project: All Security: Debug This bit indicates that an audio function reset occurred through the reset signal on the HD audio bus. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO. |
| 23:0 | Reserved Project: All Format: |

4.2.19 AUD_HDMIW_STATUS—Audio HDMI Status



4.2.20 AUD_HDMIW_HDMIEDID_A—HDMI Data EDID Block – Transcoder A

| AU | D_HDMIW_HDMIEDID_A—HDMI Data EDID Block – Transcoder A |
|---|--|
| Register Type: | MMIO |
| Address Offse | t: E2050h |
| Project: | All |
| Default Value: | 0000000h |
| Access: | R/W |
| Size (in bits): | 32 |
| the structure to must not write specification. These values a HDMI Widget o Writing sequen - Video to be - Video with has h - Pleas that f Reading seque - Video - Video with e | nce: o software sets ELD invalid, and sets the ELD access address to 0, or to the desired DWORD written. o software writes ELD data 1 DWORD at a time. The ELD access address autoincrements each DWORD write, wrapping around to address 0 when the max buffer address size of 0xF been reached. Please note that software must write an entire DWORD at a time. Se note that the audio driver checks the valid bit with each byte read of the ELD. This means the video driver can unilaterally write ELD irrespective of audio driver ELD read status. |
| Bit | Description |
| 31:0 E | DID_HDMI_Data_Block Project: All Format: |
| Ple | ease note that the contents of this buffer are not cleared when ELD is disabled. The contents of this ffer are cleared during gfx reset |



4.2.21 AUD_HDMIW_HDMIEDID_B—HDMI Data EDID Block – Transcoder B

| A | UD_ | | | DID_I | B—HD | MI Dat | a EDID | Block – T | rans | coder B | |
|-----------------|--------|--------------|---------------|-------|------|--------|--------|-----------|------|---------|--|
| Register Type: | | MMIO | | | | | | | | | |
| Address Offset: | | E2150h | | | | | | | | | |
| Project: | | All | | | | | | | | | |
| Default Valu | ie: | 00000000h | | | | | | | | | |
| Access: | | R/W | | | | | | | | | |
| Size (in bits |): | 32 | | | | | | | | | |
| See Transco | oder / | A descriptic | n. | | | | | | | | |
| Bit | | | | | | Descri | otion | | | | |
| 31:0 | EDID | _HDMI_Dat | a_Block | | | | | Project: | All | Format: | |
| | See 7 | Franscoder A | A description | | | | | | | | |

4.2.22 AUD_HDMIW_INFOFR_A—Audio Widget Data Island Packet – Transcoder A

| AUD_HD | MIW_INFOFR_A—Audio Widget Data Island Packet – Transcoder A |
|--------------------|--|
| Register Type: | MMIO |
| Address Offset: | E2054h |
| Project: | All |
| Default Value: | 0000000h |
| Access: | Read Only |
| Size (in bits): | 32 |
| When the IF type | e or dword index is not valid, the contents of the DIP will return all 0's. |
| These values are | e programmed by the audio driver in an HDMI Widget Set command. They are returned one |
| byte at a time fro | om the device on the HD audio bus as the HDMI DIP response to a Get HDMI Widget |
| | etch a specific byte, the audio driver should send an HDMI Widget HDMI DIP Index Pointer |
| | set the index, then fetch the indexed byte using the HDMI DIP get. |
| Video driver read | d sequence (for debug only): |
| Video software s | ate DIP type to the appropriate DIP, and gets the DIP access address to the desired |

Video software sets DIP type to the appropriate DIP, and sets the DIP access address to the desired DWORD.

Video software reads DIP data 1 DWORD at a time. The DIP access address auto increments with each DWORD write, wrapping around to address 0 when the max buffer address size of 0xF has been reached.



| AU | D_HDMIW_INFOFR_A—Audio Widget D | Data Island Pacl | ket – ⁻ | Transcoder A | |
|------|--|------------------|--------------------|----------------------|--|
| Bit | Description | | | | |
| 31:0 | Data_Island_Packet_Data | Project: | All | Format: | |
| | This reflects the contents of the DIP indexed by the Dare cleared during function reset or HD audio link res | | The con | tents of this buffer | |

4.2.23 AUD_HDMIW_INFOFR_B—Audio Widget Data Island Packet – Transcoder B

| AUD | D_HD | MIW_INFOFR_B—Audio | o Widget Dat | a Island Pack | et – 1 | Franscoder B |
|--------------|---------|---------------------------|--------------|---------------|--------|--------------|
| Register T | ype: | MMIO | | | | |
| Address O | ffset: | E2154h | | | | |
| Project: | | All | | | | |
| Default Val | lue: | 0000000h | | | | |
| Access: | | Read Only | | | | |
| Size (in bit | s): | 32 | | | | |
| See Transo | coder . | A description. | | | | |
| Bit | | | Descripti | ion | | |
| 31:0 | Data | _Island_Packet_Data | | Project: | All | Format: |
| | See | Transcoder A description. | | | | |

4.3 DPB Control and Aux Channel

4.3.1 DPB—DisplayPort B Control Register

| Register Type: | DPB—DisplayPort B Control Register | | | | |
|---|------------------------------------|--|--|--|--|
| • • | | | | | |
| Address Offset: | E4100h | | | | |
| Project: | All | | | | |
| Default Value: | 0000018h | | | | |
| Access: | R/W | | | | |
| Size (in bits): | 32 | | | | |
| Double Buffer Update Point: | Depends on bit | | | | |
| Please note that DisplayPort B uses the same lanes as HDMIB. Therefore +B/HDMIB and DisplayPort B | | | | | |
| cannot be enabled simultaned | busly. | | | | |



| | | DPB | — C | DisplayPort B Control Register | | | | |
|-----|---|------------------------------|------------|---|----------|--|--|--|
| Bit | | | | Description | | | | |
| 31 | DisplayPort_B_Enable | | | | | | | |
| | Project: | | All | | | | | |
| | Default Valu | ne: | 0b | | | | | |
| | Disabling th being writte | | it in i | its lowest power state. Port enable takes place on the Vbla | nk after | | | |
| | [DevIBX] When disabling the port, software must temporarily enable the port with transcoder select (bit #30) cleared to '0' after disabling the port. This is workaround for hardware issue where the transcoder select set to '1' will prevent HDMIB from being enabled on transcoder A. | | | | | | | |
| | Value | Name | Des | scription | Project | | | |
| | 0b | Disable | Dis | able and tristates the Display Port B interface | All | | | |
| | 1b | Enable | Ena | able. This bit enables the Display Port B interface | All | | | |
| 30 | Transcode | r_Select | | | | | | |
| | Project: | | All | | | | | |
| | Default Valu | ne: | 0b | 0b | | | | |
| | This bit determines from which display transcoder the source data will originate. Transcoder selection takes place on the Vblank after being written | | | | | | | |
| | [DevIBX] W that this bit port on tran | t is required enable this | | | | | | |
| | Value | Name | | Description | Project | | | |
| | 0b | Transcoder A | A | Transcoder A | All | | | |
| | 1b | Transcoder I | В | Transcoder B | All | | | |
| | | 1 | | | | | | |



| 29:28 | Link_training_pattern_enable | | | | | | | |
|-------|---|-----------|--|-------------|--|--|--|--|
| | Project: All | | | | | | | |
| | Default V | alue: | 0b | | | | | |
| | | | link initialization as defined in the DisplayPort specification. Pleas ifigured prior to sending training patterns. | e note that | | | | |
| | When enabling the port, it must be turned on with pattern 1 enabled. When retraining a link, the port must be disabled, then re-enabled with pattern 1 enabled. | | | | | | | |
| | Value | Name | Description | Project | | | | |
| | 00b | Pattern 1 | Pattern 1 enabled: Repetition of D10.2 characters | All | | | | |
| | 01b | Pattern 2 | Pattern 2 enabled: Repetition of K28.5, D11.6, K28.5, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2. Please note that the entire pattern must complete before another pattern is sent. Scrambling initialization and disparity init commence at the end of the last iteration of pattern 2. | All | | | | |
| | 10b | Idle | Idle Pattern enabled: Transmit BS followed by VB-ID with NoVideoStream_flag set to 1, five times | All | | | | |
| | 11b | Normal | Link not in training: Send normal pixels | All | | | | |
| 7:25 | Voltage_swing_level_set | | | | | | | |
| | Project: | | All | | | | | |
| | Default V | alue: | 0b | | | | | |
| | | | setting the voltage swing for pattern 1, defined as Vdiff_pp in the I or registers in the PCI express configuration. | DisplayPort | | | | |
| | Value | Name | Description | Project | | | | |
| | 000b | 0.4V | 0.4 V | All | | | | |
| | 001b | 0.6V | 0.6 V | All | | | | |
| | 010b | 0.8V | 0.8 V | All | | | | |
| | 011b | 1.2V | 1.2 V | All | | | | |
| | | 1 | | - | | | | |



| | -1 | | B—DisplayPort B Control Register | | | | | |
|-------|---|---|---|---|--|--|--|--|
| 24:22 | Pre-empl | hasis_level_se | et | | | | | |
| | Project: | | All | | | | | |
| | Default Value: 0b | | | | | | | |
| | | | setting link pre-emphasis for pattern 2, as defined i or registers in the PCI express configuration. | n the DisplayPort | | | | |
| | Value Name | | Description | Project | | | | |
| | 000b | None | No pre-emphasis | All | | | | |
| | 001b | 3.5dB | 3.5dB pre-emphasis (1.5x) | All | | | | |
| | 010b | 6 dB | 6dB pre-emphasis (2x) | All | | | | |
| | 011b | 9.5 dB | 9.5dB pre-emphasis (3x) | All | | | | |
| | 1XXb | Reserved | Reserved | All | | | | |
| 21:19 | Port_wid | Ith_Selection | | | | | | |
| | | elects the numb | All 0b ber of lanes to be enabled on the DisplayPort link. set. Locked once port is enabled. Updates wher | | | | | |
| | Default Va This bit se done as a | elects the numb | 0b per of lanes to be enabled on the DisplayPort link. | | | | | |
| | Default Va This bit se done as a re-enable | elects the numb a part of mode s ed | 0b per of lanes to be enabled on the DisplayPort link. set. Locked once port is enabled. Updates wher | n the port is disabled then | | | | |
| | Default Va This bit se done as a re-enable | elects the numb a part of mode s ed Name | 0b ber of lanes to be enabled on the DisplayPort link. set. Locked once port is enabled. Updates wher Description | h the port is disabled then Project | | | | |
| | Default Va This bit se done as a re-enable Value 000b | elects the numb a part of mode s d Name x1 | 0b ber of lanes to be enabled on the DisplayPort link. set. Locked once port is enabled. Updates when Description x1 Mode | h the port is disabled then Project All | | | | |
| | Default Va This bit se done as a re-enable Value 000b 001b | A part of mode sed Name x1 | Ob Deer of lanes to be enabled on the DisplayPort link. set. Locked once port is enabled. Updates when Description x1 Mode x2 Mode | h the port is disabled then Project All All | | | | |
| 18 | Default Va This bit se done as a re-enable Value 000b 001b 011b 011b 0thers Enhance Project: Default Va This bit se | A part of mode sed Name x1 x2 x4 Reserved | Ob Description x1 Mode x2 Mode Reserved | h the port is disabled then Project All All All All All All | | | | |
| 18 | Default Va This bit se done as a re-enable Value 000b 001b 011b 011b 0thers Enhance Project: Default Va This bit se | A part of mode sed Name x1 x2 x4 Reserved | Ob ber of lanes to be enabled on the DisplayPort link. set. Locked once port is enabled. Updates when Description x1 Mode x2 Mode x4 Mode Reserved | h the port is disabled then Project All All All All All All | | | | |
| 18 | Default Va This bit se done as a re-enable 000b 001b 011b 0thers Enhance Project: Default Va This bit se enabled. | A part of mode sed Name x1 x2 x4 Reserved | Ob ber of lanes to be enabled on the DisplayPort link. set. Locked once port is enabled. Updates when Description x1 Mode x2 Mode x4 Mode Reserved | h the port is disabled then Project All All All All All Locked once port is | | | | |
| 18 | Default Va This bit se done as a re-enable 000b 001b 011b 0thers Enhance Project: Default Va This bit se enabled. Value | A part of mode sed Name X1 X2 X4 Reserved d_Framing_Ei alue: elects enhance Updates whei Name | Ob ber of lanes to be enabled on the DisplayPort link. set. Locked once port is enabled. Updates when Description x1 Mode x2 Mode x4 Mode Reserved nable All Ob d framing. It must be set when HDCP is invoked. In n the port is disabled then re-enabled Description | h the port is disabled then Project All All All All All Locked once port is Project | | | | |



| 15 | Port_reversal | | | | | | | |
|-----|--|--|--|---|--|--|--|--|
| | Project: All | | | | | | | |
| | Default Value: 0b | | | | | | | |
| | reversal is | ne reversal within th not controlled by a hen re-enabled | he port: lane 0 mapped to lane 3, lane 1 strap. Locked once port is enabled. | mapped to lane 2, etc. Port Updates when the port is | | | | |
| | Value | Name Description | | | | | | |
| | 0b | Not Reversed | Port not reversed | All | | | | |
| | 1b | Reversed Port reversed | | | | | | |
| 4:8 | Reserved | Project: A | All | Format: MBZ | | | | |
| 7 | Scrambling Disable | | | | | | | |
| | Project: All | | | | | | | |
| | Security: Debug | | | | | | | |
| | Default Value: 0b | | | | | | | |
| | This bit disables scrambling for DisplayPort | | | | | | | |
| | Value | Name | Description | Project | | | | |
| | 0b | Enable | Scrambling enabled | All | | | | |
| | 00 | Disable Scrambling disabled All | | | | | | |
| | 1b | Disable | Scrambling disabled | All | | | | |
| 6 | 1b | Disable | Scrambling disabled | All | | | | |
| 6 | 1b | | Scrambling disabled | All | | | | |
| 6 | 1b Audio_Ou | tput_Enable | Scrambling disabled | All | | | | |
| 6 | 1b Audio_Ou Project: Default Va This bit en | t put_Enable All lue: 0b | output port. It may be enabled or disab | I | | | | |
| 6 | 1b Audio_Ou Project: Default Va This bit en | t put_Enable All lue: 0b ables audio on this | output port. It may be enabled or disab | I | | | | |
| 6 | 1b Audio_Ou Project: Default Va This bit en complete a | tput_Enable All lue: 0b ables audio on this and set to "Normal." | output port. It may be enabled or disab | led only when the link training | | | | |



| | | | -DisplayPort B Control Register | | | | | | |
|-----|---|-----------------------------------|--|-----------------------|--|--|--|--|--|
| 5 | HDCP_Port_Select | | | | | | | | |
| | - | Project: All Default Value: 0b | | | | | | | |
| | | | - | ort will be encrypted | | | | | |
| | This bit directs HDCP to this port. When enabled, the information sent on this port will be encrypted using HDCP. Please note that this bit does not enable encryption on its own, but must be used in conjunction with HDCP registers. | | | | | | | | |
| | Value | Name | Description | Project | | | | | |
| | 0b | Disable | No HDCP encryption on this port | All | | | | | |
| | 1b | Enable | Enable HDCP on this port | All | | | | | |
| | Program | nming Notes | | | | | | | |
| | HDCP can only be selected on one port at a time, per transcoder. If two or more ports are selected, encryption will be disabled. | | | | | | | | |
| 4:3 | Sync_Pol | arity | | | | | | | |
| | Project: | A | NII | | | | | | |
| | Default Value: 11b VS and HS are active high | | | | | | | | |
| | Indicates the polarity of Hsync and Vsync to be transmitted in MSA | | | | | | | | |
| | Value | Name | Description | Project | | | | | |
| | 00b | Low | VS and HS are active low (inverted) | All | | | | | |
| | 11b | VS Low, HS Hig | h VS is active low (inverted), HS is active high | All | | | | | |
| | 11b | VS High, HS Lov | W VS is active high, HS is active low (inverted) | All | | | | | |
| | 11b | High | VS and HS are active high | All | | | | | |
| 2 | Digital_Display_B_Detected | | | | | | | | |
| | Project: | | NII. | | | | | | |
| | Access: | F | Read Only | | | | | | |
| | Default Value: 0b | | | | | | | | |
| | Read-only bit indicating whether a digital display was detected during initialization. It signifies the level of the GMBUS port 4 (port B) data line at boot. | | | | | | | | |
| | Value | Name | Description | Project | | | | | |
| | | | Digital display not detected during initialization | All | | | | | |
| | 0b | Not Detected | Digital display not detected during initialization | All | | | | | |
| | 0b 1b | Not Detected Detected | Digital display detected during initialization | All | | | | | |



4.3.2 DPB_AUX_CH_CTL—Display Port B AUX Channel Control

| Register 7 Address (Project: Default Va Access: Size (in bi | Diffset: E41 All alue: 000 R/W | 10h 50000h | | | | |
|---|---|---------------------|---|---|--|--|
| Bit | | | Description | | | |
| 31 | Send/Busy Project: All Default Value: 0b Setting this bit to a one initiates the transaction, when read this bit will be a 1 until the transmission completes. The transaction is completed when the response is received or when a timeout occurs. not write a 1 again until transaction completes. Writes of 0 will be ignored. Programming Notes | | | | | |
| 30 | Done | Pr | while Busy bit 31 is asserted. oject: All Access: R/W Cle he transaction has completed. SW n | ear nust write a 1 to this bit to clear the event. | | |
| 29 | Interrupt_on_Done Project: All Format: Enable an interrupt in the hotplug status register when the transaction completes or times out. | | | | | |
| 28 | Time_out A sticky b | | oject: All Access: R/W Cle he transaction has timed out. SW m | ear ust write a 1 to this bit to clear the event. | | |
| 27:26 | Project: Default Va | alue: | All 0b In the 2X bit clock divider (bits 10:0) b | being programmed for 2MHz. | | |
| | Value | Name | Description | Project | | |
| | 00b | 400us | 400us | All | | |
| | 01b | 600us | 600us | All | | |
| | 10b | 800us | 800us | All | | |
| | 11b | 1600us | 1600us | All | | |
| 25 | A sticky b than 20 b | it that indicates t | oject: All Access: R/W Cle hat the data received was corrupted, write a 1 to this bit to clear the event. | ear not in multiples of a full byte, or more | | |



| | | | | | play Port B AUX Channel Control | | | |
|-------|--|---|---|--|--|--------------|--|--|
| 24:20 | the numb done bit is message Reads of The read | is used to i er of bytes s set, and it or the mes this field wi value will r | received in a f timeout or r sage size. Il give the re | a transac receive e sponse r vhile Bus | Format: ber bytes to transmit (including the header). It ction (including the header). This field is valid o error has not occurred. Sync/Stop are not part of message size. sy bit 31 is asserted. d. | nly when the | | |
| 19:16 | Precharg | e_Time | Project: | All | Format: | | | |
| | Default Va | alue: | 0101b | 10us | | | | |
| | Used to d | letermine th | ne precharge | time for | the Aux Channel drivers. | | | |
| | The value 2MHz). | e is the num | nber of micro | seconds | times 2 (assuming 2X bit clock divider program | nmed for | | |
| | Default is | 5 decimal | which gives | 10us of p | precharge. | | | |
| | Example: | Example: | | | | | | |
| | For 10us | precharge, | program 5 (* | 10us/2us | S). | | | |
| 15 | AUX_Aksv_select | | | | | | | |
| | Project: All | | | | | | | |
| | Default Value: 0b | | | | | | | |
| | This bit selects whether some of the data to be written over Display Port AUX comes from the HDCP internal Aksv value for HDCP authentication, or all from the AUX Data registers. | | | | | | | |
| | Set this bit before initiating a transaction to write Aksv to the Display Port sink. All AUX protocol must be followed and Message Size set to 9 bytes. The first DWord transmitted will be from the AUX Data Register 1 for the header, then the 5 byte HDCP Aksv value. The sink response is read back as usual from the AUX Data registers. | | | | | | | |
| | Value | Name | Descrip | tion | | Project | | |
| | 0b | AUX | Use AUX | Use AUX Data registers for regular data transmission | | All | | |
| | 1b | HDCP | Duse HDCP internal Aksv for part of the data transmission | | | | | |
| 14 | Invert_Manchester | | | | | | | |
| | Project: All | | | | | | | |
| | Security: | | | | | | | |
| | Default Va | alue: | 0b | | | | | |
| | Value | Name | Descriptio | n | | Project | | |
| | | | | | | | | |
| | 0b | Normal | Mancheste | er code ri | ising edge mid-clk signifies zero | All | | |



| 13 | Sync_Only_Clock_Recovery | | | | | | | |
|------|--|------------|--|--|---------|--|--|--|
| | Project: All | | | | | | | |
| | Security: Test | | | | | | | |
| | Default Value: 0b | | | | | | | |
| | Value | Value Name | | Description | Project | | | |
| | 0b | Sync and | Data | Recover clock during sync pattern and data phase | All | | | |
| | 1b | Sync Onl | у | Only recover clock during sync pattern | All | | | |
| 12 | Disable_ | De-glitch | | | | | | |
| | Project: | | Al | I | | | | |
| | Security: | | Τe | est | | | | |
| | Default Value: 0b | | | | | | | |
| | Value | Name | Descr | Description | | | | |
| | 0b | Enable | Enable Enable serial input de-glitch logic | | | | | |
| | 1b | Disable | All | | | | | |
| 11 | Double_precharge | | | | | | | |
| | Project: All | | | | | | | |
| | Security: | | | | | | | |
| | Default Value: 0b | | | | | | | |
| | Value | Name | | Description | Project | | | |
| | 0b | Program | ned | Precharge time is as programmed | All | | | |
| | 1b | Doubled | | Precharge time is doubled | All | | | |
| 10:0 | 2X_Bit_Clock_divider Project: All Format: 2*U11 | | | | | | | |
| | Used to determine the 2X bit clock the Aux Channel logic runs on. | | | | | | | |
| | This value divides the input clock frequency down to 2X bit clock rate. The 2X bit clock rate is ideally 2MHz (0.5us). The input clock is the 125mhz rawclk. | | | | | | | |
| | | | | | | | | |
| | Example | | | | | | | |



4.3.3 DPB_AUX_CH_DATA—Display Port B AUX Data Registers

| DP Aux Ch Data Format | | | | | | |
|-----------------------|---|--|--|--|--|--|
| Project: | All | | | | | |
| Bit | Description | | | | | |
| 31:0 | AUX_CH_DATA Project: All | | | | | |
| | A DWord of the message. Writes give the data to transmit during the transaction. The MSbyte is transmitted first. Reads will give the response data after transaction complete. | | | | | |

| | DPI | B_AUX_CH_DA ⁻ | TA—Disp | olay | Port B AU | X Data Registers |
|---------------|----------------|--------------------------|----------------|--------|-------------|-----------------------|
| Register Ty | /pe: MM | 10 | | | | |
| Address Of | fset: E41 | 14h | | | | |
| Project: | All | | | | | |
| Default Val | ue: 000 | 00000h | | | | |
| Access: | R/W | / | | | | |
| Size (in bits | s): 5x3 | 2 | | | | |
| The read va | alue will no | ot be valid while Bus | sy bit 31 is a | assert | ed. | |
| DWord | Bit | | | | Description | |
| 0 | 31:0 | AUX_CH_DATA1 | Project: | All | Format: | DP Aux Ch Data Format |
| 1 | 31:0 | AUX_CH_DATA2 | Project: | All | Format: | DP Aux Ch Data Format |
| 2 | 31:0 | AUX_CH_DATA3 | Project: | All | Format: | DP Aux Ch Data Format |
| 3 | 31:0 | AUX_CH_DATA4 | Project: | All | Format: | DP Aux Ch Data Format |
| 4 | 31:0 | AUX_CH_DATA5 | Project: | All | Format: | DP Aux Ch Data Format |

]



4.4 DPC Control and Aux Channel

4.4.1 DPC—Display Port C Control Register

| | | DPC- | –Display Port C Control Register | | | | | |
|--------------|--|---|--|--|--|--|--|--|
| Register Ty | ype: | MMIC | 0 | | | | | |
| Address O | | E420 | E4200h | | | | | |
| Project: | | All | | | | | | |
| Default Val | lue: | 0000 | 0018h | | | | | |
| Access: | | R/W | Protect | | | | | |
| Size (in bit | - | 32 | | | | | | |
| | ffer Update | | ends on bit | | | | | |
| o this port. | . Please no | | e write protected by Panel Power Sequencer when p Port C uses the same lanes as HDMI. Therefore H nultaneously. | | | | | |
| Bit | | | Description | | | | | |
| 31 | DisplayPo | ort_C_Enable | | | | | | |
| | Project: | | | | | | | |
| | Default Va | Default Value: 0b | | | | | | |
| | See DPB description. | | | | | | | |
| | | ed to '0' after dis | ne port, software must temporarily enable the port with tra abling the port. This is workaround for hardware issue whe HDMIC from being enabled on transcoder A. | nscoder select (bit ere the transcoder | | | | |
| | | ed to '0' after dis to '1' will prevent | abling the port. This is workaround for hardware issue whe | Project | | | | |
| | select set | ed to '0' after disato '1' will prevent | abling the port. This is workaround for hardware issue whe HDMIC from being enabled on transcoder A. | ere the transcoder | | | | |
| | select set | ed to '0' after disa to '1' will prevent Name Disable | abling the port. This is workaround for hardware issue whe HDMIC from being enabled on transcoder A. Description | ere the transcoder Project | | | | |
| 30 | select set | ed to '0' after disa to '1' will prevent Name Disable Enable | abling the port. This is workaround for hardware issue who HDMIC from being enabled on transcoder A. Description Disable and tristates the Display Port C interface | ere the transcoder Project All | | | | |
| 30 | Select set 1 Value Ob 1b | ed to '0' after disa to '1' will prevent Name Disable Enable er_Select | abling the port. This is workaround for hardware issue who HDMIC from being enabled on transcoder A. Description Disable and tristates the Display Port C interface | ere the transcoder Project All | | | | |
| 30 | Value 0b 1b | ed to '0' after disa to '1' will prevent Disable Enable er_Select | abling the port. This is workaround for hardware issue who HDMIC from being enabled on transcoder A. Description Disable and tristates the Display Port C interface Enable. This bit enables the Display Port C interface | ere the transcoder Project All | | | | |
| 30 | Select set Value 0b 1b Transcode Project: Default Value | ed to '0' after disa to '1' will prevent Disable Enable er_Select | abling the port. This is workaround for hardware issue who HDMIC from being enabled on transcoder A. Description Disable and tristates the Display Port C interface Enable. This bit enables the Display Port C interface | ere the transcoder Project All | | | | |
| 30 | Select set f Value 0b 1b Transcode Project: Default Va See DPB o [DevIBX] V that this bi | ed to '0' after disa to '1' will prevent Disable Enable er_Select description. | abling the port. This is workaround for hardware issue who HDMIC from being enabled on transcoder A. Description Disable and tristates the Display Port C interface Enable. This bit enables the Display Port C interface | ere the transcoder Project All All Ssue it is required | | | | |
| 30 | Select set f Value 0b 1b Transcode Project: Default Va See DPB o [DevIBX] V that this bi | ed to '0' after disa to '1' will prevent Disable Enable er_Select description. Vriting to this bit t be cleared whe | abling the port. This is workaround for hardware issue whe HDMIC from being enabled on transcoder A. Description Disable and tristates the Display Port C interface Enable. This bit enables the Display Port C interface All Ob only takes effect when port is enabled. Due to hardware is | ere the transcoder Project All All Ssue it is required | | | | |
| 30 | Select set f Value 0b 1b Transcode Project: Default Va See DPB of [DevIBX] V that this bi port on tra | ed to '0' after disa to '1' will prevent Disable Enable er_Select description. Vriting to this bit t be cleared when nscoder A. | abling the port. This is workaround for hardware issue whe HDMIC from being enabled on transcoder A. Description Disable and tristates the Display Port C interface Enable. This bit enables the Display Port C interface All Ob only takes effect when port is enabled. Due to hardware is en port is disabled. To clear this bit software must tempor Description | ere the transcoder Project All All Ssue it is required arily enable this | | | | |
| 30 | Select set f Value 0b 1b Transcode Project: Default Va See DPB of [DevIBX] V that this bi port on tra Value | ed to '0' after disa to '1' will prevent Disable Enable er_Select description. Vriting to this bit t be cleared when nscoder A. Name | abling the port. This is workaround for hardware issue whe HDMIC from being enabled on transcoder A. Description Disable and tristates the Display Port C interface Enable. This bit enables the Display Port C interface All Ob only takes effect when port is enabled. Due to hardware is en port is disabled. To clear this bit software must tempor Description Transcoder A | ere the transcoder Project All All ssue it is required arriy enable this Project | | | | |



| | | DP | C—Display Port C Control Register | | | | |
|-------|--|------------------------------|---|----------|--|--|--|
| 29:28 | Link_trai | Link_training_pattern_enable | | | | | |
| | Project: All | | | | | | |
| | Default Value: 0b | | | | | | |
| | | | link initialization as defined in the DisplayPort specification. Please r nfigured prior to sending training patterns. | ote that | | | |
| | | | t, it must be turned on with pattern 1 enabled. When retraining a link, re-enabled with pattern 1 enabled. | the port | | | |
| | Value | Name | Description | Project | | | |
| | 00b | Pattern 1 | Pattern 1 enabled: Repetition of D10.2 characters | All | | | |
| | 01b | Pattern 2 | Pattern 2 enabled: Repetition of K28.5, D11.6, K28.5, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2. Please note that the entire pattern must complete before another pattern is sent. Scrambling initialization and disparity init commence at the end of the last iteration of pattern 2. | All | | | |
| | 10b Idle Idle Pattern enabled: Transmit BS followed by VB-ID with NoVideoStream_flag set to 1, five times | | | | | | |
| | 11b | Normal | Link not in training: Send normal pixels | All | | | |
| | Project: Default V See DPB | alue: description. | All Ob | | | | |
| | Value | Name | Description F | Project | | | |
| | 000b | 0.4V | 0.4 V A | AII. | | | |
| | 001b | 0.6V | 0.6 V A | | | | |
| | 010b | 0.8V | 0.8 V A | | | | |
| | 011b | 1.2V | 1.2 V A | | | | |
| | 1XXb | Reserved | | | | | |
| | | | | | | | |
| 24:22 | | hasis_level_s | | | | | |
| | Project: | alua | All | | | | |
| | Default Value: 0b See DPB description. | | | | | | |
| | Value | Name | Description F | Project | | | |
| | 000b | None | No pre-emphasis | All . | | | |
| | 001b | 3.5dB | 3.5dB pre-emphasis (1.5x) | All . | | | |
| | 010b | 6 dB | 6dB pre-emphasis (2x) | All . | | | |
| | | | | | | | |
| | 011b | 9.5 dB | 9.5dB pre-emphasis (3x) | All III | | | |



| 01.10 | Devel 14/1 | | | isplay Port C Control Register | | | | |
|-----------|--|-------------------------------------|--------------------|--------------------------------|--------------|---------|--|--|
| 21:19 | Port_Wid Project: | th_Selection | All | | | | | |
| | Default Va | alue. | 0b | | | | | |
| | | description. | 00 | | | | | |
| | Value | Name | Des | cription | | Project | | |
| | 000b | x1 | x1 M | Node | | All | | |
| | 001b | x2 | x2 | Mode | | All | | |
| | 011b | x4 | x4 N | <i>l</i> ode | | All | | |
| | others | Reserved | Res | erved | | All | | |
| 18 | Enhance | d_Framing_En | able | | | | | |
| | Project: | | All | | | | | |
| | Default Va | alue: | 0b | | | | | |
| | See DPB description. | | | | | | | |
| | Value | Name | | Description | | Project | | |
| | 0b | Disable | | Enhanced framing disabled | | All | | |
| | 1b | Enable | | Enhanced framing enabled | | All | | |
| 17:16 | Reserved | Project: | AI | l Fc | rmat: N | BZ | | |
| 15 | Port_reve | ersal | | | | | | |
| | Project: All | | | | | | | |
| | Default Va | Default Value: 0b | | | | | | |
| | See DPB description. | | | | | | | |
| | Value | Name | | Description | | Project | | |
| | 0b | Not Revers | ed | Port not reversed | | All | | |
| | 1b | Reversed | | Port reversed | | All | | |
| | Reserved | Project: | AI | l Fc | rmat: N | BZ | | |
| 14:8 | 110001100 | 1 10,000 | Scrambling_Disable | | | | | |
| 14:8 7 | | | | | | | | |
| | | | All | | | | | |
| | Scrambli | | All Deb | ŋ | | | | |
| | Scrambli Project: | ng_Disable | | ŋ | | | | |
| | Scrambli Project: Security: Default Va | ng_Disable | Deb | g | | | | |
| | Scrambli Project: Security: Default Va | ng_Disable | Deb | ug Description | Proje | ct | | |
| | Scrambli Project: Security: Default Va See DPB | ng_Disable alue: description. | Deb | | Proje All | ect | | |



| | | DPC—Di | splay Port C Control Register | | | | | |
|-----|----------------------|---|--|-------------------------|--|--|--|--|
| 6 | Audio_O | utput_Enable | | | | | | |
| | Project: | All | | | | | | |
| | Default Va | | | | | | | |
| | This bit er complete | hables audio on this ou and set to "Normal." | utput port. It may be enabled or disabled only whe | en the link training is | | | | |
| | Value | Name | Description | Project | | | | |
| | 0b | Disable | Audio output disabled | All | | | | |
| | 1b | Enable | Audio output enabled | All | | | | |
| 5 | HDCP_Po | ort_Select | | | | | | |
| | Project: | All | | | | | | |
| | Default Va | | | | | | | |
| | See DPB description. | | | | | | | |
| | Value | Name | Description | Project | | | | |
| | 0b | Disable | No HDCP encryption on this port | All | | | | |
| | 1b | Enable | Enable HDCP on this port | All | | | | |
| | Progran | nming Notes | | | | | | |
| | | an only be selected or on will be disabled. | one port at a time, per transcoder. If two or mor | e ports are selected, | | | | |
| 4:3 | Sync_Pol | arity | | | | | | |
| | Project: | All | | | | | | |
| | Default Va | alue: 11b | VS and HS are active high | | | | | |
| | See DPB | description. | | | | | | |
| | Value | Name | Description | Project | | | | |
| | 00b | Low | VS and HS are active low (inverted) | All | | | | |
| | 11b | VS Low, HS High | VS is active low (inverted), HS is active high | All | | | | |
| | 11b | VS High, HS Low | VS is active high, HS is active low (inverted) | All | | | | |
| | 11b | High | VS and HS are active high | All | | | | |



| 2 | Digital_D | Display_C_Detec | ted | | |
|---|-----------|---------------------|--|--------------------------|--|
| | Project: | | All | | |
| | Access: | | Read Only | | |
| | Default V | /alue: | Ob | | |
| | Dood on | ly hit indianting w | bother a digital display was detected during initializativ | on It aignifica the low | |
| | | | hether a digital display was detected during initialization (C) data line at boot. | on. It signifies the lev | |
| | of the GN | MBUS port 3 (port | C) data line at boot. | | |



4.4.2 DPC_AUX_CH_CTL—Display Port C AUX Channel Control

| Register T | Type: MN | 110 | | | | | |
|------------------------|-----------------------|--|------------------|----------------|-----------|---------|--|
| | Offset: E42 | | | | | | |
| Project: | All | | | | | | |
| Default Va | | 050000h | | | | | |
| Access: Size (in hi | R/V | V | | | | | |
| Size (in bi Bit | ts): 32 | | | Descr | iption | | |
| 31 | Send/Bu | ev | | | . | | |
| 51 | Project: | sy | All | | | | |
| | Default V | alue. | 0b | | | | |
| | | description. | 00 | | | | |
| | Program | nming Notes | | | | | |
| | Do not o | change any field | s while Busy bit | t 31 is assert | ed. | | |
| 30 | Done See DPB | P description. | roject: All | Access: | R/W Clear | | |
| | - | - | D : | . – | | | |
| 29 | - | _ on_Done description. | Project: A | li For | nat: | | |
| 28 | Time_ou See DPB | t_error P description. | roject: All | Access: | R/W Clear | | |
| 27:26 | Project: Default V | t_timer_value alue: description. | All Ob | | | | |
| | Value | Name | Descriptio | on | | Project | |
| | 00b | 400us | 400us | | | All | |
| | 01b | 600us | 600us | | | All | |
| | 10b | 800us | 800us | | | All | |
| | 11b | 1600us | 1600us | | | All | |
| 25 | Receive_ See DPB | error P description. | roject: All | Access: | R/W Clear | | |
| 24:20 | Message | - Size P description. | roject: All | Format: | | | |



| 19:16 | Precharg Default Va See DPB | | Projec 0101b | | |
|-------|---|-----------------------------------|------------------|--|-----------------------|
| 15 | Project: Default Va | sv_select alue: descriptior | All Ob | | |
| | Value | Name | Dese | cription | Project |
| | 0b | Aux | Use | AUX Data registers for regular data transmission | All |
| | 1b | HDCP | Use | HDCP internal Aksv for part of the data transmission | All |
| 14 | Invert_Ma Project: Security: Default Va | anchester alue: | All Te: 0b | st | |
| | Value | Name | Descri | ption | Project |
| | 0b | Zero | Manch | ester code rising edge mid-clk signifies zero | All |
| | 1b | One | Manch | ester code rising edge mid-clk signifies one | All |
| 13 | Sync_Only_Clock_Recov Project: Security: Default Value: | | | y st | |
| | Value | Name | | Description | Project |
| | 0b | Sync and | Data | Recover clock during sync pattern and data phase | All |
| | 1b | Sync Onl | у | Only recover clock during sync pattern | All |
| 12 | Disable_ Project: | De-glitch | All Te: | | |
| 12 | Security: Default Va | alue: | 0b | | |
| 12 | Security: | alue: Name | 0b Descri | ption | Project |
| 12 | Security: Default V | 1 | Descri | ption serial input de-glitch logic | Project All |



| 11 | Double_ | precharge | | | |
|----|-----------|------------|---------------------------------|--------|--|
| | Project: | | All | | |
| | Security: | | Test | | |
| | Default V | alue: | 0b | | |
| | Value | Name | Description | Projec | |
| | 0b | Programmed | Precharge time is as programmed | All | |
| | | | Precharge time is doubled | All | |
| | - | | | | |

4.4.3 DPC_AUX_CH_DATA—Display Port C AUX Data Registers

| | DP | C_AUX_CH_DA ⁻ | TA—Disp | olay I | Port C AU | X Data Registers |
|---------------|----------------|--------------------------|---------------|--------|-------------|-----------------------|
| Register Ty | /pe: MM | 10 | | | | |
| Address Of | fset: E42 | :14h | | | | |
| Project: | All | | | | | |
| Default Val | ue: 000 | 00000h; | | | | |
| Access: | R/W | / | | | | |
| Size (in bits | s): 5x3 | 2 | | | | |
| The read va | alue will no | ot be valid while Bus | y bit 31 is a | assert | ed. | |
| DWord | Bit | | | | Description | |
| 0 | 31:0 | AUX_CH_DATA1 | Project: | All | Format: | DP Aux Ch Data Format |
| 1 | 31:0 | AUX_CH_DATA2 | Project: | All | Format: | DP Aux Ch Data Format |
| 2 | 31:0 | AUX_CH_DATA3 | Project: | All | Format: | DP Aux Ch Data Format |
| 3 | 31:0 | AUX_CH_DATA4 | Project: | All | Format: | DP Aux Ch Data Format |
| 4 | 31:0 | AUX_CH_DATA5 | Project: | All | Format: | DP Aux Ch Data Format |

4.5 **DPD Control and Aux Channel**



4.5.1 DPD—DisplayPort D Control Register

| | | DP | D—D | DisplayPort D Control Register | | | | |
|-------------|---|---|---|---|---|--|--|--|
| Register T | Гуре: | M | MIO | | | | | |
| Address C | Offset: | E4 | 1300h | | | | | |
| Project: | | All | | | | | | |
| Default Va | alue: | ••• | 00001 | | | | | |
| Access: | | | W Prot | tect | | | | |
| Size (in bi | • | 32 | | | | | | |
| | uffer Update | | | s on bit | analia connecto | | | |
| o this port | t. Please no | | layPor | rite protected by Panel Power Sequencer when p rt D uses the same lanes as HDMID. Therefore l aneously. | | | | |
| Bit | | | | Description | | | | |
| 31 | DisplayPo | ort_D_Enable | | | | | | |
| | Project: | | All | | | | | |
| | Default Va | lue: | 0b | | | | | |
| | See DPB description. | | | | | | | |
| | [DevIBX] V #30) cleare | , Vhen disabling ed to '0' after o | disablir | bort, software must temporarily enable the port with training the port. This is workaround for hardware issue who MID from being enabled on transcoder A. | | | | |
| | [DevIBX] V #30) cleare | , Vhen disabling ed to '0' after o | disablir ent HD | ng the port. This is workaround for hardware issue whe | | | | |
| | [DevIBX] V #30) cleare select set t | Vhen disabling ed to '0' after o to '1' will preve | disablir ent HD Des | ng the port. This is workaround for hardware issue who MID from being enabled on transcoder A. | ere the transcoder | | | |
| | [DevIBX] V #30) cleare select set t Value | Vhen disabling ed to '0' after o to '1' will preve Name | disablir ent HD Des Disa | ng the port. This is workaround for hardware issue who MID from being enabled on transcoder A. scription | ere the transcoder Project | | | |
| 30 | [DevIBX] V #30) cleare select set t Value 0b | Vhen disabling ed to '0' after o to '1' will preve Name Disable Enable | disablir ent HD Des Disa | ng the port. This is workaround for hardware issue who MID from being enabled on transcoder A. scription able and tristates the Display Port D interface | ere the transcoder Project All | | | |
| 30 | [DevIBX] V #30) cleare select set t Value 0b 1b | Vhen disabling ed to '0' after o to '1' will preve Name Disable Enable | disablir ent HD Des Disa | ng the port. This is workaround for hardware issue who MID from being enabled on transcoder A. scription able and tristates the Display Port D interface | ere the transcoder Project All | | | |
| 30 | [DevIBX] V #30) cleare select set t Ob 1b | Vhen disabling ed to '0' after of to '1' will preve Name Disable Enable er_Select | disablir ent HD Des Disa Ena | ng the port. This is workaround for hardware issue who MID from being enabled on transcoder A. scription able and tristates the Display Port D interface | ere the transcoder Project All | | | |
| 30 | [DevIBX] V #30) cleare select set t Ob 1b Transcode Project: Default Va | Vhen disabling ed to '0' after of to '1' will preve Name Disable Enable er_Select | disablir ent HD Des Disa Ena | ng the port. This is workaround for hardware issue who MID from being enabled on transcoder A. scription able and tristates the Display Port D interface | ere the transcoder Project All | | | |
| 30 | [DevIBX] V #30) cleare select set t Ob 1b Transcode Project: Default Va | Vhen disabling ed to '0' after of to '1' will preve Name Disable Enable er_Select | disablir ent HD Des Disa Ena | ng the port. This is workaround for hardware issue who MID from being enabled on transcoder A. scription able and tristates the Display Port D interface | ere the transcoder Project All | | | |
| 30 | [DevIBX] V #30) cleare select set t Value 0b 1b Transcode Project: Default Va See DPB c [DevIBX] V | Vhen disabling ed to '0' after of to '1' will preve Disable Enable er_Select lue: description. Vriting to this b | disablir ent HD Des Ena All Ob | ng the port. This is workaround for hardware issue who MID from being enabled on transcoder A. scription able and tristates the Display Port D interface | Project All All Subscription | | | |
| 30 | [DevIBX] V #30) cleare select set t Value 0b 1b Transcode Project: Default Va See DPB c [DevIBX] V that this bit | Vhen disabling ed to '0' after of to '1' will preve Disable Enable er_Select lue: description. Vriting to this b | disablir ent HD Des Ena All Ob | ng the port. This is workaround for hardware issue who MID from being enabled on transcoder A. scription able and tristates the Display Port D interface able. This bit enables the Display Port D interface | Project All All Subscription | | | |
| 30 | [DevIBX] V #30) cleare select set t Value 0b 1b Transcode Project: Default Va See DPB c [DevIBX] V that this bit port on tran | Vhen disabling ed to '0' after of to '1' will preve Disable Enable er_Select lue: description. Vriting to this b t be cleared winscoder A. | disablir ent HD Des Disa Ena All Ob bit only when p | ng the port. This is workaround for hardware issue who MID from being enabled on transcoder A. scription able and tristates the Display Port D interface able. This bit enables the Display Port D interface able. This bit enables the Display Port D interface | Project All All Ssue it is required arily enable this | | | |



| | | DPI | D—DisplayPort D Control Register | | | | |
|-------|---|-----------------------|--|--------------|--|--|--|
| 29:28 | Link_trai | ning_pattern_o | enable | | | | |
| | Project: All | | | | | | |
| | Default Value: 0b | | | | | | |
| | These bits are used for link initialization as defined in the DisplayPort specification. Please note that the link must first be configured prior to sending training patterns. | | | | | | |
| | | | it must be turned on with pattern 1 enabled. When retraining a lir e-enabled with pattern 1 enabled. | nk, the port | | | |
| | Value | Name | Description | Project | | | |
| | 00b | Pattern 1 | Pattern 1 enabled: Repetition of D10.2 characters | All | | | |
| | 01b | Pattern 2 | Pattern 2 enabled: Repetition of K28.5, D11.6, K28.5, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2. Please note that the entire pattern must complete before another pattern is sent. Scrambling initialization and disparity init commence at the end of the last iteration of pattern 2. | All | | | |
| | 10b Idle Idle Pattern enabled: Transmit BS followed by VB-ID with NoVideoStream_flag set to 1, five times | | | | | | |
| | 11b | Normal | Link not in training: Send normal pixels | All | | | |
| 27:25 | Voltage_swing_level_set Project: All Default Value: 0b See DPB description. | | | | | | |
| | Value | Name | Description | Project | | | |
| | 000b | 0.4V | 0.4 V | All | | | |
| | 001b | 0.6V | 0.6 V | All | | | |
| | 010b | 0.8V | 0.8 V | All | | | |
| | 011b | 1.2V | 1.2 V | All | | | |
| | 1XXb | Reserved | Reserved | All | | | |
| 24:22 | Pre-emphasis_level_set | | | | | | |
| | Project: | | All | | | | |
| | Default V See DPB | alue: description. | 0b | | | | |
| | Value | Name | Description | Project | | | |
| | 000b | None | No pre-emphasis | All | | | |
| | 0000 | | | | | | |
| | 000b | 3.5dB | 3.5dB pre-emphasis (1.5x) | All | | | |
| | | | 3.5dB pre-emphasis (1.5x)6dB pre-emphasis (2x) | All All | | | |
| | 001b | 3.5dB | | | | | |



| 21:19 | Port Wid | th_Selection | -DisplayPort D Control Re | | | |
|-----------|---|---|--|--------------------------|---------|--|
| 21.10 | Project: All | | | | | |
| | Default Va | | Ob | | | |
| | See DPB | description. | | | | |
| | Value | Name | Description | | Project | |
| | 000b | x1 | x1 Mode | | All | |
| | 001b | x2 | x2 Mode | | All | |
| | 011b | x4 | x4 Mode | | All | |
| | others | Reserved | Reserved | | All | |
| 18 | Enhance | d_Framing_Enal | ble | | | |
| | Project: | - | All | | | |
| | Default Va | alue: (| Ob | | | |
| | See DPB description. | | | | | |
| | Value Name | | Description | Description | | |
| | 0b | Disable | Enhanced framing disabled | | All | |
| | 1b | Enable | Enhanced framing enabled | Enhanced framing enabled | | |
| 17:16 | Reserved | Project: | All | Format: | MBZ | |
| 15 | Port_reversal | | | | | |
| | Project: | | All | | | |
| | Default Va | | Ob | | | |
| | See DPB | description. | | | | |
| | Value | Name | Description | | Project | |
| | | | | | All | |
| | 0b | Not Reversed | d Port not reversed | | 711 | |
| | Ob 1b | Not Reversed | Port not reversed Port reversed | | All | |
| 14:8 | | Reversed | Port reversed | Format: | | |
| 14:8 7 | 1b Reserved | Reversed | Port reversed | Format: | All | |
| | 1b Reserved | Reversed Project: ng_Disable | Port reversed | Format: | All | |
| | 1b Reserved Scrambli | Reversed Project: ng_Disable | Port reversed | Format: | All | |
| | 1b Reserved Scrambli Project: Security: Default Value | Reversed Project: ng_Disable alue: | All | Format: | All | |
| | 1b Reserved Scrambli Project: Security: Default Value | Reversed Project: ng_Disable | All All Debug | Format: | All | |
| | 1b Reserved Scrambli Project: Security: Default Value | Reversed Project: ng_Disable alue: | All All Debug | | All | |
| | 1b Reserved Scrambli Project: Security: Default Va See DPB | Reversed Project: ng_Disable alue: description. | Port reversed All All Debug Ob | | All | |



| | | DPD—D | isplayPort D Control Register | | | | | | |
|-----|---|---------------------------------------|--|---------|--|--|--|--|--|
| 6 | Audio_O | utput_Enable | | | | | | | |
| | Project: All | | | | | | | | |
| | Default Va | alue: Ob | | | | | | | |
| | This bit enables audio on this output port. It may be enabled or disabled only when the link training complete and set to "Normal." | | | | | | | | |
| | Value | Name | Description | Project | | | | | |
| | 0b | Disable | Audio output disabled | All | | | | | |
| | 1b | Enable | Audio output enabled | All | | | | | |
| 5 | HDCP_P | ort_Select | | | | | | | |
| | Project: All | | | | | | | | |
| | Default Value: 0b | | | | | | | | |
| | See DPB description. | | | | | | | | |
| | Value | Name | Description | Project | | | | | |
| | 0b | Disable | No HDCP encryption on this port | All | | | | | |
| | 1b | Enable | Enable HDCP on this port All | | | | | | |
| | Program | Programming Notes | | | | | | | |
| | HDCP can only be selected on one port at a time, per transcoder. If two or more ports are selected, encryption will be disabled. | | | | | | | | |
| 4:3 | Sync_Po | larity | | | | | | | |
| | Project: | All | | | | | | | |
| | Default Va | alue: 11b | VS and HS are active high | | | | | | |
| | See DPB | description. | | | | | | | |
| | Value | Name | Description | Project | | | | | |
| | 00b | Low | VS and HS are active low (inverted) | All | | | | | |
| | 11b | VS Low, HS High | VS is active low (inverted), HS is active high | All | | | | | |
| | 11b | VS High, HS Low | VS is active high, HS is active low (inverted) | All | | | | | |
| | | · · · · · · · · · · · · · · · · · · · | | | | | | | |



| 2 | Digital_D | Display_D_Detec | ted | | | |
|---|-----------|---------------------|--|---|--|--|
| | Project: | | All | | | |
| | Access: | | Read Only | | | |
| | Default V | alue: | Ob | | | |
| | Dood on | ly hit indiaating w | bother a digital diaplay was datastad during initializati | on It cignifica the law | | |
| | of the GM | MBUS port 5 (port | hether a digital display was detected during initialization D) data line at boot. | _ | | |
| | | | | on. It signifies the lev Project All | | |



4.5.2 DPD_AUX_CH_CTL—Display Port D AUX Channel Control

| Register T | vpe: MM | 110 | | | | | | |
|------------------------|--|----------------|------------|------------|----------------|-----------|---------|--|
| - | Offset: E43 | | | | | | | |
| Project: | All | | | | | | | |
| Default Va Access: | alue: 000 R/V |)50000h | | | | | | |
| Access: Size (in bi | | V | | | | | | |
| Bit | Description | | | | | | | |
| 31 | Send/Bu | sy | | | | | | |
| | Project: | - | All | | | | | |
| | Default V | alue: | 0b | | | | | |
| | See DPB | description. | | | | | | |
| | Program | nming Notes | ; | | | | | |
| | Do not o | change any fie | elds while | e Busy bit | t 31 is assert | ed. | | |
| 30 | Done | | Project: | All | Access: | R/W Clear | | |
| | See DPB description. | | | | | | | |
| 29 | Interrupt_on_Done Project: All Format: | | | | | | | |
| | See DPB description. | | | | | | | |
| 28 | Time_ou | | Project: | All | Access: | R/W Clear | | |
| | See DPB | description. | | | | | | |
| 27:26 | Time_ou | t_timer_value | е | | | | | |
| | Project: | | All | | | | | |
| | Default V | alue: | 0b | | | | | |
| | See DPB | description. | | | | | | |
| | Value | Name | D | escriptio | on | | Project | |
| | 00b | 400us | 4 | 00us | | | All | |
| | 01b | 600us | 6 | 00us | | | All | |
| | 10b | 800us | 8 | 00us | | | All | |
| | 11b | 1600us | 1 | 600us | | | All | |
| 25 | Receive | error | Project: | All | Access: | R/W Clear | | |
| | | description. | | | | | | |
| 24:20 | Message | _Size | Project: | All | Format: | | | |
| | | description. | | | | | | |



| 19:16 | Precharg Default Va See DPB | | 0101b | roject: All Format: 101b 5 decimal which gives 10us of precharge | | | | |
|-------|---|-----------------------------------|-----------------------------|---|---------|--|--|--|
| 15 | Project: Default Va | sv_select alue: description | All Ob | | | | | |
| | Value | Name | Desc | cription | Project | | | |
| | 0b | Aux | Use | AUX Data registers for regular data transmission | All | | | |
| | 1b | HDCP | Use | HDCP internal Aksv for part of the data transmission | All | | | |
| 14 | Project: Security: | | | | | | | |
| | Value | Name | Descri | Description | | | | |
| | 0b | Zero | Manch | Manchester code rising edge mid-clk signifies zero | | | | |
| | 1b | One | Manch | All | | | | |
| 13 | Sync_On Project: Security: Default V | Iy_Clock_I | Recover All Tes 0b | | | | | |
| | Value | Name | | Description | Project | | | |
| | 0b | Sync and | Data | Recover clock during sync pattern and data phase | All | | | |
| | 1b | Sync Onl | y | Only recover clock during sync pattern | All | | | |
| 12 | Disable_ Project: Security: Default Va | Ū | All Tes 0b | st | | | | |
| | Value | Name | Descri | ption | Project | | | |
| | value | | | | | | | |
| | 0b | Enable | Enable | serial input de-glitch logic | All | | | |



| 11 | Double_ | precharge | | |
|----|-----------|------------|---------------------------------|--------|
| | Project: | | All | |
| | Security: | - | Test | |
| | Default V | alue: | 0b | |
| | Value | Name | Description | Projec |
| | 0b | Programmed | Precharge time is as programmed | All |
| | | | Deschanges times in developed | All |
| | 1b | Doubled | Precharge time is doubled | 7.01 |

4.5.3 DPD_AUX_CH_DATA—Display Port D AUX Data Registers

| | DP | D_AUX_CH_DA ⁻ | TA—Disp | olay | Port D AU | X Data Registers |
|------------------------|----------------|--------------------------|---------------|--------|-----------|-----------------------|
| Register Ty | vpe: MM | 10 | | | | |
| Address Offset: E4314h | | | | | | |
| Project: | All | | | | | |
| Default Val | ue: 000 | 00000h; | | | | |
| Access: | R/W | V | | | | |
| Size (in bits | s): 5x3 | 2 | | | | |
| The read va | alue will n | ot be valid while Bus | y bit 31 is a | assert | ed. | |
| DWord | Bit | Description | | | | |
| 0 | 31:0 | AUX_CH_DATA1 | Project: | All | Format: | DP Aux Ch Data Format |
| 1 | 31:0 | AUX_CH_DATA2 | Project: | All | Format: | DP Aux Ch Data Format |
| 2 | 31:0 | AUX_CH_DATA3 | Project: | All | Format: | DP Aux Ch Data Format |
| 3 | 31:0 | AUX_CH_DATA4 | Project: | All | Format: | DP Aux Ch Data Format |
| 4 | 31:0 | AUX_CH_DATA5 | Project: | All | Format: | DP Aux Ch Data Format |



4.6 DP_BUFTRANS—DisplayPort Buffer Translation

| | DisplayPort Buffer Translation Format | | | | | | | | |
|------------------------|--|-------------|-----|---------|------|--|--|--|--|
| Project: Default Va | All alue: 00000000h | | | | | | | | |
| Bit | | Description | | | | | | | |
| 31:28 | Reserved | Project: | All | Format: | MBZ | | | | |
| 27:19 | OE These bits select the OE vswing level | Project: | All | Range: | 0511 | | | | |
| 18:17 | Reserved | Project: | All | Format: | MBZ | | | | |
| 16:12 | Pre_Emphasis These bits select the pre-emphasis level | Project: | All | Range: | 031 | | | | |
| 11:10 | Reserved | Project: | All | Format: | MBZ | | | | |
| 9:6 | P_current_drive These bits select the P current drive value | Project: | All | Range: | 015 | | | | |
| 5:4 | Reserved | Project: | All | Format: | MBZ | | | | |
| 3:0 | N_current_drive These bits select the N current drive value | Project: | All | Range: | 015 | | | | |

The register defaults for B0 silicon was provided by EV team (2/09). These MUST be programmed by software before enabling DisplayPort the first time. They only need to be programmed once after power on.

10/6/09: L3 0dB setting has been revised to pass compliance testing

| DF | o mode | Offset | Value |
|----|--------|---------|------------|
| L1 | 0dB | 0xE4F00 | 0x0100030C |
| L1 | 3.5dB | 0xE4F04 | 0x00B8230C |
| L1 | 6dB | 0xE4F08 | 0x06F8930C |
| L1 | 9.5dB | 0xE4F0C | 0x09F8E38E |
| L2 | 0dB | 0xE4F10 | 0x00B8030C |
| L2 | 3.5dB | 0xE4F14 | 0x0B78830C |



| L2 | 6dB | 0xE4F18 | 0x0FF8D3CF |
|----|-------|---------|------------|
| L3 | 0dB | 0xE4F1C | 0x01E8030C |
| L3 | 3.5dB | 0xE4F20 | 0x0FF863CF |
| L4 | 0 dB | 0xE4F24 | 0x0FF803CF |

| Vswing | 0dB pre-emphasis | 3.5dB pre-emphasis | 6dB pre-emphasis | 9.5dB pre-emphasis |
|--------|------------------|--------------------|------------------|--------------------|
| 400mV | E4F00 | E4F04 | E4F08 | E4F0C |
| 600mV | E4F10 | E4F14 | E4F18 | Not supported |
| 800mV | E4F1C | E4F20 | Not supported | Not supported |
| 1200mV | E4F24 | Not supported | Not supported | Not supported |

| | | | RANS—DisplayPort Buffer Tra | anglation | |
|---------------|----------------|----------------|--|-------------------------|---------|
| De sietes T | | | KANS—DisplayFort Buller II | | |
| Register Ty | - | - | | | |
| Address Of | | -00h | | | |
| Project: | | IBX-B+ | | | |
| Default Val | ue: 010 017 | 8038Eh; 00B833 | 88Eh; 0178838Eh; 09F8E38Eh; 00B8038E 8Eh; 09F8038Eh | n; 0978838En; 09F8B38E; | |
| Access: | | te Only | | | |
| Size (in bits | s): 10x | 32 | | | |
| • | | | pre-emphasis and voltage swing buff hasis settings in the DisplayPort Contr | | for the |
| DWord | Bit | | Description | | |
| 0 | 31:0 | Voltage_swin | g_400mV_and_Pre-emphasis_0.0dB | Project: | All |
| | | Format: | DisplayPort Buffer Translation Format | See Description Above | |
| 1 | 31:0 | Voltage_swing | g_400mV_and_Pre-emphasis_3.5dB | Project: | All |
| | | Format: | DisplayPort Buffer Translation Format | See Description Above | |
| 2 | 31:0 | Voltage_swing | g_400mV_and_Pre-emphasis_6.0dB | Project: | All |
| | | Format: | DisplayPort Buffer Translation Format | See Description Above | |
| 3 | 31:0 | Voltage_swing | g_400mV_and_Pre-emphasis_9.5dB | Project: | All |
| | | Format: | DisplayPort Buffer Translation Format | See Description Above | |
| 4 | 31:0 | Voltage_swing | g_600mV_and_Pre-emphasis_0.0dB | Project: | All |
| | | Format: | DisplayPort Buffer Translation Format | See Description Above | |
| 5 | 31:0 | Voltage_swin | g_600mV_and_Pre-emphasis_3.5dB | Project: | All |
| | | Format: | DisplayPort Buffer Translation Format | See Description Above | |



| | | DP_BUFTRANS—DisplayPort Buffer Tra | anslation | |
|---|------|---|-----------------------------------|-----|
| 6 | 31:0 | Voltage_swing_600mV_and_Pre-emphasis_6.0dB Format: DisplayPort Buffer Translation Format | Project: See Description Above | All |
| 7 | 31:0 | Voltage_swing_800mV_and_Pre-emphasis_0.0dB Format: DisplayPort Buffer Translation Format | Project: See Description Above | All |
| 8 | 31:0 | Voltage_swing_800mV_and_Pre-emphasis_3.5dB Format: DisplayPort Buffer Translation Format | Project: See Description Above | All |
| 9 | 31:0 | Voltage_swing_1200mV_and_Pre-emphasis_0.0dB Format: DisplayPort Buffer Translation Format | Project: See Description Above | All |



5. South AFE Registers (FC000h– FFFFFh)

This topic is documented separately

