

Intel[®] OpenSource HD Graphics Programmer's Reference Manual (PRM) Volume 3 Part 2: Display Registers – CPU Registers (SandyBridge)

For the 2011 Intel Core Processor Family

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1. CPU Display Registers [DevSNB+]

This chapter discusses CPU Display Registers that are active in SandyBridge and later projects, unless indicated otherwise.

1.1 1.1 Introduction and Register Summary

This chapter contains the register descriptions for the display portion of a family of integrated graphics devices. These registers do vary by devices within the family of devices so special attention needs to be paid to which devices use which registers and register fields.

Different devices within the family may add, modify, or delete registers or register fields relative to another device in the same family based on the supported functions of that device.

The following table contains the sections break down where the register information is contained within this chapter:

Address Range	Description
40000h-4FFFFh	Shared Functions
60000h-6FFFFh	Pipe and Port Controls
70000h-7FFFFh	Plane Controls

1.1.1 Terminology

Description	Software Use	Should be implemented as
Read/Write	This bit can be read or written.	
Reserved	Don't assume a value for these bits. Writes have no effect.	Writes are ignored. Reads return zero.
Reserved: write as zero, must be zero, MBZ	Software must always write a zero to these bits. This allows new features to be added using these bits that will be disabled when using old software and as the default case.	Writes are ignored. Reads return zero. Maybe be connected as Read/Write in future projects.
Reserved: PBC, software must preserve contents	Software must write the original value back to this bit. This allows new features to be added using these bits.	Read only or test mode Read/Write.
Read Only	This bit is read only. The read value is determined by hardware. Writes to this bit have no effect.	According to each specific bit. The bit value is determined by hardware and not affected by register writes to the actual bit.
Read/Clear	This bit can be read. Writes to it with a one cause the bit to clear.	Hardware events cause the bit to be set and the bit will be cleared on a write operation where the corresponding bit has a one for a value.



Description	Software Use	Should be implemented as
Double Buffered	Write when desired. Read gives the unbuffered value (written value) unless specified otherwise. Written values will update to take effect after a certain point. Some have a specific arming sequence where a write to another register is required before the update can take place. This is used to ensure atomic updates of several registers.	Two stages of registers used. First stage is written into and used for readback (unless specified otherwise). First stage value is transferred into second stage at the update point. Second stage value is used to control hardware. Arm/disarm flag needed for specific arming sequences.

1.1.2 Display Mode Set Sequence

		Wait values
	CP	U DP PLL warmup = 20uS
	CP	U FDI transmitter PLL warmup = 10us
	DN	l latency = 20uS
	FD	training pattern 1 time = 0.5uS
	FD	training pattern 2 time = 1.5uS
	FD	idle pattern time = 31uS
		Enable sequence
1.	Enable	panel power as needed to retrieve panel configuration (use AUX VDD enable bit
2.	Enable enablin	PCH clock reference source and PCH SSC modulator, wait for warmup (Can be done anytime before g port)
3.	lf enabl	ing CPU embedded DisplayPort A: (Can be done anytime before enabling CPU pipe or port)
	a.	Enable PCH 120MHz clock source output to CPU, wait for DMI latency
	b.	Configure and enable CPU DisplayPort PLL in the DisplayPort A register, wait for warmup
4.	lf enabli	ng port on PCH: (Must be done before enabling CPU pipe or FDI)
	a.	Enable PCH FDI Receiver PLL, wait for warmup plus DMI latency
	b.	Switch from Rawclk to PCDclk in FDI Receiver (FDI A OR FDI B)
	с.	[DevSNB] Enable CPU FDI Transmitter PLL, wait for warmup
	d.	[DevILK] CPU FDI PLL is always on and does not need to be enabled
5.	Enable	CPU panel fitter if needed for hires, required for VGA (Can be done anytime before enabling CPU pipe)
6.	Configu	re CPU pipe timings, M/N/TU, and other pipe settings (Can be done anytime before enabling CPU pipe)

- 7. Enable CPU pipe
- 8. Configure and enable CPU planes (VGA or hires)
- 9. If enabling port on PCH:
 - a. Program PCH FDI Receiver TU size same as Transmitter TU size for TU error checking
 - b. Train FDI
 - i. Set pre-emphasis and voltage (iterate if training steps fail)
 - ii. Enable CPU FDI Transmitter and PCH FDI Receiver with Training Pattern 1 enabled.



	iii. Wait for FDI training pattern 1 time
	iv. Read PCH FDI Receiver ISR ([DevIBX-B+] IIR) for bit lock in bit 8 (retry at least once if no lock)
	v. Enable training pattern 2 on CPU FDI Transmitter and PCH FDI Receiver
	vi. Wait for FDI training pattern 2 time
	vii. Read PCH FDI Receiver ISR ([DevIBX-B+] IIR) for symbol lock in bit 9 (retry at least once if no lock)
	viii. Enable normal pixel output on CPU FDI Transmitter and PCH FDI Receiver
	ix. Wait for FDI idle pattern time for link to become active
С.	Configure and enable PCH DPLL, wait for PCH DPLL warmup (Can be done anytime before enabling PCH transcoder)
d.	[DevCPT] Configure DPLL SEL to set the DPLL to transcoder mapping and enable DPLL to the transcoder.
e.	[DevCPT] Configure DPLL_CTL DPLL_HDMI_multipler.
f.	Configure PCH transcoder timings, M/N/TU, and other transcoder settings (should match CPU settings).
g.	[DevCPT] Configure and enable Transcoder DisplayPort Control if DisplayPort will be used
h.	Enable PCH transcoder
10. Enable	ports (DisplayPort must enable in training pattern 1)
11. Enable	panel power through panel power sequencing
12. Wait for	r panel power sequencing to reach enabled steady state
13. Disable	panel power override
14. If Displa	ayPort, complete link training
15 Enchi-	
is. Enable	panel backlight
ID. ENADIO	panel backlight Disable sequence
1. Disable	Disable sequence
 Disable Disable 	Disable sequence Panel backlight
 Disable Disable Disable 	Disable sequence Panel backlight panel power through panel power sequencing
 Disable Disable Disable Disable Disable 	Disable sequence Panel backlight panel power through panel power sequencing CPU planes (VGA or hires)
 Disable Disable Disable Disable [DevlLk Disable 	Disable sequence Panel backlight panel power through panel power sequencing CPU planes (VGA or hires) K-A] Disable CPU panel fitter
 Disable Disable Disable Disable Disable [DevlLk Disable Wait for 	Disable sequence Panel backlight panel power through panel power sequencing CPU planes (VGA or hires) (-A] Disable CPU panel fitter CPU pipe
 Disable Disable Disable Disable [DevILk Disable Wait for If disable 	Disable sequence Panel backlight panel power through panel power sequencing CPU planes (VGA or hires) K-A] Disable CPU panel fitter CPU pipe r CPU pipe off status (CPU pipe config register pipe state)
 Disable Disable Disable Disable Disable [DevILk Disable Wait for If disable Disable 	Disable sequence Panel backlight panel power through panel power sequencing CPU planes (VGA or hires) K-A] Disable CPU panel fitter CPU pipe r CPU pipe r CPU pipe off status (CPU pipe config register pipe state) ling DisplayPort on PCH, write the DisplayPort control register bit 31 to 0b.
 Disable Disable Disable Disable Disable [DevILk Disable Wait for If disable Disable 	Disable sequence Panel backlight panel power through panel power sequencing CPU planes (VGA or hires) K-A] Disable CPU panel fitter CPU pipe r CPU pipe off status (CPU pipe config register pipe state) ling DisplayPort on PCH, write the DisplayPort control register bit 31 to 0b. CPU panel fitter (Can be done anytime after CPU pipe is off)
 Disable Disable Disable Disable [DevILk Disable Wait for If disable Disable Disable If disable 	Disable sequence Panel backlight panel power through panel power sequencing CPU planes (VGA or hires) K-A] Disable CPU panel fitter CPU pipe r CPU pipe off status (CPU pipe config register pipe state) ling DisplayPort on PCH, write the DisplayPort control register bit 31 to 0b. CPU panel fitter (Can be done anytime after CPU pipe is off) ling CPU embedded DisplayPort A
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 Disable Disable Disable Disable [DevILk Disable Wait for If disable Disable If disable If disable a. c. 	Disable sequence Panel backlight panel power through panel power sequencing CPU planes (VGA or hires) K-A] Disable CPU panel fitter CPU pipe r CPU pipe off status (CPU pipe config register pipe state) ling DisplayPort on PCH, write the DisplayPort control register bit 31 to 0b. CPU panel fitter (Can be done anytime after CPU pipe is off) ling CPU embedded DisplayPort A Disable port Disable CPU DisplayPort PLL in the DisplayPort A register Disable PCH 120MHz clock source output to CPU
 Disable Disable Disable Disable Disable Disable Disable Wait for If disable Disable If disable 	Disable sequence Panel backlight panel power through panel power sequencing CPU planes (VGA or hires) K-A] Disable CPU panel fitter CPU pipe r CPU pipe off status (CPU pipe config register pipe state) ling DisplayPort on PCH, write the DisplayPort control register bit 31 to 0b. CPU panel fitter (Can be done anytime after CPU pipe is off) ling CPU embedded DisplayPort A Disable port Disable CPU DisplayPort PLL in the DisplayPort A register Disable PCH 120MHz clock source output to CPU sabling port on PCH:



- d. Wait for PCH transcoder off status (PCH transcoder config register transcoder state)
- e. [DevCPT] Disable Transcoder DisplayPort Control if DisplayPort was used
- f. [DevCPT] Disable Transcoder DPLL Enable bit in DPLL_SEL
- g. Disable PCH DPLL (Can be done anytime after PCH ports and transcoder are off)
- h. If no other PCH transcoder is enabled
 - i. Switch from PCDclk to Rawclk in PCH FDI Receiver
 - ii. [DevSNB] Disable CPU FDI Transmitter PLL
 - iii. Disable PCH FDI Receiver PLL
- 11. If SSC is no longer needed, disable PCH SSC modulator
- 12. If clock reference no longer needed, disable PCH clock reference source

Pipe timings change

Use complete disable sequence followed by complete enable sequence with new mode programmings.

Please note that pipe source size can be changed on the fly when panel fitting is enabled.

Notes

CPU FDI Transmitter should not be set to idle while PCH transcoder is enabled as this will cause PCH transcoder underflow.



2. North Shared Functions (40000h– 4FFFFh)

2.1 VGA Control Registers

	VGA	CNTRL-VG	A Display Plane Control Register	
Project: Default Val Access:	ffset: 41000 All ue: 00002 R/W	h		
Size (in bits		el fitting to be enable	ed	
Bit	requiree pair		Description	
31	BFFFF men settings. VC enabling the enabled. N VGA. See t Firmware ca	All e: 0b disable the VGA com ory aperture access GA display should on VGA, most display j ote: The VGA SR01 he VGA Registers Ba un temporarily overrid	VGA Display Enabled npatible display mode. It has no effect on VGA register or es which are controlled by the PCI configuration and VGA ly be enabled if all display planes other than VGA are dis- planes need to stay disabled, only the VGA popup (curso screen off bit must be programmed when enabling and d spec. de VGA display to be disabled, causing this bit to become this bit should be programmed to 1b even if it already rea	A register abled. After r A) can be isabling 1b (Disable).
	Value	Name	Description	Project
	0b	Enable	VGA Display Enabled	All
	1b	Disable	VGA Display Disabled	All
30	Reserved	Project: All	Format: PBC	



29	VGA Pip	e_Select					
	Project:	-	All				
	Default Value: 0b						
	changed	only when t		etermines which pipe is to receive the VGA display data. T play is in the disabled state via the VGA display disable bi			
	Value	Name		Description Project	rt		
	0b	PipeA		Selects Assigns the VGA display to Pipe A All			
	1b	PipeB		Selects Assigns the VGA display to Pipe B All			
28:27	Reserved	d Proje	ect: All	Format: PBC			
26	VGA_Bo	rder_Enab	le				
	Project:		All				
	Default Value: 0b						
	Default V	alue:	dU				
	This bit d		if the VGA b	oorder areas are included in the active display area and do	or do not		
	This bit d appear o The bord	letermines i n the port o er if enable	if the VGA b output. d will be sca	border areas are included in the active display area and do aled along with the pixel data. Setting this bit allows the po er area of the image.			
	This bit d appear o The bord	letermines i n the port o er if enable	if the VGA b output. d will be sca	aled along with the pixel data. Setting this bit allows the po er area of the image.			
	This bit of appear o The bord positione	letermines i n the port o er if enabled d overlappin	if the VGA b butput. d will be sca ng the borde Descripti	aled along with the pixel data. Setting this bit allows the po er area of the image. ion der areas are not included in the image size calculations	opup to be		
	This bit of appear of The bord positioned Value	letermines i n the port o er if enable d overlappin Name	f the VGA b butput. d will be scang the border Descripti VGA Bord for active VGA Bord	aled along with the pixel data. Setting this bit allows the po er area of the image. ion der areas are not included in the image size calculations	Project		
25	This bit of appear of The bord positioned Value Ob	letermines i n the port o er if enabled d overlappin Name Disable Enable	f the VGA b butput. d will be scang the border Descripti VGA Bord for active VGA Bord display ar	aled along with the pixel data. Setting this bit allows the po er area of the image. ion der areas are not included in the image size calculations area. der areas are enabled and passed to the display pipe for	Project		
<u>25</u> 24	This bit c appear o The bord positioned Ualue Ob 1b	letermines i n the port o er if enable d overlappin Name Disable Enable d Proj	f the VGA b butput. d will be scang the border Descripti VGA Bord for active VGA Bord display ar	aled along with the pixel data. Setting this bit allows the po er area of the image. ion der areas are not included in the image size calculations area. der areas are enabled and passed to the display pipe for nd used in the image size calculations. Format: PBC	Project		
-	This bit c appear o The bord positioned Ualue Ob 1b	letermines i n the port o er if enable d overlappin Name Disable Enable d Proj	f the VGA boutput. d will be scang the border Descripti VGA Bord for active VGA Bord display ar ect: All	aled along with the pixel data. Setting this bit allows the po er area of the image. ion der areas are not included in the image size calculations area. der areas are enabled and passed to the display pipe for nd used in the image size calculations. Format: PBC	Project		
-	This bit c appear o The bord positioned Value 0b 1b Reserved Pipe_Co	letermines i n the port o er if enable d overlappin Name Disable Enable Enable d Proju	f the VGA b butput. d will be scange the border VGA Bord for active VGA Bord display ar ect: All Conversio	aled along with the pixel data. Setting this bit allows the po er area of the image. ion der areas are not included in the image size calculations area. der areas are enabled and passed to the display pipe for nd used in the image size calculations. Format: PBC	Project		
-	This bit c appear o The bord positioned 0b 1b 1b Reserved Pipe_Co Project: Default V This bit e	letermines i n the port o er if enable d overlappin Disable Enable Enable d Proju lor_Space_ alue:	f the VGA boutput. d will be scang the border Descripti VGA Bord for active VGA Bord display ar ect: All Conversio All Ob e color space	aled along with the pixel data. Setting this bit allows the po er area of the image. ion der areas are not included in the image size calculations area. der areas are enabled and passed to the display pipe for nd used in the image size calculations. Format: PBC	Project All All		
-	This bit c appear o The bord positioned 0b 1b 1b Reserved Pipe_Co Project: Default V This bit e	letermines i n the port o er if enable d overlappin Disable Enable Enable d Proju lor_Space_ alue:	f the VGA boutput. d will be scang the border Descripti VGA Bord for active VGA Bord display ar ect: All Conversio All Ob e color space	aled along with the pixel data. Setting this bit allows the pole er area of the image.	Project All All e CSC		
-	This bit c appear o The bord positioned 0b 1b Reserved Pipe_Co Project: Default V This bit e registers	letermines i n the port o er if enabled d overlappin Disable Enable Enable d Proju lor_Space_ alue: nables pipe must be se	if the VGA b butput. d will be scange the border VGA Bord for active VGA Bord display ar ect: All Conversio All Ob e color space t to match the	aled along with the pixel data. Setting this bit allows the pole er area of the image.	Project All All		



00			A Display Plane Control Regi	
23	VGA_Pale Project:	ette_Read_Select		
	Default Va			
	This bit or		lay pipe devices and determines which palette VG	GA palette read
		tte reads are reads from	m I/O address 0x3c9.	
	Value	Name	Description	Project
	0b	Palette A	VGA palette reads will access Palette A	All
	1b	Palette B	VGA palette reads will access Palette B	All
22	VGA_Pale	ette_A_Write_Disable		
	Project:	All		
	Default Va	alue: Ob		
			e VGA palette writes will have as a destination. C re disabled, writes will not affect the palette conte	
	VGA palet	tte writes are writes to	I/O address 0x3C9h.	
	Value	Name	Description	Project
	0b	Update Palette A	VGA palette writes will update Palette A	All
	1b	Not Update Palette A	VGA palette writes will not update Palette A	All
04				
21	VGA_Pale	ette_B_Write_Disable	•	
21	VGA_Pale Project:	ette_B_Write_Disable All	3	
21		All	•	
21	Project: Default Va This deter	All alue: 0b mines which palette th	e VGA palette writes will have as a destination. C re disabled, writes will not affect the palette conte	
21	Project: Default Va This deter can be the	All alue: 0b mines which palette th	e VGA palette writes will have as a destination. C re disabled, writes will not affect the palette conte	
21	Project: Default Va This deter can be the	All alue: 0b mines which palette th e destination. If both a	e VGA palette writes will have as a destination. C re disabled, writes will not affect the palette conte	
21	Project: Default Va This deter can be the VGA palet	All alue: 0b mines which palette th e destination. If both a tte writes are writes to	e VGA palette writes will have as a destination. C re disabled, writes will not affect the palette conte I/O address 0x3C9h.	nts.
21	Project: Default Va This deter can be the VGA palet	All alue: 0b rmines which palette th e destination. If both a tte writes are writes to Name	e VGA palette writes will have as a destination. C re disabled, writes will not affect the palette conte I/O address 0x3C9h. Description VGA palette writes will update Palette B	Project
21	Project: Default Va This deter can be the VGA pale Value 0b 1b	All alue: 0b mines which palette th e destination. If both a tte writes are writes to Name Update Palette B	e VGA palette writes will have as a destination. C re disabled, writes will not affect the palette conte I/O address 0x3C9h. Description VGA palette writes will update Palette B VGA palette writes will not update Palette B	Project
	Project: Default Va This deter can be the VGA pale Value 0b 1b	All alue: 0b rmines which palette th e destination. If both a tte writes are writes to Name Update Palette B Not Update Palette B	e VGA palette writes will have as a destination. C re disabled, writes will not affect the palette conte I/O address 0x3C9h. Description VGA palette writes will update Palette B VGA palette writes will not update Palette B	Project
	Project: Default Va This deter can be the VGA palet Value 0b 1b Legacy_V	All alue: 0b rmines which palette th e destination. If both a tte writes are writes to Name Update Palette B Not Update Palette B /GA_8-Bit_Palette_Er All	e VGA palette writes will have as a destination. C re disabled, writes will not affect the palette conte I/O address 0x3C9h. Description VGA palette writes will update Palette B VGA palette writes will not update Palette B	nts. Project All
	Project: Default Va This deter can be the VGA palet 0b 1b Legacy_V Project: Default Va This bit or 8-bits of d the read.	All alue: 0b rmines which palette th e destination. If both a tte writes are writes to Name Update Palette B Not Update Palette B /GA_8-Bit_Palette_Er All alue: 0b hly affects reads and w ata are shifted up two It provides backward of E support for 8-bit pale	e VGA palette writes will have as a destination. C re disabled, writes will not affect the palette conte I/O address 0x3C9h. Description VGA palette writes will update Palette B VGA palette writes will not update Palette B	nts. Project All All All n the 6-bit mode, the ed two bits down on ault state) as well as
	Project: Default Va This deter can be the VGA palet 0b 1b Legacy_V Project: Default Va This bit or 8-bits of d the read. VESA VB	All alue: 0b rmines which palette th e destination. If both a tte writes are writes to Name Update Palette B Not Update Palette B /GA_8-Bit_Palette_Er All alue: 0b hly affects reads and w ata are shifted up two It provides backward of E support for 8-bit pale	e VGA palette writes will have as a destination. Or re disabled, writes will not affect the palette conte I/O address 0x3C9h. Description VGA palette writes will update Palette B VGA palette writes will not update Palette B VGA palette through VGA I/O addresses. In bits on the write (upper two bits are lost) and shift compatibility for original VGA programs (in it's defa	nts. Project All All All n the 6-bit mode, the ed two bits down on ault state) as well as
	Project: Default Va This deter can be the VGA palet 0b 1b Legacy_V Project: Default Va This bit or 8-bits of d the read. VESA VB MMIO pat	All alue: 0b rmines which palette the e destination. If both a tte writes are writes to Name Update Palette B Not Update Palette B /GA_8-Bit_Palette_Er All alue: 0b hly affects reads and w lata are shifted up two It provides backward of E support for 8-bit pale th.	e VGA palette writes will have as a destination. Or re disabled, writes will not affect the palette conte I/O address 0x3C9h. Description VGA palette writes will update Palette B VGA palette writes will not update Palette B A VGA palette through VGA I/O addresses. In bits on the write (upper two bits are lost) and shift compatibility for original VGA programs (in it's defa- ter. It does not affect palette accesses through the	nts. Project All All All n the 6-bit mode, the ed two bits down on ault state) as well as he palette register



19	Reserved							
	Project:	, i i i i i i i i i i i i i i i i i i i	All					
18	Reserved							
7:16	Reserved	Project:	All					
5:12	Reserved							
11:8	Reserved							
7:6	Blink_Dut	y_Cycle						
	Project:	1	All					
	Default Value: 00b							
	Controls th	ne VGA text mod	e blink duty cycle relative to the VGA cursor blink	<u>k duty cycle</u> .				
	Value	Name	Description	Project				
	00b	100%	100% Duty Cycle, Full Cursor Rate	All				
	01b	25%	25% Duty Cycle, ½ Cursor Rate	All				
	10b	50%	50% Duty Cycle, ½ Cursor Rate	All				
		75%	75% Duty Cycle, 1/2 Cursor Rate	All				
	11b	VSYNC_Blink_Rate Project: All						
5:0		link_Rate		Project: All				



2.2 Sine ROM Registers

2.2.1 2.4.1 SINE_ROM—Sine ROM

	SINE_ROM - Sine ROM								
Register [•]	Туре:	MMIO							
Address:		42200h-42203h							
Project:		All							
Default V	alue:	0000000h							
Access:		R/W Special							
Size (in b	its):	32							
angle is wi	ritten to bits	sed to calculate a sine (or cosine). The intent is to enable calculation of filter coefficients. The [16:6] as a 11 bit, fixed point, 0.11 value (example for setting different degrees below). Then bits [16:6] as a 11 bit, fixed point, 1.10 value.							
DWord	Bit	Description							
0	31:17	Reserved							

0	31:17	Reserved	
		Project:	All
	16:6	Sine	
		Default Value:	Ob
		Project:	All
		Write the angle, read the sine	
		Programming Notes	Project
		Examples of values to write:0000000000 = 0 or 360 degrees01000000000 = 90 degrees10000000000 = 180 degrees11000000000 = 270 degrees	All
	5:0	Reserved	
		Project:	All



2.3 Power Measurement Registers

These registers are read by the PMU to get information for use in device power estimation.

2.3.1 DE_POWER1 – Display Engine Power Register 1

	DE_	_POWER	1 – Display E	ngine Power Re	egister	1
Register 1 Address (Project: Default Va Access: Size (in bi	Dffset: 42400 DevSi alue: 00000 Read	9h-42403h NB 9000h				
Bit			De	escription		
31:8	Reserved	Project:	All		Format:	MBZ
7:4	Transmit_L	anes_Enable	d			
	Project:		All			
	Range		012			
	The total nu	mber of eDP &	& FDI lanes enabled.			
3:2	Enabled_Pa	anel_Fitters				
	Project:		All			
	Range		02			
	Each enable	ed panel fitter	consumes an additiona	I xxmW of power.		
1:0	Enabled_D	PLLs				
	Project:		All			
	Range		02			
	Each DPLL	enabled cons	umes xxmW of power.			



2.3.2 **DE_POWER2 – Display Engine Power Register 2**

		DE_POWER2 – Display Engine Power Regi	ister 2	
Register Type: Address Offset: Project: Default Value: Access: Size (in bits):		MMIO 42404h-42407h DevSNB 0000000h Read Only 32		
Bit		Description		
31:0	This	<pre>pandwidth_counter counter increments on every cache line put arriving at the DE. The band g the difference between two reads at a known interval. The counter is o</pre>		

2.4 DPFC Control Registers (43200h–433FFh)

2.4.1 DPFC_CB_BASE – DPFC Compressed Buffer Base Address

L	PFC	CB	_BASE -	- DPFC	Compresse	d Buffer Base A	ddress
Register Type:		MMIO					
Address Offset: Project: Default Value:		43200h	n-43203h				
		All					
		000000)00h				
Access:		R/W					
Size (in bit	s):	32					
The conter	nts of t	his regis	ster can not	be change	d while compression	on is enabled.	
	1						
Bit					Description		
Bit 31:28	Rese	erved	Project:	All	Description	Format:	MBZ
			Project: d_Frame_But				MBZ
31:28	Com	pressed	d_Frame_But	ifer_Offset_	Address	Format:	All
31:28	Com This	pressed register	d_Frame_But	ffer_Offset_ et of the Cor	Address	Format: Project:	All



2.4.2 DPFC_CONTROL— DPFC Control

		DPFC_	CON	ITROL— DPFC Control			
Project: Default Va Access: Size (in b	Dffset: 432 All alue: 000 R/V its): 32	208h-4320Bh 000000h V	chang	ged, except bit 31, while compression is	enabled		
Bit				Description			
31	Enable_Frame_Buffer_Compression Project: All Default Value: 0b This bit is used to globally enable DPFC function at the next Vertical Blank start. Frame buffer compression can only be enabled after selected primary plane has been enabled or more vertical blanks and must be disabled before disabling the primary plane.						
	Value	Name		Description		Project	
	0b	Disable		Disable frame buffer compression		All	
	1b	Enable		Enable frame buffer compression		All	
30	Plane_Se Project: Default V	All			Projec		
	Value	Name		scription	-	t	
	Value Ob 1b	NamePlane APlane B	Pla	scription Ine A Ine B	All	t	
29	0b 1b	Plane A Plane B nce_Enable All alue: 0b	Pla Pla Dis	Ine A Ine B scription splay Buffer is not in a CPU fence. No modif	All		
29	0b 1b CPU_Fer Project: Default V Value	Plane A Plane B All alue: 0b Name	Pla Pla Dis are	scription	All	Project	
29 28	0b 1b CPU_Fer Project: Default V. Value 0b	Plane A Plane B All alue: 0b Name No CPU Disp Buf CPU Disp Buf	Pla Pla Dis are	scription splay Buffer is not in a CPU fence. No modif allowed from CPU to the Display Buffer	All All ications	Project All All	
	0b 1b CPU_Fer Project: Default V. Value 0b 1b	Plane A Plane B Plane B Plane B Plane B Plane B NoCe_Enable All All All CPU Disp Buf CPU Disp Buf Project: /	Pla Pla Pla Dis are Dis	scription splay Buffer is not in a CPU fence. No modif allowed from CPU to the Display Buffer splay Buffer exists in a CPU fence	All All ications	Project All All	



25	Persister	nt_Mode								
	Project: All									
	Default Value: 0b									
	Value	Name	Description	1		Project				
	0b	Non Persistent	Non Persist	ent Mode		All				
	1b	Persistent	Persistent N	lode. Enable the invalid modify q	qualify from CS	All				
4:8	Reserved	ł								
:6	Compres	sion_Limit								
	Project:	A	.11							
	Default V	alue: 0	b							
	This register sets a minimum limit on compression. It is also used to determine the size of the compressed buffer:									
	Compression Ratio 1, Pixel Format 16 bpp - Not Supported									
	Compression Ratio 1, Pixel Format 32 bpp - Supported (CFB=FB)									
	Compression Ratio 1/2, Pixel Format 16 bpp - Supported (CFB=FB)									
	С	ompression Ratio	1/2, Pixel Forma	at 32 bpp - Supported (CFB=1/2 F	FB)					
	С	ompression Ratio	1/4, Pixel Forma	at 16 bpp - Supported (CFB=1/2F	B)					
	С	ompression Ratio	1/4, Pixel Forma	at 32 bpp – Supported (CFB=1/4 I	FB)					
	FB = Frame Buffer Size									
	CFB = Compressed Frame Buffer Size									
	V	alue	Name	Description	Project					
	0b	[Def	fault]							
	00b	1:1		1:1 compression, compressed buffer is the same size as the uncompressed buffer	All					
	01b	2:1		2:1 compression, compressed buffer is one half the size of the uncompressed buffer.	All					
	10b	4:1		4:1 compression, compressed buffer is one quarter the size of the uncompressed buffer.	All					
				-						



5:4	Write Back Watermark									
	Default Value:									
	Project:		All							
			for this amount of data mode must be a 1, or t							
	Value	Name	Description	Project						
	0b	[Default]								
	00b	4 cache lines	4 cache lines	All						
	01b	8 cache lines	8 cache lines	All						
	1Xb	Reserved	Reserved	All						
3:0	CPU_Fence_Number									
	Project:	All								
	Default Value: 0b									
		This field specifies the CPU visible FENCE number corresponding to the placement of the uncompressed frame buffer.								
	in the DPFC_CON	TROL_SA register CPU	modify message when JFNCNUM field. The fo ust be programmed to (ence field in the FBC H						

2.4.3 DPFC_RECOMP_CTL — DPFC ReComp Control

Dealerten 7									
Register 1		-							
		0Ch-4320Fh							
Project:	All								
Default Va	alue: 000	00000h							
Access:	R/V	V							
Size (in bi	t <mark>s):</mark> 32								
Bit					Description	n			
31:28	Reserved	ł				Project:	All	Format:	MBZ
27	Enable_ReComp_Stall								
	Project:		All						
	Default V	alue:	0b						
	Value	Name	Des	cription					Project
	0b	Disable [Default]	Disa	able					All
	1b	Enable	Ena	blo					All



26:16	ReComp_Stall_Invalidation_Watermark	Project: All					
	If this many or more invalidations occur in one fram watermark, then start the recomp timer.	e, stop compression until the number falls below					
15:6	Reserved Project: All	Format: MBZ					
5:0	ReCompression_Timer_Count Project: All After invalidations fall below watermark, wait this many frames before restarting the compressor. Project: All						
	A 0 means restart compression on the following frame.						

2.4.4 DPFC_STATUS — DPFC Status

		DPF	C_STATUS -	– DPFC Status	
Register T	ype: MMIO				
Address O	offset: 43210	n-43213h			
Project:	All				
Default Va	lue: 000000)00h			
Access:	Read C	Dnly			
Size (in bit	s): 32				
Bit			De	escription	
31:27	Reserved	Project:	All	Format:	MBZ
26:16	RC_Invalida	ted_Segment_	Count	Proje	ect: [DevSNB]
		h vblank, this fi ne, for RC invali		nber of segments that have been inv	alidated for the
15:11	Reserved	Project:	All	Format:	MBZ
10:0	Compressed	d_Segment_Co	ount	Proje	ect: All
			eld indicates the num the previous frame.	nber of segments that were fetched f	rom the

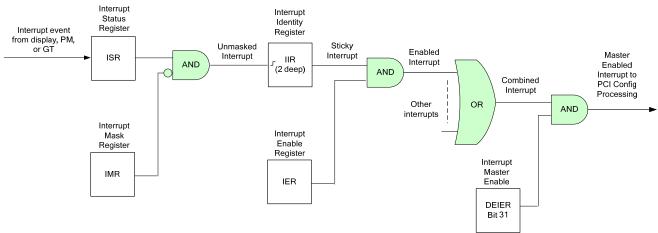


2.4.5 DPFC_CPU_Fence_Offset — Y Offset CPU Fence Base to Display Buffer Base

DPFC_	CPU_Fence_Offset — Y Offset CPU Fence Base to Display Buffer Base
C	fset: 43218h-4321Bh All ue: 0000000h R/W
	RT Display Buffer Vrtmodifyoffset Vdispoffset
Bit	Description
31:22	Reserved Project: All Format: MBZ
21:0	Yfence_disp Project: All Y offset from the CPU fence to the Display Buffer base. Image: CPU fence is always programmed to match the Display Buffer base, so this offset must be programmed to 0 to match.



2.5 Interrupt Control Registers



First Level Interrupts in Display

For every first level interrupt bit:

Interrupt event comes in from display, PM, or GT.

There may be more levels of interrupt handling behind each event. For example the PCH Display interrupt event is the result of the SDE interrupt registers.

Interrupt event goes to Interrupt Status Register (ISR) where live status can be read back.

Interrupt event is ANDed with inverted Interrupt Mask Register (IMR) so only unmasked interrupts will proceed.

Unmasked interrupt rising edge sets sticky bit in Interrupt Indentity Register (IIR).

IIR is cleared by writing a 1b to it.

<u>IIR can queue up to two interrupt events</u>. When the IIR is cleared, it will set itself again after one clock if a second event was stored.

Sticky interrupt is ANDed with Interrupt Enable Register (IER) so only enabled interrupts will proceed.

All enabled interrupts are then ORed to create the combined interrupt.

Combined interrupt is ANDed with Master Enable (DEIER Bit 31) so only master enabled interrupt will proceed.

Master enabled interrupt then goes to PCI device 2 configuration registers PCISTS2, PCICMD2, and MC which control the MSI and line interrupt.

A Function Level Reset (FLR) or Warm Reset will reset all interrupt logic in display, causing the master enabled interrupt to deassert.



2.5.1 Display Engine Interrupt Registers Bit Definition

Display Engine Interrupt Registers Bit Definition

Project: All Size (in bits): 32

Display Engine (DE) interrupt bits come from events within the display engine, except for some which explicitly list a non-display engine source. The DEIIR and GTIIR and PMIIR are ORed together to generate the CPU interrupt.

The Display Engine Interrupt Control Registers all share the same bit definitions from this table.

Bit	Description				
31	Master_Interrupt_Control Project: All Format:				
	This bit exists only in the DEIER Display Engine Interrupt Enable Register.				
	This is the master control for the Display to CPU interrupt. This bit must be set to 1 for any interrupts to propagate to the system.				
30	Reserved Project: All Format:				
29	Sprite_Plane_B_flip_done Project: All Format:				
	This is an active high pulse when a sprite plane B flip is done.				
28	Sprite_Plane_A_flip_done Project: All Format:				
	This is an active high pulse when a sprite plane A flip is done.				
27	Primary_Plane_B_flip_done Project: All Format:				
	This is an active high pulse when a primary plane B flip is done.				
26	Primary_Plane_A_flip_done Project: All Format:				
	This is an active high pulse when a primary plane A flip is done.				
25	Reserved Project: DevSNB Format:				
24	GTT_fault Project: All Format:				
	This is an active high level while either of the GTT Fault Status register bits are set.				
23	Poison Project: All Format:				
	This is an active high pulse on receiving the poison message.				
21	PCH_Display_interrupt_event Project: All Format:				
	This is an active high level while there is an interrupt being generated by the PCH Display. It will stay asserted until the interrupts in the PCH Display are all cleared. Only the rising edge of the PCH Display interrupt will cause the IIR to be set here, so all PCH Display Interrupts, including back to back interrupts, must be cleared before a new PCH Display Interrupt can cause the IIR to be set here.				
20	AUX_Channel_A Project: All Format:				
	This is an active high pulse on the AUX A done event.				
19	DP_A_Hotplug Project: All Format:				
	This is an active high level while either of the Digital Port A Hot Plug Interrupt Detect Status register bits are set.				
18	GSE Project: DevSNB Format:				
	This is an active high pulse on the GSE system level event.				



	Display Engine Interrupt Regist	ters B	it C	Definition		
17	DPST_histogram_event F	Project:	All	Format:		
	This is an active high pulse on the DPST histogram event.					
16	DPST_phase_in_event F	Project:	All	Format:		
	This is an active high pulse on the DPST phase in event.					
15	Pipe_B_vblank F	Project:	All	Format:		
	This is an active high level for the duration of the Pipe B ve	ertical bla	nk.			
14	Pipe_B_even_field F	Project:	All	Format:		
	This is an active high level for the duration of the Pipe B in	terlaced e	even	field.		
13	Pipe_B_odd_field F	Project:	All	Format:		
	This is an active high level for the duration of the Pipe B in	terlaced o	odd f	ield.		
12	Pipe_B_line_compare F	Project:	All	Format:		
	This is an active high level for the duration of the selected	Pipe B sc	an li	nes.		
11	Pipe_B_vsync F	Project:	All	Format:		
	This is an active high level for the duration of the Pipe B ve	ertical syn	IC.			
10	Pipe_B_CRC_done F	Project:	All	Format:		
	This is an active high pulse on the Pipe B CRC done.					
9	Pipe_B_CRC_error F	Project:	All	Format:		
	This is an active high pulse on the Pipe B CRC error.					
8	Pipe_B_FIFO_underrun F	Project:	All	Format:		
	This is an active high level for the duration of the Pipe B FIFO underrun.					
7	Pipe_A_vblank F	Project:	All	Format:		
	This is an active high level for the duration of the Pipe A ve	ertical bla	nk.			
6	Pipe_A_even_field F	Project:	All	Format:		
	This is an active high level for the duration of the Pipe A in	terlaced e	even	field.		
5	Pipe_A_odd_field F	Project:	All	Format:		
	This is an active high level for the duration of the Pipe A interlaced odd field.					
4	Pipe_A_line_compare F	Project:	All	Format:		
	This is an active high level for the duration of the selected Pipe A scan lines.					
3	Pipe_A_vsync F	Project:	All	Format:		
	This is an active high level for the duration of the Pipe A vertical sync.					
2	Pipe_A_CRC_done F	Project:	All	Format:		
	This is an active high pulse on the Pipe A CRC done.					
1	Pipe_A_CRC_error F	Project:	All	Format:		
	This is an active high pulse on the Pipe A CRC error.					
0	Pipe_A_FIFO_underrun F	Project:	All	Format:		
	This is an active high level for the duration of the Pipe A FI	-				



2.5.2 DEISR — Display Engine Interrupt Status Register

DEISR — Display Engine Interrupt Status Register

Register Type:	MMIO
Address Offset:	44000h-44003h
Project:	All
Default Value:	00000000h
Access:	Read Only
Size (in bits):	32

The ISR register contains the non-persistent value of all interrupt status bits. The IMR register selects which of these interrupt conditions are reported in the persistent IIR (i.e., set bits must be cleared by software). Bits in the IER are used to selectively enable IIR bits to cause CPU interrupts.

Bit		Description			
1:0	Display_ Interrupt Status_B	_			
	Project:	All			
	Format:	Display E Definition	Display Engine Interrupt Registers Bit Definition		
	FormatDesc: Display Engine (DE) interrupt bits come from events within the display engine, except for some which explicitly list a non-display engine source. The DEIIR and GTIIR and PMIIR are ORed together to generate the CPU interrupt.				
		inton upt.			
		The Displa	ay Engine Interrupt Control Registers all share the sa from this table.	ame bit	
	Value	The Displa			
	Value Ob	The Displa definitions	from this table.		
		The Displa definitions	from this table. Description	Project	
	0b 1b	The Displa definitions Name Condition Doesn't exist	from this table. Description Interrupt Condition currently does not exist	Project All	



2.5.3 DEIMR — Display Engine Interrupt Mask Register

	DEIMR -	– Display Eng	gine Interrupt M	ask Register	
Register Type: MMIO Address Offset: 44004h-44007h Project: All Default Value: FFFFFFFh Access: R/W Size (in bits): 32 The IMR register is used by software to control which		hich Interrupt Status Re	gister bits are "masl	ked" or	
"unmasked in the IIR u	". "Unmasked" bits	s will be reported in	the IIR, possibly triggeri s will not be reported in t	ng a CPU interrupt,	and will persist
Bit			Description		
31:0	Display Engine In	terrupt Mask Bits			
	Project:		All		
	Format: Display Engine Interrupt Registers Bit Definition				
	FormatDesc: Display Engine (DE) interrupt bits come from events within the display engine, except for some which explicitly list a non-display engine source. The DEIIR and GTIIR and PMIIR are ORed together to generate the CPU interrupt. The Display Engine Interrupt Control Registers all share the same bit definitions from this table. This field contains a bit mask which selects which interrupt bits from the ISR are reported in the II			in the IIR.	
	Value	Name	Description	Project	
	Ob	Not Masked	Not Masked – will be reported in the IIR	All	
			Masked – will not be reported in the IIR	All	



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2.5.4 DEIIR — Display Engine Interrupt Identity Register

	DEIIR — Display Engine Interrupt Identity Register
Register Type:	MMIO
Address Offset:	44008h
Project:	All
Default Value:	0000000h
Access:	R/W Clear
Size (in bits):	32
The IIR register co	ontains the interrupt bits that are "unmasked" by the IMR and thus can generate CPU interrupts (if

The IIR register contains the interrupt bits that are "unmasked" by the IMR and thus can generate CPU interrupts (if enabled via the IER). When a CPU interrupt is generated, this should be the first register to be interrogated to determine the source of the interrupt. Writing a '1' into the appropriate bit position within this register clears interrupts.

Bit	Description				
31:0	Display Engine Inte	errupt Identity Bits			
	Project:		All		
	Format:		Display Engine I Definition	nterrupt Registers Bit	
	FormatDesc:		come from even engine, except fo explicitly list a no source. The DEI	on-display engine IR and GTIIR and I together to generate	
			The Display Eng Registers all sha definitions from t		
	This field holds the persistent values of the interrupt bits from the ISR which are used the IMR. If enabled by the IER, bits set in this register will generate a CPU interrupt this register will remain set (persist) until the interrupt condition is cleared via soft writing a 1' to the appropriate bit(s). For each bit, the IIR can store a second pending interrupt if two or more of the same interroccur before the first condition is cleared. Upon clearing the interrupt, the IIR bit will moment then return high to indicate there is another interrupt pending.			upt. Bits set in ware by upt conditions	
	Value	Name	Description	Project	
	Ob	Condition Not Detected	Interrupt Condition Not Detected	All	
	1b	Condition Detected	Interrupt Condition Detected (may or may not have actually generated a CPU interrupt)	All	



2.5.5 DEIER — Display Engine Interrupt Enable Register

	DEIER — D	Display Engine	e Interrupt En	able Registe	r	
Project: Default Va Access: Size (in bit The IER re	ype: MMIO ffset: 4400Ch All lue: 00000000h R/W	errupt enable bit for e	each interrupt bit in t	he IIR register. A c		
Bit			Description			
31:0	Display Engine Inter	rupt Enable Bits				
	Project:	All	All			
	Format: Display Engine Interrupt Registers Bit Definition					
	FormatDesc: The bits in this registe Interrupt Identity Regist interrupts to propagate	within the display list a non-display and PMIIR are O interrupt. The Display Engi the same bit defii r enable a CPU interru ster becomes set. The		me which explicitly EIIR and GTIIR ate the CPU egisters all share enever the correspon		
	Value	Name	Description	Project		
	0b	Disable	Disable	All	1	
		Enable	Enable	All		



2.5.6 GT Interrupt Registers Bit Definition

	GT Interrupt Registers E	Bit Definition
Project: Size (in bi	All ts): 32	
The DEIIR	and GTIIR and PMIIR are ORed together to generate the O	CPU interrupt.
The GT Int	errupt Control Registers all share the same bit definition fro	om this table.
Bit	Descriptio	on
31	Reserved Project: DevSNB	Format:
30	Blitter_AS_Context_Switch_Interrupt	
	Project: DevSNB	
29	Blitter_page_directory_faults	
	Project: DevSNB	
28:27	Reserved Project: DevSNB	Format:
26	Blitter_MI_FLUSH_DW_notify	
	Project: DevSNB	
25	Blitter_Command_Streamer_error_interrupt	
	Project: DevSNB	
24	Billter_MMIO_sync_flush_status	
	Project: DevSNB	
23	Reserved Project: DevSNB	Format:
22	Blitter_Command_Streamer_MI_USER_INTERRUPT	
	Project: DevSNB	
21	Reserved Project: DevSNB	Format:
20	Video_AS_Context_Switch_Interrupt	
	Project: DevSNB	



19	Video_page_directory_faults				
	Project: DevSNB				
18	Video_Command_Streamer_Watchdog_counter_exceeded				
	Project: DevSNB				
17	Reserved Project: DevSNB	Format:	MBZ		
16	Video_MI_FLUSH_DW_notify				
	Project: DevSNB				
15	Video_Command_Streamer_error_interrupt				
	Project: DevSNB				
14	Video_MMIO_sync_flush_status				
	Project: DevSNB				
13	Reserved Project: DevSNB	Format:			
12	Video_Command_Streamer_MI_USER_INTERRUPT				
	Project: DevSNB				
1:9	Reserved Project: DevSNB	Format:			
8	Render_AS_Context_Switch_Interrupt				
	Project: DevSNB				
7	Render_page_directory_faults				
	Project: DevSNB				
6	Render_Command_Streamer_Watchdog_counter_exceeded				
	Project: DevSNB				
5	Reserved Project: DevSNB	Format:			
4	Render_PIPE_CONTROL_notify				
	Project: DevSNB				
3	Render_Command_Streamer_error_interrupt				
	Project: DevSNB				
2	Render_MMIO_sync_flush_status Project: DevSNB				



	GT Interrupt Registers Bit Definition				
1	Reserved				
	Project:	DevSNB			
0	Render_Command_Streamer_MI_USER_INTERRUPT				
	Project:	DevSNB			

2.5.7 GTISR — GT Interrupt Status Register

		GTISR — GT	Interrupt Status Register			
Register T	ype: MM	AIO				
Address Offset: 44010h		010h				
Project: All						
Default Va	lue: 000	00000h				
Access:	Rea	ad Only				
Size (in bit						
of these in	terrupt cor	nditions are reported in t	value of all interrupt status bits. The IMR reg the persistent IIR (i.e., set bits must be cleared a IIR bits to cause CPU interrupts.			
Bit	Description					
31:0	GT_Interrupt_Status_Bits					
	Project:	All	All			
	Format:	GT Interr	GT Interrupt Registers Bit Definition			
	Format D		The DEIIR and GTIIR and PMIIR are ORed together to generate the CPU interrupt.			
			nterrupt Control Registers all share the same bit from this table.			
	This field contains the non-persistent values of all interrupt status bits.					
	Value	Name	Description	Project		
	0b	Condition Doesn't Exist	Interrupt Condition currently does not exist	All		
	1b	Condition Exists	Interrupt Condition currently exists	All		
	Programming Notes					
	Some inputs to this register are short pulses; therefore software should not expect to use this register to sample these conditions.					



2.5.8 GTIMR — GT Interrupt Mask Register

	GTIMR — GT Interrupt Mask Register				
Register Type:	MMIO				
Address Offset:	44014h				
Project:	All				
Default Value:	FFFFFFh				
Access:	R/W				
Size (in bits):	32				
The IMR register	; is used by software to control which Interrupt Status Register bits are "masked" or				

The IMR register is used by software to control which Interrupt Status Register bits are "masked" or "unmasked". "Unmasked" bits will be reported in the IIR, possibly triggering a CPU interrupt, and will persist in the IIR until cleared by software. "Masked" bits will not be reported in the IIR and therefore cannot generate CPU interrupts.

For command streamer interrupts DO NOT use this register to mask interrupt events. Instead use the individual command streamer MASK bits.

			Description			
G	T Interrupt Masl	< Bits				
F	Project:		All	All GT Interrupt Registers Bit Definition		
F	Format:		GT Interrupt Reg			
F	FormatDesc:			GTIIR and PMIIR are o generate the CPU		
				Control Registers all		
			table.			
т	his field contains	a bit mask which selec				
Т	his field contains	a bit mask which selec	table.			
			table.	the ISR are reported		



2.5.9 GTIIR — GT Interrupt Identity Register

GTIIR - GT Interrupt Identity Register								
Register Type: MMIO								
Address:			44018h-4401Bh	44018h-4401Bh				
Project: All								
Default Va	alue:		0000000h					
Access:			R/W Clear					
Size (in bi	ts):		32					
enabled via determine clears int	The IIR register contains the interrupt bits that are unmasked by the IMR and thus can generate CPU interrupts (if enabled via the IER). When a CPU interrupt is generated, this should be the first register to be interrogated to determine the source of the interrupt. Writing a 1' into the appropriate bit position within this register clears interrupts.							
DWord	Bit			cription				
0	31:0	GT Interrupt I	-					
		Project:	All					
		Format:	Format: GT Interrupt Registers Bit Definition					
		FormatDesc: The DEIIR and GTIIR and PMIIR are ORe together to generate the CPU interrupt.						
		The GT Interrupt Control Registers all share the same bit definition from this table.						
		This field holds the persistent values of the interrupt bits from the ISR which are unmasked by the IMR. If enabled by the IER, bits set in this register will generate a CPU interrupt. Bits set in this register will remain set (persist) until the interrupt condition is cleared via software by writing a 1' to the appropriate bit(s). For each bit, the IIR can store a second pending interrupt if two or more of the same interru						
		conditions occur before the first condition is cleared. Upon clearing the interrupt, the IIR bit will momentarily go low, then return high to indicate there is another interrupt pending.						
		Value	Name	Description	Project			
		0b	Condition Not Detected	Interrupt Condition Not Detected	All			
		1b	Condition Detected	Interrupt Condition Detected (may or may not have actually generated a CPU interrupt)	All			



2.5.10 GTIER — GT Interrupt Enable Register

GTIER - GT Interrupt Enable Register				
Register Type:	ММЮ			
Address:	4401Ch-4401Fh			
Project:	All			
Default Value:	0000000h			
Access:	R/W			
Size (in bits):	32			
The IER register contains an interrupt enable bit for each interrupt bit in the IIR register. A disabled interrupt will still				

The IER register contains an interrupt enable bit for each interrupt bit in the IIR register. A disabled interrupt will still appear in the Interrupt Identity Register to allow polling of interrupt sources.

DWord	Bit	Description			
0	31:0	GT Interrupt Enable Bits			
		Project:		All	
		Format:		GT Interrupt Reg	sisters Bit Definition
		bit in the Interrupt Iden	FormatDesc: The DEIIR and GTIIR and PMIIR are ORed together to generate the CPU interrupt. The GT Interrupt Control Registers al share the same bit definition from this table. he bits in this register enable a CPU interrupt to be generated whenever the correspon it in the Interrupt Identity Register becomes set. The DEIER master interrupt control bit must be set to 1 for any interrupts to propagate to the system.		o generate the CPU Control Registers all bit definition from this enever the corresponding
		Value	Name	Description	Project
		0b	Disable	Disable	All
		1b	Enable	Enable	All



2.5.11 Power Management Interrupt Registers Bit Definition [DevSNB]

Power Management Interrupt Registers Bit Definition [DevSNB]

Project:	DevSNB			
Size(in bit				
The DEIIR a	and GTIIR and PMIIR are ORed together to generate the CPU inte	errupt.		
The Power	Management Interrupt Control Registers all share the same bit de	finition from thi	s tabl	e.
Bit	Description			
31:26	Reserved Project: All	Format:		
25	PCU_pcode2driver_mailbox_event	Project:	All	Format:
24	PCU_Thermal_Event	Project:	All	Format:
23:7	Reserved Project: All	For	mat:	
6	Render_Frequency_Downward_Timeout_During_RC6_inter	rupt Project	:	All Format:
5	RP_UP_threshold_interrupt	Project:	All	Format:
4	RP_DOWN_threshold_interrupt	Project:	All	Format:
3	Reserved Project: All	For	mat:	
2	Render_geyserville_UP_evaluation_interval_interrupt	Project:	All	Format:
1	Render_geyserville_Down_evaluation_interval_interrupt	Project:	All	Format:
0	Reserved Project: All	For	mat:	MBZ



2.5.12 PMISR — PM Interrupt Status Register

	PM	ISR — PM Inter	rrupt Status R	Register	
Project: Default Val Access: Size (in bit The ISR re of these int	ffset: 44020h DevSNB ue: 00000000h Read Only s): 32 gister contains the errupt conditions at	non-persistent value o re reported in the persi ectively enable IIR bits	istent IIR (i.e., set bi	ts must be cleared by	
Bit			Description		
31:0	Power Managemen Project:	nt Interrupt Status Bits	All		
	Format:		Power Manager Registers Bit De		
	FormatDesc:		ORed together t interrupt. The Power Man	GTIIR and PMIIR are to generate the CPU agement Interrupt rs all share the same n this table.	
	This field contains t	he non-persistent values	of all interrupt status b	bits.	1
	Value	Name	Description	Project	
	ОЬ	Condition Does Not Exist	Interrupt Condition currently does not exist	All	
	1b	Condition Exists	Interrupt Condition currently exists	All	
		Programming Notes	;	Project	
		s register are short pulses to use this register to san		All	



2.5.13 PMIMR — Power Management Interrupt Mask Register

PMIMR — Power Management Interrupt Mask Register

Register Type:	MMIO
Address Offset:	44024h-44027h
Project:	DevSNB
Default Value:	FFFFFFFh
Access:	R/W
Size (in bits):	32

The IMR register is used by software to control which Interrupt Status Register bits are "masked" or "unmasked". "Unmasked" bits will be reported in the IIR, possibly triggering a CPU interrupt, and will persist in the IIR until cleared by software. "Masked" bits will not be reported in the IIR and therefore cannot generate CPU interrupts.

For power management interrupts DO NOT use this register to mask interrupt events. Instead use the individual power management MASK bits in the corresponding PMunit register space.

Bit			Description		
31:0	Power Manageme	ent Interrupt Mask Bit	S		
	Project:		All		
	Format:		Power Managem Registers Bit Def		
	FormatDesc:		ORed together to interrupt.	GTIIR and PMIIR are o generate the CPU	
				agement Interrupt s all share the same n this table.	
	This field contains	a bit mask which selec	ts which interrupt bits from	the ISR are reported	in the IIR.
	Value	Name	Description	Project	
	0b	Not Masked	Not Masked – will be reported in the IIR	All	
	1b	Masked	Masked – will not be reported in the IIR	All	



2.5.14 PMIIR — Power Management Interrupt Identity Register

PN	IIIR — Power Management Interrupt Identity Register
Register Type:	MMIO
Address Offset:	44028h
Project:	DevSNB
Default Value:	0000000h
Access:	R/W Clear
Size (in bits):	32
The IIR register of	contains the interrupt bits that are "unmasked" by the IMR and thus can generate CPU
	bled via the IER). When a CPU interrupt is generated, this should be the first register to be etermine the source of the interrupt. Writing a '1' into the appropriate bit position within

this register clears interrupts.

it			Description		
:0	Power Manageme	nt Interrupt Identity E	Bits		
	Project:		All		
	Format:		Power Management In	terrupt Registers Bit D	efinition
	FormatDesc:		The DEIIR and GTIIR generate the CPU inte		ogether to
			The Power Manageme share the same bit def		gisters all
	the IMR. If enable this register will re writing a 1' to the For each bit, the IIR occur before the firs	ed by the IER, bits se emain set (persist) u appropriate bit(s). acan store a second p	of the interrupt bits fron et in this register will ge ntil the interrupt conditi ending interrupt if two or r Upon clearing the interru er interrupt pending. Description	nerate a CPU interru on is cleared via soft more of the same interr	upt. Bits set in ware by rupt conditions
	the IMR. If enable this register will re writing a 1' to the For each bit, the IIR occur before the firs then return high to i	ed by the IER, bits se emain set (persist) u appropriate bit(s). can store a second p st condition is cleared. ndicate there is anothe	et in this register will ge ntil the interrupt conditi ending interrupt if two or r Upon clearing the interru er interrupt pending.	nerate a CPU interru on is cleared via soft more of the same interr pt, the IIR bit will mome	upt. Bits set ir ware by rupt conditions



2.5.15 PMIER — Power Management Interrupt Enable Register

	PMIER — Pov	ver Managem	ent Interrupt	Enable Regist	ter
	vpe: MMIO ifset: 4402Ch-4402Fh DevSNB ue: 00000000h R/W	errupt enable bit for e	each interrupt bit in t	he IIR register. A di	
Bit			Description		
31:0	Power Management I	nterrupt Enable Bits			
	Project:		All		
	Format:		Power Managen Registers Bit De		
	FormatDesc:			GTIIR and PMIIR are o generate the CPU	
				agement Interrupt s all share the same n this table.	
	The bits in this register Interrupt Identity Regis interrupts to propagate	ter becomes set. The			
	Value	Name	Description	Project	
	0b	Disable	Disable	All]
	1b	Enable	Enable	All	
		I	1	1	J



2.5.16 Digital Port Hot Plug Control Register

		Dig	ital Port	Hot Plug Control Register	
Register Address Project: Default Va Access: Size (in b	Offset: 440 All alue: 000 R/V	30h-44033 00000h	h		
Bit				Description	
31:5	Reserved	l Proje	ect: All	Format:	
4	Project: Default V Controls	alue:	All 0b the HPD buffe	t_Input_Enable er for the digital port. The buffer state is independent of whet	her the
	Value	Name	Description	n	Project
	0b	Disable	Buffer disab	bled	All
	1b	Enable	Buffer enab	led. Hot plugs bit reflect the electrical state of the HPD pin	All
3:2	Digital_P Project:	ort_A_Hot	All	_Pulse_Duration	
3:2	Digital_P Project: Default V These bit	ort_A_Hot alue: s define the	All Ob	_Pulse_Duration	
3:2	Digital_P Project: Default V These bit	ort_A_Hot alue: s define the Name	All Ob	_Pulse_Duration The pulse defined as a short pulse. Description Project	
3:2	Digital_P Project: Default V These bit Value 00b	ort_A_Hot alue: s define the Name 2ms	All Ob	_Pulse_Duration ne pulse defined as a short pulse.	
3:2	Digital_P Project: Default V These bit Value 00b 01b	ort_A_Hot alue: s define the 2ms 4.5ms	All Ob	_Pulse_Duration ne pulse defined as a short pulse.	
3:2	Digital_P Project: Default V These bit Value 00b 01b 10b	ort_A_Hot alue: s define the 2ms 4.5ms 6ms	All Ob	_Pulse_Duration he pulse defined as a short pulse.	
	Digital_P Project: Default V These bit Value 00b 01b 10b 11b	ort_A_Hot alue: s define the 2ms 4.5ms 6ms 100ms	All Ob e duration of th	Pulse_Duration ne pulse defined as a short pulse. Description Project 2 ms All 4.5 ms All 6 ms All 100 ms All	
3:2	Digital_P Project: Default V These bit Value 00b 01b 10b 11b Digital_P	ort_A_Hot alue: s define the 2ms 4.5ms 6ms 100ms	All Ob e duration of th	_Pulse_Duration he pulse defined as a short pulse.	
	Digital_P Project: Default V These bit Value 00b 01b 10b 11b	ort_A_Hot alue: s define the 2ms 4.5ms 6ms 100ms	All Ob duration of th	_Pulse_Duration he pulse defined as a short pulse.	
	Digital_P Project: Default V These bit Value 00b 01b 10b 11b Digital_P Project: Access: Default V	ort_A_Hot alue: s define the 2ms 4.5ms 6ms 100ms ort_A_Hot	All Ob e duration of th Plug_Interro All R/W Cle Ob	_Pulse_Duration ne pulse defined as a short pulse.	
	Digital_P Project: Default V These bit Value 00b 01b 10b 11b Digital_P Project: Access: Default V This refle or for noti set. These	ort_A_Hot alue: s define the 2ms 4.5ms 6ms 100ms ort_A_Hot alue: cts hot plug fication of a	All Ob e duration of th e duration of th Plug_Intern All R/W Cle Ob detect status a sink event. N DRed together	_Pulse_Duration he pulse defined as a short pulse.	its will
	Digital_P Project: Default V These bit Value 00b 01b 10b 11b Digital_P Project: Access: Default V This refle or for noti set. These	ort_A_Hot alue: s define the 2ms 4.5ms 6ms 100ms ort_A_Hot alue: cts hot plug fication of a se bits are 0	All Ob e duration of th e duration of th Plug_Intern All R/W Cle Ob detect status a sink event. N DRed together	_Pulse_Duration ne pulse defined as a short pulse.	its will



	Digital Port	Hot Plug Control Register	
1Xb	Long Pulse	Digital port long pulse hot plug event detected	All
X1b	Short Pulse	Digital port short pulse hot plug event detected	All

2.5.17 GTT Fault Status Register

		C	GTT Fau	It Status Register		
Register T Address O Project: Default Va Access: Size (in bit	All All All All All All All All R/V	110 940h-44043h 000000h V Clear				
Bit				Description		
31:8	Reserved	d Project:	All		Format:	
7	This is a	Invalid_GTT_page_table_entry Project: All Default Value: 0b This is a sticky bit, cleared by writing 1 to it. All the GTT Fault Status bits are ORed together to go to the main ISR GTT Fault bit.				
	Value	Name	C	Description		Project
	0b	Not Detected	E	vent not detected		All
	1b	Detected	E	vent detected		All
	Invalid r	ana tabla antro	, data			
6	Project: Default V This is a	alue:	All 0b by writing 1 t	to it. All the GTT Fault Status	s bits are ORe	d together to go to
6	Project: Default V This is a	alue: sticky bit, cleared	All 0b by writing 1 t t.	to it. All the GTT Fault Status	bits are ORe	d together to go to Project
6	Project: Default V This is a the main	alue: sticky bit, cleared ISR GTT Fault bit	All 0b by writing 1 t t. [s bits are ORe	



Cursor B	_GTT_Fault_Status		
Project:	All		
Default Va	lue: 0b		
This reflec Fault Statu	ts GTT fault status for this plane is bits are ORed together to go t	. This is a sticky bit, cleared by on the main ISR GTT Fault bit.	writing 1 to it. All the GT
Value	Name	Description	Project
0b	Not Detected	Event not detected	All
1b	Detected	Event detected	All
Cursor_A	_GTT_Fault_Status All		
Default Va	lue: 0b		
This reflec Fault Statu	ts GTT fault status for this plane is bits are ORed together to go t	. This is a sticky bit, cleared by on the main ISR GTT Fault bit.	writing 1 to it. All the GT
Value	Name	Description	Project
0b	Not Detected	Event not detected	All
1b	Detected	Event detected	A 11
10	Delected	Evenit detected	All
	GTT_Fault_Status		All
			All
 Sprite_B_	GTT_Fault_Status		
Sprite_B_ Project: Default Va This reflec	GTT_Fault_Status	. This is a sticky bit, cleared by	
Sprite_B_ Project: Default Va This reflec	GTT_Fault_Status All lue: 0b ts GTT fault status for this plane	. This is a sticky bit, cleared by	
Sprite_B_ Project: Default Va This reflec Fault Statu	GTT_Fault_Status All lue: 0b ts GTT fault status for this plane is bits are ORed together to go t	. This is a sticky bit, cleared by othe main ISR GTT Fault bit.	writing 1 to it. All the GT
Sprite_B_ Project: Default Va This reflec Fault Statu	GTT_Fault_Status All lue: 0b ts GTT fault status for this plane is bits are ORed together to go t Name	. This is a sticky bit, cleared by o the main ISR GTT Fault bit.	writing 1 to it. All the GT
Sprite_B_ Project: Default Va This reflec Fault Statu Value Ob 1b	GTT_Fault_Status All lue: 0b ts GTT fault status for this plane is bits are ORed together to go t Name Not Detected	. This is a sticky bit, cleared by o the main ISR GTT Fault bit. Description Event not detected	writing 1 to it. All the GT Project All
 Sprite_B_ Project: Default Va This reflec Fault Statu Value Ob 1b	GTT_Fault_Status All lue: 0b ts GTT fault status for this plane is bits are ORed together to go t Name Not Detected Detected	. This is a sticky bit, cleared by o the main ISR GTT Fault bit. Description Event not detected	writing 1 to it. All the GT Project All
Sprite_B_ Project: Default Va This reflec Fault Statu Value Ob 1b Sprite_A_	GTT_Fault_Status All lue: 0b ts GTT fault status for this plane us bits are ORed together to go t Name Not Detected Detected GTT_Fault_Status All	. This is a sticky bit, cleared by o the main ISR GTT Fault bit. Description Event not detected	writing 1 to it. All the GT Project All
Sprite_B_ Project: Default Va This reflec Fault Statu Value 0b 1b Sprite_A_ Project: Default Va This reflec	GTT_Fault_Status All lue: 0b ts GTT fault status for this plane us bits are ORed together to go t Name Not Detected Detected GTT_Fault_Status All	 This is a sticky bit, cleared by o the main ISR GTT Fault bit. Description Event not detected Event detected This is a sticky bit, cleared by find the sticky bit, cl	writing 1 to it. All the GT Project All All
Sprite_B_ Project: Default Va This reflec Fault Statu Value 0b 1b Sprite_A_ Project: Default Va This reflec	GTT_Fault_Status All lue: 0b ts GTT fault status for this plane us bits are ORed together to go t Name Not Detected Detected GTT_Fault_Status All lue: 0b ts GTT fault status for this plane	 This is a sticky bit, cleared by o the main ISR GTT Fault bit. Description Event not detected Event detected This is a sticky bit, cleared by find the sticky bit, cl	writing 1 to it. All the GT Project All All
Sprite_B_ Project: Default Va This reflec Fault Statu Value 0b 1b Sprite_A_ Project: Default Va This reflec Fault Statu	GTT_Fault_Status All lue: 0b ts GTT fault status for this plane us bits are ORed together to go t Name Not Detected Detected GTT_Fault_Status All lue: 0b ts GTT fault status for this plane us bits are ORed together to go t	 This is a sticky bit, cleared by o the main ISR GTT Fault bit. Description Event not detected Event detected This is a sticky bit, cleared by o the main ISR GTT Fault bit. 	writing 1 to it. All the GT Project All All writing 1 to it. All the GT



Primary_E	B_GTT_Fault_Status		
Project:	All		
Default Va	lue: 0b		
		e. This is a sticky bit, cleared by w to the main ISR GTT Fault bit.	rriting 1 to it. All the GT
Value	Name	Description	Project
0b	Not Detected	Event not detected	All
1b	Detected	Event detected	All
Primary_A	_GTT_Fault_Status		
Project:	All		
Default Va	lue: 0b		
This reflec		e. This is a sticky bit, cleared by w to the main ISR GTT Fault bit.	riting 1 to it. All the GT
Fault Statu			
Fault Statu	Name	Description	Project
		Description Event not detected	Project All

2.6 Display Engine Render Response

Do not cause more than one display event to be reported in the render response.

Either mask off all but one event, using the Display Engine Render Response Mask Register (DERRMR 0x44050), or never initiate more than one event.

2.6.1 Display Engine Render Response Message Bit Definition

	Display Engine Render Response I	Message Dit Dem	intion
Project:	DevSNB		
Size(in bit	(s): 32		
Display Er	ngine Render Response Message Registers all share	the same bit definitions from	om this table.
Bit	Descriptio	on	
Bit 31:14	Description Reserved Project: All	on	Format:
	-	Project: All	Format: Format:
31:14	Reserved Project: All	Project: All	



-1

	Display Engine Render Response Messa	ige Bit	Defi	nition
11	Pipe_B_Start_of_Vertical_Blank_Event This event will be reported on the start of the Pipe B Vertical Blank	Project:	All	Format:
10	Pipe_B_Sprite_Plane_Flip_Done_Event This event will be reported on the completion of a flip for the Pipe E	Project: 3 Sprite Pla	All ne.	Format:
9	Pipe_B_Primary_Plane_Flip_Done_Event This even will be reported on the completion of a flip for the Pipe B	Project: Primary Pl	All ane.	Format:
8	Pipe_B_Scanline_Event This event will be reported on the Pipe B scan line event.	Project:	All	Format:
7:6	Reserved Project: All			Format:
5	Pipe_A_Start_of_Horizontal_Blank_Event This event will be reported on the start of the Pipe A Horizontal Bla	Project: nk.	All	Format:
4	Reserved Project: All			Format:
3	Pipe_A_Start_of_Vertical_Blank_Event This even will be reported on the start of the Pipe A Vertical Blank.	Project:	All	Format:
2	Pipe_A_Sprite_Plane_Flip_Done_Event This event will be reported on the completion of a flip for the Pipe A	Project: A Sprite Pla	All ne.	Format:
1	Pipe_A_Primary_Plane_Flip_Done_Event This even will be reported on the completion of a flip for the Pipe A	Project: Primary Pl	All ane.	Format:
0	Pipe_A_Scanline_EventThis event will be reported on the Pipe A Display scan line event.	Project:	All	Format:

F



2.6.2 DERRMR — Display Engine Render Response Mask Register

DERRMR - Display Engine Render Response Mask Register							
Register Type:	MMIO						
Address:	44050h-44053h						
Project:	DevSNB						
Default Value:	0000FFFFh						
Access: R/W							
Size (in bits):	Size (in bits): 32						

This register is used by software to control which render response message bits are masked or unmasked. Unmasked bits will cause a render response message to be sent and will be reported in that message. Masked bits will not be reported and will not cause a render response message to be sent.

Unmasked events will wake render (command streamer) as they occur, so for improved power savings it is recommended to only unmask events that are required. Programming this register can be done through MMIO or a command streamer LOAD_REGISTER_IMMEDIATE command.

DWord	Bit		Description							
0	31:0	Display Engine Render Response Message Mask Bits								
		Project:		All						
		Format:		Display Engine F Message Bit Def	Render Response					
		FormatDesc: This field contains render response m	Display Engine (DE) render resp message bits come from events within the display engine. The D Engine Render Response Messa Registers all share the same bit definitions from this table. This field contains a bit mask which selects which events cause and are reported ir							
		Value	Name	Description	Project					
		0b	Not Masked	Description Not Masked – will be cause and be reported in the message	-					



2.7 Display Arbitration Control

2.7.1 DISP_ARB_CTL—Display Arbiter Control

		DISP_AR	B_CT	L—Display Arbiter C	ontrol				
Register Ty Address O		O 00h-45003h							
Project:	All								
Default Val	ue: C22	40622h							
Access:	R/W	1							
Size (in bit									
Trusted Ty	pe: 1								
Bit				Description					
31	Reserved								
30	Reserved	Reserved							
29	Reserved								
28	Reserved	Project:	All		Format:				
27:26	HP_Queu	e_Watermark							
	Project:	A	All I						
	Default Va	alue: 0	0b						
25:24	LP_Write	_Request_Limit							
	Project:	А	All						
	Default Va	alue: 1	0b	4					
	The value accepted	in this register ind from a single clier	dicates th nt before	he maximum number of back to bac re-arbitrating.	k LP write requests that will be				
	Value	Name	De	escription	Project				
	00b	1	1		All				
	01b	2	2		All				
	10b	4	4	(default)	All				
	11b	8	8		All				
23:20	TLB_Req	uest_Limit							
	Project:	A	AII						
	Default Va	alue: 0	010b	2					
	Range:	1	15						
	The value arbitration	in this register ind loop. Range 1 -	dicates tł 15, (defa	he maximum number of TLB reques ault 2). Zero is not a valid programn	ts that can be made in an ning.				



		DISP_AF	RB_CTI	L—Display Arbiter Control				
19:16	TLB_Requ	est_In-Flight_	Limit					
	Project:		All					
	Default Val	ue:	0100b	4				
	Range:		115					
				e maximum number of TLB (or VTd) requests that can ault 4). Zero is not a valid programming.	be in flight			
15	Reserved							
14:13	Address_S	Swizzling_for_	Tiled-Surfa	aces				
	Project:		All					
	Default Val	ue:	00b					
	DRAM conf	figuration regist	ters show if	memory address swizzling is needed.				
	Value	Name		Description	Project			
	00b	No Display		No display request address swizzling	All			
	01b	Enable		Enable display request address bit[6] swizzling for tiled surfaces	All			
	1Xb	Reserved		Reserved	All			
12	Reserved	Project:	All	Format:				
11:8	HP_Page_	Break_Limit						
	Project:		All					
	Default Val	ue:	0110b	6				
	Range:		115					
	The value in this register represents the maximum number of page breaks allowed in a HP request chain. Range 1 – 15, (default 6). Zero is not a valid programming.							
7	Reserved	Project:	All	Format:				
6:0	HP_Data_F	Request_Limit	:					
	Project:		All					
	Default Val	ue:	01000010b	34				
	Range:		1127					
				he maximum number of cachelines allowed in a HP re- ero is not a valid programming.	quest			



2.7.2 DISP_ARB_CTL2—Display Arbiter Control 2 [DevSNB]

	DISP	_ARB_CT	L2—	-Display Arbiter Control 2 [De	vSNB]	
Register Ty Address O Project: Default Val Access: Size (in bit	ffset: 4500 Dev: lue: 0000 R/W	04h-45007h SNB 00000h				
Bit	, 			Description		
31	Reserved					
30:9	Reserved	Project:	All	Forma	t: MBZ	
8	register is	lue: in this register i used to specify	when	only when Opportunistic Fetches are enabled. Th an opportunistic fetch can happen. For any oppo the process of waking the system.		
	Value	Name	Desc	ription		Project
	0b	FE inSR	Fetch	n on falling edge of inSR		All
	1b	Not inSR	Fetch	n when not inSR		All
7	Project: Default Va The value register re fetch to ha	in this register i presents the fet ppen, display s	All 0h s valid ch beh	only when Opportunistic Fetches are enabled. The avior when an opportunistic fetch is triggered. For not be in the process of waking the system.	r any oppor	
	Value	Name		Description	Project	
	0h	One Burst		One Burst Only	All	
	1h	Fill FIFO		Fill FIFO to Top	All	
6	Reserved	Project:	All	Forma	t: MBZ	



5:4	Inflight_H	IP_Read_Request_L	imit							
	Project:	All								
	Default Value: 00b									
		in this register repres any given time.	ents the maximum number of HP read req	uest transactions that can						
	Value	Name	Description	Project						
	00b	128 HP	128 HP inflight transactions limit	All						
	01b	64 HP	64 HP inflight transactions limit	All						
	10b	32 HP	32 HP inflight transactions limit	All						
	11b	16 HP	16 HP inflight transactions limit	All						
3:2	Reserved	Project: All		Format:						
:0	RTID_FIF	O_Watermark								
	Project:	All								
	Default Va	alue: Ob								
			ents the watermark value for the RTID FIF ve or equal the watermark	O. HP transactions will star						
	Value	Name	Description	Project						
	00b	8 RTIDs	8 RTIDs available in FIFO	All						
	01b	16 RTIDs	16 RTIDs available in FIFO	All						
		32 RTIDs	32 RTIDs available in FIFO	All						
	10b	32 KTIDS								

2.8 Display Watermark Registers

The watermark registers are used to control the display to memory request timing. The watermarks must be programmed according to the rules provided in the "Programming Watermarks" document. The default values of the watermarks should allow the display to operate in any mode supported by the memory configuration. However, the default watermarks are not optimized for power or memory bandwidth efficiency. Watermarks must enable from the bottom up, meaning if WM2 is disabled, WM3 must also be disabled, and if WM1 is disabled, both WM2 and WM3 must also be disabled.



2.8.1 WM0_PIPE_A—Pipe A Main Watermarks

		WM0_PI	PE_A	—Pipe A Main Watermarks			
Register Ty Address Of Project: Default Val Access: Size (in bits	ffset: 4510 All ue: 0078 R/W	D 0h-45103h 3818h					
Bit		Description					
31:23	Reserved	Project:	All	Format:			
22:16	-	Pipe_A_Primary_Watermark Project: All Number in 64Bs of data in FIFO below which the Pipe A Primary stream will generate requests to memory All					
15:14	Reserved	Project:	All	Format:			
13:8		Pipe_A_Sprite_Watermark Project: All Number in 64Bs of data in FIFO below which the Pipe A Sprite stream will generate requests to memory All					
7:5	Reserved	Project:	All	Format:			
4:0	-	ursor_Waterma 64Bs of data in		Project: low which the Pipe A Cursor stream will generate requests to	All		

2.8.2 WM0_PIPE_B—Pipe B Main Watermarks

		WM0_PI	PE_B-	-Pipe B Main Watermarks
Register T	ype: MN	10		
Address C	offset: 451	04h-45107h		
Project:	All			
Default Va	lue: 007	83818h		
Access:	R/V	V		
Size (in bit	t <mark>s):</mark> 32			
Trusted Ty	/pe: 1			
Bit				Description
31:23	Reserved	Project:	All	Format:
22:16	Pipe_B_	Primary_Watern	nark	Project: All
	Number i memory	n 64Bs of data in	FIFO below	which the Pipe B Primary stream will generate requests to
15:14	Reserved	Project:	All	Format:



				–Pipe B Main Watermarks	
13:8	Pipe_B_Spr	ite_Waterma	rk	Project:	All
	Number in 64 memory	4Bs of data in	FIFO below	w which the Pipe B Sprite stream will generate requests to	
7:5	Reserved	Project:	All	Format:	
4:0	Pipe_B_Cur	sor_Waterm	ark	Project:	All
	Number in 64 memory	4Bs of data in	FIFO below	w which the Pipe B Cursor stream will generate requests to	

2.8.3 WM1—Low Power 1 Display Watermarks

	WM1—Low Power 1 Display	Watermarks
Register T	Type: MMIO	
Address C	Dffset: 45108h-4510Bh	
Project:	All	
Default Va	alue: 00000000h	
Access:	R/W	
Size (in bi		
	termark values will be used only when one pipe is enable for using the Low Power 1 Sprite Watermark are met) an	
Bit	Description	
31	Enabled	Project: All
	Enables LP1 watermarks	
30:24	Latency	Project: All
	The latency associated with the LP1 watermarks in half usec	S.
23:20	FBC_LP1_Watermark	Project: All
	Number of equivalent lines of the primary display for this WM	
19:17	Reserved Project: All	Format:
16:8	LP1_Primary_Watermark	Project: All
	Number in 64Bs of data in FIFO below which the Primary stre	eam will generate requests to memory.
7:6	Reserved Project: All	Format:
5:0	LP1_Cursor_Watermark	Project: All



2.8.4 WM2—Low Power 2 Display Watermarks

	WM2—Low Power 2 Display Watermarks	S					
Address O	egister Type: MMIO ddress Offset: 4510Ch-4510Fh						
Project: Default Va							
Access: Size (in bit	R/W s): 32						
These wate	ermark values will be used only when one pipe is enabled and no sprites of LP2 state.	are enabled and the					
Bit	Description						
31	Enabled Enables LP2 watermarks	Project: All					
	LP2 watermarks must be disabled when the Low Power 1 Sprite Watermark is [DevILK] This bit must be programmed to 0 when FBC is enabled and FBC wat						
30:24	Latency The latency associated with the LP2 watermarks in half usecs.	Project: All					
23:20	FBC_LP2_Watermark Number of equivalent lines of the primary display for this WM	Project: All					
19:17	Reserved Project: All Form	nat:					
16:8	LP2_Primary_Watermark Number in 64Bs of data in FIFO below which the Primary stream will generate in	Project: All requests to memory.					
7:6	Reserved Project: All Form	nat:					
5:0	LP2_Cursor_Watermark Number in 64Bs of data in FIFO below which the Cursor stream will generate re	Project: All equests to memory.					



2.8.5 WM3—Low Power 3 Display Watermarks

egister 1	Type: MMIO	
-	Dffset: 45110h-45113h	
Project:	All	
Default Va	alue: 00000000h	
Access:	R/W	
Size (in bi		
	termark values will be used only when one pipe is enabled a in LP3 state.	and no sprites are enabled and the
Bit	Description	
31	Enabled	Project: All
	Enables LP3 watermarks	
30:24	Latency	Project: All
	The latency associated with the LP3 watermarks in half usecs.	
23:20	FBC_LP3_Watermark	Project: All
	Number of equivalent lines of the primary display for this WM	
19:17	Reserved Project: All	Format:
16:8	LP3_Primary_Watermark	Project: All
	Number in 64Bs of data in FIFO below which the Primary stream	n will generate requests to memory.
7:6	Reserved Project: All	Format:
	LP3_Cursor_Watermark	Project: All
5:0		110,000. 7 11



2.8.6 WM1S—Low Power 1 Sprite Watermark

		WM ²	1S—Low Pow	ver 1 Sprite Watermark			
Register ⁻	gister Type: MMIO						
Address (Offset:	45120h-45123	Sh				
Project:		All					
Default Va	alue:	0000000h					
Access:		R/W					
Size (in b	its):	32					
Bit		isplay is in LF		Description			
Dit							
31	Enab	ed		Project: All			
31	Enabl enabl enabl	es LP1 Sprite v ed. The WM2 L	ow Power 2 Display \	Project: All llows memory self refresh to be entered when sprite is Watermark needs to be disabled when this watermark is when sprite is not enabled or display LP1 watermarks are			
31 30:8	Enabl enabl enabl	es LP1 Sprite v ed. The WM2 L ed. This bit sho abled.	ow Power 2 Display \ ould only be changed	lows memory self refresh to be entered when sprite is Watermark needs to be disabled when this watermark is			
	Enabl enabl enabl not er	es LP1 Sprite v ed. The WM2 L ed. This bit sho abled.	ow Power 2 Display Nould only be changed	lows memory self refresh to be entered when sprite is Watermark needs to be disabled when this watermark is when sprite is not enabled or display LP1 watermarks are			
30:8	Enabl enabl enabl not er	es LP1 Sprite v ed. The WM2 L ed. This bit sho abled. ved Proje Sprite_Waterm	ow Power 2 Display Nould only be changed	lows memory self refresh to be entered when sprite is Watermark needs to be disabled when this watermark is when sprite is not enabled or display LP1 watermarks are			
30:8	Enabl enabl enabl not er Rese LP1_ Project	es LP1 Sprite v ed. The WM2 L ed. This bit sho abled. ved Proje Sprite_Waterm	ow Power 2 Display Nould only be changed ect: All	lows memory self refresh to be entered when sprite is Watermark needs to be disabled when this watermark is when sprite is not enabled or display LP1 watermarks are			



2.9 Backlight Control and Modulation Histogram Registers

2.9.1 BLC_PWM_CTL2—Backlight PWM Control Register 2

Register 1			2—Backlight PWM Control		_			
Address (0h-48253h						
Project:	All							
Default Va		0000h						
Access:	R/W							
Size (in bi	bits): 32 Description							
Bit			Description					
31	PWM_Ena	ble						
	Project:	All						
	Default Val	ue: 0b						
	This bit ena	ables the PWM cou	nter logic					
	Value	Name	Description		Project			
	0b	Disable	PWM disabled (drives 0 always)		All			
	1b	Enable	PWM enabled		All			
30	Reserved	Project: A	NII	Format:				
29	PWM_Pipe	e_assignment						
	Project:	All						
	Default Val	ue: 0b						
			e. The PWM counter will run off of this pip hange the value of this field.	e's PLL. The PW	M function			
	must be dis							
	Value	Name	Description	Projec	ct			
		-	Description Pipe A	Projec All	ct			
	Value	Name	-	-	ct			
28:27	Value 0b	NamePipe APipe B	Pipe A	All	ct			
28:27 26	Value Ob 1b Reserved	NamePipe APipe B	Pipe A Pipe B	All	ct			
-	Value Ob 1b Reserved	Name Pipe A Pipe B Project: A	Pipe A Pipe B	All	ct			
-	Value Ob 1b Reserved Phase-In_I	Name Pipe A Pipe B Project: A Interrupt_Status All	Pipe A Pipe B	All	ct			
-	Value Ob 1b Neserved Phase-In_I Project:	Name Pipe A Pipe B Project: A Interrupt_Status All R/W	Pipe A Pipe B	All	ct			
-	Value Ob 1b 1b Reserved Phase-In_I Project: Access: Default Val This bit will	Name Pipe A Pipe B Project: A Interrupt_Status All R/M ue: Ob be set by hardward	Pipe A Pipe B	All All Format:				
-	Value Ob 1b 1b Reserved Phase-In_I Project: Access: Default Val This bit will	Name Pipe A Pipe B Project: A Interrupt_Status All R/W lue: 0b be set by hardware ', which will reset th	Pipe A Pipe B VI V Clear e when a Phase-In interrupt has occurred.	All All Format:				



24	Phase_In_Inter	-	upt to be generated when the DWM phase in is as	Project: All			
	-		upt to be generated when the PWM phase in is co	mpieted.			
23:16	Phase_In_time						
	Project:	All					
	Default Value: 0b						
	This field determ	nines the numbe	er of VBLANK events that pass before one increme	ent occurs.			
	Value	Name	Description	Project			
	0b [Default]		Invalid	All			
	01h-FFh		VBlank Count	All			
15:8	Phase_In_Cou	Phase In Count					
	This field determines the number of increment events in this phase in. Writes to this register should only occur when hardware-phase-ins are disabled. Reads to this register can occur any time, where the value in this field indicates the number of increment events remaining to fully apply a phase-in request as hardware automatically decrements this value. A value of 0 is invalid.						
7:0	Phase_In_Incre		Project: All				
	This field indicates the amount to adjust the PWM duty cycle register on each increment event.						
	This is a two's complement number.						

2.9.2 BLC_PWM_CTL—Backlight PWM Control Register

	BLC_	PWM_	CTL—Backlight	PWM Control Re	gister	
Register Ty Address O Project: Default Val Access: Size (in bit:	ffset: 48254h- All ue: 0000000 R/W					
Bit			Des	cription		
31:16	Reserved	Project:	All		Format:	
15:0	control. This s A value equal is desired to c cycle. This val multiplied by 1	ermines the should new to the bac change the lue represe 128.	er be larger than the frequent klight modulation frequence intensity of the backlight, ents the active time of the	nts for the active portion of th ency field. A value of zero w y field will be full on. This fie t will take affect at the end of PWM stream in PCH display	ill turn the b ld gets upda the current raw clock pe	acklight off. ated when it PWM eriods
			itten only as a full 32 bit d	vord. Byte or word writes are	not suppor	ted.



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2.9.3 BLM_HIST_CTL—Image Enhancement Histogram Control Register

BLN	I_HIST	_CTL—	Image	Enhancement Hist	ogram Control Re	gister		
Register T Address C Project: Default Va Access: Size (in bi	Diffset: 482 All alue: 000 R/V	2 60h-48263 000000h	h					
Bit				Description				
31	Project: Default V	alue:	All Ob	am_Enabled	llect data.			
	Value	Name	Descripti	on		Project		
	0b	Disable	Image his	nage histogram is disabled				
	1b	Enable	zero to a	e histogram is enabled. When one, histogram calculations wil of the assigned pipe.		All		
	Project: Default V This bit e		All 0b mage Enha	ncement modification table.				
	Value	Name	Descripti	Description				
	0b	Disable	Disabled			All		
	1b	Enable		Enabled. When this bit is changed from a zero to a one, modifications begin after the next VBLANK of the assigned pipe.				
29	Project: Default V This bit a	Image_Enhancement_Pipe_assignment Project: All Default Value: 0b This bit assigns the IE function to a pipe. IE events will be synchronized to the VBLANK of the pipe. The IE function must be disabled in order to change the value of this field.						
	Value	Name		Description	Project			
	0b	Pipe A		Pipe A	All			
	46	Pipe B		Pipe B	All			
	1b	т іре в		Tipe B	,			



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24	Histogram	n Mode Se	elect				
	Project:		All				
	Default Va	alue:	0b				
	Value	Name		Description	Project		
	0b	YUV		YUV Luma Mode	All		
	1b	HSV		HSV Intensity Mode	All		
23:16	Sync_to_Phase_In_Count Project: All This field indicates the phase in count number on which the Image Enhancement table will be loaded if the Sync to Phase in is enabled. Superiord						
15	Reserved			Form	 nat:		
14:13	Enhance	ment_mod					
-	Project: Default Va		All 00b				
	Value	Name		Description	Project		
	00b	Direct		Direct look up mode	All	All	
	01b	Additiv	e	Additive mode	All	All	
	10b	Multipli	cative	Multiplicative mode	All	All	
	11b	Reserved		Reserved	All	All	
12		s bit enabl	es the doub he next vbla	le buffered registers to be loaded on the		ject: All e	
11	Project: Default Va	alue:	tion_Select All 0b hat data is l	t being written to or read from the bin dat	ta register.		
	Value	Name	Descripti	on		Project	
	Ob	BTC	bin's three	Bin Threshold Count. A read from the bin data register returns that bin's threshold value from the most recent vblank load event (guardband threshold trip). Valid range for the Bin Index is 0 to 31.			
	1b	BIE	Bin Image Enhancement Value. Valid range for the Bin Index is 0 to 32				
10:7	Reserved	Projec	t: All	Form	nat:		
6:0	-	ster_Inde>		er whose data can be accessed throug		ject: All	



2.9.4 Image Enhancement Bin Data Register

Image Enhancement Bin Data Register(F0 Threshold Count Usage)

Register Type:	ММЮ
Address Offset:	48264h-48267h
Project:	All
Exists If:	BLM_HIST_CTL:Bin Register Function Select = 0
Default Value:	0000000h
Access:	Read Only
Size (in bits):	32

Writes to this address are steered to the correct register by programming the Bin Register Function Select and the Bin Register Index.

Function 0 usage (Threshold Count) this Function is Read Only

Bit	Description
31	Busy_Bit Project: All
	If set , the engine is busy, the rest of the register is undefined. If clear, the register contains valid data.
30:22	Reserved Project: All Format:
21:0	Bin_Count Project: All
	The total number of pixels in this bin, value is updated at the start of each vblank.

Image Enhancement Bin Data Register(F1 Image Enhancement Usage)

Register Type.	
Address Offset:	48264h-48267h
Project:	All
Exists If:	BLM_HIST_CTL:Bin Register Function Select = 1
Default Value:	0000000h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Next vblank if in normal mode, or on phase in Sync event frame if it is enabled

Writes to this address are steered to the correct register by programming the Bin Register Function Select and the Bin Register Index.

Function 1 usage (Image Enhancement) this Function is Read/Write

Bit	Description						
31:10	Reserved	Project:	All	Format:			
9:0	Image_Bin_	Correction_F	actor	Project: All			
	normal mode	e, or on the ph	ase in Syr	tes to this register are double buffered on the next vblank if in ic event frame if it is enabled. The value written here is the 10bit st point of the bin.			



	_			hreshold Guardband Registe	-		
Register ⁻			MMIO				
Address	Offset:		48268h-48	326Bh			
Project:			All				
Default Va	alue:		000000000	n			
Access: Size (in b	ite).		R/W 32				
•	uffer Update	Point [.]		rtical blank			
Bit			Clair of Vo	Description			
31	Histogra	m_Interrup	t enable				
•••	Project:		All				
	Default V	alue:	0b				
	Value	Name	Description				
	0b	Disable	Disabled				
	1b	Enable	This generates a histogram interrupt once a Histogram event occurs. Software must always program 1.				
30	Histogra	m Event «	status				
	Project:	Histogram_Event_status Project: All					
	Access:		R/W 0	lear			
		Default Value: 0b					
	When a H	Histogram event has occurred, this will get set by the hardware. For any more Histogr o occur, the software needs to clear this bit by writing a '1'. The default state for this bit					
	Value	Name		Description	Project		
	0b	Not Oc	curred	Histogram event has not occurred	All		
	1b	Occurr	ed	Histogram event has occurred	All		
29:22	Guardba	nd_Interru	pt_Delay		Proj	ect: All	
				l after this many consecutive frames of the guard buffered on start of vblank. A value of 0 is inva		old being	
21:0	Threshol	d_Guardb	and		Proj	ect: All	
	Threshold_Guardband Project: All This value is used to determine the guardband for the threshold interrupt generation. This single value is used for all the segments. This value is double buffered on start of vblank Project: All						

2.9.5 Histogram Threshold Guardband Register



2.10 Motion Blur Mitigation (MBM) Control

These registers are use to control the MBM logic. (Sometimes called LOT, panel overdrive, or LRTC).

Before enabling MBM, software should have identically programmed both pipes source size and gamma tables. Additionally, before executing a flip on the selected pipe (which generates the MBM frame) software should have loaded the address of the reference frame into the second plane(s), this can be done by MMIO or by a flip command. The second pipe does not need to have it's panel fitter or FDI enabled (or anything else down the pipe from MBM).

2.10.1 MBM_CTRL—MBM Control

			MBM	_CTRL—MBM Control			
Register Type:MMIOAddress Offset:48800h-48803hProject:AllDefault Value:00000000hAccess:R/WSize (in bits):32		h					
Bit	Description						
31	MBM_Enable Project: All Default Value: 0b This bit enables MBM logic.						
	Value	Name		Description	Project		
	0b	Disable	1	MBM is Disabled	All		
	1b	Enable		MBM is Enabled	All		
30	Reserved	l Proje	ect: All	Format:			
29	MBM Pipe	e Select					
	Project: Default Va	alue:	All 0b 1 modificatio	on to the selected pipe.			
	Value	Name	Descripti	on	Project		
	0b	Pipe A		PipeA (PipeA will fetch the current buffer and PipeB will fetch the All previous buffer)			
	1b	Pipe B	PipeB (Pip previous b	peB will fetch the current buffer and PipeA will fetch the puffer)	All		



8:27	MBM_Surf	ace select					
	Project:	—	All				
	Default Val	ue:	0b				
	Value	Name	Description	Project			
	00b	None	None	All			
	01b	Sprite	Sprite Only	All			
	10b	Primary	Primary Only	All			
	11b	Both	Both sprite and primary	All			
26:24	Reserved	Project:	All	Format:			
23:16	MBM_Delta	a_Threshol	d				
	Project:		All				
	Default Value: 00000000b						
			en the current and previous compo enerated. Otherwise, the current	onent values exceed this threshold a value is passed through.			
15:0	Reserved	Project	All	Format:			

2.10.2 MBM_TBL—MBM Overdrive Table

		MBM_TBL—MBM Overdrive	Table							
Register Ty	egister Type: MMIO									
Address Off	set: 48	h-4890Bh								
Project:	All									
Default Valu	e: 0000000h									
Access:	R/\	N								
Size (in bits): 63:	<32								
		t to 0, so the first address actually corresponds to th coded to 256, so only 7 rows total are programma								
DWord	Bit	Description								
062	31:24	Reserved Project: All	Format:							
	23:16	Red_MBM_overdrive_value Project:								
	15:8	Green_MBM_overdrive_value	Project: All							
	7:0	Blue_MBM_overdrive_value	Project: All							



Overdrive table address offsets:

	0	31	63	95	127	159	191	223	255
0	0	0	0	0	0	0	0	0	0
31	48810h	48814h	48818h	4881Ch	48820h	48824h	48828h	4882Ch	48830h
63	48834h	48838h	4883Ch	48840h	48844h	48848h	4884Ch	48850h	48854h
95	48858h	4885Ch	48860h	48864h	48868h	4886Ch	48870h	48874h	48878h
127	4887Ch	48880h	48884h	48888h	4888Ch	48890h	48894h	48898h	4889Ch
159	488A0h	488A4h	488A8h	488ACh	488B0h	488B4h	488B8h	488BCh	488C0h
191	488C4h	488C8h	488CCh	488D0h	488D4h	488D8h	488DCh	488E0h	488E4h
223	488E8h	488ECh	488F0h	488F4h	488F8h	488FCh	48900h	48904h	48908h
255	256	256	256	256	256	256	256	256	256

Previous Pixel Value Range

Current Pixel Value Range

Address Offset

Hard Coded Value

2.11 Color Conversion and Control Registers

These registers contain the coefficients of the pipe color space converter. There are 12 values in 6 registers for each pipe. This color space conversion is used to convert the RGB frame buffer data into YUV data for use on the HDMI or DisplayPort. Or alternately a YUV frame buffer could be converted to RGB.

The high color channel is the most significant bits of the color. The low color channel is the least significant bits of the color. The medium color channel is the bits between high and low. For example: In RGB modes Red is in the High channel, Green in Medium, and Blue in Low. In YUV modes, U is in the High channel, Y in Medium, and V in Low.

The color space conversion registers are double buffered and are updated on the start of vertical blank following a write to the CSC Mode register for the respective pipe.



	<mark>ts):</mark> 16 ts for the C	SC are store		n-exponent-mantissa format. Two CS ta packing in each dword.	C coefficients	are stored
Bit				Description		
15	Sign Project: All					
	Value	le Name		Description		Project
	0b	Positive		Positive		All
	1b	1b Negative		Negative		All
14:12	Exponen Project: Represer	ted as 2^{-n}	All			
	Value	Name	Desc	ription	Proje	ct
	110b	4	4 or r	nantissa is bb.bbbbbbb	All	
	111b	2	2 or r	nantissa is b.bbbbbbbb	All	
	000b	1	1 or r	nantissa is 0.bbbbbbbbb	All	
	001b	0.5	0.5 o	r mantissa is 0.0bbbbbbbbb	All	
	010b	0.25	0.25	or mantissa is 0.00bbbbbbbbbb	All	
	011b	0.125	0.12	5 or mantissa is 0.000bbbbbbbbb	All	
	others	Reserved	Rese	rved	All	
	Mantissa				Dr	oject: All

The matrix equations are as follows:

Y = (RY * R) + (GY * G) + (BY * B)U = (RU * R) + (GU * G) + (BU * B)

$$V = (RV * R) + (GV * G) + (BV * B)$$



	Bt.601		Bt.709	
	Value	Program	Value	Program
RU	0.2990	0x1990	0.21260	0x2D98
GU	0.5870	0x0968	0.71520	0x0B70
BU	0.1140	0x3E98	0.07220	0x3940
RV	-0.1687	0xAAC8	-0.11460	0xBEA8
GV	-0.3313	0x9A98	-0.38540	0x9C58
BV	0.5000	0x0800	0.50000	0x0800
RY	0.5000	0x0800	0.50000	0x0800
GY	-0.4187	0x9D68	-0.45420	0x9E88
BY	-0.0813	0xBA68	-0.04580	0xB5E0

The standard programming for RGB to YUV is in the following table.

The standard programming for YUV to sRGB without scaling is in the following table.

The input is VYU on high, medium, and low channels respectively.

The output is RGB on high, medium, and low channels respectively.

Program the pre-CSC offsets to -128, -16, and -128 for high, medium, and low channels respectively.

The coefficients can be scaled if desired.

	Bt.601 Rev	verse	Bt.709 Reverse	
	Value	Program	Value	Program
GY	1.000	0x7800	1.000	0x7800
BY	0.000	0x0000	0.000	0x0000
RY	1.371	0x7AF8	1.574	0x7C98
GU	1.000	0x7800	1.000	0x7800
BU	-0.336	0x9AC0	-0.187	0xABF8
RU	-0.698	0x8B28	-0.468	0x9EF8
GV	1.000	0x7800	1.000	0x7800
BV	1.732	0x7DD8	1.855	0x7ED8
RV	0.000	0x0000	0.000	0x0000



2.11.1 Pipe A Color Control

2.11.1.1 CSC_A_Coefficients 1

		CSC_A_Coefficients 1		
Register Type: Address Offset: Project: Default Value: Access: Size (in bits): Double Buffer Update Point: Double Buffer Armed By:		MMIO 49010h-49013h All 00000000h R/W 32 Start of vertical blank after armed Write to CSC_A_Mode		
Bit		Description		
31:16	RY Project: Format: FormatDesc: CSC coefficient. Se	All CSC COEFFICIENT DESCRIPTION Coefficients for the CSC are stored in sign-exponent- mantissa format. Two CSC coefficients are stored in each dword, the table below show the data packing in each dword.		
15:0 GY Project: Format: FormatDesc:		All CSC COEFFICIENT DESCRIPTION Coefficients for the CSC are stored in sign-exponent- mantissa format. Two CSC coefficients are stored in each dword, the table below show the data packing in each dword. the format description above.		



2.11.1.2 CSC_A_Coefficients 2

			CSC_A_Co	efficients 2
Register T	ype:	MMI	C	
Address O	ffset:	4901	4h-49017h	
Project:		All		
Default Val	lue:	0000	0000h	
Access:		R/W		
Size (in bit	s):	32		
Double Bu	ffer Update Point:	Start	of vertical blank after	er armed
Double Bu	ffer Armed By:	Write	to CSC_A_Mode	
Bit				Description
31:16	BY			
	Project:			All
	Format:			CSC COEFFICIENT DESCRIPTION
	FormatDesc:			Coefficients for the CSC are stored in sign-exponent-mantissa format. Two CSC coefficients are stored in each dword, the table below show the data packing in each dword.
	CSC coefficient.	See forma	at description above	
15:0	Reserved F	Project:	All	Format:



2.11.1.3 CSC_A_Coefficients 3

		CSC_A_Coe	fficients 3
Register Type: Address Offset: Project: Default Value: Access: Size (in bits): Double Buffer Update Point: Double Buffer Armed By:		MMIO 49018h-4901Bh All 00000000h R/W 32 Start of vertical blank after Write to CSC_A_Mode	
Bit			escription
31:16	RU Project: Format: FormatDesc: CSC coefficient. Se	e format description above.	All CSC COEFFICIENT DESCRIPTION Coefficients for the CSC are stored in sign-exponent-mantissa format. Two CSC coefficients are stored in each dword, the table below show the data packing in each dword.
15:0	GU Project: Format: FormatDesc:		All CSC COEFFICIENT DESCRIPTION Coefficients for the CSC are stored in sign-exponent-mantissa format. Two CSC coefficients are stored in each dword, the table below show the data packing in each dword.
	CSC coefficient. Se	ee format description above.	



2.11.1.4 CSC_A_Coefficients 4

			CSC_A_Co	efficients 4
Register T	ype:	MMI	C	
Address O		4901	Ch-4901Fh	
Project:		All		
Default Val	lue:	0000	0000h	
Access:		R/W		
Size (in bit	s):	32		
Double Bu	ffer Update Point	: Start	of vertical blank after	r armed
Double Bu	ffer Armed By:	Write	to CSC_A_Mode	
Bit			I	Description
31:16	BU			
	Project:			All
	Format:			CSC COEFFICIENT DESCRIPTION
	FormatDesc:			Coefficients for the CSC are stored in sign-exponent-mantissa format. Two CSC coefficients are stored in each dword, the table below show the data packing in each dword.
	CSC coefficient.	See forma	at description above.	
15:0	Reserved	Project:	All	Format:



2.11.1.5 CSC_A_Coefficients 5

		CSC_A_Coe	fficients 5
Register Type: Address Offset: Project: Default Value: Access: Size (in bits): Double Buffer Update Point: Double Buffer Armed By:		MMIO 49020h-49023h All 00000000h R/W 32 Start of vertical blank after Write to CSC_A_Mode	armed
Bit		D	escription
31:16	RV Project: Format: FormatDesc: CSC coefficient. See format description abov		All CSC COEFFICIENT DESCRIPTION Coefficients for the CSC are stored in sign-exponent-mantissa format. Two CSC coefficients are stored in each dword, the table below show the data packing in each dword.
15:0	GV Project: Format: FormatDesc: CSC coefficient. See format description above		All CSC COEFFICIENT DESCRIPTION Coefficients for the CSC are stored in sign-exponent-mantissa format. Two CSC coefficients are stored in each dword, the table below show the data packing in each dword.



2.11.1.6 CSC_A_Coefficients 6

Register Type:		MMIO		
Address Offset:		49024h-49027h		
Project:		All		
Default Value:		0000000h		
Access:		R/W		
Size (in bits):		32		
Double Buffer Update Point:		Start of vertical blank after armed		
Double Buffer Armed By:		Write to CSC_A_Mode		
Bit		Description		
31:16	BV			
	Project:		All	
	Format:		CSC COEFFICIENT DESCRIPTION	
	FormatDesc:		Coefficients for the CSC are stored in sign-exponent-mantissa format. Two CSC coefficients are stored in each dword, the table below show the data packing in each dword.	
	CSC coefficient. Se	e format description above).	
15:0	Reserved Pro	ject: All	Format:	



2.11.1.7 CSC_A_Mode

			CSC_A_Mode			
Register T	Гуре:	MI	MIO			
Address Offset:			49028h-4902Bh			
Project:						
Default Va	alue:		000000h			
Access:		R/				
Size (in bi		32 Delation St	art of vertical blank			
	uffer Update	r arm CSC_A r				
Bit			Description			
31:3	Reserved	d Project:	All Format:			
2	CSC_Bla	ck_Screen_O	ffset			
	Project:		All			
	Default V	alue:	Ob			
	Adds an offset to the data output from CSC					
	In sRGB ouput mode: RGB is defined as $R^+ 1/16$, $G^+ 1/16$, $B^+ 1/16$					
	In rcYUV output mode: YUV is defined as Y'+ 1/16, U and V are output in excess 2048 format					
	In rcyOV output mode: YOV is defined as Y + 1/16, O and V are output in excess 2048 form					
	Value	Name	Description	Project		
	0b	No Offset	CSC output has no offset added (will be RGB or YUV, depending on bit 0)	All		
	1b	Offset	CSC output has offset added (will be sRGB or rcYUV depending on bit 0)	All		
1	CSC_Pos	sition				
	Project:		All			
	Default V	alue:	Ob			
	Selects the CSC position in the pipe.					
	Value	Name	Description	Project		
	0b	CSC After	CSC is after gamma and DPST image enhancement	All		
	1b	CSC Before	CSC is before gamma and DPST image enhancement	All		
0	CSC_Mo	de				
	Project:		All			
	Default Value: 0b					
	Selects th	he CSC direction	on.			
	Value	Name	Description	Project		
	0b	RGB to YUV	RGB to YUV conversion	All		
	1b	YUV to RGB	YUV to RGB conversion	All		



2.11.1.8 Pre-CSC_A High Color Channel Offset

Register T	ype:	MMIO		
Address O		49030h-49033h		
Project:		All		
Default Va	ue:	00000000h		
Access:		R/W		
Size (in bit	s):	32		
Double Buffer Update Point:		Start of vertical blank after	er armed	
Double Bu	ffer Armed By:	Write to CSC_A_Mode		
Bit			Description	
31:13	Reserved Pro	ect: All	Forma	at:
12:0	Pre-CSC_High_Co	lor_Channel_Offset		Project: All
	This 13-bit 2's comp	lement value is used to giv	ve an offset to the color channel as	it enters CSC logic.

2.11.1.9 **Pre-CSC_A Medium Color Channel Offset**

Register T	vne.	ΜΜΙΟ		
Address Offset:		49034h-49037h		
Project:		All		
Default Value:		0000000h		
Access:		R/W		
Size (in bits):		32		
Double Bu	ffer Update Point:	Start of vertical blank after armed		
Double Bu	ffer Armed By:	Write to CSC_A_Mode		
Bit		Des	cription	
31:13	Reserved Pro	ject: All	Format:	
12:0	Pre-CSC_Medium_	Color_Channel_Offset	Project: All	
	This 13-bit 2's comp	plement value is used to give ar	n offset to the color channel as it enters CSC logic.	



Register 1	Гуре:	MMIO		
Address (Offset:	49038h-4903Bh		
Project:		All		
Default Va	alue:	00000000h		
Access:		R/W		
Size (in bits):		32		
Double Buffer Update Point:		Start of vertical blank after armed		
Double Buffer Armed By:		Write to CSC_A_Mode		
Bit	Desc		ption	
31:13	Reserved Project: All		Format:	
12:0 Pre-CSC_Low_Co		lor_Channel_Offset	Project: All	
	This 13-bit 2's com	plement value is used to give an o	ffset to the color channel as it enters CSC logic.	

2.11.1.10 Pre-CSC_A Low Color Channel Offset

2.11.2 Pipe B Color Control

2.11.2.1 CSC_B_Coefficients 1

Register Type:	MMIO	
Address Offset:	49110h-49113h	
Project:	All	
Default Value:	0000000h	
Access:	R/W	
Size (in bits):	32	
Double Buffer Update Poin	: Start of vertical blank afte	r armed
Double Buffer Armed By:	Write to CSC_B_Mode	
Bit	C. C	Description
31:16 RY		
Project:		All
Format:		CSC COEFFICIENT DESCRIPTION
FormatDesc:		Coefficients for the CSC are stored in sign-exponent-mantissa format. Two CSC coefficients are stored in each dword, the table below show the data packing in each dword.



	CSC_B_Coefficients 1				
15:0	GY				
	Project:	All			
	Format:	CSC COEFFICIENT DESCRIPTION			
	FormatDesc:	Coefficients for the CSC are stored in sign-exponent-mantissa format. Two CSC coefficients are stored in each dword, the table below show the data packing in each dword.			
	CSC coefficient. See format description above.				

2.11.2.2 CSC_B_Coefficients 2

			CSC_B_	Coefficients 2
Register T	ype:	MMI	C	
Address O	ffset:	4911	4h-49117h	
Project:		All		
Default Val	lue:	0000	0000h	
Access:		R/W		
Size (in bit	s):	32		
Double Bu	ffer Update Poin	t: Start	of vertical blank	k after armed
Double Bu	ffer Armed By:	Write	e to CSC_B_Mo	de
Bit				Description
31:16	BY			
	Project:			All
	Format:			CSC COEFFICIENT DESCRIPTION
	FormatDesc:			Coefficients for the CSC are stored in sign-exponent-mantissa format. Two CSC coefficients are stored in each dword, the table below show the data packing in each dword.
	CSC coefficient	. See forma	at description ab	bove.
15:0	Reserved	Project:	All	Format:



2.11.2.3 CSC_B_Coefficients 3

		CSC_B_Coe	fficients 3
Register Type: Address Offset: Project: Default Value: Access: Size (in bits): Double Buffer Update Point: Double Buffer Armed By:		MMIO 49118h-4911Bh All 00000000h R/W 32 Start of vertical blank after Write to CSC_B_Mode	armed
Bit		De	escription
31:16	RU Project: Format: FormatDesc: CSC coefficient. Se	e format description above.	All CSC COEFFICIENT DESCRIPTION Coefficients for the CSC are stored in sign-exponent-mantissa format. Two CSC coefficients are stored in each dword, the table below show the data packing in each dword.
15:0	GU Project: Format: FormatDesc: CSC coefficient. Se	e format description above.	All CSC COEFFICIENT DESCRIPTION Coefficients for the CSC are stored in sign-exponent-mantissa format. Two CSC coefficients are stored in each dword, the table below show the data packing in each dword.



2.11.2.4 CSC_B_Coefficients 4

		CSC_B_Coe	fficients 4
Register T	ype:	MMIO	
Address O	ffset:	4911Ch-4911Fh	
Project:		All	
Default Val	lue:	00000000h	
Access:		R/W	
Size (in bit	s):	32	
Double Bu	ffer Update Point:	Start of vertical blank after	armed
Double Bu	ffer Armed By:	Write to CSC_B_Mode	
Bit		D	escription
31:16	BU		
	Project:		All
	Format:		CSC COEFFICIENT DESCRIPTION
	FormatDesc:		Coefficients for the CSC are stored in sign-exponent-mantissa format. Two CSC coefficients are stored in each dword, the table below show the data packing in each dword.
	CSC coefficient. Se	e format description above.	
15:0	Reserved Proje	ect: All	Format:



2.11.2.5 CSC_B_Coefficients 5

		CSC_B_Coe	fficients 5
Register Type: Address Offset: Project: Default Value: Access: Size (in bits): Double Buffer Update Point: Double Buffer Armed By:		MMIO 49120h-49123h All 00000000h R/W 32 Start of vertical blank after Write to CSC_B_Mode	armed
Bit		D	escription
31:16	RV Project: Format: FormatDesc: CSC coefficient. Se	e format description above.	All CSC COEFFICIENT DESCRIPTION Coefficients for the CSC are stored in sign-exponent-mantissa format. Two CSC coefficients are stored in each dword, the table below show the data packing in each dword.
15:0	GV Project: Format: FormatDesc: CSC coefficient. Se	e format description above.	All CSC COEFFICIENT DESCRIPTION Coefficients for the CSC are stored in sign-exponent-mantissa format. Two CSC coefficients are stored in each dword, the table below show the data packing in each dword.



2.11.2.6 CSC_B_Coefficients 6

		CSC_B_Coe	fficients 6
Register T	ype:	MMIO	
Address O	ffset:	49124h-49127h	
Project:		All	
Default Val	lue:	0000000h	
Access:		R/W	
Size (in bit	s):	32	
Double Bu	ffer Update Point:	Start of vertical blank after	armed
Double Bu	ffer Armed By:	Write to CSC_B_Mode	
Bit		D	escription
31:16	BV		
	Project:		All
	Format:		CSC COEFFICIENT DESCRIPTION
	FormatDesc:		Coefficients for the CSC are stored in sign-exponent-mantissa format. Two CSC coefficients are stored in each dword, the table below show the data packing in each dword.
	CSC coefficient. Se	e format description above.	
15:0	Reserved Proje	ect: All	Format:

2.11.2.7 CSC_B_Mode

	CSC_B_I	Vode
Register Type:	MMIO	
Address Offset:	49128h-4912Bh	
Project:	All	
Default Value:	0000000h	
Access:	R/W	
Size (in bits):	32	
Double Buffer Update Point:	Start of vertical blank	
Writes to this register arm	CSC_B registers	
Bit	De	scription
31:3 Reserved F	Project: All	Format:



			CSC_B_Mode						
2	CSC_Bla	CSC_Black_Screen_Offset							
	Project:	A	All						
	Default V	alue: ()b						
	Adds an offset to the data output from CSC								
	In sRGB	ouput mode: R	GB is defined as R`+ 1/16, G`+ 1/16, B`+ 1/16						
		-	YUV is defined as Y'+ 1/16, U and V are output in excess 2048 form	nat					
	Value	Name	Description	Project					
	0b	No Offset	CSC output has no offset added (will be RGB or YUV, depending All on bit 0)						
	1b	Offset	CSC output has offset added (will be sRGB or rcYUV depending All on bit 0)						
1	CSC_Pos Project: Default V	ŀ	on bit 0)						
1	Project: Default V Selects tl	A alue: (he CSC positio	on bit 0) All Db n in the pipe.	Droinet					
1	Project: Default V Selects th	/ alue: (he CSC positio Name	on bit 0) All Db n in the pipe. Description	Project					
1	Project: Default V Selects the Value Ob	A alue: 0 he CSC positio Name CSC After	on bit 0) All Db n in the pipe. Description CSC is after gamma and DPST image enhancement	All					
1	Project: Default V Selects th	/ alue: (he CSC positio Name	on bit 0) All Db n in the pipe. Description	-					
0	Project: Default V Selects the Value Ob	Alue: 0 he CSC positio Name CSC After CSC Before	on bit 0) All Db n in the pipe. Description CSC is after gamma and DPST image enhancement	All					
	Project: Default V Selects the Ob 1b	A alue: 0 he CSC positio Name CSC After CSC Before de	on bit 0) All Db n in the pipe. Description CSC is after gamma and DPST image enhancement	All					
	Project: Default V Selects the Ob 1b	Alue: C he CSC positio Name CSC After CSC Before de	on bit 0) All Ob n in the pipe. Description CSC is after gamma and DPST image enhancement CSC is before gamma and DPST image enhancement	All					
	Project: Default V Selects th Ob 1b CSC_Mo Project: Default V	Alue: 0 he CSC positio Name CSC After CSC Before de Alue: 0	on bit 0) All Db n in the pipe. Description CSC is after gamma and DPST image enhancement CSC is before gamma and DPST image enhancement	All					
	Project: Default V Selects th Ob 1b CSC_Mo Project: Default V	Alue: 0 he CSC positio Name CSC After CSC Before de Alue: 0	on bit 0) All Db n in the pipe. Description CSC is after gamma and DPST image enhancement CSC is before gamma and DPST image enhancement	All					
	Project: Default V Selects th Ob 1b CSC_Mo Project: Default V Selects th	Alue: 0 he CSC positio Name CSC After CSC Before de Alue: 0 he CSC directio	on bit 0) All Db n in the pipe. Description CSC is after gamma and DPST image enhancement CSC is before gamma and DPST image enhancement All Db on. Input and output formats and position within the pipe Description	All					



2.11.2.8 **Pre-CSC_B High Color Channel Offset**

Register T	ype:	MMIO			
Address C		49130h-49133h			
Project:		All			
Default Va	lue:	0000000h			
Access:		R/W			
Size (in bi	ts):	32			
Double Bu	Iffer Update Point:	Start of vertical blank after armed			
Double Bu	uffer Armed By:	Write to CSC_B_Mode			
Bit		Descript	ion		
31:13	Reserved Project: All Format:				
12:0	Pre-CSC_B_High_Color_Channel_Offset Project: All				
This 13-bit 2's complement value is used to give an offset to the color channel as it enters CSC logic.					

2.11.2.9 **Pre-CSC_B Medium Color Channel Offset**

Register T	ype:	MMIO		
Address C	offset:	49134h-49137h		
Project:		All		
Default Va	lue:	0000000h		
Access:		R/W		
Size (in bit	ts):	32		
Double Bu	Iffer Update Point:	Start of vertical blank after armed		
Double Bu	iffer Armed By:	Write to CSC_B_Mode		
Bit		Descript	ion	
31:13	Reserved Project: All Format:			
12:0	Pre-CSC_B_Mediu	m_Color_Channel_Offset	Project: All	
	This 13-bit 2's comp	plement value is used to give an offs	et to the color channel as it enters CSC logic.	



Register T	Гуре:	MMIO						
Address C	Offset:	49138h-4913Bh						
Project:		All						
Default Value: 00000000h								
Access:		R/W						
Size (in bi	ts):	32						
Double Bu	uffer Update Point:	Start of vertical blank after armed						
Double Bu	uffer Armed By:	Write to CSC_B_Mode						
Bit		Descripti	on					
31:13	Reserved Project: All Format:							
12:0	Pre-CSC_B_Low_	Color_Channel_Offset	Project: All					
	This 13-bit 2's com	This 13-bit 2's complement value is used to give an offset to the color channel as it enters CSC logic.						

2.11.2.10 Pre-CSC_B Low Color Channel Offset

2.12 Display Palette Registers (4A000h–4CFFFh)

The display palette provides a means to correct the gamma of an image stored in a frame buffer to match the gamma of the monitor or presentation device. Additionally, the display palette provide a method for converting indexed data values to color values for VGA and 8-bpp indexed display modes. The display palette is located after the plane blender. Using the individual plane gamma enables, the blended pixels can go through or bypass the palette on a pixel by pixel basis.

The display palette can be accessed through multiple methods and operate in one of three different modes.

8 bit legacy palette mode (for indexed VGA and 8 bpp formats and for legacy gamma):

256 entries of 24 bits each (8 bits per color).

For indexed formats, an 8 bit per pixel value is used to lookup a 24 bit per pixel value from the palette which then is padded to 36 bits. This permits a compact data format to choose from 256 colors out of a larger palette of colors. The legacy palette is accessible through both MMIO and VGA palette register I/O addresses. Through VGA palette register I/O addresses, the palette can look as though there are only 6 bits per color component (this mapping is handled inside the VGA engine).

For legacy gamma, the 36 bits per pixel gamma input is chopped to 24 bits and used to lookup a 24 bit pixel value from the palette which then is padded to 36 bits. This permits a color to be remapped to a different brightness for gamma correction. This provides the lowest quality gamma and should only be used for legacy requirements.

10 bit precision palette mode (for 10 bit gamma):

1024 entries of 30 bits each (10 bits per color).



For 10 bit gamma, the 36 bits per pixel gamma input is chopped to 30 bits and used to lookup a 30 bit pixel value from the palette which then is padded to 36 bits. This permits a color to be remapped to a different brightness for gamma correction. This provides the highest quality gamma for non-indexed pixel data formats of 30 bits per pixel or less.

12 bit interpolated gamma mode:

512 entries of 16 bits each (format described in 12 bit interpolated gamma programming notes).

For 12 bit interpolated gamma, the 36 bits per pixel gamma input is used to lookup reference points (16 bits per color in 12.4 format) along a gamma curve and interpolate a 36 bit pixel result. This permits a color to be re-mapped to a different brightness for gamma correction. This provides the highest quality gamma for pixel data formats greater than 30 bits per pixel.

Pixel chopping refers to removing the LSBs of each color component to reduce bits per pixel. Pixel padding refers to adding LSBs to each color component to increase bits per pixel.

Accesses to the palette entries require that the core display clock is running at the time of the update. Do not access the palette if the pipe is enabled and mode set is not yet complete. All write accesses to the palette must be in dwords. Byte or word writes to the palettes are not allowed.

2.12.1 LGC_PALETTE_A—Pipe A Legacy Display Palette

LGC_PALETTE_A—Pipe A Legacy Display Palette							
Register Type: MMIO							
Address Of	f <mark>set:</mark> 4A0	00h-4A3FFh					
Project:	All						
Default Val	ue: UUl	JUUUUUh					
Access:	R/W	/ (DWORD acce	ess only, n	o byte acce	ess)		
Size (in bits	s): 256	x32					
DWord	Bit				, I	Description	
0255	31:24	Reserved	Project:	All			Format:
	23:16	Red_Palette_	Entry	Project:	All	Format:	
	15:8	Green_Palette	e_Entry	Project:	All	Format:	
	7:0	Blue_Palette_	Entry	Project:	All	Format:	



2.12.2 LGC_PALETTE_B—Pipe B Legacy Display Palette

LGC_PALETTE_B—Pipe B Legacy Display Palette							
Register Ty	<mark>/pe:</mark> MM	10					
Address Of	Address Offset: 4A800h-4ABFFh						
Project:	Project: All						
Default Val	ue: UUl	JUUUUUh					
Access:	R/W	(DWORD access only	/, no byte acce	ess)			
Size (in bits	<mark>s):</mark> 256	x32	-	-			
DWord	Bit			I	Description		
0255	31:24	Reserved Project	t: All		Fo	rmat:	
	23:16	Red_Palette_Entry	Project:	All	Format:		
	15:8	Green_Palette_Entr	y Project:	All	Format:		
	7:0	Blue_Palette_Entry	Project:	All	Format:		

2.12.3 PREC_PALETTE_A—Pipe A Precision Display Palette

	10 bit Precision Palette Mode Format						
Project:	All						
Format for	Format for 10 bit precision palette mode.						
Bit	Bit Description						
31:30	Reserved Project: All	Format:					
29:20	Red_Palette_Entry	Project: All					
19:10	Green_Palette_Entry	Project: All					
9:0	Blue_Palette_Entry	Project: All					

12-bit Interpolated Precision Palette Mode (odd Dword) Format					
Project:	All				
Format for	12 bit interpolated gamma mode, odd dwords.				
Bit	Description				
31:30	Reserved Project: All	Format:			
29:20	Red_ Base[11:2]	Project: All			
19:10	Green_ Base[11:2]	Project: All			
9:0	Blue_Base[11:2]	Project: All			



12-bit Interpolated Precision Palette Mode (even Dword) Format

Project: All Format for 12 bit interpolated gamma mode, odd dwords..

			Description		
Reserved	Project:	All		Format:	MBZ
Red_Base[1:0]]			Project:	All
Red_Fraction				Project:	All
Reserved	Project:	All		Format:	
Green_Base[1	:0]			Project:	All
Green_Fractio	n			Project:	All
Reserved	Project:	All		Format:	
Blue_Base[1:0)]			Project:	All
Blue_Fraction				Project:	All
Reserved	Project:	All		Format:	
	Red_Base[1:0] Red_Fraction Reserved Green_Base[1 Green_Fraction Reserved Blue_Base[1:0 Blue_Fraction	Red_Base[1:0]Red_FractionReservedProject:Green_Base[1:0]Green_FractionReservedProject:Blue_Base[1:0]Blue_Fraction	Red_Base[1:0] Red_Fraction Reserved Project: All Green_Base[1:0] Green_Fraction Reserved Project: All Blue_Base[1:0] Blue_Fraction	Reserved Project: All Red_Base[1:0] Reserved Reserved Project: All Green_Base[1:0] Green_Fraction Reserved Project: All Blue_Base[1:0] Blue_Fraction	ReservedProject:AllFormat:Red_Base[1:0]Project:Project:Red_FractionProject:AllFormat:Green_Base[1:0]Project:AllFormat:Green_FractionProject:AllFormat:Blue_Base[1:0]Project:AllFormat:Blue_Base[1:0]Project:AllFormat:Project:AllFormat:Project:AllFormat:Blue_Base[1:0]Project:AllProject:Project:Project:AllProject:Project:

PREC_PALETTE_A—Pipe A Precision Display Palette(10 bit)							
Register Type: MMIO							
Address Of	fset:	4B0(00h-4BFFFh				
Project:		All					
Exists If:		PIPE	ACONF:Pipe_A_P	alette/Gamma	_Unit_	mode = 01b	
Default Val	ue:	UUU	IUUUUUh				
Access:		R/W	(DWORD access o	nly, no byte ad	cess)		
Size (in bits	s):	1024	1x32		-		
DWord	Bit					Description	
01023	31:0)	10bit_mode	Project:	All	Format:	10 bit Precision Palette Mode Format
			See format description above				



PREC_PALETTE_A—Pipe A Precision Display Palette(12 bit)								
Register Ty	gister Type: MMIO							
Address Of	fset: 4B0	000h-4BFFFh						
Project:	All							
Exists If:	PIP	EACONF:Pipe_A_Palette/Gamma_Unit_mode = 10b						
Default Valu	ue: UUl	JUUUUUh						
Access:	R/W	/ (DWORD access only, no byte access)						
Size (in bits	;): 102	4x32						
DWord	Bit	Description						
01023	63:32	12bit_odd Project: All Format: 12-bit Interpolated Precision Palette Mode (odd Dword) Format						
		FormatDesc: Format for 12 bit interpolated gamma mode, odd dwords.						
	31:0	12bit_even Project: All Format: 12-bit Interpolated Precision Palette Mode (even Dword) Format						
		FormatDesc: Format for 12 bit interpolated gamma mode dwords						

2.12.4 PREC_PALETTE_B—Pipe B Precision Display Palette

PREC_PALETTE_B—Pipe B Precision Display Palette(10 bit)								
Register Ty	<mark>/pe:</mark> N	MMIO						
Address Of	ifset: 4	C000h-4CFFFh						
Project:	A	JI						
Exists If:	Р	PIPEBCONF:Pipe_B_P	alette/Gamma	_Unit_	mode = 01b			
Default Val	ue: U	IUUUUUUh						
Access:	R	W (DWORD access c	nly, no byte ad	cess)				
Size (in bits	s): 1	024x32						
DWord	Bit				Description			
01023	31:0	10bit_mode	Project:	All	Format:	10 bit Precision Palette Mode Format		
		FormatDesc: Form	FormatDesc: Format for 10 bit precision palette mode.					



PREC_PALETTE_B—Pipe B Precision Display Palette(12 bit)								
Register Type: MMIO								
Address Of	s Offset: 4C000h-4CFFFh							
Project:	t: All							
Exists If:	xists If: PIPEBCONF:Pipe_B_Palette/Gamma_Unit_mode = 10b							
Default Val	Default Value: UUUUUUUh							
Access:	R/W	/ (DWORD access only, no byte access)						
Size (in bits	s): 102	4x32						
DWord	Bit	Description						
01023	63:32	12bit_odd Project: All Format: 12-bit Interpolated Precision Palette Mode (odd Dword) Format						
	Format Desc: Format for 12 bit interpolated gamma mode, odd dwords.							
	31:0	12bit_even Project: All Format: 12-bit Interpolated Precision Palette Mode (even Dword) Format						
		FormatDesc: Format for 12 bit interpolated gamma mode dwords.						

12-bit Interpolated Gamma Programming Notes:

The 12-bit gamma correction curve is represented by specifying a set of reference points spaced equally along the desired curve. Red, Green, and Blue each have 513 reference points. The first 512 reference points are stored in the precision palette RAM, and the final value is stored in the GCMAX register. The first 512 reference points are 16 bits represented in a 12.4 format with 12 integer and 4 fractional bits. The final reference points are 17 bits represented in a 13.4 format with 13 integer and 4 fractional bits.

During operation the appropriate reference point pairs (adjacent) are selected for each color, and the output is interpolated between these two reference point values.

To program the gamma correction reference points, calculate the desired gamma curve for inputs from 0 to 4096. Every 8th point on the curve (0, 8, 16 ... 4088, 4096) becomes a reference point. Convert the gamma value to the 13.4 format. The first 512 reference points are saved to the precision palette RAM, where the even DWords contain the lower 6 bits of the reference point value, and the odd DWords contain the upper 10 bits of the reference point value. The final 513th reference point is saved in the GCMAX registers in 13.4 format.

Example equation for gamma curve of 2.2:

For (X = 0..4096) { gamma = [(X / 4096) ^ 2.2] * 4096 }

The curve must be flat or increasing, never decreasing.



2.12.5 PIPEAGCMAX—Pipe A Gamma Correction Max

Pipe Max Gamma Correction Format						
Project: Default Va	All lue: 00010000h					
Bit	Description					
31:17	Reserved Project: All	Format:				
16:0	Max_Color_Gamma_Correction_Point 513 th reference point for the color channel of the 12-bit pipe piecewise linear value should always be programmed to be less than or equal to 4096.0.	Project: All ar gamma correction. The				

	Р	IPEAGCMA	X—Pipe A	A Ga	mma Co	prrection Max
Register Ty Address Of Project: Default Val Access: Size (in bit:	ifset: 4D0 All ue: 000 R/W	1000h-4D00Bh 10000h /				
DWord	Bit				Description	
0	31:0	Red	Project:	All	Format:	Pipe Max Gamma Correction Format
1	31:0	Green	Project:	All	Format:	Pipe Max Gamma Correction Format
2	31:0	Blue	Project:	All	Format:	Pipe Max Gamma Correction Format



2.12.6 PIPEBGCMAX — Pipe B Gamma Correction Max

	Р	IPEBGCMA	X—Pipe E	3 Ga	mma Co	rrection Max
Register Ty Address O Project: Default Val Access: Size (in bit	ffset: 4D0 All lue: 000 R/V	0 10h-4D01Bh 010000h V				
DWord	Bit				Description	
0	31:0	Red	Project:	All	Format:	Pipe Max Gamma Correction Format
1	31:0	Green	Project:	All	Format:	Pipe Max Gamma Correction Format
2	31:0	Blue	Project:	All	Format:	Pipe Max Gamma Correction Format

2.13 Software Flag Registers (4F000h–4F10Fh)

2.13.1 Software Flag Registers

Software Flag Registers								
Register Type: MMIO								
Address Off	set: 4F0	00h-4F08Fh						
Project:	All	All						
Default Valu	e: 000	0000000h						
Access:	R/W							
Size (in bits): 36x	32						
	These registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.							
DWord	Bit Description			Description				
035	31:0	Reserved	Project:	All	Format: PBC			



2.13.2 DE_LOAD_SL — Display Load Scan Lines

	DE_LOAD_SL—Display Load Scan Lines					
Register Type:	MMIO					
Address Offset:	4F100h-4F103h					
Project:	DevSNB					
Default Value:	0000000h					
Access:	R/W					
Size (in bits):	32					
This register is u	This register is used to initiate a display scan line compare on DevSNB:D2 and later steppings.					

When this register is written with the Init_Compare bit set to 1b, the Display Engine (DE) will start comparing the display pipe timing generator current scan line value (current scan line) with the start scan line value (current scan line >= start scan line) and the end scan line value (current scan line <= end scan line) to decide if the the pipe scan line is inside or outside the scan line window of interest. DE will wait until the current scan line is either outside (Inclusive mode) or inside (Exclusive mode) the scan line window, then trigger a scan line event and stop any further comparing.

The scan line event can cause display to send a scan line compare response to the render command streamer, used for releasing a MI_WAIT_FOR_EVENT on scan line window, if unmasked in the DERRMR mask register 0x44050. The scan line event can also cause display to generate a scan line compare interrupt, if unmasked and enabled in the DEIMR and DEIER display engine interrupt registers.

The end scan line value must be greater than or equal to the start scan line value.

The current scan line is a 13 bit value, but the scan line comparison is only done on the upper 10 bits. This gives an 8 line granularity on the compare.

The programmable range can include the vertical blank.

In interlaced display timings, the current scan line is the the current line of the current interlaced field.

Notes for command streamer programming to use this display load scan lines register:

- Either MMIO or a MI_LOAD_REGISTER_IMM command can be used to unmask the scan line render response 0x44050. That can be done any time before programming this register.
- In order to use MI_WAIT_FOR_EVENT on scan line window, DE_LOAD_SL must be programmed using MI_LOAD_REGISTER_IMM immediately prior to the MI_WAIT_FOR_EVENT on scan line window, both commands must be in the same cacheline, both commands must be executed using the same tail or batch update, and if sync flush is enabled, MI_SUSPEND_FLUSH must be used to suspend flushes prior to the commands.



Bit	1		D_SL—Display Load Scan Lines Description							
			Description							
31	Initiate_C	-								
		Default Value: 0b								
		This field initiates the scan line compare.								
		When this register is written with this bit set to 1b, the display engine will do one complete comparison cycle, trigger a scan line event, then stop comparing.								
	, ,	Do not write this register again until after any previous scan line compare has completed.								
	A compare can not be cancelled by writing with this bit set to 0b.									
	Value	Name	Description	Project						
	0b	Do nothing	Do nothing	All						
	1b	Initiate	Initiate the scan line compare.	All						
30	Inclusive	_Exclusive_Sele	ct							
	Default Va	alue: C	b							
			ne scan line compare is done in exclusive mode, where display trig							
			e the window (wait while outside window), or inclusive mode, when	e display						
	triggers th	e scan line event	when outside the scan line window (wait while inside window).							
	Value	Name	Description	Project						
	0b	Exclusive	Exclusive mode: trigger scan line event when inside the scan line window (wait while outside window)	All						
	1b	Inclusive	Inclusive mode: trigger scan line event when outside the scan line window (wait while inside window)	All						
29	Pipe_Sel	ect								
	Default Va	alue: C	b							
	This field	selects which disp	play pipe timing generator scan line value to use for the compare.							
	Value	Name	Description	Project						
	0b	Pipe A	Display Pipe A	All						
	0b 1b	Pipe A Pipe B	Display Pipe A Display Pipe B	All All						
28:19		Pipe B		All						
28:19	1b Start_Sca	Pipe B	Display Pipe B	All at:						
28:19	1b Start_Sca This field	Pipe B an_Line specifies the <u>upp</u>	Display Pipe B Project: DevSNB Forma	All at:						
	1b Start_Sca This field	Pipe B an_Line specifies the <u>upp</u> 3 bits are reserv	Display Pipe B Project: DevSNB Forma er 10 bits of the starting scan line number of the scan line window.	All at:						
28:19 18:13 12:3	1b Start_Sca This field The <u>lowe</u>	Pipe B an_Line specifies the <u>upper</u> 3 bits are reserv Project:	Display Pipe B Project: DevSNB Forma er 10 bits of the starting scan line number of the scan line window. ed below and not programmable and not compared. All Format:	All						
	1b Start_Sca This field The lowe Reserved End_Sca	Pipe B an_Line specifies the <u>upp</u> 1 3 bits are reserv Project: n_Line	Display Pipe B Project: DevSNB Forma er 10 bits of the starting scan line number of the scan line window. ed below and not programmable and not compared. All Format:	All at:						
18:13	1b Start_Sca This field The lowe Reserved End_Sca This field	Pipe B an_Line specifies the <u>upper</u> 3 bits are reserv Project: n_Line specifies the <u>upper</u>	Display Pipe B Project: DevSNB Forma er 10 bits of the starting scan line number of the scan line window. ed below and not programmable and not compared. All Format: Project: DevSNB Forma	All						



3. North Pipe and Port Controls (60000h–6FFFh)

3.1 Pipe A Timing

3.1.1 HTOTAL_A—Pipe A Horizontal Total Register

	нт	OTAL_A	—Pipe A	Horizontal Total R	egister		
Register Ty Address O Project: Default Val Access: Size (in bits	ffset: 60000h All ue: 000000 R/W	-60003h 00h					
Bit				Description			
31:29	Reserved	Project:	All		Format:	MBZ	
28:16	Pipe_A_Hori	zontal_Total	_Display_Clock	(S		Project:	All
		d, front/back l		ip to 8192 pixels encompassin ce period. This field is program			locks
	This number of clocks needs to be a multiple of two when driving the LVDS port in two channel mode. This value should always be equal or greater to the sum of the horizontal active and the horizontal blank, and border region sizes.						
15:12	Reserved	Project:	All		Format:	MBZ	
11:0	Pipe_A_Hori	zontal_Activ	e_Display_Pixe	ls		Project:	All
		tive display pi		Display resolutions up to 4096 d pixel number 0. The value p	•		
				o multiples of two pixels when orizontal active display size all	0	0	VDS



3.1.2 HBLANK_A—Pipe A Horizontal Blank Register

Register Type: MMIO Address Offset: 60004h-60007h Project: All Default Value: 0000000h Access: R/W Size (in bits): 32 Bit Description 31:29 Reserved Project: All Pipe_A_Horizontal_Blank_End Project: All This 13-bit field specifies the position of Horizontal Blank End expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HBLANK End pixel position, where the first active pixel is considered position 0; the second active pixel is considered position 1, etc. Horizontal blank ending at the same point as the horizontal total indicates that there is no left hand border area. HBLANK size has a minimum value of 32 clocks. The number of clocks within blank needs to be a multiple of two when driving the LVDS port in two channel mode. The value loaded in the register would be equal to RightBorder+Active+HBlank-1. The value loaded in the register must always be programmed to the same value as the Horizontal Total. 15:13 Reserved Project: All This 13-bit field specifies the Horizontal Blank Start position expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HBLANK Start pixel position, where the first active pixel is considered positi		HB	LANK_A	-Pip	e A Horizontal Blank Register	
31:29 Reserved Project: All Format: 28:16 Pipe_A_Horizontal_Blank_End Project: All This 13-bit field specifies the position of Horizontal Blank End expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HBLANK End pixel position 1, etc. Horizontal active pixel is considered position 0; the second active pixel is considered position 1, etc. Horizontal blank ending at the same point as the horizontal total indicates that there is no left hand border area. HBLANK size has a minimum value of 32 clocks. The number of clocks within blank needs to be a multiple of two when driving the LVDS port in two channel mode. The value loaded in the register would be equal to RightBorder+Active+HBlank-1. The border must be 0, so this register must always be programmed to the same value as the Horizontal Total. Format: 15:13 Reserved Project: All This 13-bit field specifies the Horizontal Blank Start position expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HBLANK Start pixel position , where the first active pixel is considered position 0; the second active pixel is considered position 1, etc. The number of clocks for both left and right borders need to be a multiple of two when driving the LVDS port in two channel mode. The value loaded in the register would be equal to RightBorder+Active-1.	Address Of Project: Default Val Access:	ffset: 600041 All ue: 000000 R/W				
28:16 Pipe_A_Horizontal_Blank_End Project: All This 13-bit field specifies the position of Horizontal Blank End expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HBLANK End pixel position 1, etc. Horizontal blank ending at the same point as the horizontal total indicates that there is no left hand border area. HBLANK size has a minimum value of 32 clocks. The number of clocks within blank needs to be a multiple of two when driving the LVDS port in two channel mode. The value loaded in the register would be equal to RightBorder+Active+HBlank-1. The border must be 0, so this register must always be programmed to the same value as the Horizontal Total. Project: All 15:13 Reserved Project: All 12:0 Pipe_A_Horizontal_Blank_Start Project: All This 13-bit field specifies the Horizontal Blank Start position expressed in terms of the absolute pixel number relative to the horizontal active pixel is considered position 0; the second active pixel is considered position 1, etc. 12:0 Pipe_A_Horizontal_Blank_Start Project: All The number of clocks for both left and right borders need to be a multiple of two when driving the LVDS port in two channel mode. The value programmed should be the HBLANK Start pixel position 1, etc. The unmber of clocks for both left and right borders need to be a multiple of two when driving the LVDS port in two channel mode. Horizontal blank should only start after the end of the horizontal active region. The va	Bit				Description	
This 13-bit field specifies the position of Horizontal Blank End expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HBLANK End pixel position, where the first active pixel is considered position 0; the second active pixel is considered position 1, etc. Horizontal blank ending at the same point as the horizontal total indicates that there is no left hand border area. HBLANK size has a minimum value of 32 clocks. The number of clocks within blank needs to be a multiple of two when driving the LVDS port in two channel mode. The value loaded in the register would be equal to RightBorder+Active+HBlank-1. The border must be 0, so this register must always be programmed to the same value as the Horizontal Total. 15:13 Reserved Project: All Format: Pipe_A_Horizontal_Blank_Start This 13-bit field specifies the Horizontal Blank Start position expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HBLANK Start pixel position, where the first active pixel is considered position 0; the second active pixel is considered position 1, etc. The number of clocks for both left and right borders need to be a multiple of two when driving the LVDS port in two channel mode. Horizontal blank should only start after the end of the horizontal active region. The ualue loaded in the register would be equal to RightBorder+Active-1.	31:29	Reserved	Project:	All	Format:	
12:0 Pipe_A_Horizontal_Blank_Start Project: All This 13-bit field specifies the Horizontal Blank Start position expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HBLANK Start pixel position, where the first active pixel is considered position 0; the second active pixel is considered position 1, etc. The number of clocks for both left and right borders need to be a multiple of two when driving the LVDS port in two channel mode. Horizontal blank should only start after the end of the horizontal active region. The value loaded in the register would be equal to RightBorder+Active-1.	28:16	This 13-bit field specifies the position of Horizontal Blank End expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HBLANK End pixel position, where the first active pixel is considered position 0; the second active pixel is considered position 1, etc. Horizontal blank ending at the same point as the horizontal total indicates that there is no left hand border area. HBLANK size has a minimum value of 32 clocks. The number of clocks within blank needs to be a multiple of two when driving the LVDS port in two channel mode. The value loaded in the register would be equal to RightBorder+Active+HBlank-1. The border must be 0, so this register must always be programmed to the same value as the				
 This 13-bit field specifies the Horizontal Blank Start position expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HBLANK Start pixel position, where the first active pixel is considered position 0; the second active pixel is considered position 1, etc. The number of clocks for both left and right borders need to be a multiple of two when driving the LVDS port in two channel mode. Horizontal blank should only start after the end of the horizontal active region. The value loaded in the register would be equal to RightBorder+Active-1. 	15:13	Reserved	Project:	All	Format:	
I THE DOLLAR MUST BE USED TO THE FOUND A SWALL AND A SUBJECT TO THE SAME WALL AND A SECTION AND A SECTION AND A	12:0	This 13-bit fi number relat Start pixel po considered p The number LVDS port in active region The value lo	eld specifies t tive to the hori osition, where osition 1, etc. of clocks for to two channel n. aded in the re	he Horizon zontal acti the first ar both left ar mode. Ho gister wou	ntal Blank Start position expressed in terms of the absolute pixel ive display start. The value programmed should be the HBLANK ctive pixel is considered position 0; the second active pixel is nd right borders need to be a multiple of two when driving the prizontal blank should only start after the end of the horizontal and be equal to RightBorder+Active-1.	



	HSYNC_A—Pipe A Horizon						
Register T							
Address C	Dffset: 60008h-6000Bh All						
Project: Default Va							
Size (in bi							
Bit	Descrip	tion					
31:29	Reserved Project: All	Format: MBZ					
28:16	Pipe_A_Horizontal_Sync_End						
	Project: All						
	Default Value: 0b						
	number relative to the horizontal active display start. The End pixel position, where the first active pixel is considered position 1, etc. The number of clocks in the sync period needs to be a two channel mode. This value should be greater than the	lered position 0; the second active pixel is multiple of two when driving the LVDS port in the horizontal sync start position and would be					
	loaded with the Active+RightBorder+FrontPorch+Sync-						
15:13	Reserved Project: All	Format: MBZ					
12:0	Pipe_A_Horizontal_Sync_Start						
	Project: All						
	Default Value: 0b						
	This 13-bit field specifies the horizontal Sync Start posi number relative to the horizontal active display start. T						
	Start pixel position, where the first active display start. T Start pixel position 1, etc. Note that when HSYNC Start HSYNC and HBLANK will be asserted on the same pix than HBLANK start.	dered position 0; the second active pixel is art is programmed equal to HBLANK Start, both					

3.1.3 HSYNC_A—Pipe A Horizontal Sync Register



3.1.4 VTOTAL_A—Pipe A Vertical Total Register

VTOTAL_A—Pipe A Vertical Total Register							
Project: Default Val Access:	Address Offset:6000Ch-6000FhProject:AllDefault Value:00000000hAccess:R/WSize (in bits):32						
Bit	Description						
31:29	Reserved	Project:	All	Format:			
28:16	Pipe_A_Vertical_Total_Display_Lines Project: All This 13 bit field provides Vertical Total up to 8192 lines encompassing the Vertical Active Display Lines, top/bottom border and retrace period. The value programmed should be the number of lines required minus one. Vertical total needs to be large enough to be greater than the sum of the vertical active, vertical border, and the vertical blank regions. The vertical counter is incremented on the leading edge of the horizontal sync. For interlaced display modes, this indicates the total number of lines in both fields. In interlaced modes, hardware automatically divides this number by 2 to get the number of lines in each field.						
15:12	Reserved	Project:	All	Format:			
11:0	with the desir	eld provides v ed number o e area must b h fields. In ir	ertical activ f lines minu e seven line iterlaced mo	hes Project: All e display resolutions up to 4096 lines. It should be programmed one. When using the internal panel fitting logic, the minimum s. For interlaced display modes, this indicates the total number des, hardware automatically divides this number by 2 to get the			



3.1.5 VBLANK_A—Pipe A Vertical Blank Register

	VI	BLANK_	A—Pi	pe A Vertical Blank Register	
Register Ty Address O Project: Default Val Access: Size (in bit	ffset: 60010h All lue: 000000 R/W	1-60013h 100h			
Bit				Description	
31:29	Reserved	Project:	All	Format:	
28:16	6 Pipe_A_Vertical_Blank_End Project: All This 13-bit field specifies the Vertical Blank End position expressed in terms of the absolute Line number relative to the vertical active display start. The value programmed should be the VBLANK End line position, where the first active line is considered line 0, the second active line is considered line 1, etc. The end of vertical blank should be after the start of vertical blank and before or equal to the vertical total. This register should be loaded with the Vactive+BottomBorder+VBlank-1. For interlaced display modes, hardware automatically divides this number by 2 to get the vertical blank end in each field. It does not count the two half lines that get added when operating in modes with half lines. The border must be 0, so this register must always be programmed to the same value as the Vertical Total.				
15:13	Reserved	Project:	All	Format:	
12:0	relative to the position, whe Minimum ver active. This hardware au count the two	eld specifies t e vertical activer ere the first activer tical blank siz register is loa tomatically di o half lines the	the Vertica ve display ctive line is ze is requir aded with the vides this r at get adde	Project: All Blank Start expressed in terms of the absolute line number start. The value programmed should be the VBLANK Start line considered line 0, the second active line is considered line 1, etc. ed to be at least three lines. Blank should start after the end of ne Vactive+BottomBorder-1. For interlaced display modes, number by 2 to get the vertical blank start in each field. It does not ed when operating in modes with half lines. r must always be programmed to the same value as the Vertical	



3.1.6 VSYNC_A—Pipe A Vertical Sync Register

	VSYNC_/	A—Pipe A Vertica	al Sync Register
Register Ty Address O Project: Default Val Access: Size (in bits	pe: MMIO fset: 60014h-60017h All ue: 00000000h R/W		
Bit		Descrip	tion
31:29	Reserved Project:	All	Format:
28:16	number relative to the verti line position, where the firs etc. This register should be display modes, hardware a	e Vertical Sync End position cal active display start. The t active line is considered lin e loaded with Vactive+Botto utomatically divides this nur	Project: All n expressed in terms of the absolute Line value programmed should be the VSYNC End ue 0, the second active line is considered line 1, mBorder+FrontPorch+Sync-1. For interlaced nber by 2 to get the vertical sync end in each d when operating in modes with half lines.
15:13	Reserved Project:	All	Format:
12:0	number relative to the verti line position, where the firs etc. This register would be modes, hardware automati	e Vertical Sync Start positio cal active display start. The t active line is considered lin loaded with Vactive+Botton cally divides this number by	Project: All on expressed in terms of the absolute line value programmed should be the VSYNC Start e 0, the second active line is considered line 1, nBorder+FrontPorch-1. For interlaced display 2 to get the vertical sync start in each field. It operating in modes with half lines.



	PIP	EASRC—Pipe	A Source Image S	ize		
Register Ty Address O Project: Default Val Access: Size (in bit Double Bu	ype: ffset: ue:	MMIO 6001Ch-6001Fh All 00000000h R/W 32 Start of vertical blank				
Bit			Description			
31:28	Reserved Proj	ect: All		Format:	MBZ	
27:16	Pipe_A_Horizontal	_Source_Image_Size			Project:	All
	image created by th image size minus or It must represent as	e display planes sent to t ne. size that is a multiple of tw	nage size up to 4096. This o he blender. The value progra vo (even numbers) when driv e, the value programmed wil	ammed sho ving the LV	uld be the so DS port in tw	ource
	programmed to a va		n an external device, this reg ntal active. This is the only r pe is enabled.			isters
15:12	Reserved Proj	ect: All		Format:	MBZ	
11:0	Pipe_A_Vertical_S	ource_Image_Size			Project:	All
		y the display planes sent	mage size up to 4096 lines. to the blender. The value p			
		of panel fitting internal or i alue identical to the vertica	n an external device, this reg al active.	gister field v	would be	
	For interlaced displa source image size ir		natically divides this number	by 2 to get	the vertical	

3.1.7 **PIPEASRC—Pipe A Source Image Size**



3.1.8 VSYNCSHIFT_A— Vertical Sync Shift Register

	VS	YNCSHI	FT_A— V	ertical Sync Shift R	egister	
Register Ty Address O Project: Default Val Access: Size (in bit Trusted Ty	ffset: 60028 All lue: 000000 R/W s): 32	h-6002Bh 000h				
Bit				Description		
31:13	Reserved	Project:	All		Format:	
12:0	This value s terms of the This value w Typically, the between suc (horizontal s (use the actu programmed This vertical	pecifies the ve absolute pixel vill only be use e interlaced se ccessive horizo sync start - floo ual horizontal s d into the regis sync shift only	I number relatived if the PIPEAC econd field vertice ontal syncs, so or[horizontal tota sync start and heters)	the interlaced second field. In a	start. laced mode. fter the point halfway be programmed to: e minus one values	

3.1.9 Pipe A M/N Values

Calculation of TU is as follows:

For modes that divide into the link frequency evenly,

Active/TU = payload/capacity

Please note that this is the same ratio as data m/n:

Payload/capacity = dot clk * bytes per pixel / ls_clk * # of lanes



3.1.9.1 PipeADataM1— Pipe A Data M value 1

	PipeAD	DataM1— P	ipe A Data	M value 1		
pe: MMIO						
f <mark>set:</mark> 60030h	n-60033h					
All						
ue: 000000)00h					
R/W						
s): 32						
en switching b	between two re	efresh rates, both	the M1/N1 data an	d link values and the		
			Description			
Reserved	Project:	All		Format:	MBZ	
TU_Size					Project:	All
This field is t	he size of the	transfer unit for D	P, minus one.			
Default value	e to program	= 111111 (TU siz	ze of 64)			
Reserved	Project:	All		Format:	MBZ	
Pipe_A_Data	a_M_value				Project:	All
This field is t	he m value fo	r internal use of th	ne DDA. Calculatio	on of this value is as fo	ollows:	
Data m/n = o	dot clock * by	/tes per pixel / Is	_clk * # of lanes			
Please note t	that in the Dis	playPort specifica	tion, dot clock is re	ferred to as strm_clk		
			t factor needs to be	e taken into account. ٦	The calculation	on of
Data M/N =	(dot_clock *	bytes_per_pixe	l) /			
(ls_c	lk * num_lan	es * pix_repeat	_factor)			
r	fset: 60030h All All 000000 R/W : 32 imary pipe da en switching b grammed. Da Reserved TU_Size This field is t Default valu Reserved Pipe_A_Data This field is t Data m/n = 0 In HDMI pixe this value wo Data M/N =	fset: 60030h-60033h All Ite: 0000000h R/W): 32 imary pipe data M value us en switching between two regrammed. Data M value 1 is Reserved Project: TU_Size This field is the size of the Default value to program Reserved Project: Pipe_A_Data_M_value This field is the m value fo Data m/n = dot clock * by Please note that in the Dis In HDMI pixel-repeat mode this value would then be as Data M/N = (dot_clock *	fset: 60030h-60033h All All ie: 00000000h R/W): 32 imary pipe data M value used for embedded en switching between two refresh rates, both prammed. Data M value 1 is used for the high Reserved Project: All TU_Size This field is the size of the transfer unit for D Default value to program = 111111 (TU siz) Reserved Project: All Pipe_A_Data_M_value This field is the m value for internal use of th Data m/n = dot clock * bytes per pixel / Is Please note that in the DisplayPort specifica In HDMI pixel-repeat modes, the pixel repeat this value would then be as follows: Data M/N = (dot_clock * bytes_per_pixel	fset: 60030h-60033h All All ie: 0000000h R/W): 32 imary pipe data M value used for embedded DisplayPort and FI en switching between two refresh rates, both the M1/N1 data an prammed. Data M value 1 is used for the higher power M value Description Reserved Project: All TU_Size This field is the size of the transfer unit for DP, minus one. Default value to program = 111111 (TU size of 64) Reserved Project: All Pipe_A_Data_M_value This field is the m value for internal use of the DDA. Calculatic Data m/n = dot clock * bytes per pixel / ls_clk * # of lanes Please note that in the DisplayPort specification, dot clock is re In HDMI pixel-repeat modes, the pixel repeat factor needs to be	First: 60030h-60033h All Ite: 00000000h R/W): 32 imary pipe data M value used for embedded DisplayPort and FDI. It is used in conjuren switching between two refresh rates, both the M1/N1 data and link values and the ligrammed. Data M value 1 is used for the higher power M value setting. Description Reserved Project: All Format: TU_Size This field is the size of the transfer unit for DP, minus one. Default value to program = 111111 (TU size of 64) Reserved Project: All Format: Pipe_A_Data_M_value This field is the m value for internal use of the DDA. Calculation of this value is as for Data m/n = dot clock * bytes per pixel / Is_clk * # of lanes Please note that in the DisplayPort specification, dot clock is referred to as strm_clk In HDMI pixeI-repeat modes, the pixeI repeat factor needs to be taken into account. This value would then be as follows: Data M/N = (dot_clock * bytes_per_pixel) /	Set: 60030h-60033h All Ie: 00000000h R/W): 32 imary pipe data M value used for embedded DisplayPort and FDI. It is used in conjunction with th en switching between two refresh rates, both the M1/N1 data and link values and the M2/N2 link varammed. Data M value 1 is used for the higher power M value setting. Description Reserved Project: All Format: MBZ TU_Size Toject: All Format: MBZ Default value to program = 111111 (TU size of 64) Reserved Project: All Format: MBZ Pipe_A_Data_M_value Project: All Project: All Project: MBZ Pipe_A_Data_M_value Project: All Project: All Project: All



3.1.9.2 PipeADataN1— Pipe A Data N value 1

	PipeADataN1— Pipe A Data N value 1
Register Type:	MMIO
Address Offset:	60034h-60037h
Project:	All
Default Value:	0000000h
Access:	R/W
Size (in bits):	32
the data M value M2/N2 link value	ry pipe data N value used for embedded DisplayPort and FDI. It is used in conjunction with 1. When switching between two refresh rates, both the M1/N1 data and link values and the s must be programmed. This value updates at the beginning of vblank. Data N value 1 is her power N value setting.

Bit Description 31:24 All Format: MBZ Reserved Project: 23:0 Pipe_A_Data_N_value Project: All This field is the n value for internal use of the DDA. Calculation of this value is as follows: Data m/n = dot clock * bytes per pixel / ls_clk * # of lanes Please note that in the DisplayPort specification, dot clock is referred to as strm_clk In HDMI pixel-repeat modes, the pixel repeat factor needs to be taken into account. The calculation of this value would then be as follows: Data M/N = (dot_clock * bytes_per_pixel) / (ls_clk * num_lanes * pix_repeat_factor)



3.1.9.3 PipeADataM2— Pipe A Data M value 2

	Pi	i peAD a	ataM2— Pipe	A Data M valu	e 2		
the data N M2/N2 link	fset: 60038h-600 All All ue: 00000000h R/W Si: second pipe data value 2.	M value witching b	etween two refresl ed. This value upd	d DisplayPort and FDI. h rates, both the M1/N ates at the beginning c	1 data and	l link values	and the
Bit			De	escription			
31	Reserved Pr	roject:	All		Format:	MBZ	
30:25	TU_Size	ze of the t	ransfer unit for DP, m	ninus one		Project:	All
			= 111111 (TU size of				
24	Reserved Pr	roject:	All		Format:	MBZ	
23:0	Data m/n = dot c Please note that ir	n value for clock * byt n the Displ	es per pixel / ls_clk layPort specification,	DA. Calculation of this va * # of lanes dot clock is referred to a tor needs to be taken into	s strm_clk		All on of
		t_clock * t	follows: pytes_per_pixel) / es * pix_repeat_fac	tor)			



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3.1.9.4 PipeADataN2— Pipe A Data N value 2

	PipeADataN2— Pipe A Data N value 2
Register Type:	MMIO
Address Offset:	6003Ch-6003Fh
Project:	All
Default Value:	0000000h
Access:	R/W
Size (in bits):	32
This is the secon	nd pipe data N value used for DisplayPort and FDI. It is used in conjunction with the data N

value 2. When switching between two refresh rates, both the M1/N1 data and link values and the M2/N2 link values must be programmed. This value updates at the beginning of vblank. Data N value 2 is used for the lower power N value setting.

Bit	Descriptio	on						
31:24	Reserved Project: All	Format: MBZ						
23:0	Pipe_A_Data_N_value	Project: All						
	This field is the n value for internal use of the DDA. Cald	culation of this value is as follows:						
	Data m/n = dot clock * bytes per pixel / ls_clk * # of la	anes						
	Please note that in the DisplayPort specification, dot clock is referred to as strm_clk							
	In HDMI pixel-repeat modes, the pixel repeat factor need this value would then be as follows:	ds to be taken into account. The calculation of						
	Data M/N = (dot_clock * bytes_per_pixel) /							
	(ls_clk * num_lanes * pix_repeat_factor)							



3.1.9.5 PipeADPLinkM1— Pipe A Link M value 1

Link M/N = dot_clock / (ls_clk * pix_repeat_factor)

Register T	vpe: MMIO	-				
-	offset: 60040	n-60043h				
Project:	All					
Default Va	lue: 000000)00h				
Access:	R/W					
Size (in bit	t <mark>s):</mark> 32					
seu ioi ili						
Bit	e higher powe			cription		
	Reserved	Project:		cription Format:	MBZ	
Bit		Project:	Desc		MBZ Project:	All
Bit 31:24	Reserved Pipe_A_Linl	Project: <_M_value he m value fe	All		Project:	
Bit 31:24	Reserved Pipe_A_LinI This field is t	Project: <_M_value he m value fe bllows:	All or external transmission in	Format:	Project:	
Bit 31:24	Reserved Pipe_A_Linl This field is t value is as fo Link m/n = p	Project: k_M_value he m value fo bilows: bixel clk / ls_	All or external transmission in _clk	Format:	Project:	



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3.1.9.6 PipeADPLinkN1— Pipe A Link N value 1

	PipeADPLinkN1— Pipe A Link N value 1
Register Type:	MMIO
Address Offset:	60044h-60047h
Project:	All
Default Value:	0000000h
Access:	R/W
Size (in bits):	32
	ry link data N value used for embedded DisplayPort and FDI. It is used in conjunction with When switching between two refresh rates, both the M1/N1 data and link values and the

the link N value 1. When switching between two refresh rates, both the M1/N1 data and link values and the M2/N2 link values must be programmed. This value updates at the beginning of vblank. Link N value 1 is used for the higher power N value setting.

Bit		Description
31:24	Reserved Project: All	Format: MBZ
23:0	Pipe_A_Link_N_value	Project: All
	This field is the n value for external tran of this value is as follows (to be filled in) Link m/n = pixel clk / ls_clk	smission in the Main Stream Attributes and VB-ID. Calculation :
		ification, pixel clk is referred to as strm_clk
	In HDMI pixel-repeat modes, the pixel re this value would then be as follows:	epeat factor needs to be taken into account. The calculation of



3.1.9.7 PipeADPLinkM2— Pipe A Link M value 2

		PI	peade		Pipe A Link	w value z		
Register 1		1MIO						
Address (Offset:	0048h-60	004Bh					
Project:	1	11						
Default Va	alue: (0000000	h					
Access:		2/W						
Size (in bi	ts): :	2						
				ammed. This va setting.	alue upuales al li			value z
					Description			
s used for		er power				Format:	MBZ	
s used for Bit	r the low Reser	er power	M value	setting.				All
s used for Bit 31:24	r the low Reser Pipe_ This fi	er power red	M value Project: I_value m value fo	setting.	Description		MBZ Project:	All
s used for Bit 31:24	r the low Reser Pipe_/ This fi value	red A_Link_M eld is the s as follow	M value Project: I_value m value fo	All	Description	Format:	MBZ Project:	All
s used for Bit 31:24	Reser Reser Pipe_, This fi value Link r	ved Link_N Id is the s as follow Nn = pixe	M value Project: I_value m value fo ws: el clk / ls_	All or external transmi	Description	Format: ream Attributes. Cal	MBZ Project:	All
s used for Bit 31:24	r the low Reser Pipe_/ This fi value Link r Please In HDI	red <u>Link_M</u> eld is the s as follow n/n = pixe note that Il pixel-re	Project: I_value m value fo ws: el clk / ls_	All All or external transmi clk es, the pixel repea	Description ssion in the Main Si tion, pixel clk is refe	Format: ream Attributes. Cal	MBZ Project: Iculation of th	All



3.1.9.8 PipeADPLinkN2— Pipe A Link N value 2

Link M/N = dot_clock / (ls_clk * pix_repeat_factor)

		PipeADF	PLinkN2— Pipe	A Link N value	2		
Register T	ype: MMIO						
Address O	ffset: 6004Cl	6004Ch-6004Fh					
Project:	All	All					
Default Val	lue: 000000	0000000h					
Access:	R/W						
Size (in bit	s): 32						
s used for	the lower pov	ver N value s	setting.				
Bit			Des	cription			
Bit 31:24	Reserved	Project:	All	ription Fo	rmat:	MBZ	
	Reserved Pipe_A_Link	•		-	rmat:	MBZ Project:	All
31:24	Pipe_A_Link This field is the	x_ N_value he n value for	All	-		Project:	
31:24	Pipe_A_Link This field is the of this value	x_ N_value he n value for	All external transmission in to be filled in):	Fo		Project:	
31:24	Pipe_A_Link This field is the of this value Link m/n = p	 he n value for is as follows (t bixel clk / ls_c	All external transmission in to be filled in): clk	Fo	s and V	Project:	



3.2 Pipe B Timing

3.2.1 HTOTAL_B—Pipe B Horizontal Total Register

	HTOTAL_B—Pipe B Horizontal	Total Register	
Register Ty	ype: MMIO		
Address O	ffset: 61000h-61003h		
Project:	All		
Default Val	ue: 0000000h		
Access:	R/W		
Size (in bit	s): 32		
Bit	Description		
31:29	Reserved Project: All	Format:	MBZ
28:16	Pipe_B_Horizontal_Total_Display_Clocks	Project:	All
	See pipe A description		
15:12	Reserved Project: All	Format:	MBZ
11:0	Pipe_B_Horizontal_Active_Display_Pixels	Project:	All
	See pipe A description		

3.2.2 HBLANK_B—Pipe B Horizontal Blank Register

Desident and Th						
Register T						
Address O		ո-61007h				
Project:	All					
Default Va	lue: 000000	000h				
Access:	R/W					
Size (in bit	s): 32					
Bit				Description		
31:29	Reserved	Project:	All		Format:	
28:16	Pipe B Hor	izontal Blan	k_End		Project:	All
	See pipe A d	lescription	_			
15:13	Reserved	Project:	All		Format:	
12:0	Pipe_B_Hor	izontal_Blan	k_Start		Project:	All
	See pipe A d	escription				



3.2.3 HSYNC_B—Pipe B Horizontal Sync Register

	Н	SYNC_B	—Pipe	B Horizontal Sync Register
Register Ty	ype: MMIO			
Address O	<mark>ffset:</mark> 61008h	1-6100Bh		
Project:	All			
Default Val	ue: 000000)00h		
Access:	R/W			
Size (in bit	<mark>s):</mark> 32			
Bit				Description
31:29	Reserved	Project:	All	Format:
28:16	Pipe_B_Hor	izontal_Sync	End	Project: All
	See pipe A d	-	_	
15:13	Reserved	Project:	All	Format:
12:0	Pipe_B_Hor	izontal_Sync	_Start	Project: All
	See pipe A d	escription		

3.2.4 VTOTAL_B—Pipe B Vertical Total Register

	VTOTAL_B—Pipe B Vertical	Total Register
Register Ty Address O Project: Default Val Access: Size (in bits	ifset: 6100Ch-6100Fh All ue: 00000000h R/W	
Bit	Description	
31:29	Reserved Project: All	Format:
28:16	Pipe_B_Vertical_Total_Display_Lines See pipe A description	Project: All
15:12	Reserved Project: All	Format:
11:0	Pipe_B_Vertical_Active_Display_Lines See pipe A description	Project: All



3.2.5 VBLANK_B—Pipe B Vertical Blank Register

	V	BLANK	_B—Pi	ipe B Vertical Blank Register	
Register Ty Address O Project: Default Val Access: Size (in bit	ffset: 61010 All lue: 00000 R/W)h-61013h			
Bit				Description	
31:29	Reserved	Project:	All	Format:	
28:16	Pipe_B_Ve See pipe A	rtical_Blank_ description	End	Project:	All
15:13	Reserved	Project:	All	Format:	
12:0	Pipe_B_Ve See pipe A	rtical_Blank_ description	Start	Project:	All

3.2.6 VSYNC_B—Pipe B Vertical Sync Register

	VSYNC_B-	Pipe B Vertical Sync Register	
Register Ty Address O Project: Default Val Access: Size (in bits	ffset: 61014h-61017h All ue: 00000000h R/W		
Bit		Description	
31:29	Reserved Project: All	Format:	
28:16	Pipe_B_Vertical_Sync_End See pipe A description	Project:	All
15:13	Reserved Project: All	Format:	
12:0	Pipe_B_Vertical_Sync_Start See pipe A description	Project:	All



3.2.7 PIPEBSRC—Pipe B Source Image Size

	PIP	EBSRC-	–Pipe	B Source Image	e Size	
Register Type:		MMIO				
Address Offset:		6101Ch-610	01Fh			
Project:		All				
Default Value:		00000000h				
Access:	R/W					
Size (in bits):	32					
Double Buffer Up	date Point:	Start of vert	ical blank			
Bit				Description		
31:28 Rese	erved Pro	ject: All			Format:	MBZ
27:16 Pipe	_B_Horizonta	I_Source_Ima	age_Size		Project:	All
See	pipe A descript	ion	_		-	
15:12 Rese	erved Pro	ject: All			Format:	MBZ
11:0 Pipe	_B_Vertical_S	ource_Image	_Size		Project:	All
See	pipe A descript	ion				

3.2.8 VSYNCSHIFT_B— Vertical Sync Shift Register

	VSYNCSHIFT_B-V	ertical Sync Shift Register
Register Ty Address O Project: Default Val Access: Size (in bits	fset: 61028h-6102Bh All ue: 00000000h R/W	
Bit		Description
31:13	Reserved Project: All	Format:
12:0	Pipe_B_Second_Field_Vertical_Sync_S See pipe A description	Shift Project: All



3.3 Pipe B M/N Values

3.3.1 PipeBDataM1— Pipe B Data M value 1

		PipeB	DataM	11— Pipe B Data M value 1	
Register T	<mark>ype:</mark> M	MIO			
Address Offset:		030h-61033h			
Project:		I			
Default Value:)000000h			
Access:	R	W			
Size (in bit	s): 32	2			
See pipe A	descript	ion			
Bit				Description	
31	Reserv	ed Project:	All	Format:	MBZ
30:25	TU_Siz	e		Project:	All
	See pip	e A description			
24	Reserv	ed Project:	All	Format:	MBZ
23:0	Pipe_B	_Data_M_value		Project:	All
	See pip	e A description			

3.3.2 PipeBDataN1— Pipe B Data N value 1

Register 1	Type:	MMIO					
Address (61034h-	61037h				
Project:		All					
Default Va	alue:	000000	0h				
Access:		R/W					
Size (in bi	its):	32					
See pipe /	A descri	otion					
					Description		
Bit			Duciest	All		Format:	MBZ
31:24	Reser	ved	Project:				
			Project: N_value			Project:	All



3.3.3 PipeBDataM2— Pipe B Data M value 2

		PipeB	DataM2—	- Pipe B Data M	value 2	
Register T Address O Project: Default Va Access: Size (in bit	offset: 61038 All All Iue: 000000 R/W R/W	h-6103Bh 000h				
-	description					
Bit				Description		
31	Reserved	Project:	All		Format:	MBZ
30:25	TU_Size See pipe A c	lescription			Project:	All
24	Reserved	Project:	All		Format:	MBZ
23:0	Pipe_B_Dat See pipe A c				Project:	All

3.3.4 PipeBDataN2— Pipe B Data N value 2

			PipeB	DataN2-	– Pipe B	Data N valu	e 2	
Register T	ype:	MMIO						
Address Offset:		6103CI	n-6103Fh					
Project:		All						
Default Va	lue:	000000	000h					
Access:		R/W						
Size (in bit	ts):	32						
See pipe A	A desci	ription						
Bit					Descri	ption		
31:24	Rese	erved	Project:	All			Format:	MBZ
23:0	Pipe	_B_Data	a_N_value				Project:	All
	See	pipe A d	escription					



3.3.5 PipeBDPLinkM1— Pipe B Link M value 1

			PipeBDF	PLinkM1–	– Pipe B Link M	I value 1		
Register Ty	ype:	MMIO						
Address O	ffset:	61040	n-61043h					
Project:		All						
Default Value:		00000	000h					
Access:		R/W						
Size (in bit	s):	32						
See pipe A	descri	ption						
Bit					Description			
31:24	Rese	erved	Project:	All		Format:	MBZ	
23:0	Pipe	_B_Lin	k_M_value			Project:	All	
	See	pipe A c	lescription					

3.3.6 PipeBDPLinkN1— Pipe B Link N value 1

			PipeBDI	PLink	1— Pipe B Lin	k N value 1			
Register Ty	vpe:	MMIO							
Address Of	fset:	61044h	-61047h						
Project:		All							
Default Value:		000000	00h						
Access:		R/W							
Size (in bits	s):	32							
See pipe A	descri	iption.							
Bit					Description				
31:24	Rese	rved	Project:	All		Format:	MBZ		
23:0	Pipe_	B_Link	_N_value			Project:	All		
	See p	oipe A de	escription						



3.3.7 PipeBDPLinkM2— Pipe B Link M value 2

			PipeBD	PLinkM	2— P	ipe B Link	M value 2	
Register Ty Address Of Project:			-6104Bh					
Default Val Access:		0000	00h					
<mark>Size (in bit</mark> See pipe A	-							
Bit						Description		
31:24	Reserve	d	Project:	All			Format:	MBZ
23:0	-		_M_value escription				Project:	All

3.3.8 PipeBDPLinkN2— Pipe B Link N value 2

			PipeBDI	PLinkN2	2— Pipe B Link	N value 2		
Register T	ype:	MMIO						
Address C	offset:	6104CI	n-6104Fh					
Project:		All						
Default Value:		000000)00h					
Access:		R/W						
Size (in bit	ts):	32						
See pipe A	desci	iption						
Bit	1				Description			
31:24	Rese	erved	Project:	All		Format:	MBZ	
23:0	Pipe	_B_Link	_N_value			Project:	All	
	See	oipe A d	escription					



3.4 Embedded DP CTL & Aux Channel

3.4.1 DP_A—DisplayPort A Control Register

		DP_A—	DisplayPort A Control Register	
Register 7 Address (Project: Default Va Access: Bize (in bi	Dffset: 6400 All alue: 0000 R/W	00h 00018h		
Bit			Description	
		lue: 0	II b in its lowest power state. Port enable takes place on the Vbl	lank after
	DisplayPo	If DisplayPort A a rt A the FDI PLL i	and another port have been both enabled, then prior to disabli nust be enabled in either FDI_TXA_CTL or FDI_TXB_CTL, the ed, and then the FDI PLL can be restored to its previous state	ng nen
	[DevSNB] DisplayPo	If DisplayPort A a rt A the FDI PLL i	and another port have been both enabled, then prior to disabli nust be enabled in either FDI_TXA_CTL or FDI_TXB_CTL, th	ng nen
	[DevSNB] DisplayPol DisplayPol	If DisplayPort A a rt A the FDI PLL r rt A can be disabl	and another port have been both enabled, then prior to disabli nust be enabled in either FDI_TXA_CTL or FDI_TXB_CTL, th ed, and then the FDI PLL can be restored to its previous state	ng nen e.
	[DevSNB] DisplayPol DisplayPol	If DisplayPort A a rt A the FDI PLL r rt A can be disabl	and another port have been both enabled, then prior to disabli must be enabled in either FDI_TXA_CTL or FDI_TXB_CTL, th ed, and then the FDI PLL can be restored to its previous state Description	ng nen e. Project
30	[DevSNB] DisplayPor DisplayPor Value 0b 1b Pipe_Sele Project: Default Va This bit de	If DisplayPort A a rt A the FDI PLL r rt A can be disable Disable Enable Ect A lue: 0 termines from wh	and another port have been both enabled, then prior to disabli must be enabled in either FDI_TXA_CTL or FDI_TXB_CTL, the ed, and then the FDI PLL can be restored to its previous state Description Disable and tristates the Display Port A interface Enable. This bit enables the Display Port A interface.	ng hen e. Project All All
30	[DevSNB] DisplayPor DisplayPor Value 0b 1b Pipe_Sele Project: Default Va This bit de	If DisplayPort A a rt A the FDI PLL r rt A can be disable Disable Enable ect A lue: 0	and another port have been both enabled, then prior to disabli must be enabled in either FDI_TXA_CTL or FDI_TXB_CTL, the ed, and then the FDI PLL can be restored to its previous state Description Disable and tristates the Display Port A interface Enable. This bit enables the Display Port A interface.	ng hen e. Project All All
30	[DevSNB] DisplayPor DisplayPor Ob 1b Pipe_Sele Project: Default Va This bit de on the Vbla	If DisplayPort A a rt A the FDI PLL r rt A can be disable Disable Enable Enable Ct A lue: 0 termines from wh ank after being w	And another port have been both enabled, then prior to disabli must be enabled in either FDI_TXA_CTL or FDI_TXB_CTL, the ed, and then the FDI PLL can be restored to its previous state Description Disable and tristates the Display Port A interface Enable. This bit enables the Display Port A interface. Ill b b ich display pipe the source data will originate. Pipe selection ritten	ng hen e. Project All All takes place



9:28	Link_trai	ning_patte	ern_enable)		
	Project:		All			
	Default V	alue:	0b			
				alization as defined in the DisplayPort specificatior I prior to sending training patterns.	n. Please no	ote that
	When ena must be o	abling the p disabled, th	oort, it must en re-enab	t be turned on with pattern 1 enabled. When retrain led with pattern 1 enabled.	ning a link, t	he port
	Value	Name	Descript	tion		Project
	00b	P1	Pattern	1 enabled: Repetition of D10.2 characters		All
	01b	P2	D10.2, D pattern n initializat	2 enabled: Repetition of K28.5, D11.6, K28.5, D11 010.2, D10.2, D10.2, D10.2. Please note that the e nust complete before another pattern is sent. Scra ion and disparity init commence at the end of the la of pattern 2.	entire Imbling	All
	10b	Idle		tern enabled: Transmit BS followed by VB-ID with Stream_flag set to 1, five times		
	11b	None	Link not	in training: Send normal pixels		
7:22	-	swing_Pre	e-emphasis	s_level_set_SNB		<u> </u>
7:22	Project: Default V	alue:	e-emphasis DevSNI 000000	s_level_set_SNB B		
7:22	Project: Default V	alue:	e-emphasis DevSNI 000000	s_level_set_SNB B b	Project	<u></u>
7:22	Project: Default V These bit	alue: s are used	e-emphasis DevSNI 000000 for setting	s_level_set_SNB B b link voltage swing and pre-emphasis.	Project DevSNB	
7:22	Project: Default V These bit Value	alue: s are used	e-emphasis DevSNI 000000 for setting	s_level_set_SNB B b link voltage swing and pre-emphasis. Description		<u> </u>
7:22	Project: Default V These bit Value	alue: s are used Name 0 400mv 600mv	e-emphasis DevSNI 000000 for setting 0db/ 0db	s_level_set_SNB B b link voltage swing and pre-emphasis. Description 400mv 0dB / 600mv 0dB		<u> </u>
7:22	Project: Default V These bit Value	alue: s are used Name 0 400mv 600mv	e-emphasis DevSNI 000000 for setting	s_level_set_SNB B b link voltage swing and pre-emphasis. Description 400mv 0dB / 600mv 0dB Actual 0.5v transition and 0.5v non-transition	DevSNB	
7:22	Project: Default V These bit Value 0000001	alue: s are used Name b 400mv 600mv b 400mv	e-emphasis DevSNI 000000 for setting 0db/ 0db	s_level_set_SNB B b link voltage swing and pre-emphasis. Description 400mv 0dB / 600mv 0dB Actual 0.5v transition and 0.5v non-transition 400mv 3.5dB Actual 0.5v transition and 0.33v non-transition	DevSNB DevSNB	
7:22	Project: Default V These bit Value	alue: s are used Name b 400mv 600mv b 400mv	e-emphasis DevSNI 000000 for setting 	s_level_set_SNB B b link voltage swing and pre-emphasis. Description 400mv 0dB / 600mv 0dB Actual 0.5v transition and 0.5v non-transition 400mv 3.5dB Actual 0.5v transition and 0.33v non-transition 400mv 6dB / 600mv 6dB	DevSNB	
7:22	Project: Default V These bit 0000000 0000001 1110100	alue: s are used Name 0 400mv 600mv 0 400mv 0 400mv 600mv	e-emphasis DevSNI 000000 for setting 0db/ 0db 3.5db	s_level_set_SNB B b link voltage swing and pre-emphasis. Description 400mv 0dB / 600mv 0dB Actual 0.5v transition and 0.5v non-transition 400mv 3.5dB Actual 0.5v transition and 0.33v non-transition 400mv 6dB / 600mv 6dB Actual 1v transition and 0.5v non-transition	DevSNB DevSNB DevSNB	
7:22	Project: Default V These bit Value 0000001	alue: s are used Name 0 400mv 600mv 0 400mv 0 400mv 600mv 0 600mv	e-emphasis DevSNI 000000 for setting 	 s_level_set_SNB b link voltage swing and pre-emphasis. Description 400mv 0dB / 600mv 0dB Actual 0.5v transition and 0.5v non-transition 400mv 3.5dB Actual 0.5v transition and 0.33v non-transition 400mv 6dB / 600mv 6dB Actual 1v transition and 0.5v non-transition 600mv 3.5dB / 800mv 3.5dB 	DevSNB DevSNB	
7:22	Project: Default V These bit 0000000 00000010 1110010 1110010	alue: s are used Name b 400mv 600mv b 400mv c 400mv 600mv 600mv 600mv	2-emphasis DevSNI 000000 for setting 	s_level_set_SNB B b link voltage swing and pre-emphasis. Description 400mv 0dB / 600mv 0dB Actual 0.5v transition and 0.5v non-transition 400mv 3.5dB Actual 0.5v transition and 0.33v non-transition 400mv 6dB / 600mv 6dB Actual 1v transition and 0.5v non-transition 600mv 3.5dB / 800mv 3.5dB Actual 1v transition and 0.66v non-transition	DevSNB DevSNB DevSNB DevSNB	
7:22	Project: Default V These bit 0000000 0000001 1110100	alue: s are used Name b 400mv 600mv b 400mv c 400mv 600mv 600mv 600mv	2-emphasis DevSNI 000000 for setting 	 s_level_set_SNB b link voltage swing and pre-emphasis. Description 400mv 0dB / 600mv 0dB Actual 0.5v transition and 0.5v non-transition 400mv 3.5dB Actual 0.5v transition and 0.33v non-transition 400mv 6dB / 600mv 6dB Actual 1v transition and 0.5v non-transition 600mv 3.5dB / 800mv 3.5dB 	DevSNB DevSNB DevSNB	

-1



1:19	Port_Wic	th_Selection	on	
	Project:		All	
	Default V	alue:	0b	
		elects the ne a part of mo	umber of lanes to be enabled on the DisplayP de set.	ort link. Port width change must be
	Value	Name	Description	Project
	000b	x1	x1 Mode (Default)	All
	001b	x2	x2 Mode.	All
	010b	Reserved	Reserved	All
	011b	x4	x4 Mode.	All
	1XXb	Reserved	Reserved	All
			All	
		elects enha	Ob nced framing. s enabled. Updates when the port is disable	ed then re-enabled
	This bit s	elects enha	0b nced framing.	ed then re-enabled Project
	This bit s Locked o	elects enha	0b nced framing. s enabled. Updates when the port is disable	
	This bit s Locked o Value	elects enha	0b nced framing. enabled. Updates when the port is disable Description	Project
7:16	This bit s Locked o Value Ob 1b	A selects enha once port is Name Disable Enable Frequency	0b nced framing. enabled. Updates when the port is disable Description Enhanced framing disabled Enhanced framing enabled.	Project All
7:16	This bit s Locked o Value 0b 1b DP_PLL Project:	A selects enha once port is Name Disable Enable Frequency	0b nced framing. enabled. Updates when the port is disable Description Enhanced framing disabled Enhanced framing enabled. r_Select All	Project All
7:16	This bit s Locked c Ob 1b DP_PLL Project: Default V	A conce port is concept to the concept c	0b nced framing. enabled. Updates when the port is disable Description Enhanced framing disabled Enhanced framing enabled. Select All 0b	Project All All
7:16	This bit s Locked c Value Ob 1b DP_PLL Project: Default V Value	A selects enhance port is a solution of the selects enhance port is a solution of the select	Ob nced framing. senabled. Updates when the port is disable Description Enhanced framing disabled Enhanced framing enabled. r_Select All Ob	Project All All Project Project



5	Port_rev	ersal							
	Project:		All						
	Default V	alue:	0b						
	reversal c	loes not affec	AUX channel la	ne 0 mapped to lane 3, lane 1 mapped to ne mapping. s when the port is disabled then re-ena					
	Value	Name	Description		Project				
	0b	Normal	Port not reve	rsed	All				
	1b Reversed		Port reversed	Port reversed					
14	DP_PLL_enable								
	Project: All								
	Default V	alue:	0b						
				te that software must wait for the PLL wa	rmup cycle before				
	-	-	h bit 31 of this re	egister. nabling DP PLL while a pipe is enabled g					
			-	nk on the enabled pipe going to FDI					
		Program DP F							
	Value	- T T	Description		Project				
	0b		OP PLL not enak	bled	All				
	00		OP PLL enabled		All				
			OP PLL enabled						
	1b	Enable							
3:8	1b Reserved		: All	Forma	at: MBZ				
3:8 7		d Project	: All	Forma	nt: MBZ				
	Reserved	d Project		Forma					
7	Reserved	d Project d d Project							
7 6	Reserved Reserved Reserved	d Project d Project d Project							
7 6 5	Reserved Reserved Reserved Reserved	d Project d Project d Project							
7 6 5	Reserved Reserved Reserved Reserved Sync_Po	d Project d Project d Project	: All						
7 6 5	Reserved Reserved Reserved Reserved Sync_Po Project: Default Va	d Project d Project d Project d Iarity alue:	All All 11b	Forma					
7 6 5	Reserved Reserved Reserved Reserved Sync_Po Project: Default Va	d Project d Project d Project d Iarity alue:	All All 11b	Forma VS and HS are active high					
7 6 5	Reserved Reserved Reserved Reserved Sync_Po Project: Default Va Indicates	d Project d Project d Project d I larity alue: the polarity o	All All 11b Hsync and Vsyr	Forma VS and HS are active high nc to be transmitted in MSA.	ıt: MBZ				
7 6 5	Reserved Reserved Reserved Reserved Sync_Po Project: Default Value	d Project d Project d Project d larity alue: the polarity o Name	All All 11b Hsync and Vsyr Descr VS an	Forma VS and HS are active high nc to be transmitted in MSA. iption	it: MBZ				
7 6 5	Reserved Reserved Reserved Reserved Sync_Po Project: Default Value 00b	d Project d Project d Project d I larity alue: the polarity of Name Low	All All 11b Hsync and Vsyr Descr VS an S_High VS is a	Forma VS and HS are active high nc to be transmitted in MSA. iption d HS are active low (inverted)	it: MBZ				



2	Digital_D)isplay_A_Det	ected			
	Project:		All			
	Default Value:		0b			
	Read-only bit indicating whether a digital display was detected during initialization. This bit is qualified with the Embedded DisplayPort A capability fuse.					
				Project		
	Value 0b	-mbedded Disp Name No Detect	Description Digital display not detected during initialization	Project		

3.4.2 DPA_AUX_CH_CTL—Display Port A AUX Channel Control

	DPA_AUX_CH_CTL—Display Port A AUX Channel Control
Register Ty Address Of Project: Default Val Access: Size (in bits	ffset: 64010h-64013h All ue: 00050000h R/W Special
Bit	Description
31	Send/Busy Project: All Format: Setting this bit to a one initiates the transaction, when read this bit will be a 1 until the transmission completes. The transaction is completed when the response is received or when a timeout occurs. Do not write a 1 again until transaction completes. Writes of 0 will be ignored. Programming Notes Do not change any fields while Busy bit 31 is asserted.
30	Done Project: All Access: R/W Clear A sticky bit that indicates the transaction has completed. SW must write a 1 to this bit to clear the event
29	Interrupt_on_DoneProject:AllFormat:Enable an interrupt in the hotplug status register when the transaction completes or times out.
28	Time_out_errorProject:AllAccess:R/W ClearA sticky bit that indicates the transaction has timed out.SW must write a 1 to this bit to clear the event.



27:26	Time_ou	t_timer_va	lue						
	Project:		All						
	Default V		0b						
	The time	count depe	ends on the 2X	bit clock divider (bits 10:0) being programmed for 2M	1Hz.				
	Value	Name	Description		Project				
	00b	400us	400us		All				
	01b	600us	600us		All				
	10b	800us	800us		All				
	11b	1600us	1600us		All				
25	Receive_	error	Project:	All					
	Access:		R/W Clea	ar					
	Default V	alue:	0b						
		A sticky bit that indicates that the data received was corrupted, not in multiples of a full byte, or more than 20 bytes. SW must write a 1 to this bit to clear the event.							
24:20	Message	_Size	Project:	All Format:					
	This field is used to indicate the total number bytes to transmit (including the header). It also in the number of bytes received in a transaction (including the header). This field is valid only whe done bit is set and timeout or receive error has not occurred. Sync/Stop are not part of the mes or the message size. Reads of this field will give the response message size.								
	The read value will not be valid while Busy bit 31 is asserted.								
				-					
19:16		sizes of 0 o	not be valid whi or >20 are not a Project:	-					
19:16	Message	sizes of 0 o	or >20 are not a	allowed.					
19:16	Message Precharg Default V	sizes of 0 o je_Time alue:	or >20 are not a Project: 0101b	allowed.					
19:16	Message Precharg Default V Used to c	sizes of 0 o je_Time alue: determine tl	or >20 are not a Project: 0101b he precharge ti	allowed. All 10 us precharge	mmed for				
19:16	Message Precharg Default V Used to o The value	sizes of 0 o je_Time alue: determine the e is the num	or >20 are not a Project: 0101b he precharge ti	allowed. All 10 us precharge ime for the Aux Channel drivers.	mmed for				
19:16	Message Precharg Default V Used to o The value 2MHz). Example	sizes of 0 o je_Time alue: determine the e is the num :	or >20 are not a Project: 0101b he precharge ti	All All 10 us precharge ime for the Aux Channel drivers. econds times 2 (assuming 2X bit clock divider progra	mmed for				
19:16	Message Precharg Default V Used to o The value 2MHz). Example	sizes of 0 o je_Time alue: determine the e is the num : precharge,	or >20 are not a Project: 0101b he precharge ti nber of microse	All All 10 us precharge ime for the Aux Channel drivers. econds times 2 (assuming 2X bit clock divider progra	mmed for				
	Message Precharg Default V Used to o The value 2MHz). Example For 10us Reserved	sizes of 0 o je_Time alue: determine the e is the num : precharge,	or >20 are not a Project: 0101b he precharge ti nber of microse program 5 (10	All All 10 us precharge ime for the Aux Channel drivers. econds times 2 (assuming 2X bit clock divider progra	mmed for				
15:11	Message Precharg Default V Used to o The value 2MHz). Example For 10us Reserved 2X_Bit_O	sizes of 0 o je_Time alue: determine the e is the num : precharge, d Clock_divice	or >20 are not a Project: 0101b he precharge ti nber of microse program 5 (10	All All 10 us precharge ime for the Aux Channel drivers. econds times 2 (assuming 2X bit clock divider progra	mmed for				
15:11	Message Precharg Default V Used to o The value 2MHz). Example For 10us Reserved Used to o This value	sizes of 0 o je_Time alue: determine the e is the num precharge, d Clock_divic determine the e divides the	or >20 are not a Project: 0101b he precharge ti nber of microse program 5 (10 der Project: he 2X bit clock	All All 10 us precharge ime for the Aux Channel drivers. econds times 2 (assuming 2X bit clock divider progra bus/2us). : All the Aux Channel logic runs on. requency down to 2X bit clock rate. The 2X bit clock					
15:11	Message Precharg Default V Used to o The value 2MHz). Example For 10us Reserved Used to o This value	sizes of 0 o je_Time alue: determine the e is the num precharge, d Clock_divic determine the e divides the 5us). The	or >20 are not a Project: 0101b he precharge ti nber of microse program 5 (10 der Project: he 2X bit clock fr he input clock fr	All All 10 us precharge ime for the Aux Channel drivers. econds times 2 (assuming 2X bit clock divider progra bus/2us). : All the Aux Channel logic runs on. requency down to 2X bit clock rate. The 2X bit clock					



3.4.3 DPA_AUX_CH_DATA1—Display Port A AUX Data Register 1

C	PA_	_AUX_CH_DATA1—Display Port A AUX Data Register 1
Register T	ype:	MMIO
Address O	ffset:	64014h-64017h
Project:		All
Default Va	lue:	0000000h
Access:		R/W Special
Size (in bit	ts):	32
The read v	alue w	vill not be valid while Busy bit 31 is asserted.
Bit		Description
31:0	AUX	_CH_DATA1 Project: All Format:
		first DWord of the message. The MSbyte is transmitted first. Reads will give the response data transaction complete.

3.4.4 DPA_AUX_CH_DATA2—Display Port A AUX Data Register 2

		AUX_CH_	DATA2-	-usp	iay Port A	AUX Data Register 2
Register 1	Гуре:	MMIO				
Address (Offset:	64018h-6401Bh	า			
Project:		All				
Default Value:		00000000h				
Access:		R/W Special				
Size (in bi	its):	32				
The read	value w	vill not be valid v	while Busy b	oit 31 is as	sserted.	
Bit					Description	
31:0	AUX	_CH_DATA2	Project:	All	Format:	
					byte is transmitte data after transad	d first. Only used if the message size is



3.4.5 DPA_AUX_CH_DATA3—Display Port A AUX Data Register 3

D	PA_	AUX_CH_DATA3—Display Port A AUX Data Register 3								
Register Ty	/pe:	MMIO								
Address Of	ffset:	6401Ch-6401Fh								
Project:		All								
Default Value:		0000000h								
Access:		R/W Special								
Size (in bits	s):	32								
The read va	alue w	vill not be valid while Busy bit 31 is asserted.								
Bit		Description								
31:0	AUX	CH_DATA3 Project: All Format:								
		hird DWord of the message. The MSbyte is transmitted first. Only used if the message size is er than 8. Reads will give the response data after transaction complete.								

3.4.6 DPA_AUX_CH_DATA4—Display Port A AUX Data Register 4

D	PA_	AUX_CH_DATA4—Display Port A AUX Data Register 4
Register Ty	ype:	MMIO
Address O	ffset:	64020h-64023h
Project:		All
Default Value:		0000000h
Access:		R/W Special
Size (in bit	s):	32
The read va	alue w	ill not be valid while Busy bit 31 is asserted.
Bit		Description
31:0	AUX	CH_DATA4 Project: All Format:
		ourth DWord of the message. The MSbyte is transmitted first. Only used if the message size is er than 12. Reads will give the response data after transaction complete.

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3.4.7 DPA_AUX_CH_DATA5—Display Port A AUX Data Register 5

Register T	ype:	MMIO
Address C	Offset:	64024h-64027h
Project:		All
Default Value:		0000000h
Access:		R/W Special
Size (in bi	ts):	32
The read v	alue w	ill not be valid while Busy bit 31 is asserted.
Bit		Description
Bit 31:0	AUX	_CH_DATA5 Project: All Format:

3.5 Panel Fitter Control Registers

3.5.1 **PF_WIN_POS—Panel Fitter Window Position**

Register T	ype:		MMIO						
Address C	offset:		68070h-68073h						
Project:			All						
Default Va	lue:		0000000h						
Access:			R/W	R/W					
Size (in bits):			32	32					
Double Buffer Update Point:			Start of vertical blank after armed						
Double Bu	iffer Armed By:		Write	e to PFA_WIN_	SZ				
Bit					Description				
31:29	Reserved	Pro	ject:	All		Format:	MBZ		
28:16	XPOS	Pro	ject:	All					
	The X coordir	nate (in	pixel	s) of the upper l	eft most pixel of the pa	anel fitted display win	dow.		
15:12	Reserved	Pro	ject:	All		Format:	MBZ		
11:0	YPOS	Pro	ject:	All					
	The Y coordir	nate (in	lines)) of the upper le	ft most pixel of the par	nel fitter display winde	ow.		
				rlaced modes.	· ·				



Register T	ype:	MM	0					
Address O	ffset:	688	70h-68873h					
Project:			All					
Default Value:			0000000h					
Access:			R/W					
Size (in bits):			32					
Double Bu	ffer Update Point	: Star	t of vertical blank after armed					
Double Bu	ffer Armed By:	Writ	e to PFB_WIN_SZ					
Bit			Descript	ion				
31:29	Reserved	Project:	All	Format:	MBZ			
28:16	XPOS	Project:	All					
	See PFA descrip	-						
15:12	Reserved	Project:	All	Format:	MBZ			
11:0	YPOS	Project:	All					
	See PFA descrip	otion						

3.5.2 **PF_WIN_SZ**—Panel Fitter Window Size

Coordinates are determined with a value of (0,0) being the upper left corner of the display device (rotation does not affect this). Writes to the window size arm PF registers for the pipe.

Register Type:			IIO						
Address C	Offset:	680	68074h-68077h						
Project:		All	All						
Default Value:			0000000h						
Access:		R/V	R/W						
Size (in bits):									
Double Bu	uffer Update Po	oint: Sta	rt of vertion	cal blank					
Bit				Description					
31:29	Reserved	Project:	All		Format:	MBZ			
28:16	XSIZE	Project:	All						
	The horizonta	al size in pix	els of the	desired panel fitted window.					
15:12	Reserved	Project:	All		Format:	MBZ			
11:0	YSIZE	Project:	All						
	The vertical s	size in nixels	of the de	sired panel fitted window. LSB n	nust be zero for in	terlaced modes			



	P	FB_WIN	SZ—Par	nel Fitter B Windo	w Size					
Register T	ype:	MMI	MMIO							
Address O	ffset:	6887	68874h							
Project:		All	All							
Default Va	lue:	0000	0000000h							
Access:		R/W	R/W							
Size (in bit	s):	32								
Double Bu	ffer Update Po	oint: Start	of vertical blan	K						
Bit				Description						
31:29	Reserved	Project:	All		Format:	MBZ				
28:16	XSIZE	Project:	All							
	See PFA des	•								
15:12	Reserved	Project:	All		Format:	MBZ				
11:0	YSIZE	Project:	All							
	See PFA des	scription								

3.5.3 **PF_CTRL_1—Panel Fitter Control 1**

Register Type:	MMIO			
Address Offset:	68080h-68083h			
Project:	All			
Default Value:	0000000h			
Access:	R/W			
Size (in bits):	32			
Double Buffer Update Poir	Start of vertical blank after armed			
Double Buffer Armed By:	Write to PFA_WIN_SZ			
	wnscaling (pipe source size is larger than panel fitter window size) the maximum e reduced by the downscale amount.			
Bit	Description			

Enable_Pipe_Scaler							
Project:	A	11					
Default Value:		b					
Value	Name	Description	Project				
0b	Disable	Data bypasses the scaler	All				
1b	Enable	The scaler is enabled	All				
Reserved							
Reserved							
Reserved							
	Project: Default Va Ob 1b Reserved Reserved	Project: A Default Value: 0 Value Name 0b Disable 1b Enable Reserved	Project: All Default Value: 0b Value Name Description 0b Disable Data bypasses the scaler 1b Enable The scaler is enabled Reserved				



27	VADAPT Puts the a		Proj cal filter		All daptive mode, intended for use in interlace output mode	es only.			
	Value	Name	Desc	ription	1	Project			
	0b	Disable Adaptive fil			ering disabled	All			
	1b	Enable Adaptive fil			ering enabled	All			
26:25	VADAPT_MODE Project: All								
	Puts the a	Puts the adaptive vertical filter into adaptive mode, intended for use in interlace output mode							
	Value	Name			Description	Project			
	00b	Least Adap	tive		Least Adaptive (Recommended)	All			
	01b	Moderately	Adaptiv	/e	Moderately Adaptive	All			
	10b	Reserved			Reserved	All			
	11b	11b Most Adaptive Most Adaptive							
	FILTER_SELECT Project: All Filter coefficient selection Image: Selection								
	Value				ription	Project			
	00b	Programme			rammed Coefficients (Recommended)	All			
	01b	Hardcoded		Hardcoded Coefficients for Medium 3x3 Filtering		All			
	10b	Edge Enha			dcoded Coefficients for Edge Enhancing 3x3 Filtering				
	11b	Edge Softe	n	Hard	dcoded Coefficients for Edge Softening 3x3 Filtering				
22	CHR_PREF Project: All Chroma Pre-filter enable. Image: Chroma Pre-filter enable.								
	Value	Name	Desc	ription	I	Project			
	0b	Disable	Pre-fi	lter dis	abled	All			
	1b	Enable Pre-filter enabled							
21	Reserved	ł							
20	Reserve	d							



		PFB	CTRL 1	—Panel Fitter B Control	1	
Double Bu When usir supported Bit	offset: lue: s): ffer Update ffer Armed ng panel fitt pixel rate v	M 6 A 00 R 33 Point: S By: W ter downsca will be reduc	IMIO 8880h-6888 II 0000000h /W 2 tart of vertica /rite to PFB_ ling (pipe s	al blank after armed		e maximum
31	Enable_P Project: Default Va	ipe_Scaler	All Ob			
1	Value	Name	D	escription	Pi	oject
	0b	Disable	D	ata bypasses the scaler	AI	I
	1b	Enable	Т	The scaler is enabled		I
30	Reserved					
29	Reserved					
28	Reserved	l				
27	VADAPT Puts the a	daptive vertic	Project: al filter into a	All adaptive mode, intended for use in interlace	ce output modes	only.
	Value	Name	Descriptio	n		Project
	0b	Disable	Adaptive fi	Itering disabled		All
	1b	Enable	Adaptive fi	Itering enabled		All
26:25	VADAPT_ Puts the a	_	Project: al filter into a	All adaptive mode, intended for use in interla	ce output modes	only.
	Value	Name		Description		Project
	00b	Least Adapt	ive	Least Adaptive (Recommended)		All
	01b	Moderately	Adaptive	Moderately Adaptive		All
	10b	Reserved		Reserved		All
	11b	Most Adapti	ve	Most Adaptive		All



24:23	FILTER_SELECT Project: All Filter coefficient selection							
	Value	Name		Description	Project			
	00b	Programme	d	Programmed Coefficients (Recommended)	All			
	01b	Hardcoded Med Edge Enhance Edge Soften		Hardcoded Coefficients for Medium 3x3 Filtering	All			
	10b			Hardcoded Coefficients for Edge Enhancing 3x3 Filtering	All			
	11b			Hardcoded Coefficients for Edge Softening 3x3 Filtering	All			
	CHR PR	FF	Pro	liect: ΔII				
22	CHR_PR Chroma F	EF Pre-filter enab		ject: All				
22			le.	ject: All cription	Project			
22	Chroma F	Pre-filter enab	le. Desc		Project All			
22	Chroma F	Pre-filter enab	le. Desc Pre-f	cription	-			
22	Chroma F Value 0b	Pre-filter enab Name Disable Enable	le. Desc Pre-f	cription ilter disabled	All			
	Chroma P Value 0b 1b	Pre-filter enab Name Disable Enable	le. Desc Pre-f	cription ilter disabled	All			

3.5.4 Panel Fitter Coefficient Registers

Coefficients for the panel fitter filters are stored in sign-exponent-mantissa format. The number of mantissa bit varies based on the filter. Two filter coefficients are stored in each dword, the tables below show the data packing in each of the words. Unused bits are considered reserved and should be written zero. The default value of all coefficient registers is 00000000h. Coefficients greater than 1.0 are only allowed in the center tap of the filter.

For RGB modes the Luma and Chroma filter coeffs are programmed with the same values.

Project:	All								
Bit		Description							
15	Sign_bit Project: All								
	Value	Name		Description	Project				
	0b	Positive		Positive	All				
	1b	Negative		Negative	All				
14	Reserved	Project:	All	Format:	MBZ				



3:12	Exponent_bits							
	Project:	All	I					
	The meaning of the exponent bits varies for center tap or non-center tap coefficients.							
	Value	Name	Description	Project				
	00b	2 or 0.125	Center taps: 2 or mantissa is b.bbbbbb	All				
			Non-center taps: 0.125 or mantissa is 0.000bbbbbbb					
	01b	1	1 or mantissa is 0.bbbbbbbb	All				
	10b	0.5	0.5 or mantissa is 0.0bbbbbbbb	All				
	11b	0.25	0.25 or mantissa is 0.00bbbbbbbb	All				
	others	Reserved	Reserved	All				
11:3	Mantissa Project: All							
	Size of the mantissa varies based on the filter, but the MSB of the mantissa is always bit 11.							
	Center tap coefficients use all 9 bits of mantissa.							
	Non-center tap coefficients use only the upper 7 bits of mantissa and the lower 2 bits are ignored.							
2:0	Reserved	Project:	All Forr	nat: MBZ				

3.6 Panel Fitter Horizontal Coefficients

Coefficients are packed in the horizontal coefficient registers as follows (with the letter representing the tap and the number representing the coefficient set):

Address	bits [31:16]	bits[15:0]
68x00	B0	A0
68x04	D0	C0
68x08	F0	E0
68x0C	A1	G0
68x10	C1	B1

etc....



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3.6.1 **PF_HFILTL_COEF—Panel Fitter Horizontal Luma/Red** Coefficients

PFA_HFILTL_COEF—Panel Fitter A Horizontal Luma/Red Coefficients									
Register Type: MMIO									
Address Of	fset: 681	00h-681EFh							
Project:	All								
Default Value	Default Value: 0000000h								
Access:	R/V	V							
Size (in bits	Size (in bits): 60x32								
17 phases of	17 phases of 7 taps require 60 dwords								
Center coef	ficient is	1.2.9							
Other coefficients are 1.2.7									
DWord	DWord Bit Description								
059	31:16	Coefficient2	Project:	All	Format:	Panel Fitter Coefficient Definition			
	15:0	Coefficient1	Project:	All	Format:	Panel Fitter Coefficient Definition			

PFB_HFILTL_COEF—Panel Fitter B Horizontal Luma/Red Coefficients

Register Ty	<mark>/pe:</mark> M	MIO				
Address Of	<mark>ffset:</mark> 68	3900h-689EFh				
Project:	A	I				
Default Val	ue: 00)000000h				
Access:	R	W				
Size (in bits	<mark>s):</mark> 60)x32				
17 phases	of 7 taps	require 60 dwords				
Center coe Other coeff						
DWord	Bit				Description	
059	31:16	Coefficient2	Project:	All	Format:	Panel Fitter Coefficient Definition
	15:0	Coefficient1	Project:	All	Format:	Panel Fitter Coefficient Definition



3.6.2 PF_HFILTC_COEF—Panel Fitter Horizontal Chroma/Green and Blue Coefficients

PFA_HFILTC_COEF—Panel Fitter A Horizontal Chroma/Green and Blue Coefficients

Register Ty	<mark>ype:</mark> M	IMIO						
Address O	ffset: 6	8200h-682EFh						
Project:	A	ll						
Default Val	ue: 0	000000h						
Access:	R	/W						
Size (in bit	<mark>s):</mark> 60	0x32						
17 phases of 7 taps require 60 dwords								
Center coe	fficient is	s 1.2.9						
Other coeff	ficients a	ire 1.2.7						
DWord	Bit				Description			
059	31:16	Coefficient2	Project:	All	Format:	Panel Fitter Coefficient Definition		
	15:0	Coefficient1	Project:	All	Format:	Panel Fitter Coefficient Definition		
	1							

PFB HFILTC COEF—Panel Fitter B Horizontal Chroma/Green and Blue Coefficients Register Type: MMIO Address Offset: 68A00h-68AEFh Project: All **Default Value:** 0000000h Access: R/W Size (in bits): 60x32 17 phases of 7 taps require 60 dwords Center coefficient is 1.2.9 Other coefficients are 1.2.7 **DWord** Bit **Description** 0..59 31:16 Coefficient2 Project: All Format: Panel Fitter Coefficient Definition

All

Format:

Project:

15:0

Coefficient1

Panel Fitter Coefficient Definition



3.7 Panel Fitter Vertical Coefficients

Coefficients are packed in the vertical coefficient registers as follows (with the letter representing the tap and the number representing the coefficient set). When the vertical filter is in 3 line mode the three taps used are A, C & E, B & C must be programmed to zero in three line mode.

Address	bits [31:16]	bits[15:0]	
68x00	B0	A0	
68x04	D0	C0	
68x08	A1	E0	
68x0C	C1	B1	
68x10	E1	D1	

etc....

3.7.1 **PF_VFILTL_COEF**—Panel Fitter Vertical Luma/Red Coefficients

Register Type:	MMIO					
Address Offset:	68300h-683	3ABh				
Project: All						
Default Value:	00000000h					
Access:	R/W					
Size (in bits): 43x32						
Center coefficier Other coefficient						
DWord B	it				Description	
042 31:	16 Coeff	icient2	Project:	All	Format:	Panel Fitter Coefficient Definition



PFB_VFILTL	_COEF-	-Panel Fitter	r B Vertica	I Luma/Red	Coefficients
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Register Type:	MMIO
Address Offset:	MMIO 68B00h-68BABh
Project:	All
Default Value:	0000000h
Access:	R/W
Size (in bits):	43x32

17 phases of 5 taps require 43 dwords

Center coefficient is 1.2.9

Other coefficients are 1.2.7

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DWord	Bit	Description				
042	31:16	Coefficient2	Project:	All	Format:	Panel Fitter Coefficient Definition
	15:0	Coefficient1	Project:	All	Format:	Panel Fitter Coefficient Definition

3.7.2 PF_VFILTC_COEF—Panel Fitter Vertical Chroma/Green and Blue Coefficients

PFA_	VFILT	C_COEF—I		er A V		Chroma/Green and Blue
Register Ty	v <mark>pe:</mark> N	1MIO				
Address Of	fset: 6	8400h-684ABh				
Project:	A	.11				
Default Val	ue: 0	0000000h				
Access:	R	2/W				
Size (in bits	s): 4	3x32				
17 phases o	of 5 taps	s require 43 dword	ds			
Center coef	ficient i	s 1.2.9				
Other coeffi	icients a	are 1.2.7				
DWord	Bit				Description	
042	31:16	Coefficient2	Project:	All	Format:	Panel Fitter Coefficient Definition
	15:0	Coefficient1	Project:	All	Format:	Panel Fitter Coefficient Definition



PFB_VF	ILTC	COEF—Pa	anel Fitte Coef			Chroma/Green and Blue
Register Type:	MM	10				
Address Offset	68C	00h-68CABh				
Project:	All					
Default Value:	000	00000h				
Access:	R/W	/				
Size (in bits):	43x	32				
17 phases of 5	taps r	equire 43 dwords				
Center coefficie	ent is 1	1.2.9				
Other coefficier	its are	9 1.2.7				
DWord I	Bit				Description	
042 3	1:16	Coefficient2	Project:	All	Format:	Panel Fitter Coefficient Definition
1	5:0	Coefficient1	Project:	All	Format:	Panel Fitter Coefficient Definition



4. Plane Controls (70000h–7FFFFh)

4.1 Display Pipeline A

4.1.1 PIPEA_DSL—Pipe A Display Scan Line

	PIPEA_DSL—Pipe A Display Scan Line
Register Type:	MMIO
Address Offset:	70000h-70003h
Project:	All
Default Value:	0000000h
Access:	Read Only
Size (in bits):	32
This register ena	bles the read back of the display pipe vertical "line counter". The value increments at the

This register enables the read back of the display pipe vertical "line counter". The value increments at the leading edge of HSYNC and can be safely read any time. The value resets to line zero at the first active line of the display. In interlaced display timings, the scan line counter provides the current line in the field. One field will have a total number of lines that is one greater than the other field. Content locked display will adjust the total number of lines displayed.

Bit	Description					
31	Current	Field				
	Project:		All			
	Default Value: 0					
	Provides	read back	of the current field being displayed on disp	splay pipe A.		
	Value	Name	Description		Project	
	0b	Odd	First field (odd field)		All	
	1b	Even	Second field (even field)		All	
30:13	Reserve	d Pro	ect: All	Format:		
12:0	Line_Co	unter_for_	Display	Projec	t: All	
			of the display pipe A vertical line counter be used by software to synchronize with		rent	



4.1.2 **PIPEA_SLC**—Pipe A Display Scan Line Count Range Compare

PI	PEA_SI	LC—Pipe /	A Display So	an Line Count	Range C	ompa	re		
Register T	ype: MM	10							
Address C		04h-70007h							
Project:	All	000001							
Default Va Access:	R/W	00000h /							
Size (in bi									
		ed. The waid for	scan line is prograi	mmed through DE_LOAI	D SEL 0x4F10	0.			
esult of thi The value p	s compariso programmed	n is used to gene should be desire	rate interrupts and i d value – 1, so for I	ith the display line value render responses. Ine 0, the value program ne total number of lines of	med is VTOTA				
Bit				Description					
31	Inclusive	/Exclusive							
	Project: DevILK								
	Default Value: 0b								
	Value Name Description						Project		
	0b Exclusive Exclusive: outside of the range						All		
	1b Inclusive Inclusive: within the range								
30:29	Reserved	I	Project:	DevILK		Format:	MBZ		
28:16	Start_Sca	an_Line_Numbe	r Project:	DevILK		Format:			
	Range:								
	This field specifies the starting scan line number of the Scan Line Window.								
	Scan line	0 is the first line	of the display frame						
15:13	Reserved	I	Project:	DevILK		Format:	MBZ		
12:0	End_Sca	n_Line_Number	Project:	DevILK		Format:			
	Range: 0Vertical Total								
	This field specifies the ending scan line number of the Scan Line Window.								
	Scan line	0 is the first line	of the display frame						
31:13	Reserved	l	Project:	DevSNB		Format:	MBZ		
12:0	Scan_Lin	e_Number							
	Project:	I	Pre-DevSNB:D2						
	Range	(0Vertical Total						
	This field	specifies the scar	n line number on wh	ich to generate scan line	e interrupt and	render res	sponse.		



4.1.3	PIPEACONF -	-Pipe A	Configuration	Register
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	Ρ	IPEACONF-	-Pipe A Configuration Register		
	vpe: ifset: ue:	MMIO 70008h-70 All 000000001 R/W 32	000Bh		
Bit			Description		
31	on this pipe. have been c Synchroniza	All e: 0b bit to the value of on Changing it to a ze disabled. Turning the ation pulses to the dis	e, turns on pipe A. This must be done before any planes ro should only be done when all planes that are assigned pipe enable bit off disables the timing generator in this p splay are not maintained if the timing generator is disable id values before this bit is enabled.	to this pipe pipe.	
	Value	Name	Description Pr		
	0b	Disable	Disable	All	
	1b	Enable	Enable	All	
30		cates the actual state	e of the pipe. Since there can be some delay between diang off, this bit indicates the true current state of the pipe.	sabling the	
	Value	Name	Description	Project	
	0b	Disable	Disable State	All	
	1b	Enable	Enable State	All	
29	Reserved	Project: All			
28:27	Reserved				
26	Reserved	Project: Dev	/SNB		



25:24	Pipe_A_I	Palette/Gamn	na_Unit_Mode						
	Project: All								
	Default Value: 0b								
	Registers		mode the pipe gamma correction logic works in. See the Display Pale on on the different palette/gamma modes. Other gamma units such as / this bit.						
	Value	Name	Description	Project					
	00b	8 bit	8-bit Legacy Palette Mode	All					
	01b	10 bt	10-bit Precision Palette Mode	All					
	10b	12 bit	12-bit Interpolated Gamma Mode	All					
	11b	Reserved	Reserved	All					
23:21									
	Interlace	d Mode							
		d_Mode	All						
	Project: Default V	_	All Ob						
	Project: Default V These bit	alue: s are used for		y if the					
	Project: Default V These bit pipe is off	alue: s are used for f, or in the ver	0b software control of interlaced behavior. They are updated immediatel	y if the					
	Project: Default V These bit pipe is off	alue: s are used for f, or in the ver	0b software control of interlaced behavior. They are updated immediatel tical blank after programming if pipe is enabled.	-					
	Project: Default V These bit pipe is off Note: VG	alue: s are used for f, or in the vert A display mo	0b software control of interlaced behavior. They are updated immediatel tical blank after programming if pipe is enabled. odes do not work while in interlaced fetch modes	-					
	Project: Default V These bit pipe is off Note: VG Value	alue: s are used for f, or in the vert A display mo Name	Ob software control of interlaced behavior. They are updated immediatel tical blank after programming if pipe is enabled. odes do not work while in interlaced fetch modes Description	Project					
	Project: Default V These bit pipe is off Note: VG Value 000b	alue: s are used for f, or in the ver A display mo Name PF-PD	Ob software control of interlaced behavior. They are updated immediatel tical blank after programming if pipe is enabled. odes do not work while in interlaced fetch modes Description Progressive Fetch / Progressive display Progressive Fetch / Interlaced display (HDMI) Requires panel	Project					
	Project: Default V These bit pipe is off Note: VG Value 000b 001b	alue: s are used for f, or in the vert A display mo Name PF-PD PF-ID	Ob software control of interlaced behavior. They are updated immediatel tical blank after programming if pipe is enabled. odes do not work while in interlaced fetch modes Description Progressive Fetch / Progressive display Progressive Fetch / Interlaced display (HDMI) Requires panel fitting to be enabled	Project All All					
	Project: Default V These bit pipe is off Note: VG Value 000b 001b 010b	alue: s are used for f, or in the vert a A display mo Name PF-PD PF-ID Reserved	Ob software control of interlaced behavior. They are updated immediatel tical blank after programming if pipe is enabled. odes do not work while in interlaced fetch modes Description Progressive Fetch / Progressive display Progressive Fetch / Interlaced display (HDMI) Requires panel fitting to be enabled Reserved Interlaced Fetch / Interlaced display (programmable sync,	Project All All All					
	Project: Default V These bit pipe is off Note: VG Value 000b 001b 010b 011b	alue: s are used for f, or in the vert A display mo Name PF-PD PF-ID Reserved IF-ID	Ob software control of interlaced behavior. They are updated immediatel tical blank after programming if pipe is enabled. odes do not work while in interlaced fetch modes Description Progressive Fetch / Progressive display Progressive Fetch / Interlaced display (HDMI) Requires panel fitting to be enabled Reserved Interlaced Fetch / Interlaced display (programmable sync, normal interlaced) Interlaced embedded panel with interlaced fetch (pixel	Project All All All All All					



1

		PIPEA		F—Pipe A Configuration Register				
20	Display_	Power_M	ode_Sw	itch				
	Project: All							
	Default Value: 0b							
	power sa must be If LVDS o enabled	ivings moo set to 00 in clockgating	le on the n order fo g is disab 0 cleared	to set the power saving progressive mode. The pipe enters or ex- vblank after this bit is written. Please note that bits 17:16 of this r or this bit to take effect. bled (bits 14, 30 set to '1' in 0xC2020), then clockgating must be te to '0') when toggling Display Power Mode Switch followed by wai again.	egister mporarily			
	Value	Name		Description	Project			
	0b	Progres	sive	Pipe is in progressive mode	All			
	1b	Power s	ave	Pipe is in power savings progressive mode	All			
19:18	Project: Default V This field	selects th	D 0 le vertica	DevSNB 0b I blank line on which MSA is sent. It is intended for use with ember port sDRRS. The sDRRS timing switch shall occur on same line as				
	Value	Name	Descri	Description				
	00b	Line1	MSA ar	MSA and sDRRS timing switch occur within the first line of vertical blank				
	01b	Line2	MSA a blank	MSA and sDRRS timing switch occur within the second line of vertical				
	10b	Line3	MSA ar blank	MSA and sDRRS timing switch occur within the third line of vertical blank				
	11b	Line4	MSA and sDRRS timing switch occur within the fourth line of vertical blank					
19:18	Reserve	d Proje	ect: De	evILK Format: MBZ				
17:16	Reserve	d Pro	oject:	All Format: MBZ				
15:14	Project: Default V These ar	e informat	A 0 ive bits s	ul b set by software to indicate this pipe is being rotated. Software show d software rotation cases. Hardware rotation is <u>not</u> enabled throug				
	Value	Name	Desc	ription	Project			
	00b	None	No ro	otation on this pipe	All			
	01b	90	90° r	otation on this pipe	All			
				90° rotation on this pipe				
	10b	180	180°	180° rotation on this pipe				

г



13	Color_Ra	ange_Select						
	Project:		All					
	Default Value: 0b							
	This bit is	used to sele	ect the color range of outputs.					
	Value	Name	Description	Project				
	0b	Full	Apply full 0-2 ⁿ - 1 color range to the output	All				
	1b	CE	Apply CE color range to the output	All				
12:11	Pipe_out	 put_color_ອ	space_select					
	Project: All							
	Default Va	Default Value: 0b						
		ne ports of th what is seled	e pipe output color space. Plane data formats and CSC need to be pr ted here.	ogrammed				
	Value Name Description							
	00b RGB		RGB	All				
	01b YUV 601		YUV 601	All				
	10b	YUV 709	YUV 709	All				
	11b	Reserved	Reserved	All				
10:9	Reserved	l Projec	ct: DevSNB					
8	Reserved	l Projec	ct: All Format: MBZ					
7:5	Bits_Per_	Color						
	Project:		All					
	Default Va	alue:	Ob					
7:5	This field selects the number of bits per color sent to a receiver device connected to this pipe. Color format takes place on the Vblank after being written. Color format change can be done independent of a pixel clock change.							
	a pixel clo Software	ock change. should enab	ble dithering in the pipe/port if selecting a pixel color depth higher or low of the frame buffer.	ver than				
	a pixel clo Software	ock change. should enab		ver than Project				
	a pixel clo Software the pixel	ock change. should enab color depth c	of the frame buffer.					
	a pixel clo Software the pixel o Value	ock change. should enab color depth c Name	Description	Project				
	a pixel clo Software the pixel o Value 000b	ock change. should enab color depth c Name 8 bits	Description 8 bits per color	Project All				
	a pixel clo Software the pixel o Value 000b 001b	ock change. should enab color depth c Name 8 bits 10 bits	Description 8 bits per color 10 bits per color	Project All All				



		PIPEAC	CONF—Pipe A Configurati	on Register				
4	Dithering	_enable						
	Project: All							
	Default Value: 0b							
	This bit enables dithering							
	Value	Name	Description		Project			
	0b	Disable	Dithering disabled		All			
	1b	Enable	Dithering enabled		All			
	Default V These bit	alue: s select dith	0b ering type.					
	Value	Name	Description		Project			
	00b	Spatial	Spatial only		All			
	01b	ST1	Spatio-Temporal 1		All			
	10b	ST2	Spatio-Temporal 2 (testmode)		All			
	11b	Temporal	Temporal only (testmode)		All			
1	Reserve	d						
0	Reserve	d Proje	ct: All	Format:	MBZ			

(intel)

4.2 Display Pipeline A Counters and Timestamps

4.2.1 **PIPEA_FRMCOUNT—Pipe A Frame Counter**

Register T	ype:	MMIO				
Address O	ffset:	70040h-70043h				
Project:		All				
Default Val	lue:	00000000h				
Access:		Read Only				
Size (in bit	s):	32				
Bit					Description	
31:0 Pip e		_Frame_Counter	Project:	All	Format:	
		des read back of th al blank and rolls o			counter. This counter increments on every start of 32 frames	

4.2.2 PIPEA_FLIPCOUNT—Pipe A Flip Counter

PIPEA_FLIPCOUNT—Pipe A Flip Counter			
Register T Address O Project: Default Va Access: Size (in bit	offset: lue:	MMIO 70044h-70047h All 0000000h Read Only 32	
Bit		Description	
31:0	Provi of the	Flip_CounterProject:AllFormat:des read back of the display pipe flip counter.This counter increments on each flip of the surfacprimary plane on this pipe.This includes command streamer asynchronous and synchronousnd any MMIO writes to the primary plane surface address.It rolls over back to 0 after 2^32 flips.	



4.2.3 **PIPEA_FRMTIMESTAMP—Pipe A Frame Time Stamp**

Register T	vpe:	MMIO						
• •		70048h-7004Bh						
Project:		All						
Default Value:		0000000h						
Access:		Read Only						
Size (in bit	s):	32						
Bit		Des	cription					
31:0	Pipe	_Frame_Time_Stamp	Proje	ect:	All	Format:		
		ides read back of the display pipe frame time s of vertical blank. The TIMESTAMP register has						

4.2.4 PIPEA_FLIPTIMESTAMP—Pipe A Flip Time Stamp

		PIPEA_FLIPTIMESTAMP—F	Pipe A Flip Time Stamp			
Register Ty	ype:	MMIO				
Address O	ffset:	7004Ch-7004Fh				
Project:		All				
Default Value:		0000000h				
Access:		Read Only				
Size (in bit	s):	32				
Bit		Des	cription			
31:0	Pipe	_Flip_Time_Stamp	Project: All Format:			
	Provides read back of the display pipe flip time stamp. The time stamp value is sampled on each flip of the surface of the primary plane on this pipe. This includes command streamer asynchronous and synchronous flips and any MMIO writes to the primary plane surface address. The TIMESTAMP register has information on the time stamp value.					

4.3 Display Timestamp

This register provides an elapsed real-time value that can be used as a timestamp for GPU events over short periods of time.

The register counts at a constant frequency by adjusting the increment amount according to the actual core display clock frequency. SW therefore does not need to know the reference clock frequency.



4.3.1 **TIMESTAMP_HI**—Time Stamp High Value

		TIMEST	AMP_H	l I— Tir	ne Stamp High Value
Register Ty	/pe:	MMIO			
Address Of	ffset:	70070h-70073h			
Project:		All			
Default Val	ue:	00000000h			
Access:		R/W Clear			
Size (in bit	s):	32			
Bit					Description
31:0	TIME	STAMP_High	Project:	All	Format:
	regis	ters when flips occur ter value will reset if a	, and in the	Pipe Frai	value in this field is latched in the Pipe Flip TIMESTAMP me TIMESTAMP registers at start of vertical blank. The o it. The register is not reset by a graphics software

4.4 Display Pipeline B

4.4.1 **PIPEB_DSL—Pipe B Display Scan Line**

		PIPEB_D	SL—Pipe B Display Scan Line	
Register T	ype: MMIC	C		
Address O	ffset: 7100	0h-71003h		
Project:	All			
Default Va	lue: 0000	0000h		
Access:	Read	d Only		
Size (in bit	s): 32			
See Pipe A	A description	۱		
Bit			Description	
31	Current_F	ield		
	Project:	AI	1	
	Default Val	ue: Ob)	
	Provides r	ead back of the cu	urrent field being displayed on display pipe B.	
	Value	Name	Description	Project
	0b	First	First field (odd field)	All
	1b	Second	Second field (even field)	All
			Project: All Format: M	



	PIPEB_DSL—Pipe B Display Scan Line							
12:0	Line_Counter_for_Display See pipe A description.	Project: All Format:						

4.4.2 **PIPEB_SLC—Pipe B Display Scan Line Count Range Compare**

PII	PEB_	_SLC-	-Pipe	B Display S	can Line	Count	Range (Compar	е		
Register Type: MMIO											
Address O	ffset:	71004h-7 ⁻	1 007 h								
Project:		All									
Default Val	ue:	00000000	h								
Access:		R/W									
Size (in bit	s):	32									
See Pipe A	descri	iption									
Bit					Description						
31:13	Reser	rved		Project:	DevSNB			Format:	MBZ		
12:0	Scan	_Line_Nu	mber								
	Projec	ct:		Pre-DevSNB:D2							
	Range	е		0Vertical Total							
	See p	ipe A deso	cription								
12:0	Reser	rved	Project:	DevSNB:D2+			Format:	MBZ			



4.4.3 **PIPEBCONF**—Pipe B Configuration Register

	Р	IPEBCONF-	-Pipe B Configuration Regist	er			
Register T Address C Project:		MMIO 71008h-7 1	100Bh				
Default Va Access:		00000000 R/W					
Size (in bi Double Bu	ts): uffer Update F	32 Point: Start of ve	rtical blank OR pipe disabled				
Bit			Description				
31	Pipe_B_En	able					
	Project:	All					
	Default Valu	ue: Ob					
	on this pipe have been Synchroniza	. Changing it to a ze disabled. Turning th ation pulses to the di	he, turns on pipe B. This must be done before an ero should only be done when all planes that are e pipe enable bit off disables the timing generato splay are not maintained if the timing generator i lid values before this bit is enabled.	assigned to this pipe r in this pipe.			
	Value	Name	Description	Project			
	0b	Disable	Disable	All			
	1b	Enable	Enable	All			
30	Pipe_State Project: Default Valu This bit indi pipe and the	All ue: Ob cates the actual state	e of the pipe. Since there can be some delay be ng off, this bit indicates the true current state of	tween disabling the the pipe.			
	Value	Name	Description	Project			
			-	-			
	0b	Disable	Disable	All			
	0b 1b	Disable Enable	Disable Enable	All All			
29		2.000.00		All			
29 28:27	1b	Enable	Enable	All			



25:24	Pipe_B_Palette/Gamma_Unit_Mode								
	Project: All								
	Default Value: 0b								
	These bits select which mode the pipe gamma correction logic works in. See the Display Pale Registers for information on the different palette/gamma modes. Other gamma units such as in sprite are unaffected by this bit.								
	Value	Name	Description	Project					
	00b	8 bit	8-bit Legacy Palette Mode	All					
	01b	10 bit	10-bit Precision Palette Mode	All					
	10b	12 bit	12-bit Interpolated Gamma Mode	All					
	11b	Reserved	Reserved						
23:21	Interlaced Mode								
20.21	Interlace	d_Mode							
20.21	Interlace Project:	d_Mode	All						
20.21			All Ob						
20.21	Project: Default V These bit	alue: s are used for		y if the					
20.21	Project: Default V These bit pipe is off	alue: s are used for f, or in the ver	0b software control of interlaced behavior. They are updated immediatel	y if the					
20.21	Project: Default V These bit pipe is off	alue: s are used for f, or in the ver	0b software control of interlaced behavior. They are updated immediatel tical blank after programming if pipe is enabled.	y if the Project					
20.21	Project: Default V These bit pipe is off Note: VG	alue: s are used for f, or in the ver A display mo	0b software control of interlaced behavior. They are updated immediatel tical blank after programming if pipe is enabled. odes do not work while in interlaced fetch modes	-					
20.21	Project: Default V These bit pipe is off Note: VG Value	alue: s are used for f, or in the ver A display mo Name	0b software control of interlaced behavior. They are updated immediatel tical blank after programming if pipe is enabled. odes do not work while in interlaced fetch modes Description	Project					
20.21	Project: Default V These bit pipe is off Note: VG Value 000b	alue: s are used for f, or in the ver A display mo Name PF-PD	Ob software control of interlaced behavior. They are updated immediately tical blank after programming if pipe is enabled. odes do not work while in interlaced fetch modes Description Progressive Fetch / Progressive display Progressive Fetch / Interlaced display (HDMI) Requires panel	Project All					
20.21	Project: Default V These bit pipe is off Note: VG Value 000b 001b	alue: s are used for f, or in the ver a display mo Name PF-PD PF-ID	Ob software control of interlaced behavior. They are updated immediately tical blank after programming if pipe is enabled. odes do not work while in interlaced fetch modes Description Progressive Fetch / Progressive display Progressive Fetch / Interlaced display (HDMI) Requires panel fitting to be enabled	Project All All					
20.21	Project: Default V These bit pipe is off Note: VG Value 000b 001b 010b	alue: s are used for f, or in the ver a A display mo Name PF-PD PF-ID Reserved	Ob Software control of interlaced behavior. They are updated immediately tical blank after programming if pipe is enabled. Odes do not work while in interlaced fetch modes Description Progressive Fetch / Progressive display Progressive Fetch / Interlaced display (HDMI) Requires panel fitting to be enabled Reserved Interlaced Fetch / Interlaced display (programmable sync,	Project All All All					
20.21	Project: Default V These bit pipe is off Note: VG Value 000b 001b 010b 011b	alue: s are used for f, or in the ver A display mo Name PF-PD PF-ID Reserved IF-ID	Ob software control of interlaced behavior. They are updated immediately tical blank after programming if pipe is enabled. odes do not work while in interlaced fetch modes Description Progressive Fetch / Progressive display Progressive Fetch / Interlaced display (HDMI) Requires panel fitting to be enabled Reserved Interlaced Fetch / Interlaced display (programmable sync, normal interlaced) Interlaced embedded panel with interlaced fetch (pixel	Project All All All All					



	-	PIPE	SCON	F—Pipe B Configuration Register						
20	Display_Power_Mode_Switch									
	Project: All									
	Default Value: 0b									
	power sa	This bit is used for software to set the power saving progressive mode. The pipe enters or exits the power savings mode on the vblank after this bit is written. Please note that bits 17:16 of this register must be set to 00 in order for this bit to take effect.								
	enabled		0 cleared	oled (bits 14, 30 set to '1' in 0xC2020), then clockgating must be ter I to '0') when toggling Display Power Mode Switch followed by wait again.						
	Value	Name		Description	Project					
	0b	Progres	ssive	Pipe is in progressive mode	All					
	1b	Power Save		Pipe is in power savings progressive mode						
19:18		ning_Del	-							
	Project: DevSNB									
		Default Value: 00b								
	This field selects the vertical blank line on which MSA is sent. It is intended for use with embedded DisplayPort panels that support sDRRS. The sDRRS timing switch shall occur on same line as the MSA.									
	Value	Name	Descri	ption	Project					
	00b	Line1	MSA ar	nd sDRRS timing switch occur within the first line of vertical blank	All					
	01b	Line2	MSA a blank	MSA and sDRRS timing switch occur within the second line of vertical blank						
	10b	Line3	MSA a blank	MSA and sDRRS timing switch occur within the third line of vertical blank						
	Diank 11b Line4 MSA and sDRRS timing switch occur within the fourth line of vertical blank									



17:16	Refresh	Rate Pow	ver_Savings_Mode_Association					
	Project: All							
	Default Value: 00b							
	00, bits 2 directly is that supp	3:21 of this not allowe ort corresp	w refresh rates are switched on pipe B. When they are set to anything ot register must be programmed to 000. Switching between 01 and 10 set d. Software is responsible for enabling this mode only for integrated displ onding mode. The refresh rate hardware control register has additional so refresh rate switching.	ings ay panels				
	Value	Name	Description	Project				
	00b	None	No dynamic refresh rate change enabled. Software control through bits 23:21 only	All				
	01b	PTP	Progressive-to-progressive refresh rate change enabled. For the CPU and PCH, link and data M and N 1 values are used for high power settings, M and N 2 values for low power settings. For the PCH, pixel clock FPB0 values are used for high power settings, FPB1 values for low power settings.	All				
	10b	PTI	Progressive-to-interlaced refresh rate change enabled. Pixel clock value does not change in this case. However, data and link M values in the CPU and PCH (as appropriate) are divided by 2 (shifted right by 1 bit). If scaling is enabled, the planes will fetch progressive data which will be interlaced by the panel fitter. If scaling is disabled, the planes will fetch interlaced data, reducing the amount of data fetched	All				
	11b	Reserv ed	Reserved	All				
15:14	Display_Rotation_Info							
	Project:		All					
	Default V	alue:	Ob					
			ve bits set by software to indicate this pipe is being rotated. Software sho vare and software rotation cases. Hardware rotation is <u>not</u> enabled throu					
	Value	Name	Description	Project				
	00b	None	No rotation on this pipe	All				
	01b	90	90° rotation on this pipe	All				
	10b	180	180° rotation on this pipe	All				
	11b	270	270° rotation on this pipe	All				



13	Color_Ra	ange_Select						
	Project: All							
	Default Value: 0b							
	This bit is used to select the color range of outputs.							
	Value	Name	Description	Project				
	Ob Full Apply full 0-2 ⁿ - 1 color range to the output							
	1b	CE	Apply CE color range to the output	All				
12:11	Pipe_out	put_color_s	space_select					
	Project:		All					
	Default V	alue:	Ob					
		ne ports of th what is seled	e pipe output color space. Plane data formats and CSC need to be ted here.	e programmed				
	Value	Name	Description	Project				
	00b	RGB	RGB	All				
	01b	YUV 601	YUV 601	All				
	10b	YUV 709	YUV 709	All				
	11b	Reserved	Reserved	All				
10:9	Reserved	d Project:	DevSNB					
8	Reserved	d Proje	ct: All Format: N	BZ				
7:5	Bits_Per	Color						
	Project: All							
	Default V		Ob					
	This field selects the number of bits per color sent to a receiver device connected to this pipe. Color format takes place on the Vblank after being written. Color format change can be done independent of a pixel clock change.							
	Software should enable dithering in the pipe/port if selecting a pixel color depth higher or lower than the pixel color depth of the frame buffer.							
	For furthe to "DP Fr	er details on equency Pro	Display Port fixed frequency programming to accommodate these f gramming" in DPLL section of Bspec.	ormats refer				
	Value	Name	Description	Project				
	000b	8 bits	8 bits per color	All				
	001b	10 bits	10 bits per color	All				
	010b	6 bits	6 bits per color	All				
	011b	12 bits	12 bits per color	All				



		PIPEB	CONF—Pipe B Config	uration Register								
4	Dithering	Dithering_enable										
	Project:		All									
	Default Value: 0b											
	This bit e	nables dithe	ering									
	Value	Name	Description		Project							
	0b	Disable	Dithering disabled		All							
	1b	Enable	Dithering enabled		All							
3:2	Dithering	_type										
	Project:		All									
	Default V	alue:	Ob									
	Security:		Test									
	These bit	s select dith	nering type.									
	Value	Name	Description		Project							
	00b	Spatial	Spatial only		All							
	01b	ST1	Spatio-Temporal 1		All							
1	Reserve	d										
0	Reserved	d Proje	ect: All	Format:	MBZ							

4.5 **Display Pipeline B Counters and Timestamps**

4.5.1 **PIPEB_FRMCOUNT—Pipe B Frame Counter**

	PIPEB_FRMCOUNT—Pipe B Frame Counter								
Register Ty Address O Project: Default Val Access: Size (in bit	ffset: lue:	MMIO 71040h-71043h All 00000000h Read Only 32							
Bit					Description				
31:0		_Frame_Counter Pipe A description	Project:	All	Format:				



4.5.2 **PIPEB_FLIPCOUNT—Pipe B Flip Counter**

	PIPEB_FLIPCOUNT—Pipe B Flip Counter							
Register Ty Address O Project: Default Val Access: Size (in bits	ffset: ue:	MMIO 71044h-71047h All 00000000h Read Only 32						
Bit					Description			
31:0	-	_ Flip_Counter Pipe A description	Project:	All	Format:			

4.5.3 PIPEB_FRMTIMESTAMP—Pipe B Frame Time Stamp

	Ρ	IPEB_FRMTIMEST	AMP—Pipe B Frame Time Stamp
Register Type:		MMIO 71048h-7104Bh All 00000000h Read Only 32	
Bit			Description
31:0	•	_ Frame_Time_Stamp Pipe A description	Project: All Format:

4.5.4 **PIPEB_FLIPTIMESTAMP—Pipe B Flip Time Stamp**

		PIPEB_FLIPTIMESTAMP-	-Ріре В Гіір	D TIME 5	tam	D
Register T	ype:	MMIO				
Address Offset		7104Ch-7104Fh				
Project:		All				
Default Value:		0000000h				
Access:		Read Only				
Size (in bit	s):	32				
Bit		c	Description			
31:0	Pipe	_Flip_Time_Stamp		Project:	All	Format:
	See	Pipe A description				



4.6 Cursor A Plane Control Registers

The CURACNTR active register will be updated on the vertical blank or when pipe is disabled, after the CURABASE or CURAPOPUPBASE trigger register is written, or when cursor A is not yet enabled – thus providing an atomic update of the cursor A control and base address registers.

4.6.1 CURACNTR—Cursor A Control Register

		CUR	ACNTE	R—Cursor A Control	Register	
Register T Address C Project: Default Va Access:	Offset:		MMIO 70080h-70 All 00000000 R/W			
Size (in bi Double Bu Double Bu	uffer Update	By:	32 Start of ve Write to C	ertical blank or pipe disabled or curs URABASE or CURAVGAPOPUPB to pipe A only. For VGA popup	BASE	e select.
Bit				Description		
31:28	Reserved	l Proje	ect: All		Format:	
	Project:		All			
	Default Va This bit sh	nould be tur	0b ned on whe	en using Cursor A as a popup curs ess as a <u>physical</u> address instead o		, hardware
	Default Va This bit sh	nould be tur	0b ned on whe			, hardware
	Default Va This bit sh interprets	nould be tur the cursor l	0b ned on whe	ess as a <u>physical</u> address instead o	of a graphics address.	, hardware
	Default Va This bit sh interprets Value	nould be tur the cursor l	0b ned on whe	ess as a <u>physical</u> address instead o Description	of a graphics address. Project	, hardware
26	Default Va This bit sh interprets Value 0b 1b Cursor_C Project: Default Va This bit or	Name Name Hi-Res VGA Gamma_En alue: hly has an e	0b ned on whe base addre abled All 0b	ess as a <u>physical</u> address instead o Description Cursor A is hi-res	of a graphics address.	
26	Default Va This bit sh interprets Value 0b 1b Cursor_C Project: Default Va This bit or	Name Name Hi-Res VGA Gamma_En alue: hly has an e	0b ned on whe base addre abled All 0b	ess as a <u>physical</u> address instead o Description Cursor A is hi-res Cursor A is popup using the cursor in a non-VGA mo he gamma (palette) unit.	of a graphics address.	
26	Default Va This bit sh interprets Value 0b 1b Cursor_C Project: Default Va This bit or cursor dat	Name Name Hi-Res VGA Gamma_En alue: hly has an e ta will alway	0b ned on whe base addre abled All 0b effect when vs bypass th Descripti	ess as a <u>physical</u> address instead o Description Cursor A is hi-res Cursor A is popup using the cursor in a non-VGA mo he gamma (palette) unit.	of a graphics address. Project All All All	tion, the
26	Default Va This bit sh interprets Value 0b 1b Cursor_C Project: Default Va This bit or cursor dat	Name Name Name NGA NGA NGA Name Name Name	0b ned on whe base addre abled All 0b effect when vs bypass th Descripti Cursor piz	ess as a <u>physical</u> address instead o Description Cursor A is hi-res Cursor A is popup using the cursor in a non-VGA mo he gamma (palette) unit. ion	of a graphics address. Project All All All Ode. In VGA pop-up opera	tion, the



		CUF	RACNTR—Cursor A Control Register					
24	Pipe_Co	lor_Space	e_Conversion_Enable					
	Project:		All					
	Default Value: 0b							
	This bit e registers	nables pip must be se	e color space conversion for the cursor pixel data. CSC mode in the pipe (et to match the format of the cursor pixel data.	CSC				
	Value	Name	Description	Project				
	0b	Bypass	Cursor pixel data bypasses the pipe color space conversion logic	All				
	1b	Pass	Cursor pixel data passes through the pipe color space conversion logic	All				
23:16	Reserved	d Pro	ject: All Format:					
15	180°_Rot	ation						
	Project:		All					
	Default V		0b					
			the cursor to be rotated 180°. Only 32 bits per pixel cursors can be rotated when the cursor format is 2 bits per pixel.	. This				
	Value	Value Name Description						
	0b	None	No rotation	All				
	1b	180	180° Rotation of 32 bit per pixel cursors	All				
14	Trickle F	eed_Ena	ble					
	Project:		DevSNB					
	Default V	alue:	0b					
	Value	Name	Description	Project				
	Ob	Enable	Trickle Feed Enabled - Data requests are sent whenever there is space in the Display Data Buffer	All				
	1b	Disable Trickle Feed Disabled - Data requests are sent in bursts						
13:6	Reserved	d Pro	ject: All Format:					
5	Cursor_	Node_Sel	ect[5]					
	Project:		All					
	Default Value: 0b							
	Cursor Mode Select							
	Cursor N	lode Sele						
	Cursor M Bit 5	Bits 2:0	Mode					
	Bit	Bits	Mode Cursor is disabled. This is the default after reset. When the cursor register value changes from enabled to disabled, the cursor will stop fetching data the following VBLANK event.	er at				
	Bit 5	Bits 2:0	Cursor is disabled. This is the default after reset. When the cursor register value changes from enabled to disabled, the cursor will stop fetching data	at				



	0	010	128 x 128 32bpp AND/INVERT (not available for VGA use)
			See description off 64 x 64 32bpp AND/INVERT format for byte usage
	0	011	256 x 256 32bpp AND/INVERT (not available for VGA use)
			See description off 64 x 64 32bpp AND/INVERT format for byte usage
	0	100	64 x 64 2bpp Indexed 3-color and transparency mode
	0	101	64 x 64 2bpp Indexed AND/XOR 2-plane mode
	0	110	64 x 64 2bpp Indexed 4-color mode
	0	111	 64 x 64 32bpp AND/INVERT (not available for VGA use) For each pixel: Least significant three bytes provides cursor RGB 888 color information Most Significant Byte: All Ones: Opaque, show the cursor color All Zeros: Transparent (color must also equal zero) Other: Invert the underlying display pixel data (ignore the color)
	1	000	Reserved
	1	001	Reserved
	1	010	128 x 128 32bpp ARGB (8:8:8:8 MSB-A:R:G:B) (not available for VGA use)
	1	011	256 x 256 32bpp ARGB (8:8:8:8 MSB-A:R:G:B) (not available for VGA use)
	1	100	 64 x 64 32bpp AND/XOR (not available for VGA use) For each pixel: Least significant three bytes provides cursor RGB 888 color information Most Significant Byte: All Ones: Opaque, show the cursor color All Zeros: Transparent (color must also equal zero) Other: XOR the cursor color with the underlying display pixel data
	1	101	128 x 128 32bpp AND/XOR (not available for VGA use)
		-	See description off 64 x 64 32bpp AND/XOR format for byte usage
	1	110	256 x 256 32bpp AND/XOR (not available for VGA use) See description off 64 x 64 32bpp AND/XOR format for byte usage
	1	111	64 x 64 32bpp ARGB (8:8:8:8 MSB-A:R:G:B) (not available for VGA use)
	I	!	J
3	Reserved	l Pr	oject: All Format:
	Cursor_N Project: Default Va		lect[2:0] All Ob



11:0

Reserved

Project:

All

4.6.2 CURABASE—Cursor A Base Address Register

	CURA	BASE—Cursor A Base Address Register			
Register T	ype:	MMIO			
Address Offset:		70084h-70087h			
Project:		All			
Default Va	lue:	0000000h			
Access:		R/W			
Size (in bit	s):	32			
Double Bu	ffer Update Point:	Start of vertical blank or pipe disabled			
		AN CUIRSON A IS IN THA NI-RAS MORA IN VIGA NONLIN MORA			
CURAVGA	POPUPBASE is u	en cursor A is in the hi-res mode. In VGA popup mode used instead and this register <u>must not be written</u> . This register specifies the which the cursor image data is located. Description			
CURAVGA	POPUPBASE is u	used instead and this register <u>must not be written</u> . This register specifies the which the cursor image data is located. Description			
CURAVGA praphics m Bit	NPOPUPBASE is under the second	used instead and this register <u>must not be written</u> . This register specifies the which the cursor image data is located. Description			
CURAVGA graphics m Bit	NPOPUPBASE is underse at a comparison of the second	Used instead and this register <u>must not be written</u> . This register specifies the which the cursor image data is located. Description Idress[31:12]			
CURAVGA graphics m Bit	POPUPBASE is un nemory address at Cursor_Base_Ad Project: Address: This field specifie:	used instead and this register <u>must not be written.</u> This register specifies the which the cursor image data is located. Description Idress[31:12] All			

Format:



4.6.3 CURAPOS—Cursor A Position Register

	CUF	APOS—Cu	rsor A Positi	on Register		
Register Ty		MMIO				
Address Of		70088h-7008Bh				
Project:		All				
Default Valu	le:	0000000h				
Access:		R/W				
Size (in bits	•	32				
	fer Update Point:		lank or pipe disabled	<u> </u>		
			e cursor. The origin be that the cursor is	of the cursor position assigned.	is always th	ie uppe
Bit			Description			
31	Cursor_Y-Position	_Sign_Bit			Project:	All
	For normal high reso	olution display mod	es, the cursor must h	ecifies the horizontal pos ave at least a single pixe or must be positioned ov	l positioned	over
30:28	Reserved Proj	ect: All		Format:	MBZ	
27:16	Cursor_Y-Position	_Magnitude_Bits			Project:	All
	cursor. The sign bit entire cursor must b	of this value is pro e positioned over t	vided by bit 31of this he active area of the	value that specifies the v register. For use as a V VGA image. Enabling th s the border in what is co	GA Popup, t le border in V	he ∕GA
			ld specifies the vertica e unrotated orientation	al position of the lower rig n	ght corner re	lative
15	Cursor_X-Position	_Sign_Bit			Project:	All
	For normal high reso the active screen. F	olution display mod or use as a VGA P Enabling the borde	es, the cursor must h opup, the entire curso r in VGA (VGA Borde	ecifies the horizontal pos ave at least a single pixe or must be positioned ov r Enable bit in the VGA (el positioned er the active	over area
14:12	Reserved Proj	ect: All		Format:	MBZ	
11:0	Cursor_X-Position	_Magnitude_Bits			Project:	All
	These 12 bits provided by bit			the horizontal position of	-	e sign
			ld specifies the horizo rea in the unrotated o	ntal position of the lower rientation.	right corner	



Size (in bits):

F

4.6.4 CURAVGAPOPUPBASE—Cursor A VGA Popup Base Address Register

CURAVGAPOP	CURAVGAPOPUPBASE—Cursor A VGA Popup Base Address Register				
Register Type:	MMIO				
Address Offset:	7008Ch-7008Fh				
Project:	All				
Default Value:	0000000h				
Access:	R/W				

Double Buffer Update Point:Start of vertical blank or pipe disabledWrites to this register arm CURA registers

32

This register is only used when cursor A is in the VGA popup mode. In hi-res mode CURABASE is used instead and this register <u>must not be written.</u> This register specifies the physical memory address at which the cursor image data is located.

Bit	Description						
31:12	Cursor_VGA_Popup_Base_Address[31:12]						
	Project: All						
	Address: PhysicalAddress[31:12]						
	This field specifies bits 31:12 of the <u>physical</u> address of the base of the cursor for VGA popup mode. The <u>graphics</u> address used for hi-res cursor is in the CURABASE register.						
	The cursor surface address must be 4K byte aligned. The cursor must be in linear memory, it cannot be tiled.						
11:7	Reserved Project: All Format:						
6:0	Cursor_VGA_Popup_Base_Address_MSBs[38:32]						
	Project: All						
	Address: PhysicalAddress[38:32]						
	This field specifies bits 38:32 of the <u>physical</u> address of the base of the cursor for VGA popup mode. See restrictions in Cursor VGA Popup Base Address field.						



4.6.5 CURAPALET—Cursor A Palette registers

Cursor Palette Format								
Project:	All							
Bit				Description				
31:24	Reserved Project	t: All			Format:	MBZ		
23:16	Red_or_Y_Value	Project:	All	Format:				
	These registers specify unsigned for the Y and and bypass the gamma	excess 128	notation	for the UV values.	The data can be pre-			
15:8	Green_or_U_Value	Project:	All	Format:				
7:0	Blue_or_V_Value	Project:	All	Format:				

CURAPALET—Cursor A Palette registers						
Register Type:	MMIO					
Address Offset:	70090h-7009Fh					
Project:	All					
Default Value:	0000000h					
Access:	R/W					
Size (in bits):	4x32					
Double Buffer Update Point:	Start of vertical blank or pipe disabled					

The cursor palette provides color information when using one of the indexed modes. The two-bit index selects one of the four colors or two of the colors when in the AND/XOR cursor mode. The cursor palette provides color information when using one of the indexed modes. The two-bit index selects one of the four colors or two of the colors when in the AND/XOR cursor mode for colors or two of the colors when in the AND/XOR cursor mode.

The table below describes the palette usage for different cursor modes and indexes.

Index	2 color	3color	4color
00	palette 0	palette 0	palette 0
01	palette 1	palette 1	palette 1
10	transparent	transparent	palette 2
11	invert destination	palette 3	palette 3
	(palette 3 all 1s)		

Palette 3 must be programmed with all 1s for invert destination.

DWord	Bit	Description					
0	31:0	CURAPALET0	Project:	All	Format:	Cursor Palette Format	
1	31:0	CURAPALET1	Project:	All	Format:	Cursor Palette Format	



Г

CURAPALET—Cursor A Palette registers								
2	31:0	CURAPALET2	Project:	All	Format:	Cursor Palette Format		
3	31:0	CURAPALET3	Project:	All	Format:	Cursor Palette Format		

4.6.6 CURASURFLIVE—Cursor A Live Surface Base Address

	CU	RASURFLIVE—Cursor A Live	Surface Base Address
Register Ty Address Of Project: Default Val Access: Size (in bits	fset: ue:	MMIO 700ACh-700AFh All 00000000h Read Only 32	
Bit		Descript	ion
31:0		<pre>sor_A_Live_Surface_Base_Address gives the live value of the surface base address as</pre>	Project: All Format: being currently used for the plane.

4.7 Cursor B Plane Control Registers

The CURBCNTR active register will be updated on the vertical blank or when pipe is disabled, after the CURBBASE trigger register is written, or when cursor B is not yet enabled – thus providing an atomic update of the cursor B control and base address registers.



CURBCNTR—Cursor B Control Register Register Type: MMIO Address Offset: 700C0h-700C3h Project: All Default Value: 0000000h

4.7.1 CURBCNTR—Cursor B Control Register

Access:		R/W				
Size (in bit	s):	32				
Double Bu	ffer Update Point:	Start of vertical blank or pipe disabled or cursor disabled, after armed				
Double Bu	ffer Armed By:	Write to CURBBASE				
Cursor B is	Cursor B is connected to pipe B only.					
D		Provident of the second s				

ursor B i								
Bit		Description						
31:27	Reserve	ed Project: All Format: MB2						
26	Cursor_	Gamma_Ena	able					
	Project:		All					
	Default V	alue:	0b					
	Value	Name	Descri	otion			Pro	oject
	0b	Bypass	Cursor	pixel data bypasses gamma corr	rection		All	
	1b	Corrected	Cursor	pixel data is gamma to be correc	cted		All	
25	Reserve	d Proje	ct: All		Fo	ormat:		
24	Pipe_Co	lor Space	Conversio	n Enchla				
			2011461310	n_Enable				
	Project:		All					
	Project: Default V			n_Enable				
	Default V	′alue:	All Ob		data. CSC n	node in th	ne pipe C	SC
	Default V This bit e	alue: nables pipe	All 0b color space	n_Enable e conversion for the cursor pixel he format of the cursor pixel data		node in th	ne pipe C	SC
	Default V This bit e	alue: nables pipe	All 0b color space	e conversion for the cursor pixel ne format of the cursor pixel data		node in th	ne pipe C	
	Default V This bit e registers	′alue: nables pipe must be set	All 0b color space to match th Descripti	e conversion for the cursor pixel ne format of the cursor pixel data	l			
	Default V This bit e registers Value	alue: nables pipe must be set	All Ob color space to match th Descripti Cursor piv	e conversion for the cursor pixel on the format of the cursor pixel data on	space conve	ersion logi	ic	Project
23:16	Default V This bit e registers Value 0b	'alue: nables pipe must be set Name Bypass pass	All Ob color space to match th Descripti Cursor pix	e conversion for the cursor pixel on the format of the cursor pixel data on kel data bypasses the pipe color	space conve color space	ersion logi	ic	Projec All
	Default V This bit e registers Value 0b 1b Reserved	falue: mables pipe must be set Name Bypass pass d Proje	All Ob color space to match th Descripti Cursor pix	e conversion for the cursor pixel on the format of the cursor pixel data on kel data bypasses the pipe color	space conve color space	ersion logi conversio	ic	Projec All
23:16 15	Default V This bit e registers Value 0b 1b Reserved 180°_Ro	falue: mables pipe must be set Name Bypass pass d Proje	All Ob color space to match th Descripti Cursor pix Cursor pix ct: All	e conversion for the cursor pixel on the format of the cursor pixel data on kel data bypasses the pipe color	space conve color space	ersion logi conversio	ic	Projec All
	Default V This bit e registers Value 0b 1b Reserved	falue: mables pipe must be set Name Bypass pass d Proje tation	All Ob color space to match th Descripti Cursor pix	e conversion for the cursor pixel on the format of the cursor pixel data on kel data bypasses the pipe color	space conve color space	ersion logi conversio	ic	Projec All
	Default V This bit e registers Value 0b 1b Reserved 180°_Ro Project: Default V	alue: nables pipe must be set Name Bypass pass pass d Proje tation	All Ob color space to match th Descripti Cursor pix Cursor pix ct: All All Ob	e conversion for the cursor pixel on the format of the cursor pixel data on kel data bypasses the pipe color	space conve color space Fo	ersion logi conversio prmat:	on logic.	Projec All All
	Default V This bit e registers Value 0b 1b Reserved 180°_Ro Project: Default V This mod	 alue: nables pipe must be set Name Bypass pass d Proje tation alue: le causes the 	All Ob color space to match th Descripti Cursor pix Cursor pix ct: All All Ob	e conversion for the cursor pixel one format of the cursor pixel data on kel data bypasses the pipe color kel data passes through the pipe	space conve color space Fo	ersion logi conversio prmat:	on logic.	Project All All
	Default V This bit e registers Value 0b 1b Reserved 180°_Ro Project: Default V This mod	 alue: nables pipe must be set Name Bypass pass d Proje tation alue: le causes the 	All Ob color space to match th Descripti Cursor pix Cursor pix ct: All All Ob	e conversion for the cursor pixel one format of the cursor pixel data on kel data bypasses the pipe color kel data passes through the pipe	space conve color space Fo	ersion logi conversio prmat:	on logic.	Project All All
	Default V This bit e registers Value 0b 1b Reserver 180°_Ro Project: Default V This mod field mus	Yalue: mables pipe must be set Name Bypass pass pass d Proje tation Yalue: le causes the t be zero wh	All Ob color space to match th Descripti Cursor pix Cursor pix ct: All All Ob	e conversion for the cursor pixel one format of the cursor pixel data on kel data bypasses the pipe color kel data passes through the pipe be rotated 180°. Only 32 bits pe for format is 2 bits per pixel.	space conve color space Fo	ersion logi conversio prmat:	rotated.	Projec All All



14	Trickle_	Feed_Enab	le				
	Project:		DevSNB				
	Default V	/alue:	0b				
	Value	Name	Description				Projec
	0b	Enable	Trickle Feed space in the			sent whenever there is	All
	1b	Disable	Trickle Feed	Disabled	- Data requests are	sent in bursts.	All
13:6	Reserve	d Proj	ect: All			Format: MB	Z
5	Cursor I	Mode_Sele Mode Selec in CURACN	•	All Control R	Format: egister Bit 5.		
4:3	Reserve	d Proje	ect: All			Format:	
2:0	Cursor	Mode_Sele	ct Project:	All	Format:		

4.7.2 CURBBASE—Cursor B Base Address Register

	CURBB	ASE—Cursor B Base Address	Registe	r			
Register T	ype:	MMIO					
Address O	ffset:	700C4h-700C7h					
Project:		All					
Default Va	ue:	0000000h					
Access:		R/W					
Size (in bit	s):	32					
Double Bu	ffer Update Point:	Start of vertical blank or pipe disabled					
Writes to thi	s register arm CURB	registers					
This registe	r specifies the graphic	s memory address at which the cursor image data i	s located.				
Bit		Description					
31:12	Cursor_Base_Add	ress[31:12]					
	Project:	All					
	Address:	GraphicsAddress[31:12]					
	This register specifies the graphics address of the cursor. It also acts as a trigger event to force the update of active registers on the next display event.						
	The cursor surface address must be 4K byte aligned. The cursor must be in linear memory, it cannot be tiled. When performing 180° rotation, this address does not change, hardware will internally offset to start from the last pixel of the last line of the cursor.						
11:0	Reserved Pro	ject: All	Format:	MBZ			



4.7.3 CURBPOS—Cursor B Position Register

	CU	RBPOS—Cursor B	Position Register		
Register T	ype:	MMIO			
Address C		700C8h-700CBh			
Project:		All			
Default Va	lue:	0000000h			
Access:		R/W			
Size (in bi	ts):	32			
	Iffer Update Point:	Start of vertical blank or pipe			
		een position of the cursor. Th for the display pipe that the o	e origin of the cursor position i cursor is assigned.	s always th	e uppe
Bit		Desc	ription		
31	Cursor_Y-Positio	n_Sign_Bit		Project:	All
			e that specifies the horizontal posi or must have at least a single pixe		
30:28	Reserved Pro	oject: All	Format:	MBZ	
27:16	Cursor_Y-Positio	n_Magnitude_Bits		Project:	All
		des the magnitude bits of a signe bit of this value is provided by bit	d 13-bit value that specifies the v 31of this register.	ertical positio	on of
		180° rotation, this field specifies t ctive video area in the unrotated	he vertical position of the lower rigorientation.	ght corner re	lative
15	Cursor_X-Position	n_Sign_Bit		Project:	All
	For normal high re-		e that specifies the horizontal posi or must have at least a single pixe		
	the active screen.				
14:12		oject: All	Format:	MBZ	
14:12 11:0	Reserved Pro	oject: All n_Magnitude_Bits	Format:	MBZ Project:	All
	Reserved Pro Cursor_X-Position These 12 bits prov	n_Magnitude_Bits	Format: pecifies the horizontal position of	Project:	



4.7.4 CURBPALET—Cursor B Palette registers

CURBPALET—Cursor B Palette registers						
Register Type:	ММІО					
Address Offset:	700D0h-700DFh					
Project:	All					
Default Value:	0000000h					
Access:	R/W					
Size (in bits):	4x32					
Double Buffer Update Point:	Start of vertical blank or pipe disabled					

The cursor palette provides color information when using one of the indexed modes. The two-bit index selects one of the four colors or two of the colors when in the AND/XOR cursor mode. The cursor palette provides color information when using one of the indexed modes. The two-bit index selects one of the four colors or two of the colors when in the AND/XOR cursor mode. See Cursor A palette usage table.

DWord	Bit	Description					
0	31:0	CURBPALET0	Project:	All	Format:	Cursor Palette Format	
1	31:0	CURBPALET1	Project:	All	Format:	Cursor Palette Format	
2	31:0	CURBPALET2	Project:	All	Format:	Cursor Palette Format	
3	31:0	CURBPALET3	Project:	All	Format:	Cursor Palette Format	

4.7.5 CURBSURFLIVE—Cursor B Live Surface Base Address Register

CURBSURFLIVE—Cursor B Live Surface Base Address Register

Register Ty	rpe: MMIO	
Address Of	f <mark>set:</mark> 700ECh-700Efh	
Project:	All	
Default Val	ue: 0000000h	
Access:	Read Only	
Size (in bits	s): 32	
Bit	Descript	ion
31:0	Cursor_Live_Surface_Base_Address	Project: All Format:
	This gives the live value of the surface base address as	being currently used for the plane.



4.8 Primary A Plane Control

The DSPACNTR and DSPASTRIDE active registers will be updated on the vertical blank or when pipe is disabled, after the DSPASURF trigger register is written, or when the primary A is not yet enabled – thus providing an atomic update of the primary A control, stride, and base address registers.

4.8.1.1 DSPACNTR—Primary A Control Register

		DSP	ACNTR—Primary A Control Register	
Register T	Гуре:		MMIO	
Address C	Offset:		70180h-70183h	
Project:			All	
Default Va	alue:		0000000h	
Access:			R/W	
Size (in bits):			32	
Double Buffer Update Point:			Start of vertical blank or pipe disabled or primary disabled, after armed	
Double Buffer Armed By:			Write to DSPASURF	
Primary A	Plane is cor	nnected to p	bipe A only.	
Bit			Description	
31 Primary_Plane_En			able Project: All Format:	Enable
	memory t the plane	fetches cea e. When in S	the primary plane will generate pixels for display. When set to zero, prir se and plane output is transparent. The display pipe must be enabled to Self Refresh Big FIFO mode, write to this register to enable the plane wil and delayed while Big FIFO mode is exiting.	o enable
30	Gamma	Enable		
	Project:		All	
	Default \	Value:	0b	
		ipe gamma	be changed after the plane has been disabled. It controls the bypassing unit for the plane pixel data. For 8-bit indexed display data, this bit sho	
	Value	Name	Description	Project
	0b	Bypass	Plane pixel data bypasses the display pipe gamma correction logic	All
	1b	Correct	Plane pixel data is gamma corrected in the display pipe gamma	All



29:26	Source	Pixel_Form	nat			
	Project:	_	All			
	Default V	alue:	Ob			
	These bit uses the pixel.	ts should or pipe palette	nly be changed after the plane has been disable e. Before entering the blender, each source for	ed. Pixel format of 8-bit in mat is converted to 12 bits	dexed per	
	Value	Name		Description	Project	
	0010b	8bpp		8-bpp Indexed	All	
	0101b	16-bit BG	RX (5:6:5 MSB-R:G:B)	pixel format (XGA compatible).	All	
	0110b	32-bit BG	RX (8:8:8:8 MSB-X:R:G:B)	pixel format. Ignore alpha	ı All	
	1000b	1000b 32-bit RGBX (2:10:10:10 MSB-X:B:G:R) pixel format. Ignore alpha				
	1010b	1010b 32-bit BGRX (2:10:10:10 MSB-X:R:G:B) pixel format. Ignore alpha				
	1100b	1100b 64-bit RGBX Floating Point(16:16:16:16 MSB-X:B:G:R) pixel format. Ignore alph				
		Use of 64 80% of co	Ibpp format will limit the maximum dot clock to dclk			
	1110b	32-bit RG	BX (8:8:8:8 MSB-X:B:G:R)	pixel format. Ignore alpha	ı All	
	others Reserved Reserved					
25	Reserved	d Proj	ect: DevSNB	Format:		
24	Pipe_Col	lor_Space	_Conversion_Enable			
	Project:		All			
		nables pipe	0b e color space conversion for the plane pixel data t to match the format of the plane pixel data.	a. CSC mode in the pipe C	SC	
	Value	Name	Description		Project	
	0b	Bypass	Plane pixel data bypasses the pipe color space	e conversion logic	All	
	1b	1b Pass Plane pixel data passes through the pipe color space conversion logi				
23:16	Reserved	d Proj	ect: All	Format:		
15	180°_Dis	play_Rota	tion			
	Project:		All			
	Default V		Ob			
			ne plane to be rotated 180°. In addition to settir offset to the lower right corner of the unrotated		so set	
	Value	Name	Description		Project	
	0b	None	No rotation		All	



14	Trickle_I	Feed_Enab	ble			
	Project:		All			
	Default V	alue:	0b			
	This bit m	ust always	be programmed to '1'.			
	Value	Name	Description	Project		
	0b	Enable	Trickle Feed Enabled - Plane data requests are sent whenever there is space in the Display Data Buffer.	All		
	1b	Disable	Trickle Feed Disabled - Plane data requests are sent in bursts	All		
2:11	Reserved	l Proj	ect: All Format:			
10	Tiled_Su	rface				
	Project:		All			
	Default V	alue:	Ob			
	This bit indicates that the plane surface data is in tiled memory. Only X tiling is supported for display surfaces.					
	When thi DSPASU	s bit is set, RF registe	it affects the hardware interpretation of the DSPATILEOFF, DSPALINOF rs.	F, and		
	When this DSPASU	s bit is set, RF register Name	it affects the hardware interpretation of the DSPATILEOFF, DSPALINOF rs. Description			
	DSPASU	RF register	rs.			
	DSPASU Value	RF register	Description	Project		
9	DSPASU Value 0b 1b	RF register Name Linear X-tiled	Description Plane uses linear memory	Project All		
9	DSPASU Value 0b 1b	RF register Name Linear X-tiled	Description Plane uses linear memory Plane uses X-tiled memory	Project All		
9	DSPASU Value 0b 1b Asynchro	RF register Name Linear X-tiled	Description Plane uses linear memory Plane uses X-tiled memory face_Address_Update_Enable	Project All		
9	DSPASU Value 0b 1b Project: Default V This bit w address	RF register Name Linear X-tiled Donous_Sur alue: vill enable a will change	Description Plane uses linear memory Plane uses X-tiled memory rface_Address_Update_Enable All	Project All All e surface		
9	DSPASU Value 0b 1b Project: Default V This bit w address	RF register Name Linear X-tiled DODOUS_SUR alue: vill enable a will change rtical blank	The set of the surface address when written by MMIO. The with the next TLB request or when start of vertical blank is reached. Update. Update	Project All All e surface		
9	DSPASU Value 0b 1b Noject: Default V This bit w address v during ve Restricti	RF register Name Linear X-tiled Conous_Sur alue: vill enable a will change rtical blank ons:	The set of the surface address when written by MMIO. The with the next TLB request or when start of vertical blank is reached. Update. Update	Project All All e surface dates		
9	DSPASU Value Ob 1b Noject: Default V This bit w address w during ve Restricti - No is - W	RF register Name Linear X-tiled Conous_Sur alue: vill enable a vill change rtical blank ons: co command enabled.	Description Plane uses linear memory Plane uses X-tiled memory Plane uses X-tiled memory rface_Address_Update_Enable All Ob asynchronous updates of the surface address when written by MMIO. Th with the next TLB request or when start of vertical blank is reached. Upd may not complete until after the first few active lines are displayed. d streamer initiated surface address updates to this plane are allowed wh done indication in pipe status register before writing the surface address restrict	Project All All e surface dates en this bi		
9	DSPASU Value Ob 1b Noject: Default V This bit w address w during ve Restricti - No is - W	RF register Name Linear X-tiled Conous_Sur alue: will enable a will change rtical blank ons: co command enabled. dait for flip co	Description Plane uses linear memory Plane uses X-tiled memory Plane uses X-tiled memory rface_Address_Update_Enable All Ob asynchronous updates of the surface address when written by MMIO. Th with the next TLB request or when start of vertical blank is reached. Upd may not complete until after the first few active lines are displayed. d streamer initiated surface address updates to this plane are allowed wh done indication in pipe status register before writing the surface address restrict	Project All All e surface dates en this bit		
9	DSPASU Value Ob 1b Nroject: Default V This bit w address v during ve Restricti - Nv is - W ag	RF register Name Linear X-tiled Conous_Sur alue: will enable a will change rtical blank ons: co command enabled. dait for flip c gain with th	Description Plane uses linear memory Plane uses X-tiled memory Plane uses X-tiled memory rface_Address_Update_Enable All Ob asynchronous updates of the surface address when written by MMIO. Th with the next TLB request or when start of vertical blank is reached. Upd may not complete until after the first few active lines are displayed. d streamer initiated surface address updates to this plane are allowed wh done indication in pipe status register before writing the surface address ris bit set.	Project All All e surface dates en this bit egister		

Primary Plane Source Pixel Format Mapping of Bits to Colors:



Note: For 64-bit Floating Point format, each of the 16 bit color components is 1:5:10 MSB-sign:exponent:fraction

PRIMARY RGB	Ignored	Red	Green	Blue
16-bit BGRX 5:6:5	N/A	15:11	10:5	4:0
32-bit BGRX 8:8:8	31:24	23:16	15:8	7:0
32-bit RGBX 10:10:10	31:30	9:0	19:10	29:20
32-bit BGRX 10:10:10	31:30	29:20	19:10	9:0
64-bit RGBX Float 16:16:16	63:48	15:0	31:16	47:32
32-bit RGBX 8:8:8	31:24	7:0	15:8	23:16

4.8.2 DSPALINOFF—Primary A Linear Offset Register

Register Type:		MMIO			
Address Offset:		70184h-70187h			
Project:		All			
Default Value:		0000000h			
Access:		R/W			
Size (in bits):		32			
Double Bu	ffer Update Point:	Start of vertical blank or pipe disa	bled		
Bit		Descript	tion		
31:0	Primary_Linear_O	ffset	Project: All Format:		
	surface address to aligned. When per- pixel of the last line	get the address of the first pixel to b forming 180° rotation, the unpanned	o the primary plane. This value is added to the e displayed. This offset must be at least pixel offset must be the difference between the last prientation and the display surface address. re ignored.		



Register Type:		MMIO		
Address C	Offset:	70188h-7018	3h	
Project:		All		
Default Va	lue:	00000000h		
Access:		R/W		
Size (in bit	ts):	32		
Double Bu	Iffer Update Point:	Start of vertica	ıl blank or	r pipe disabled or primary disabled, after armed
Double Bu	Iffer Armed By:	Write to DSPA	SURF	
Bit				Description
31:16	Reserved Pro	ject: All		Format:
15:6	Primary_Stride	Project:	All	Format:
	aligned. When usin line to line increment	g tiled memory, at for the display. and stream or wri	this must This regi	es. When using linear memory, this must be 64 byte be 512 byte aligned. This value is used to determine the gister is updated through either a command packet passed s register. The stride is limited to a maximum of 32K bytes

4.8.3 DSPASTRIDE—Primary A Stride Register

4.8.4 DSPASURF—Primary A Surface Base Address Register

Register Type:	MMIO
Address Offset:	7019Ch-7019Fh
Project:	All
Default Value:	0000000h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe disabled



Bit			De	scription		
31:12	Primary_Surfac	ce_Base_A	Address			
	Project:	All				
	Address:	Gra	aphicsAddress[31:12]			
	(x, y) offsets in t	the DSPAT		When the surface is tiled, n the surface is in linear me ⁻ register.		
	tiled memory, th software or by c	is address command p	must be 256K aligned. ackets in the command	ng asynchronous flips and This register can be writte stream. It represents an o pages through the global G	n directly	/ through
11:3	tiled memory, th software or by c memory apertury	is address command p	must be 256K aligned. ackets in the command	This register can be writte stream. It represents an o pages through the global G	n directly	/ through
11:3 2	tiled memory, th software or by c memory apertury	is address command p re base and	must be 256K aligned. ackets in the command d is mapped to physical	This register can be writte stream. It represents an o pages through the global G	n directly ffset fror STT.	/ through

4.8.5 DSPATILEOFF—Primary A Tiled Offset Register

	DSPA1	FILEOF	F—Primary A Tiled Offs	et Reg	ist	er
Register Ty	ype:	MMIO				
Address O	ffset:	701A4	h-701A7h			
Project:		All				
Default Val	ue:	00000	000h			
Access:		R/W				
Size (in bit	s):	32				
Double Bu	ffer Update Point:	Start of	f vertical blank or pipe disabled			
register are from the be		the surfac	is specified in the DSPALINOFF reg e is tiled, the start position is specifi			
Bit			Description			
31:28	Reserved P	roject:	All	Form	nat:	MBZ
27:16	Primary_Start_Y	-Position	Р	roject: A	.11	Format:
	the display surfac	e. When p	rtical position in lines of the beginning of performing 180° rotation, this field specif art of the active display plane in the unre	ies the verti	ical p	osition of the lower
15:12	Reserved P	roject:	All	Form	nat:	MBZ



DSPATILEOFF—Primary A Tiled Offset Register					
11:0	Primary_Start_X-Position	Project: All Format:			
	These 12 bits specify the horizontal offset in pixels to the display surface. When performing 180° rotat lower right corner relative to the start of the active of				

4.8.6 DSPASURFLIVE—Primary A Live Surface Base Address

Register	Type:	MMIO				
Address Offset:		701ACh-701AFh				
Project: All		All				
Default Value:		00000000h				
Access:		Read Only				
Size (in b	oits):	32				
Trusted	Гуре:	1				
Bit	Desc	ription				
31:0	Prin	nary_Live_Surfa	ace_Base_Address			
	Proj	ect:	All			
	Add	ress:	GraphicsAddress[31:0]			
	This	aives the live va	alue of the surface base address as being currently used for the plane.			



4.9 Primary B Plane Control

The DSPBCNTR and DSPBSTRIDE active registers will be updated on the vertical blank or when pipe is disabled, after the DSPBSURF trigger register is written, or when the primary B is not yet enabled – thus providing an atomic update of the primary B control, stride, and base address registers.

4.9.1 DSPBCNTR—Primary B Control Register

		D3FI	BCNTR—Primary B Control Register		
Register Type:			MMIO		
Address Offset:			71180h-71183h		
Project:			All		
Default Va	alue:		0000000h		
Access:			R/W		
Size (in bi			32		
	uffer Update		Start of vertical blank or pipe disabled or primary disabled, after armed	ł	
	uffer Armed		Write to DSPBSURF		
^{>} rimary B	Plane is co	nnected t	to pipe B only		
Bit			Description		
31	Primary_F	Plane_Ena	able Project: All Format:	Enable	
	memory fe the plane.	etches cea When in S	the primary plane will generate pixels for display. When set to zero, prir use and plane output is transparent. The display pipe must be enabled to Self Refresh Big FIFO mode, write to this register to enable the plane will and delayed while Big FIFO mode is exiting.	o enable	
30	Gamma_E	Enable			
30	Project:		All		
30	1 10/000	Default Value: 0b			
30	,	alue:	0b		
30	Default Va This bit sh	ould only l	0b be changed after the plane has been disabled. It controls the bypassing unit for the plane pixel data. For 8-bit indexed display data, this bit sho		
30	Default Va This bit sh display pip	ould only l	be changed after the plane has been disabled. It controls the bypassing	uld be set	
30	Default Va This bit sh display pip to a one.	ould only l be gamma	be changed after the plane has been disabled. It controls the bypassing unit for the plane pixel data. For 8-bit indexed display data, this bit sho		



29:26	Source_Pixel_Format					
	Project: All					
	Default V	alue:	Ob			
			nly be changed after the plane has been disable e. Before entering the blender, each source for			
	Value	Name		Description	Projec	
	0010b	8bpp		8-bpp Indexed	All	
	0101b	16-bit BG	RX (5:6:5 MSB-R:G:B)	pixel format (XGA compatible).	All	
	0110b	32-bit BG	RX (8:8:8:8 MSB-X:R:G:B)	pixel format. Ignore alpha	All	
	1000b	32-bit RG	BX (2:10:10:10 MSB-X:B:G:R)	pixel format. Ignore alpha	All	
	1010b	32-bit BG	RX (2:10:10:10 MSB-X:R:G:B)	pixel format. Ignore alpha	All	
	1100b	64-bit RG	BX Floating Point(16:16:16:16 MSB-X:B:G:R)	pixel format. Ignore alpha	All	
		Use of 64bpp format will limit the maximum dot clock to 80% of cdclk.				
	1110b	32-bit RG	BX (8:8:8:8 MSB-X:B:G:R)	pixel format. Ignore alpha	All	
	others	Reserved Reserved				
25	Reserved	l Proje	ect: DevSNB			
24	Pipe_Col Project:	or_Space_	Conversion_Enable			
	Default V	alue:	0b			
			color space conversion for the plane pixel data t to match the format of the plane pixel data.	a. CSC mode in the pipe C	SC	
	Value	Name	Description		Project	
	0b	Bypass	Plane pixel data bypasses the pipe color space	e conversion logic	All	
	1b	Pass Plane pixel data passes through the pipe color space conversion logic.				
23:16	Reserved	d Project: All Format:				
15	180°_Display_Rotation					
	Project: All					
	Default Value: 0b This mode causes the plane to be rotated 180°. In addition to setting this bit, software must also set the surface address offset to the lower right corner of the unrotated image.					
	Value	Name	Description		Project	
	Value					
	0b	None	No rotation		All	



	DSPBCNTR—Primary B Control Register					
14	Trickle_F	Feed_Enab	le			
	Project:AllDefault Value:0bThis bit must always be programmed to '1'.					
	Value Name Description F					
	0b	Enable	Trickle Feed Enabled - Plane data requests are sent whenever there is space in the Display Data Buffer.	All		
	1b	Disable	Trickle Feed Disabled - Plane data requests are sent in bursts	All		
13	Reserve	d				
12:11	Reserved	l Proje	ect: All Format:			
10	Project: All Default Value: 0b This bit indicates that the plane surface data is in tiled memory. Only X tiling is supported for dis surfaces. When this bit is set, it affects the hardware interpretation of the DSPBTILEOFF, DSPBLINOFF, a					
	DSPBSURF registers.					
	Value	Name	Description	Project		
	0b	Linear	Plane uses linear memory	All		
	1b	X-tiled	Plane uses X-tiled memory	All		
address will change with the next TLB request or when start of during vertical blank may not complete until after the first few as Restrictions:			All	dates		
	- Wait for flip done indication in pipe status register before writing the surface address register again with this bit set.					
	ay		Description	Project		
	Value	Name	Description			
		Name Sync	Surface Address MMIO writes will update synchronous to start of vertical blank	All		
	Value	-	Surface Address MMIO writes will update synchronous to start of	-		



See DSPACNTR - Primary Plane Source Pixel Format Mapping of Bits to Colors

Register 1	Гуре:	MMIO		
Address (Offset:	71184h-71187h		
Project:		All		
Default Va	alue:	0000000h		
Access:		R/W		
Size (in bits):		32		
Double Buffer Update Point:		Start of vertical blank or pipe disabled		
Bit	Description			
31:0	Primary_Linear_O	ffset	Project: All	
	This register provides the linear panning byte offset into the primary plane. This value is added to the surface address to get the address of the first pixel to be displayed. This offset must be at least pixel aligned. When performing 180° rotation, the unpanned offset must be the difference between the last pixel of the last line of the display data in its unrotated orientation and the display surface address. When the surface is tiled, the contents of this register are ignored.			

4.9.2 DSPBLINOFF—Primary B Linear Offset Register

4.9.3 DSPBSTRIDE—Primary B Stride Register

Deviator T		BSTRIDE—Primary E	3		
Register T		MMIO			
Address O	ffset:	71188h-7118Bh			
Project:		All			
Default Va	lue:	0000000h			
Access:		R/W			
Size (in bit	s):	32			
Double Buffer Update Point:		Start of vertical blank or pipe disabled or primary disabled, after armed			
Double Bu	ffer Armed By:	Write to DSPBSURF			
Bit	Description				
31:16	Reserved Pro	ject: All	Format:	MBZ	
15:6	Primary_Stride		Project:	All	
	This is the stride for the primary plane in bytes. When using linear memory, this must be 64 byte aligned. When using tiled memory, this must be 512 byte aligned. This value is used to determine line to line increment for the display. This register is updated through either a command packet pathrough the command stream or writes to this register. The stride is limited to a maximum of 32K for both linear and tiled memory.				

Reserved

Project:

All

5:0

Format:

MBZ



4.9.4 DSPBSURF—Primary B Surface Base Address Register

	DSPBSUR	F—Pri	mary B Surface Base Address Register		
Register Type:		MMIC			
Address O	ffset:	71190	Ch-7119Fh		
Project:		All	All		
Default Val	ue:	00000	0000000h		
Access:		R/W			
Size (in bit	s):	32			
Double But	ffer Update Point:	Start of	of vertical blank or pipe disabled		
Writes to th	nis register arm D	SPB regi	sters		
Bit			Description		
31:12	Primary_Surface	e_Base_A	ddress		
	Project:	All			
	Address:	Gra	phicsAddress[31:12]		
	(x, y) offsets in th	surface base address. When the surface is tiled, panning is specified using LEOFF register. When the surface is in linear memory, panning is et in the DSPBLINOFF register.			
	This address must be 4K aligned. When performing asynchronous flips and the display surface is in tiled memory, this address must be 256K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT.				
11:3	Reserved F	Project:	All Format:		
2	Reserved				
0	Reserved F	Project:	All Format: MBZ		



4.9.5 DSPBTILEOFF—Primary B Tiled Offset Register

Address Offset:	711A4h
Default:	0000000h
Normal Access: Double Buffer Update Point:	Read/Write Start of vertical blank or pipe disabled

Size: 32 bits

This register specifies the panning for the display surface. The surface base address is specified in the DSPBSURF register, and this register is used to describe an offset from that base address. When the surface is in linear memory, the offset is specified in the DSPBLINOFF register and the contents of this register are ignored. When the surface is tiled, the start position is specified in this register as an (x, y) offset from the beginning of the surface.

Bit	Descriptions			
31:28	Reserved: Write as zero			
27:16	Primary Start Y-Position: These 12 bits specify the vertical position in lines of the beginning of the active display plane relative to the display surface. When performing 180° rotation, this field specifies the vertical position of the lower right corner relative to the start of the active display plane in the unrotated orientation.			
15:12	Reserved: Write as zero			
11:0	Primary Start X-Position: These 12 bits specify the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. When performing 180° rotation, this field specifies the horizontal position of the lower right corner relative to the start of the active display plane in the unrotated orientation.			



4.9.6 DSPBSURFLIVE—Primary B Live Surface Base Address

	DSP	BSURFLIVE—	Primary B Live Surface Base Address	
Register Type:		IMIO		
Address O	ffset:	11ACh-711AFh		
Project:		AII		
Default Value:		0000000h		
Access:		Read Only		
Size (in bits):		2		
Bit			Description	
31:0 Prin		y_Live_Surface_Base	_Address	
	Projec	: All		
	Addres	s: Graphi	csAddress[31:0]	
This		s gives the live value of the surface base address as being currently used for the plane.		

4.10 Video Sprite A Control

Two video sprites are provided for the display of video content. These sprite planes provide windowing and keying functions as well as gamma and color space conversion from YUV to RGB. Each sprite plane is attached to only one of the pipes, Video Sprite A to pipe A and Video Sprite B to pipe B. Apart from the pipe assignments, the functionality is identical.

The DVSACNTR, DVSASTRIDE, DVSAPOS, DVSASIZE, and DVSASCALE active registers will be updated on the vertical blank or when pipe is disabled, after the DVSASURF trigger register is written, or when the sprite A is not yet enabled – thus providing an atomic update of the video sprite A control, stride, position, size, scale, and base address registers.



4.10.1 DVSACNTR—Video Sprite A Control Register

			NTR—Video Sprite A Control Register	
Register T			MMIO	
Address C	Offset:		72180h-72183h	
Project:			All	
Default Va	lue:		00000000h	
Access:			R/W	
Size (in bit				
	uffer Update		Start of vertical blank or pipe disabled or sprite disabled, after armed Write to DVSASURF	
	uffer Armed ite A Plane		ted to pipe A only.	
Bit			Description	
31	Sprite_E	nable	Project: All Format: Enable	
	memory f the plane	etches cea . When in S	the sprite plane will generate pixels for display. When set to zero, sprite se and plane output is transparent. The display pipe must be enabled to Self Refresh Big FIFO mode, write to this register to enable the plane with and delayed while Big FIFO mode is exiting.	o enable
30	Gamma	Enable		
30		Enable	All	
30	Project: Default V	alue:	Ob	he comme
30	Project: Default V There are correctior display pl default va	alue: e two gamm n in the disp ane. Gamr alues into th	0b na adjustments possible in the video sprite data path. This bit controls t play pipe not the gamma control in this plane. It affects only the pixel da ma correction logic that is contained in the video sprite is disabled by lo nose registers.	ata from this ading the
30	Project: Default V There are correction display pl	alue: two gamm in the disp ane. Gamr	0b na adjustments possible in the video sprite data path. This bit controls t play pipe not the gamma control in this plane. It affects only the pixel da ma correction logic that is contained in the video sprite is disabled by lo	ata from this ading the
30	Project: Default V There are correctior display pl default va	alue: e two gamm n in the disp ane. Gamr alues into th	0b na adjustments possible in the video sprite data path. This bit controls t play pipe not the gamma control in this plane. It affects only the pixel da ma correction logic that is contained in the video sprite is disabled by lo nose registers.	ata from this
30	Project: Default V There are correction display pl default va	alue: two gamm in the disp ane. Gamr alues into th Name	Ob na adjustments possible in the video sprite data path. This bit controls t play pipe not the gamma control in this plane. It affects only the pixel da ma correction logic that is contained in the video sprite is disabled by lo nose registers.	ata from this ading the Project
29	Project: Default V There are correctior display pl default va Value 0b	alue: two gamm in the disp ane. Gamr alues into th Name Disable Enable	Ob na adjustments possible in the video sprite data path. This bit controls to blay pipe not the gamma control in this plane. It affects only the pixel data a correction logic that is contained in the video sprite is disabled by lonose registers. Description Plane pixel data bypasses the display pipe gamma correction logic Plane pixel data is gamma corrected in the pipe gamma correction logic	Ata from this ading the Project
	Project: Default V There are correction display pl default va Value 0b 1b Reserved	alue: two gamm in the disp ane. Gamr alues into the Name Disable Enable d Proje	Ob na adjustments possible in the video sprite data path. This bit controls to blay pipe not the gamma control in this plane. It affects only the pixel data a correction logic that is contained in the video sprite is disabled by lonose registers. Description Plane pixel data bypasses the display pipe gamma correction logic Plane pixel data is gamma corrected in the pipe gamma correction logic	Ata from this ading the Project
29	Project: Default V There are correction display pl default va Value 0b 1b Reserved	alue: two gamm in the disp ane. Gamr alues into the Name Disable Enable d Proje	Ob na adjustments possible in the video sprite data path. This bit controls to blay pipe not the gamma control in this plane. It affects only the pixel data ma correction logic that is contained in the video sprite is disabled by lonose registers. Description Plane pixel data bypasses the display pipe gamma correction logic Plane pixel data is gamma corrected in the pipe gamma correction logic ect: All Format: MB2	Ata from this ading the Project
29	Project: Default V There are correction display pl default va Value Ob 1b Reserved YUV_By	alue: e two gamm in the disp ane. Gamr alues into th Disable Enable d Proje pass_Exce	Ob na adjustments possible in the video sprite data path. This bit controls to blay pipe not the gamma control in this plane. It affects only the pixel data ma correction logic that is contained in the video sprite is disabled by lonose registers. Description Plane pixel data bypasses the display pipe gamma correction logic Plane pixel data is gamma corrected in the pipe gamma correction logic ect: All Format: MB2 ess-512_Format_Conversion	Ata from this ading the Project
29	Project: Default V There are correction display pl default va Value 0b 1b 1b Reserved YUV_Byp Project:	alue: e two gamm in the disp ane. Gamr alues into th Disable Enable d Proje pass_Exce	Ob na adjustments possible in the video sprite data path. This bit controls to blay pipe not the gamma control in this plane. It affects only the pixel data ma correction logic that is contained in the video sprite is disabled by lo nose registers. Description Plane pixel data bypasses the display pipe gamma correction logic Plane pixel data is gamma corrected in the pipe gamma correction logic ect: All Format_Conversion All	Ata from this ading the Project All All
29	Project: Default V There are correction display pl default va Value 0b 1b 1b Reserved YUV_Byp Project: Default V	alue: two gamm in the disp ane. Gamr alues into th Disable Enable d Proje pass_Exce alue:	Ob Da adjustments possible in the video sprite data path. This bit controls to blay pipe not the gamma control in this plane. It affects only the pixel data ma correction logic that is contained in the video sprite is disabled by lonose registers. Description Plane pixel data bypasses the display pipe gamma correction logic Plane pixel data is gamma corrected in the pipe gamma correction logic ect: All Format_Conversion All Ob	Ata from this ading the Project All All



	• -	orrection_	-			
	Project:		All			
	Default V		0b			
	expanded	to full rang	e RGB, setting th	e correction logic. Normally the range compres his bit will generate range compressed RGB. The erial is used. This bit has no effect on RGB sou	his bit shou	uld also
	Value	Name	Description	P	Project	
	0b	Enable	Range correction	on enabled A	All	
	1b	Disable	No range corre	ction A	All	
26:25	Source_I	Pixel_Form	at			
	Project:		DevSNB			
	Default V	alue:	0b			
		selects the I to 12 bits		he sprite. Before entering the blender, each so	urce forma	t is
	Value	Name		Description		Project
	00b	YUV 4:2:2	2	YUV 4:2:2 packed pixel format (byte order programmed separately)		All
	01b	RGB 32-t	bit 2:10:10:10	RGB 32-bit 2:10:10:10 pixel format (color order programmed separately). Ignore alpha.	er	All
	10b	RGB 32-t	bit 8:8:8:8	RGB 32-bit 8:8:8:8 pixel format (color order programmed separately). Ignore alpha.		All
	11b	RGB 64-b	oit 16:16:16:16	RGB 64-bit 16:16:16:16 floating point pixel for		All
		limit the n	bpp format will naximum dot 0% of cdclk.	(color order programmed separately). Ignore	alpha.	
24	Pipe Col	or Space	_Conversion_En	able		
47	Project:		All			
27	Default V	alue:	0b			
27			olor chaco con	version for the plane pixel data. This is separat		
27	conversio	on logic with	nin the sprite plan	ie. CSC mode in the pipe CSC registers must be r the color conversion logic within the sprite pla		aton
27	conversio	on logic with	nin the sprite plan	ne. CSC mode in the pipe CSC registers must b	ne.	Project
27	conversion the formation	on logic with it of the pla	nin the sprite plan ne pixel data afte Description	ne. CSC mode in the pipe CSC registers must b	ne.	



22	Project: Default V This bit e	nables sou	 Finable All Ob arce color keying. Sprite pixel values that match (within range) the be key can not be enabled if destination key is enabled. 	key will become
	Value	Name	Description Pro	oject
	0b	Disable	Sprite source key is disabled All	l
	1b	Enable	Sprite source key is enabled All	
21	Reserved	d Proj	ect: DevSNB Format:	
	Project: Default V	alue:	DevSNB 0b	
	I his field is ignored		select the color order when using RGB data formats. For other for	rmats, this field
			-	rmats, this field
	is ignored	d.	-	oject
	is ignored Value	d. Name	Description Pro-	oject
20	is ignored Value 0b	Name BGRX RGBX	DescriptionProBGRX (MSB-X:R:G:B)AllRGBX (MSB-X:B:G:R)All	oject
20 19	is ignored Value 0b 1b Reserved Project: Default V This bit e	d. Name BGRX RGBX roj noversion_ alue: nables or c to be used	Description Pro BGRX (MSB-X:R:G:B) All RGBX (MSB-X:B:G:R) All ect: DevILK	oject I
-	is ignored Value 0b 1b Reserved Project: Default V This bit e intended	d. Name BGRX RGBX roj noversion_ alue: nables or c to be used	Description Product BGRX (MSB-X:R:G:B) All RGBX (MSB-X:B:G:R) All ect: DevILK Format: Totabled All Ob disables the color conversion logic internal to the sprite. Color conversion	oject
-	is ignored Value 0b 1b Reserved Project: Default V This bit e intended source fo	d. Name BGRX BGRX RGBX Proj Drversion_ alue: alue: brables or c to be used brmats.	Description Product of the sprite BGRX (MSB-X:R:G:B) All RGBX (MSB-X:B:G:R) All ect: DevILK Format: Disabled All Ob disables the color conversion logic internal to the sprite. Color conversion with the formats that support YUV format. This bit is ignored whe	version is en using RGB



18	-	JVJAC	NTR—Video Sprite A Control Registe	21
	YUV_For	mat		
	Project:		All	
	Default V	alue:	Ob	
			e source YUV format for the YUV to RGB color conversion ope e data is RGB.	eration. This field is
	Value	Name	Description	Project
	0b	BT.601	ITU-R Recommendation BT.601	All
	1b	BT.709	ITU-R Recommendation BT.709	All
17:16	YUV_Byt	e_Order		
	Project:		All	
	Default V	alue:	Ob	
	This field field is ign		select the byte order when using YUV 4:2:2 data formats. Fo	r other formats, this
	Value	Name	Description	Project
	00b	YUYV	YUYV (8:8:8:8 MSB-V:Y ₂ :U:Y ₁)	All
	01b	UYVY	UYVY (8:8:8:8 MSB-Y _{2:} V:Y _{1:} U)	All
	10b	YVYU	YVYU (8:8:8:8 MSB-U:Y ₂ :V:Y ₁)	All
	11b	VYUY	VYUY (8:8:8:8 MSB-Y ₂ :U:Y ₁ :V)	All
15	180°_Dis	play_Rota	ion	
	Project:		All	
	Default V	alue:	Ob	
	the surface	ce address	ne plane to be rotated 180°. In addition to setting this bit, soft offset to the lower right corner of the unrotated and unscaled ative to the lower right corner.	
	Value	Name	Description	Project
		1	No. underlie u	
	0b	None	No rotation	All
	0b 1b	None 180	180° rotation	All
14	1b		180° rotation	
14	1b	180	180° rotation	
14	1b Trickle-F	180 Feed_Enabl	180° rotation e	
14	1b Trickle-F Project:	180 Feed_Enabl	180° rotation e DevSNB	
14	1b Trickle-F Project: Default V	180 eed_Enabl alue:	180° rotation e DevSNB 0b	All Project
14	1b Trickle-F Project: Default V Value	180 eed_Enabl alue: Name	180° rotation e DevSNB 0b Description Trickle Feed Enabled - Data requests are sent whenever th	All Project



DVSAST When this registers.	alue: ndicates tha RIDE regis s bit is set,	All 0b at the surface data is in tiled memory. The tile pitch ter. Only X tiling is supported for display surfaces. it affects the hardware interpretation of the DVSAS	
Default Va This bit ir DVSAST When this registers.	ndicates tha RIDE regis s bit is set,	0b at the surface data is in tiled memory. The tile pitch ter. Only X tiling is supported for display surfaces.	
DVSAST When this registers.	RIDE regis s bit is set,	ter. Only X tiling is supported for display surfaces.	
registers.		it affects the hardware interpretation of the DVSAS	
M.1.			TAKT and DVSASUKFADDR
Value	Name	Description	Project
0b	Linear	Linear memory	All
1b	Tiled	Tiled memory	All
	- · · · · ·		Format: MBZ
-	estination	•	
	alue:	Ob	
key value	in DVSAK	EYVAL the sprite pixel is used, otherwise the prima	ary plane pixel is passed
Value	Name	Description	Project
0b	Disable	Destination Key is disabled	All
1b	Enable	Destination Key is enabled	All
	Reserved Sprite_De Project: Default V: This bit e key value through th Value 0b	Reserved Project: Project: Default Value: This bit enables the key value in DVSAK through the blender Value Name 0b Disable	Reserved Project: All Sprite_Destination_Key Project: All Default Value: 0b 0b This bit enables the destination key function. If the pixel for the primary key value in DVSAKEYVAL the sprite pixel is used, otherwise the primary through the blender unmodified. Destination Key can not be enabled if Value Name Description 0b Disable Destination Key is disabled

Sprite Source Pixel Format Mapping of Bits to Colors:

Note: For RGB formats, see the primary source pixel format mapping

SPRITE YUV	¥1	U	Y2	v
YUV 4:2:2 YUYV	7:0	15:8	23:16	31:24
YUV 4:2:2 UYVY	15:8	7:0	31:24	23:16
YUV 4:2:2 YVYU	7:0	31:24	23:16	15:8
YUV 4:2:2 VYUY	15:8	23:16	31:24	7:0



4.10.2 DVSALINOFF—Video Sprite A Linear Offset Register

Register Type:	ММЮ
Address Offset:	72184h-72187h
Project:	All
Default Value:	0000000h
Access:	R/W
Size (in bits):	32
Double Buffer Upo	te Point: Start of vertical blank or pipe disabled
Bit	Description
31:0 Sprite	Linear_Offset Project: All Format:
surfac aligne perform line of	ister provides the linear panning byte offset into the sprite plane. This value is added to the address to get the address of the first pixel to be displayed. This offset must be at least pixel for unrotated RGB formats and even pixel aligned for unrotated YUV formats. When ng 180° rotation, the unpanned offset must be the difference between the last pixel of the last e display data in its unrotated orientation and the display surface address. When the surface the contents of this register are ignored.

4.10.3 DVSASTRIDE—Video Sprite A Stride Register

	DVSAS	SIRIDE-	-Video	Sprite A Stride Register
Register T	ype:	MMIO		
Address C	offset:	72188h-721	8Bh	
Project:		All		
Default Va	lue:	00000000h		
Access:		R/W		
Size (in bit	ts):	32		
Double Bu	Iffer Update Point:	Start of vert	ical blank	or pipe disabled or sprite disabled, after armed
Double Bu	Iffer Armed By:	Write to DV	SASURF	
Bit				Description
31:15	Reserved Pro	ject: All		Format:
14:6	Sprite_Stride	Project	All	Format:
	When using tiled me command packet pa	emory, this mu assed through K bytes when	ist be 512 the comm sprite sca	hen using linear memory, this must be 64 byte aligned. byte aligned. This register is updated through either a hand stream or writes to this register. The stride is limited ling is not enabled, 4K bytes when sprite scaling is
5:0	Reserved Pro	ject: All		Format:



4.10.4 DVSAPOS—Video Sprite A Position Register

DVSAF	POS—Video Sprite A Position Register
Register Type:	MMIO
Address Offset:	7218Ch-7218Fh
Project:	All
Default Value:	0000000h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe disabled or sprite disabled, after armed
Double Buffer Armed By:	Write to DVSASURF, DVSAPOS write does not disarm
This register specifies the posi	tion of the sprite. Software must take care that the sprite does not extend out

of the display active area. ie. Xposition + Xsize =< Xsrcsize

Bit	Description		
31:28	Reserved Project: All For	rmat:	MBZ
27:16	Sprite_Y-PositionProject:AllFormat:These 12 bits specify the vertical position in lines of the sprite (upper left corner beginning of the active video area. When performing 180° rotation, this field sposition of the lower right corner relative to the end of the active video area in The defined sprite rectangle must always be completely contained within the or screen image.	specifies the unr	s the vertical otated orientation.
15:12	Reserved Project: All For	rmat:	MBZ
11:0	Sprite_X-PositionProject:AllFormat:These 12 bits specify the horizontal position in pixels of the sprite (upper left or beginning of the active video area. When performing 180° rotation, this field sp position of the original lower right corner relative to the original end of the active unrotated orientation. The defined sprite rectangle must always be completely 	pecifiés ve video	the horizontal area in the



4.10.5 DVSASIZE—Video Sprite A Size Register

	DVS	ASIZE—	Vide	o Sprite A Size Regi	ster	
Register Ty	/pe:	MMIO				
Address O	ffset:	72190h-72 ²	193h			
Project:		All				
Default Val	ue:	00000000h				
Access:		R/W				
Size (in bit	•	32				
	ffer Update Point:			nk or pipe disabled or sprite disabl	led, after a	rmed
	ffer Armed By:	Write to DV				
	active area. ie. Xp			ware must take care that the sp Xsrcsize		
Bit				Description		
31:28	Reserved Pro	ject: All			Format:	MBZ
27:16	Sprite_Height	Project:	All	Format:		
		he defined sp	rite rec	neight of the sprite in lines. The va tangle must always be completely		
15:12	Reserved Pro	ject: All			Format:	MBZ
11:0	Sprite_Width	Project:	All	Format:		
	same as the stride	but should be e. The defined	less th sprite	width of the sprite in pixels. This d an or equal to the stride in pixels. rectangle must always be complet	The value	in the register is
				dth minus one value) is limited to e iply is set to Line/Pixel doubling or		



4.10.6 DVSAKEYVAL—Video Sprite A Color Key Value Register

Register T	vpe:	MMIO		
Address C	· ·	72194h-72197h		
Project:		All		
Default Va	lue:	0000000h		
Access:		R/W		
Size (in bi	ts):	32		
•	Iffer Update Point:	Start of vertical blank or pipe disabled		
compare v		m value for the range compare. In destin		
Bit		Description		
Bit 31:24		Description	Format:	MBZ
	Reserved Pro	· · · · ·	Format: Project: All	MBZ Format:
31:24	Reserved Pro V_Source_Key_Mi	ject: All n_Value/R_Source/Dest_Key_Value key (minimum) value for the sprite V channel s	Project: All	Format:
31:24	Reserved Pro V_Source_Key_Mi Specifies the color key color or destination key color	ject: All n_Value/R_Source/Dest_Key_Value key (minimum) value for the sprite V channel s	Project: All	Format:
31:24 23:16	Reserved Pro V_Source_Key_Mi Specifies the color H or destination key c Y_Source_Key_Mi Specifies the color H	ject: All n_Value/R_Source/Dest_Key_Value key (minimum) value for the sprite V channel so ompare value.	Project: All source key or the Re Project: All	Format: d channel source Format:
31:24 23:16	Reserved Pro V_Source_Key_Mi Specifies the color H or destination key c Y_Source_Key_Mi Specifies the color H Source or destination	ject: All n_Value/R_Source/Dest_Key_Value key (minimum) value for the sprite V channel s ompare value. n_Value/G_Source/Dest_Key_Value key (minimum) value for the sprite Y channel s	Project: All source key or the Re Project: All	Format: d channel source Format:



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4.10.7 DVSAKEYMSK—Video Sprite A Color Key Mask Register

DVSAKEYM	SK—Video Sprite A Color Key Mask Register
Register Type:	MMIO
Address Offset:	72198h-7219Bh
Project:	All
Default Value:	0000000h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe disabled

For source key this register specifies which channels to perform range checking on.

For destination key this register specifies the key mask to be used with the color value bits to determine if the display source data matches the key when enabled. A zero bit in the mask indicates that the corresponding bit match failure should be ignored when determining if the pixel matches.

Note that source key and destination key are mutually exclusive modes of operation, they can not be used simultaneously. For the function that is not enabled, the associated bits in this register should be programmed to zeroes.

Bit	Description			
31:27	Reserved Project: All	Forma	at:	MBZ
26	V/R_Channel_Source_Key_Enable Specifies the source color key enable for the V/Red channel	Project:	All	Format:
25	Y/G_Channel_Source_Key_Enable Specifies the source color key enable for the Y/Green channel	Project:	All	Format:
24	U/B_Channel_Source_Key_Enable Specifies the source color key enable for the U/Blue channel	Project:	All	Format:
23:16	R_mask_Dest_Key_Value Specifies the destination color key mask for the sprite R channel	Project:	All	Format:
15:8	G_mask_Dest_Key_Value Specifies the destination color key mask for the sprite G channel	Project:	All	Format:
7:0	B_mask_Dest_Key_Value Specifies the destination color key mask for the sprite B channel	Project:	All	Format:



4.10.8 DVSASURF—Video Sprite A Surface Address Register

	DVSASURF		s Register
Register Ty	/pe:	MMIO	
Address Of	ffset:	7219Ch-7219Fh	
Project:		All	
Default Val	ue:	0000000h	
Access:		R/W	
Size (in bits	s):	32	
Double But	ffer Update Point:	Start of vertical blank or pipe disabled	
Writes to the	nis register arm DVS	A registers	
Bit		Description	
31:12	Sprite_Surface_Ba	se_Address	
	Project:	All	
	Address:	Graphicsdress[31:12]	
	(x, y) offsets in the [ies the surface base address. When the surface is tiled, DVSATILEOFF register. When the surface is in linear m ear offset in the DVSALINOFF register.	
	is mapped to physic	e 4K aligned. It represents an offset from the graphics i al pages through the global GTT. The value in this regis with synchronous flips.	
11:0	Reserved Proj	ect: All F	ormat:



4.10.9 DVSAKEYMAXVAL—Video Sprite A Color Key Max Value Register

Register T	Type:	MMIO			
Address C		/21A0h-721A3h			
Project:		All			
Default Va	alue: (0000000h			
Access:	F	R/W			
Size (in bi	ts):	32			
Double Bu	uffer Update Point:	Start of vertical blank or pipe disabled			
	he key. This register w	ill only have an effect when the spr	ite source color k	key is	enabled
Bit	he key. This register w	ill only have an effect when the spr Description	ite source color k	key is	enabled
	he key. This register w Reserved Project	Description	ite source color k	-	enabled MBZ
Bit		Description		-	
Bit 31:24	Reserved Project	Description	Form	at:	MBZ
Bit 31:24	Reserved Project	t: All	Form	at:	MBZ
Bit 31:24 23:16	Reserved Project V_Key_Max_Value Specifies the color key Y_Key_Max_Value	t: All	Form Project:	at: All	MBZ Format:
Bit 31:24 23:16	Reserved Project V_Key_Max_Value Specifies the color key Y_Key_Max_Value	t: All value for the sprite V channel	Form Project:	at: All	MBZ Format:



4.10.10 DVSATILEOFF—Video Sprite A Tiled Offset Register

Register Type:	MMIO
Address Offset:	721A4h-721A7h
Project:	All
Default Value:	0000000h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe disabled

specified in the DVSASURFADDR register, and this register is used to describe an offset from that base address. When the surface is in linear memory, the offset is specified in the DVSALINOFF register and the contents of this register are ignored. When the surface is tiled, the start position is specified in this register as an (x, y) offset from the beginning of the surface.

Bit	Description	
31:28	Reserved Project: All	Format: MBZ
27:16	Sprite_Start_Y-Position These 12 bits specify the vertical position in lines of the beg the display surface. When performing 180° rotation, this fie right corner relative to the start of the active display plane in	Id specifies the vertical position of the lower
15:12	Reserved Project: All	Format: MBZ
11:0	Sprite_Start_X-Position These 12 bits specify the horizontal offset in pixels of the be to the display surface. The offset must be even pixel aligne performing 180° rotation, this field specifies the horizontal p the start of the active display plane in the unrotated orientat	d for unrotated YUV formats. When osition of the lower right corner relative to



4.10.11DVSASURFLIVE—Video Sprite A Live Surface Base Address Register

Register T	vpe: MMIO							
-	ffset: 721ACh	-721AFh						
Project:	All							
Default Va	lue: 000000	e: 0000000h						
Access:	Read Only							
Size (in bit	t <mark>s):</mark> 32							
Bit		Description						
31:0	Sprite_Surfac	ce_Base_Address						
	Project:	All						
	Address:	GraphicsAddress[31:0]						
	This gives the	live value of the surface base address as being currently used for the plane.						



4.10.12DVSASCALE—Video Sprite A Scaler Control

DVSASCALE—Video Sprite A Scaler Control						
Register Type:	MMIO					
Address Offset:	72204h-72207h					
Project:	All					
Default Value:	0000000h					
Access:	R/W					
Size (in bits):	32					
Double Buffer Update Point:	Start of vertical blank or pipe disabled or sprite disabled, after armed					
Double Buffer Armed By:	Write to DVSASURF					

This register controls the sprite scaling. The DVSASIZE register gives the destination (output to pipe) size of the sprite. This register gives the source (input to sprite) size of the sprite. When scaling is enabled, the source size will be scaled up or down to the destination size.

Upscaling of any amount is allowed. Downscaling up to 16X (source/destination) is allowed. Downscaling greater than 2X will involve decimation. Downscaling increases memory bandwidth requirements. Scaling can not be used with the sprite 64bpp source pixel format. Source and destination sizes must be 3x3 (3x6 when interlacing) or greater when scaling is enabled.

Horizontal downscaling limits the maximum dot clock allowed as percent of cdclk. Rules to calculate the allowed dot clock:

Start with maximum dot clock 90% of cdclk. (There is a separate requirement that planes using 64bpp formats can not be enabled with dot clock >80% of cdclk. Subtract 10% more per horizontal decimation step (decimation steps at 2x, 4x, 8x, and 16x downscale).

Subtract 10% more if sprite is using the RGB data format.

Subtract 10% more if sprite scaling is enabled on the other pipe.

Then divide that by horizontal downscale amount within each decimation step.

The result is the maximum allowed dot clock as percent of cdclk frequency.

Example:

Scale factor	Decimation amount	YUV single pipe dot clock %	YUV dual pipe dot clock %	RGB single pipe dot clock %	RGB dual pipe dot clock %	Comment
1	1	90	80	80	70	No scaling
1.5	1	60	53	53	46	
1.99	1	45	40	40	35	Max downscale before decimation starts
2	2	80	70	70	60	
3	2	53	46	46	40	
3.99	2	40	35	35	30	
4	4	70	60	60	50	



		DVSA	SCALE-	–Video S	Sprite A	Scale	Control	
6		4	46	40	40	33		
7.99		4	35	30	30	25		
8		8	60	50	50	40		
12		8	40	33	33	26		
15.99		8	30	25	25	20	Worst case dot clock	
				_				
16		16	50	40	40	30	Max downscaling allow	ved
Bit					Description			
31	Scaling_EnableProject:AllFormat:EnableEnables the scaling function.Source width can be no more than 4k bytes. For best picture quality, disable when scaling is not required. When in Self Refresh Big FIFO mode, scaling enable will be masked off while Big FIFO mode is exiting.							
	masked o	off while Big	g FIFO mode	e is exiting.				
30:29	masked o	off while Big	g FIFO mode	e is exiting.				
30:29		off while Big	g FIFO mode	e is exiting.		-		
30:29	Filter_Co Project: Default Va	off while Big ontrol alue:	g FIFO mode	e is exiting.				
30:29	Filter_Co Project:	off while Big ontrol alue:	g FIFO mode	e is exiting.				
30:29	Filter_Co Project: Default Va	off while Big ontrol alue:	g FIFO mode All Ob	e is exiting.				Project
30:29	Filter_Co Project: Default Va Filter sele	off while Big ontrol alue: ection	g FIFO mode All Ob Desc	e is exiting.				
30:29	Filter_Co Project: Default V: Filter sele	off while Big ontrol alue: ection Name	g FIFO mode All Ob Desc Mediu	e is exiting.	iltering			Project
30:29	Filter_Co Project: Default Va Filter sele Value 00b	off while Big ontrol alue: ection Name Medium	g FIFO mode All Ob Desc Media ng Edge	e is exiting. r iption um Filtering	-		I	Project All
30:29	Filter_Co Project: Default Va Filter sele Value 00b 01b	off while Big ontrol alue: ection Name Medium Enhancin	g FIFO mode All Ob Desc Medii ng Edge g Edge	e is exiting. Fription um Filtering Enhancing Filt Softening Filt	-			Project All
30:29 28	Filter_Co Project: Default V Filter sele O0b 01b 10b 11b Even/Ode Project: Default V	off while Big ontrol alue: ection Name Medium Enhancin Softening Reserve d_Field_C alue: e vertical o	g FIFO mode All Ob Desc Medii ng Edge g Edge d Rese Vffset All Ob	e is exiting. ription um Filtering Enhancing Filt Softening Filt rved	tering	sponsible for		Project All All All All
	Filter_Co Project: Default V Filter sele Value 00b 01b 10b 11b Even/Ode Project: Default V Select the	off while Big ontrol alue: ection Name Medium Enhancin Softening Reserve d_Field_C alue: e vertical o	g FIFO mode All Ob Desc Mediu ng Edge g Edge d Rese Offset All Ob ffset of the fi	e is exiting. ription um Filtering Enhancing Filt Softening Filt rved Itered data. S	tering	sponsible for	updating this to match t	Project All All All All
	Filter_Co Project: Default V Filter sele 00b 01b 10b 11b Even/Ode Project: Default V Select the surface d	off while Big ontrol alue: ection Medium Enhancin Softening Reserve d_Field_C alue: e vertical o ata.	g FIFO mode All Ob Desc Mediu ng Edge d Rese Offset All Ob ffset of the fi	e is exiting. ription um Filtering Enhancing Filt Softening Filt rved Itered data. S	tering Software is res	sponsible for	updating this to match t	Project All All All All



27	Even/Odd_Field_Enable								
	Project:		All						
		Default Value: 0b							
	Enable adjustment of the vertical offset of the filtered data.								
	Value	Name	Description	Project					
	0b	Disable	Off (Vertical initial phase is 1/2 the scale factor)	All					
	1b	Enable	On (Vertical initial phase is selected by the Even/Off Field Offset bit)	All					
26:16	Source_	Width	Project: All Format:						
			f the source image to be scaled in pixels. Max number of pixels is 2048;	minimum					
	4k bytes,	counting fro	rammed is one less than the number of pixels. Source width can be no r om a 64 byte alignment. The sprite width (actual width, not the width min ven values when YUV source pixel format is used.						
15:11	4k bytes,	counting fro	om a 64 byte alignment. The sprite width (actual width, not the width min ven values when YUV source pixel format is used.						
15:11 10:0	4k bytes, value) is	counting fro limited to ev d Proje	om a 64 byte alignment. The sprite width (actual width, not the width min ven values when YUV source pixel format is used.						
	4k bytes, value) is Reserved Source_ The verti lines in th	counting fro limited to ev d Proje Height cal size of t ne field. Ma	om a 64 byte alignment. The sprite width (actual width, not the width min ven values when YUV source pixel format is used. ect: All Format: MBZ	number of					

4.10.13 DVSAGAMC—Video Sprite A Gamma Correction Registers

DVSGAMC Reference Point								
Project:	All							
Bit		Description						
31:30	Reserved	Project: All Format:						
29:20	Red Gamma Reference Point	Project: All Format:						
19:10	Green Gamma Reference Point	Project: All Format:						
9:0	Blue Gamma Reference Point	Project: All Format:						

	DVSGAMC Max Reference Point						
Project:	All						
Bit		Description					
31:11	Reserved Project: All	Format:					
10:0	Final Gamma Max Reference Point	Project: All Format:					



DVSAGAMC—Video Sprite A Gamma Correction Registers

Register Type:	MMIO
Address Offset:	72300h-7234Bh
Project:	All
Default Value:	00000000h; 04010040h; 08020080h; 0C0300C0h; 10040100h; 14050140h; 18060180h; 1C0701C0h; 20080200h; 24090240h; 280A0280h; 2C0B02C0h; 300C0300h; 340D0340h; 380E0380h; 3C0F03C0h; 00000400h; 00000400h; 00000400h;
Access:	R/W
Size (in bits):	19x32

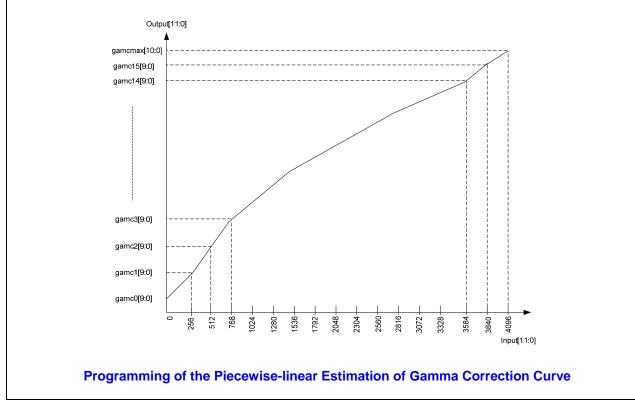
These registers are used to determine the characteristics of the gamma correction for the sprite pixel data *pre-blending*. Additional gamma correction can be done in the display pipe gamma if desired.

The gamma correction curve is represented by specifying a set of reference points spaced equally along the desired curve. Red, Green, and Blue each have 17 reference points. The first 16 reference points are 10 bit values with Red, Green, and Blue sharing a single register for each point. The final max reference point is an 11 bit value with separate registers for Red, Green, and Blue. The curve must be flat or increasing, never decreasing.

During operation the appropriate reference point pairs (adjacent) are selected for each color, and the output is interpolated between these two reference point values.

The gamma correction registers are not double-buffered. They should only be updated when the sprite is off, otherwise, screen artifacts may show.

To pass sprite pixel data through gamma correction unchanged, program the gamma reference points to the default linear ramp values. When the output from sprite is set in YUV format by programming CSC bypass, the sprite gamma correction will be bypassed.





I	DVSAG	GAMC—Vide	o Sprite /	A Ga	imma Co	prrection Registers
DWord	Bit				Description	
0	31:0	GAMC0	Project:	All	Format:	DVSGAMC Reference Point
1	31:0	GAMC1	Project:	All	Format:	DVSGAMC Reference Point
2	31:0	GAMC2	Project:	All	Format:	DVSGAMC Reference Point
3	31:0	GAMC3	Project:	All	Format:	DVSGAMC Reference Point
4	31:0	GAMC4	Project:	All	Format:	DVSGAMC Reference Point
5	31:0	GAMC5	Project:	All	Format:	DVSGAMC Reference Point
6	31:0	GAMC6	Project:	All	Format:	DVSGAMC Reference Point
7	31:0	GAMC7	Project:	All	Format:	DVSGAMC Reference Point
8	31:0	GAMC8	Project:	All	Format:	DVSGAMC Reference Point
9	31:0	GAMC9	Project:	All	Format:	DVSGAMC Reference Point
10	31:0	GAMC10	Project:	All	Format:	DVSGAMC Reference Point
11	31:0	GAMC11	Project:	All	Format:	DVSGAMC Reference Point
12	31:0	GAMC12	Project:	All	Format:	DVSGAMC Reference Point
13	31:0	GAMC13	Project:	All	Format:	DVSGAMC Reference Point
14	31:0	GAMC14	Project:	All	Format:	DVSGAMC Reference Point
15	31:0	GAMC15	Project:	All	Format:	DVSGAMC Reference Point
16	31:0	GAMCmaxR	Project:	All	Format:	DVSGAMC Max Reference Point
17	31:0	GAMCmaxG	Project:	All	Format:	DVSGAMC Max Reference Point
18	31:0	GAMCmaxB	Project:	All	Format:	DVSGAMC Max Reference Point

4.11 Video Sprite B Control

The DVSBCNTR, DVSBSTRIDE, DVSBPOS, DVSBSIZE, and DVSBSCALE active registers will be updated on the vertical blank or when pipe is disabled, after the DVSBSURF trigger register is written, or when the sprite B is not yet enabled – thus providing an atomic update of the video sprite B control, stride, position, size, scale, and base address registers.



4.11.1 DVSBCNTR—Video Sprite B Control Register

Register	Туре:		MMIO	
Address			73180h-73183h	
Project:			All	
Default V	alue:		0000000h	
Access:			R/W	
Size (in b		_	32	
	uffer Update		Start of vertical blank or pipe disabled or sprite disabled, after armed	
	uffer Armed		Write to DVSBSURF cted to pipe B only.	
lueo Spi				
Bit			Description	
31	Sprite_E	nable	Project: All Format: Enable	
	memory f the plane	etches cea . When in S	the sprite plane will generate pixels for display. When set to zero, sprite se and plane output is transparent. The display pipe must be enabled t Self Refresh Big FIFO mode, write to this register to enable the plane wi and delayed while Big FIFO mode is exiting.	o enable
30	-			
30	Gamma_	Enable		
30	Gamma_ Project:	Enable	All	
30	Project: Default V	alue:	Ob	he damma
30	Project: Default V There are correction this displ the defau	alue: e two gamm n in the disp ay plane. C ilt values in	0b na adjustments possible in the video sprite data path. This bit controls to play pipe not the gamma control in this plane. It affects only the pixel da Gamma correction logic that is contained in the video sprite is disabled b to those registers.	ata from by loading
30	Project: Default V There are correction this displi- the defau	alue: e two gamm n in the disp ay plane. C ilt values in Name	0b na adjustments possible in the video sprite data path. This bit controls t play pipe not the gamma control in this plane. It affects only the pixel da Gamma correction logic that is contained in the video sprite is disabled b	ata from by loading Project
30	Project: Default V There are correction this displ the defau	alue: e two gamm n in the disp ay plane. C ilt values in	0b na adjustments possible in the video sprite data path. This bit controls to play pipe not the gamma control in this plane. It affects only the pixel da Gamma correction logic that is contained in the video sprite is disabled b to those registers.	ata from by loading
30	Project: Default V There are correction this displi- the defau	alue: e two gamm n in the disp ay plane. C ilt values in Name	Ob na adjustments possible in the video sprite data path. This bit controls t play pipe not the gamma control in this plane. It affects only the pixel da Gamma correction logic that is contained in the video sprite is disabled b to those registers.	ata from by loading Project
29	Project: Default V There are correction this displative the defau	alue: e two gamm n in the disp ay plane. C ilt values in Name Disable Enable	Ob na adjustments possible in the video sprite data path. This bit controls to play pipe not the gamma control in this plane. It affects only the pixel data Gamma correction logic that is contained in the video sprite is disabled to those registers. Description Plane pixel data bypasses the display pipe gamma correction logic Plane pixel data is gamma corrected in the pipe gamma correction logic	Ata from by loading Project All All
	Project: Default V There are correction this displi- the defau Value 0b 1b Reserved	alue: e two gamm n in the disp ay plane. C llt values in Name Disable Enable Enable	Ob na adjustments possible in the video sprite data path. This bit controls to play pipe not the gamma control in this plane. It affects only the pixel data Gamma correction logic that is contained in the video sprite is disabled to those registers. Description Plane pixel data bypasses the display pipe gamma correction logic Plane pixel data is gamma corrected in the pipe gamma correction logic	Ata from by loading Project All All
29	Project: Default V There are correction this displi- the defau Value 0b 1b Reserved	alue: e two gamm n in the disp ay plane. C llt values in Name Disable Enable Enable	Ob na adjustments possible in the video sprite data path. This bit controls to play pipe not the gamma control in this plane. It affects only the pixel data Gamma correction logic that is contained in the video sprite is disabled to those registers. Description Plane pixel data bypasses the display pipe gamma correction logic Plane pixel data is gamma corrected in the pipe gamma correction logic ect: All Format: MBZ	Ata from by loading Project All All
29	Project: Default V There are correction this displative the defau 0b 1b Reserved YUV_By	alue: e two gamm n in the disp ay plane. C ilt values in Name Disable Enable Enable d Proje	Ob na adjustments possible in the video sprite data path. This bit controls to play pipe not the gamma control in this plane. It affects only the pixel data Gamma correction logic that is contained in the video sprite is disabled to those registers. Description Plane pixel data bypasses the display pipe gamma correction logic Plane pixel data is gamma corrected in the pipe gamma correction logic ect: All Format: MBZ ess-512_Format_Conversion	Ata from by loading Project All All
29	Project: Default V There are correction this displi- the defau Value 0b 1b Reserved YUV_Byp Project:	alue: e two gamm n in the disp ay plane. C ilt values in Name Disable Enable Enable d Proje	Ob na adjustments possible in the video sprite data path. This bit controls to play pipe not the gamma control in this plane. It affects only the pixel data Gamma correction logic that is contained in the video sprite is disabled to those registers. Description Plane pixel data bypasses the display pipe gamma correction logic Plane pixel data is gamma corrected in the pipe gamma correction logic ect: All Format_Conversion All	Ata from by loading Project All All
29	Project: Default V There are correction this displ- the defau 0b 1b Reserved YUV_Byp Project: Default V	alue: e two gamm n in the disp ay plane. O ilt values in Disable Enable d Proje pass_Exce alue:	Ob na adjustments possible in the video sprite data path. This bit controls to play pipe not the gamma control in this plane. It affects only the pixel data Gamma correction logic that is contained in the video sprite is disabled to those registers. Description Plane pixel data bypasses the display pipe gamma correction logic Plane pixel data is gamma corrected in the pipe gamma correction logic ect: All Format MBZ ss-512_Format_Conversion All Ob	Ata from by loading Project All All



	_	orrection_	Disable			
	Project:		All			
	Default V		0b			
	expanded	to full rang	e RGB, setting th	e correction logic. Normally the range compress is bit will generate range compressed RGB. T rial is used. This bit has no effect on RGB sou	his bit sho	uld also
	Value	Name	Description	F	Project	
	0b	Enable	Range correctio	n enabled	All	
	1b	Disable	No range correct	tion /	4II	
26:25	Source_I	Pixel_Form	at			
	Project:		DevSNB			
	Default V	alue:	0b			
		selects the to 12 bits		e sprite. Before entering the blender, each so	ource forma	it is
	Value	Name		Description		Projec
	00b	YUV 4:2:	2	YUV 4:2:2 packed pixel format (byte order programmed separately)		All
	01b	RGB 32-t	bit 2:10:10:10	RGB 32-bit 2:10:10:10 pixel format (color order programmed separately). Ignore alpha.		All
	10b	RGB 32-ł	bit 8:8:8:8	RGB 32-bit 8:8:8:8 pixel format (color order programmed separately). Ignore alpha.		All
	11b	RGB 64-b	oit 16:16:16:16	RGB 64-bit 16:16:16:16 floating point pixel f		All
		limit the n	bpp format will naximum dot 0% of cdclk.	(color order programmed separately). Ignor	re alpha.	
	Pipe_Col	or_Space	Conversion_Ena	able		
24	Project:		All			
24	Default V	alue:	0b			
24				version for the plane pixel data. This is separa e. CSC mode in the pipe CSC registers must	be set to m	
24	conversio			the color conversion logic within the sprite pla	ano.	
24	conversio			the color conversion logic within the sprite pla		Project
24	conversion the formation	at of the pla	ne pixel data after Description	bypasses the pipe color space conversion log		Project All



22	Sprite_S	ource_Key	/_Enable				
	Project:		All				
	Default V	alue:	Ob				
			rce color keying. Sprite pixel values that match (vertice key can not be enabled if destination key is enabled		ill become		
	Value	Name	Description	Project			
	0b	Disable	Sprite source key is disabled	All			
	1b	Enable	Sprite source key is enabled	All			
22	Sprite_S	ource_Key	r_Enable				
	Project:		All				
	Default V						
	Default Value: 0b This bit enables source color keying. Sprite pixel values that match (within range) the key will transparent. Source key can not be enabled if destination key is enabled.						
		nables soul	rce color keying. Sprite pixel values that match (w		ll become		
		nables soul	rce color keying. Sprite pixel values that match (w		Il become		
	transpare	nables sour nt. Source	rce color keying. Sprite pixel values that match (w key can not be enabled if destination key is enab		1		
	transpare Value	nables sour nt. Source	rce color keying. Sprite pixel values that match (w key can not be enabled if destination key is enab Description		Project		
21	transpare Value 0b	nables sour nt. Source	rce color keying. Sprite pixel values that match (w key can not be enabled if destination key is enab Description Sprite source key is disabled Sprite source key is enabled		Project		
21 20	transpare Value 0b 1b Reserved	nables sour nt. Source Name	rce color keying. Sprite pixel values that match (w key can not be enabled if destination key is enab Description Sprite source key is disabled Sprite source key is enabled		Project		
	transpare Value 0b 1b Reserved	nables sour nt. Source Name Proje	rce color keying. Sprite pixel values that match (w key can not be enabled if destination key is enab Description Sprite source key is disabled Sprite source key is enabled		Project		
	transpare Value 0b 1b Reserved RGB_Co	Name Name Proje	rce color keying. Sprite pixel values that match (we key can not be enabled if destination key is enabled Description Sprite source key is disabled Sprite source key is enabled ect: DevSNB		Project		
	transpare Value 0b 1b Reserved RGB_Co Project: Default V	Name Name Name Nor Projute Nor Order Naue: Name Name Name Name Name Name Name Name	rce color keying. Sprite pixel values that match (w key can not be enabled if destination key is enab Description Sprite source key is disabled Sprite source key is enabled ect: DevSNB DevSNB	led.	Project All All		
	transpare Value 0b 1b Reserved RGB_Co Project: Default V This field	Name Name Name Nor Projute Nor Order Naue: Name Name Name Name Name Name Name Name	rce color keying. Sprite pixel values that match (w key can not be enabled if destination key is enab Description Sprite source key is disabled Sprite source key is enabled ect: DevSNB DevSNB Ob	led.	Project All All		
	transpare Value 0b 1b Reserved RGB_Co Project: Default V This field is ignored	Name Name Name Name Nor_Order Naue: Name Name Name Name Name Name Name Name	rce color keying. Sprite pixel values that match (w key can not be enabled if destination key is enab Description Sprite source key is disabled Sprite source key is enabled ect: DevSNB DevSNB 0b select the color order when using RGB data formation	Ied.	Project All All		



			NTR—Video Sprite B Control Register	
19		onversion_		
	Project:		All	
	Default V		Ob	
		to be used	disables the color conversion logic internal to the sprite. Color con with the formats that support YUV format. This bit is ignored whe	
	Value	Name	Description	Project
	0b	Enable	Pixel data is sent through the sprite color conversion logic (only applies to YUV formats)	/ All
	1b	Disable	Pixel data is not sent through the sprite YUV->RGB color conve logic.	ersion All
18	YUV_For	mat		
	Project:		All	
	Default V	alue:	Ob	
			e source YUV format for the YUV to RGB color conversion operati e data is RGB.	ion. This field is
	-			
	Value	Name		roject
	Value Ob	Name BT.601		-
			Description	1
17:16	0b	BT.601 BT.709	Description Pr ITU-R Recommendation BT.601 Al	1
17:16	0b 1b	BT.601 BT.709	Description Pr ITU-R Recommendation BT.601 Al	1
17:16	0b 1b YUV_Byt	BT.601 BT.709	DescriptionPrITU-R Recommendation BT.601AIITU-R Recommendation BT.709AI	1
17:16	0b 1b YUV_Byt Project: Default V	BT.601 BT.709 te_Order alue:	Description Pr ITU-R Recommendation BT.601 AI ITU-R Recommendation BT.709 AI	-
17:16	0b 1b YUV_Byt Project: Default V This field	BT.601 BT.709 te_Order alue:	Description Provide the system ITU-R Recommendation BT.601 All ITU-R Recommendation BT.709 All All Ob select the byte order when using YUV 4:2:2 data formats. For other select the byte order when using YUV 4:2:2 data formats.	-
17:16	0b 1b YUV_Byt Project: Default V This field field is ig	BT.601 BT.709 te_Order alue: I is used to nored.	Description Provide the system ITU-R Recommendation BT.601 All ITU-R Recommendation BT.709 All All Ob select the byte order when using YUV 4:2:2 data formats. For other select the byte order when using YUV 4:2:2 data formats.	ner formats, this
17:16	0b 1b YUV_Byt Project: Default V This field field is ig Value	BT.601 BT.709 te_Order alue: I is used to nored. Name	Description Provide the second se	ner formats, this
17:16	0b 1b YUV_Byt Project: Default V This field field is ig Value 00b	BT.601 BT.709 BT.709 BE_Order alue: l is used to nored. Name YUYV	Description Presentation ITU-R Recommendation BT.601 Al ITU-R Recommendation BT.709 Al All Ob select the byte order when using YUV 4:2:2 data formats. For other other when using YUV 4:2:2 data formats. For other YUYV (8:8:8:8 MSB-V:Y_2:U:Y_1)	roject



15		play_Rota	NTR—Video Sprite B Control Registe		
	Project:	p	All		
	Default V	alue:	Ob		
	the surfa	ce address	ne plane to be rotated 180°. In addition to setting this bit, soft offset to the lower right corner of the unrotated and unscaled ative to the lower right corner.	ware must a l image and	also set I calculate
	Value	Name	Description	Project	
	0b	None	No rotation	All	
	1b	180	180° rotation	All	
14	Trickle-F	eed_Enab	le		
	Project:		DevSNB		
	Default V	alue:	0b		
	Value	Name	Description		Project
	0b	Enable	Trickle Feed Enabled - Data requests are sent whenever th space in the Display Data Buffer	ere is	All
	1b	Disable	Trickle Feed Disabled - Data requests are sent in bursts.		All
13:11	Reserved	d Proj	ect: All Format	:	
10	Tiled_Su	rface			
	Project:		All		
	Default V	alue:	Ob		
			at the surface data is in tiled memory. The tile pitch is specifie ter. Only X tiling is supported for display surfaces.	d in bytes i	n the
	When thi registers.		it affects the hardware interpretation of the DVSBSTART and	DVSBSUR	FADDR
	Value	Name	Description	Project	
	0b	Linear	Linear memory	All	
	1b	Tiled	Tiled memory	All	



2	Sprite_D	estination_	_Кеу	
	Project:		All	
	Default V	alue:	0b	
	key value	e in DVSBK	destination key function. If the pixel for the prin EYVAL the sprite pixel is used, otherwise the p	primary plane pixel is passed
	key value	e in DVSBK		primary plane pixel is passed
	key value through t	e in DVSBK he blender	EYVAL the sprite pixel is used, otherwise the punmodified. Destination Key can not be enable	primary plane pixel is passed ed if source key is enabled.

See DVSACNTR - Sprite Source Pixel Format Mapping of Bits to Colors

4.11.2 DVSBLINOFF—Video Sprite B Linear Offset Register

Register Type	:	MMIO		
Address Offse	et:	73184h-7318	7h	
Project:		All		
Default Value:		00000000h		
Access:		R/W		
Size (in bits):		32		
Double Buffer	Update Point:	Start of vertica	al blank (or pipe disabled
Bit				Description
31:0 S	prite_Linear_Offse	t Project:	All	Format:
su al pe lir	urface address to ge igned for unrotated erforming 180° rotat	t the address RGB formats a ion, the unpan a in its unrotat	of the first and ever aned offs aned orient	te offset into the sprite plane. This value is added to the st pixel to be displayed. This offset must be at least pixel n pixel aligned for unrotated YUV formats. When et must be the difference between the last pixel of the last tation and the display surface address. When the surface red.



4.11.3 DVSBSTRIDE—Video Sprite B Stride Register

Register T	ype:	MMIO		
Address O	Offset:	73188h-7318E	Bh	
Project:		All		
Default Va	lue:	00000000h		
Access:		R/W		
Size (in bit	ts):	32		
Double Bu	Iffer Update Point:	Start of vertica	l blank or	pipe disabled or sprite disabled, after armed
Double Bu	Iffer Armed By:	Write to DVSB	SURF	
Bit				Description
31:15	Reserved Pro	ject: All		Format:
14:6	Sprite_Stride	Project:	All	Format:
	When using tiled makes the command packet pa	emory, this must assed through the K bytes when sp	be 512 by e comma rite scalir	n using linear memory, this must be 64 byte aligned. yte aligned. This register is updated through either a nd stream or writes to this register. The stride is limited ng is not enabled, 4K bytes when sprite scaling is

4.11.4 DVSBPOS—Video Sprite B Position Register

			o Sprite B Positio	Shinegister	
Register 1	Гуре:	MMIO			
Address (Offset:	7318Ch-7318Fh			
Project:		All			
Default Va	alue:	0000000h			
Access:		R/W			
Size (in bi	ts):	32			
Double B	uffer Update Point:	Start of vertical b	lank or pipe disabled or sp	rite disabled, after a	rmed
Double B	uffer Armed By:	Write to DVSBSL	JRF, DVSAPOS write does	s not disarm	
		Xposition + Xsize	Software must take car	re that the sprite o	loes not extend out
ot the disp	nay active area. le.				
of the disp Bit			Description		
		ject: All		Format:	MBZ
Bit		ject: All		Format:	MBZ



DVSBPOS—Video Sprite B Position Register						
15:12	Reserved Project	t: All			Format:	MBZ
11:0	Sprite_X-Position	Project:	All	Format:		
	These 12 bits specify beginning of the active position of the original unrotated orientation. displayable area of the	video area. V lower right co The defined s	Vhen per rner relat prite rect	forming 180° rotat ive to the original	ion, this field specifies end of the active video	the horizontal o area in the

4.11.5 DVSBSIZE—Video Sprite B Size Register

	DVS	BSIZE-	-Vid	eo Sprite B S	Size Register	
Register Ty	/pe:	MMIO				
Address O		73190h-73	8193h			
Project:		All				
Default Val	ue:	00000000	n			
Access:		R/W				
Size (in bit	s):	32				
Double But	fer Update Point:	Start of ve	rtical bl	ank or pipe disabled	or sprite disabled, after a	rmed
Double But	fer Armed By:	Write to D	VSBSU	RF		
	active area. ie. Xp				are that the sprite does	
Bit				Description		
31:28	Reserved Pro	ject: All			Format:	MBZ
27:16	Sprite_Height	Project:	All	Format:		
		he defined s	prite re		n lines. The value in the i be completely contained	
15:12	Reserved Pro	ject: All			Format:	MBZ
11:0	Sprite_Width	Project:	All	Format:		
	same as the stride	but should be. The define	e less tl d sprite	han or equal to the s	n pixels. This does not ha tride in pixels. The value ays be completely contair	in the register is
					e) is limited to even value ixel doubling or Pixel doul	



4.11.6 DVSBKEYVAL—Video Sprite B Color Key Value Register

	DVSBKEYVA	L—Video Sp	rite B Color K	ey Value F	Reg	ister
Register Ty	/pe:	MMIO				
Address O		73194h-73197h				
Project:		All				
Default Val	ue:	00000000h				
Access:		R/W				
Size (in bits):		32				
Double But	ffer Update Point:	Start of vertical blan	k or pipe disabled			
matches th	e key. This register value is the minimum	will only have an e	h the mask bits to de ffect when the sprite e compare. In desti	color key is en	ableo	d. In source key
Bit			Description			
31:24	Reserved Proj	ect: All		Forma	at:	MBZ
23:16	V_Source_Key_Mir	_Value/R_Source/D	est_Key_Value	Project:	All	Format:
	Specifies the color k or destination key co		or the sprite V channel	source key or th	e Rec	d channel source
15:8	Y_Source_Key_Mir	_Value/G_Source/D	est_Key_Value	Project:	All	Format:
	Specifies the color k source or destination		or the sprite Y channel	source key or th	e Gre	en channel
7:0	U_Source_Key_Mir	_Value/B_Source/D	est_Key_Value	Project:	All	Format:
	Specifies the color ker source or destination	•	or the sprite U channel	source key or th	e Blu	e channel



4.11.7 DVSBKEYMSK—Video Sprite B Color Key Mask Register

DVSBKEYM	SK—Video Sprite B Color Key Mask Register
Register Type:	ММІО
Address Offset:	73198h-7319Bh
Project:	All
Default Value:	0000000h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe disabled
Double Buffer Update Point:	Start of vertical blank or pipe disabled

For source key this register specifies which channels to perform range checking on.

For destination key this register specifies the key mask to be used with the color value bits to determine if the display source data matches the key when enabled. A zero bit in the mask indicates that the corresponding bit match failure should be ignored when determining if the pixel matches.

Note that source key and destination key are mutually exclusive modes of operation, they can not be used simultaneously. For the function that is not enabled, the associated bits in this register should be programmed to zeroes.

Bit	Description			
31:27	Reserved Project: All	Forma	at:	MBZ
26	V/R_Channel_Source_Key_Enable Specifies the source color key enable for the V/Red channel	Project:	All	Format:
25	Y/G_Channel_Source_Key_Enable Specifies the source color key enable for the Y/Green channel	Project:	All	Format:
24	U/B_Channel_Source_Key_Enable Specifies the source color key enable for the U/Blue channel	Project:	All	Format:
23:16	R_mask_Dest_Key_Value Specifies the destination color key mask for the sprite R channel	Project:	All	Format:
15:8	G_mask_Dest_Key_Value Specifies the destination color key mask for the sprite G channel	Project:	All	Format:
7:0	B_mask_Dest_Key_Value Specifies the destination color key mask for the sprite B channel	Project:	All	Format:

Γ



4.11.8 DVSBSURF—Video Sprite B Surface Address Register

	DVSBSU	RF—Video Spri	te B Surface Address Register				
Register Ty	/pe:	MMIO					
Address O	ffset:	7319Ch-7319Fh					
Project:		All					
Default Value:		0000000h	0000000h				
Access:		R/W	R/W				
Size (in bit	s):	32					
Double But	ffer Update Point	: Start of vertical blar	nk or pipe disabled				
Writes to the	nis register arm D	OVSB registers					
Bit	Description						
31:12	Sprite_Surface	Base_Address					
	Project:	All					
	Address:	GraphicsAddress	[31:12]				
	(x, y) offsets in t		address. When the surface is tiled, panning is specified using er. When the surface is in linear memory, panning is BLINOFF register.				
This address must be 4K aligned. It represents an offset from the graphics memory aperture base is mapped to physical pages through the global GTT. The value in this register is updated through command streamer with synchronous flips.							
11:0	Reserved	Project: All	Format:				

4.11.9 DVSBKEYMAXVAL—Video Sprite B Color Key Max Value Register

Register Type	:	MMIO	
Address Offse	et:	731A0h-731A3h	
Project:		All	
Default Value:	:	0000000h	
Access:		R/W	
Size (in bits): Double Buffer Update Point:		32	
		Start of vertical blank or pipe disabled	
•			the sprite source color key is enabled.
•			the sprite source color key is enabled.
Bit	ey. This register	r will only have an effect when	the sprite source color key is enabled.
Bit 31:24 R	ey. This register	r will only have an effect when Descri ject: All	the sprite source color key is enabled.



DVS	DVSBKEYMAXVAL—Video Sprite B Color Key Max Value Register						
15:8	Y_Key_Max_Value Specifies the color key value for the sprite Y channel	Project:	All	Format:			
7:0	U_Key_Max_Value Specifies the color key value for the sprite U channel	Project:	All	Format:			

4.11.10DVSBTILEOFF—Video Sprite B Tiled Offset Register

Register Type:	ММІО
Address Offset:	731A4h-731A7h
Project:	All
Default Value:	0000000h
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Double Buffer Update Point:	Start of vertical blank or pipe disabled

This register specifies the panning for the sprite surface in tiled memory. The surface base address is specified in the DVSBSURFADDR register, and this register is used to describe an offset from that base address. When the surface is in linear memory, the offset is specified in the DVSBLINOFF register and the contents of this register are ignored. When the surface is tiled, the start position is specified in this register as an (x, y) offset from the beginning of the surface.

Bit	Description	
31:28	Reserved Project: All	Format: MBZ
27:16	Sprite_Start_Y-Position	Project: All Format:
	These 12 bits specify the vertical position in lines of the beginnir the display surface. When performing 180° rotation, this field sp right corner relative to the start of the active display plane in the	becifies the vertical position of the lower
15:12	Reserved Project: All	Format: MBZ
11:0	Sprite_Start_X-Position	Project: All Format:
	These 12 bits specify the horizontal offset in pixels of the beginn to the display surface. The offset must be even pixel aligned for performing 180° rotation, this field specifies the horizontal position the start of the active display plane in the unrotated orientation.	unrotated YUV formats. When



4.11.11DVSBSURFLIVE—Video Sprite B Live Surface Base Address Register

DVSBSURFLIVE—Video Sprite B Live Surface Base Address Register

Register Ty	ype:	MMIO			
Address O	ffset:	731ACh-731AF	ĥ		
Project:		All			
Default Val	ue:	0000000h			
Access:		Read Only			
Size (in bit	s):	32			
Bit	it Description				
31:0	Sprit	e_Surface_Bas	e_Address		
	Proje	ct:	All		
	Addr	ess:	GraphicsAddress[31:0]		
	This	gives the live val	ue of the surface base address as being currently used for the plane.		
	L				

4.11.12DVSBSCALE—Video Sprite B Scaler Control

DVSB	DVSBSCALE—Video Sprite B Scaler Control			
Register Type:	MMIO			
Address Offset:	73204h-73207h			
Project:	All			
Default Value:	0000000h			
Access:	R/W			
Size (in bits):	32			
Double Buffer Update Point:	Start of vertical blank or pipe disabled or sprite disabled, after armed			
Double Buffer Armed By:	Write to DVSBSURF			

This register controls the sprite scaling. The DVSBSIZE register gives the destination (output to pipe) size of the sprite. This register gives the source (input to sprite) size of the sprite. When scaling is enabled, the source size will be scaled up or down to the destination size.

Upscaling of any amount is allowed. Downscaling up to 16X (source/destination) is allowed. Downscaling greater than 2X will involve decimation. Downscaling increases memory bandwidth requirements. Scaling can not be used with the sprite 64bpp source pixel format. Source and destination sizes must be 3x3 (3x6 when interlacing) or greater when scaling is enabled.

Horizontal downscaling limits the maximum dot clock allowed as percent of cdclk. See DVSASCALE for the rules to calculate the allowed dot clock.

Bit				Description	
31	Scaling_Enable	Project:	All	Format:	Enable
		is not required.	. When ir		than 4k bytes. For best picture quality, Big FIFO mode, scaling enable will be



	-	DA2R2	SCALE—Video Sprite B Scaler Control				
30:29	Filter_Co Project: Default V Filter sele	alue:	All Ob				
	Value	Name	Description	Project			
	00b Medium		Medium Filtering	All			
	01b	Enhancin	g Edge Enhancing Filtering	All			
	10b	Softening	Edge Softening Filtering	All			
	11b Reserved		Reserved	All			
28	28 Even/Odd_Field_Offset Project: All Default Value: 0b Select the vertical offset of the filtered data. Software is responsible for updating this to match surface data.						
	Value	Name	Description	Project			
	0b	0	Vertical initial phase of 0	All			
	1b	0.5	Vertical initial phase of 0.5	All			
27	Project: Default V	Even/Odd_Field_Enable Project: All Default Value: Ob Enable adjustment of the vertical offset of the filtered data.					
	Value	Name	Description Proje				
	Ob Disable Off (Vertical initial phase is 1/2 the scale factor)			All			
	1b	Enable	On (Vertical initial phase is selected by the Even/Off Field Offset bit)	All			
26:16	Source_WidthProject:AllFormat:The horizontal size of the source image to be scaled in pixels.Max number of pixels is 2048; minimumis 3. The value programmed is one less than the number of pixels.Source width can be no more than4k bytes, counting from a 64 byte alignment.The sprite width (actual width, not the width minus one value) is limited to even values when YUV source pixel format is used.						
15:11	Reserved	d Proje	ect: All Format: MBZ				
	Source_HeightProject:AllFormat:The vertical size of the source image to be scaled in lines. If the source is a field, this is the number of lines in the field. Max number of lines is 2048; minimum is 3 (6 when interlacing). The value programmed is one less than the number of lines.The height must be even when sprite scaling is enabled and the pipe has set planes to interlaced fetch.						

(intel)

4.11.13 DVSBGAMC—Video Sprite B Gamma Correction Registers

DVSBGAMC—Video Sprite B Gamma Correction Registers

Register Type:	MMIO
Address Offset:	73300h
Project:	All
Default Value:	00000000h; 04010040h; 08020080h; 0C0300C0h; 10040100h; 14050140h; 18060180h; 1C0701C0h; 20080200h; 24090240h; 280A0280h; 2C0B02C0h; 300C0300h; 340D0340h; 380E0380h; 3C0F03C0h; 00000400h; 00000400h; 00000400h;
Access:	R/W
Size (in bits):	19x32

See Video Sprite A description

	1	T				
DWord	Bit				Description	
0	31:0	GAMC0	Project:	All	Format:	DVSGAMC Reference Point
1	31:0	GAMC1	Project:	All	Format:	DVSGAMC Reference Point
2	31:0	GAMC2	Project:	All	Format:	DVSGAMC Reference Point
3	31:0	GAMC3	Project:	All	Format:	DVSGAMC Reference Point
4	31:0	GAMC4	Project:	All	Format:	DVSGAMC Reference Point
5	31:0	GAMC5	Project:	All	Format:	DVSGAMC Reference Point
6	31:0	GAMC6	Project:	All	Format:	DVSGAMC Reference Point
7	31:0	GAMC7	Project:	All	Format:	DVSGAMC Reference Point
8	31:0	GAMC8	Project:	All	Format:	DVSGAMC Reference Point
9	31:0	GAMC9	Project:	All	Format:	DVSGAMC Reference Point
10	31:0	GAMC10	Project:	All	Format:	DVSGAMC Reference Point
11	31:0	GAMC11	Project:	All	Format:	DVSGAMC Reference Point
12	31:0	GAMC12	Project:	All	Format:	DVSGAMC Reference Point
13	31:0	GAMC13	Project:	All	Format:	DVSGAMC Reference Point
14	31:0	GAMC14	Project:	All	Format:	DVSGAMC Reference Point
15	31:0	GAMC15	Project:	All	Format:	DVSGAMC Reference Point
16	31:0	GAMCmaxR	Project:	All	Format:	DVSGAMC Max Reference Point
17	31:0	GAMCmaxG	Project:	All	Format:	DVSGAMC Max Reference Point
18	31:0	GAMCmaxB	Project:	All	Format:	DVSGAMC Max Reference Point
18	31:0	GAMCmaxB	Project:	All	Format:	DVSGAMC Max Reference Point



Revision History

Revision Number	Description	Revision Date
1.0	First 2011 OpenSource edition	May 2011

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