



Open Graphics Programming Manual

Chrome9 HD Graphics Processor

VX900 Series
System Processor

Part II: 3D / Video

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TABLE OF CONTENTS

REVISION HISTORY	I
TABLE OF CONTENTS.....	II
LIST OF TABLES	IV
INTRODUCTION.....	1
ABOUT THIS PROGRAMMING GUIDE	1
VIDEO REGISTERS.....	3
VIDEO REGISTER SUMMARY	3
VIDEO DISPLAY ENGINE REGISTER DESCRIPTIONS (200-12F0H)	10
DVD / VIDEO CONTROL REGISTER (3260-326CH)	35
VIDEO CAPTURE ENGINE REGISTER DESCRIPTIONS (300-37CH)	36
HQV ENGINE REGISTER DESCRIPTIONS (380-3FFH).....	44
HQV REGISTERS.....	55
HQV REGISTER SUMMARY	55
HQV ENGINE REGISTER DESCRIPTIONS	57
HQV Engine Control (370-3FFh).....	57
COMMAND REGULATOR (CR) REGISTERS.....	69
SETTINGS OF 3D/CR REGISTERS	70
HPARATYPE 00H: PRIMITIVE VERTEX DATA OR VERTEX INDEX.....	73
HPARATYPE 10H: COMMANDS FOR COMMAND REGULATOR.....	74
Sub-Address (Bits [31:24]): 00-74h	74
HPARATYPE 11H: COMMANDS FOR COMMAND REGULATOR.....	81
Sub-Address (Bits [31:24]): 00-6Bh.....	81
3D REGISTERS.....	88
HPARATYPE 00H: PRIMITIVE VERTEX DATA OR VERTEX INDEX.....	89
HPARATYPE 01H: ATTRIBUTE OTHER THAN TEXTURE.....	90
Sub-Address (Bits [31:24]): 00-AAh	90
HPARATYPE 02H: ATTRIBUTE OF TEXTURE STAGE N (HPARASUBTYPE: 00-0FH)	121
Sub-Address (Bits [31:24]): 00-51h	121
HPARATYPE 02H: ATTRIBUTE OF TEXTURE SAMPLE STAGE N (HPARASUBTYPE: 20-2FH).....	129
Sub-Address (Bits [31:24]): 00-51h	129
HPARATYPE 02H: ATTRIBUTE OF TEXTURE STAGE N (HPARASUBTYPE: FEH)	133
Sub-Address (Bits [31:24]): 00-13h	133
HPARATYPE 03H: PALETTE (HPARASUBTYPE: 00-22H)	144
HPARATYPE 04H: VERTEX AND PRIMITIVE SETTING	154
Sub-Address (Bits [31:24]): 00-AAh	154
HParaType = 04h, Sub-Address = 40-52h: Clipping Window to Screen Window Transformation Setting.....	171
HPARATYPE 08H: CDC AND PPC SETTINGS	174
Sub-Address (Bits [31:24]): 00-03h	174

HPARATYPE 10H: COMMANDS FOR COMMAND REGULATOR..... 176
HPARATYPE 11H: COMMANDS FOR FRAME BUFFER SWAPPING AND CR'S MISCELLANEOUS SETTING 176

LIST OF TABLES

TABLE 1. VIDEO DISPLAY ENGINE REGISTERS	3
TABLE 2. VIDEO CAPTURE ENGINE AND HIGH QUALITY VIDEO REGISTERS.....	6
TABLE 3. GRAPHICS HARDWARE COLOR CURSOR OPERATION.....	29
TABLE 4. HIGH QUALITY VIDEO REGISTERS	55

INTRODUCTION

This document contains detailed graphics registers descriptions and other general information for the Chrome9 HD graphics engine. The graphics registers for the Chrome9 HD main features and its underlying subsystems are described explicitly in the following chapters.

About This Programming Guide

A brief description of each chapter is given below:

Part I:

Introduction.

An overview of the Chrome9 HD design features is given in this chapter, along with block diagram and product model.

Register Overview

Register specifications for register addressing and I/O space division are shown in this chapter.

AGP Graphics Control Register Descriptions

This chapter provides detailed AGP graphics control register descriptions. Those registers locate in PCI configuration space Device 0 Function 1.

VGA I/O Register Descriptions

This chapter provides detailed VGA-related register descriptions. The various video modes supported by the Chrome9 HD controller are also included in the configuration section.

2D Engine Register Descriptions

This chapter provides detailed 2D Engine register summary and descriptions.

DMA Register Descriptions

This chapter provides detailed DMA register summary and descriptions.

CBU Rotation Register Descriptions

This chapter provides detailed CBU rotation register summary and descriptions.

LVDS and DVI Register Descriptions

This chapter provides detailed LVDS and DVI register descriptions.

Display Port Register Descriptions

This chapter provides detailed Display Port register descriptions.

Part II:

Video Register Descriptions

This chapter provides both detailed video display engine register and video capture engine register summary and descriptions.

HQV Register Descriptions

This chapter provides detailed HQV register summary and descriptions.

Command Regulator (CR) Register Descriptions

This chapter provides detailed CR register descriptions.

3D Engine Register Descriptions

This chapter provides detailed 3D Engine register descriptions.

VIDEO REGISTERS

This chapter provides detailed video register summary table. Register descriptions on video play back, blending, engine capture and high quality video registers are followed in the sequent sections.

Video Register Summary

This graphics engine has an integrated video playback and blending engine. The video playback engine can simultaneously support up to three live video windows, and each video window can be independently scaled. Two blending engines support the graphics-to-video blending, followed by video-to-video blending effect. The blending factor is from constant, alpha stream or is combined with graphics data. Table 1 summarizes the video playback and blending engine registers. Detail register description follows.

Table 1. Video Display Engine Registers

Offset (Hex)	Register Name	Attribute
Video Related Engines Register Space 1 (0x00000200 ~ 0x000003FF)		
203-200	Interrupt Flags & Masks Control	RW
207-204	Address Flip Status	RO
20B-208	Alpha Window / HI (For Second Display) Horizontal and Vertical Location Start	RW
20F-20C	Alpha Window Horizontal and Vertical End & HI (For Second Display) Center Offset	RW
213-210	Alpha Window Control	RW
217-214	CRT Starting Address	RW
21B-218	The Second Display Starting Address	RW
21F-21C	Alpha Stream Frame Buffer Stride	RW
223-220	Primary Display Color Key	RW
227-224	Alpha Window & HI (For Second Display) Frame Buffer Starting Address	RW
23B-228	Chroma Key Lower Bound	RW
22F-22C	Chroma Key Upper Bound	RW
233-230	Video Stream 1 Control	RW
237-234	Video Window 1 Fetch Count	RW
23B-238	Video Window 1 Frame Buffer Y Starting Address 1	RW
23F-23C	Video Window 1 Frame Buffer Stride	RW
243-240	Video Window 1 Horizontal and Vertical Start Location	RW
247-244	Video Window 1 Horizontal and Vertical Ending Location	RW
24B-248	Video Window 1 Frame Buffer Y Starting Address 2	RW
24F-24C	Video Window 1 Display Zoom Control	RW
253-250	Video Window 1 Minify and Interpolation Control	RW
257-254	Video Window 1 Frame Buffer Y Starting Address 0	RW
25B-258	Video 1 FIFO Depth and Threshold Control	RW
25F-25C	Video Window 1 Horizontal and Vertical Starting Location Offset	RW
263-260	HI Control For Second Display	RW
267-264	The Second Display Color Key	RW
26B-268	V3 and Alpha Window FIFO Pre-threshold Control	RW
26F-26C	Video Window 1 Display Count On Screen Control	RW
273-270	HI Transparent Color For Second Display	RW
277-274	HI Inverse Color For Second Display	RW
27B-278	V3 and Alpha Window FIFO Depth and Threshold Control	RW
27F-27C	V3 Display Count On Screen Control	RW
283-280	Primary Display Second Color Key	RW
287-284	V1 Color Space Conversion & Enhancement Control 1	RW

28B-288	V1 Color Space Conversion & Enhancement Control 2	RW
28F-28C	P Signature Adder Result 1	RW
293-290	Alpha Window/Color Cursor Ending Position (For Primary Display)	RW
297-294	3D AGP Pause Address MMIO Port	WO
29B-298	Compose Output Modes Select	RW
29F-29C	V3 Frame Buffer Starting Address 2	RW
2A3-2A0	V3 Control	RW
2A7-2A4	V3 Frame Buffer Starting Address 0	RW
2AB-2A8	V3 Frame Buffer Starting Address 1	RW
2AF-2AC	V3 Frame Buffer Stride	RW
2B3-2B0	V3 Horizontal and Vertical Start	RW
2B7-2B4	V3 Horizontal and Vertical End	RW
2BB-2B8	V3 and Alpha Window Fetch Count	RW
2BF-2BC	V3 Display Zoom Control	RW
2C3-2C0	V3 Minify & Interpolation Control	RW
2C7-2C4	V3 Color Space Conversion & Enhancement Control 1	RW
2CB-2C8	V3 Color Space Conversion & Enhancement Control 2	RW
2CF-2CC	T Signature Adder Result 1	RW
2D3-2D0	Graphics Hardware Cursor Mode Control	RW
2D7-2D4	Graphics Hardware Cursor Position	RW
2DB-2D8	Graphics Hardware Cursor Origin	RW
2DF-2DC	Graphics Hardware Cursor Background Color	RW
2E3-2E0	Graphics Hardware Cursor Foreground Color	RW
2E7-2E4	T Signature Data Result 1	RW
2EB-2E8	HI for Primary Display FIFO Control Signal	RW
2EF-2EC	HI for Primary Display Transparent color	RW
2F3-2F0	HI for Primary Display Control Signal	RW
2F7-2F4	HI for Primary Display Frame Buffer Starting Address	RW
2FB-2F8	HI for Primary Display Horizontal and Vertical Start	RW
2FF-2FC	HI for Primary Display Center Offset	RW
Video Related Engines Register Space 2 (0x00001200 ~ 0x000013FF)		
1203-1200	Video 1Gamma R Correction Control	RW
1207-1204	Video 1Gamma G Correction Control	RW
120B-1208	Video 1Gamma B Correction Control	RW
120F-120C	HI for Primary Display Inverse Color	RW
1213-1210	PCIe Shadow Register 1	RW
1217-1214	PCIe Shadow Register 2	RW
121B-1218	PCIe Shadow Register 3	RW
121F-121C	PCIe Shadow Register 4	RW
1223-1220	Video 3 Gamma R Correction Control	RW
1227-1224	Video 3 Gamma G Correction Control	RW
122B-1228	Video 3 Gamma B Correction Control	RW
122F-122C	Video 3 Position Offset	RW
127C-1230	Reserved	RO
1283-1280	Interrupt Flags and Masks Control	RW
1287-1284	Logic Signature Setting	RW
128B-1288	P Logic Signature Address Result 0	RW
128F-128C	T Logic Signature Address Result 0	RW
1293-1290	IGA1 Display Position Counter 0	RO
1297-1294	IGA1 Display Position Counter 1	RO
129B-1298	IGA1 Display Position Counter 2	RW
129F-129C	T Logic Signature Data Result 0	RW

12A3-12A0	IGA2 Display Position Counter 0	RO
12A7-12A4	IGA2 Display Position Counter 1	RO
12AB-12A8	IGA2 Display Position Counter 2	RW
12B3-12B0	Primary Display Data Color Space Conversion and Enhancement Control 1	RW
12B7-12B4	Primary Display Data Color Space Conversion and Enhancement Control 2	RW
12BB-12B8	Primary Display Data Color Space Conversion and Enhancement Control 3	RW
12BF-12BC	Primary Display Data Color Space Conversion and Enhancement Control 4	RW
12F0-12C0	Reserved	RO
Extended Video Engines Register Space 2 (0x00003200 ~ 0x000033FF)		
3260	DVD / Video ID Control	
326C	DVD / Video Wait Control Register	

Note: 1) Port Address: MB1 + Offset Address

MB1 is declared in the register with offset address 18h~1Fh in the PCI configuration space.

- 2) There is additional register space to match the above register definition. When write a register to this space, it will be sent to “command regulator” first and then pass to video display engine. However, register read will be same as the original action. The relationship between the additional register space and original register space is:

(The additional register address) = (The original register address) + 16’h2000.

Table 2. Video Capture Engine and High Quality Video Registers

Offset (Hex)	Register Name	Attribute
Video Capture Engine Register		
303-300	Capture Interrupt Control and Flags	RW
307-304	Reserved	RO
30B-308	Transport Stream Control	RW
30F-30C	Reserved	RO
313-310	Capture Interface Control	RW
317-314	Active Video Horizontal Range (CCIR601 only)	RW
31B-318	Active Video Vertical Range (CCIR601 only)	RW
31F-31C	Active Video Scaling Control	RW
323-320	VBI Data Horizontal Range	RW
327-324	VBI Data Vertical Range	RW
32B-328	First VBI Buffer Starting Address	RW
32F-32C	VBI Buffer Stride	RW
333-330	Ancillary Data Count Setting	RW
337-334	Maximum Data Count of Active Video	RW
33B-338	Maximum Data Count of VBI or ANC	RW
33F-33C	Capture Data Count	RO
343-340	First Active Video Frame Buffer Starting Address	RW
347-344	Second Active Video Frame Buffer Starting Address	RW
34B-348	Third Active Video Frame Buffer Starting Address	RW
34F-34C	Second VBI Buffer Starting Address	RW
353-350	Stride of Active Video Buffer and Coring Function Control	RW
357-354	TS Buffer 0 Error Packet Indicator	RO
35B-358	TS Buffer 1 Error Packet Indicator	RO
35F-35C	TS Buffer 2 Error Packet Indicator	RO
360-37C	Reserved	RO

Offset (Hex)	Register Name	Attribute
HQV (High Quality Video) Engine Registers		
383-380	HQV Source Data Offset Control 1	RW
387-384	HQV Source Data Offset Control 2	RW
38B-388	HQV Source Data Offset Control 3	RW
38F-38C	HQV Source Data Offset Control 4	RW
393-390	HQV Parameters of Hardware Tuning Performance/Quality	RW
397-394	HQV Extended Control	RW
39B-398	HQV Static Record Frame Buffer Starting Address	RW
39F-39C	HQV Static Record Frame Buffer Stride	RW
3A3-3A0	HQV Color Adjustment Control 1	RW
3A7-3A4	HQV Color Adjustment Control 2	RW
3AB-3A8	HQV Color Adjustment Control 3	RW
3AF-3AC	HQV Color Adjustment Control 4	RW
3B3-3B0	HQV Horizontal Scale Control	RW
3B7-3B4	HQV Vertical Scale Control	RW
3BB-3B8	HQV Default Video Color	RW
3BF-3BC	HQV De-blocking Factor	RW
3C3-3C0	HQV Sub-picture Frame Buffer Stride and Control	RW
3C7-3C4	HQV Sub-picture Frame Buffer Starting Address	RW
3CB-3C8	HQV Sub-picture 4 x 16 RAM Table Write Control	RW
3D3-3D0	HQV Stream Control and Status	RW
3D7-3D4	HQV SW Source Data –Luma or Packed Starting Address	RW
3DB-3D8	HQV SW Source Data – Chroma Starting Address	RW
3DF-3DC	HQV Linear/Tile Address Mode, Color Space Conversion, Gamma and De-blocking Control	RW
3E3-3E0	HQV Source Data Line Count and Fetch Count Per Line	RW
3E7-3E4	HQV Motion Adaptive De-interlace Control & Threshold	RW
3EF-3EC	HQV Destination Frame Buffer Starting Address 0	RW
3F3-3F0	HQV Destination Frame Buffer Starting Address 1	RW
3F7-3F4	HQV Destination Frame Buffer Stride	RW
3FB-3F8	HQV Source Frame Buffer Stride	RW
3FF-3FC	HQV Destination Data Starting Address 2	RW

Offset (Hex)	Register Name	Attribute
Second Capture Engine Registers (Refer to Rx300-37C register descriptions for detail.)		
1303-1300	Capture Interrupt Control and Flags	RW
1307-1304	Reserved	RO
130B-1308	Transport Stream Control	RW
130F-130C	Reserved	RO
1313-1310	Capture Interface Control	RW
1317-1314	Active Video Horizontal Range (CCIR601 only)	RW
131B-1318	Active Video Vertical Range (CCIR601 only)	RW
131F-131C	Active Video Scaling Control	RW
1323-1320	VBI Data Horizontal Range	RW
1327-1324	VBI Data Vertical Range	RW
132B-1328	First VBI Buffer Starting Address	RW
132F-132C	VBI Buffer Stride	RW
1333-1330	Ancillary Data Count Setting	RW
1337-1334	Maximum Data Count of Active Video	RW
133B-1338	Maximum Data Count of VBI or ANC	RW
133F-133C	Capture Data Count	RO
1343-1340	First Active Video Frame Buffer Starting Address	RW
1347-1344	Second Active Video Frame Buffer Starting Address	RW
134B-1348	Third Active Video Frame Buffer Starting Address	RW
134F-134C	Second VBI Buffer Starting Address	RW
1353-1350	Stride of Active Video Buffer and Coring Function Control	RW
1357-1354	TS Buffer0 Error Packet Indicator	RO
135B-1358	TS Buffer1 Error Packet Indicator	RO
135F-135C	TS Buffer2 Error Packet Indicator	RO
1360-137C	Reserved	RO

Offset (Hex)	Register Name	Attribute
Second HQV Engine Registers (Refer to Rx380-3FF register descriptions for detail.)		
1380-13B8	Reserved	RO
13BF-13BC	De-blocking Factor	RW
13C3-13C0	Subpicture Frame Buffer Stride and Control	RW
13C7-13C4	Subpicture Frame Buffer Starting Address	RW
13CB-13C8	Subpicture 4 X 16 RAM Table Write Control	RW
13CF-13CC	HQV Source Data Offset Control	RW
13D3-13D0	HQV Stream Control and Status	RW
13D7-13D4	HQV SW Source Data –Luma or Packed Starting Address	RW
13DB-13D8	HQV SW Source Data – Chroma Starting Address	RW
13DF-13DC	HQV Linear/Tile Address Mode and Color Space Conversion First Control	RW
13E3-13E0	HQV Source Data Line Count and Fetch Count Per Line	RW
13E7-13E4	HQV Motion Adaptive De-interlace Control and Threshold	RW
13EB-13E8	HQV Scale Control	RW
13EF-13EC	HQV Destination Data Starting Address 0	RW
13F3-13F0	HQV Destination Data Starting Address 1	RW
13F7-13F4	HQV Destination Frame Buffer Stride	RW
13FB-13F8	HQV Source Frame Buffer Stride	RW
13FF-13FC	HQV Destination Data Starting Address 2	RW

Note:1) Port Address: MB1 + Offset Address

MB1 is declared in the register with offset address 18h~1Fh in the PCI configuration space.

- 2) There is additional register space to match the above register definition. When write a register to this space, it will be sent to “command regulator” first and then pass to video display engine. However, register read will be same as the original action. The relationship between the additional register space and original register space is

$$(\text{The additional register address}) = (\text{The original register address}) + 16'h2000$$

Video Display Engine Register Descriptions (200-12F0h)

Offset Address: 203-200h
Interrupt Flags and Masks Control
Default Value: 0000 0000h

Bit	Attribut	Default	Description
31	RW	0	Interrupt Enable 0: Disable 1: Enable
30	RW	0	LVDS Sense Interrupt Enable 0: Disable 1: Enable
29	RW	0	Capture 0 VBI Capture End Interrupt Enable 0: Disable 1: Enable
28	RW	0	Capture 0 Active Video Data Capture End Enable 0: Disable 1: Enable
27	RW1C	0	LVDS Sense Interrupt Status
26	RW	0	Capture 1 VBI Capture End Interrupt Enable 0: Disable 1: Enable
25	RW	0	First HQV Engine Interrupt Enable 0: Disable 1: Enable (Refer to 03D0h)
24	RW	0	Capture 1 Active Video Data Capture End Enable 0: Disable 1: Enable
23	RW	0	DMA1 Transfer Done Interrupt Enable 0: Disable 1: Enable
22	RW	0	DMA1 Descriptor Done Interrupt Enable 0: Disable 1: Enable
21	RW	0	DMA0 Transfer Done Interrupt Enable 0: Disable 1: Enable
20	RW	0	DMA0 Descriptor Done Interrupt Enable 0: Disable 1: Enable
19	RW	0	VGA VSYNC Interrupt Mask Enable 0: Disable 1: Enable
18	RW	0	MC Complete Frame Interrupt Mask Enable 0: Disable 1: Enable
17	RW	0	Secondary Display VSYNC Interrupt Enable 0: Disable 1: Enable
16	RW	0	DVI Sense Interrupt Enable 0: Disable 1: Enable
15	RW1C	0	Secondary Display VSYNC Interrupts Status
14	RW1C	0	Capture 1 VBI Capture End Interrupt Status
13	RW1C	0	Capture 0 VBI Capture End Interrupt Status
12	RW1C	0	Capture 0 Active Video Data Capture End Interrupt Status
11	RW	0	Second HQV Engine Interrupt Enable 0: Disable 1: Enable (Refer to 13D0h for more detail.)
10	RW	0	Second HQV Engine Interrupt Status (Refer to 13D0h for more detail.)
9	RW1C	0	First HQV Engine Interrupt Status (Refer to 03D0h for more detail.)
8	RW1C	0	Capture 1 Active Video Data Capture End Interrupt Status
7	RW1C	0	DMA 1 Transfer Done Interrupt Status
6	RW1C	0	DMA 1 Descriptor Done Interrupt Status
5	RW1C	0	DMA 0 Transfer Done Interrupt Status
4	RW1C	0	DMA 0 Descriptor Done Interrupt Status
3	RW1C	0	VGA VSYNC Interrupt Status
2	RW1C	0	MC Complete Frame Interrupt Status
1	RO	0	Vertical Blanking Status
0	RW1C	0	DVI Sense Interrupt Status

Offset Address: 207-204h
Address Flip Status
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:12	RO	0	Reserved
11	RO	0	Video Window 1 SW Flip Status (R) Write B0+254'h port to clear this bit.
10	RO	0	Video Window 3 SW Flip Status (R) Write B0+2A4'h port to clear this bit.
9:6	RO	0	Reserved
5	RW1C	0	CR Interrupt Status
4	RO	0	Alpha Window Starting Address Update Status 0: Updated 1: Not yet updated It will be set as writes Rx224, and be clear as starting address is updated.
3	RO	0	Video Window 3 Starting Address Update Status 0: Updated 1: Not yet updated It will be set as writes Rx2A4, and be clear as starting address is updated.
2	RO	0	IGA2 Vertical Blanking Status
1	RO	0	Graphics Starting Address Update Status 0: Updated 1: Not yet updated It will be set as writes Rx214, and be clear as starting address is updated.
0	RO	0	Video Window 1 Starting Address Update Status 0: Updated 1: Not yet updated It will be set as writes Rx254, and be clear as starting address is updated.

Offset Address: 20B-208h
Alpha Window / Hardware Icon (HI) Horizontal and Vertical Location Start
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:27	RO	0	Reserved
26:16	WO	0	Alpha Window / Hardware Icon Horizontal (X) Starting Location <i><u>Depend on Hardware Icon Enable (Rx260[0]):</u></i> <i>When Rx260[0]=0:</i> Alpha window horizontal (X) starting location <i>When Rx260[0]=1:</i> Hardware icon horizontal (X) starting location Unit: Pixel
15:11	RO	0	Reserved
10:0	WO	0	<i><u>When Write:</u></i> Alpha Window / Hardware Icon Vertical (Y) Starting Location Depend on Hardware Icon Enable (Rx260[0]) <i>When Rx260[0]=0:</i> Alpha window vertical (Y) starting location <i>When Rx260[0]=1:</i> Hardware icon vertical (Y) starting location Unit: Line <i><u>When Read:</u></i> Graphic Display Vertical Line Number Unit: Line

Offset Address: 20F-20Ch
Alpha Window Horizontal and Vertical Location End / Hardware Icon (HI) Center Offset Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:27	RW	0	Reserved
26:16	RW	0	Alpha Window / Hardware Icon Horizontal (X) Ending Location <i>Depend on Hardware Icon Enable (Rx260[0])</i> <i>When Rx260[0]=0:</i> Bits[26:16] = Alpha window Horizontal (X) ending location <i>When Rx260[0]=1:</i> Bits[22:16] = Hardware icon Horizontal (X) center offset Unit: Line
15:11	RO	0	Reserved
10:0	RW	0	Alpha Window / Hardware Icon Vertical (Y) Ending Location <i>Depend on Hardware Icon Enable (Rx260[0])</i> <i>When Rx260[0]=0:</i> Bits[10:0] = Alpha window vertical (Y) ending location <i>When Rx260[0]=1:</i> Bits[6:0] = Hardware icon vertical (Y) enter offset Unit: Line

Offset Address: 213-210h
Alpha Window Control
Default Value: 0000 FF00h

Bit	Attribute	Default	Description
31:21	RO	0	Reserved
20:16	RW	0	Alpha Stream Request Expire Number Unit: 4 Requests
15:8	RW	FFh	Constant Alpha Factor Setting For Graphics Blending
7:2	RO	0	Reserved
1:0	RW	00b	Graphics Blending Alpha Select (Alpha*VID+(1-Alpha)*GRA) 00: Blending using constant alpha factor [15:8] 01: Alpha is from alpha stream 10: Alpha is from graphics stream 11: Reserved

Offset Address: 217-214h
CRT Starting Address Shadow
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RW	0	IGA1 Down Scaling Flip Address equivalent to 3X5.EC[1]
30	RW	0	IGA1 Down Scaling Line Flip Enable
29	RO	0	Reserved
28:0	RW	0	Primary Display Starting Address or IGA1 Down Scaling Source Starting Address (Valid when 3X5.EC[0] = 1) Address equivalent to: 3X5.48 [4:0] 3X5.34 [7:0] 3X5.0C [7:0] 3X5.0D [7:0]

Note: In monochrome mode, the “X” in the above table stands for “B”. In color mode, the “X” in the above table stands for “D”.

Offset Address: 21B-218h
The Second Display Starting Address
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:29	RO	0	Display Address Selection 00: S.L Others are not supported
28:3	RW	0	The Second Display Starting Address or IGA2 Down Scaling Source Starting Address (Valid when 3X5.E8[4] = 1) Unit: 8 bytes
2	RO	0	Reserved
1	RW	0	IGA2 Down Scaling Line Flip Enable
0	RW	0	IGA2 Down Scaling Flip Address equivalent to 3X5.E8[5].

Note: This register should be the same with 3X5.5E, 5D and 5C registers.

Offset Address: 21F-21Ch
Alpha Stream Frame Buffer Stride
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:13	RO	0	Reserved
12:4	RW	0	Alpha Stream Frame Buffer Stride Unit: 16 bytes
3:0	RO	0	Reserved

Offset Address: 223-220h
Primary Display Color Key
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RW	0	CRT Color Key For RGB10 color mode [29].
30	RW	0	CRT Color Key Enable 0: Disable 1: Enable
29	RW	0	CRT Color Key Inverse Control 0: Display video if color key match 1: Display video if not color key match
28:0	RW	0	CRT Color Key Bits [28:0]: For RGB10 color mode [28:0] Bits [23:0]: For 32-bit true color mode Bits [15:0]: For 565 Hi color mode Bits [14:0]: For 555 Hi color mode Bits [7:0]: For 256 color mode

Offset Address: 227-224h
Alpha Window / Hardware Icon Frame Buffer Starting Address
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RO	0	Reserved
30:29	RW	00b	Target of Frame Buffer Starting Address 00: S.L 01: S.F 10: Reserved 11: L.L
28:4	RW	0	Alpha Window / Hardware Icon Frame Buffer Starting Address <i>Depend on Hardware Icon Enable (Rx260[0])</i> <i>When Rx260[0]=0:</i> Frame buffer starting address for alpha window <i>When Rx260[0]=1:</i> Frame buffer starting address for hardware icon Unit: 16 bytes
3:0	RO	0	Reserved

Offset Address: 22B-228h
Chroma Key Lower Bound
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RW	0	Chroma Key Lower for Y/G Bit [1]
30	RW	0	Chroma Key Enable 0: Disable 1: Enable
29	RW	0	Chroma Key Inverse Control 0: Display video if chroma key not match 1: Display video if chroma key match
28:0	RW	0	Chroma Key Lower {[23:16], [31], [28]}: Y/G {[15:8], [27:26]}: U/R {[7:0], [25:24]}: V/B

Offset Address: 22F-22Ch
Chroma Key Upper Bound
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RO	0	Reserved
30	RW	0	Chroma Key Select 1 : Select Video 3 0 : Select Video 1
29:0	RO	0	Chroma Key Upper {[23:16], [29:28]} Y/G {[15:8], [27:26]}: U/R {[7:0], [25:24]}: V/B

Offset Address: 233-230h
Video Stream 1 Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RW	0	V1 Display to CRT or the Second Display 0: CRT 1: Second Display
30	RW	0	V1 Window Pre-fetch Enable
29	RW	0	V1 Window Gamma Function Enable
28	RW	0	V1 Window De-Gamma Function Enable
27	RW	0	V1 Window Adder Tile Mode Enable
26:25	RW	00b	V1 Flip Control 00: SW Flip 01: HW Flip and trigger by the HQV engine. 10: HW Flip and trigger by the Capture Port 0. 11: HW Flip and trigger by the Capture Port 1.
24	RW	0	V1 Frame to Field Enable 0: Disable 1: Enable If enabled, the stride will 2 times of original values. This bit is valid at 1. Software flip. 2. HQV flip. 3. Capture frame mode flip. 4. MC frame mode flip.
23	RO	0	Reserved
22	RW	0	V1 De-interlace Mode If enabled hardware will add one line to the top of odd (bottom) field. 0: Disable 1: Enable
21	RW	0	V1 Line Flip Only in Non Video Active Period Enable 0: Disable 1: Enable
20:16	RW	0	V1 Request Expire Number (Unit: 4 requests)
15:10	RO	0	Reserved
9	RW	0	Divided V1 Flip for HQV Engine VSYNC Number to Half Enable 0: Disable 1: Enable
8	RW	0	V1 Color Space Conversion Disable 0: Enable 1: Disable
7	RW	0	V1 Color Space Conversion Chroma Sign Bits Conversion
6:5	RO	0	Reserved
4:2	RW	000b	V1 Stream Data Format 000: YUV422 001: RGB32 010: RGB15 011: RGB16 100: YUV411 101: RGB10 Other : reserved
1	RW	0	V1 Scaling Enable on IGA1 0: Disable V1 scaling on IGA1 1: Enable V1 scaling on IGA1
0	RW	0	V1 Enable 0: Disable 1: Enable

Offset Address: 237-234h
Video Window 1 Fetch Count
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:30	RO	0	Reserved
29:20	RW	0	V1 Per Line Fetch Count It is equal, no-sizing line fetch count / minify times (Unit: 16 bytes)
19:0	RO	0	Reserved

Offset Address: 23B-238h
Video Window 1 Fetch Buffer Y Starting Address 1
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RW	0	V1 Length Internal Guard Bit 0: Old design 1: New design
30:26	RO	0	Reserved
30:29	RW	00b	Target of The Second Frame Buffer Starting Address 00: S.L. 01: S.F 10: Reserved 11: L.L.
28:3	RW	0	V1 Packed Mode The second frame buffer starting address.
2:0	RO	0	Reserved

Offset Address: 23F-23Ch
Video Window 1 Frame Buffer Stride
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:14	RO	0	Reserved
13:4	RW	0	V1 Packed Mode Frame buffer stride (Unit: 16 bytes)
3:0	RO	0	Reserved

Offset Address: 243-240h
Video Window 1 Horizontal and Vertical Starting Location
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:27	RO	0	Reserved
26:16	RW	0	Video Window 1 Horizontal (X) Starting Location (-1). (Unit: pixel)
15:11	RO	0	Reserved
10:0	RW	0	Video Window 1 Vertical (Y) Starting Location (-1). (Unit: Line)

Offset Address: 247-244h
Video Window 1 Horizontal and Vertical Ending Location
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:27	RO	0	Reserved
26:16	RW	0	Video Window 1 Horizontal (X) Ending Location (-1). (Unit: pixel)
15:11	RO	0	Reserved
10:0	RW	0	Video Window 1 Vertical (Y) Ending Location (-1). (Unit: Line)

Offset Address: 24B-248h
Video Window 1 Frame Buffer Y Starting Address 2
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RO	0	Reserved
30:29	RW	00b	Target of The Third Frame Buffer Starting Address 00: S.L. 01: S.F 10: Reserved 11: L.L.
28:3	RW	0	V1 Packed Mode The third frame buffer starting address. (Unit: 16 bytes)
2:0	RO	0	Reserved

Offset Address: 24F-24Ch
Video Window 1 Display Zoom Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RW	0	Video Window 1 Horizontal (X) Zoom Enable 0: Disable 1: Enable
30:27	RO	0	Reserved
26:16	RW	0	Video Window 1 Horizontal (X) Zoom Factor
15	RW	0	Video Window 1 Vertical (Y) Zoom Enable 0: Disable 1: Enable
14:10	RO	0	Reserved
9:0	RW	0	Video Window 1 Vertical (Y) Zoom Factor

Offset Address: 253-250h
Video Window 1 Minify & Interpolation Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:27	RO	0	Reserved
26:24	RW	000b	V1 Horizontal (X) Minify Control 000: No minify; 001: Minify by a factor of 2 010: Reserved 011: Minify by a factor of 4 101: Minify by a factor of 8 111: Minify by a factor of 16 Other cases: reserved
23:19	RO	0	Reserved
18:16	RW	000b	V1 Vertical (Y) Minify Control 000: No minify 001: Minify by a factor of 2 010: Reserved 011: Minify by a factor of 4 101: Minify by a factor of 8 111: Minify by a factor of 16 Other cases: reserved
15:3	RO	0	Reserved
2	RW	0	V1 Luma-only Interpolation When the Vertical Interpolation Is Enabled 0: Only luma values interpolated. 1: All YUV/YcbCr values interpolated.
1	RW	0	V1 Horizontal (X) Interpolation Mode Select 0: Pixel is replicated 1: Enable interpolation
0	RW	0	V1 Vertical (Y) Interpolation Mode Select 0: Pixel is replicated 1: Enable interpolation

Offset Address: 257-254h
Video Window 1 Frame Buffer Y Starting Address 0
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RO	0	V1 Play Odd / Even Field Control This bit is valid when SW Playback and Field Base Picture are selected. 0: Play even field 1: Play odd field
30:29	RO	00b	Target of The First Frame Buffer Starting Address 00: S.L. 01: S.F 10: Reserved 11: L.L.
28:2	RO	0	V1 Packed Mode The first frame buffer starting address. (Unit : 4 bytes)
1:0	RO	0	Reserved

Note: In packed mode, we could use Rx254[3:2] to get

- 1.No minify: 4 bytes alignment. Rx254[3:2] are valid
2. (Minify = 2): 8 bytes alignment. Rx254[3] is valid, and Rx254[2] is omitted.
3. (Minify > 2): 16 bytes alignment. a Rx254[3:2] are omitted.

Offset Address: 25B-258h
Video 1 FIFO Depth and Threshold Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:24	RW	0	V1 FIFO Pre-threshold Let V1 to issue request early. Normally, this value is more or equal than V1 FIFO threshold (Rx258[15:8]). (Unit : level)
23:26	RO	0	Reserved
15:8	RW	0	V1 FIFO Threshold Let V1 request priority from low to high. (Unit: level)
7:0	RW	0	V1 FIFO Depth (- 1) (Unit: level)

Note: One level is equal to 16 bytes.

Offset Address: 25F-25Ch
Video Window 1 Horizontal and Vertical Starting Location Offset
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:27	RO	0	Reserved
26:16	RW	0	Video Window 1 Horizontal (X) Starting Location Offset (Unit: 16 bytes)
15:11	RO	0	Reserved
10:0	RW	0	Video Window 1 Vertical (Y) Starting Location Offset (Unit: Line)

Offset Address: 263-260h
Hardware Icon (HI) Control (Only for Second Display)
Default Value: 000F 00F0h

Bit	Attribut	Default	Description
31	RW	0	V4 Displays to CRT (0) or Secondary Display (1) 0: CRT 1: Secondary Display
30	RW	0	V4 Window Pre-fetch Enable
29	RW	0	HWI + (1-alpha)*Graphics Mode 0 Disable 1 Enable
28	RW	0	Alpha Value Come From Where (Only for the true color Hardware icon) 0: From bit [23:16] 1: From the bit [31:24] of Hardware icon
27:26	RW	00b	HI Window Size 00: 32x32 01: 64x64 1x: 128x128 Unit: Pixel X line
25:24	RW	00b	HI Data Stream Format 00: RGB555 01: RGB565 10: RGB32 11: RGB10
23:20	RO	0	Reserved
19:16	RW	Fh	HI Constant Alpha [3:0] (HIAPA)
15:12	RW	0	Alpha Changed Value (HICV) Per Frame As HI Fan In/Out Turn on Rx260[8] ALPHAn[7:0] = ALPHAn-1[7:0] +/- HICV[3:0], where just ALPHAn[7:4] is valid alpha value and ALPHA0 = {HIAPA}.
11:10	RW	0	DMA1 Descriptor Done Interrupt Enable 0: Disable 1: Enable
9	RW	0	HI Fan In / Out Selector 0: Default 1: Fan in (+)
8	RW	0	HI Fan In / Out Enable 0: Disable 1: Enable
7:4	RW	Fh	HI Constant Alpha[7:4] (HIAPA) The reset bits are put on [19:16].
3	RW	0	V4 Request Length Disable 0: Enable length 1:Disable length Length = 0
2	RW	0	HI Blending Enable 0: Disable 1: Enable
1	RO	0	Reserved
0	RW	0	HI Enable 0: Disable 1: Enable

Offset Address: 267-264h
The Second Display Color Key
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RW	0	The Second Display Color Key Bit [29] For RGB10 True Color Mode See also bits [28:0] for detail.
30	RW	0	Second Display Color Key Enable 0: Disable 1: Enable
29	RW	0	Second Display Color Key Inverse Control 0: Display video if color key match 1: Display video if not color key match
28:0	RW	0	The Second Display Color Key Bits [31], [28:0]: For RGB10 true color mode Bits [23:0]: For 32-bit true color mode Bits [15:0]: For 565 Hi color mode Bits [14:0]: For 555 Hi color mode Bits [7:0]: For 256 color mode

Offset Address: 26B-268h
V3 and Alpha Window FIFO Pre-Threshold Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:23	RO	0	Reserved
22:16	RW	0	Alpha Window FIFO Pre-threshold Let alpha engine issues request early. This value is normally more than or equal to the alpha engine FIFO threshold (Rx278[30:24]). Unit : Level
15:8	RO	0	Reserved
7:0	RW	0	V3 FIFO Pre-threshold Let V3 issues request early. This value is normally more than or equal to V3 FIFO threshold (Rx278[15:8]). Unit: Level

Offset Address: 26F-26Ch
Video Window 1 Display Count On Screen Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:28	RO	0	Reserved
27:26	RW	0	V1 Vertical Line Count That Shows On Screen (Unit: Line)
25:12	RO	0	Reserved
11:0	RW	0	V1 Horizontal Pixel Count That Shows On Screen (-1) (unit: pixel)

Offset Address: 273-270h
Hardware Icon (HI) Transparent Color (Only For Second Display)
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:30	RO	0	Reserved
29:0	RW	0	HI Transparent Color Bits [29:0]: For RGB10 Bits [23:0]: For RGB32 Bits [15:0]: For RGB565 Bits [14:0]: For RGB555

Offset Address: 277-274h
Hardware Icon (HI) Inverse Color (Only For Second Display)
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:30	RO	0	Reserved
29:0	RW	0	HI Inverse Color Bits [29:0]: For RGB10 Bits [23:0]: For RGB32 Bits [15:0]: For RGB565 Bits [14:0]: For RGB555

Offset Address: 27B-278h
V3 and Alpha Window FIFO Depth and Threshold Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RO	0	Reserved
30:24	RW	0	Alpha Window FIFO Threshold Unit: Level
23	RO	0	Reserved
22:16	RW	0	Alpha Window FIFO Depth (-1) Unit: Level
15:8	RW	0	Video Window 3 FIFO Threshold Unit: Level
7:0	RW	0	Video Window 3 FIFO Depth (-1) Unit: Level

Note: One level is equal to 16 bytes.

Offset Address: 27F-27Ch
Video Window 3 Display Count On Screen Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:28	RO	0	Reserved
27:26	RW	0	V3 Vertical Line Count That Shows On Screen (Unit: Line)
15:12	RO	0	Reserved
11:0	RW	0	V1 Horizontal Pixel Count That Shows On Screen (-1) (Unit: pixel)

Offset Address: 283-280h
Primary Display Second Color Key
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RO	0	Reserved
30	RW	0	CRT Color Key Enable 0: Disable 1: Enable
29	RW	0	CRT Color Key Inverse Control 0: Display video if color key match 1: Display video if not color key match
28:24	RO	0	Reserved
23:0	RW	0	Primary Display Color Key Bits [23:0]: For 32-bit true color mode Bits [15:0]: For 565 Hi color mode Bits [14:0]: For 555 Hi color mode Bits [7:0]: For 256 color mode

Offset Address: 287-284h
Video Window 1 Color Space Conversion and Enhancement Control 1
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RW	0	SDTV (BT601) Coefficient Enable 0: Disable 1: Enable
30	RW	0	HDTV (BT709) Coefficient Enable 0: Disable 1: Enable
29	RO	0	Reserved
28:24	RW	0	Coefficient A X.XXXXX From 0 to 1.9375
23:22	RO	0	Reserved
21:16	RW	0	Coefficient B1 SXX.XXX S=1 negative S=0 positive, from -2.125 to 2.125
15:14	RO	0	Reserved
13:8	RW	0	Coefficient C1 SXX.XXX S=1 negative S=0 positive, from -2.125 to 2.125
7:0	RW	0	Coefficient D 2's complement integer from -128 to 127

 Note: R = AY+B₁Cb+C₁C_r+D

Offset Address: 28B-288h
Video Window 1 Color Space Conversion and Enhancement Control 2
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:29	RO	0	Reserved
28:24	RW	0	Coefficient B2 SX.XXX S=1 negative S=0 positive, from -1.875 to 1.875
23:21	RO	0	Reserved
20:16	RW	0	Coefficient C2 SX.XXX S=1 negative S=0 positive, from -1.875 to 1.875
15:14	RO	0	Reserved
13:8	RW	0	Coefficient B3 SXX.XXX S=1 negative S=0 positive, from -3.875 to 3.875
7:6	RO	0	Reserved
5:0	RW	0	Coefficient C3 SXX.XXX S=1 negative S=0 positive, from -3.875 to 3.875

 Note: G = AY+B₂Cb+C₂C_r+D

 B = AY+B₃Cb+C₃C_r+D

Offset Address: 28F-28Ch
P Logic Adder Result 1
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:0	RW	0	P Logic Adder Result 1

Offset Address: 293-290h
Alpha Window / Color Cursor Ending (Only For Primary Display)
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:28	RO	0	Reserved
27:16	RW	0	Hardware Icon Horizontal (X) Ending Position
15:11	RO	0	Reserved
10:0	RW	0	Hardware Icon Vertical (Y) Ending Position Unit: Line

Offset Address: 297-294h
3D AGP Pause Address MMIO Port
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:0	RW	0	3D AGP Pause Address MMIO Port

Offset Address: 29B-298h
Compose Output Mode Select
Default Value: 0300 0000h

Bit	Attribute	Default	Description
31	RW	0	Video 1 Command End, V1 Load New Register Setting 1: Fire If registers are updated to engine, this bit will be cleared to 0 and the default is set at 0.
30	RW	0	Video 3 Command End, V3 Load New Register Setting 1: Fire If registers are updated to engine, this bit will be cleared to 0 and the default is set at 0.
29	RW	0	Video Register Always Loaded For hardware simulation and the default is set at 0.
28	RW	0	Video Register Loaded at Vertical Blanking Without Waiting Source Flip Need to write [31] or [30] and default is set at 0.
27	RW	0	Video 3 Register Always Loaded For hardware simulation and the default is set at 0.
26	RW	0	Video 3 Register Loaded at Vertical Blanking Without Waiting Source Flip Need to write [31] or [30] and default is set at 0.
25:24	RW	11b	Interpolation FIFO Clock Select 00: Not in use 01: V1 HDTV 10: V3 HDTV 11: V1 SDTV and V3 SDTV
23:21	RO	0	Reserved
20	RW	0	Video Output Overlap Control 0: V1 is on top 1: V3 is on top
19:18	RO	0	Reserved
17	RW	0	Bypass CRT Horizontal Magnify Function
16	RW	0	Bypass CRT Vertical Magnify Function
15:8	RO	0	Reserved
7	RW	0	MCK Bypass Enable 0: Disable 1: Enable
6	RO	0	Reserved
5	RW	0	Bypass LCD Horizontal Magnify Function
4	RW	0	Bypass LCD Vertical Magnify Function
3	RW	0	Video 3 Line Flip Enable 0: Disable 1: Enable
2	RW	0	Video 1 Line Flip Enable 0: Disable 1: Enable
1	RO	0	Reserved
0	RW	0	Video 1 Round Control Enable 0: Disable 1: Enable

Offset Address: 29F-29Ch
Video Window 3 Frame Buffer Starting Address 2
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RO	0	Reserved
30:29	RW	00b	Target of The Third Frame Buffer Starting Address 00: S.L. 01: S.F. 10: Reserved 11: L.L.
28:3	RW	0	The Third Frame Buffer Starting Address of V3 Unit: 16 bytes
2:0	RO	0	Reserved

Offset Address: 2A3-2A0h
Video Stream 3 Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RO	0	Reserved
30	RW	0	V3 Window Pre-fetch Enable 0: Disable 1: Enable
29	RW	0	V3 Window Gamma Function Enable 0: Disable 1: Enable
28:27	RO	0	Reserved
26:25	RW	00b	V3 Flip Control 00: SW flip 01: HW flip and triggle by the HQV engine 10: Reserved 10: HW flip and triggle by the Capture Port 0 11: Reserved 11: HW flip and triggle by the Capture Port 1
24	RW	0	V3 Frame to Field Enable 0: Disable 1: Enable If enabled, the stride will be 2 times of original values. This bit is valid at: Software flip, HQV flip.
23	RO	0	Reserved
22	RW	0	V3 De-interlace Mode 0: Disable 1: Enable If enabled, hardware will add one line to the top of odd (bottom) field
21	RW	0	V3 Line Flip Only in Non Video Active Period Enable 0: Disable 1: Enable
20:16	RW	0	V3 Request Expire Number Unit: 4 requests
15:10	RO	0	Reserved
9	RW	0	Divided V3 Flip for HQV Engine VSYNC Number to Half Enable 0: Disable 1: Enable
8	RW	0	V3 Color Space Conversion Disable 0: Enable 1: Disable
7	RW	0	V3 Color Space Conversion Chroma Sign Bits Conversion 1: Inverse
6:5	RO	0	Reserved
4:2	RW	000b	V3 Stream Data Format x00: YUV422 001: RGB32 x10: RGB15 011: RGB16
1	RW	0	V3 scaling enable on IGA1 0: disable V3 scaling on IGA1 1: enable V3 scaling on IGA1
0	RW	0	V3 Enable 0: Disable 1: Enable

Offset Address: 2A7-2A4h
Video Window 3 Frame Buffer Starting Address 0
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RW	0	Play Odd (1) / Even (0) Field When SW Playback and Field Base Picture Are Selected
30:29	RO	00b	Target of The First Frame Buffer Starting Address 00: S.L. 01: S.F. 10: Reserved 11: L.L.
28:2	RW	0	The First Frame Buffer Starting Address of V3 Unit: 4 bytes
1:0	RO	0	Reserved

Offset Address: 2AB-2A8h
Video Window 3 Frame Buffer Starting Address 1
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RW	0	V3 Length Internal Guard Bit 0: Old design 1: New design
30:29	RW	00b	Target of The Second Frame Buffer Starting Address 00: S.L. 01: S.F. 10: Reserved 11: L.L.
28:3	RW	0	The Second Frame Buffer Starting Address of V3 Unit: 16 bytes
2:0	RO	0	Reserved

Offset Address: 2AF-2ACh
Video Window 3 Frame Buffer Stride
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:14	RO	0	Reserved
13:4	RW	0	V3 Frame Buffer Stride Unit: 16 bytes
3:0	RO	0	Reserved

Offset Address: 2B3-2B0h
Video Window 3 Horizontal and Vertical Start
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:27	RO	0	Reserved
26:16	RW	0	V3 Horizontal (X) Starting Location Unit: Pixel
15:11	RO	0	Reserved
10:0	RW	0	V3 Vertical (Y) Starting Location Unit: Line

Offset Address: 2B7-2B4h
Video Window 3 Horizontal and Vertical End
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:27	RO	0	Reserved
26:16	RW	0	V3 Horizontal (X) Ending Location Unit: Pixel
15:11	RO	0	Reserved
10:0	RW	0	V3 Vertical (Y) Ending Location Unit: Line

Offset Address: 2BB-2B8h
Video Window 3 and Alpha Window Fetch Count
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:30	RO	0	Reserved
29:20	RW	0	V3 Per Line Fetch Count Unit: Pixel
19:10	RO	0	Reserved
9:0	RW	0	Alpha Window Per Line Fetch Count Unit: Line

Offset Address: 2BF-2BCh
Video Window 3 Display Zoom Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RW	0	V3 Horizontal (X) Zoom Enable 0: Disable 1: Enable
30:27	RO	0	Reserved
26:16	RW	0	V3 Horizontal (X) Zoom Factor
15	RW	0	V3 Vertical (Y) Zoom Enable 0: Disable 1: Enable
14:10	RO	0	Reserved
9:0	RW	0	V3 Vertical (Y) Zoom Factor

Offset Address: 2C3-2C0h
Video Window 3 Minify and Interpolation Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:27	RW	0	Reserved
26:24	RW	000b	V3 Horizontal (X) Minify Control 000: No minify 001: Minify by a factor of 2 010: Reserved 011: Minify by a factor of 4 101: Minify by a factor of 8 111: Minify by a factor of 16 Other cases are reserved.
23:19	RO	0	Reserved
18:16	RW	000b	V3 Vertical (Y) Minify Control 000: No minify 001: Minify by a factor of 2 010: Reserved 011: Minify by a factor of 4 101: Minify by a factor of 8 111: Minify by a factor of 16 Other cases are reserved.
15:3	RO	0	Reserved
2	RW	0	V3 Luma-only Interpolation When The Vertical Interpolation Is Enabled 0: Only luma values interpolated 1: All YUV/YcbCr values interpolated
1	RW	0	V3 Horizontal (X) Interpolation Mode Select 0: Pixel is replicated 1: Enable interpolation
0	RW	0	V3 Vertical (Y) Interpolation Mode Select 0 Pixel is replicated 1 Enable interpolation Note: V1 and V3 can support interpolation simultaneously when both video source resolutions are lower than 800x600. If anyone exceeds the 800x600 resolution, only one of them can support interpolation. The control bit is defined at 0x298[25:24].

Offset Address: 2C7-2C4h
Video Window 3 Color Space Conversion and Enhancement Control 1
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RW	0	SDTV (BT601) Coefficient Enable 0: Disable 1: Enable
30	RW	0	HDTV (BT709) Coefficient Enable 0: Disable 1: Enable
29	RO	0	Reserved
28:24	RW	0	Coefficient A X.XXXXX from 0 to 1.9375
23:22	RO	0	Reserved
21:16	RW	0	Coefficient B1 SXX.XXX S=1 negative S=0 positive From - 2.125 to 2.125
15:14	RO	0	Reserved
13:8	RW	0	Coefficient C1 SXX.XXX S=1 negative S=0 positive From - 2.125 to 2.125
7:0	RW	0	Coefficient D[10:3] 2's complement integer from -128 to 127

Note: R=AY+B1Cb+C1Cr+D

Offset Address: 2CB-2C8h
Video Window 3 Color Space Conversion and Enhancement Control 2
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:29	RW	0	Coefficient D[2:0] 2's complement integer from -128 to 127
28:24	RW	0	Coefficient B2 SX.XXX S=1 negative S=0 positive, from -1.875 to 1.875
23:21	RO	0	Reserved
20:16	RW	0	Coefficient C2 SX.XXX S=1 negative S=0 positive, from -1.875 to 1.875
15:14	RO	0	Reserved
13:8	RW	0	Coefficient B3 SXX.XX S=1 negative S=0 positive, from 0 to 3.75
7:6	RO	0	Reserved
5:0	RW	0	Coefficient C3 SX.XX S=1 negative S=0 positive, from -3.875 to 3.875

Note: G = AY+B2Cb+C2Cr+D, B = AY+B3Cb+C3Cr+D

Offset Address: 2CF-2CCh
T Logic Adder Result 1
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:0	RW	0	T Logic Adder Result 1

Offset Address: 2D3-2D0h
Graphic Hardware Cursor Mode Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RW	0	Mono Cursor Display Path 0: Primary 1: Secondary
30:29	RW	00b	Target of The Hardware Cursor Buffer Starting Address 00: S.L. 01: S.F. 10: Reserved 11: L.L.
28:26	RO	0	Reserved
25:8	RW	0	Hardware Cursor Base Address Up to 64M bytes For 32x32x2 pattern: Bits [25:8] define the base address For 64x64x2 pattern: Bits [25:10] define the base address
7:2	RO	0	Reserved
1	RW	0	Hardware Cursor Size 0: 64x64x2 1: 32x32x2
0	RW	0	Hardware Cursor Enable 0: Disable 1: Enable

Offset Address: 2D7-2D4h
Graphic Hardware Cursor Position
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:27	RO	0	Reserved
26:16	RW	0	Hardware Cursor Position in the X-coordinate
15:11	RO	0	Reserved
10:0	RW	0	Hardware Cursor Position in the Y-coordinate

Offset Address: 2DB-2D8h
Graphic Hardware Cursor Origin
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:27	RO	0	Reserved
26:16	RW	0	Hardware Cursor Origin in the X-coordinate
15:11	RO	0	Reserved
10:0	RW	0	Hardware Cursor Origin in the Y-coordinate

Offset Address: 2DF-2DCh
Graphic Hardware Cursor Background
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:24	RO	0	Reserved
23:0	RW	0	For 256 Color Mode Bits [7:0] specify hardware cursor background color For 555 Hi Color Mode Bits [14:0] specify hardware cursor background color For 565 Hi Color Mode Bits [15:0] specify hardware cursor background color For 32-bits True Color Mode Bits [23:0] specify hardware cursor background color

Offset Address: 2E3-2E0h

Graphic Hardware Cursor Foreground

Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:24	RO	0	Reserved
23:0	RW	0	For 256 Color Mode Bits [7:0] specify hardware cursor foreground color. For 555 Hi Color Mode Bits [14:0] specify hardware cursor foreground color. For 565 Hi Color Mode Bits [15:0] specify hardware cursor foreground color. For 32-bits True Color Mode Bits [23:0] specify hardware cursor foreground color.

Table 3 below shows the hardware color cursor operation. Please be noted this table is only applicable to the graphics modes. For the text modes, the VGA registers control the hardware color cursor.

Table 3. Graphics Hardware Color Cursor Operation

Pixel Operation	AND Plane	XOR Plane
Choose graphics hardware color cursor background color	0	0
Choose graphics hardware color cursor foreground color	0	1
Transparent	1	0
VGA data is inverted	1	1

Offset Address: 2E7-2E4h

T Logic Data Result 1

Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:0	RW	0	T Logic Data Result 1

Offset Address: 2EB-2E8h

HI FIFO Depth and Threshold Control (Only For Primary Display)

Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:24	RW	0	HI FIFO Pre-threshold Let HI to issue request early. Normally, this value is more than or equal to HI FIFO threshold (Rx2E8[14:8]). (Unit: level)
23:16	RO	0	Reserved
15:8	RW	0	HI FIFO Threshold Let HI request priority from low to high. (Unit: level)
7:0	RO	0	HI FIFO Depth (- 1) Unit: level

Offset Address: 2EF-2ECh

Hardware Icon (HI) Transparent Color (Only For Primary Display)

Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:30	RO	0	Reserved
29:0	RW	0	HI Transparent Color Bits [29:0]: For RGB10 Bits [23:0]: For RGB32 Bits [15:0]: For RGB565 Bits [14:0]: For RGB555

Offset Address: 2F3-2F0h
Hardware Icon (HI) Control (Only for Primary Display)
Default Value: 000F 00F0h

Bit	Attribut	Default	Description
31	RO	0	Reserved
30	RW	0	HI Window Pre-fetch Enable
29	RW	0	HWI + (1-alpha)*Graphics Mode 0 Disable 1 Enable
28	RW	0	Alpha Value Come From Where Only for the true color hardware icon. 0: From bit [23:16] 1: From the bit [31:24] of hardware icon
27:26	RW	00b	HI Window Size 00: 32 x 32 01: 64 x 64 1x: 128 x 128 Unit: Pixel x line
25:24	RW	00b	HI Data Stream Format 00: RGB555 01: RGB565 10: RGB32 11: RGB10
23:20	RO	0	Reserved
19:16	RW	Fh	HI Constant Alpha [3:0] (HIAPA)
15:12	RW	0	Alpha Changed Value (HICV) Per Frame as HI Fan In / Out Turn On Rx260[8] ALPHAn[7:0] = ALPHAn-1[7:0] +/- HICV[3:0], where just ALPHAn[7:4] is valid alpha value and ALPHA0 = {HIAPA}.
11:10	RO	0	Reserved
9	RW	0	HI Fan In / Out Selector 0: Default 1: Fan in (+)
8	RW	0	HI Fan In / Out Enable 0: Disable 1: Enable
7:4	RW	Fh	HI Constant Alpha[7:4] (HIAPA) The Rest Bits are put on bits [19:16]
3	RW	0	V5 Request Length Disable 0: Enable length 1: Disable length Length = 0
2	RW	0	HI Blending Enable 0: Default 1: Enable
1	RW	0	V5 scaling enable on IGA1 0: Disable V5 scaling on IGA1 1: enable V5 scaling on IGA1
0	RW	0	HI Enable 0: Default 1: Enable

Offset Address: 2F7-2F4h
Hardware Icon Frame Buffer Starting Address (Only For Primary Display)
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RO	0	Reserved
30:29	RW	00b	Target of The Frame Buffer Starting Address 00: S.L. 01: S.F. 10: Reserved 11: L.L.
28:4	RW	0	Frame Buffer Starting Address for Hardware Icon Unit: 16 bytes
3:0	RO	0	Reserved

Offset Address: 2FB-2F8h
Hardware Icon (HI) Horizontal and Vertical Location Start (Only For Primary Display) Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:27	RO	0	Reserved
26:16	RW	0	Hardware Icon Horizontal (X) Starting Location Unit: Pixel
15:11	RO	0	Reserved
10:0	RW	0	Hardware Icon Vertical (Y) Starting Location Unit: Line

Offset Address: 2FF-2FCh
Hardware Icon (HI) Center Offset (Only For Primary Display) Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:23	RO	0	Reserved
22:16	RW	0	Hardware Icon Horizontal (X) Center Offset Unit: Pixel
15:7	RO	0	Reserved
6:0	RW	0	Hardware Icon Horizontal (Y) Center Offset Unit: Line

Offset Address: 1203-1200h
Video Gamma Color R Register for Video 1 Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:26	RO	0	Reserved
25:16	RW	0	Color Value After Gamma Function
15:5	RO	0	Reserved
4:0	RW	0	Color Index Number for Gamma Function Division

Offset Address: 1207-1204h
Video Gamma Color G Register for Video 1 Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:26	RO	0	Reserved
25:16	RW	0	Color Value After Gamma Function
15:5	RO	0	Reserved
4:0	RW	0	Color Index Number for Gamma Function Division

Offset Address: 120B-1208h
Video Gamma Color B Register for Video 1 Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:26	RO	0	Reserved
25:16	RW	0	Color Value After Gamma Function
15:5	RO	0	Reserved
4:0	RW	0	Color Index Number for Gamma Function Division

Offset Address: 120F-120Ch
Hardware Icon (HI) Inverse Color (Only For Primary Display) Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:30	RO	0	Reserved
29:0	RW	0	HI Inverse Color Bits [29:0]: For RGB10 Bits [23:0]: For RGB32 Bits [15:0]: For RGB565 Bits [14:0]: For RGB555

Offset Address: 1223-1220h
Video Gamma Color R Register for Video 3
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:26	RO	0	Reserved
25:16	RW	0	Color Value After Gamma Function
15:5	RO	0	Reserved
4:0	RW	0	Color Index Number for Gamma Function Division

Offset Address: 1227-1224h
Video Gamma Color G Register for Video 3
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:26	RO	0	Reserved
25:16	RW	0	Color Value After Gamma Function
15:5	RO	0	Reserved
4:0	RW	0	Color Index Number for Gamma Function Division

Offset Address: 122B-1228h
Video Gamma Color B Register for Video 3
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:26	RO	0	Reserved
25:16	RW	0	Color Value After Gamma Function
15:5	RO	0	Reserved
4:0	RW	0	Color Index Number for Gamma Function Division

Offset Address: 122F-122Ch
Video Window 3 Horizontal and Vertical Starting Location Offset
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:27	RO	0	Reserved
26:16	RW	0	Video Window 3 Horizontal (X) Starting Location Offset (Unit: 16 bytes)
15:11	RO	0	Reserved
10:0	RW	0	Video Window 3 Vertical (Y) Starting Location Offset (Unit: Line)

Offset Address: 1283-1280h
Interrupt Flags and Masks Control
Default Value: 0000 0000h

Bit	Attribut	Default	Description
31	RW1C	0	MSI Pending Interrupt Re-trigger Bit When SW wants to exit interrupt service, please clear the bit. HW may send out interrupt again if pending interrupt exists. The function is enabled when MSI Enable = 1'b1.
30:20	RO	0	Reserved
19	RW	0	DMA3 Transfer Done Interrupt Enable 0: Disable 1: Enable
18	RW	0	DMA3 Descriptor Done Interrupt Enable 0: Disable 1: Enable
17	RW	0	DMA2 Transfer Done Interrupt Enable 0: Disable 1: Enable
16	RW	0	DMA2 Descriptor Done Interrupt Enable 0: Disable 1: Enable
15:5	RO	0	Reserved
4	RO	0	CRT Sense Interrupt Status
3	RO	0	DMA3 Transfer Done Interrupt Status
2	RO	0	DMA3 Descriptor Done Interrupt Status
1	RO	0	DMA2 Transfer Done Interrupt Status
0	RO	0	DMA2 Descriptor Done Interrupt Status

Note: Write 1 to bit [4:0] to clear bits

Offset Address: 1287-1284h
Logic Signature Setting
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:8	RO	0	Reserved
7	RW	0	T Signature RD Disable 1
6	RW	0	P & T Select Signal 1
5	RW	0	T Signature Enable 1
4	RW	0	P Signature Enable 1
3	RW	0	T Signature RD Disable 0
2	RW	0	P & T Select Signal 0
1	RW	0	T Signature Enable 0
0	RW	0	P Signature Enable 0

Offset Address: 128B-1288h
P Logic Adder Result 0
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:0	RW	0	P Logic Adder Result 0

Offset Address: 128F-128Ch
T Logic Adder Result 0
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:0	RW	0	T Logic Adder Result 0

Offset Address: 1293-1290h
IGA1 Display Position Counter 0
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:16	RO	0	IGA1 Display Line Counter
15:0	RO	0	IGA1 Display Frame Counter

Offset Address: 1297-1294h
IGA1 Display Position Counter 1
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:16	RO	0	Reserved
15:0	RO	0	IGA1 Display Frame Counter

Offset Address: 129B-1298h
IGA1 Display Position Counter 2
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:16	RO	0	Reserved
15:0	RW	0	IGA1 Display Frame Counter Enable 0: Disable 1: Enable When this bit is disabled, frame counter always gets 16'h0.

Offset Address: 129F-129Ch
T Logic Data Result 0
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:0	RW	0	T Logic Data Result 0

Offset Address: 12A3-12A0h
IGA2 Display Position Counter 0
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:16	RO	0	IGA2 Display Line Counter
15:0	RO	0	IGA2 Display Frame Counter

Offset Address: 12A7-12A4h
IGA2 Display Position Counter 1
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:16	RO	0	Reserved
15:0	RO	0	IGA2 Display Frame Counter

Offset Address: 12AB-12A8h
IGA2 Display Position Counter 2
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:16	RO	0	Reserved
15:0	RW	0	IGA2 Display Frame Counter Enable 0: Disable 1: Enable When this bit is disabled, frame counter always gets 16'h0.

Offset Address: 12B3-12B0h
Primary Display Data Color Space Conversion and Enhancement Control 1
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:30	RO	0	Reserved
29:20	RW	0	A1 <= XXXXXXXXXXXX
19:10	RW	0	B1 <= XXXXXXXXXXXX
9:0	RW	0	C1 <= XXXXXXXXXXXX

 Note: $Y = A1R + B1G + C1B + D$

Coefficient A1, B1, C1: 10 bits, 0.XXXXXXXXXX from 0 to 0.99903 Coefficient D: 8 bit positive integer from 16 to 255

Offset Address: 12B7-12B4h
Primary Display Data Color Space Conversion and Enhancement Control 2
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:30	RO	0	Reserved
29:20	RW	0	A2[9:0] <= XXXXXXXXXXXX
19:10	RW	0	B2[9:0] <= XXXXXXXXXXXX
9:0	RW	0	C2[9:0] <= XXXXXXXXXXXX

 Note: $Cr = A2R + B2G + C2B + 128$

Coefficient A2, B2, C2: 11 bits S.XXXXXXXXXX 2's complement from -0.99903 to 0.99903

Offset Address: 12BB-12B8h
Primary Display Data Color Space Conversion and Enhancement Control 3
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:30	RO	0	Reserved
29:20	RW	0	A3[9:0] <= XXXXXXXXXXXX
19:10	RW	0	B3[9:0] <= XXXXXXXXXXXX
9:0	RW	0	C3[9:0] <= XXXXXXXXXXXX

 Note: $Cr = A3R + B3G + C3B + 128$

Coefficient A3, B3, C3: 11 bits S.XXXXXXXXXX 2's complement from -0.99903 to 0.99903

Offset Address: 12BF-12BCh
Primary Display Data Color Space Conversion and Enhancement Control 4
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:14	RO	0	Reserved
13	RW	0	A2[10] <= S
12	RW	0	B2[10] <= S
11	RW	0	C2[10] <= S
10	RW	0	A3[10] <= S
9	RW	0	B3[10] <= S
8	RW	0	C3[10] <= S
7:0	RW	0	D

DVD / Video Control Register (3260-326Ch)
Offset Address: 3260h

DVD / Video ID Control - Refer to 3D Chapter's "CR Registers in Video Control Register Space" for more details

Offset Address: 326Ch

DVD / Video Wait Control - Refer to 3D Chapter's "CR Registers in Video Control Register Space" for more details

Video Capture Engine Register Descriptions (300-37Ch)

Offset Address: 303-300h
Capture Interrupt Control and Flags
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:11	RO	0	Reserved
10	RW	0	Current Writing VBI Buffer ID
9	RW	0	End of VBI Interrupt Enable
8	RW	0	End of Active Video Interrupt Enable If TS (Transport Stream) is enabled, it defines as TS data over a buffer interrupt enable.
7	RO	0	Video Capture Port Internal FIFO Full Status
6	RO	0	Current Active Video Input Field Status 0: Top field 1: Bottom field
5	RO	0	Current Input Vsync Status 0: Vertical blanking 1: Active video
4:3	RO	0	Current Writing Active Video (or TS data) Frame Buffer ID
2	RO	0	Flipping Active Video Field Status 0: Top field 1: Bottom field
1	RO	0	Video Capture End-of-VBI Status
0	RO	0	Video Capture End-of-Active Video Status If TS is enabled, it defines as TS data over a buffer status

Note: Write 1 to clear bits [1:0] and [7]

Offset Address: 30B-308h
Transport Stream Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:23	RO	0	Reserved
22	RW	0	Serial Input Enable 0: Enable parallel TS input 1: Enable serial TS input
21	RW	0	Bit Alignment Serial input mode only 0: LSB first 1: MSB first
20	RW	0	Packet Starting Signal Disable 0:Enable 1:Disable
19	RW	0	Change Buffer Mode 0: According to count packet number 1: According to byte count
18:4	RW	0	When bit 19 = 0 Packet_Number_Minus_One There are (Packet_Number_Minus_One + 1) packets per buffer. When bit 19 = 1 KBytes_Count There are KBytes_Count Kbytes per buffer.
3:2	RW	00b	Method to Move Received TS Data 0x: Capture engine write data to FB. After fill a buffer, trigger an interrupt to driver. 10: Capture engine write data to FB. After fill a buffer, trigger an interrupt to DMA. 11: Capture engine control DMA to move data. (not via frame buffer) (In mode = 2'b11, set FIFO Threshold Rx310[27:24] to 1)
1	RW	0	Drop Error Packet This bit is only valid when TS_DERR pin is available 0: Write all received data out. 1: Drop the data of error packet
0	RW	0	Transport Stream Input Enable 0: Disable 1: Enable Turn on this bit before enabling capture engine Rx310[0].

Offset Address: 313-310h
Capture Interface Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RW	0	Capture CLK Enable 0: Disable 1: Enable This bit should be turned on before Rx310[0].
30	RW	0	Capture FIELD Signal Output Inverted Select 1: Inverted
29	RW	0	Vertical Count Starting Reference 0: Negative edge of VREF 1: Positive edge of VREF
28	RW	0	Horizontal Count Starting Reference 0: Negative edge of HREF 1: Positive edge of HREF
27:24	RW	0	Capture FIFO Threshold (Unit: level) Once the queuing captured data is more than the threshold, it starts to write data out. Unit of the 1st capture engine is 4-levels, the FIFO size is 64 level x 64 bit. Unit of the 2nd capture engine is 2-levels, the FIFO size is 32 level x 64 bit.
23	RW	0	Switch Capture Clock Source Since there are two capture clock sources, use this bit to switch it. In VIP2.0 while using task bit to differentiate video stream, it needs to switch the clock source as the same one. For 1st Capture Engine: 0: Clock from 1st capture CLK pin 1: Clock from 2nd capture CLK pin For 2nd Capture Engine: 0: Clock from 2nd capture CLK pin 1: Clock from 1st capture CLK pin
22	RW	0	Capture FIELD Input Inverted Select 1: Inverted
21	RW	0	Capture HREF Input Inverted Select 1: Inverted
20	RW	0	Capture VREF Input Inverted Select 1: Inverted
19	RW	0	Capture CLK Input Inverted Select 1: Inverted
18:16	RW	000b	Capture Horizontal Filter Mode Select (2P) 000: No filtering 001: 2 tap (1,1)/2 010: 3 tap (1,2,1)/4 011: 4 tap (1,3,3,1)/8 100: 5 tap (1,2,2,2,1)/8 101~111:Reserved
15	RW	0	Capture Flipping Control When Rx310[13:12] Is Set to 11b 0: Capture engine flips to HQV or video engine after captured a frame. 1: Capture engine flips to HQV or video engine after captured a field (HQV or Video should set to frame_to_field).
14	RW	0	4:2:2 to 4:4:4 Cb, Cr Type Select 0: Duplication 1: Interpolation
13:12	RW	00b	Capture De-interlace Mode Select 00: Capture odd field only, 30fps 01: Capture even field only, 30fps 10: Capture odd / even field, 60fps; place on the same location 11: Capture odd / even field, 30fps; place in interlace fashion doubling the storage space
11	RW	0	Input FIELD Signal Enable If TS is enabled, it defines as TS_DERR signal enable. 0: Disable 1: Enable
10	RW	0	VIP Type 0: VIP1.1, VBI data region specify by task bit. 1: VIP2, VBI data region specify by SAV / EAV during vertical blanking period.

(Continued for Rx310h)

Bit	Attribute	Default	Description
9:8	RW	00b	Byte Swapping Control 00: 0123 (no swap: YUYV) 01: 1032 (C, Y swap: UYVY) 10: 0321 (Cr, Cb swap: YVYU) 11: 3012 (Cr, Cb swap and Y swap: VYUY)
7	RW	0	16 Bit Input Low/High Swap 1: Low/high byte inverted
6	RW	0	CCIR656-16 Bit Header Decode Mode 0: Low 8bit 1: 16bit all
5:4	RW	00b	Input Stream Type 00: CCIR601-8bit 01: CCIR656-8bit 10: CCIR601-16bit 11: CCIR656-16bit
3	RW	0	VIP Enable 0: Disable 1: Enable
2	RW	0	Buffer Mode 0: Double buffers, use starting address 1 and 2 1: Triple buffers, use starting address 1, 2 and 3
1	RW	0	Bit Stream Selection of VIP2.0 In VIP2.0, task bit to differentiate video stream. For the 1st capture engine: 0: Capture the data of task bit is 0 1: Capture the data of task bit is 1 For the 2nd capture engine: 0: Capture the data of task bit is 1 1: Capture the data of task bit is 0
0	RW	0	Capture Enable 0: Disable 1: Enable

Offset Address: 317-314h
Active Video Horizontal Range
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:30	RO	0	Reserved
27:16	RW	0	Horizontal Ending Line (CCIR601 only). (Unit: Line)
15:12	RO	0	Reserved
11:0	RW	0	Horizontal Starting Line (CCIR601 only). (Unit: Line)

Offset Address: 31B-318h
Active Video Vertical Range
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:30	RO	0	Reserved
27:16	RW	0	Vertical Ending Line (CCIR601 only). (Unit: Line)
15:11	RO	0	Reserved
10:0	RW	0	Vertical Starting Line (CCIR601 only). (Unit: Line)

Offset Address: 31F-31Ch
Active Video Scaling Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:28	RO	0	Reserved
26	RW	0	Vertical Minify Enable 0: Disable 1: Enable
25:16	RW	0	Vertical Minify Factor
15:12	RO	0	Reserved
11	RW	0	Horizontal Minify Enable 0: Disable 1: Enable
10:0	RW	0	Horizontal Minify Factor

Offset Address: 323-320h
VBI Data Horizontal Range
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:28	RO	0	Reserved
27:16	RW	0	Horizontal Ending Line (Unit: Line)
15:12	RO	0	Reserved
11:0	RW	0	Horizontal Starting Line (Unit: Line)

Offset Address: 327-324h
VBI Data Vertical Range
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:27	RO	0	Reserved
26:16	RW	0	Vertical Ending Line (Unit: Line)
15:11	RO	0	Reserved
10:0	RW	0	Vertical Starting Line (Unit: Line)

Offset Address: 32B-328h
First VBI Buffer Starting Address
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RW	0	VBI Data Enable 0: Disable 1: Enable
30	RW	0	VBI Mode Select 0: Range depend on SAV/EAV 1: Capture by specify range (define by register 320h, 324h) If VIP enable (Rx310[3]=1), this bit setting would be ignored, capture VBI data defined as VIP spec.
29	RO	0	Reserved
28:4	RW	0	VBI or ANC Buffer 0 Starting Address (Unit: 16 bytes)
3:2	RO	0	Reserved
1:0	RW	00b	Buffer Selection 00: S.L 01: S.F 10: S.M 11: L.L

Offset Address: 32F-32Ch
VBI Buffer Stride
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:14	RO	0	Reserved
13	RW	0	VBI Data Placement Method 0: Linear, no stride needed 1: With stride
12:4	RW	0	VBI Buffer Stride (Unit: 16 bytes)
3:0	RO	0	Reserved

Offset Address: 333-330h
Ancillary Data Count Setting
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:15	RO	0	Reserved
14	RW	0	Ancillary Data Type 0: Type2 – 00-FF-FF-DID-SDID-NN-.....-ChecksumByte-FillBytes. Total captured data are (8Bytes + NN*4Bytes). 1: Type1 – 00-FF-FF-DID-DBN-NN-.....-ChecksumByte-FillBytes. Total captured data are (8Bytes + (DBN+NN)*4Bytes).
13	RW	0	Ancillary Data Enable 0: Disable 1: Enable
12	RW	0	Ancillary Data Count Reference Select 0: By header decoder 1: By register (define by Rx330[11:0]).
11:0	RW	0	Ancillary Data Should Be Capture Length (Unit: Double-word)

Offset Address: 337-334h
Maximum Data Count of Active Video
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:26	RO	0	Reserved
26:16	RW	0	Maximum Active Video Line Count In A Field (Unit: Line) If TS enable, it defines as the maximum TS data count of a packet (Unit: Byte)
15:9	RO	0	Reserved
8:0	RW	0	Maximum Active Video QW Count In A Line (Unit: 8 bytes)

Offset Address: 33B-338h
Maximum Data Count of VBI or ANC
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:26	RO	0	Reserved
26:16	RW	0	Maximum VBI or ANC Line Count In A Field (Unit: Line)
15:9	RO	0	Reserved
8:0	RW	0	Maximum VBI or ANC QW Count In A Line (Unit: 8 bytes)

Offset Address: 33F-33Ch
Capture Data Count
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:27	RO	0	Reserved
26:16	RW	0	Current Active Video Line Counter (Unit: Line)
15:13	RO	0	Reserved
12:0	RW	0	VBI or ANC Data Length That Has Been Captured (Unit: 8 bytes)

Offset Address: 343-340h
First Active Video Frame Buffer Starting Address
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:29	RO	0	Reserved
28:4	RW	0	Active Video Frame Buffer 0 Starting Address (Unit: 16 bytes) If TS is enabled, it defines as frame buffer 0 starting address for TS data.
3:2	RO	0	Reserved
1:0	RW	00b	Buffer Selection 00: S.L 01: S.F 10: S.M 11: L.L

Offset Address: 347-344h
Second Active Video Frame Buffer Starting Address
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:29	RO	0	Reserved
28:4	RW	0	Active Video Frame Buffer 1 Starting Address (Unit: 16 bytes) If TS is enabled, it defines as frame buffer 1 starting address for TS data.
3:2	RO	0	Reserved
1:0	RW	00b	Buffer Selection 00: S.L 01: S.F 10: S.M 11: L.L

Offset Address: 34B-348h
Third Active Video Frame Buffer Starting Address
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:29	RO	0	Reserved
28:4	RW	0	Active Video Frame Buffer 2 Starting Address (Unit: 16 bytes) If TS is enabled, it defines as frame buffer 2 starting address for TS data.
3:2	RO	0	Reserved
1:0	RW	00b	Buffer Selection 00: S.L 01: S.F 10: S.M 11: L.L

Offset Address: 34F-34Ch
Second VBI Buffer Starting Address
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:29	RO	0	Reserved
28:4	RW	0	VBI or ANC Buffer 1 Starting Address (Unit: 16 bytes)
3:2	RO	0	Reserved
1:0	RW	00b	Buffer Selection 00: S.L 01: S.F 10: S.M 11: L.L

Offset Address: 353-350h
Stride of Active Video Buffer & Coring Function Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:24	RO	0	Reserved
23	RW	0	Coring Function Enable
22:16	RW	0	Coring Function Compare Data (CCD) If coring function enable (Rx350[23]) and $-(\text{CCD}+1) \leq U, V \leq \text{CCD}$, then all of these U and V will be truncated to zero)
15:13	RO	0	Reserved
12:4	RW	0	Stride of Active Video Buffer (Unit: 8 bytes)
3:0	RO	0	Reserved

Offset Address: 357-354h
TS Buffer 0 Error Packet Indicator
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RO	0	Last Error Packet Indicator 0: Less than one error packet in this buffer, defined at bits [15:0] 1: More than two error packets, the last error packet ID defined at bits [30:16]
30:16	RO	0	Last Error Packet ID
15	RO	0	First Error Packet Indicator 0: No error packet in this buffer 1: More than one error packet, the first error packet ID defined at bits [14:0]
14:0	RO	0	First Error Packet ID

Offset Address: 35B-358h
TS Buffer 1 Error Packet Indicator
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RO	0	Last Error Packet Indicator 0: Less than one error packet in this buffer, defined at bits [15:0] 1: More than two error packets, the last error packet ID defined at bits [30:16]
30:16	RO	0	Last Error Packet ID
15	RO	0	First Error Packet Indicator 0: No error packet in this buffer 1: More than one error packet, the first error packet ID defined at bits [14:0]
14:0	RO	0	First Error Packet ID

Offset Address: 35F-35Ch
TS Buffer 2 Error Packet Indicator
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RO	0	Last Error Packet Indicator 0: Less than one error packet in this buffer, defined at bits [15:0] 1: More than two error packets, the last error packet ID defined at bits [30:16]
30:16	RO	0	Last Error Packet ID
15	RO	0	First Error Packet Indicator 0: No error packet in this buffer 1: More than one error packet, the first error packet ID defined at bits [14:0]
14:0	RO	0	First Error Packet ID

Note:

Capture supports 2 input interface; therefore, an additional register space is provided to match the above registers definition.

Writing a register to this space, it will write to the second Capture Engine.

The relationship between the additional register space and original register space is

(The additional register address) = (The original register address) + 16'h1000.

HQV Engine Register Descriptions (380-3FFh)

Offset Address: 383-380h

HQV Source Data Offset Control 1

Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:27	RO	0	Reserved
26:16	RW	0	Horizontal Offset of Start Point for Video Location In Destination Picture Unit: pixel (2P) Either video or sub-picture destination data horizontal offset of start point should be set to zero.
15:11	RO	0	Reserved
10:0	RW	0	Vertical Offset of Start Point for Video Location In Destination Picture Unit: line (2P) Either video or sub-picture destination data vertical offset of start point should be set to zero.

Offset Address: 387-384h

HQV Source Data Offset Control 2

Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:27	RO	0	Reserved
26:16	RW	0	Horizontal Offset of Start Point for Sub-picture Location In Destination Picture Unit: pixel (2P) Either video or sub-picture destination data horizontal offset of start point should be set to zero.
15:11	RO	0	Reserved
10:0	RW	0	Vertical Offset of Start Point for Sub-picture Location In Destination Picture Unit: line (2P) Either video or sub-picture destination data vertical offset of start point should be set to zero.

Offset Address: 38B-388h

HQV Source Data Offset Control 3

Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:27	RO	0	Reserved
26:16	RW	0	Horizontal Offset of End Point for Video Location In Destination Picture Unit: pixel (2P)
15:11	RO	0	Reserved
10:0	RW	0	Vertical Offset of End Point for Video Location In Destination Picture Unit: line (2P)

Offset Address: 38F-38Ch

HQV Source Data Offset Control 4

Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:27	RO	0	Reserved
26:16	RW	0	Horizontal Offset of End Point for Sub-picture Location In Destination Picture Unit: byte (2P)
15:11	RO	0	Reserved
10:0	RW	0	Vertical Offset of End Point for Sub-picture Location In Destination Picture Unit: line (2P)

Offset Address: 393-390h
HQV Parameters of Hardware Tuning Performance / Quality
Default Value: 4664 8688h

Bit	Attribute	Default	Description
31	RO	0	Reserved
30:28	RW	100b	Threshold of Inter-Field Complexity for Pull Down Detection (x4) Calculate the difference between current & previous field.
27	RO	0	Reserved
26:25	RW	11b	Factor of Calculating Threshold of Intra-Field Complexity 00: Threshold = 390[30:28]*4 + 390[30:28]*1 01: Threshold = 390[30:28]*4 + 390[30:28]*2 10: Threshold = 390[30:28]*4 + 390[30:28]*3 11: Threshold = 390[30:28]*4 + 390[30:28]*4
24:23	RO	0	Reserved
22:21	RW	11b	Static Judgment Number (SJNI) As static record number is equal to SJNI, then static flag is asserted
20	RW	0	The Field Number for The Increment of Static Record 0: 1 field / (static record) 1: 2 fields / (static record)
19:18	RW	01b	Pull-down Factor 2 Apply this factor while pull-down detected 00: 3/8 01: 4/8 10: 5/8 11: 6/8
17:16	RW	00b	Pull-down Factor 1 Apply this factor while pull-down not yet detected. 00: 2/8 01: 3/8 10: 4/8 11: 5/8
15:14	RW	10b	Threshold for Pull Down Detection (Rx3DC.[10:0]<<Rx390.[15:14]) as the minimum threshold for valid pull down detection
13:12	RO	0	Reserved
11:8	RW	6h	Threshold for Motion Detection (x2)
7:4	RW	8h	Edge Detection Threshold: for Degree 90 (x2)
3:0	RW	8h	Maximum Difference between Block Boundary (x4) Apply de-blocking with sin(x) function while the difference between block boundary is greater than this setting.

Offset Address: 397-394h
HQV Extended Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:8	RO	0	Reserved
7	RW	0	Color Adjustment Enable 0: Disable 1: Enable
6	RW	0	Bob De-interlacing Method 0: Line average 1: Line duplication (for TV output)
5	RW	0	YUV Output Format Control (2P) 0: YUV422 out 1: YUV444 out This bit is effective when (H or V scaling size) < (1/2 H or V original) size. For the other cases, it just uses YUV422 out
4	RW	0	Color Space Conversion Method 0: BT601 1: BT709
3	RW	0	Color Format Convert Method (from YUV420 → YUV422) 0: 4-tap interpolation 1: Method 1 (-1 9 9 -1).
2:1	RW	00b	Color Format Convert Method (from YUV422 → YUV444) 00: Method 1 (WMV9 and H.264) 01: Reserved 1x: Method 3 (-1 9 9 -1)
0	RW	0	Color Format Convert Method (from YUV444 → YUV422) 0: Method 1 (1 1) 1: Method 2 (Drop) This bit is effective as (no scaling) or (scaling size) > (1/2 original size). For the other cases, it just uses method 2.

Offset Address: 39B-398h
HQV Static Record Frame Buffer Starting Address
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:29	RO	0	Reserved
28:4	RW	0	Static Record Frame Buffer Starting Address Unit: 16 bytes
3:2	RO	0	Reserved
1:0	RW	0	Memory Location

Offset Address: 39F-39Ch
HQV Static Record Frame Buffer Stride
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:14	RO	0	Reserved
9:4	RW	0	Static Record Frame Buffer Stride Unit: 16 bytes
3:0	RO	0	Reserved

Offset Address: 3A3-3A0h
HQV Color Adjustment Control 1
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:30	RO	0	Reserved
29:20	RW	0	Coefficient C1(s[28:27].[26:20]) (2p)
19:10	RW	0	Coefficient B1(s[18:17].[16:10]) (2p)
9:0	RW	0	Coefficient A1(s[8:7].[6:0]) (2p)

 Note: $Y'(R') = A1*Y(R) + B1*Cb(G) + C1*Cr(B) + D1$

Offset Address: 3A7-3A4h
HQV Color Adjustment Control 2
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:30	RO	0	Reserved
29:20	RW	0	Coefficient C2(s[28:27],[26:20]) (2p)
19:10	RW	0	Coefficient B2(s[18:17],[16:10]) (2p)
9:0	RW	0	Coefficient A2(s[8:7],[6:0]) (2p)

 Note: $Cb'(G') = A2*Y(R) + B2*Cb(G) + C2*Cr(B) + D2$
Offset Address: 3AB-3A8h
HQV Color Adjustment Control 3
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:30	RO	0	Reserved
29:20	RW	0	Coefficient C3(s[28:27],[26:20]) (2p)
19:10	RW	0	Coefficient B3(s[18:17],[16:10]) (2p)
9:0	RW	0	Coefficient A3(s[8:7],[6:0]) (2p)

 Note: $Cr'(B') = A3*Y(R) + B3*Cb(G) + C3*Cr(B) + D3$
Offset Address: 3AF-3ACh
HQV Color Adjustment Control 4
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:30	RO	0	Reserved
29:20	RW	0	Coefficient D3(s[28:21],[20]) (2p)
19:10	RW	0	Coefficient D2(s[18:11],[10]) (2p)
9:0	RW	0	Coefficient D1(s[8:1],[0]) (2p)

Offset Address: 3B3-3B0h
HQV Horizontal Scale Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RW	0	Horizontal Scale Enable 1: Enable (2p)
30	RO	0	Reserved
29:28	RW	00b	Horizontal Scale Function (2P) 00: Scale up 01: 1~1/4 10: 1/4~1/8* 11: <1/8
27:15	RO	0	Reserved
14:0	RW	0	Horizontal Scale Factor [14:12],[11:0] (2p)

Note: Scale factor:

1. Scale up: source/destination
2. 1~1/4: source/(destination+0.5)
3. 1/4~1/8*: source/destination.
4. <1/8: destination/source

Offset Address: 3B7-3B4h
HQV Vertical Scale Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RW	0	Vertical Scale Enable 1: Enable (2p)
30:29	RO	0	Reserved
28	RW	0	Vertical Scale Function (2p) 0: Scale up. 1: Scale down
27:17	RO	0	Reserved
16:0	RW	0	Vertical Scale Factor [16:12].[11:0] (2p)

Note: Scale factor

1. Scale up: source/destination;
2. Scale down: source/(destination+0.5)

PS:

For all scaling calculation, the final results should be rounded to the nearest integer(round off).

 For bi-linear factor, please use 6 binary fraction of factor (need be rounded to the nearest 6th fraction) to do the calculation.

Offset Address: 3BB-3B8h
HQV Default Video Color
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:30	RO	0	Reserved
29:20	RW	0	Luma(Y) or Red Color Value
19:10	RW	0	Chroma(Cb) or Green Color Value
9:0	RW	0	Chroma(Cr) or Blue Color Value

Offset Address: 3BF-3BCh
HQV De-blocking Factor
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:20	RO	0	Reserved
19:18	RO	0	HQV Current Process Destination Buffer ID
17	RW	0	HQV Output Field 1: Bottom field
16	RW	0	HQV Current Process Field 1: Bottom field
15:0	RO	0	Reserved

Offset Address: 3C3-3C0h
HQV Sub-picture Frame Buffer Stride and Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:24	RW	0	MC Flipping Count For MC flip to HQV path: Read only For SW flip path: R/W HQV update read out register data at the beginning of HQV processing a frame.
23:20	RO	0	Reserved
19	RW	0	Sub-picture Format 0: AI44 or IA44 1: AYUV (MSB A(8)-Y(8)-U(8)-V(8) LSB)
18	RW	0	Inverse Alpha Value in AI44 Mode 1: Inverse (One's Complement)
17	RW	0	Alpha, Index Exchange in AI44 Mode 0: AI44 1: IA44
16	RW	0	HQV Sub-picture Enable 0: Disable 1: Enable Only active at HQV source format is YUV.
15:14	RO	0	Reserved
13:4	RW	0	Subpicture Frame Buffer Stride Unit: 16 bytes
3:0	RO	0	Reserved

Offset Address: 3C7-3C4h
HQV Sub-picture Frame Buffer Starting Address
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:29	RO	0	Reserved
28:4	RW	0	Sub-picture Frame Buffer Starting Address (Unit: 16 bytes)
3:2	RO	0	Reserved
1:0	RW	0	Memory Location

Offset Address: 3CB-3C8h
HQV Sub-picture 4x16 RAM Table Write Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:8	RW	0	RAM Table Write Data V: Bits [31:24] U: Bits [23:16] Y: Bits [15:8]
7:4	RW	0	RAM Table Read / Write Address Indicate which entry of palette table will be written or read. Palette table contains 16 entries of palette data. (HQV3C8[7:4] = 0x0000 ~ HQV3C8[7:4] = 0x1111) Need to program HQV3C8[31:8] and HQV3C8[7:4] 16 times to fill the subpicture palette table.
3	RO	0	Reserved
2	RW	0	V Write Enable 0: Disable 1: Enable
1	RW	0	U Write Enable 0: Disable 1: Enable
0	RW	0	Y Write Enable 0: Disable 1: Enable

Offset Address: 3D3-3D0h
HQV Stream Control and Status
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:28	RW	0	Video Data Stream Format [3:0] 0000: RGB32 – (X8R8G8B8) 0001: RGB32 – (X2R10G10B10) 0010: RGB16 – (R5G6B5) 0011: RGB15 – (X1R5G5B5) 0100: YUV444 – (X8Y8U8V8) 0101: V410 – (V10Y10U10X2) 1000: YUV422 – (V8Y _i U8Y _o 8) 1100: YUV420 – (NV12; planar mode) Others:reserved
27	RW	0	High Quality Video Enable 0: Disable 1: Enable
26	RW	0	Buffer Mode 0: Double destination buffers 1: Triple destination buffers
25:24	RW	00b	Video Stream Source [1:0] 00: SW 01: Reserved 10: Capture 0 11: Capture 1
23	RW	0	Advanced De-interlace Mode Enable Reference more than one field.
22	RW	0	Vertical Low Pass Filter Enable 0: Disable 1: Enable
21	RO	0	Reserved
20	RW	0	Planar Mode Chrominance Source Data Format 0: Source Chrominance is saved by frame picture 1: Source Chrominance is saved by field picture
19	RW	0	Inverse Input Field 1: Inversed
18	RW	0	Frame To Field 1: Frame base source, extract a field from a frame.
17	RW	0	Field To Frame 1: Field source, de-interlace to progressive frame.
16	RO	0	Reserved
15	RW	0	Sub-Picture Flip Software writes 1 to this bit indicates a new sub-picture need to blend. After blending completes, hardware clears it to 0. Software can read this bit to check the status if hardware completes blending.
14:13	RO	0	Reserved
12	RO	0	HQV Flip FIFO Full Status The FIFO depth defined in Rx3F8 [17:16]
11	RO	0	Reserved
10:8	RO	0	State Machine Status of HQV Flip Module
7	RW	0	HQV Interrupt Enable 0: Disable HQV interrupt. 1: HQV send interrupt signal after done a frame. Relative setting: Rx3D0[0].
6	RW	0	Single Destination Buffer 1: Single buffer used Rx3D0[26] would be ignored.
5	RW	0	Field of Software Source Input 0: Top 1: Bottom
4	RW	0	Software Source Flip Software writes 1 to flip a image to HQV. (Rx3D0[25:24] should be 00b) After processing completes, hardware clears it to 0. Software reads this bit to check flip status.
3	RO	0	HQV Engine Idle State 1: Idle
2:1	RO	0	HQV Output Buffer ID HQV destination buffer ID
0	RW	0	HQV End of Frame Status 1:HQV has been output an image. (Software writes 1 to clear this bit) After HQV done an image, this bit will be pulled high, and it will be pulled down only when software writes 1b to it.

Offset Address: 3D7-3D4h
HQV SW Source Data – Luma or Packed Starting Address
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RO	0	Reserved
30:29	RO	0	Reserved
28:4	RW	0	SW Source Data Y or Packed Mode Starting Address (Unit: 16 bytes)
3:2	RO	0	Reserved
1:0	RW	0	Memory Location

Offset Address: 3DB-3D8h
HQV SW Source Data – Chroma Starting Address
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:29	RO	0	Reserved
28:4	RW	0	SW Source Buffer U, V Starting Addresses (Unit: 16 bytes)
3:2	RO	0	Reserved
1:0	RW	0	Memory Location

Offset Address: 3DF-3DC h
HQV Linear / Tile Address Mode, Color Space Conversion, Gamma, De-blocking Control Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:30	RW	00b	Linear / Tile Address Mode Control (Tile address only enable at source data from MC, 3D0[25:24]=01) 00: Linear 01: Reserved 10: 256 bits tile mode (Addr = SA + (Y[10:4]*PTH*16) + {X[6:1],Y[3:0],X[0]}) 11: 512 bits tile mode (Addr = SA + (Y[10:4]*PTH*16) + {X[6:2], Y[3:0],X[1:0]}). Where unit of X is 128-bit; unit of Y is line.
29	RW	0	HQV Output Data Pack In 32-bits Mode. 0:16 bits (RGB565). 1:32 bits (RGB888) Only valid when the source is YUV and color space conversion is enabled.
28	RW	0	Color Space Conversion Enable 0: Disable 1: Enable
27	RW	0	De-blocking Enable
26:25	RO	0	Reserved
24:20	RW	0	HQV Output FIFO Threshold for Write Request Control (Unit: level) HQV output FIFO has 64 levels, once the data in output FIFO touch the threshold (32+3DC.[24:20]), the write request would be triggered.
19:16	RO	0	Reserved
15	RW	0	Constant Alpha of RGB32 Format 0: Alpha = 00 1: Alpha = FF
14	RW	0	Enable Synchronization Flipping Field with Interlaced IGA 1: Enable
13	RW	0	IGA Field Inverse 1: Inverse
12:11	RO	0	Reserved
10:0	RW	0	Image Size / 1024 Pull-down detection use.

Offset Address: 3E3-3E0h
HQV Source Data Line Count and Fetch Count Per Line
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:29	RO	0	Reserved
28:16	RW	0	Video Source Data Fetch Count Per Line (-1) Unit: Bytes
15:11	RO	0	Reserved
10:0	RW	0	Video Source Data Line Number (-1) Unit: Line

Offset Address: 3E7-3E4h
HQV Motion Adaptive De-interlace Control & Threshold
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RW	0	2:2 Pull Down Sequence Detection Enable 0: Disable 1: Enable Relative setting: Rx3DC[10:0]
30:28	RO	0	Reserved
27	RW	0	3:2 Pull Down Sequence Detection Enable 0: Disable 1: Enable Relative setting: Rx3DC[10:0]
26:25	RO	0	Reserved
24	RW	0	2:3:3:2 Pull Down Sequence Detection Enable 0: Disable 1: Enable Relative setting: Rx3DC[10:0]
23:13	RO	0	Reserved
12:8	RW	0	Motion Detection Enable
7	RO	0	2:2 Pull Down Detection Status
6	RO	0	3:2 Pull Down Detection Status
5	RO	0	2:3:3:2 Pull Down Detection Status
4:1	RO	0	Reserved
0	RW	0	Edge Detection Enable 0: Disable 1: Enable

Offset Address: 3EF-3ECh
HQV Destination Frame Buffer Starting Address 0
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RW	0	HQV Output Data Pack In 32 Bits xRGB2-10-10-10 Format After HQV's Color Space Conversion 1: Enable Note: Only one of {Rx3EC[31], Rx3DC[29]} can be set to 1.
30	RW	0	Enable Output In Tile Mode 1: Enable. Addr = ST_ADDR[28:4] + Y[10:3]*{PITCH[10:0], 3'b0} + {X[10:1], Y[2:0], X[0]}
29	RO	0	Reserved
28:4	RW	0	Destination Frame Buffer Starting Address 0 Unit: 16 bytes
3:2	RO	0	Reserved
1:0	RW	0	Memory Location

Offset Address: 3F3-3F0h
HQV Destination Frame Buffer Starting Address 1
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:29	RO	0	Reserved
28:4	RW	0	Destination Frame Buffer Starting Address 1 Unit: 16 bytes
3:2	RO	0	Reserved
1:0	RW	0	Memory Location

Offset Address: 3F7-3F4h
HQV Destination Frame Buffer Stride
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:14	RO	0	Reserved
13:4	RW	0	Destination Frame Buffer Stride (2P) Unit: 16 bytes
3:0	RO	0	Reserved

Offset Address: 3FB-3F8h
HQV Source Frame Buffer Stride
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RW	0	Load Starting Address Rx3D4[25:4], Rx3D8[25:4] for Advanced De-interlacing 0: Not used. Hardware keep starting address 1: Load starting address to current field Note: Command sequence Step1: Write Rx3D4, Rx3D8 Step2: Write Rx3F8; new address to PN Step3: Write Rx3D4, Rx3D8 Step4: Write Rx3F8; PN to PC; new address to PN Step5: Write Rx3D4, Rx3D8 Step6: Write Rx3F8; PC to PP; PN to PC; new address to PN
30	RW	0	SJN Reset 1: Reset static judgment number
29	RW	0	Pull Down Detection Low-Threshold Value For fixing bug: Spare register.
28	RW	0	Pull Down Detection Error Sequence Check One Time
27:26	RW	0	For Fixing Bug: Spare Register
25	RW	0	Not Check Size 0: Check size 1: Not check size
24:21	RW	0	For Fixing Bug. Spare Register
20	RW	0	Software Flip Queue Enable 0: Pull Rx3D0[4] low at frame done. 1: Pull Rx3D0[4] low at beginning of processing frame
19	RW	0	Read Debugging Register
18	RO	0	Reserved
17:16	RW	00b	FIFO Depth of HQV Flip Control Engine For hardware flip only. Rx3D0[25:24] != 00b. Only supports 2 stages FIFO queuing hardware flipping. 00: Pull "FIFO full status Rx3D0[12]" high, while both two stage are queuing. Drop current processing frame while both two stage are queuing. 01: Pull "FIFO full status Rx3D0[12]" high, while one stage is queuing. Drop current processing frame while both two stage are queuing. 10: Pull "FIFO full status Rx3D0[12]" high, while both two stage are queuing. Never drop current processing frame. 11: Pull "FIFO full status Rx3D0[12]" high, while one stage is queuing. Never drop current processing frame.
15:14	RO	0	Reserved
13:4	RW	0	Source Frame Buffer Stride (Unit: 16 bytes)
3:0	RO	0	Reserved

Offset Address: 3FF-3FCh

HQV Destination Data Starting Address 2

Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:29	RO	0	Reserved
28:4	RW	0	Destination Data Starting Address 2 Unit: 16 bytes
3:2	RO	0	Reserved
1:0	RW	0	Memory Location

Note: HQV supports 2 Video Streams; therefore, an additional register space is provided to match the above registers definition. Writing a register to this space, it will write to the second HQV, which output to V3 and source is from the second MC engine.

The relationship between the additional register space and the original register space is
 (The additional register address) = (The original register address) + 16'h1000.

HQV REGISTERS

This document provides detailed HQV register summary table. Register descriptions on high quality video registers are followed in the sequent sections.

HQV Register Summary

These HQV register tables document the I/O port, I/O index and attribute (“Attribute”) for each register.

Table 4. High Quality Video Registers

Offset (Hex)	Register Name	Attribute
First HQV (High Quality Video) Engine Registers		
373-370	HQV Video Start Point Offset Control in Source	RW
377-374	HQV Sub-picture Start Point Offset Control in Source	RW
37B-378	HQV Video End Point Offset Control in Source	RW
37F-37C	HQV Sub-picture End Point Offset Control in Source	RW
383-380	HQV Video Start Point Offset Control in Destination	RW
387-384	HQV Sub-picture Start Point Offset Control in Destination	RW
38B-388	HQV Video End Point Offset Control in Destination	RW
38F-38C	HQV Sub-picture End Point Offset Control in Destination	RW
393-390	HQV Parameters of Hardware Tuning Performance/Quality	RW
397-394	HQV Extended Control	RW
39B-398	HQV Static Record Frame Buffer Starting Address	RW
39F-39C	HQV Static Record Frame Buffer Stride	RW
3A3-3A0	HQV Color Adjustment Control	RW
3A7-3A4	HQV Sharpness Control and Decoder Handshake Control	RW
3AB-3A8	HQV SW Macro Set Valid Table 0	RW
3AF-3AC	HQV SW Macro Set Valid Table 1	RW
3B3-3B0	HQV Video Horizontal Scale Control	RW
3B7-3B4	HQV Video Vertical Scale Control	RW
3BB-3B8	HQV Background Color	RW
3BF-3BC	HQV Segment Residue Pixel Frame Buffer Starting Address	RW
3C3-3C0	HQV Sub-picture Frame Buffer Stride and Control	RW
3C7-3C4	HQV Sub-picture Frame Buffer Starting Address	RW
3CB-3C8	HQV Sub-picture 4 x 16 RAM Table Write Control	RW
3CF-3CC	HQV Background Offset	RW
3D3-3D0	HQV Stream Control and Status	RW
3D7-3D4	HQV SW Source Buffer –Luma or Packed Starting Address	RW
3DB-3D8	HQV SW Source Buffer – Chroma Starting Address	RW
3DF-3DC	HQV Linear/Tile Address Mode, Color Space Conversion, Gamma and De-blocking Control	RW
3E3-3E0	HQV Sub-picture Horizontal Scale Control	RW
3E7-3E4	HQV Motion Adaptive De-interlace Control & Threshold	RW
3EB-3E8	HQV Sub-picture Vertical Scale Control	RW
3EF-3EC	HQV Destination Frame Buffer Starting Address 0	RW
3F3-3F0	HQV Destination Frame Buffer Starting Address 1	RW
3F7-3F4	HQV Destination Frame Buffer Stride	RW
3FB-3F8	HQV Source Frame Buffer Stride	RW
3FF-3FC	HQV Destination Frame Buffer Starting Address 2	RW
Second HQV Engine Registers (Refer to Rx370-3FC register descriptions for detail.)		
1373-1370	HQV Video Start point Offset Control in Source	RW
1377-1374	HQV Sub-picture Start point Offset Control in Source	RW
137B-1378	HQV Video End point Offset Control in Source	RW

Offset (Hex)	Register Name	Attribute
137F-137C	HQV Sub-picture End point Offset Control in Source	RW
1383-1380	HQV Video Start point Offset Control in Destination	RW
1387-1384	HQV Sub-picture Start point Offset Control in Destination	RW
138B-1388	HQV Video End point Offset Control in Destination	RW
138F-138C	HQV Sub-picture End point Offset Control in Destination	RW
1393-1390	HQV Parameters of Hardware Tuning Performance/Quality	RW
1397-1394	HQV Extended Control	RW
139B-1398	HQV Static Record Frame Buffer Starting Address	RW
139F-139C	HQV Static Record Frame Buffer Stride	RW
13A3-13A0	HQV Color Adjustment Control	RW
13A7-13A4	HQV Sharpness Control	RW
13AB-13A8	HQV Decoder Handshake Control	RW
13AF-13AC	HQV Reserved	RO
13B3-13B0	HQV Video Horizontal Scale Control	RW
13B7-13B4	HQV Video Vertical Scale Control	RW
13BB-13B8	HQV Background Color	RW
13BF-13BC	HQV Segment Residue Pixel Frame Buffer Starting Address	RW
13C3-13C0	HQV Sub-picture Frame Buffer Stride and Control	RW
13C7-13C4	HQV Sub-picture Frame Buffer Starting Address	RW
13CB-13C8	HQV Sub-picture 4 x 16 RAM Table Write Control	RW
13CF-13CC	HQV Background Offset	RW
13D3-13D0	HQV Stream Control and Status	RW
13D7-13D4	HQV SW Source Buffer –Luma or Packed Starting Address	RW
13DB-13D8	HQV SW Source Buffer – Chroma Starting Address	RW
13DF-13DC	HQV Linear/Tile Address Mode, Color Space Conversion, Gamma and De-blocking Control	RW
13E3-13E0	HQV Sub-picture Horizontal Scale Control	RW
13E7-13E4	HQV Motion Adaptive De-interlace Control & Threshold	RW
13EB-13E8	HQV Sub-picture Vertical Scale Control	RW
13EF-13EC	HQV Destination Frame Buffer Starting Address 0	RW
13F3-13F0	HQV Destination Frame Buffer Starting Address 1	RW
13F7-13F4	HQV Destination Frame Buffer Stride	RW
13FB-13F8	HQV Source Frame Buffer Stride	RW
13FF-13FC	HQV Destination Frame Buffer Starting Address 2	RW

Note:1) Port Address: MB1 + Offset Address

MB1 is declared in the register with offset address 17h-14h in the PCI configuration space.

- 2) There is additional register space to match the above register definition. When write a register to this space, it will be sent to “command regulator” first and then pass to video display engine. However, register read will be same as the original action. The relationship between the additional register space and original register space is

$$(\text{The additional register address}) = (\text{The original register address}) + 16'h2000$$

HQV Engine Register Descriptions

The relationship between the additional register space and the original register space is: (The additional register address) = (The original register address) + 16'h1000.

HQV Engine Control (370-3FFh)

Offset Address: 373-370h

HQV Video Start Point Offset Control in Source

Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:27	RO	0	Reserved
26:16	RW	0	Horizontal Offset of Start Point for Video Location in Source Picture Unit: Pixel (2P)
15:11	RO	0	Reserved
10:0	RW	0	Vertical Offset of Start Point for Video Location in Source Picture Unit: Pixel (2P)

Offset Address: 377-374h

HQV Sub-picture Start Point Offset Control in Source

Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:27	RO	0	Reserved
26:16	RW	0	Horizontal Offset of Start Point for Sub-picture Location in Source Picture Unit: Pixel (2P)
15:11	RO	0	Reserved
10:0	RW	0	Vertical Offset of Start Point for Sub-picture Location in Source Picture Unit: Pixel (2P)

Offset Address: 37B-378h

HQV Video End Point Offset Control in Source

Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:27	RO	0	Reserved
26:16	RW	0	Horizontal Offset of End Point for Video Location in Source Picture Unit: Pixel (2P)
15:11	RO	0	Reserved
10:0	RW	0	Vertical Offset of End Point for Video Location in Source Picture Unit: Pixel (2P)

Offset Address: 37F-37Ch
HQV Sub-picture End point Offset Control in Source
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:27	RO	0	Reserved
26:16	RW	0	Horizontal Offset of End Point for Sub-picture Location in Source Picture Unit: Pixel (2P)
15:11	RO	0	Reserved
10:0	RW	0	Vertical Offset of End Point for Sub-picture Location in Source Picture Unit: Pixel (2P)

Offset Address: 383-380h
HQV Video Start Point Offset Control in Destination
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:27	RO	0	Reserved
26:16	RW	0	Horizontal Offset of Start Point for Video Location In Destination Picture Unit: Pixel (2P) Either video or sub-picture destination data horizontal offset of start point should be set to zero.
15:11	RO	0	Reserved
10:0	RW	0	Vertical Offset of Start Point for Video Location In Destination Picture Unit: Line (2P) Either video or sub-picture destination data vertical offset of start point should be set to zero.

Offset Address: 387-384h
HQV Sub-picture Start Point Offset Control in Destination
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:27	RO	0	Reserved
26:16	RW	0	Horizontal Offset of Start Point for Sub-picture Location In Destination Picture Unit: Pixel (2P) Either video or sub-picture destination data horizontal offset of start point should be set to zero.
15:11	RO	0	Reserved
10:0	RW	0	Vertical Offset of Start Point for Sub-picture Location In Destination Picture Unit: Line (2P) Either video or sub-picture destination data vertical offset of start point should be set to zero.

Offset Address: 38B-388h
HQV Video End Point Offset Control in Destination
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:27	RO	0	Reserved
26:16	RW	0	Horizontal Offset of End Point for Video Location In Destination Picture Unit: Pixel (2P)
15:11	RO	0	Reserved
10:0	RW	0	Vertical Offset of End Point for Video Location In Destination Picture Unit: Line (2P)

Offset Address: 38F-38Ch
HQV Sub-picture End Point Offset Control in Destination
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:27	RO	0	Reserved
26:16	RW	0	Horizontal Offset of End Point for Sub-picture Location In Destination Picture Unit: Byte (2P)
15:11	RO	0	Reserved
10:0	RW	0	Vertical Offset of End Point for Sub-picture Location In Destination Picture Unit: Line (2P)

Offset Address: 393-390h
HQV Parameters of Hardware Tuning Performance / Quality
Default Value: 4060 8688h

Bit	Attribute	Default	Description
31:28	RW	0100b	Threshold of Inter-Field Complexity for Pull Down Detection (x4) Calculate the difference between current & previous field.
27	RO	0	Reserved
26:25	RW	0	Reserved
24:23	RO	0	Reserved
22:21	RW	11b	Static Judgment Number (SJN) As static record number is equal to SJN, then static flag is asserted.
20	RW	0	The Field Number for The Increment of Static Record 0: 1 field / (static record) 1: 2 fields / (static record)
19:16	RW	0	Reserved
15:14	RW	10b	Threshold for Pull Down Detection (Rx3DC.[10:0]<<Rx390.[15:14]) as the minimum threshold for valid pull down detection
13:12	RO	0	Reserved
11:8	RW	6h	Threshold for Motion Detection (x2)
7:4	RW	8h	Edge Detection Threshold: for Degree 90 (x2)
3:0	RW	8h	Maximum Difference between Block Boundary (x4) Apply de-blocking with sin(x) function while the difference between block boundary is greater than this setting.

Offset Address: 397-394h
HQV Extended Control
Default Value: 4200 0000h

Bit	Attribute	Default	Description
31:28	RW	4h	Edge Detection Trend Close Threshold (x4)
27:24	RW	2h	Edge Detection Trend Threshold
23:11	RO	0	Reserved
10:8	RW	0	Constriction Enable 000: Constriction disable 001~111: Rounding LSB1~LSB7
7	RW	0	Color Adjustment Enable 0: Disable 1: Enable
6	RW	0	Bob de-interlacing Method 0: Line average 1: Line duplication (for TV output)
5	RW	0	YUV Output Format Control (2P) 0: YUV422 out 1: YUV444 out This bit is effective when (H or V scaling size) < (1/2 H or V original) size. For the other cases, it just uses YUV422 out
4	RW	0	Color Space Conversion Method 0: BT601 1: BT709
3	RW	0	Color Format Convert Method (from YUV420 → YUV422) 0: 4-tap interpolation 1: Method 1 (-1 9 9 -1)
2:1	RW	00b	Color Format Convert Method (from YUV422 → YUV444) 00: Method 1 (WMV9 and H.264) 01: Reserved 1x: Method 3 (-1 9 9 -1)
0	RW	0	Color Format Convert Method (from YUV444 → YUV422) 0: Method 1 (1 1) 1: Method 2 (Drop) This bit is effective as (no scaling) or (scaling size) > (1/2 original size). For the other cases, it just uses method 2.

Offset Address: 39B-398h
HQV Static Record Frame Buffer Starting Address
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:29	RO	0	Reserved
28:4	RW	0	Static Record Frame Buffer Starting Address Unit: 16 bytes
3:2	RO	0	Reserved
1:0	RW	0	Memory Location

Offset Address: 39F-39Ch
HQV Static Record Frame Buffer Stride
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:10	RO	0	Reserved
9:4	RW	0	Static Record Frame Buffer Stride Unit: 16 bytes
3:0	RO	0	Reserved

Offset Address: 3A3-3A0h
HQV Color Adjustment Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:28	RW	0	Coefficient Index
27:17	RW	0	Coefficient D (s[26:18],[17]). (2p)
16:0	RW	0	Coefficient ABC (s[15:8],[7:0]) (2p)

 Note: $Y'(R') = A1*Y(R) + B1*Cb(G) + C1*Cr(B) + D1$
Offset Address: 3A7-3A4h
HQV Sharpness Control and Decoder Handshake Control
Default Value: c000 0008h

Bit	Attribute	Default	Description
31	RW	1	Sharpness Enable
30:29	RW	10b	Sharpness Threshold.
28:27	RW	0	Sharpness Coefficient ID.
26	RW	0	Wait Frame Done Enable
25:20	RW	0	Source Frame ID
19	RW	1b	Wait Time Out Enable
18:13	RW	1h	Wait Time Out Cycle (unit : 500k cycle)
12:11	RW	0	SW Set Frame Valid Function 00:No SW Set/reset, 01:SW Macro Set/reset Valid 10:SW Reset Valid with Index, 11: SW Set Valid with Index
10:5	RW	0	SW Set Frame Valid Index
4:0	RO	0	Reserved

Notes: Flow of HQV wait decoder frame done

1. Decode HQV register

2. HQV received fire command in Rx3D0.

A. If Rx3A4[26] Wait Frame Done Enable is disable, HQV fire with source address decode at 1.

B. If Rx3A4[26] is enable, HQV will check the valid from frame address table index by Rx3A4[25:20] Source Frame ID. At this state, HQV time out counter start count.

3. If Rx3A4[19] Wait Time out Enable is disable, HQV will always wait valid in frame address table.

4. If Rx3A4[19] Wait Time out Enable is enable and the time out counter is larger than Rx3A4[18:13] Wait Time Out Cycle or receive valid in frame address table, HQV will fire with source address from the frame address table. HQV then clear the valid in the table.

Offset Address: 3AB-3A8h
HQV SW Macro Set Valid Table 0
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:0	RW	0	HQV Valid Table[31:0]

Offset Address: 3AF-3ACh
HQV SW Macro Set Valid Table 1
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:0	RW	0	HQV Valid Table[63:32]

Offset Address: 3B3-3B0h
HQV Video Horizontal Scale Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RW	0	Horizontal Scale Enable 1: Enable (2p)
30	RO	0	Reserved
29:28	RW	00b	Horizontal Scale Function (2p) 00: Scale up. 01: 1~1/4 10: 1/4~1/8 ⁺ 11: <1/8
27:15	RO	0	Reserved
14:0	RW	0	Horizontal Scale Factor [14:12],[11:0] (2p)

Note: Scale factor:

1. Scale up: source/destination
2. 1~1/4: source/(destination+0.5)
3. 1/4~1/8⁺: source/destination.
4. <1/8: destination/source

Offset Address: 3B7-3B4h
HQV Video Vertical Scale Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RW	0	Vertical Scale Enable 1: Enable (2p)
30:29	RO	0	Reserved
28	RW	0	Vertical Scale Function (2p) 0: Scale up. 1: Scale down
27:17	RO	0	Reserved
16:0	RW	0	Vertical Scale Factor [16:12,11:0] (2p)

Note: Scale factor

1. Scale up: source/destination;
2. Scale down: source/(destination+0.5)

General Reminders:

1. For all scaling calculation, the final results should be rounded to the nearest integer.
2. For bi-linear factor, please use 6 binary fraction of factor (need be rounded to the nearest 6th fraction) to do the calculation.

Offset Address: 3BB-3B8h
HQV Background Color
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:30	RO	0	Reserved
29:20	RW	0	Luma(Y) or Red Color Value
19:10	RW	0	Chroma(Cb) or Green Color Value
9:0	RW	0	Chroma(Cr) or Blue Color Value

Offset Address: 3BF-3BCh
HQV Segment Residue Pixel Frame Buffer Starting Address
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RO	0	HQV Output Field
30	RO	0	HQV Current Process Field 1: Bottom field
29	RO	0	Reserved
28:4	RW	0	Segment Residue Pixel Frame Buffer Starting Address Unit : 16 bytes
3:2	RO	0	HQV Current Process Destination Buffer ID 1: Bottom field
1:0	RW	0	Memory Location

Offset Address: 3C3-3C0h
HQV Sub-picture Frame Buffer Stride and Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:24	RW	0	MC Flipping Count For MC flip to HQV path: Read only For SW flip path: R/W HQV update read out register data at the beginning of HQV processing a frame.
23:21	RO	0	Reserved
20	RW	0	Sub-picture Blending Option 0: Blending before scaling 1: Scaling before blending
19	RW	0	Sub-picture Format 0: AI44 or IA44 1: AYUV (MSB A(8)-Y(8)-U(8)-V(8) LSB)
18	RW	0	Inverse Alpha Value in AI44 Mode 1: Inverse (One's Complement)
17	RW	0	Alpha, Index Exchange in AI44 Mode 0: AI44 1: IA44
16	RW	0	HQV Sub-picture Enable 1: Enable 0: Disable Only active at HQV source format is YUV.
15:14	RO	0	Reserved
13:4	RW	0	Subpicture Frame Buffer Stride Unit: 16 bytes
3:0	RO	0	Reserved

Offset Address: 3C7-3C4h

HQV Sub-picture Frame Buffer Starting Address
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:29	RO	0	Reserved
28:4	RW	0	Sub-picture Frame Buffer Starting Address Unit: 16 bytes
3:2	RO	0	Reserved
1:0	RW	0	Memory Location

Offset Address: 3CB-3C8h
HQV Sub-picture 4x16 RAM Table Write Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:8	RW	0	RAM Table Write Data V: Bits [31:24] U: Bits [23:16] Y: Bits [15:8]
7:4	RW	0	RAM Table Read / Write Address Indicate which entry of palette table will be written or read. Palette table contains 16 entries of palette data. (HQV3C8[7:4] = 0x0000 ~ HQV3C8[7:4] = 0x1111) Need to program bits [31:8] and [7:4] 16 times to fill the subpicture palette table.
3	RO	0	Reserved
2	RW	0	V Write Enable 0: Disable 1: Enable
1	RW	0	U Write Enable 0: Disable 1: Enable
0	RW	0	Y Write Enable 0: Disable 1: Enable

Offset Address: 3CF-3CCh
HQV Background Offset
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:27	RO	0	Reserved
26:16	RW	0	Background Horizontal Offset (-1) Unit: Pixel
15:11	RO	0	Reserved
10:0	RW	0	Background Vertical Offset (-1) Unit: Pixel

Offset Address: 3D3-3D0h
HQV Stream Control and Status
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:28	RW	0	Video Data Stream Format [3:0] 0000: RGB32 – (X8R8G8B8) 0001: RGB32 – (X2R10G10B10) 0010: RGB16 – (R5G6B5) 0011: RGB15 – (X1R5G5B5) 0100: YUV444 – (X8Y8U8V8) 0101: V410 – (V10Y10U10X2) 1000: YUV422 – (V8Y ₁ 8U8Y ₀ 8) 1001: UYVY – (Y ₁ 8V8Y ₀ 8U8) 1100: YUV420 – (NV12; planar mode) 1101: YUV411 – (NV11; planar mode : Y ₃ 8Y ₂ 8Y ₁ 8Y ₀ 8 V ₀ 8U ₀ 8 Y ₇ 8Y ₆ 8Y ₅ 8Y ₄ 8 V ₁ 8U ₁ 8) 1110: P208 – (YUV422 planar mode) Others:reserved
27	RW	0	High Quality Video Enable 0: Disable 1: Enable
26	RW	0	Buffer Mode 0: Double destination buffers 1: Triple destination buffers
25:24	RW	00b	Video Stream Source [1:0] 00: SW 01: Reserved 10: Capture 0 11: Capture 1
23	RW	0	Advanced De-interlace Mode Enable Reference more than one field.
22	RW	0	Vertical Low Pass Filter Enable 0: Disable 1: Enable
21	RO	0	Reserved
20	RW	0	Planar Mode Chrominance Source Data Format 0: Source Chrominance is saved by frame picture 1: Source Chrominance is saved by field picture
19	RW	0	Inverse Input Field 1: Inversed
18	RW	0	Frame To Field 1: Frame base source, extract a field from a frame.
17	RW	0	Field To Frame 1: Field source, de-interlace to progressive frame.
16	RO	0	Reserved
15	RW	0	Sub-Picture Flip Software writes 1 to this bit indicates a new sub-picture need to blend. After blending completes, hardware clears it to 0. Software can read this bit to check the status if hardware completes blending.
14:13	RO	0	Reserved
12	RO	0	HQV Flip FIFO Full Status The FIFO depth defined in Rx3F8 [17:16].
11	RO	0	Reserved
10:8	RO	0	State Machine Status of HQV Flip Module
7	RW	0	HQV Interrupt Enable 0: Disable HQV interrupt. 1: HQV send interrupt signal after done a frame. Relative setting: Rx3D0[0].
6	RW	0	Single Destination Buffer 1: Single buffer used Rx3D0[26] would be ignored.
5	RW	0	Field of Software Source Input 0: Top 1: Bottom
4	RW	0	Software Source Flip Software writes 1 to flip a image to HQV. (Rx3D0[25:24] should be 00b) After processing completes, hardware clears it to 0. Software reads this bit to check flip status.
3	RO	0	HQV Engine Idle State 1: Idle
2:1	RO	0	HQV Output Buffer ID HQV destination buffer ID

0	RW	0	HQV End of Frame Status 1:HQV has been output an image. (Software writes 1 to clear this bit) After HQV done an image, this bit will be pulled high, and it will be pulled down only whent software writes 1b to it.
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Offset Address: 3D7-3D4h
HQV SW Source Buffer – Luma or Packed Starting Address
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RO	0	Reserved
30:29	RO	0	Reserved
28:4	RW	0	SW Source Buffer Y or Packed Mode Starting Address Unit: 16 bytes
3:2	RO	0	Reserved
1:0	RW	0	Memory Location

Offset Address: 3DB-3D8h
HQV SW Source Buffer – Chroma Starting Address
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:29	RO	0	Reserved
28:4	RW	0	SW Source Buffer U, V Starting Addresses Unit: 16 bytes
3:2	RO	0	Reserved
1:0	RW	0	Memory Location

Offset Address: 3DF-3DCh
HQV Linear / Tile Address Mode, Color Space Conversion, Gamma, De-blocking Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:30	RW	00b	Linear / Tile Address Mode Control (Tile address only enable at source data from MC, 3D0[25:24]=01) 00: Linear 01: 256 bits x 8 tile mode (Addr = SA + (Y[10:3]*PTH*8) + {X[7:1],Y[2:0],X[0]}) 10: 256 bits x 16 tile mode (Addr = SA + (Y[10:4]*PTH*16) + {X[6:1],Y[3:0],X[0]}) 11: 512 bits tile mode (Addr = SA + (Y[10:4]*PTH*16) + {X[6:2], Y[3:0],X[1:0]}). Where unit of X is 128-bit; unit of Y is line.
29	RW	0	HQV Output Data Pack In 32-bits Mode 0:16 bits (RGB565). 1:32 bits (RGB888) Only valid when the source is YUV and color space conversion is enabled.
28	RW	0	Color Space Conversion Enable 0: Disable 1: Enable
27	RW	0	De-blocking Enable
26:25	RO	0	Reserved
24:20	RW	0	HQV Output FIFO Threshold for Write Request Control Unit: Level HQV output FIFO has 64 levels, once the data in output FIFO touch the threshold (32+3DC.[24:20]), the write request would be triggered.
19:16	RO	0	Reserved
15	RW	0	Constant Alpha of RGB32 Format 0: Alpha = 00 1: Alpha = FF
14	RW	0	Enable Synchronization Flipping Field with Interlaced IGA 1: Enable
13	RW	0	IGA Field Inverse 1: Inverse
12:11	RO	0	Reserved
10:0	RW	0	Image Size / 1024 Pull-down detection use.

Offset Address: 3E3-3E0h
HQV Sub-picture Horizontal Scale Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RW	0	Horizontal Scale Enable 0: Disable 1: Enable
30	RO	0	Reserved
29:28	RW	0	Horizontal Scale Function (2p) 00: Scale up 01: 1~1/4 10: 1/4~1/8* 11: <1/8
27:15	RO	0	Reserved
14:0	RW	0	Horizontal Scale Factor [14:12,11] (2p) Scale up : Source/destination 1~1/4 : Source/(destination + 0.5) 1/4~1/8* : Source/destination <1/8 : Destination/source

Offset Address: 3E7-3E4h
HQV Motion Adaptive De-interlace Control & Threshold
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RW	0	2:2/2:2:2:4 Pull Down Sequence Detection Enable 0: Disable 1: Enable
30	RW	0	3:2:3:2:2 Pull Down Sequence Detection Enable 0: Disable 1: Enable
29	RW	0	5:5 Pull Down Sequence Detection Enable 0: Disable 1: Enable
28	RW	0	6:4 Pull Down Sequence Detection Enable 0: Disable 1: Enable
27	RW	0	3:2 Pull Down Sequence Detection Enable 0: Disable 1: Enable
26	RW	0	8:7 Pull Down Sequence Detection Enable 0: Disable 1: Enable
25	RO	0	Reserved
24	RW	0	2:3:3:2 Pull Down Sequence Detection Enable 0: Disable 1: Enable
23:13	RO	0	Reserved
12	RW	0	Motion Detection Enable
7	RO	0	2:2 Pull Down Detection Status
6	RO	0	3:2 Pull Down Detection Status
5	RO	0	2:3:3:2 Pull Down Detection Status
4	RO	0	3:2:3:2:2 Pull Down Detection Status
3	RO	0	5:5 Pull Down Detection Status
2	RO	0	6:4 Pull Down Detection Status
1	RO	0	8:7 Pull Down Detection Status
0	RW	0	Edge Detection Enable 0: Disable 1: Enable

Offset Address: 3EA-3E8h
HQV Sub-picture Vertical Scale Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RW	0	Vertical Scale Enable 0: Disable 1: Enable
30:29	RO	0	Reserved
28	RW	0	Vertical Scale Function (2p) 0: Scale up 1: Scale down
27:17	RO	0	Reserved
16:0	RW	0	Vertical Scale Factor [14:12,11] (2p) Scale up : Source/destination Scale down : Source/(destination + 0.5)

Offset Address: 3EF-3ECh
HQV Destination Frame Buffer Starting Address 0
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RW	0	HQV Output Data Pack In 32 Bits xRGB2-10-10-10 Format After HQV's Color Space Conversion 1: Enable Note: Only one of {Rx3EC[31], Rx3DC[29]} can be set to 1.
30	RW	0	Enable Output In Tile Mode 1: Enable. Addr = ST_ADDR[28:4] + Y[10:3]*{PITCH[10:0], 3'b0} + {X[10:1], Y[2:0], X[0]}
29	RO	0	Reserved
28:4	RW	0	Destination Frame Buffer Starting Address 0 Unit: 16 bytes
3:2	RO	0	Reserved
1:0	RW	0	Memory Location

Offset Address: 3F3-3F0h
HQV Destination Frame Buffer Starting Address 1
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:29	RO	0	Reserved
28:4	RW	0	Destination Frame Buffer Starting Address 1 Unit: 16 bytes
3:2	RO	0	Reserved
1:0	RW	0	Memory Location

Offset Address: 3F7-3F4h
HQV Destination Frame Buffer Stride
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:14	RO	0	Reserved
13:4	RW	0	Destination Frame Buffer Stride (2p) Unit: 16 bytes
3:0	RO	0	Reserved

Offset Address: 3FB-3F8h
HQV Source Frame Buffer Stride
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RW	0	Load Starting Address Rx3D4[25:4], Rx3D8[25:4] for Advanced De-interlacing 0: Not used. Hardware keep starting address 1: Load starting address to current field Notes: Command sequence Step1: Write Rx3D4, Rx3D8 Step2: Write Rx3F8; new address to PN Step3: Write Rx3D4, Rx3D8 Step4: Write Rx3F8; PN to PC; new address to PN Step5: Write Rx3D4, Rx3D8 Step6: Write Rx3F8; PC to PP; PN to PC; new address to PN
30	RW	0	SJN Reset 1: Reset static judgment number
29	RW	0	Pull Down Detection Low-Threshold Value
28	RW	0	Pull Down Detection Error Sequence Check One Time
27:26	RW	0	For Fixing Bug: Spare Register
25	RW	0	Not Check Size 0: Check size 1: Not check size
24:21	RW	0	Reserved
20	RW	0	Software Flip Queue Enable 0: Pull Rx3D0[4] low at frame done. 1: Pull Rx3D0[4] low at beginning of processing frame
19	RW	0	Read Debugging Register
18	RO	0	Reserved
17:16	RW	00b	FIFO Depth of HQV Flip Control Engine For hardware flip only. Rx3D0[25:24] = 00b. Only supports 2 stages FIFO queuing hardware flipping. 00: Pull "FIFO full status Rx3D0[12]" high, while both two stage are queuing. Drop current processing frame while both two stage are queuing. 01: Pull "FIFO full status Rx3D0[12]" high, while one stage is queuing. Drop current processing frame while both two stage are queuing. 10: Pull "FIFO full status Rx3D0[12]" high, while both two stage are queuing. Never drop current processing frame. 11: Pull "FIFO full status Rx3D0[12]" high, while one stage is queuing. Never drop current processing frame.
15:14	RO	0	Reserved
13:4	RW	0	Source Frame Buffer Stride Unit: 16 bytes
3:0	RO	0	Reserved

Offset Address: 3FF-3FCh
HQV Destination Frame Buffer Starting Address 2
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:29	RO	0	Reserved
28:4	RW	0	Destination Frame Buffer Starting Address 2 Unit: 16 bytes
3:2	RO	0	Reserved
1:0	RW	0	Memory Location

Note: HQV supports 2 Video Streams; therefore, an additional register space is provided to match the above registers definition. Writing a register to this space, it will write to the second HQV, which output to V3 and source is from the second MC engine.

COMMAND REGULATOR (CR) REGISTERS

This chapter provides detailed Command Regulator register descriptions.

Settings of 3D/CR Registers

The I/O Register Base Address for 3D/CR (Command Regulator) is 400h. Offsets Rx1Ch to Rx3Bh are used to set CR registers. These registers are allowed to be set through the starting address Rx1Ch or Rx3Ch with the same HParaType 10h and HparaType 11h. Settings through Rx1Ch would not enable the 3D Engine clock, while settings through Rx3Ch would enable the 3D Engine clock.

Setting of Command Regulator

Scope	Offset	Description	Field Name													
Transmission Setting	1Ch	The Beginning of Internal Address for Parameter Programming	HParaAdr													
	1Dh	Offset Setting for Some Special Parameter Types	HParaOS													
	1Eh	Parameter Type		HParaType												
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	1111 1111b	Reserved														
For more details for the parameters, please refer to Definition of Parameter section.																
1Fh	Parameter Type Sub-code	HParaSubType														
Transmission Space	23h-20h	Parameter 0	Hpara0													
	27h-24h	Parameter 1	Hpara1													
	2Bh-28h	Parameter 2	Hpara2													
														
	3Bh-38h	Parameter 6	Hpara6													

Setting of 3D Engine

Scope	Offset	Description	Field Name										
Transmission Setting	3Ch	The Beginning of Internal Address for Parameter Programming	HParaAdr										
	3Dh	Offset Setting for Some Special Parameter Types	HParaOS										
	3Eh	Parameter Type	HParaType										
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Scope	Offset	Description	Field Name
		0011 0000 = Vertex Buffer(multiple streams) Base and Pitch 0011 0001 = Vertex Shader Instruction 0011 0010 = Vertex Shader Constant Register 0011 0011 = Vertex Shader Integer Register	
	0000 0100b	Vertex and Primitive Setting	
	0000 0101b ~ 0000 0111b	Reserved	
	0000 1001b ~ 0000 1111b	Reserved	
	0001 0000b	Command Decoded in front of Command Regulator	
	0001 0001b	Command for Frame Buffer AutoSwapping and CR's Miscellaneous Setting	
	1111 1101b ~ 0001 0010b	Reserved	
<i>For details of the parameters, please refer to Definition of Parameter section.</i>			
	3Fh	Parameter Type Sub-code	HParaSubType
Transmission Space	43h-40h	Parameter 0	Hpara0
	47h-44h	Parameter 1	Hpara1
	4Bh-48h	Parameter 2	Hpara2
	
	1F7h-1F4h	Parameter 109	Hpara6D
	1FBh-1F8h	Parameter 110	Hpara6E
	1FFh-1FCh	Parameter 111	Hpara6F
	
	2FFh-2FCh	Parameter 175	HparaAF

HParaType 00h: Primitive Vertex Data or Vertex Index

HParaType 00h is used for Primitive Vertex Data (for Vertex Command Mode) or Vertex Index (for Vertex Buffer Index Mode). There is no sub-address in this ParaType. The steps to fire 3D Engine are as follows:

- Step 1: Set the correct value to all the related 3D globe registers through ParaType 01h, 02h, 03h, 04h, 10h, 11h and FEh.
- Step 2: Sent Vertex Data or Vertex Index (according to HVertexMode) through ParaType 00h. CR would configure the vertex (according HVFVLEN and HnFVF) and generate fire signal automatically whenever all the vertices of a primitive are ready (according to HVCycle, H2and1VT and HPMTType). CR would also generate the PLEND (Primitive List End) signal whenever the entire listed vertexes are finished (according to HVTXnum), or receive a “Stop Command”.

For next primitive list, repeat the two steps above.

HParaType 10h: Commands for Command Regulator

Sub-Address (Bits [31:24]): 00-74h

HParaType = 10h, Sub-Address = 00h

PCI Command Setting

Bits [23:0]	Attribute	Default	Description
23:9	WO		Reserved
8	WO	0	Enable of Packaging the PCI Command In Front of CR 0: Disable 1: Enable
7:0	WO	8h	Number of ECLK Cycle for PCI Command Packaging Time Out

HParaType = 10h, Sub-Address = 02h

Read Register Back Command Setting

Bits [23:0]	Attribute	Default	Description
23:21	WO		Reserved
20:12	WO		Reading-Back Register to Debug Port Address [10:2] for Reading-Back Register to Debug port; will be multiplexed with HI2CR_RADR[8:2].
11	WO	0	Enable Reading-Back Register to Debug Port 0: Disable 1: Enable
10:8	WO		Reserved
7:0	WO		ID for Reading-Back Register 0000 0000: Reading the RB registers from CR 0000 0001: Reading the RB registers from FE (including VP, CL and SE) 0000 0010: Reading the RB registers from PE (including RZ and CZ) 0000 0011: Reading the RB registers from RC 0000 0100: Reading the RB registers from PS 0000 0101: Reading the RB registers from XE 0000 0110: Reading the RB registers from BE (including GEMI) 0000 0111: Reading the RB registers for Performance Counters Others: Reserved

HParaType = 10h, Sub-Address = 03h

Address for Reading-Back Register

Bits [23:0]	Attribute	Default	Description
23:0	WO		Address for Reading-Back Register Bits[23:16]: HParaSubType Bits[15:8]: HParaType Bits[7: 0]: Sub-Address

HParaType = 10h, Sub-Address = 04h

CR Command Dispatch Setting

Bits [23:0]	Attribute	Default	Description
23:3	WO		Reserved
2:1	WO	00b	Switch Mode Between Normal GFX and Video Related GFX Command 00: Video related 3D/2D command has high priority 01: Normal 3D/2D command has high priority 1x: Round robin
0	WO	0	Video Related 3D/2D Command Dispatch to HQV Data Path Enable 0: Video related 3D/2D command would be sent to GFX data path. 1: Video related 3D/2D command would be sent to video data path.

Note: If command switch is enabled, traditional wait/fence and traditional branch will be disabled. They can not be used at same time.

HParaType = 10h, Sub-Address = 05-07h: Reserved

Preemption Command Setting (08-0Bh)
HParaType = 10h, Sub-Address = 08h
Preemption Command Setting

Bit [23:0]	Attribute	Default	Description
23:20	WO		Reserved
19:0	WO		Higher 20-Bit Preemption Fence Command Base Address for PCI Master Write It is A[43:24].

HParaType = 10h, Sub-Address = 09h
Preemption Command Setting

Bit [23:0]	Attribute	Default	Description
23:4	WO		Lower 20-Bit Preemption Fence Command Base Address for PCI Master Write It is A[23:4].
3:0	WO		Reserved

HParaType = 10h, Sub-Address = 0Ah
Preemption Command Setting

Bit [23:0]	Attribute	Default	Description
23:0	WO		Lower 24-Bit Preemption Fence Command ID <HPPFCID[31:8]>

HParaType = 10h, Sub-Address = 0Bh
Preemption Command Setting

Bit [23:0]	Attribute	Default	Description
23:16	WO		Reserved
15:8	WO		Higher 8-Bit Preemption Fence Command ID <HPPFCID[7:0]>
7:3	WO		Reserved
2:1	WO		Preemption Fence Mode 00: After finishing preemption, write out HPPFCID to System Memory. 01: After finishing preemption, CR will generate interrupt signal and write fence queue and record fence ID. 10: After finishing preemption, CR will generate interrupt signal and record HPPFCID into fence queue and write out fence ID to system memory. 11: Reserved
0	WO		Trig CR to Do Preemption

CRMI Setting (0C-0Eh)
HParaType = 10h, Sub-Address = 0Ch
CRMI Setting

Bit [23:0]	Attribute	Default	Description
23:16	WO	32h	Kill Number of Each Request Interrupt whenever this bit's request of the same engine got accepted.
15:8	WO	FEh	Main Command Buffer Request Priority Mask
7:0	WO	FCh	Virtual Queue Request Priority Mask

HParaType = 10h, Sub-Address = 0Dh
CRMI Setting

Bit [23:0]	Attribute	Default	Description
23:16	WO	F8h	Sub-main Command Buffer Request Priority Mask
15:8	WO	F0h	Video Command Buffer Request Priority Mask
7:0	WO	E0h	GFX Command Buffer Request Priority Mask

HParaType = 10h, Sub-Address = 0Eh
CRMI Setting

Bit [23:0]	Attribute	Default	Description
23:16	WO	C0h	Decoder Command Buffer Request Priority Mask
15:8	WO	80h	GFX Data Buffer Request Priority Mask
7:0	WO	00h	3D Write Back Request Priority Mask

Note:

Arbitration Marks Bit

- Bit [0] of each arbitration mask represents the priority setting of Main Command Buffer Request
- Bit [1] of each arbitration mask represents the priority setting of Virtual Queue Request
- Bit [2] of each arbitration mask represents the priority setting of Sub-main Buffer Request
- Bit [3] of each arbitration mask represents the priority setting of Video Path Request
- Bit [4] of each arbitration mask represents the priority setting of Graphic Path Command Request
- Bit [5] of each arbitration mask represents the priority setting of Decoder Path Request
- Bit [6] of each arbitration mask represents the priority setting of Graphic Path Data Request
- Bit [7] of each arbitration mask represents the priority setting of 3D Save Request

AGP Command Setting (60-68h)

Please be noted that:

1. AGP address execute priority : Pause > Jump > End (i.e. if Address_Pause = Address_End, execute Pause function).
2. Jump and end are the same function. When the address equals to jump or end, CR will go back to the start address automatically.
3. If users want to stop the AGP command, SW set a pause address with PID = 10b.
4. AGP commands have higher priority than PCI command, only when AGP paused with PID=10b, PCI command can get into CR.
5. The minimum kick off command length is 2QW, it means Min (current pause address – last pause address) = 2QW.

HParaType = 10h, Sub-Address = 60h
AGP Command

Bit [23:0]	Attribute	Default	Description
23:4	WO		Lower 3 Bytes of AGP Buffer Start Address It is A[23:0] which A[3:0] is useless, 128-bit alignment.
3:2	WO		Reserved
1:0	WO		AGP Buffer Location 00: SL 01: SF 10: SM 11: LL

HParaType = 10h, Sub-Address = 61h
AGP Command

Bit [23:0]	Attribute	Default	Description
23:8	WO		Reserved
7:0	WO		Higher Bytes of AGP Buffer Start Address It is A[31:24].

HParaType = 10h, Sub-Address = 62h
AGP Command

Bit [23:0]	Attribute	Default	Description
23:4	WO		Lower 3 Bytes of AGP Buffer End Address It is A[23:0] which A[3:0] is useless, 128-bit alignment.
3:0	WO		Reserved

HParaType = 10h, Sub-Address = 63h
AGP Command

Bit [23:0]	Attribute	Default	Description
23:8	WO		Reserved
7:0	WO		Higher Bytes of AGP Buffer End Address It is A[31:24].

HParaType = 10h, Sub-Address = 64h
AGP Command

Bit [23:0]	Attribute	Default	Description
23:4	WO		Lower 3 Bytes of AGP Buffer Pause Address It is A[31:0] which A[3:0] is useless, 128-bit alignment.
3:0	WO		Reserved

HParaType = 10h, Sub-Address = 65h
AGP Command

Bit [23:0]	Attribute	Default	Description
23:10	WO		Reserved
9:8	WO		AGP Buffer Pause Address ID 00: It is pause point. When the Main Command Buffer Address hits pause address, it will pause until the pause address changed. And start on the next address. 01: It is jump point. When the Main Command Buffer Address hits pause address, it will pause until receive next pause address(with PauseID=00b/10b). And start to fetch command from start address. 10: It is stop point. When the Main Command Buffer Address hits pause address, it will stop to fetch command until HAGPBTrig is set. 11: Reserved
7:0	WO		Higher Bytes of AGP Buffer Pause Address It is A[31:24].

HParaType = 10h, Sub-Address = 66h
AGP Command

Bit [23:0]	Attribute	Default	Description
23:4	WO		Lower 3 Bytes of AGP Buffer Jump Address It is A[23:0] which A[3:0] is useless, 128-bit alignment.
3:0	WO		Reserved

HParaType = 10h, Sub-Address = 67h
AGP Command

Bit [23:0]	Attribute	Default	Description
23:8	WO		Reserved
7:0	WO		Higher Byte of AGP Buffer Jump Address It is A[31:24].

HParaType = 10h, Sub-Address = 68h
AGP Command

Bit [23:0]	Attribute	Default	Description
23:22	WO		Reserved
21:16	WO	8h	Threshold Value of Read AGP Command
15:6	WO		Reserved
5	WO	0	Format of AGP Header1 Data to 2D Engine 0: 128-bits format 1: 32-bits format
4	WO		Clear Fence Queue
3	WO		Clear AGP Cycle
2	WO		Trigger Restore AGP Command Cycle HW will only restore AGP command.
1	WO		Trigger Restore 3D Register Cycle
0	WO		Trigger AGP Cycle <HAGPBTrig> The Trig signal of AGP command.

CMDQ Setting (70-76h)
HParaType = 10h, Sub-Address = 70h
CMDQ Setting

Bit [23:0]	Attribute	Default	Description
23:4	WO		Lower 3 Bytes of Command Queue Start Address It is A[23:0] which A[3:0] is useless, 128 bit alignment.
3:2	WO		Reserved
1:0	WO		Command Queue Location 00: SL 01: SF 10: SM 11: LL

HParaType = 10h, Sub-Address = 71h
CMDQ Setting

Bit [23:0]	Attribute	Default	Description
23:4	WO		Lower 3 Bytes of Command Queue End Address It is A[23:0] which A[3:0] is useless, 128 bit alignment.
3:0	WO		Reserved

HParaType = 10h, Sub-Address = 72h
CMDQ Setting

Bit [23:0]	Attribute	Default	Description
23:16	WO		Reserved
15:8	WO		Higher Byte of Command Queue End Address 128-bit alignment
7:0	WO		Higher Byte of Command Queue Start Address. 128 bit alignment

HParaType = 10h, Sub-Address = 73h
CMDQ Setting

Bit [23:0]	Attribute	Default	Description
23:0	WO		Length of Command Queue in Unit of 128 Bits The minimum value is 24'h800.

HParaType = 10h, Sub-Address = 74h
CMDQ Setting

Bit [23:0]	Attribute	Default	Description
23:22	WO		Reserved
21:16	WO		Threshold Value of Write Command Queue FIFO
15:14	WO		Reserved
13:8	WO		Threshold Value of Read Command Queue FIFO
7:4	WO		Control Setting for CMDQ Read Request Interrupting Write Request 0000: Never interrupt, CMDQ read request only after CMDQ write finished. 0001: Interrupt CMDQ write request whenever CMDQ read request. 1000: Interrupt whenever 16 CMDQ write requests accepted. 1001: Interrupt whenever 32 CMDQ write requests accepted. 1100: Interrupt whenever 32 CMDQ write request cycle. 1101: Interrupt whenever 64 CMDQ write request cycle. Others:Reserved
3	WO		Reserved
2	WO		CMDQ Used for Command from AGP or PCI 0: Store command from PCI 1: Store command from AGP
1	WO		Enable Request Length for CMDQ of Command Regulator 0: Disable, always 1 128-bit command per request. 1: Enable it, 1, 2, or 4 128-bit commands per request is possible.
0	WO		Enable Command Queue 0: Disable 1: Enable

Note : If Enable VQ1, Branch header, Branch AGP header (FE8x) is forbidden, since HW can not stop VQ read data from FB when detect Branch AGP header (FE8x).

HParaType 11h: Commands for Command Regulator

Sub-Address (Bits [31:24]): 00-6Bh

HParaType = 11h, Sub-Address = 00h

E3/E2 Lock Setting

Bits [23:0]	Attribute	Default	Description
23:18	WO		Reserved
17	WO	1b	Enable HW Lock 2D and 3D 0: Disable. 3D and 2D lock each other by SW (use wait command) 1: Enable. 3D 2D locks each other by HW. Only one engine can work at same time.
16	WO	0	Enable 2D/3D Request Lock Control 0: Disable. When one of 3D/2D engine is busy, do not sent commands to another engine. 1: Enable. When one of 3D/2D engine is busy, CR sent commands to another engine but another engine do not access memory. Only one of the 2D and 3D engines is working at a time. However, 3D Command can be sent to 3D engine when 2D engine is busy. Also, 2D Command can send to 2D engine when 3D engine is busy. In the first case, Command Regulator will set CR Lock 3D Command before issuing 3D Command and reset CR Lock 3D Command after 3D engine became idle, and CR Lock 2D Command works in the same way.
15:0	WO		Reserved

HParaType = 11h, Sub-Address = 02h: Reserved

Fence Command Setting (03-07h)
HParaType = 11h, Sub-Address = 03h
Fence Command Setting

Bits [23:0]	Attribute	Default	Description
23	WO		Fence Command Wait 3D Idle
22	WO		Fence Command Wait 2D Idle
21	WO		Fence Command Wait VD Idle
20	WO		Fence Command Wait HQV0 Idle
19	WO		Fence Command Wait HQV1 Idle
18	WO		Fence Command Wait DMA3 Idle
17	WO		Fence Command Wait DMA2 Idle
16	WO		Fence Command Wait DMA1 Idle
15	WO		Fence Command Wait DMA0 Idle
14	WO		Fence Command wait HQV0EOF
13	WO		Fence Command wait HQV1EOF
12:9	WO		Reserved
8:4	WO		Wait Idle Count
3:1	WO		Reserved
0	WO		Fence Command Needs to Wait All Engine Idle

HParaType = 11h, Sub-Address = 04h
Fence Command Setting

Bits [23:0]	Attribute	Default	Description
23:20	WO		Reserved
19:0	WO		Fence Command Control 1 If HFCMode[2]=0, higher 12-bit Fence Type. It is FenceType[31:20]. If HFCMode[2]=1, higher 20-bit Fence Command Base address for PCI Master Write. It is A[43:24].

HParaType = 11h, Sub-Address = 05h
Fence Command Setting

Bits [23:0]	Attribute	Default	Description
23:4	WO		Fence Command Control 2 If HFCMode[2]=0, lower 24-bit Fence Type. It is FenceType[19:0]. If HFCMode[2]=1, lower 24-bit Fence Command Base address for PCI Master Write. It is A[23:4].
3:0	WO		Reserved

HParaType = 11h, Sub-Address = 06h
Fence Command Setting

Bits [23:0]	Attribute	Default	Description
23:0	WO		Lower 24-Bit Fence Command ID

HParaType = 11h, Sub-Address = 07h
Fence Command Setting

Bits [23:0]	Attribute	Default	Description
23	WO		Reserved
22	WO	0	Fence Command Queue Full Skip Active at first CR command. (for HFCMode with Writes Fence Queue and generate interrupt signal). 0: CR command (41c/420) pause, until Fence Command Queue has space. 1: CR keep running, overwrite Fence_ID to current write point in Fence queue.
21	WO		Fence Command Interrupt Wait For HFCMode with Writes Fence Queue & generate interrupt signal. 0: CR keep running, when CR_INT active, and write Fence_ID to Fence queue. 1: CR pause, until CR_INT is cleared by MMIO write (204[5]).
20	WO		Fence Command Trigger
19:16	WO		Fence Command Mode <HFCMode> 0000: Just record the HFCID 0001: Record the HFCID when all engines idle 0010: Just writes Fence Queue & generate interrupt signal and record the HFCID 0011: Writes Fence Queue & generate interrupt signal and record the HFCID when all engines idle 0100: Just Write out HFCID to System Memory and record the HFCID 0101: Write out HFCID to System Memory and record the HFCID when all engines idle 0110: Just Write out HFCID to System Memory, writes Fence Queue & generate interrupt signal and record the HFCID 0111: Write out HFCID to System Memory, writes Fence Queue & generate interrupt signal and record the HFCID when all engines idle Others: Reserved
15:8	WO		Higher 8-Bit Fence Command ID
7:0	WO		Reserved

Note: Traditional fence command can be put in main command buffer and sub-main command buffer.

Save Command Setting (08-0Bh)
HParaType = 11h, Sub-Address = 08h
Save Command Setting

Bit [23:0]	Attribute	Default	Description
23:4	WO		Lower 24-Bits of Save Buffer Start Base Address It is A[23:0] which A[3:0] is useless, 128 bit alignment.
3:2	WO		Reserved
1:0	WO		Save Buffer Location 00: SL 01: SF 10: SM 11: LL

HParaType = 11h, Sub-Address = 09h
Save Command Setting

Bit [23:0]	Attribute	Default	Description
23:9	WO		Reserved
8	WO	0	Store 3D Engine's Register Write Enable 0:Disable. It is not necessary to store 3D's register. 1:Enable. Store 3D's register.
7:0	WO		Higher 8-Bit of Save Buffer Start Base Address It is A[31:24].

HParaType = 11h, Sub-Address = 0Ah: Reserved
HParaType = 11h, Sub-Address = 0Bh
Save Command Setting

Bit [23:0]	Attribute	Default	Description
23:1	WO		Reserved
0	WO		Safe Trig for Save 3D Write Back Registers When this register set, CR save 3D write back registers and then keep run

Note : Priority T11A0B[0] (HParaType = 11h, Sub-Address = 0Bh, Bit [0]) > T11A09[8] (HParaType = 11h, Sub-Address = 09h, Bit [8]). If T11A0B[0] =1, all 3D save register will save to {T11A09[7:0], T11A08[23:4]} (HParaType = 11h, Sub-Address = 09h, Bit [7:0], HParaType = 11h, Sub-Address = 08h, Bit [23:4]) not T11A08[23:4] and T11A09[7:0].

Frame Buffer Automatic Swapping Setting (10-34h)
HParaType = 11h, Sub-Address = 10h
Frame Buffer Automatic Swapping Setting

Bit [23:0]	Attribute	Default	Description
23:3	WO		Lower 3-Bytes of Display Frame Buffer Base Address of IGA1
2	WO		Reserved
1:0	WO		Display Frame Buffer Location of IGA1 00: SL 01: SF 10: SM 11: LL

HParaType = 11h, Sub-Address = 11h
Frame Buffer Automatic Swapping Setting

Bit [23:0]	Attribute	Default	Description
23:8	WO		Frame Flip Count of IGA1
7:0	WO		Higher Byte of Display Frame Buffer Base Address of IGA1

HParaType = 11h, Sub-Address = 12h
Frame Buffer Automatic Swapping Setting

Bit [23:0]	Attribute	Default	Description
23:4	WO		Reserved
3	WO		Enable Frame Buffer Automatic Swapping for IGA1
2	WO	0	Skip to Wait Blank When Automatic Swapping for IGA1
1:0	WO		Reserved

HParaType = 11h, Sub-Address = 13-17h: Reserved
HParaType = 11h, Sub-Address = 18h
Frame Buffer Automatic Swapping Setting

Bit [23:0]	Attribute	Default	Description
23:3	WO		Lower 3 Bytes of Display Frame Buffer Base Address of IGA2
2	WO		Reserved
1:0	WO		Display Frame Buffer Location of IGA2 00: SL 01: SF 10: SM 11: LL

HParaType = 11h, Sub-Address = 19h
Frame Buffer Automatic Swapping Setting

Bit [23:0]	Attribute	Default	Description
23:8	WO		Frame Flip Count of IGA2
7:0	WO		Higher Byte of Display Frame Buffer Base Address of IGA2

HParaType = 11h, Sub-Address = 1Ah
Frame Buffer Automatic Swapping Setting

Bit [23:0]	Attribute	Default	Description
23:4	WO		Reserved
3	WO		Enable Frame Buffer Automatic Swapping for IGA2
2	WO	0	Skip to Wait Blank When Automatic Swapping for IGA2
1:0	WO		Reserved

HParaType = 11h, Sub-Address = 1B-2Fh: Reserved
HParaType = 11h, Sub-Address = 30h
Frame Buffer Automatic Swapping Setting

Bit [23:0]	Attribute	Default	Description
23:3	WO		Lower 3 Bytes of Display Frame Buffer Base Address of IGA
2	WO		Reserved
1:0	WO		Display Frame Buffer Location of IGA 00: SL 01: SF 10: SM 11: LL

HParaType = 11h, Sub-Address = 31h
Frame Buffer Automatic Swapping Setting

Bit [23:0]	Attribute	Default	Description
23:8	WO		Frame Flip Count of IGA
7:0	WO		Higher Byte of Display Frame Buffer Base Address of IGA

HParaType = 11h, Sub-Address = 32h
Frame Buffer Automatic Swapping Setting

Bit [23:0]	Attribute	Default	Description
23:4	WO		Reserved
3	WO		Enable Frame Buffer Automatic Swapping for IGA
2	WO	0	Skip to Wait Blank When Automatic Swapping for IGA
1:0	WO		Reserved

HParaType = 11h, Sub-Address = 33-34h: Reserved

Tradition Branch Command Setting (68-6Bh)

Please be noted that HParaType 11h, Sub-Address 68-6Bh (T11A68-6B) are only active in “AGP format” command.

HParaType = 11h, Sub-Address = 68h
Traditional Branch Command Setting

Bit [23:0]	Attribute	Default	Description
23:1	WO		Reserved
0	WO	0	Branch Type 0: Branch for Normal. Branch commands independent on previous command, Insert Branch commands in CR command queue. 1: Branch for Restore. Wait till all previous commands are finished before Branch header (FE8x), and then active Branch request.

HParaType = 11h, Sub-Address = 69h
Traditional Branch Command Setting

Bit [23:0]	Attribute	Default	Description
23:1	WO		Lower 3 Bytes of Branch Buffer Start Address It is A[23:1] which A[0] is useless. In unit of word (16-bit alignment).
0	WO		Reserved

HParaType = 11h, Sub-Address = 6Ah
Traditional Branch Command Setting

Bit [23:0]	Attribute	Default	Description
23:22	WO		Branch Buffer Location 00: SL 01: SF 10: SM 11: LL
21:8	WO		Reserved
7:0	WO		Higher Byte of Branch Buffer Start Address It is A[31:24].

Note: Branch command trigger is hidden in AGP header (FE8x). “nested” branch buffer is forbidden.

HParaType = 11h, Sub-Address = 6Bh
Traditional Branch Command Setting

Bit [23:0]	Attribute	Default	Description
23:0	WO		Size of Branch Buffer in Unit of 16 Bytes 128 bits.

3D REGISTERS

This chapter provides detailed 3D register descriptions. Please also refer to Chapter “Command Regulator”, Section “Settings of 3D/CR Registers” for basic introduction on 3D/CR operations and 3D/CR register summary table.

HParaType 00h: Primitive Vertex Data or Vertex Index

HParaType 00h is used for Primitive Vertex Data (for Vertex Command Mode) or Vertex Index (for Vertex Buffer Index Mode).

There is no sub-address in this ParaType. The steps of how to fire 3D Engine are as follows:

- Step 1: Set the correct value to all the related 3D globe registers through ParaType 01h, 02h, 03h, 04h, 10h, 11h and FEh.
- Step 2: Sent Vertex Data or Vertex Index (according to HVertexMode) through ParaType 00h. CR would configure the vertex (according HVFVLEN and HnFVF) and generate fire signal automatically whenever all the vertices of a primitive are ready (according to HVCycle, H2and1VT and HPMType). CR would also generate the PLEND (Primitive List End) signal whenever the entire listed vertexes are finished (according to HVTXnum), or receive a “Stop Command”.

For next primitive list, repeat the two steps above.

HParaType 01h: Attribute Other Than Texture

Sub-Address (Bits [31:24]): 00-AAh

HParaType = 01h, Sub-Address = 00-0Fh

Enable Setting 1

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	Reserved
22	WO	xxh	Inverse Enable (Disable) BE's 32-byte (Adjacent 128-bit) Packing 0: Enable 1: Disable
21	WO	xxh	Inverse Enable (Disable) BE's Smart Packing 0: Enable 1: Disable
20	WO	xxh	Enable Alpha Test Result of RT0 for All Render Targets (RTn) 0: The success or failure of alpha test for RTn depends on its own alpha test result and HenATMRTn, where n = 0 .. 3. 1: Execution of the alpha test for RT0 and all render targets depend on the result to be killed or not. HenATMRT0, HenATMRT1, HenATMRT2 & HenATMRT3 are ignored
19	WO	xxh	Enable Alpha Test for Render Target 3 <HenATMRT3> 0: Disable 1: Enable
18	WO	xxh	Enable Alpha Test for Render Target 2 <HenATMRT2> 0: Disable 1: Enable
17	WO	xxh	Enable Alpha Test for Render Target 1 <HenATMRT1> 0: Disable 1: Enable
16	WO	xxh	Enable Alpha Test for Render Target 0 <HenATMRT0> 0: Disable 1: Enable
15	WO	xxh	Enable Specula Color for Render Target 3 0: Disable 1: Enable
14	WO	xxh	Enable Specula Color for Render Target 2 0: Disable 1: Enable
13	WO	xxh	Enable Specula Color for Render Target 1 0: Disable 1: Enable
12	WO	xxh	Enable Specula Color for Render Target 0 0: Disable 1: Enable
11	WO	xxh	Enable Fog for Render Target 3 0: Disable 1: Enable
10	WO	xxh	Enable Fog for Render Target 2 0: Disable 1: Enable
9	WO	xxh	Enable Fog for Render Target 1 0: Disable 1: Enable
8	WO	xxh	Enable Fog for Render Target 0 0: Disable 1: Enable
7	WO	xxh	Enable Alpha Blending for Render Target 3 0: Disable 1: Enable
6	WO	xxh	Enable Alpha Blending for Render Target 2 0: Disable 1: Enable
5	WO	xxh	Enable Alpha Blending for Render Target 1 0: Disable 1: Enable
4	WO	xxh	Enable Alpha Blending for Render Target 0 0: Disable 1: Enable
3	WO	xxh	Enable Dither for Render Target 3 0: Disable 1: Enable
2	WO	xxh	Enable Dither for Render Target 2 0: Disable 1: Enable
1	WO	xxh	Enable Dither for Render Target 1 0: Disable 1: Enable
0	WO	xxh	Enable Dither for Render Target 0 0: Disable 1: Enable

HParaType = 01h, Sub-Address = 01h
Enable Setting 2

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	Enable Line Drawing from Up/Left to Down/Right 0: Draw line from vertex a to vertex b. 1: For vertical line, draw from up vertex to down vertex. For horizontal line, draw from left vertex to right vertex.
22	WO	xxh	Enable Diamond Rule for Line Drawing 0: Disable 1: Enable
21	WO	xxh	Enable Point Sprite 0: Disable 1: Enable This setting is only available for PMType "point" and "triangle point". All Points have sizes (default is 1.0), and Point Sprite only affects the texture coordinate. <u>If non-PointSprite points:</u> All the texture coordinates of point 4 vertexes are all those from FVF. <u>If PointSprite points:</u> Texture coordinate of the upper-left corner is (0, 0, 0, 1). Texture coordinate of the upper-right corner is (1, 0, 0, 1). Texture coordinate of the lower-left corner is (0, 1, 0, 1). Texture coordinate of the lower-right corner is (1, 1, 0, 1).
20	WO	xxh	Reserved
19	WO	xxh	Enable Fog Perspective Correction 0: Disable 1: Enable
18	WO	xxh	Enable Spectra Color Perspective Correction 0: Disable 1: Enable
17	WO	xxh	Enable Diffuse Color Perspective Correction 0: Disable 1: Enable
16:14	WO	xxh	Number of Render Target 000: Only RT0 001: RT0 & RT1 010: RT0, RT1 and RT2 011: RT0, RT1, RT2 and RT3 1xx: Reserved
13	WO	xxh	Enable of Coarse Z Test 0: Disable 1: Enable Note that Coarse Z Test is only available for triangles, not the lines.
12	WO	xxh	Enable Vertex Cache 0: Disable 1: Enable
11	WO	xxh	Enable Clipping Engine 0: Disable 1: Enable
10	WO	xxh	Reserved
9	WO	xxh	Enable Writing Coarse Z Buffer 0: Do not update the Coarse Z Buffer 1: Enable
8	WO	xxh	Enable Texture Cache 0: Disable Texture Cache and Clear Texture Cache 1: Enable
7	WO	xxh	Enable Back Face Culling <HenBFCull> 0: Disable 1: Enable
6	WO	xxh	Enable Color Write 0: Disable 1: Enable
5	WO	xxh	Enable Anti-Aliasing 0: Disable 1: Enable
4	WO	xxh	Enable Stencil Test 0: Disable (Always pass) 1: Enable (Depth buffer must contain stencil bits)
3	WO	xxh	Enable Z Test 0: Disable (Always pass) 1: Enable
2	WO	xxh	Enable Z Write 0: Disable 1: Enable
1	WO	xxh	Enable Stipple Pattern 0: Disable 1: Enable
0	WO	xxh	Enable Line Pattern 0: Disable 1: Enable

HParaType = 01h, Sub-Address = 02h
Enable Setting 3

Bits [23:0]	Attribute	Default	Description
23:2	WO	xxh	Reserved
1	WO	xxh	Clear Read-Color Cache (RC Cache) RC Cache will be cleared while this bit is set to 1.
0	WO	xxh	Enable Read-Color Cache 0: Disable 1: Enable

HParaType = 01h, Sub-Address = 03-0Fh: Reserved (for Enable Setting)

HParaType = 01h, Sub-Address = 10h
Z Setting 1

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	ZW Buffer Base Address In unit of 256 bytes.

HParaType = 01h, Sub-Address = 11h
Z Setting 2

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	Reserved
22:13	WO	xxh	ZW Buffer Pitch <HZWBPit> In unit of 32 bytes for linear mode. In unit of tile (256 bytes) for tile mode.
12	WO	xxh	Enable Reading-Z Cache 0: Disable 1: Enable
11	WO	xxh	Clear Reading-Z Cache
10	WO	xxh	Mode of Reading-Z Cache 0: 128-bit mode 1: 256-bit mode
9	WO	xxh	Z and Stencil Value are written through to BE directly 0: Fully data path from PERZ through PS and RC, and then to BE 1: Short data path from PERZ to BE directly
8:2	WO	xxh	Reserved
1:0	WO	xxh	Location Setting of Z Buffer 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: Reserved (System Memory) 11: Reserved (Local Memory Local Frame Buffer (L.L.))

HParaType = 01h, Sub-Address = 12h
Z Setting 3

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	ZW Buffer Type 0: ZW buffer stores Z value 1: ZW buffer stores W value (PP replaces Z by W)
22	WO	xxh	Reserved
21	WO	xxh	Force the Z Value from 1.0 to 1.0- (from 1.00000000h to 0.FFFFFFFFh) 0: Keep the original 1.0 1: Force to 1.0- whenever Z equals to 1.0 This register is only useful for fixed-point format.
20	WO	xxh	Clamp the Z Value is over 1.0 to 1.0- (from 1.xxxxxxxxh to 0.FFFFFFFFh) 0: Keep the original value over 1.0 1: Clamp to 1.0- whenever Z is over 1.0 This register is only useful for fixed-point format.
19	WO	xxh	Clamp the Z Value is Negative to Zero for Z Test - (from -x.xxxxxxxxh to 0.00000000 h) 0: Keep the original negative value 1: Clamp to 0.0- whenever Z is negative Note: These clamping registers do not affect the test of nearby or distant plane. The test of the nearby or distant plane is by the original biased and un-clamped Z value with floating format.
18:16	WO	xxh	ZW Buffer Format For Z Buffer 000: 16-bit fixed-point format, $0.0 \leq Z < 1.0$ 001: 16-bit floating format s[5].10 from $+2^{31} * 1.FFFF$ to $-2^{31} * 1.FFFF$ 010: Reserved 011: Reserved 100: 32-bit fixed-point format, $0.0 \leq Z < 1.0$ 101: 32-bit fixed-point format s[8].23 110: 24-bit fixed-point format Z, $0.0 \leq Z < 1.0$, and Stencil Z is located in bit [31:8], Stencil is located in bit [7:0]
15:7	WO	xxh	Reserved
6:5	WO	xxh	Location Setting of Separated Stencil Buffer 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: Reserved (System Memory) 11: Reserved (Local Memory Local Frame Buffer (L.L.))
4	WO	xxh	Write Stencil Value of the Separated Stencil Buffer to the Z Buffer 0: Normal 1: Force "STVALID" as true and stencil operation as "Keep", so the stencil value in the separated buffer can be filled into Z buffer.
3	WO	xxh	Synchronized with the Separated Stencil Value in Z Buffer Indicate whether the stencil value in the separated stencil buffer is synchronized with the stencil value in Z buffer. 0: No synchronization. Hardware just updates the stencil value in the separated stencil buffer, which may not be synchronized to the stencil value in Z buffer. 1: The stencil value in the separated stencil buffer is synchronized to the stencil value in Z buffer. Hardware would update the separated stencil buffer and Z buffer.
2	WO	xxh	Existence of Separated Stencil Buffer 0: No separated stencil buffer 1: There is a separated stencil buffer
1	WO	xxh	Extend for Z Format Transformation 0: Do nothing. For Z with 32-bit floating s[8].23 and mantissa as 1.Z[22:0], it will be extended to 1.{Z[22:0], 8'h00} and transformed to fixed-format. 1: Extend mantissa to 32 bits before format transformation. Consider Z with 32-bit floating s[8].23 and mantissa as 1.Z[22:0], it will be extended to 1.{Z[22:0], 1'b1, Z[22:16]} and transformed to fixed format.
0	WO	xxh	Memory Mode of ZW Buffer 0: Linear mode 1: Tile mode

HParaType = 01h, Sub-Address = 13h
Z Setting 4

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	Reserved
22:19	WO	xxh	Reserved
18:16	WO	xxh	ZW Test Mode <HZWTMD> 000: Z or W test never pass 001: Z or W test pass if Znew < Zdst 010: Z or W test pass if Znew = Zdst 011: Z or W test pass if Znew ≤ Zdst 100: Z or W test pass if Znew > Zdst 101: Z or W test pass if Znew ≠ Zdst 110: Z or W test pass if Znew ≥ Zdst 111: Z or W test always pass Where Znew is the calculated Z value and Zdst is the Z stored in the Z buffer.
15:8	WO	xxh	Reserved
7:0	WO	xxh	Z Normalization Factor The range is from 0 to 255. By definition, Z can be divided by a value of power of 2. Thus, it allows the input Z free from the constrain of Z < 1. Z Normalization is $Z = Z_{in} / 2^{HZNF}$

HParaType = 01h, Sub-Address = 14h
Z Setting 5

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Lower 3 Bytes of ZW Clear Data

HParaType = 01h, Sub-Address = 15h
Z Setting 6

Bits [23:0]	Attribute	Default	Description
23:8	WO	xxh	Negative of Mask to the Zsrc's Last 16-bit Mantissa Note that this mask is just implemented to the rendered Z value for format transformation, then a Z test is conducted and wrote-back to Z buffer. Consider the generated Z value "Zsrc[31:0]" with floating s[8].23: Step1: Zsrc[15:0] = Zsrc[15:0] & ~HZWMMSK_N[15:0] Step2: Format transform Zsrc according to HZWFM Step3: Z test Step4: Updated Z buffer with the format transformed Zsrc if Z test is passed
7:0	WO	xxh	Highest Byte of ZW Clear Data

HParaType = 01h, Sub-Address = 16h
Z Setting 7

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Lower 3 Bytes of Z Bias Offset With 32-bit floating format, since Z format transformation is between fixed and floating, and HZBiasOffset description is suggested to be modified as below: If (HZWBFM == 32-bit fixed) $HZBiasOffset = HZBiasOffset * (2^{32} - 1) / 2^{32}$ Else if (HZWBFM == 24-bit fixed) $HZBiasOffset = HZBiasOffset * (2^{24} - 1) / 2^{24}$ Else if (HZWBFM == 16-bit fixed) $HZBiasOffset = HZBiasOffset * (2^{16} - 1) / 2^{16}$

HParaType = 01h, Sub-Address = 17h
Z Setting 8

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	Bias Scale with 32-bit Floating Format
15:8	WO	xxh	Reserved
7:0	WO	xxh	Highest Byte of Z Bias Offset SEZbias = max(Zdx, Zdy) * HZBiasScale + HZBias Offset

HParaType = 01h, Sub-Address = 18h
Z Setting 9

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Z Bias Scale With 32-bit Floating Format

HParaType = 01h, Sub-Address = 19h
Z Setting 10

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Low 23 Bits of Low Boundary to Clamp the Z Bias With format of 32-bit floating.

HParaType = 01h, Sub-Address = 1Ah
Z Setting 11

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Low 23 Bits of High Boundary to Clamp the Z Bias With format of 32-bit floating.

HParaType = 01h, Sub-Address = 1Bh
Z Setting 12

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	Enhance Z's Precision During PE Rendering 0: Disable 1: Enable
22:16	WO	xxh	Reserved
15:8	WO	xxh	High 8 Bits of High Boundary to Clamp the Z Bias With format of 32-bit floating.
7:0	WO	xxh	High 8 Bits of Low Boundary to Clamp the Z Bias With format of 32-bit floating.

HParaType = 01h, Sub-Address = 1Ch
Z Setting 13

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Low 24 Bits Occlusion Count of both Z Test and Stencil Test Result

HParaType = 01h, Sub-Address = 1Dh
Z Setting 14

Bits [23:0]	Attribute	Default	Description
23:8	WO	xxh	Reserved
7:0	WO	xxh	High 8 Bits Occlusion Count of Both Z Test and Stencil Test Result

HParaType = 01h, Sub-Address = 1Eh
Z Setting 15

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Lower 24 Bits of Clip Plane's Far Value

HParaType = 01h, Sub-Address = 1Fh
Z Setting 16

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Lower 24 Bits of Clip Plane's Near Value

HParaType = 01h, Sub-Address = 20h
Z Setting 17

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	Reserved
15:8	WO	xxh	Higher 8 Bits of Clip Plane's Far Value With format of 32-bit floating.
7:0	WO	xxh	Higher 8 Bits of Clip Plane's Near Value With format of 32-bit floating. Check each pixel's Z value before depth testing, and remove this pixel if it's out of the range. If (Z > HZClipFar Z < HZClipNear) Drop this pixel Else Do Depth Testing Note that this check is in higher priority than "Z Window".

HParaType = 01h, Sub-Address = 23h
Stencil Setting 1

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	Stencil Test Reference Value for Clock-Wise Face <HSTCWREF> This value is a positive 8-bit fixed point number with range from 0 to 255, which is used for Stencil Test as the comparison result between Stencil and HSTCWREF.
15:8	WO	xxh	Stencil Test Operation Mask for Clock-Wise Face <HSTCWOPMSK> Indicates the comparison result between (Stencil & HSTOPMSK) and (HSTREF & HSTOPMSK). <i>If Clockwise:</i> HSTOPMSK = HSTCWOPMSK HSTREF = HSTCWREF <i>Else:</i> HSTOPMSK = HSTCCWOPMSK HSTREF = HSTCCWREF
7:0	WO	xxh	Stencil Buffer Bit Mask for Clock-Wise Face <HSTCWBMASK> If this bit = 0, the corresponding bit in the stencil buffer cannot be changed. Otherwise, it can be changed.

HParaType = 01h, Sub-Address = 24h
Stencil Setting 2

Bits [23:0]	Attribute	Default	Description
23:19	WO	xxh	Reserved
18:16	WO	xxh	Stencil Test Mode for Clock-Wise Face 000: Stencil Test never pass 001: Stencil Test pass if (HSTCCWREF & HSTCCWOPMSK) < (Stencil & HSTCCWOPMSK) 010: Stencil Test pass if (HSTCCWREF & HSTCCWOPMSK) = (Stencil & HSTCCWOPMSK) 011: Stencil Test pass if (HSTCCWREF & HSTCCWOPMSK) ≤ (Stencil & HSTCCWOPMSK) 100: Stencil Test pass if (HSTCCWREF & HSTCCWOPMSK) > (Stencil & HSTCCWOPMSK) 101: Stencil Test pass if (HSTCCWREF & HSTCCWOPMSK) ≠ (Stencil & HSTCCWOPMSK) 110: Stencil Test pass if (HSTCCWREF & HSTCCWOPMSK) ≥ (Stencil & HSTCCWOPMSK) 111: Stencil Test always pass
15:9	WO	xxh	Reserved
8:6	WO	xxh	Stencil Operation for Stencil Test Fail for Clock-Wise Face 000: KEEP 001: ZERO 010: REPLACE 011: INCRSAT 100: DECRSAT 101: INVERT 110: INCR 111: DECR
5:3	WO	xxh	Stencil Operation for Stencil Test Pass and Z Test Fail for Clock-Wise Face 000: KEEP 001: ZERO 010: REPLACE 011: INCRSAT 100: DECRSAT 101: INVERT 110: INCR 111: DECR
2:0	WO	xxh	Stencil Operation for Stencil Test Pass and Z Test Pass for Clock-Wise Face 000: KEEP 001: ZERO 010: REPLACE 011: INCRSAT 100: DECRSAT 101: INVERT 110: INCR 111: DECR

HParaType = 01h, Sub-Address = 25h
Stencil Setting 3

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	Stencil Test Reference Value for Counter-Clock-Wise Face <HSTCCWREF> This value is a positive 8-bit fixed point number with range from 0 to 255, which is used for Stencil Test as the comparison result between Stencil and HSTCCWREF.
15:8	WO	xxh	Stencil Test Operation Mask for Counter-Clock-Wise Face <HSTCCWOPMSK> Indicates the comparison result between (Stencil & HSTCCWOPMSK) and (HSTCCWREF & HSTCCWBMSK).
7:0	WO	xxh	Stencil Buffer Bit Mask for Counter-Clock-Wise Face <HSTCCWBMSK> If this bit = 0, the corresponding bit in the stencil buffer cannot be changed. Otherwise, it can be changed.

HParaType = 01h, Sub-Address = 26h
Stencil Setting 4

Bits [23:0]	Attribute	Default	Description
23:19	WO	xxh	Reserved
18:16	WO	xxh	Stencil Test Mode for Counter-Clock-Wise Face 000: Stencil Test never pass 001: Stencil Test pass if (HSTCCWREF & HSTCCWOPMSK) < (Stencil & HSTCCWOPMSK) 010: Stencil Test pass if (HSTCCWREF & HSTCCWOPMSK) = (Stencil & HSTCCWOPMSK) 011: Stencil Test pass if (HSTCCWREF & HSTCCWOPMSK) ≤ (Stencil & HSTCCWOPMSK) 100: Stencil Test pass if (HSTCCWREF & HSTCCWOPMSK) > (Stencil & HSTCCWOPMSK) 101: Stencil Test pass if (HSTCCWREF & HSTCCWOPMSK) ≠ (Stencil & HSTCCWOPMSK) 110: Stencil Test pass if (HSTCCWREF & HSTCCWOPMSK) ≥ (Stencil & HSTCCWOPMSK) 111: Stencil Test always pass
15:9	WO	xxh	Reserved
8:6	WO	xxh	Stencil Operation for Stencil Test Fail for Counter-Clock-Wise Face 000: KEEP 001: ZERO 010: REPLACE 011: INCRSAT 100: DECRSAT 101: INVERT 110: INCR 111: DECR
5:3	WO	xxh	Stencil Operation for Stencil Test Pass and Z Test Fail for Counter-Clock-Wise Face 000: KEEP 001: ZERO 010: REPLACE 011: INCRSAT 100: DECRSAT 101: INVERT 110: INCR 111: DECR
2:0	WO	xxh	Stencil Operation for Stencil Test Pass and Z Test Pass for Counter-Clock-Wise Face 000: KEEP 001: ZERO 010: REPLACE 011: INCRSAT 100: DECRSAT 101: INVERT 110: INCR 111: DECR

HParaType = 01h, Sub-Address = 27h
Setting for Fast-Z-Clear 1

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	Reserved
15:12	WO	xxh	Index of ZW Buffer for Current Scene
11:8	WO	xxh	Length of HZWBIdx in Unit of Bit 0000: Disable ZW buffer index 0001: Use the LSB 1 bit as ZW buffer index 0010: Use the LSB 2 bits as ZW buffer index 0011: Use the LSB 3 bits as ZW buffer index 0100: Use the LSB 4 bits as ZW buffer index 1111 ~ 0101: Reserved
7:1	WO	xxh	Reserved
0	WO	xxh	Enable Fast-Z-Clear 0: Disable 1: Enable

HParaType = 01h, Sub-Address = 28h
Setting for Fast-Z-Clear 2

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Stencil Buffer's Base Address <HSTBas> In unit of 256 bytes. The pitch of the separated stencil buffer is just the setting of the Z buffer pitch. Since there is only Z24S8 format for the stencil value, the Z must be 32 bpp when separated stencil buffer is enabled. No matter Z buffer is in linear or tile mode, the HZWBPit is just $(W+7) \gg 3$, where W is the screen coordinate. $E3R(W)STADR = HSTBas * 256 + Y[10:3] * HZWBPit * 64 + X[10:3] * 64 + Y[2:1] * 16$

HParaType = 01h, Sub-Address = 29h
Setting for Coarse Z Test Function 1

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	Force CZ Retest If Original Is "Reject" and the Related Primitive Is Clock-Wise Force the CZ result as "ReTEST" if original is "REJECT" and the related primitive is Clock-Wise. 0: Normal CZ test 1: Never reject
22	WO	xxh	Force CZ Retest If Original Is "Pass" and the Related Primitive Is Clock-Wise Force the CZ result as "ReTEST" if original is "Pass" and the related primitive is Clock-Wise. 0: Normal CZ test 1: Never pass
21:20	WO	xxh	Coarse Z Buffer Location Setting 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: Reserved (System Memory) 11: Reserved (Local Memory Local Frame Buffer (L.L.))
19:18	WO	xxh	Reserved
17	WO	xxh	Inverse Mode for CZ Test 0: Smaller Z value as nearer and larger Z value as farer, for HZWTMD is LESS or LESSEQUAL 1: Larger Z value as nearer and smaller Z value as farer, for HZWTMD is GREATER or GREATEREQUAL
16	WO	xxh	Coarse Z Write Back Mode 0: Whenever the CZTAG_CNT is "0" and CZTAG_UPDATED, write the CZ in cache back to video memory 1: Whenever the cell is selected for new CZ value and CZTAG_UPDATED, write the old CZ in cache back to video memory, and then read the new CZ value.
15	WO	xxh	Reset of CZ Cache's TAG Instead of having software to clear this setting, it would be auto-cleared by hardware. 0: Normal 1: Rest
14	WO	xxh	Reserved
13:12	WO	xxh	Coarse Z Test by Using Conservative Mode 00: Use optimized merging rule 01: Use Conservative Merging Rule and only update both "MIN" value and "MAX" value 10: Use Conservative Merging Rule and only update "MIN" value 11: Reserved
11	WO	xxh	Force CZ Retest If Original Is "Reject" and the Related Primitive Is Counter-Clock-Wise Force the CZ result as "ReTEST" if original is "REJECT" and the related primitive is Counter-Clock-Wise. 0: Normal CZ test 1: Never reject
10	WO	xxh	Force CZ Retest If Original Is "Pass" and the Related Primitive Is Counter-Clock-Wise Force the CZ result as "ReTEST" if original is "REJECT" and the related primitive is Counter-Clock-Wise. 0: Normal CZ test 1: Never reject
9	WO	xxh	Force ReTest as the Result of HZ Test 0: Normal 1: Force
8:0	WO	xxh	Coarse Z Buffer's Pitch In unit of 32 bytes.

HParaType = 01h, Sub-Address = 2Ah
Setting for Coarse Z Test Function 2

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Coarse Z Buffer's Base Address In unit of 256 bytes. $E3R(W)CZADR = HCZBas*256 + Y*HCZPit*32 + (2*X)*16$

HParaType = 01h, Sub-Address = 33h
Alpha Setting 1

Bits [23:0]	Attribute	Default	Description
23:15	WO	xxh	Reserved
14:12	WO	xxh	Alpha Test Mode 000: Alpha test never pass 001: Alpha test pass if Anew < HATREF (bits [10:0]) 010: Alpha test pass if Anew = HATREF 011: Alpha test pass if Anew ≤ HATREF 100: Alpha test pass if Anew > HATREF 101: Alpha test pass if Anew ≠ HATREF 110: Alpha test pass if Anew ≥ HATREF 111: Alpha test always pass
11	WO	xxh	Reserved
10:0	WO	xxh	Alpha Test Reference Value <HATREF> Positive fixed-point from 0.0 to 1.0.

HParaType = 01h, Sub-Address = 34h
Alpha Setting 2
Alpha Blending Equation of RGB:

Equation of RGB: Cout = ((AB_FCa * AB_Ca) AB_Cop (AB_FCb * AB_Cb))

If (HABLCsat = false) Clamp Cout to 1.0 to 0.0

Bits [23:0]	Attribute	Default	Description																																																				
23:17	WO	xxh	Reserved																																																				
16	WO	xxh	RGB Saturation Control of Alpha Blending Calculation <HABLCsat> 0: Cout will be clamp to 0.0 ~ 1.0 1: Cout will not be clamp to 0.0 ~ 1.0																																																				
15:10	WO	xxh	Ca of Alpha Blending Equation <HABLCa> HABLCa[5:4] Reserved <table border="1"> <thead> <tr> <th>HABLCa[3:0]</th> <th>R_of_OPca</th> <th>G_of_OPca</th> <th>B_of_OPca</th> </tr> </thead> <tbody> <tr> <td>0001</td> <td>Rsrc</td> <td>Gsrc</td> <td>Bsrc</td> </tr> <tr> <td>0001</td> <td>Rdst</td> <td>Gdst</td> <td>Bdst</td> </tr> <tr> <td>0101</td> <td>R of HABLRCa</td> <td>G of HABLRCa</td> <td>B of HABLRCa</td> </tr> <tr> <td>0110</td> <td>min (Rsrc, Rdst)</td> <td>min (Gsrc, Gdst)</td> <td>min (Bsrc, Bdst)</td> </tr> <tr> <td>0111</td> <td>max (Rsrc, Rdst)</td> <td>max (Gsrc, Gdst)</td> <td>max (Bsrc, Bdst)</td> </tr> <tr> <td>Others</td> <td>Reserved</td> <td>Reserved</td> <td>Reserved</td> </tr> </tbody> </table>	HABLCa[3:0]	R_of_OPca	G_of_OPca	B_of_OPca	0001	Rsrc	Gsrc	Bsrc	0001	Rdst	Gdst	Bdst	0101	R of HABLRCa	G of HABLRCa	B of HABLRCa	0110	min (Rsrc, Rdst)	min (Gsrc, Gdst)	min (Bsrc, Bdst)	0111	max (Rsrc, Rdst)	max (Gsrc, Gdst)	max (Bsrc, Bdst)	Others	Reserved	Reserved	Reserved																								
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9:4	WO	xxh	FCa of Alpha Blending Equation <HABLFCa> <table border="1"> <thead> <tr> <th>HABLFCa[5:4]</th> <th>R of AB_Fca</th> <th>G of AB_FCa</th> <th>B of AB_FCa</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>R_of_OPFCa</td> <td>G_of_OPFCa</td> <td>B_of_OPFCa</td> </tr> <tr> <td>01</td> <td>1.0 - R_of_OPFCa</td> <td>1.0 - G_of_OPFCa</td> <td>1.0 - B_of_OPFCa</td> </tr> <tr> <td>11</td> <td>Reserved</td> <td>Reserved</td> <td>Reserved</td> </tr> <tr> <td>Other</td> <td>Reserved</td> <td>Reserved</td> <td>Reserved</td> </tr> </tbody> </table> <table border="1"> <thead> <tr> <th>HABLFCa[3:0]</th> <th>R_of_OPFCa</th> <th>G_of_OPFCa</th> <th>B_of_OPFCa</th> </tr> </thead> <tbody> <tr> <td>0000</td> <td>Rsrc</td> <td>Gsrc</td> <td>Bsrc</td> </tr> <tr> <td>0001</td> <td>Rdst</td> <td>Gdst</td> <td>Bdst</td> </tr> <tr> <td>0010</td> <td>Asrc</td> <td>Asrc</td> <td>Asrc</td> </tr> <tr> <td>0011</td> <td>Adst</td> <td>Adst</td> <td>Adst</td> </tr> <tr> <td>0101</td> <td>R of HABLRFca</td> <td>G of HABLRFca</td> <td>B of HABLRFca</td> </tr> <tr> <td>1000</td> <td>min (Asrc, 1-Adst)</td> <td>min (Asrc, 1-Adst)</td> <td>min (Asrc, 1-Adst)</td> </tr> <tr> <td>Others</td> <td>Reserved</td> <td>Reserved</td> <td>Reserved</td> </tr> </tbody> </table>	HABLFCa[5:4]	R of AB_Fca	G of AB_FCa	B of AB_FCa	00	R_of_OPFCa	G_of_OPFCa	B_of_OPFCa	01	1.0 - R_of_OPFCa	1.0 - G_of_OPFCa	1.0 - B_of_OPFCa	11	Reserved	Reserved	Reserved	Other	Reserved	Reserved	Reserved	HABLFCa[3:0]	R_of_OPFCa	G_of_OPFCa	B_of_OPFCa	0000	Rsrc	Gsrc	Bsrc	0001	Rdst	Gdst	Bdst	0010	Asrc	Asrc	Asrc	0011	Adst	Adst	Adst	0101	R of HABLRFca	G of HABLRFca	B of HABLRFca	1000	min (Asrc, 1-Adst)	min (Asrc, 1-Adst)	min (Asrc, 1-Adst)	Others	Reserved	Reserved	Reserved
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Others	Reserved	Reserved	Reserved																																																				
3:0	WO	xxh	Reserved																																																				

HParaType = 01h, Sub-Address = 35h
Alpha Setting 3

Bits [23:0]	Attribute	Default	Description																																																
23:16	WO	xxh	Reserved																																																
15:14	WO	xxh	Cop of Alpha Blending Equation <HABLCop> <table border="1"> <thead> <tr> <th>HABLCop</th> <th>Cop</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>+</td> </tr> <tr> <td>01</td> <td>-</td> </tr> <tr> <td>10</td> <td>Max</td> </tr> <tr> <td>11</td> <td>Min</td> </tr> </tbody> </table>	HABLCop	Cop	00	+	01	-	10	Max	11	Min																																						
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13:8	WO	xxh	Cb of Alpha Blending Equation <HABLCb> HABLCb[5:4] Reserved <table border="1"> <thead> <tr> <th>HABLCb[3:0]</th> <th>R_of_OPcb</th> <th>G_of_OPcb</th> <th>B_of_OPcb</th> </tr> </thead> <tbody> <tr> <td>0000</td> <td>Rsrc</td> <td>Gsrc</td> <td>Bsrc</td> </tr> <tr> <td>0001</td> <td>Rdst</td> <td>Gdst</td> <td>Bdst</td> </tr> <tr> <td>0101</td> <td>R of HABLRCb</td> <td>G of HABLRCb</td> <td>B of HABLRCb</td> </tr> <tr> <td>Others</td> <td>Reserved</td> <td>Reserved</td> <td>Reserved</td> </tr> </tbody> </table>	HABLCb[3:0]	R_of_OPcb	G_of_OPcb	B_of_OPcb	0000	Rsrc	Gsrc	Bsrc	0001	Rdst	Gdst	Bdst	0101	R of HABLRCb	G of HABLRCb	B of HABLRCb	Others	Reserved	Reserved	Reserved																												
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7:2	WO	xxh	FCb of Alpha Blending Equation <HABLFCb> <table border="1"> <thead> <tr> <th>HAB_FCb[5:4]</th> <th>R of AB_FCb</th> <th>G of AB_FCb</th> <th>B of AB_FCb</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>R_of_OPFCb</td> <td>G_of_OPFCb</td> <td>B_of_OPFCb</td> </tr> <tr> <td>01</td> <td>1.0 - (R_of_OPFCb)</td> <td>1.0 - (G_of_OPFCb)</td> <td>1.0 - (B_of_OPFCb)</td> </tr> <tr> <td>Others</td> <td>Reserved</td> <td>Reserved</td> <td>Reserved</td> </tr> </tbody> </table> <table border="1"> <thead> <tr> <th>HAB_FCb[3:0]</th> <th>R_of_OPFCb</th> <th>G_of_OPFCb</th> <th>B_of_OPFCb</th> </tr> </thead> <tbody> <tr> <td>0000</td> <td>Rsrc</td> <td>Gsrc</td> <td>Bsrc</td> </tr> <tr> <td>0001</td> <td>Rdst</td> <td>Gdst</td> <td>Bdst</td> </tr> <tr> <td>0010</td> <td>Asrc</td> <td>Asrc</td> <td>Asrc</td> </tr> <tr> <td>0011</td> <td>Adst</td> <td>Adst</td> <td>Adst</td> </tr> <tr> <td>0101</td> <td>R of HABLRFcb</td> <td>G of HABLRFcb</td> <td>B of HABLRFcb</td> </tr> <tr> <td>1000</td> <td>min (Asrc, 1-Adst)</td> <td>min (Asrc, 1-Adst)</td> <td>min (Asrc, 1-Adst)</td> </tr> <tr> <td>Others</td> <td>Reserved</td> <td>Reserved</td> <td>Reserved</td> </tr> </tbody> </table>	HAB_FCb[5:4]	R of AB_FCb	G of AB_FCb	B of AB_FCb	00	R_of_OPFCb	G_of_OPFCb	B_of_OPFCb	01	1.0 - (R_of_OPFCb)	1.0 - (G_of_OPFCb)	1.0 - (B_of_OPFCb)	Others	Reserved	Reserved	Reserved	HAB_FCb[3:0]	R_of_OPFCb	G_of_OPFCb	B_of_OPFCb	0000	Rsrc	Gsrc	Bsrc	0001	Rdst	Gdst	Bdst	0010	Asrc	Asrc	Asrc	0011	Adst	Adst	Adst	0101	R of HABLRFcb	G of HABLRFcb	B of HABLRFcb	1000	min (Asrc, 1-Adst)	min (Asrc, 1-Adst)	min (Asrc, 1-Adst)	Others	Reserved	Reserved	Reserved
HAB_FCb[5:4]	R of AB_FCb	G of AB_FCb	B of AB_FCb																																																
00	R_of_OPFCb	G_of_OPFCb	B_of_OPFCb																																																
01	1.0 - (R_of_OPFCb)	1.0 - (G_of_OPFCb)	1.0 - (B_of_OPFCb)																																																
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HAB_FCb[3:0]	R_of_OPFCb	G_of_OPFCb	B_of_OPFCb																																																
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1000	min (Asrc, 1-Adst)	min (Asrc, 1-Adst)	min (Asrc, 1-Adst)																																																
Others	Reserved	Reserved	Reserved																																																
1:0	WO	xxh	Reserved																																																

HParaType = 01h, Sub-Address = 36h
Alpha Setting 4
Equation of A:
Equation of RGB:

$$A_{out} = ((AB_FAa * AB_Aa) AB_Aop (AB_FAb * AB_Ab))$$

If (HABLASat = false) Clamp Aout to 1.0 to 0.0

Bits [23:0]	Attribute	Default	Description																										
23:17	WO	xxh	Reserved																										
16	WO	xxh	Alpha Saturation Control of Alpha Blending Calculation <HABLASat> 0: Aout will be clamped to 0.0 ~ 1.0 1: Aout will not be clamped to 0.0 ~ 1.0																										
15:10	WO	xxh	Aa of Alpha Blending Equation <HABLAa> HABLAa[5:4] Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>HABLAa[3:0]</th> <th>OPAA</th> </tr> </thead> <tbody> <tr><td>0000</td><td>0</td></tr> <tr><td>0001</td><td>Asrc</td></tr> <tr><td>0010</td><td>Adst</td></tr> <tr><td>0101</td><td>min (Asrc, Adst)</td></tr> <tr><td>0111</td><td>max (Asrc, Adst)</td></tr> <tr><td>1000</td><td>Reserved</td></tr> <tr><td>1001</td><td>HABLRaa</td></tr> <tr><td>1111-1010</td><td>Reserved</td></tr> <tr><td>Others</td><td>Reserved</td></tr> </tbody> </table>	HABLAa[3:0]	OPAA	0000	0	0001	Asrc	0010	Adst	0101	min (Asrc, Adst)	0111	max (Asrc, Adst)	1000	Reserved	1001	HABLRaa	1111-1010	Reserved	Others	Reserved						
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9:4	WO	xxh	FAa of Alpha Blending Equation <HABLFAa> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>HABLFAa[5:4]</th> <th>AB FAa</th> </tr> </thead> <tbody> <tr><td>00</td><td>OPFAa</td></tr> <tr><td>01</td><td>1 - OPFAa</td></tr> <tr><td>11</td><td>Reserved</td></tr> <tr><td>Other</td><td>Reserved</td></tr> </tbody> </table> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>HABLFAa[3:0]</th> <th>OPFAa</th> </tr> </thead> <tbody> <tr><td>0000</td><td>0</td></tr> <tr><td>0001</td><td>Asrc</td></tr> <tr><td>0010</td><td>Adst</td></tr> <tr><td>1000</td><td>min (Asrc, 1-Adst)</td></tr> <tr><td>1001</td><td>HABLRFAa</td></tr> <tr><td>1111-1101</td><td>Reserved</td></tr> <tr><td>Others</td><td>Reserved</td></tr> </tbody> </table>	HABLFAa[5:4]	AB FAa	00	OPFAa	01	1 - OPFAa	11	Reserved	Other	Reserved	HABLFAa[3:0]	OPFAa	0000	0	0001	Asrc	0010	Adst	1000	min (Asrc, 1-Adst)	1001	HABLRFAa	1111-1101	Reserved	Others	Reserved
HABLFAa[5:4]	AB FAa																												
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Other	Reserved																												
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0000	0																												
0001	Asrc																												
0010	Adst																												
1000	min (Asrc, 1-Adst)																												
1001	HABLRFAa																												
1111-1101	Reserved																												
Others	Reserved																												
3:0	WO	xxh	Reserved																										

HParaType = 01h, Sub-Address = 37h
Alpha Setting 5

Bits [23:0]	Attribute	Default	Description	
23:16	WO	xxh	Reserved	
15:14	WO	xxh	Aop of Alpha Blending Equation <HABLAop>	
			HABLAop	AB_Aop
			00	+
			01	-
			10	Max
			11	Min
13:8	WO	xxh	Ab of Alpha Blending Equation <HABLAB>	
			HABLAB[5:4] Reserved	
			HABLAB[3:0]	OPAb
			0000	0
			0001	Asrc
			0010	Adst
			1000	min (Asrc, 1-Adst)
			1001	HABLRAb
			1111-1001	Reserved
			Others	Reserved
7:2	WO	xxh	Fab of Alpha Blending Equation <HABLFab>	
			HABLFab[5:4]	AB_FAb
			00	OPFAb
			01	1 - OPFAb
			Others	Reserved
			HABLFab[3:0]	OPFAb
			0000	0
			0001	Asrc
			0010	Adst
			1000	min (Asrc, 1-Adst)
			1001	HABLRFAb
			Others	Reserved
			1:0	WO

HParaType = 01h, Sub-Address = 38h
Alpha Setting 6

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	Reserved
22:12	WO	xxh	G of HABLRCa This is an 11-bit positive fixed-point number from 0.0 to 1.0.
11	WO	xxh	Reserved
10:0	WO	xxh	B of HABLRCa This is an 11-bit positive fixed-point number from 0.0 to 1.0.

HParaType = 01h, Sub-Address = 39h
Alpha Setting 7

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	Reserved
22:12	WO	xxh	R of HABLRFCA This is an 11-bit positive fixed-point number from 0.0 to 1.0.
11	WO	xxh	Reserved
10:0	WO	xxh	R of HABLRCa This is an 11-bit positive fixed-point number from 0.0 to 1.0.

HParaType = 01h, Sub-Address = 3Ah
Alpha Setting 8

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	Reserved
22:12	WO	xxh	G of HABLRFCA This is an 11-bit positive fixed-point number from 0.0 to 1.0.
11	WO	xxh	Reserved
10:0	WO	xxh	B of HABLRFCA This is an 11-bit positive fixed-point number from 0.0 to 1.0.

HParaType = 01h, Sub-Address = 3Bh
Alpha Setting 9

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	Reserved
22:12	WO	xxh	G of HABLRCB This is an 11-bit positive fixed-point number from 0.0 to 1.0.
11	WO	xxh	Reserved
10:0	WO	xxh	B of HABLRCB This is an 11-bit positive fixed-point number from 0.0 to 1.0.

HParaType = 01h, Sub-Address = 3Ch
Alpha Setting 10

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	Reserved
22:12	WO	xxh	R of HABLRCB This is an 11-bit positive fixed-point number from 0.0 to 1.0.
11	WO	xxh	Reserved
10:0	WO	xxh	R of HABLRCB This is an 11-bit positive fixed-point number from 0.0 to 1.0.

HParaType = 01h, Sub-Address = 3Dh
Alpha Setting 11

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	Reserved
22:12	WO	xxh	G of HABLRCB This is an 11-bit positive fixed-point number from 0.0 to 1.0.
11	WO	xxh	Reserved
10:0	WO	xxh	B of HABLRCB This is an 11-bit positive fixed-point number from 0.0 to 1.0.

HParaType = 01h, Sub-Address = 3Eh
Alpha Setting 12

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	Reserved
22:12	WO	xxh	Constant Register of Aa This is an 11-bit positive fixed-point number from 0.0 to 1.0.
11	WO	xxh	Reserved
10:0	WO	xxh	Constant Register of FAa <HABLRFAa> This is an 11-bit positive fixed-point number from 0.0 to 1.0.

HParaType = 01h, Sub-Address = 3Fh
Alpha Setting 13

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	Reserved
22:12	WO	xxh	Constant Register of Ab <HABLRAb> This is an 11-bit positive fixed-point number from 0.0 to 1.0.
11	WO	xxh	Reserved
10:0	WO	xxh	Constant Register of FAb <HABLRFAb> This is an 11-bit positive fixed-point number from 0.0 to 1.0.

HParaType = 01h, Sub-Address 40-4Fh: Reserved (for Alpha Setting)

HParaType = 01h, Sub-Address = 50h
Destination Setting – Render Target 0 – Setting 1

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Render Target0's Base Address In unit of 256 bytes.

HParaType = 01h, Sub-Address = 51h
Destination Setting – Render Target 0 – Setting 2

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	Memory Mode of Render Target 0 0: Linear mode 1: Tile mode
22	WO	xxh	Render Target0's Tile Is 16-pixel High <HMRT0TileH16> 0: Normal 8-pixel high 1: 16-pixel high
21:20	WO	xxh	Location Setting of Render Target 0 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: Reserved (System Memory) 11: Reserved (Local Memory Local Frame Buffer (L.L.))
19:0	WO	xxh	Reserved

HParaType = 01h, Sub-Address = 52h
Destination Setting – Render Target 0 – Setting 3

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	<p>Render Target0's Format</p> <p>For Bit [23:19]: 00000: Reserved 00001: Reserved 00010: Luminance format 00011: Reserved 00100: Reserved 00101: Reserved 00110: YUV(Video Texture) format 00111-10000: Reserved 10001: ARGB_16bpp format 10010: Reserved 10011: ARGB_32bpp format 10100: Reserved 10101: ABGR_16bpp format 10110: Reserved 10111: ABGR_32bpp format 11000: Reserved 11001: RGBA_16bpp format 11010: Reserved 11011: RGBA_32bpp format 11100: BGRA_16bpp format 11101: BGRA_32bpp format 11110: Floating Color format 11111: Reserved</p> <p><i>If there is NO Alpha channel in the defined format, fill 1.0 as Alpha value.</i></p> <p>For Bit [18:16]: For Luminance Format: 000-100: Reserved 101: AL88 (Bits [15:8] = A, Bits [7:0] = L) 110: L16 (Bits [15:0] = L) For L16 format, post-rendering must be disabled. 111: Reserved</p> <p>For YUV Format (Video Texture): 000: Package mode (Bits [31:24] = V or Cr, Bits [23:16] = Y1, Bits [15:8] = U or Cb, Bits [7:0] = Y0) Others: Reserved</p> <p>For reading color, consider the 8-bit Y as positive 8-bit G, 8-bit U as positive 8-bit R, and 8-bit V as positive 8-bit B. Then extend them to s1.10 according to setting of Color Extending Mode (see bit 15).</p> <p>For writing color, the adjacent 2 pixels are combined into 32 bits and share same 8-bit U and V. Consider an even pixel with R0, G0 & B0 (dithered 8-bit color), and the next odd pixel with R1, G1 & B1 (dithered 8-bit color), the packed result is {(B0 + B1)/2, G1, (R0+R1)/2, G0}. Note the (B0+B1)/2 and (R0+R1)/2 are the result of rounding.</p> <p>For ARGB 16bpp Format: 000: RGB555 (Bits [14:10] = R, Bits [9:5] = G, Bits [4:0] = B) 001: RGB565 (Bits [15:11] = R, Bits [10:5] = G, Bits [4:0] = B) 010: ARGB1555 (Bit [15] = A, Bits [14:10] = R, Bits [9:5] = G, Bits [4:0] = B) 011: ARGB4444 (Bits [15:12] = A, Bits [11:8] = R, Bits [7:4] = G, Bits [3:0] = B) 100: Reserved 101: RGB565 for write color: Bits [15:11] = B, Bits [10:5] = G, Bits [4:0] = R. As for read color: Bits [15:11] = B, Bits [10:6] = G, Bits [4:0] = R 11x: Reserved</p> <p>For ARGB 32bpp Format: 000: ARGB0888 (Bits [23:16] = R, Bits [15:8] = G, Bits [7:0] = B) 001: ARGB8888 (Bits [31:24] = A, Bits [23:16] = R, Bits [15:8] = G, Bits [7:0] = B) 010: ARGB2_10_10_10 (Bits [31:30] = A, Bits [29:20] = R, Bits [19:10] = G, Bits [9:0] = B) 011-1xx: Reserved</p> <p>For ABGR 16bpp Format: 000: BGR555 (Bits [14:10] = B, Bits [9:5] = G, Bits [4:0] = R) 001: BGR565 (Bits [15:11] = B, Bits [10:5] = G, Bits [4:0] = R) 010: ABGR1555 (Bit [15] = A, Bits [14:10] = B, Bits [9:5] = G, Bits [4:0] = R) 011: ABGR4444 (Bits [15:12] = A, Bits [11:8] = B, Bits [7:4] = G, Bits [3:0] = R) 100: Reserved 101: BGR565 for write color, Bits [15:11] = B, Bits [10:5] = G, Bits [4:0] = R.</p>

			<p>As for read color, Bits [15:11] = B, Bits [10:6] = G, Bits [4:0] = R. 11x: Reserved</p> <p><u>For ABGR 32bpp Format:</u> 000: ABGR0888 (Bits [23:16] = B, Bits [15:8] = G, Bits [7:0] = R) 001: ABGR8888 (Bits [31:24] = A, Bits [23:16] = B, Bits [15:8] = G, Bits [7:0] = R) 010: ABGR2_10_10_10 (Bits [31:30] = A, Bits [29:20] = B, Bits [19:10] = G, Bits [9:0] = R) 011: G16R16 (Bits [31:16] = G, Bits [15:0] = R). For G16R16 format, post-rendering must be disabled. 1xx: Reserved</p> <p><u>For RGBA 16bpp Format:</u> 000: RGB555 (Bits [15:11] = R, Bits [10:6] = G, Bits [5:1] = B) 001: RGB565 (Bits [15:11] = R, Bits [10:5] = G, Bits [4:0] = B) A = 1.0 010: RGBA1555 (Bits [15:11] = R, Bits [10:6] = G, Bits [5:1] = B, Bit [0] = A) 011: RGBA4444 (Bits [15:12] = R, Bits [11:8] = G, Bits [7:4] = B, Bits [3:0] = A) 100: Reserved 101: RGB565 for write color, Bits [15:11] = R, Bits [10:5] = G, Bits [4:0] = B. As for read color, Bits [15:11] = R, Bits [10:6] = G, Bits [4:0] = B, A = 1.0. 11x: Reserved</p> <p><u>For RGBA 32bpp Format:</u> 000: RGBA8880 (Bits [31:24] = R, Bits [23:16] = G, Bits [15:8] = B) A = 1.0 001: RGBA8888 (Bits [31:24] = R, Bits [23:16] = G, Bits [15:8] = B, Bits [7:0] = A) 010: RGBA10_10_10_2 (Bits [31:22] = R, Bits [21:12] = G, Bits [11:2] = B, Bits [1:0] = R) 011-1xx: Reserved</p> <p><u>For ABGR 16bpp Format:</u> 000: BGR555 (Bits [15:11] = B, Bits [10:6] = G, Bits [5:1] = R) A = 1.0 001: BGR565 (Bits [15:11] = B, Bits [10:5] = G, Bits [4:0] = R) A = 1.0 010: BGRA1555 (Bits [15:11] = B, Bits [10:6] = G, Bits [5:1] = R, Bit [0] = A) 011: BGRA4444 (Bits [15:12] = B, Bits [11:8] = G, Bits [7:4] = R, Bits [3:0] = A) 100: Reserved 101: BGR565 for write color, Bits [15:11] = B, Bits [10:5] = G, Bits [4:0] = R But for read color, Bits [15:11] = B, Bits [10:6] = G, Bits [4:0] = R A = 1.0 11x: Reserved</p> <p><u>For BGRA 32bpp Format:</u> 000: BGRA8880 (Bits [31:24] = B, Bits [23:16] = G, Bits [15:8] = R) A = 1.0 001: BGRA8888 (Bits [31:24] = B, Bits [23:16] = G, Bits [15:8] = R, Bits [7:0] = R) 010: BGRA10_10_10_2 (Bits [31:22] = B, Bits [21:12] = G, Bits [11:2] = R, Bits [1:0] = R) 011-1xx: Reserved</p> <p><u>For Floating Color Format:</u> 000: R16F (Bits [15:0] = R) 100: G16FR16F (Bits [31:16] = R, Bits [15:0] = G) 101: R32F (Bits [31:0] = R) For floating color format, post-rendering must be disabled</p>
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15	WO	xxh	<p>Color Extending Mode (Excluding Alpha)</p> <p>0: Extending with high color bit Translate to 1.10 format.</p> <p>10 => 11 $C_{11} = C_{10} * (1024/1023) = C_{10} + (1/1023) * C_{10}$ $C_{10} < 1023, \quad C_{11} = 0.\text{xxxxxxxxxx}(C_{10})$ $C_{10} == 1023, \quad C_{11} = 1.0000000000$</p> <p>8 => 11 $C_{11} = C_8 * (1024/255) = 4 * C_8 + (4/255) * C_8$ $C_8 < 64, \quad C_{11} = 0.C_800$ $64 \leq C_8 < 128, \quad C_{11} = 0.C_801$ $128 \leq C_8 < 192, \quad C_{11} = 0.C_810$ $192 \leq C_8 < 255, \quad C_{11} = 0.C_811$ $C_8 == 255, \quad C_{11} = 1.0000000000$</p> <p>6 => 11 $C_{11} = C_6 * (1024/63) = 16 * C_6 + (16/63) * C_6$ $C_6 < 4, \quad C_{11} = 0.C_60000$ $4 \leq C_6 < 8, \quad C_{11} = 0.C_60001$ $8 \leq C_6 < 12, \quad C_{11} = 0.C_60010$ $12 \leq C_6 < 16, \quad C_{11} = 0.C_60011$ $16 \leq C_6 < 20, \quad C_{11} = 0.C_60100$ $20 \leq C_6 < 24, \quad C_{11} = 0.C_60101$ $24 \leq C_6 < 28, \quad C_{11} = 0.C_60110$ $28 \leq C_6 < 32, \quad C_{11} = 0.C_60111$ $32 \leq C_6 < 36, \quad C_{11} = 0.C_61000$ $36 \leq C_6 < 40, \quad C_{11} = 0.C_61001$ $40 \leq C_6 < 44, \quad C_{11} = 0.C_61010$ $44 \leq C_6 < 48, \quad C_{11} = 0.C_61011$ $48 \leq C_6 < 52, \quad C_{11} = 0.C_61100$ $52 \leq C_6 < 56, \quad C_{11} = 0.C_61101$ $56 \leq C_6 < 60, \quad C_{11} = 0.C_61110$ $60 \leq C_6 < 63, \quad C_{11} = 0.C_61111$ $C_6 == 63, \quad C_{11} = 1.0000000000$</p> <p>5 => 11 $C_{11} = C_5 * (1024/31) = 33 * C_5 + (1/31) * C_5 = 32 * C_5 + C_5 + (1/31) * C_5$ $C_5 < 31, \quad C_{11} = 0.C_5C_5$ $C_5 == 31, \quad C_{11} = 1.0000000000$</p> <p>4 => 11 $C_{11} = C_4 * (1024/15) = 68 * C_4 + (4/15) * C_4 = 64 * C_4 + 4 * C_4 + (4/15) * C_4$ $C_4 < 4, \quad C_{11} = C_4C_400$ $4 \leq C_4 < 8, \quad C_{11} = C_4C_401$ $8 \leq C_4 < 12, \quad C_{11} = C_4C_410$ $12 \leq C_4 < 15, \quad C_{11} = C_4C_411$ $C_4 == 15, \quad C_{11} = 1.0000000000$</p> <p>1: Extending with zero Considering 6=>11 as example: C11 = 0. C60000</p>
14:13	WO	xxh	Reserved
12	WO	xxh	<p>Saturation of PS's Output for Render Target "M"</p> <p>0: Clamp PS's output color oCm to related render tager format's range For format ARGB and Luminance: MINVALUE = 0.0, MAXVALUE = 1.0 . For 16-bit floating color format: MINVALUE = 16'hFBFF, MAXVALUE = 16'h7BFF. For 32-bit floating color format: MINVALUE = 32'h7FFFFFFF, MAXVALUE = 32'hFF7FFFFFFF. Clamped Value = min(MAXVALUE, max(oCm, MINVALUE)) Note if oCm is "NAN", clamped value is MINVALUE.</p> <p>1: oCm doesn't clamp</p>
11:10	WO	xxh	Reserved
9:0	WO	xxh	<p>Render Target0's Pitch</p> <p>In unit of 32 bytes for linear mode. In unit of tile (256 bytes or 512 bytes depend on HMRT0TileH16) for tile mode.</p>

HParaType = 01h, Sub-Address = 53h
Destination Setting – Render Target 0 – Setting 4

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	Render Target0's Y Inverse for Dither 0: Not inverse 1: Inverse
22:21	WO	xxh	Render Target0's Y Bias for Dither
20	WO	xxh	Render Target0's X Inverse for Dither 0: Not inverse 1: Inverse
19:18	WO	xxh	Render Target0's X Bias for Dither
17	WO	xxh	Reserved
16:15	WO	xxh	Render Target0's Dither Mode 00: Dither Table with multiplied by (2 ⁿ – 1) 10: Rounding with multiplied by (2 ⁿ – 1) 01: Dither Table without multiplied by (2 ⁿ – 1) 11: Rounding without multiplied by (2 ⁿ – 1)
14:12	WO	xxh	Reserved
11:8	WO	xxh	Render Target0's Raster Operation 0000: BLACK 0 0001: NOT_MERGE_PEN DPon 0010: MASK_NOT_PEN DPna 0011: NOT_COPY_PEN Pn 0100: MASK_PEN_NOT PDna 0101: NOT Dn 0110: XOR_PEN DPx 0111: NOT_MASK_PEN DPan 1000: MASK_PEN DPa 1001: NOT_XOR_PEN DPxn 1010: NOP D 1011: MERGE_NOT_PEN DPno 1100: COPY_PEN P 1101: MERGE_PEN_NOT PDno 1110: MERGE_PEN DPo 1111: WHITE 1
7	WO	xxh	Reserved
6	WO	xxh	DeGamma for Render Target0's Reading Color 0: Disable 1: Enable. Use one-by-one mapping to deGamma the readen color from 2.2 to 1.0 color field before alpha blending operation.
5:4	WO	xxh	Render Target0 is SRGB 00: Gamma 1.0 field. Disable Gamma correction of writing back color. 01: Gamma correction enabled. Use one-by-one mapping to transform the color to gamma 2.2 field before written back to color buffer. 10: Gamme correction enabled. Use Gamma Table "HGTWC" to transform each color channel to a specific color field before written back to color buffer. 11: Reserved
3	WO	xxh	Mask of Render Target0's Alpha Channel 0: The relative data bit will remain the same in Frame Buffer 1: The relative data bit will be updated by a new calculated number
2	WO	xxh	Mask of Render Target0's Red Channel 0: The relative data bit will remain the same in Frame Buffer 1: The relative data bit will be updated by a new calculated number
1	WO	xxh	Mask of Render Target0's Green Channel 0: The relative data bit will remain the same in Frame Buffer 1: The relative data bit will be updated by a new calculated number
0	WO	xxh	Mask of Render Target0's Blue Channel 0: The relative data bit will remain the same in Frame Buffer 1: The relative data bit will be updated by a new calculated number

HParaType = 01h, Sub-Address = 54 – 57h: Reserved (for Destination Setting – Render Target 0)

HParaType = 01h, Sub-Address = 58h
Destination Setting – Render Target 1 – Setting 1

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Render Target1's Base Address In unit of 256 bytes.

HParaType = 01h, Sub-Address = 59h
Destination Setting – Render Target 1 – Setting 2

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	Memory Mode of Render Target 1 0: Linear mode 1: Tile mode
22	WO	xxh	Render Target1's Tile is 16-Pixel high <HMRT1TileH16> 0: Normal 8-pixel high 1: 16-pixel high
21:0	WO	xxh	Reserved

HParaType = 01h, Sub-Address = 5Ah
Destination Setting – Render Target 1 – Setting 3

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	Render Target1's Format <i>The definition is same as Render Target0's Format.</i> <i>Please refer to HParaType 01h, Sub-Address 52h bits [23:16] for details.</i>
15	WO	xxh	Color Extending Mode (Excluding Alpha) 0: Extending with high color bit (Translate to 1.10 format) 1: Extending with zero <i>Please refer to HParaType 01h, Sub-Address 52h bit [15] for details.</i>
14:13	WO	xxh	Reserved
12	WO	xxh	Saturation of PS's Output for Render Target "M" 0: Clamp PS's output color oCm to related render tager format's range For format ARGB and Luminance: MINVALUE = 0.0, MAXVALUE = 1.0 For 16-bit floating color format: MINVALUE = 16'hFBFF, MAXVALUE = 16'h7BFF For 32-bit floating color format: MINVALUE = 32'h7F7FFFFF, MAXVALUE = 32'hFF7FFFFF Clamped Value = min(MAXVALUE, max(oCm, MINVALUE)) Note if oCm is "NAN", clamped value is MINVALUE 1: oCm doesn't clamp
11:10	WO	xxh	Reserved
9:0	WO	xxh	Render Target1's Pitch In unit of 32 bytes for linear mode. In unit of tile (256 bytes or 512 bytes depend on HMRT1TileH16) for tile mode.

HParaType = 01h, Sub-Address = 5Bh
Destination Setting – Render Target 1 – Setting 4

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	Render Target1's Y Inverse for Dither 0: Not inverse 1: Inverse
22:21	WO	xxh	Render Target1's Y Bias for Dither
20	WO	xxh	Render Target1's X Inverse for Dither 0: Not inverse 1: Inverse
19:18	WO	xxh	Render Target1's X Bias for Dither
17	WO	xxh	Reserved
16:15	WO	xxh	Render Target1's Dither Mode 00: Dither Table with multiplied by (2^n - 1) 10: Rounding with multiplied by (2^n - 1) 01: Dither Table without multiplied by (2^n - 1) 11: Rounding without multiplied by (2^n - 1)
14:12	WO	xxh	Reserved

11:8	WO	xxh	Render Target1's Raster Operation 0000: BLACK 0 0001: NOT_MERGE_PEN DPon 0010: MASK_NOT_PEN DPna 0011: NOT_COPY_PEN Pn 0100: MASK_PEN_NOT PDna 0101: NOT Dn 0110: XOR_PEN DPx 0111: NOT_MASK_PEN DPan 1000: MASK_PEN DPa 1001: NOT_XOR_PEN DPxn 1010: NOP D 1011: MERGE_NOT_PEN DPno 1100: COPY_PEN P 1101: MERGE_PEN_NOT PDno 1110: MERGE_PEN DPo 1111: WHITE 1
7	WO	xxh	Reserved
6	WO	xxh	DeGamma for Render Target1's Reading Color 0: Disable 1: Enable. Use one-by-one mapping to deGamma the readen color from 2.2 to 1.0 color field before alpha blending operation.
5:4	WO	xxh	Render Target1 is SRGB 00: Gamma 1.0 field. Disable Gamma correction of writing back color 01: Gamma correction enabled. Use one-by-one mapping to transform the color to gamma 2.2 field before written back to color buffer 10: Gamme correction enabled. Use Gamma Table "HGTWC" to transform each color channel to a specific color field before written back to color buffer 11: Reserved
3	WO	xxh	Mask of Render Target1's Alpha Channel 0: The relative data bit will remain the same in Frame Buffer 1: The relative data bit will be updated by a new calculated number
2	WO	xxh	Mask of Render Target1's Red Channel 0: The relative data bit will remain the same in Frame Buffer 1: The relative data bit will be updated by a new calculated number
1	WO	xxh	Mask of Render Target1's Green Channel 0: The relative data bit will remain the same in Frame Buffer 1: The relative data bit will be updated by a new calculated number
0	WO	xxh	Mask of Render Target1's Blue Channel 0: The relative data bit will remain the same in Frame Buffer 1: The relative data bit will be updated by a new calculated number

HParaType = 01h, Sub-Address = 5C-5Fh: Reserved (for Destination Setting – Render Target 1)

HParaType = 01h, Sub-Address = 60h

Destination Setting – Render Target 2 – Setting 1

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Render Target2's Base Address In unit of 256 bytes.

HParaType = 01h, Sub-Address = 61h

Destination Setting – Render Target 2 – Setting 2

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	Memory Mode of Render Target 2 0: Linear mode 1: Tile mode
22	WO	xxh	Render Target2's Tile is 16-pexel high <HMRT2TileH16> 0: Normal 8-pixel high 1: 16-pixel high
21:0	WO	xxh	Reserved

HParaType = 01h, Sub-Address = 62h
Destination Setting – Render Target 2 – Setting 3

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	Render Target2's Format The definition is same as <i>Render Target0's Format</i> . Please refer to HParaType 01h, Sub-Address 52h bits [23:16] for details.
15	WO	xxh	Color Extending Mode (Excluding Alpha) 0: Extending with high color bit 1: Extending with zero Please refer to HParaType 01h, Sub-Address 52h bit [15] for details.
14:13	WO	xxh	Reserved
12	WO	xxh	Saturation of PS's Output for Render Target "M" 0: Clamp PS's output color oCm to related render tager format's range For format ARGB and Luminance: MINVALUE = 0.0, MAXVALUE = 1.0 For 16-bit floating color format: MINVALUE = 16'hFBFF, MAXVALUE = 16'h7BFF For 32-bit floating color format: MINVALUE = 32'h7FFFFFFF, MAXVALUE = 32'hFF7FFFFFFF Clamped Value = min(MAXVALUE, max(oCm, MINVALUE)) Note if oCm is "NAN", clamped value is MINVALUE 1: oCm doesn't clamp
11:10	WO	xxh	Reserved
9:0	WO	xxh	Render Target2's Pitch In unit of 32 bytes for linear mode. In unit of tile (256 bytes or 512 byte depend on HMRT2TileH16) for tile mode.

HParaType = 01h, Sub-Address = 63h
Destination Setting – Render Target 2 – Setting 4

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	Render Target2's Y Inverse for Dither 0: Not inverse 1: Inverse
22:21	WO	xxh	Render Target2's Y Bias for Dither
20	WO	xxh	Render Target2's X Inverse for Dither 0: Not inverse 1: Inverse
19:18	WO	xxh	Render Target2's X Bias for Dither
17	WO	xxh	Reserved
16:15	WO	xxh	Render Target2's Dither Mode 00: Dither Table with multiplied by (2^n - 1) 10: Rounding with multiplied by (2^n - 1) 01: Dither Table without multiplied by (2^n - 1) 11: Rounding without multiplied by (2^n - 1)
14:12	WO	xxh	Reserved
11:8	WO	xxh	Render Target2's Raster Operation 0000: BLACK 0 0001: NOT_MERGE_PEN DPon 0010: MASK_NOT_PEN DPna 0011: NOT_COPY_PEN Pn 0100: MASK_PEN_NOT PDna 0101: NOT Dn 0110: XOR_PEN DPx 0111: NOT_MASK_PEN DPan 1000: MASK_PEN DPa 1001: NOT_XOR_PEN DPxn 1010: NOP D 1011: MERGE_NOT_PEN DPno 1100: COPY_PEN P 1101: MERGE_PEN_NOT PDno 1110: MERGE_PEN DPo 1111: WHITE 1
7	WO	xxh	Reserved
6	WO	xxh	DeGamma for Render Target2's Reading Color 0: Disable 1: Enable. Use one-by-one mapping to deGamma the readen color from 2.2 to 1.0 color field before alpha blending operation.

5:4	WO	xxh	Render Target2 is SRGB 00: Gamma 1.0 field. Disable Gamma correction of writing back color 01: Gamma correction enabled. Use one-by-one mapping to transform the color to gamma 2.2 field before written back to color buffer 10: Gamme correction enabled. Use Gamma Table "HGTWC" to transform each color channel to a specific color field before written back to color buffer 11: Reserved
3	WO	xxh	Mask of Render Target2's Alpha Channel 0: The relative data bit will remain the same in Frame Buffer 1: The relative data bit will be updated by a new calculated number
2	WO	xxh	Mask of Render Target2's Red Channel 0: The relative data bit will remain the same in Frame Buffer 1: The relative data bit will be updated by a new calculated number
1	WO	xxh	Mask of Render Target2's Green Channel 0: The relative data bit will remain the same in Frame Buffer 1: The relative data bit will be updated by a new calculated number
0	WO	xxh	Mask of Render Target2's Blue Channel 0: The relative data bit will remain the same in Frame Buffer 1: The relative data bit will be updated by a new calculated number

HPParaType = 01h, Sub-Address = 64-67h: Reserved (for Destination Setting – Render Target 2)

HPParaType = 01h, Sub-Address = 68h

Destination Setting – Render Target 3 – Setting 1

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Render Target3's Base Address In unit of 256 bytes.

HPParaType = 01h, Sub-Address = 69h

Destination Setting – Render Target 3 – Setting 2

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	Memory Mode of Render Target 3 0: Linear mode 1: Tile mode
22	WO	xxh	Render Target3's Tile is 16-pixel high <HMRT3TileH16> 0: Normal 8-pixel high 1: 16-pixel high
21:0	WO	xxh	Reserved

HPParaType = 01h, Sub-Address = 6Ah

Destination Setting – Render Target 3 – Setting 3

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	Render Target3's Format <i>The definition is same as Render Target0's Format.</i> <i>Please refer to HPParaType 01h, Sub-Address 52h bits [23:16] for details.</i>
15	WO	xxh	Color Extending Mode (Excluding Alpha) 0: Extending with high color bit 1: Extending with zero <i>Please refer to HPParaType 01h, Sub-Address 52h bit [15] for details.</i>
14:13	WO	xxh	Reserved
12	WO	xxh	Saturation of PS's Output for Render Target "M" 0: Clamp PS's output color oCm to related render tager format's range. For format ARGB and Luminance: MINVALUE = 0.0, MAXVALUE = 1.0 For 16-bit floating color format: MINVALUE = 16'hFBFF, MAXVALUE = 16'h7BFF For 32-bit floating color format: MINVALUE = 32'h7F7FFFFF, MAXVALUE = 32'hFF7FFFFF Clamped Value = min(MAXVALUE, max(oCm, MINVALUE)) Note if oCm is "NAN", clamped value is MINVALUE 1: oCm doesn't clamp
11:10	WO	xxh	Reserved

9:0	WO	xxh	Render Target3's Pitch In unit of 32 bytes for linear mode. In unit of tile (256 bytes or 512 bytes depend on HMRT3TileH16) for tile mode.
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HPParaType = 01h, Sub-Address = 6Bh
Destination Setting – Render Target 3 – Setting 4

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	Render Target3's Y Inverse for Dither 0: Not inverse 1: Inverse
22:21	WO	xxh	Render Target3's Y Bias for Dither
20	WO	xxh	Render Target3's X Inverse for Dither 0: Not inverse 1: Inverse
19:18	WO	xxh	Render Target3's X Bias for Dither
17	WO	xxh	Reserved
16:15	WO	xxh	Render Target3's Dither Mode 00: Dither Table with multiplied by (2^n - 1) 10: Rounding with multiplied by (2^n - 1) 01: Dither Table without multiplied by (2^n - 1) 11: Rounding without multiplied by (2^n - 1)
14:12	WO	xxh	Reserved
11:8	WO	xxh	Render Target3's Raster Operation 0000: BLACK 0001: NOT_MERGE_PEN DPon 0010: MASK_NOT_PEN DPna 0011: NOT_COPY_PEN Pn 0100: MASK_PEN_NOT PDna 0101: NOT Dn 0110: XOR_PEN DPx 0111: NOT_MASK_PEN DPan 1000: MASK_PEN DPa 1001: NOT_XOR_PEN DPxn 1010: NOP D 1011: MERGE_NOT_PEN DPno 1100: COPY_PEN P 1101: MERGE_PEN_NOT PDno 1110: MERGE_PEN DPo 1111: WHITE 1
7	WO	xxh	Reserved
6	WO	xxh	DeGamma for Render Target3's Reading Color 0: Disable 1: Enable. Use one-by-one mapping to deGamma the readen color from 2.2 to 1.0 color field before alpha blending operation.
5:4	WO	xxh	Render Target3 is SRGB 00: Gamma 1.0 field. Disable Gamma correction of writing back color 01: Gamma correction enabled. Use one-by-one mapping to transform the color to gamma 2.2 field before written back to color buffer 10: Gamme correction enabled. Use Gamma Table "HGTWC" to transform each color channel to a specific color field before written back to color buffer 11: Reserved
3	WO	xxh	Mask of Render Target3's Alpha Channel 0: The relative data bit will remain the same in Frame Buffer 1: The relative data bit will be updated by a new calculated number
2	WO	xxh	Mask of Render Target3's Red Channel 0: The relative data bit will remain the same in Frame Buffer 1: The relative data bit will be updated by a new calculated number
1	WO	xxh	Mask of Render Target3's Green Channel 0: The relative data bit will remain the same in Frame Buffer 1: The relative data bit will be updated by a new calculated number
0	WO	xxh	Mask of Render Target3's Blue Channel 0: The relative data bit will remain the same in Frame Buffer 1: The relative data bit will be updated by a new calculated number

HPParaType = 01h, Sub-Address = 6C-6Fh: Reserved (for Destination Setting – Render Target 3)

HParaType = 01h, Sub-Address = 70h
Fog Setting 1

Bits [23:0]	Attribute	Default	Description
23:8	WO	xxh	Reserved
7	WO	xxh	Fog Factor Sourec From PS 0: Fog factor is generated in PE (Including vertex, linear or exponential Fog) 1: Fog factor and Fog operation is dealt by the PS Instead of 8-bit fixed Fog factor, PE sends "Fog coordinate" with format floating s[7].10 to PS. <i>Note: When this bit is set, HenFOGRT0, HenFOGRT1, HenFOGMRT2 and HenFOGMRT3 should be disabled.</i>
6	WO	xxh	Linear Fog Calculation Factor Setting 2 <HFogLF2> 0: Use W or Z to calculate linear Fog by setting of bit 4 1: Use attributre "Fog" as fog coordinate to calculate linear Fog If (HFogLF2 == 1) // this bit Use Fog attribute to calculate linear fog or exponential fog (fog per pixel) Else if (HFogLF == 0) // bit 4 Use Z attribute to calculate linear fog or exponential fog (fog per pixel) Else Use W attribute to calculate linear fog or exponential fog (fog per pixel)
5	WO	xxh	Fog Factor from Spectra Color's Alpha 0: Individual Fog attribute 1: Use Spectral (Color 2) Alpha as Fog factor
4	WO	xxh	Linear Fog Calculation Factor Setting <HFogLF> 0: Use W to calculate linear Fog 1: Use Z to calculate linear Fog
3	WO	xxh	Fog Equation 0: Use Fog equation 0: $C_{out} = f * (C_{in} + C_{sepc}) + (1-f) * HC_{Fog}$ 1: Use Fog equation 1: $C_{out} = (1-f) * (C_{in} + C_{spec}) + f * HC_{Fog}$
2:0	WO	xxh	Fog Mode When substituting for vertex Z, Z is calculated in PS (HZSrcPS = 1), linear or non-linear Fog from Z is not allowed. 000: Local Fog 001: Reserved (Global Fog) 010: Linear Fog 011: Reserved 100: Exponential Fog 101: Exponential_2 Fog 11x: Reserved <i>Note: Setting of 1xx: is for Non-linear Fog (Use Fog Table).</i>

HParaType = 01h, Sub-Address = 71h
Fog Setting 2

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	Reserved
22:12	WO	xxh	G of HCFogCL Positive fixed-point from 0 to 1.0
11	WO	xxh	Reserved
10:0	WO	xxh	G of HCFogCL Positive fixed-point from 0 to 1.0

HParaType = 01h, Sub-Address = 72h
Fog Setting 3

Bits [23:0]	Attribute	Default	Description
23:11	WO	xxh	Reserved
10:0	WO	xxh	R of Fog Color Positive fixed-point from 0 to 1.0

HParaType = 01h, Sub-Address = 73h
Fog Setting 4

Bits [23:0]	Attribute	Default	Description
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23:15	WO	xxh	Reserved
14:0	WO	xxh	Fog Start Floating-point is used to calculate Fog factor. The format is floating-point [8].7.

HParaType = 01h, Sub-Address = 74h
Fog Setting 5

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Reserved

HParaType = 01h, Sub-Address = 75h
Fog Setting 6

Bits [23:0]	Attribute	Default	Description
23:4	WO	xxh	Reserved
3:0	WO	xxh	Mantissa Part of the One Over (Fog End - Fog Start) <HFogOOdMF> Note: The leading one is not included.

HParaType = 01h, Sub-Address = 76h
Fog Setting 7

Bits [23:0]	Attribute	Default	Description
23:8	WO	xxh	Reserved
7:0	WO	xxh	Exponential Part of the One Over (Fog End - Fog Start) <HFogOOdEF> Format is IEEE's floating presentation. The value of $1/(\text{Fog End} - \text{Fog Start})$ is $(1.\text{HfogOOdMF}[1:0] * 2^{(\text{HfogOOdEF} - 127)})$.

HParaType = 01h, Sub-Address = 77h
Fog Setting 8

Bits [23:0]	Attribute	Default	Description
23:15	WO	xxh	Reserved
14:0	WO	xxh	Lower 3 Bytes of Fog End <HFogEnd> The format of HFogEnd is floating-point [8].7.

HParaType = 01h, Sub-Address = 78h
Fog Setting 9

Bits [23:0]	Attribute	Default	Description
23:21	WO	xxh	Reserved
20:8	WO	xxh	Fog Density with Positive Floating Format [8].5.
7:0	WO	xxh	Reserved

HParaType = 01h, Sub-Address = 79-7Fh: Reserved (for Fog Setting)

HParaType = 01h, Sub-Address = 80h
Miscellaneous Setting 1

Bits [23:0]	Attribute	Default	Description
23:12	WO	xxh	Color Window Top Clipping Value in the Range of 0 to 2048
11:0	WO	xxh	Color Window Bottom Clipping Value in the Range of 0 to 2048

HParaType = 01h, Sub-Address = 81h
Miscellaneous Setting 2

Bits [23:0]	Attribute	Default	Description
23:12	WO	xxh	Color Window Left Clipping Value in the Range of 0 to 2048
11:0	WO	xxh	Color Window RightClipping Value in the Range of 0 to 2048

HParaType = 01h, Sub-Address = 82h
Miscellaneous Setting 3

Bits [23:0]	Attribute	Default	Description
23:12	WO	xxh	Scissor Window Top Clipping Value in the Range of 0 to 2048
11:0	WO	xxh	Scissor Window Bottom Clipping Value in the Range of 0 to 2048

HParaType = 01h, Sub-Address = 83h
Miscellaneous Setting 4

Bits [23:0]	Attribute	Default	Description
23:12	WO	xxh	Scissor Window Left Clipping Value in the Range of 0 to 2048
11:0	WO	xxh	Scissor Window Right Clipping Value in the Range of 0 to 2048

HParaType = 01h, Sub-Address = 84h
Miscellaneous Setting 5

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	Reserved
15:0	WO	xxh	Line Pattern The Line Pattern bit starts from the LSB.

HParaType = 01h, Sub-Address = 85h
Miscellaneous Setting 6

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	Line Pattern Reset Hardware would reset related repeat counter automatically whenever this register is set to "1". It is NOT necessary for driver to clear this bit. Hardware would clear it after the counter reset.
22:16	WO	xxh	Reserved
15:0	WO	xxh	Line Pattern Repeat Factor This number denotes how many times that a line pattern bit will be used for several line pixels.

HParaType = 01h, Sub-Address = 86h
Miscellaneous Setting 7 - Lower 3 Bytes of Solid Shading Color <HSolidCL>

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	R of Solid Shading Color
15:8	WO	xxh	G of Solid Shading Color
7:0	WO	xxh	B of Solid Shading Color

HParaType = 01h, Sub-Address = 87h
Miscellaneous Setting 8 - Highest Byte of Solid Shading Color <HSolidCH>

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	Reserved
22:8	WO	xxh	Reserved
7:0	WO	xxh	Alpha of Solid Shading Color

HParaType = 01h, Sub-Address = 88h
Miscellaneous Setting 9

Bits [23:0]	Attribute	Default	Description
23:13	WO	xxh	Reserved
12:0	WO	xxh	Guard Band Window Left Clipping Value Format as s12 2's complement

HParaType = 01h, Sub-Address = 89h
Miscellaneous Setting 10

Bits [23:0]	Attribute	Default	Description
23:13	WO	xxh	Reserved
12:0	WO	xxh	Guard Band Window Right Clipping Value Format as s12 2's complement

HParaType = 01h, Sub-Address = 8Ah
Miscellaneous Setting 11

Bits [23:0]	Attribute	Default	Description
22:18	WO	xxh	Reserved
17	WO	xxh	TS ZTAG Deadlock ECO Enable Signal 0: Disable (default) 1: Enable
16	WO	xxh	Zero Round Mode for the Texture Coordinate from PE to PS 0: Round to zero 1: Round to 0 ⁺
15:4	WO	xxh	Bottom Y Value for PS's Location Register <HYB4LocationReg> As 12 positive integer
3	WO	xxh	Enable HYB4LocationReg HYB4LocationReg is defined in bits [15:4]. 0: Disable 1: Enable If (HPSLocationReg == true) If (HenYB4LocationReg == true) // T01A90[19] LocationReg.Y = floating(HYB4LocationReg – PEY) Else LocationReg.Y = floating(PEY)
2	WO	xxh	PreModulate Color 0 (Diffuse Color) with Ws 0: Not pre-modulated; multiply C0 and Ws in SE 1: Pre-modulated; don't multiply C0 and Ws in WS
1	WO	xxh	PreModulate Color 1 (Specula Color) with Ws 0: Not pre-modulated; multiply C1 and Ws in SE 1: Pre-modulated; don't multiply C1 and Ws in WS
0	WO	xxh	PreModulate Fog with Ws 0: Not pre-modulated; multiply Fog and Ws in SE 1: Pre-modulated; don't multiply Fog and Ws in WS

HParaType = 01h, Sub-Address = 8B-8Fh: Reserved (for Miscellaneous Setting)

HParaType = 01h, Sub-Address = 90h-9Ah: Reserved

HParaType = 01h, Sub-Address = AAh
Software Inspection

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	Reserved
15:0	WO	xxh	Flag Number for Software Inspection

HParaType 02h: Attribute of Texture Stage N (HParaSubType: 00-0Fh)

The register table in this section is used for following HParaSubTypes (from 00h to 0Fh).

- HParaSubType = 0000 0000 (00h) -- For Texture 0
- HParaSubType = 0000 0001 (01h) -- For Texture 1
- HParaSubType = 0000 0010 (02h) -- For Texture 2
- HParaSubType = 0000 0011 (03h) -- For Texture 3
- HParaSubType = 0000 0100 (04h) -- For Texture 4
- HParaSubType = 0000 0101 (05h) -- For Texture 5
- HParaSubType = 0000 0110 (06h) -- For Texture 6
- HParaSubType = 0000 0111 (07h) -- For Texture 7
- HParaSubType = 0000 1000 (08h) -- For Texture 8
- HParaSubType = 0000 1001 (09h) -- For Texture 9
- HParaSubType = 0000 1010 (0Ah) -- For Texture A
- HParaSubType = 0000 1011 (0Bh) -- For Texture B
- HParaSubType = 0000 1100 (0Ch) -- For Texture C
- HParaSubType = 0000 1101 (0Dh) -- For Texture D
- HParaSubType = 0000 1110 (0Eh) -- For Texture E
- HParaSubType = 0000 1111 (0Fh) -- For Texture F

Sub-Address (Bits [31:24]): 00-51h

HParaType = 02h (HParaSubType = 00h-0Fh), Sub-Address = 00h

Face 0 Level 0 Base Address

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Face 0's Level 0 Base Address This is A31 to A8 in unit of 256 bytes.

HParaType = 02h (HParaSubType = 00h-0Fh), Sub-Address = 01h

Face 1 Level 0 Base Address

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Face 1's Level 0 Base Address This is A31 to A8 in unit of 256 bytes.

HParaType = 02h (HParaSubType = 00h-0Fh), Sub-Address = 02h

Face 2 Level 0 Base Address

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Face 2's Level 0 Base Address This is A31 to A8 in unit of 256 bytes. Program it back to 0.

HParaType = 02h (HParaSubType = 00h-0Fh), Sub-Address = 03h
Face 3 Level 0 Base Address

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Face 3's Level 0 Base Address This is A31 to A8 in unit of 256 bytes.

HParaType = 02h (HParaSubType = 00h-0Fh), Sub-Address = 04h
Face 4 Level 0 Base Address

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Face 4's Level 0 Base Address This is A31 to A8 in unit of 256 bytes.

HParaType = 02h (HParaSubType = 00h-0Fh), Sub-Address = 05h
Face 5 Level 0 Base Address

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Face 5's Level 0 Base Address in unit of 256 bytes This is A31 to A8.

Note: HTXSnLmBasOffset is defined in a palette with HParaType 03h and HsubParaType 10h.

HParaType = 02h (HParaSubType = 00h-0Fh), Sub-Address = 06-17h: Reserved

HParaType = 02h (HParaSubType = 00h-0Fh), Sub-Address = 18h
Texture Control 1

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	Force Miss for Texture n's Texture Cache Hit Detection 0: Detect hit or miss normally 1: Always force to miss
22:18	WO	xxh	Reserved
17:16	WO	xxh	Texture Location of Face5 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: Reserved (System Memory) 11: Reserved (Local Memory Local Frame Buffer (L.L.))
15:14	WO	xxh	Texture Location of Face5 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: Reserved (System Memory) 11: Reserved (Local Memory Local Frame Buffer (L.L.))
13	WO	xxh	Reserved
12	WO	xxh	Base Address Mode for Texture Sample N 0: HTXSnLmOffset is not offset related to Level 0, but an independent Base Address of Level m. Base Address of Level m = HTXSnLmOffset. 1: This mode is for cubic texture and planner mode texture Base Address of Level m = HTXSnFfLOBas + HTXSnLmOffset
11:8	WO	xxh	Mode of Texture N 0000: Reserved 0001: 2 Dimension, both S and T coordinates. 0010: 3 Dimension volume texture. S, T, R coordinates. 0011: Cube texture 1xxx: Projection texture Others: Reserved
7:6	WO	xxh	Texture Location of Face0 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: Reserved (System Memory) 11: Reserved (Local Memory Local Frame Buffer (L.L.))
5:4	WO	xxh	Texture Location of Face2 or Cr Buffer for Y-Cb-Cr Format 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: Reserved (System Memory) 11: Reserved (Local Memory Local Frame Buffer (L.L.))
3:2	WO	xxh	Texture Location of Face1, Cb Buffer for Y-Cb-Cr Format, or Crb Buffer for Y-Crb Format 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: Reserved (System Memory) 11: Reserved (Local Memory Local Frame Buffer (L.L.))
1:0	WO	xxh	Texture Location of Face0 or Y Buffer for Y-Cb-Cr or Y-Crb Format 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: Reserved (System Memory) 11: Reserved (Local Memory Local Frame Buffer (L.L.))

Note:

The procedure to determine the location of accessed texture:

Consider fetch the texture with level "l" of texture stage "n"'s face "f"

If (HTXnBaseMode == 1 | HTXnPower2 == 1) { // with offset mode for the base address

LOC = HTXnFfLOC

} else { // with base mode for the base address

If ("l" == 0) {

LOC = HTXnF0LOC

} else if ("l" <= 7) {

LOC = HTXnLlLOC

} else { // "l" == 8,9,10 or 11

LOC = HTXnL8LOC

}

}

HPParaType = 02h (HPParaSubType = 00h-0Fh), Sub-Address = 19-1Fh: Reserved (Texture Control)

HPParaType = 02h (HPParaSubType = 00h-0Fh), Sub-Address = 20h

Texture Control 2

Bits [23:0]	Attribute	Default	Description
23:12	WO	xxh	Height of Texture Level 0 The height of each level is calculated from HTXSnLOH Height at Level "l" = HTXSnLOH >> l. Maximum is 2048.
11:0	WO	xxh	Width of Texture Level 0 The Width of each level is calculated from HTXSnLOW Width at Level "l" = HTXSnLOW >> l. Maximum is 2048.

HPParaType = 02h (HPParaSubType = 00h-0Fh), Sub-Address = 21h

Texture Control 3

Bits [23:0]	Attribute	Default	Description
23:12	WO	xxh	Reserved
11:0	WO	xxh	Length of Texture Level 0, Maximum to 2048 (for 3D Volume Texture's R Axis) The Length of each level is calculated from HTXSnL0L Length at Level "l" = HTXSnL0L >> l, but NO MIP for 3D volume texture.

HPParaType = 02h (HPParaSubType = 00h-0Fh), Sub-Address = 22h

Texture Control 4

Bits [23:0]	Attribute	Default	Description
23:18	WO	xxh	Reserved
17	WO	xxh	Memory Mode of Texture N 0: Linear mode 1: Tile mode
16	WO	xxh	Texture N's Tile Is 16-texel High 0: Normal 8-texel high 1: 16-texel high
15	WO	xxh	Texture N's Width and Height Are Both Power of 2 0: Non-power of 2 texture 1: Power of 2 texture
14:12	WO	xxh	Reserved
11:8	WO	xxh	Exponential of Length of Texture N Level 0 Maximum is up to 11(2 ¹¹).
7:4	WO	xxh	Exponential of Height of Texture N Level 0 Maximum is up to 11(2 ¹¹).
3:0	WO	xxh	Exponential of Width of Texture N Level 0 Maximum is up to 11(2 ¹¹).

HPParaType = 02h (HPParaSubType = 00h-0Fh), Sub-Address = 23-2Fh: Reserved (Texture Control)

HPParaType = 02h (HPParaSubType = 00h-0Fh), Sub-Address = 30h
Texture Control 5

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	<p>Texture Format</p> <p>Bit [23:19]:</p> <ul style="list-style-type: none"> 00000: Reserved 00001: Intensity format R, G, B <= I A <= 1.0 00010: Luminance format R, G, B <= L A <= 1.0 or A 00011: Alpha format R, G, B <= 0.0 A <= A 00100: Reserved 00101: Compressed feature 00110: YUV (Video texture) format 00111: Format for BumpMapping 11111-01000: Reserved 10000: Reserved 10001: ARGB_16bpp format 10010: Reserved 10011: ARGB_32bpp format 10100: Reserved 10101: ABGR_16bpp format 10110: Reserved 10111: ABGR_32bpp format 11000: Reserved 11001: RGBA_16bpp format 11010: Reserved 11011: RGBA_32bpp format 11100: BGRA_16bpp format 11101: BGRA_32bpp format 11110: Floating Color format 11111: Scale (Said Z format or only one component) <p><i>If there is NO Alpha channel in the defined format, fill 1.0 as Alpha value.</i></p> <p>Bit [18:16]:</p> <p><u>For Intensity Format:</u></p> <ul style="list-style-type: none"> 000: Reserved 001: Reserved 010: T4 (Bits [3:0] = T) 011: T8 (Bits [7:0] = T) 1xx: Reserved <p><u>For Luminance Format:</u></p> <ul style="list-style-type: none"> 000: Reserved 001: Reserved 010: L4 (Bits [3:0] = L) 011: L8 (Bits [7:0] = L) 100: AL44 (Bits [7:4] = A, Bits [3:0] = L) 101: AL88 (Bits [15:8] = A, Bits [7:0] = L) 110: L16 (Bits [15:0] = L) <p><u>For L16 Format:</u></p> <ul style="list-style-type: none"> A = 1.0f R = G = B = float (L/65536) // if (L = FFFFh) R = G = B = 1.0 // else fill "0" into mantissa 111: Reserved <p><u>For Alpha Format:</u></p> <ul style="list-style-type: none"> 000: Reserved 001: Reserved 010: A4 (Bits [3:0] = A) 011: A8 (Bits [7:0] = A) R = G = B = 0.0 1xx: Reserved

For Compressed Format:

000: Reserved
 001: DXT1, 16-bpp format
 010: DXT2, DXT3, 4-bit Alpha format
 011: DXT4, DXT5, 3-bit Alpha format
 100-101: Reserved
 The G8R8_G8B8 can be defined by set as YUV format's package mode and set HTXnYUV2RGBmode to RGB mode

For YUV format (Video Texture):

000: Package mode (Bits [31:24] = V or Cr, Bits [23:16] = Y1, Bits [15:8] = U or Cb, Bits [7:0] = Y0) A = 1.0
 001: AYUV (Bits [31:24] = A, Bits [23:16] = Y, Bits [15:8] = U, Bits [7:0] = V)
 010: IA44 (Bits [7:4] = I as a 16 entries index to get a Y(R)8U(G)8V(B)8 texel, Bits [3:0] = A. A does not come from palette)
 011: AI44 (Bits [7:4] = A. A does not come from palette, Bits [3:0] = I as a 16 entries index to get a Y(R)8U(G)8V(B)8 texel)
 100-101: Reserved
 111: V410 mode (Bits [31:22] = V or Cr, Bits [21:12] = Y, Bits [11:2] = U or Cb) A = 1.0

For BumpMapping Format (Reserved):

000: VU88 (Bits [15:8] = dV, Bits [7:0] = dU)
 001: LVU655 (Bits [15:10] = L, Bits [9:5] = dV, Bits [4:0] = dU)
 010: LVU888 (Bits [23:16] = L, Bits [15:8] = dV, Bits [7:0] = dU)
 011: QWUV8888 (Bits [31:24] = dQ, Bits [23:16] = dW, Bits [15:8] = dV, Bits [7:0] = dU)
 100: VU16 (Bits [31:16] = dV, Bits [15:0] = dU)
 101: AWVU2_10_10_10 (Bits [31:30] = A, Bits [29:20] = dW, Bits [19:10] = dV, Bits [9:0] = dU)
 110: CVUx88 Reserved
 111: Reserved

For ARGB 16bpp Format:

000: RGB555 (Bits [14:10] = R, Bits [9:5] = G, Bits [4:0] = B)
 001: RGB565 (Bits [15:11] = R, Bits [10:5] = G, Bits [4:0] = B) A = 1.0
 010: ARGB1555 (Bit [15] = A, Bits [14:10] = R, Bits [9:5] = G, Bits [4:0] = B)
 011: ARGB4444 (Bits [15:12] = A, Bits [11:8] = R, Bits [7:4] = G, Bits [3:0] = B)
 100: Reserved
 101: RGB565 for write color, Bits [15:11] = R, Bits [10:5] = G, Bits [4:0] = B
 But for read color, Bits [15:11] = R, Bits [10:6] = G, Bits [4:0] = B, A = 1.0
 11x: Reserved

For ARGB 32bpp Format:

000: ARGB0888 (Bits [23:16] = R, Bits [15:8] = G, Bits [7:0] = B)
 001: ARGB8888 (Bits [31:24] = A, Bits [23:16] = R, Bits [15:8] = G, Bits [7:0] = B) A = 1.0
 010: ARGB2_10_10_10 (Bits [31:30] = A, Bits [29:20] = R, Bits [19:10] = G, Bits [9:0] = B)
 011-111: Reserved

For ABGR 16bpp Format:

000: BGR555 (Bits [14:10] = B, Bits [9:5] = G, Bits [4:0] = R)
 001: BGR565 (Bits [15:11] = B, Bits [10:5] = G, Bits [4:0] = R) A = 1.0
 010: ABGR1555 (Bits [15] = A, Bit [14:10] = B, Bits [9:5] = G, Bits [4:0] = R)
 011: ABGR4444 (Bits [15:12] = A, Bits [11:8] = B, Bits [7:4] = G, Bits [3:0] = R)
 100: Reserved
 101: BGR565 for write color: Bits [15:11] = B, Bits [10:5] = G, Bits [4:0] = R.
 But for read color: Bits [15:11] = B, Bits [10:6] = G, Bits [4:0] = R, A = 1.0
 11x: Reserved

For ABGR 32bpp Format:

000: ABGR0888 (Bits [23:16] = B, Bits [15:8] = G, Bits [7:0] = R) A = 1.0.
 001: ABGR8888 (Bit [31:24] = A, Bits [23:16] = B, Bits [15:8] = G, Bits [7:0] = R)
 010: ABGR2_10_10_10 (Bits [31:30] = A, Bits [29:20] = B, Bits [19:10] = G, Bits [9:0] = R)
 011: G16R16 (Bits [31:16] = G, Bits [15:0] = R) for this format, A = B = 1.0f, G and R are transformed to s[7].16
 1xx: Reserved

For RGBA 16bpp Format:

000: RGB555 (Bits [15:11] = R, Bits [10:6] = G, Bits [5:1] = B)
 001: RGB565 (Bits [15:11] = R, Bits [10:5] = G, Bits [4:0] = B) A = 1.0
 010: RGBA1555 (Bits [15:11] = R, Bits [10:6] = G, Bits [5:1] = B, Bit [0] = A)
 011: RGBA4444 (Bits [15:12] = R, Bits [11:8] = G, Bits [7:4] = B, Bits [3:0] = A)
 100: Reserved
 101: RGB565 for write color: Bits [15:11] = R, Bits [10:5] = G, Bits [4:0] = B
 But for read color: Bits [15:11] = R, Bits [10:6] = G, Bits [4:0] = B, A = 1.0
 11x: Reserved

For RGBA 32bpp Format:

			<p>000: RGBA8880 (Bits [31:24] = R, Bits [23:16] = G, Bits [15:8] = B) A = 1.0 001: RGBA8888 (Bits [31:24] = R, Bits [23:16] = G, Bits [15:8] = B, Bits [7:0] = A) 010: RGBA10_10_10_2 (Bits [31:22] = R, Bits [21:12] = G, Bits [11:2] = B, Bits [1:0] = R) 011-111: Reserved</p> <p><u>For ABGR 16bpp Format:</u> 000: BGR555 (Bits [15:11] = B, Bits [10:6] = G, Bits [5:1] = R) A = 1.0 001: BGR565 (Bits [15:11] = B, Bits [10:5] = G, Bits [4:0] = R) A = 1.0 010: BGRA1555 (Bits [15:11] = B, Bits [10:6] = G, Bits [5:1] = R, Bit [0] = A) 011: BGRA4444 (Bits [15:12] = B, Bits [11:8] = G, Bits [7:4] = R, Bits [3:0] = A) 100: Reserved 101: BGR565 for write color: Bits [15:11] = B, Bits [10:5] = G, Bits [4:0] = R. But for read color: Bits [15:11] = B, Bits [10:6] = G, Bits [4:0] = R, A = 1.0 11x: Reserved</p> <p><u>For BGRA 32bpp Format:</u> 000: BGRA8880 (Bits [31:24] = B, Bits [23:16] = G, Bits [15:8] = R), A = 1.0 001: BGRA8888 (Bits [31:24] = B, Bits [23:16] = G, Bits [15:8] = R, Bits [7:0] = R) 010: BGRA10_10_10_2 (Bits [31:22] = B, Bits [21:12] = G, Bits [11:2] = R, Bits [1:0] = R) 011-11: Reserved</p> <p><u>For Floating Color Format (Filter not supported):</u> 000: R16F (Bits [15:0] = R) s[5].10 A = G = B = 1.0f, and R is extended to s[7].16 with "0". 100: G16FR16F (Bits [31:16] = G, Bits [15:0] = R) s[5].10 A = B = 1.0f, R and G are extended to s[7].16 with "0" 101: R32F (Bits [31:0] = R) s[8].23 A = G = B = 1.0f, and R is clamped to s[7].16(saturation) 111: Reserved</p> <p><u>For Z Format:</u> 000: 16-bit fixed-point format, $0.0 \leq Z < 1.0$ 001: 16-bit floating format s[5].10 from $+2^{63} * 1.FFFF$ to $-2^{63} * 1.FFFF$. <*Only Nearest> 010-011: Reserved 100: 32-bit fixed-point format, $0.0 \leq Z < 1.0$. <*Only Nearest> 101: 32-bit floating format s[8].23. <*Only Nearest> 110: 24-bit fixed-point format Z, $0.0 \leq Z < 1.0$, and Stencil. <*Only Nearest> Z is located in D[31:8], Stencil is located in D[7:0] 111: Reserved</p>
15	WO	xxh	<p>Texture Color Extending Mode (Excluding Alpha) For Alpha channel, always extend it with high color bit. For YUV format (video texture) and when HTXnYUV2RGBmode set as 0, always extend it with zero. 0: Extending with high color bit 1: Extending with zero</p>
14	WO	xxh	<p>Inverse the Texel Order in One Byte for Those Texture with 1bpp, 2bpp or 3bpp 0: Normal Consider Index 1: Bit [7] for tex[8n+7], bit [6] for tex[8n+6].....bit [0] for tex[8n] Consider Index 2: Bits [7:6] for tex[4n+3], bits [5:4] for tex[4n+2].....bits [1:0] for tex[4n] Consider Index 4: Bits [7:4] for tex[2n+1], bits [3:0] for tex[2n] 1: Inverse Consider Index 1: Bit [7] for tex[8n], bit [6] for tex[8n+1].....bit [0] for tex[8n+7] Consider Index 2: Bits [7:6] for tex[4n], bits [5:4] for tex[4n+1].....bits [1:0] for tex[4n+3] Consider Index 4: Bits [7:4] for tex[2n], bits [3:0] for tex[2n+1]</p>
13:11	WO	xxh	<p>Mode for Z (Depth) Format Texture 000: D3D Mode R = 0.0 G = Z B = 0.0 A = 1.0 010: Luminance mode R = Z G = Z B = Z A = 1.0 100: Intensity mode</p>

			<p>R = Z G = Z B = Z A = Z</p> <p>110: Alpha mode R = 0.0 G = 0.0 B = 0.0 A = Z</p>
10:9	WO	xxh	Reserved
8	WO	xxh	<p>Texture Is as sRGB (Non-gamma 1.0). The deGamma correction is necessary for deGamma table "HDGTRTX". DeGamma correction is only used to R, G and B component. Any color format could be deGammaed just after the filtering (& color space conversation). 0: Disable DeGamma 1: Enable DeGamma</p>
7:2	WO	xxh	Reserved
1:0	WO	xxh	<p>Video Texture Is as BT601(SDTV), BT709(HDTV) or Just RGB</p> <p>00: RGB For this format, consider the 8-bit Y as positive 8-bit G, 8-bit U as positive 8-bit R, and 8-bit V as positive 8-bit B. Then extend them to s1.10 according to setting of HTXnCEExtend. Then filter the texels. For this setting, YUV2RGB transform is not done in format decoder module or YUV2RGB transformed implemented by PS.</p> <p>01: BT601(SDTV) R = clip (round (((Y - 16)*1.164383 + (V - 128)*1.596027)*256/255)) G = clip (round (((Y - 16)*1.164383 - (U - 128)*0.391762) - (V - 128)*0.812968)) * 256 / 255) B = clip (round (((Y - 16)*1.164383 + (U - 128)*2.017232) * 256 / 255))</p> <p>10: BT709(HDTV) R = clip (round (((Y - 16)*1.164383 - (U - 128)*0.0002) + (V - 128)*1.7927) * 256 / 255) G = clip (round (((Y - 16)*1.164383 - (U - 128)*0.2132) - (V - 128)*0.5329)) * 256 / 255) B = clip (round (((Y - 16)*1.164383 + (U - 128)*2.2114) - (V - 128)*0.0001)) * 256 / 255)</p> <p>11: Table For 8-bit YUV R = clip (round ((Y*A + U*B1 + V*C1 + D) * 256 / 255)) G = clip (round ((Y*A + U*B2 + V*C2 + D) * 256 / 255)) B = clip (round ((Y*A + U*B3 + V*C3 + D) * 256 / 255)) For 10-bit YUV R = clip (round ((Y*A + U*B1 + V*C1 + D) * 1024 / 1023)) G = clip (round ((Y*A + U*B2 + V*C2 + D) * 1024 / 1023)) B = clip (round ((Y*A + U*B3 + V*C3 + D) * 1024 / 1023))</p>

HParaType = 02h (HParaSubType = 00h-0Fh), Sub-Address = 50h
Software Inspection for Texture N – 1st Flag Number

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	Reserved
15:0	WO	xxh	Texture N's 1st Flag Number for SW inspection

HParaType = 02h (HParaSubType = 00h-0Fh), Sub-Address = 51h
Software Inspection for Texture N – 2nd Flag Number

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	Reserved
15:0	WO	xxh	Texture n's 2nd Flag Number for SW inspection

HParaType 02h: Attribute of Texture Sample Stage N (HParaSubType: 20-2Fh)

The register table in this section is used for the following HParaSubTypes (from 20h to 2Fh).

- HParaSubType = 0010 0000 (20h) For Texture Sample 0
- HParaSubType = 0010 0001 (21h) For Texture Sample 1
- HParaSubType = 0010 0010 (22h) For Texture Sample 2
- HParaSubType = 0010 0011 (23h) For Texture Sample 3
- HParaSubType = 0010 0100 (24h) For Texture Sample 4
- HParaSubType = 0010 0101 (25h) For Texture Sample 5
- HParaSubType = 0010 0110 (26h) For Texture Sample 6
- HParaSubType = 0010 0111 (27h) For Texture Sample 7
- HParaSubType = 0010 1000 (28h) For Texture Sample 8
- HParaSubType = 0010 1001 (29h) For Texture Sample 9
- HParaSubType = 0010 1010 (2Ah) For Texture Sample A
- HParaSubType = 0010 1011 (2Bh) For Texture Sample B
- HParaSubType = 0010 1100 (2Ch) For Texture Sample C
- HParaSubType = 0010 1101 (2Dh) For Texture Sample D
- HParaSubType = 0010 1110 (2Eh) For Texture Sample E
- HParaSubType = 0010 1111 (2Fh) For Texture Sample F

Sub-Address (Bits [31:24]): 00-51h

HParaType = 02h (HParaSubType = 20h-2Fh), Sub-Address = 00h-2Fh: Reserved

HParaType = 02h (HParaSubType = 20h-2Fh), Sub-Address = 30h Texture Level Control 1

Bits [23:0]	Attribute	Default	Description
23:22	WO	xxh	Reserved
21:12	WO	xxh	Texture Level 0 Offset Format: 2's Complement fixed-point number with 5-bit integer and 5-bit fraction. The real Level 0 is (Texture Minimum Level + HTXnLOOS). Bits [21:17]: 5-bit integer of Texture n Level 0. Bits [16:12]: 5-bit fraction of Texture n Level 0.
11:6	WO	xxh	Maximum Texture Level 000000: Texture n Maximum Level = 0 000001: Texture n Maximum Level = 1 000010: Texture n Maximum Level = 2 000011: Texture n Maximum Level = 3 000100: Texture n Maximum Level = 4 000101: Texture n Maximum Level = 5 000110: Texture n Maximum Level = 6 000111: Texture n Maximum Level = 7 001000: Texture n Maximum Level = 8 001001: Texture n Maximum Level = 9 001010: Texture n Maximum Level = A 001011: Texture n Maximum Level = B Others: Reserved
5:0	WO	xxh	Minimum Texture Level 000000: Texture n Minimum Level = 0 000001: Texture n Minimum Level = 1 000010: Texture n Minimum Level = 2 000011: Texture n Minimum Level = 3 000100: Texture n Minimum Level = 4 000101: Texture n Minimum Level = 5 000110: Texture n Minimum Level = 6 000111: Texture n Minimum Level = 7 001000: Texture n Minimum Level = 8 001001: Texture n Minimum Level = 9 001010: Texture n Minimum Level = A 001011: Texture n Minimum Level = B Others: Reserved

HParaType = 02h (HParaSubType = 20h-2Fh), Sub-Address = 31h
Texture Filter Control 1

Bits [23:0]	Attribute	Default	Description
23:21	WO	xxh	Reserved
20:16	WO	xxh	Maximum Ratio for Anisotropy (Maximum up to 16) 00000: Max ratio to 0 (no anisotropy) 00001: Max ratio to 1 (no anisotropy) 00010: Max ratio to 2 00011: Max ratio to 3 00100: Max ratio to 4 01111: Max ratio to 15 10000: Max ratio to 16 Others: Reserved
15:13	WO	xxh	Texture Filter Setting in S Direction for Texture Enlargement 000: Nearest 001: Linear 010: Linear Anisotropy 011: 4x4 filter Others: Reserved
12:10	WO	xxh	Texture Filter Setting in S Direction for Texture Shrinking 000: Nearest 001: Linear 010: Linear Anisotropy 011: 4x4 filter Others: Reserved
9:7	WO	xxh	Texture Filter Setting in T Direction for Texture Enlargement 000: Nearest 001: Linear 010: Linear Anisotropy 011: 4x4 filter Others: Reserved <i>*HTXSnFLTe & HTXSnFLSe must be the same when Linear Anisotropy is set.</i>
6:4	WO	xxh	Texture Filter Setting in T Direction For Texture Shrinking 000: Nearest 001: Linear 010: Linear Anisotropy 011: 4x4 filter Others: Reserved <i>* HTXSnFLT_s & HTXSnFLS_s must be the same when Linear Anisotropy is set.</i>
3:0	WO	xxh	Texture Filter Setting in D Direction For Texture Shrinking 0000: Always uses Texture Level 0 0001: Nearest 0010: Linear 0011: Reserved 0100: Dither Others: Reserved

HPParaType = 02h (HPParaSubType = 20h-2Fh), Sub-Address = 32h
Texture Filter Control 2 & Texture Mapping Control

Bits [23:0]	Attribute	Default	Description
23:22	WO	xxh	Reserved
21:19	WO	xxh	Texture Filter Setting in R Direction for Texture Enlargement (Only for 3D Volume Texture) 000: Nearest 001: Linear Others: Reserved
18:16	WO	xxh	Texture Filter Setting in R Direction For Texture Shrinking (Only for 3D Volume Texture) 000: Nearest 001: Linear Others: Reserved
15:12	WO	xxh	Reserved
11:0	WO	xxh	Texture Mapping Mode <u>Bits [11:9]: Reserved</u> <u>Bits [8:6]: R Axis Setting (for 3D Volume texture)</u> 000: Border Color 001: Clamp 010: Repeat 011: Mirror 110-100: Reserved 111: Mirror Once <u>Bits [5:3]: T Axis Setting</u> 000: Border Color 001: Clamp 010: Repeat 011: Mirror 110-100: Reserved 111: Mirror Once <u>Bits [2:0]: S Axis Setting</u> 000: Border Color 001: Clamp 010: Repeat 011: Mirror 110-100: Reserved 111: Mirror Once

HPParaType = 02h (HPParaSubType = 20h-2Fh), Sub-Address = 33-34h: Reserved

HPParaType = 02h (HPParaSubType = 20h-2Fh), Sub-Address = 35h
Texture Border Control 1

Bits [23:0]	Attribute	Default	Description
23:12	WO	xxh	Red Color or U Component of Texture Border <HTXS_nTBR> As s1.10 from -1.0 to 1.0
11:0	WO	xxh	Green Color or Y Component of Texture Border <HTXS_nTBG> As s1.10 from -1.0 to 1.0

HPParaType = 02h (HPParaSubType = 20h-2Fh), Sub-Address = 36h

Texture Border Control 2

Bits [23:0]	Attribute	Default	Description
23:12	WO	xxh	Blue Color or V Component of Texture Border <HTXSnTBB> As s1.10 from -1.0 to 1.0
11:0	WO	xxh	Texture Border Alpha <HTXSnTBA> As s1.10 from -1.0 to 1.0 <i>Note for texture border color's usage:</i> If (((HTXnFM == L16 or VU16 or G16R16 or G16FR16F or G32F) (HTXnFM == Z-format) & (HTXnZMode ≠ Percentage Closer Filter)) & (any filtered texel is border color)) { A channel of filter output = HTXSnTBA R channel of filter output = HTXSnTBR G channel of filter output = HTXSnTBG B channel of filter output = HTXSnTBB } else if ((HTXnFM == 24-bit fixed Z-format) & (HTXnZMode == Percentage Closer Filter) & (texel is border color)) { Use {HTXSnTBR[11:0], HTXSnTBG[11:0]} as border value with format .24 } else { If (the texel is border color) { A channel of filter input of the texel = HTXSnTBA R channel of filter input of the texel = HTXSnTBR G channel of filter input of the texel = HTXSnTBG B channel of filter input of the texel = HTXSnTBB } else { //the texel is just from the texture A channel of filter input of the texel = A after "color extending" R channel of filter input of the texel = R after "color extending" G channel of filter input of the texel = G after "color extending" B channel of filter input of the texel = B after "color extending" } } Note for YUV format and HTXnYUV2RGBmode is SDTV or HDTV, the border color is not in RGB space any more. It must be inverse transformed to YUV space as HTXSnTBG <= Y, HTXSnTBR <= U & HTXSnTBB <= V. And the HTXSnTBG[1:0], HTXSnTBR[1:0] & HTXSnTBB[1:0] are all zero.

HPParaType = 02h (HPParaSubType = 20h-2Fh), Sub-Address = 37-40h: Reserved

HPParaType = 02h (HPParaSubType = 20h-2Fh), Sub-Address = 50h

Software Inspection for Texture Sample N – 1st Flag Number

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	Reserved
15:0	WO	xxh	Texture Sample n's 1st Flag Number for SW Inspection

HPParaType = 02h (HPParaSubType = 20h-2Fh), Sub-Address = 51h

Software Inspection for Texture Sample N – 2nd Flag Number

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	Reserved
10:0	WO	xxh	Texture Sample N's 2nd Flag Number for SW Inspection

HParaType 02h: Attribute of Texture Stage N (HParaSubType: FEh)

The register tables in this section are used for HParaSubType (FEh).

Sub-Address (Bits [31:24]): 00-13h

HParaType = 02h (HParaSubType = FEh), Sub-Address = 00h

General Texture Attribute Control

For General Texture Attribute and User Defined Clipping Plane.

Bits [23:0]	Attribute	Default	Description
23:8	WO	xxh	Reserved
7:4	WO	xxh	Number of Texture n: n Texture, max up to 8
3:2	WO	xxh	Configuration of Data FIFO for Reading Texture 00: DFIFO1 is assigned to System memory's 1 st T-Arbitrator (SL) DFIFO2 is assigned to System memory's 2 nd T-Arbitrator (SF) DFIFO3 is assigned to Local Memory's T-Arbitrator 01: DFIFO1 is assigned to System memory's 1 st T-Arbitrator (SL) DFIFO2 is assigned to Local Memory's T-Arbitrator DFIFO3 is assigned to System memory's 2 nd T-Arbitrator (SF) 10: DFIFO1 is assigned to Local Memory's T-Arbitrator DFIFO2 is assigned to System memory's 2 nd T-Arbitrator (SF) DFIFO3 is assigned to System memory's 1 st T-Arbitrator (SL) 11: Reserved
1	WO	xxh	Fetch Texture 2 QWs (256 bits) or 4 QWs (512 bits) for Each Request 0: Fetch 4 QWs (512 bits) for tiled-mode texture 1: Fetch 2 QWs (256 bits)
0	WO	xxh	Clear Texture Cache 0: Don't care 1: Clear texture cache

HParaType = 02h (HParaSubType = FEh), Sub-Address = 01h
Attribute of Texture 0/1/2

Texture 0 to Texture 7 are defined for Primitive Engine.

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	Reserved
22:21	WO	xxh	Perspective Mode of Texture 2 00: Disable 01: Enable perspective correction 10: Enable projection and be implemented to UVD module 11: Reserved
20:18	WO	xxh	Source of Texture 2 000: Texture comes from Texture A 001: Texture comes from Texture B 010: Texture comes from Texture C 011: Texture comes from Texture D 100: Texture comes from Texture E 101: Texture comes from Texture F 110: Texture comes from Texture G 111: Texture comes from Texture H
17:16	WO	xxh	Dimension of Texture 2 00: 1 dimension; only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture; S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates
15	WO	xxh	Reserved
14:13	WO	xxh	Perspective Mode of Texture 1 00: Disable 01: Enable perspective correction 10: Enable projection and be implemented to UVD module 11: Reserved
12:10	WO	xxh	Source of Texture 1 000: Texture comes from Texture A 001: Texture comes from Texture B 010: Texture comes from Texture C 011: Texture comes from Texture D 100: Texture comes from Texture E 101: Texture comes from Texture F 110: Texture comes from Texture G 111: Texture comes from Texture H
9:8	WO	xxh	Dimension of Texture 1 00: 1 dimension; only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture; S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates
7	WO	xxh	Reserved
6:5	WO	xxh	Perspective Mode of Texture 0 00: Disable 01: Enable perspective correction 10: Enable projection and be implemented to UVD module 11: Reserved
4:2	WO	xxh	Source of Texture 0 000: Texture comes from Texture A 001: Texture comes from Texture B 010: Texture comes from Texture C 011: Texture comes from Texture D 100: Texture comes from Texture E 101: Texture comes from Texture F 110: Texture comes from Texture G 111: Texture comes from Texture H
1:0	WO	xxh	Dimension of Texture 0 00: 1 dimension; only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture; S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates

HParaType = 02h (HParaSubType = FEh), Sub-Address = 02h
Attribute of Texture 3/4/5

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	Reserved
22:21	WO	xxh	Perspective Mode of Texture 5 00: Disable 01: Enable perspective correction 10: Enable projection and be implemented to UVD module 11: Reserved
20:18	WO	xxh	Source of Texture 5 000: Texture comes from Texture A 001: Texture comes from Texture B 010: Texture comes from Texture C 011: Texture comes from Texture D 100: Texture comes from Texture E 101: Texture comes from Texture F 110: Texture comes from Texture G 111: Texture comes from Texture H
17:16	WO	xxh	Dimension of Texture 5 00: 1 dimension; only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture; S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates
15	WO	xxh	Reserved
14:13	WO	xxh	Perspective Mode of Texture 4 00: Disable 01: Enable perspective correction 10: Enable projection and be implemented to UVD module 11: Reserved
12:10	WO	xxh	Source of Texture 4 000: Texture comes from Texture A 001: Texture comes from Texture B 010: Texture comes from Texture C 011: Texture comes from Texture D 100: Texture comes from Texture E 101: Texture comes from Texture F 110: Texture comes from Texture G 111: Texture comes from Texture H
9:8	WO	xxh	Dimension of Texture 4 00: 1 dimension; only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture; S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates
7	WO	xxh	Reserved
6:5	WO	xxh	Perspective Mode of Texture 3 00: Disable 01: Enable perspective correction 10: Enable projection and be implemented to UVD module 11: Reserved
4:2	WO	xxh	Source of Texture 3 000: Texture comes from Texture A 001: Texture comes from Texture B 010: Texture comes from Texture C 011: Texture comes from Texture D 100: Texture comes from Texture E 101: Texture comes from Texture F 110: Texture comes from Texture G 111: Texture comes from Texture H
1:0	WO	xxh	Dimension of Texture 3 00: 1 dimension; only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture; S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates

HParaType = 02h (HParaSubType = FEh), Sub-Address = 03h
Attribute of Texture 6/7

Bits [23:0]	Attribute	Default	Description
23:19	WO	xxh	Threshold Value for Mip-map Linear Mode Format is positive fixed .5.
18:15	WO	xxh	Reserved
14:13	WO	xxh	Perspective Mode of Texture 7 00: Disable 01: Enable perspective correction 10: Enable projection and be implemented to UVD module 11: Reserved
12:10	WO	xxh	Source of Texture 7 000: Texture comes from Texture A 001: Texture comes from Texture B 010: Texture comes from Texture C 011: Texture comes from Texture D 100: Texture comes from Texture E 101: Texture comes from Texture F 110: Texture comes from Texture G 111: Texture comes from Texture H
9:8	WO	xxh	Dimension of Texture 7 00: 1 dimension; only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture; S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates
7	WO	xxh	Reserved
6:5	WO	xxh	Perspective Mode of Texture 6 00: Disable 01: Enable perspective correction 10: Enable projection and be implemented to UVD module 11: Reserved
4:2	WO	xxh	Source of Texture 6 000: Texture comes from Texture A 001: Texture comes from Texture B 010: Texture comes from Texture C 011: Texture comes from Texture D 100: Texture comes from Texture E 101: Texture comes from Texture F 110: Texture comes from Texture G 111: Texture comes from Texture H
1:0	WO	xxh	Dimension of Texture 6 00: 1 dimension; only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture; S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates

HParaType = 02h (HParaSubType = FEh), Sub-Address = 04h
Texture Coordinate Control

Bits [23:0]	Attribute	Default	Description
23:20	WO	xxh	Exponential of Width for the Texture Coordinate Replaced by (x, y) <HTXXYrpSTWE> $s = x / 2^{\text{HTXXYrpSTWE}}$
19:16	WO	xxh	Exponential of High for the Texture Coordinate Replaced by (x, y) <HTXXYrpSTHE> $t = y / 2^{\text{HTXXYrpSTHE}}$
15:8	WO	xxh	Reserved
7:0	WO	xxh	Use Screen Coordinates (x,y) to Replace (s, t) <i>The value of bit[n] is used to control the setting of corresponding Textue[n]. (ex. bit[0] for Texture 0, bit[1] for Texture 1)</i> 0: Normal (s,t) for Texture n 1: Use (x,y) to replace (s, t) for Texture n

HParaType = 02h (HParaSubType = FEh), Sub-Address = 05h
User Defined Clipping Planes Control - 1st/2nd Groups

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	Reserved
15	WO	xxh	Enable of 2nd Group of User Defined Clipping Planes <HTXUCPIEnable> 0: Disable. No user defined clipping plane or only 1 texture is used for "User defined Clipping Plane". 1: Enable. A 2 nd texture is used for "User defined Clipping Plane".
14	WO	xxh	Perspective Mode of the Texture for 2nd Group of User Defined Clipping Planes 0: Disable 1: Enable perspective correction
13:10	WO	xxh	Source of the Texture for 2nd Group of User Defined Clipping Planes 0000: Texture comes from Texture A 0001: Texture comes from Texture B 0010: Texture comes from Texture C 0011: Texture comes from Texture D 0100: Texture comes from Texture E 0101: Texture comes from Texture F 0110: Texture comes from Texture G 0111: Texture comes from Texture H 1000: Texture comes from Texture I 1001: Texture comes from Texture J Others: Reserved
9:8	WO	xxh	Dimension of the Texture for 2nd Group of User Defined Clipping Planes 00: 1 dimension; only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture; S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates
7	WO	xxh	Enable of 1st Group of User Defined Clipping Planes <HTXUCP0Enable> 0: Disable. No user defined clipping plane. 1: Enable. A texture is used for "User defined Clipping Plane".
6	WO	xxh	Perspective Mode of the Texture for 1st Group of User Defined Clipping Planes 0: Disable 1: Enable perspective correction
5:2	WO	xxh	Source of the Texture for 1st Group of User Defined Clipping Planes 0000: Texture come from Texture A 0001: Texture come from Texture B 0010: Texture come from Texture C 0011: Texture come from Texture D 0100: Texture come from Texture E 0101: Texture come from Texture F 0110: Texture come from Texture G 0111: Texture come from Texture H 1000: Texture come from Texture I 1001: Texture come from Texture J Others: Reserved
1:0	WO	xxh	Dimension of the Texture for 1st Group of User Defined Clipping Planes 00: 1 dsimension; only S coordinate 01: 2 dimensions; both S and T coordinate 10: 3 dimensions; volume texture; S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates

HParaType = 02h (HParaSubType = FEh), Sub-Address = 06-07h: Reserved

HParaType = 02h (HParaSubType = FEh), Sub-Address = 08h
Texture A-H Control 1

Texture A to Texture H is defined in Vertex Buffer.

Bits [23:0]	Attribute	Default	Description
23:22	WO	xxh	Reserved
21	WO	xxh	Texture S Coordinate Input Mode – for Texture B 0: Un-normalized 1: Normalized
20	WO	xxh	Texture T Coordinate Input Mode – for Texture B 0: Un-normalized 1: Normalized
19	WO	xxh	Texture R Coordinate Input Mode – for Texture B 0: Un-normalized 1: Normalized
18	WO	xxh	Texture Q Coordinate Input Mode – for Texture B 0: Un-normalized 1: Normalized
17:16	WO	xxh	Dimension of Texture B 00: 1 dimension; only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture. S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates
15:14	WO	xxh	Reserved
13	WO	xxh	Texture S Coordinate Input Mode – for Texture A 0: Un-normalized 1: Normalized
12	WO	xxh	Texture T Coordinate Input Mode – for Texture A 0: Un-normalized 1: Normalized
11	WO	xxh	Texture R Coordinate Input Mode – for Texture A 0: Un-normalized 1: Normalized
10	WO	xxh	Texture Q Coordinate Input Mode – for Texture A 0: Un-normalized 1: Normalized
9:8	WO	xxh	Dimension of Texture A 00: 1 dimension, only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture. S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates
7:4	WO	xxh	Reserved
3:0	WO	xxh	Number of Texture Coordinate Register in Vertex Buffer's Output Register n: n Textures Note: The less resource used (texture coordinate register, input register, output register and temporary register), the more threads be dealt with in the VS, and the better performance.

HParaType = 02h (HParaSubType = FEh), Sub-Address = 09h
Texture A-H Control 2

Bits [23:0]	Attribute	Default	Description
23:22	WO	xxh	Reserved
21	WO	xxh	Texture S Coordinate Input Mode – for Texture E 0: Un-normalized 1: Normalized
20	WO	xxh	Texture T Coordinate Input Mode – for Texture E 0: Un-normalized 1: Normalized
19	WO	xxh	Texture R Coordinate Input Mode – for Texture E 0: Un-normalized 1: Normalized
18	WO	xxh	Texture Q Coordinate Input Mode – for Texture E 0: Un-normalized 1: Normalized
17:16	WO	xxh	Dimension of Texture E 00: 1 dimension; only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture; S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates
15:14	WO	xxh	Reserved
13	WO	xxh	Texture S Coordinate Input Mode – for Texture D 0: Un-normalized 1: Normalized
12	WO	xxh	Texture T Coordinate Input Mode – for Texture D 0: Un-normalized 1: Normalized
11	WO	xxh	Texture R Coordinate Input Mode – for Texture D 0: Un-normalized 1: Normalized
10	WO	xxh	Texture Q Coordinate Input Mode – for Texture D 0: Un-normalized 1: Normalized
9:8	WO	xxh	Dimension of Texture D 00: 1 dimension; only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture; S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates
7:6	WO	xxh	Reserved
5	WO	xxh	Texture S Coordinate Input Mode – for Texture C 0: Un-normalized 1: Normalized
4	WO	xxh	Texture T Coordinate Input Mode – for Texture C 0: Un-normalized 1: Normalized
3	WO	xxh	Texture R Coordinate Input Mode – for Texture C 0: Un-normalized 1: Normalized
2	WO	xxh	Texture Q Coordinate Input Mode – for Texture C 0: Un-normalized 1: Normalized
1:0	WO	xxh	Dimension of Texture C 00: 1 dimension; only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture; S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates

HParaType = 02h (HParaSubType = FEh), Sub-Address = 0Ah
Texture A-H Control 3

Bits [23:0]	Attribute	Default	Description
23:22	WO	xxh	Reserved
21	WO	xxh	Texture S Coordinate Input Mode – for Texture H 0: Un-normalized 1: Normalized
20	WO	xxh	Texture T Coordinate Input Mode – for Texture H 0: Un-normalized 1: Normalized
19	WO	xxh	Texture R Coordinate Input Mode – for Texture H 0: Un-normalized 1: Normalized
18	WO	xxh	Texture Q Coordinate Input Mode – for Texture H 0: Un-normalized 1: Normalized
17:16	WO	xxh	Dimension of Texture H 00: 1 dimension; only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture; S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates
15:14	WO	xxh	Reserved
13	WO	xxh	Texture S Coordinate Input Mode – for Texture G 0: Un-normalized 1: Normalized
12	WO	xxh	Texture T Coordinate Input Mode – for Texture G 0: Un-normalized 1: Normalized
11	WO	xxh	Texture R Coordinate Input Mode – for Texture G 0: Un-normalized 1: Normalized
10	WO	xxh	Texture Q Coordinate Input Mode – for Texture G 0: Un-normalized 1: Normalized
9:8	WO	xxh	Dimension of Texture G 00: 1 dimension, only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture; S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates
7:6	WO	xxh	Reserved
5	WO	xxh	Texture S Coordinate Input Mode – for Texture F 0: Un-normalized 1: Normalized
4	WO	xxh	Texture T Coordinate Input Mode – for Texture F 0: Un-normalized 1: Normalized
3	WO	xxh	Texture R Coordinate Input Mode – for Texture F 0: Un-normalized 1: Normalized
2	WO	xxh	Texture Q Coordinate Input Mode – for Texture F 0: Un-normalized 1: Normalized
1:0	WO	xxh	Dimension of Texture F 00: 1 dimension; only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture; S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates

HPParaType = 02h (HPParaSubType = FEh), Sub-Address = 0Bh
Texture A-H Control 4

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	Reserved
15	WO	xxh	Texture D Wrap Correction along S Coordinate 0: No wrap 1: Wrap
14	WO	xxh	Texture D Wrap Correction along T Coordinate 0: No wrap 1: Wrap
13:12	WO	xxh	Reserved
11	WO	xxh	Texture C Wrap Correction along S Coordinate 0: No wrap 1: Wrap
10	WO	xxh	Texture C Wrap Correction along T Coordinate 0: No wrap 1: Wrap
9:8	WO	xxh	Reserved
7	WO	xxh	Texture B Wrap Correction along S Coordinate 0: No wrap 1: Wrap
6	WO	xxh	Texture B Wrap Correction along T Coordinate 0: No wrap 1: Wrap
5:4	WO	xxh	Reserved
3	WO	xxh	Texture A Wrap Correction along S Coordinate 0: No wrap 1: Wrap
2	WO	xxh	Texture A Wrap Correction along T Coordinate 0: No wrap 1: Wrap
1:0	WO	xxh	Reserved

HPParaType = 02h (HPParaSubType = FEh), Sub-Address = 0Ch
Texture A-H Control 5

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	Reserved
15	WO	xxh	Texture H Wrap Correction along S Coordinate 0: No wrap 1: Wrap
14	WO	xxh	Texture H Wrap Correction along T Coordinate 0: No wrap 1: Wrap
13:12	WO	xxh	Reserved
11	WO	xxh	Texture G Wrap Correction along S Coordinate 0: No wrap 1: Wrap
10	WO	xxh	Texture G Wrap Correction along T Coordinate 0: No wrap 1: Wrap
9:8	WO	xxh	Reserved
7	WO	xxh	Texture F Wrap Correction along S Coordinate 0: No wrap 1: Wrap
6	WO	xxh	Texture F Wrap Correction along T Coordinate 0: No wrap 1: Wrap
5:4	WO	xxh	Reserved
3	WO	xxh	Texture E Wrap Correction along S Coordinate 0: No wrap 1: Wrap
2	WO	xxh	Texture E Wrap Correction along T Coordinate 0: No wrap 1: Wrap
1:0	WO	xxh	Reserved

HPParaType = 02h (HPParaSubType = FEh), Sub-Address = 0Dh
Texture A-H Control 6

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	Exponential of Modulus
15:8	WO	xxh	Reserved
7	WO	xxh	Do “Modulus of 2^{HTXMODE}” with Texture H’s Coordinate
6	WO	xxh	Do “Modulus of 2^{HTXMODE}” with Texture G’s Coordinate
5	WO	xxh	Do “Modulus of 2^{HTXMODE}” with Texture F’s Coordinate
4	WO	xxh	Do “Modulus of 2^{HTXMODE}” with Texture E’s Coordinate
3	WO	xxh	Do “Modulus of 2^{HTXMODE}” with Texture D’s Coordinate
2	WO	xxh	Do “Modulus of 2^{HTXMODE}” with Texture C’s Coordinate
1	WO	xxh	Do “Modulus of 2^{HTXMODE}” with Texture B’s Coordinate
0	WO	xxh	Do “Modulus of 2^{HTXMODE}” with Texture A’s Coordinate

HPParaType = 02h (HPParaSubType = FEh), Sub-Address = 0Eh
Texture I/J Control

Bits [23:0]	Attribute	Default	Description
23:14	WO	xxh	Reserved
13	WO	xxh	Texture S Coordinate Input Mode – for Texture J 0: Un-normalized 1: Normalized
12	WO	xxh	Texture T Coordinate Input Mode – for Texture J 0: Un-normalized 1: Normalized
11	WO	xxh	Texture R Coordinate Input Mode – for Texture J 0: Un-normalized 1: Normalized
10	WO	xxh	Texture Q Coordinate Input Mode – for Texture J 0: Un-normalized 1: Normalized
9:8	WO	xxh	Dimension of Texture J 00: 1 dimension; only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture. S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates
7:6	WO	xxh	Reserved
5	WO	xxh	Texture S Coordinate Input Mode – for Texture I 0: Un-normalized 1: Normalized
4	WO	xxh	Texture T Coordinate Input Mode – for Texture I 0: Un-normalized 1: Normalized
3	WO	xxh	Texture R Coordinate Input Mode – for Texture I 0: Un-normalized 1: Normalized
2	WO	xxh	Texture Q Coordinate Input Mode – for Texture I 0: Un-normalized 1: Normalized
1:0	WO	xxh	Dimension of Texture I 00: 1 dimension, only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture; S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates

HPParaType = 02h (HPParaSubType = FEh), Sub-Address = 0Fh: Reserved

HPParaType = 02h (HPParaSubType = FEh), Sub-Address = 10h
Coefficient Setting 1

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	YUV422 (Packet Mode) Texture Decode Mode 0: Even texel in S direction (Y_e, U_n, V_n) Odd texel in S direction (Y_o, U_n, V_n) 1: Even texel in S direction (Y_e, U_n, V_n) Odd texel in S direction ($Y_o, (U_n + U_{n+1})/2, (V_n + V_{n+1})/2$) Note: If (HTXYUV422DM == true & HTXnFM == 00110 000b & (HTXSnFLSe == nearest for enlarge HTXSnFLSs == nearest for shrink) & (odd texel in S direction) & (not the rightest texel of texture)) { $Y = Y_o$ $U = (U_n + U_{n+1})/2$ $V = (V_n + V_{n+1})/2$ } else { $Y = Y$ $U = U_n$ $V = V_n$ }
22:12	WO	xxh	Coefficient D of YUV to RGB Conversion Format as 2's complement s2.8
11	WO	xxh	Reserved
10:0	WO	xxh	Coefficient A of YUV to RGB Conversion Format as 2's complement s2.8

HPParaType = 02h (HPParaSubType = FEh), Sub-Address = 11h
Coefficient Setting 2

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	Reserved
22:12	WO	xxh	Coefficient C1 of YUV to RGB Conversion Format as 2's complement s2.8
11	WO	xxh	Reserved
10:0	WO	xxh	Coefficient B1 of YUV to RGB Conversion Format as 2's complement s2.8

HPParaType = 02h (HPParaSubType = FEh), Sub-Address = 12h
Coefficient Setting 3

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	Reserved
22:12	WO	xxh	Coefficient C2 of YUV to RGB Conversion Format as 2's complement s2.8
11	WO	xxh	Reserved
10:0	WO	xxh	Coefficient B2 of YUV to RGB Conversion Format as 2's complement s2.8

HPParaType = 02h (HPParaSubType = FEh), Sub-Address = 13h
Coefficient Setting 4

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	Reserved
22:12	WO	xxh	Coefficient C3 of YUV to RGB Conversion Format as 2's complement s2.8
11	WO	xxh	Reserved
10:0	WO	xxh	Coefficient B3 of YUV to RGB Conversion Format as 2's complement s2.8

HParaType 03h: Palette (HParaSubType: 00-22h)

HParaType = 03h (HParaSubType = 00h)

Texture Palette 0

This is only for Video Texture with A144 and IA44. There are just 16 entries with 24-bit width as Y8U8V8.

Bits	Attribute	Default	Description
31:24	WO	xxh	Reserved
23:16	WO	xxh	Y of Texture Palette N Data
15:8	WO	xxh	U of Texture Palette N Data
7:0	WO	xxh	V of Texture Palette N Data

HParaType = 03h (HParaSubType = 01h): Reserved (Texture Palette1 1)

HParaType = 03h (HParaSubType = 02h): Reserved (Texture Palette1 2)

HParaType = 03h (HParaSubType = 03h): Reserved (Texture Palette1 3)

HParaType = 03h (HParaSubType = 04h): Reserved (Texture Palette1 4)

HParaType = 03h (HParaSubType = 05h): Reserved (Texture Palette1 5)

HParaType = 03h (HParaSubType = 06h): Reserved (Texture Palette1 6)

HParaType = 03h (HParaSubType = 07h): Reserved (Texture Palette1 7)

HParaType = 03h (HParaSubType = 08-0Fh): Reserved

HParaType = 03h (HParaSubType = 10h)

Offset or Base Address of Texture from Level 1 to Level 8 for the 16 Texture Samples

There are 16 texture samples and each sample can be up to 8 levels, so there should be 16x8 = 128 entries.

- HParaAdr 0 → HTXS0L1Offset
- HParaAdr 1 → HTXS0L2Offset
-
- HParaAdr 7 → HTXS0L8Offset
- HParaAdr 8 → HTXS1L1Offset
- HParaAdr 9 → HTXS1L2Offset
-
- HParaAdr 15 → HTXS1L8Offset
- HParaAdr 16 → HTXS2L1Offset
- HParaAdr 17 → HTXS2L2Offset
-
- HParaAdr 23 → HTXS2L8Offset
-
-
- HParaAdr 118 → HTXSFL1Offset
- HParaAdr 119 → HTXSFL2Offset
-
- HParaAdr 127 → HTXSFL8Offset

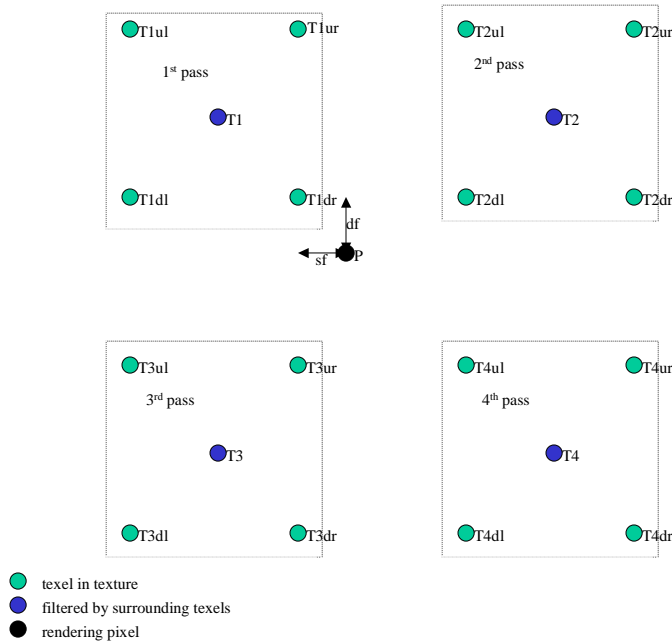
To sum up, consider HTXS n L m BasOffset, its entry is ($n*8 + m$), where n is from 0 to Fh, and m is from 1 to 8h.

Bits	Attribute	Default	Description
31:30	WO	xxh	Location of Texture Sample n's Level m 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: Reserved (System Memory) 11: Reserved (Local Memory Local Frame Buffer (L.L.))
29:24	WO	xxh	Reserved
23:0	WO	xxh	Offset Related to Texture Sample n's Level 0 for Level m Base Address In unit of byte. This must be 256-byte boundary (in unit of 256 bytes or [31:8]).

HParaType = 03h (HParaSubType = 11h)
Texture 4x4 Filter Coefficient Table

There are $2^5 = 32$ entries. The 5-bit fraction of “sf” or “tf” is the index.

Bits	Attribute	Default	Description
31:22	WO	xxh	Reserved
21:16	WO	xxh	Coefficient Cm for 4x4 Filter Format as 1.5 positive fixed-point; maximum is 1.0.
15	WO	xxh	Double the Coefficient Cr 0: Crd = HTX4X4FltCrd 1: Crd = HTX4X4FltCrd << 1
14:8	WO	xxh	Coefficient C2 for 4x4 Filter Format as s1.5 2’s complement fixed-point; maximum is 1.0 and minimum is -0.5.
7	WO	xxh	Double the Coefficient Clu 0: Clu = HTX4X4FltClu 1: Clu = HTX4X4FltClu << 1
6:0	WO	xxh	Coefficient Clu for 4x4 Filter Format as s1.5 2’s complement fixed-point; maximum is 1.0 and minimum is -0.5.



$$Cl = HTX4X4Clu(sf) * 2^{HTX4X4CluE(sf)}$$

$$Cr = HTX4X4Crd(sf) * 2^{HTX4X4CrdE(sf)}$$

$$Csm = HTX4X4Cm(sf)$$

$$Cu = HTX4X4Clu(tf) * 2^{HTX4X4CluE(tf)}$$

$$Cd = HTX4X4Crd(tf) * 2^{HTX4X4CrdE(tf)}$$

$$Ctm = HTX4X4Cm(tf)$$

$$Cp1 = (1 - Csm) * (1 - Ctm)$$

$$Cp2 = Csm * (1 - Ctm)$$

$$Cp3 = (1 - Csm) * Ctm$$

$$Cp4 = Csm * Ctm$$

$$T1 = (1 - Cl) * (1 - Cu) * T1ul + Cl * (1 - Cu) * T1ur + (1 - Cl) * Cu * T1dl + Cl * Cu * T1dr$$

$$T2 = (1 - Cr) * (1 - Cu) * T2ul + Cr * (1 - Cu) * T2ur + (1 - Cr) * Cu * T2dl + Cr * Cu * T2dr$$

$$T3 = (1 - Cl) * (1 - Cd) * T3ul + Cl * (1 - Cd) * T3ur + (1 - Cl) * Cd * T3dl + Cl * Cd * T3dr$$

$$T4 = (1 - Cr) * (1 - Cd) * T4ul + Cr * (1 - Cd) * T4ur + (1 - Cr) * Cd * T4dl + Cr * Cd * T4dr$$

$$P = T1 * Cp1 + T2 * Cp2 + T3 * Cp3 + T4 * Cp4$$

HParaType = 03h (HParaSubType = 14h)
Stipple Palette

Bits	Attribute	Default	Description
31:0	WO	xxh	32-Bit Stipple Palette Data

HParaType = 03h (HParaSubType = 15h), HParaAdr = 00h
De-Gamma Table for Reading Texture

Bits	Attribute	Default	Description
31:30	WO	xxh	Rounding Mode 00: Truncate 01: Rounding 1x: Reserved
29:20	WO	xxh	De-Gamma Table Value for Reading Texture at C = 10'h0C0
19:10	WO	xxh	De-Gamma Table Value for Reading Texture at C = 10'h080
9:0	WO	xxh	De-Gamma Table Value for Reading Texture at C = 10'h040

HParaType = 03h (HParaSubType = 15h), HParaAdr = 01h
De-Gamma Table for Reading Texture

Bits	Attribute	Default	Description
31:30	WO	xxh	Reserved
29:20	WO	xxh	De-Gamma Table Value for Reading Texture at C = 10'h180
19:10	WO	xxh	De-Gamma Table Value for Reading Texture at C = 10'h140
9:0	WO	xxh	De-Gamma Table Value for Reading Texture at C = 10'h100

HParaType = 03h (HParaSubType = 15h), HParaAdr = 02h
De-Gamma Table for Reading Texture

Bits	Attribute	Default	Description
31:30	WO	xxh	Reserved
29:20	WO	xxh	De-Gamma Table Value for Reading Texture at C = 10'h240
19:10	WO	xxh	De-Gamma Table Value for Reading Texture at C = 10'h200
9:0	WO	xxh	De-Gamma Table Value for Reading Texture at C = 10'h1C0

HParaType = 03h (HParaSubType = 15h), HParaAdr = 03h
De-Gamma Table for Reading Texture

Bits	Attribute	Default	Description
31:30	WO	xxh	Reserved
29:20	WO	xxh	De-Gamma Table Value for Reading Texture at C = 10'h300
19:10	WO	xxh	De-Gamma Table Value for Reading Texture at C = 10'h2C0
9:0	WO	xxh	De-Gamma Table Value for Reading Texture at C = 10'h280

HParaType = 03h (HParaSubType = 15h), HParaAdr = 04h
De-Gamma Table for Reading Texture

Bits	Attribute	Default	Description
31:30	WO	xxh	Reserved
29:20	WO	xxh	De-Gamma Table Value for Reading Texture at C = 10'h3C0
19:10	WO	xxh	De-Gamma Table Value for Reading Texture at C = 10'h380
9:0	WO	xxh	De-Gamma Table Value for Reading Texture at C = 10'h340

HParaType = 03h (HParaSubType = 17h), HParaAdr = 00h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	Rounding Mode for R Channel 00: Truncate 01: Rounding 1x: Reserved
29:20	WO	xxh	Gamma Table Value for Writing R Channel at R = 10'h001
19:10	WO	xxh	Gamma Table Value for Writing G Channel at G = 10'h001
9:0	WO	xxh	Gamma Table Value for Writing B Channel at B = 10'h001

HParaType = 03h (HParaSubType = 17h), HParaAdr = 01h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	Rounding Mode for G Channel 00: Truncate 01: Rounding 1x: Reserved
29:20	WO	xxh	Gamma Table Value for Writing R Channel at R = 10'h002
19:10	WO	xxh	Gamma Table Value for Writing G Channel at G = 10'h002
9:0	WO	xxh	Gamma Table Value for Writing B Channel at B = 10'h002

ParaType = 03h (HParaSubType = 17h), HParaAdr = 02h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	Rounding Mode for B Channel 00: Truncate 01: Rounding 1x: Reserved
29:20	WO	xxh	Gamma Table Value for Writing R Channel at R = 10'h003
19:10	WO	xxh	Gamma Table Value for Writing G Channel at G = 10'h003
9:0	WO	xxh	Gamma Table Value for Writing B Channel at B = 10'h003

HParaType = 03h (HParaSubType = 17h), HParaAdr = 03h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31	WO	xxh	Instead of Gamma Correction, but deGamma correction for R Channel 0: Gamma correction 1: de-Gamma correction
30	WO	xxh	Reserved
29:20	WO	xxh	Gamma Table Value for Writing R Channel at R = 10'h004
19:10	WO	xxh	Gamma Table Value for Writing G Channel at G = 10'h004
9:0	WO	xxh	Gamma Table Value for Writing B Channel at B = 10'h004

HParaType = 03h (HParaSubType = 17h), HParaAdr = 04h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31	WO	xxh	Instead of Gamma Correction, but deGamma correction for G Channel 0: Gamma correction 1: de-Gamma correction
30	WO	xxh	Reserved
29:20	WO	xxh	Gamma Table Value for Writing R Channel at R = 10'h006
19:10	WO	xxh	Gamma Table Value for Writing G Channel at G = 10'h006
9:0	WO	xxh	Gamma Table Value for Writing B Channel at B = 10'h006

HParaType = 03h (HParaSubType = 17h), HParaAdr = 05h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31	WO	xxh	Instead of Gamma Correction, but deGamma correction for B Channel 0: Gamma correction 1: de-Gamma correction
30	WO	xxh	Reserved
29:20	WO	xxh	Gamma Table Value for Writing R Channel at R = 10'h008
19:10	WO	xxh	Gamma Table Value for Writing G Channel at G = 10'h008
9:0	WO	xxh	Gamma Table Value for Writing B Channel at B = 10'h008

HParaType = 03h (HParaSubType = 17h), HParaAdr = 06h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	Reserved
29:20	WO	xxh	Gamma Table Value for Writing R Channel at R = 10'h00C
19:10	WO	xxh	Gamma Table Value for Writing G Channel at G = 10'h00C
9:0	WO	xxh	Gamma Table Value for Writing B Channel at B = 10'h00C

HParaType = 03h (HParaSubType = 17h), HParaAdr = 07h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	Reserved
29:20	WO	xxh	Gamma Table Value for Writing R Channel at R = 10'h010
19:10	WO	xxh	Gamma Table Value for Writing G Channel at G = 10'h010
9:0	WO	xxh	Gamma Table Value for Writing B Channel at B = 10'h010

HParaType = 03h (HParaSubType = 17h), HParaAdr = 08h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	Reserved
29:20	WO	xxh	Gamma Table Value for Writing R Channel at R = 10'h018
19:10	WO	xxh	Gamma Table Value for Writing G Channel at G = 10'h018
9:0	WO	xxh	Gamma Table Value for Writing B Channel at B = 10'h018

HParaType = 03h (HParaSubType = 17h), HParaAdr = 09h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	Reserved
29:20	WO	xxh	Gamma Table Value for Writing R Channel at R = 10'h020
19:10	WO	xxh	Gamma Table Value for Writing G Channel at G = 10'h020
9:0	WO	xxh	Gamma Table Value for Writing B Channel at B = 10'h020

HParaType = 03h (HParaSubType = 17h), HParaAdr = 0Ah
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	Reserved
29:20	WO	xxh	Gamma Table Value for Writing R Channel at R = 10'h030
19:10	WO	xxh	Gamma Table Value for Writing G Channel at G = 10'h030
9:0	WO	xxh	Gamma Table Value for Writing B Channel at B = 10'h030

HParaType = 03h (HParaSubType = 17h), HParaAdr = 0Bh
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	Reserved
29:20	WO	xxh	Gamma Table Value for Writing R Channel at R = 10'h040
19:10	WO	xxh	Gamma Table Value for Writing G Channel at G = 10'h040
9:0	WO	xxh	Gamma Table Value for Writing B Channel at B = 10'h040

HParaType = 03h (HParaSubType = 17h), HParaAdr = 0Ch
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	Reserved
29:20	WO	xxh	Gamma Table Value for Writing R Channel at R = 10'h050
19:10	WO	xxh	Gamma Table Value for Writing G Channel at G = 10'h050
9:0	WO	xxh	Gamma Table Value for Writing B Channel at B = 10'h050

HParaType = 03h (HParaSubType = 17h), HParaAdr = 0Dh
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	Reserved
29:20	WO	xxh	Gamma Table Value for Writing R Channel at R = 10'h060
19:10	WO	xxh	Gamma Table Value for Writing G Channel at G = 10'h060
9:0	WO	xxh	Gamma Table Value for Writing B Channel at B = 10'h060

HParaType = 03h (HParaSubType = 17h), HParaAdr = 0Eh
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	Reserved
29:20	WO	xxh	Gamma Table Value for Writing R Channel at R = 10'h070
19:10	WO	xxh	Gamma Table Value for Writing G Channel at G = 10'h070
9:0	WO	xxh	Gamma Table Value for Writing B Channel at B = 10'h070

HParaType = 03h (HParaSubType = 17h), HParaAdr = 0Fh
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	Reserved
29:20	WO	xxh	Gamma Table Value for Writing R Channel at R = 10'h080
19:10	WO	xxh	Gamma Table Value for Writing G Channel at G = 10'h080
9:0	WO	xxh	Gamma Table Value for Writing B Channel at B = 10'h080

HParaType = 03h (HParaSubType = 17h), HParaAdr = 10h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	Reserved
29:20	WO	xxh	Gamma Table Value for Writing R Channel at R = 10'h0A0
19:10	WO	xxh	Gamma Table Value for Writing G Channel at G = 10'h0A0
9:0	WO	xxh	Gamma Table Value for Writing B Channel at B = 10'h0A0

HParaType = 03h (HParaSubType = 17h), HParaAdr = 11h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	Reserved
29:20	WO	xxh	Gamma Table Value for Writing R Channel at R = 10'h0C0
19:10	WO	xxh	Gamma Table Value for Writing G Channel at G = 10'h0C0
9:0	WO	xxh	Gamma Table Value for Writing B Channel at B = 10'h0C0

HParaType = 03h (HParaSubType = 17h), HParaAdr = 12h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	Reserved
29:20	WO	xxh	Gamma Table Value for Writing R Channel at R = 10'h0E0
19:10	WO	xxh	Gamma Table Value for Writing G Channel at G = 10'h0E0
9:0	WO	xxh	Gamma Table Value for Writing B Channel at B = 10'h0E0

HParaType = 03h (HParaSubType = 17h), HParaAdr = 13h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	Reserved
29:20	WO	xxh	Gamma Table Value for Writing R Channel at R = 10'h100
19:10	WO	xxh	Gamma Table Value for Writing G Channel at G = 10'h100
9:0	WO	xxh	Gamma Table Value for Writing B Channel at B = 10'h100

HParaType = 03h (HParaSubType = 17h), HParaAdr = 14h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	Reserved
29:20	WO	xxh	Gamma Table Value for Writing R Channel at R = 10'h140
19:10	WO	xxh	Gamma Table Value for Writing G Channel at G = 10'h140
9:0	WO	xxh	Gamma Table Value for Writing B Channel at B = 10'h140

HParaType = 03h (HParaSubType = 17h), HParaAdr = 15h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	Reserved
29:20	WO	xxh	Gamma Table Value for Writing R Channel at R = 10'h180
19:10	WO	xxh	Gamma Table Value for Writing G Channel at G = 10'h180
9:0	WO	xxh	Gamma Table Value for Writing B Channel at B = 10'h180

HParaType = 03h (HParaSubType = 17h), HParaAdr = 16h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	Reserved
29:20	WO	xxh	Gamma Table Value for Writing R Channel at R = 10'h1C0
19:10	WO	xxh	Gamma Table Value for Writing G Channel at G = 10'h1C0
9:0	WO	xxh	Gamma Table Value for Writing B Channel at B = 10'h1C0

HParaType = 03h (HParaSubType = 17h), HParaAdr = 17h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	Reserved
29:20	WO	xxh	Gamma Table Value for Writing R Channel at R = 10'h200
19:10	WO	xxh	Gamma Table Value for Writing G Channel at G = 10'h200
9:0	WO	xxh	Gamma Table Value for Writing B Channel at B = 10'h200

HParaType = 03h (HParaSubType = 17h), HParaAdr = 18h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	Reserved
29:20	WO	xxh	Gamma Table Value for Writing R Channel at R = 10'h240
19:10	WO	xxh	Gamma Table Value for Writing G Channel at G = 10'h240
9:0	WO	xxh	Gamma Table Value for Writing B Channel at B = 10'h240

HParaType = 03h (HParaSubType = 17h), HParaAdr = 19h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	Reserved
29:20	WO	xxh	Gamma Table Value for Writing R Channel at R = 10'h280
19:10	WO	xxh	Gamma Table Value for Writing G Channel at G = 10'h280
9:0	WO	xxh	Gamma Table Value for Writing B Channel at B = 10'h280

HParaType = 03h (HParaSubType = 17h), HParaAdr = 1Ah
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	Reserved
29:20	WO	xxh	Gamma Table Value for Writing R Channel at R = 10'h2C0
19:10	WO	xxh	Gamma Table Value for Writing G Channel at G = 10'h2C0
9:0	WO	xxh	Gamma Table Value for Writing B Channel at B = 10'h2C0

HParaType = 03h (HParaSubType = 17h), HParaAdr = 1Bh
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	Reserved
29:20	WO	xxh	Gamma Table Value for Writing R Channel at R = 10'h300
19:10	WO	xxh	Gamma Table Value for Writing G Channel at G = 10'h300
9:0	WO	xxh	Gamma Table Value for Writing B Channel at B = 10'h300

HParaType = 03h (HParaSubType = 17h), HParaAdr = 1Ch
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	Reserved
29:20	WO	xxh	Gamma Table Value for Writing R Channel at R = 10'h340
19:10	WO	xxh	Gamma Table Value for Writing G Channel at G = 10'h340
9:0	WO	xxh	Gamma Table Value for Writing B Channel at B = 10'h340

HPParaType = 03h (HPParaSubType = 17h), HPParaAdr = 1Dh
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	Reserved
29:20	WO	xxh	Gamma Table Value for Writing R Channel at R = 10'h380
19:10	WO	xxh	Gamma Table Value for Writing G Channel at G = 10'h380
9:0	WO	xxh	Gamma Table Value for Writing B Channel at B = 10'h380

HPParaType = 03h (HPParaSubType = 17h), HPParaAdr = 1Eh
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	Reserved
29:20	WO	xxh	Gamma Table Value for Writing R Channel at R = 10'h3C0
19:10	WO	xxh	Gamma Table Value for Writing G Channel at G = 10'h3C0
9:0	WO	xxh	Gamma Table Value for Writing B Channel at B = 10'h3C0

HPParaType = 03h (HPParaSubType = 20h-22h): Reserved

HPParaType = 03h (HPParaSubType = 30h)
Vertex Buffer (Multiple Streams) Base Address & Pitch

There are total 16 entries.

Bits	Attribute	Default	Description
31:10	WO	xxh	Vertex Buffer (Vertex Stream) Base Address for Data n <HVBnBase> In unit of 1024 bytes, where "n" is from 0 to F. Therefore there are at most 16 Vertex Data.
9	WO	xxh	Reserved
8:0	WO	xxh	Vertex Buffer (Vertex Stream) Pitch for Data n (in unit of 4 bytes)

HPParaType = 03h (HPParaSubType = 31h-33h): Reserved

HParaType 04h: Vertex and Primitive Setting

Sub-Address (Bits [31:24]): 00-AAh

HParaType = 04h, Sub-Address = 00h

Flexible Vertex Format and Multiple Streams 1

Bits [23:0]	Attribute	Default	Description
23:22	WO	xxh	Flexibility Vertex Format's (X, Y) Test Mode Test the VS's oPos. 00: Disable 01: If (X or Y is "Not-a-Number) then ignore corresponded <i>primitive</i> 1x: If (X or Y is "Not-a-Number) then ignore corresponded <i>primitive list</i>
21:20	WO	xxh	Flexibility Vertex Format's Z Test Mode Test the VS's oPos. 00: Disable 01: If (Z is "Not-a-Number) then ignore corresponded <i>primitive</i> 1x: If (Z is "Not-a-Number) then ignore corresponded <i>primitive list</i>
19:18	WO	xxh	Flexibility Vertex Format's W Test Mode Test the VS's oPos. 00: Disable 01: If (W is "Not-a-Number) then ignore corresponded <i>primitive</i> 1x: If (W is "Not-a-Number) then ignore corresponded <i>primitive list</i>
17	WO	xxh	Switch the Flexibility Vertex Format's X to Y, and Y to X Switch X, Y channel of VS's oPos. 0: Keep 1: Switch
16:15	WO	xxh	Location of Vertex Buffer 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: Reserved (System Memory) 11: Reserved (Local Memory Local Frame Buffer (L.L.))
14:12	WO	xxh	Reserved
11:8	WO	xxh	Number of Used Vertex Buffers Data in VS (or the Number of Input Registers Needed in VS) <HVBDNum> 0: VBD0 used 1: VBD0 & VBD1 used 2: VBD0, VBD1 & VBD2 used ... n: VBD0, VBD1 ...& VBDn used Maximum to 15 (16 vertex buffer datas used)
7	WO	xxh	Reserved
6:0	WO	xxh	Sum of All the Vertex Buffer Data According to HVBDNum & HVBD0FM In unit of 4 bytes.

HParaType = 04h, Sub-Address = 01h

Flexible Vertex Format and Multiple Streams 2

Bits [23:0]	Attribute	Default	Description
23:20	WO	xxh	Vertex Buffer ID of Vertex Data 0
19:12	WO	xxh	Offset for D0 to HVB0Base In unit of 4 bytes and max 255*4 bytes. Please refer to T03A30[31:10] HVBNBase, n represents 0, 1...etc.
11:8	WO	xxh	Indicate which "Input Registr" for the VB's D0 (1st Vertex Data) 0000: IR0 0001: IR1 ... 1111: IRf. This index indicates one of the 16 input register.
7:0	WO	xxh	Format of VB's D0 (1st Data) <HVBD0FM> Bits [7:6] Dimension 00: 1D and fill IR as (value0, 0, 0, 1) 01: 2D and fill IR as (value0, value1, 0, 1) 10: 3D and fill IR as (value0, value1, value2, 1) 11: 4D and fill IR as (value0, value1, value2, value3) Where "value" is transformed as 32-bit floating.

			<p>Bits [5:1] Format</p> <p>00000: Un-used and fill (x, y, z, w) as (0, 0, 0, 1)</p> <p>00001: 32-bit floating as $s[8].23(s[1.23]*2^{(8)-127})$ IR.x <= [31:0], IR.y <= [63:32], IR.z <= [95:64], IR.w <= [127:96]</p> <p>00010: 16-bit floating as $s[5].10(s[1.10]*2^{(5)-15})$ IR.x <= [15:0], IR.y <= [31:16], IR.z <= [47:32], IR.w <= [63:48]</p> <p>00011: Unsigned byte (8-bit, 0 to 255) IR.x <= [7:0], IR.y <= [15:8], IR.z <= [23:16], IR.w <= [31:24]</p> <p>00100: Unsigned short (16-bit, 0 to $2^{16} - 1$) IR.x <= [15:0], IR.y <= [31:16], IR.z <= [47:32], IR.w <= [63:48]</p> <p>00101: Short (16-bit, -2^{15} to $2^{15} - 1$) IR.x <= [15:0], IR.y <= [31:16], IR.z <= [47:32], IR.w <= [63:48]</p> <p>00110: Unsigned decade (10-bit, 0 to $2^{10} - 1$) IR.x <= [9:0], IR.y <= [19:10], IR.z <= [29:20], IR.w <= 1.0</p> <p>00111: Decade (10-bit, -2^9 to $2^9 - 1$) IR.x <= [9:0], IR.y <= [19:10], IR.z <= [29:20], IR.w <= 1.0</p> <p>01000: Color (8-bit, 0 to 255) IR.x <= [23:16], IR.y <= [15:8], IR.z <= [7:0], IR.w <= [31:24]</p> <p>Others: Reserved</p> <p>Bit [0] Normalize</p> <p>0: Disable</p> <p>1: Enable</p> <p style="padding-left: 20px;">For “unsigned byte” or “Color” value = value / 255</p> <ol style="list-style-type: none"> 1. Check if 1.0 or not(FFh). 2. Extension to {[7:0], [7:0], [7:0], [7:1]}. 3. Find leading one and LSH. <p style="padding-left: 20px;">For “unsigned short” value = value / ($2^{16} - 1$)</p> <ol style="list-style-type: none"> 1. Check if 1.0 or not(FFFFh). 2. Extension to {[15:0], [15:0], [15:9]}. 3. Find leading one and LSH. <p style="padding-left: 20px;">For “short” value = value / ($2^{15} - 1$)</p> <ol style="list-style-type: none"> 1. Determine sign by [15]. 2. Check if 1.0(7FFFh), -1.0(8000h or 8001h) or not. 3. Two’s complement if negative($\sim[14:0] + 1$). 4. Extension to {[14:0], [14:0], [14:7]}. 5. Find leading one and LSH. <p style="padding-left: 20px;">For “unsigned decade” value = value / 1023</p> <ol style="list-style-type: none"> 1. Check if 1.0 or not(3FFh). 2. Extension to {[9:0], [9:0], [9:0], [9:7]}. 3. Find leading one and LSH. <p style="padding-left: 20px;">For “decade” value = value / (511)</p> <ol style="list-style-type: none"> 1. Determine sign by [9]. 2. Check if 1.0(1FFh), -1.0(200h or 201h) or not. 3. Two’s complement if negative($\sim[8:0] + 1$). 4. Extension to {[8:0], [8:0], [8:0], [8:4]}. 5. Find leading one and LSH. <p>Note: Convert from D3DDECLTYPE to HVBD0FM and</p> <table style="margin-left: 20px;"> <tr><td>Float1</td><td>=></td><td>00 00001 0b</td></tr> <tr><td>Float2</td><td>=></td><td>01 00001 0b</td></tr> <tr><td>Float3</td><td>=></td><td>10 00001 0b</td></tr> <tr><td>Float4</td><td>=></td><td>11 00001 0b</td></tr> <tr><td>D3DColor</td><td>=></td><td>11 01000 1b</td></tr> <tr><td>UBYTE4</td><td>=></td><td>11 00011 0b</td></tr> <tr><td>UBYTE4N</td><td>=></td><td>11 00011 1b</td></tr> <tr><td>SHORT2</td><td>=></td><td>01 00101 0b</td></tr> <tr><td>SHORT4</td><td>=></td><td>11 00101 0b</td></tr> <tr><td>SHORT2N</td><td>=></td><td>01 00101 1b</td></tr> <tr><td>SHORT4N</td><td>=></td><td>11 00101 1b</td></tr> <tr><td>USHORT2N</td><td>=></td><td>01 00100 1b</td></tr> <tr><td>USHORT4N</td><td>=></td><td>11 00100 1b</td></tr> <tr><td>UDEC3</td><td>=></td><td>10 00110 0b</td></tr> </table>	Float1	=>	00 00001 0b	Float2	=>	01 00001 0b	Float3	=>	10 00001 0b	Float4	=>	11 00001 0b	D3DColor	=>	11 01000 1b	UBYTE4	=>	11 00011 0b	UBYTE4N	=>	11 00011 1b	SHORT2	=>	01 00101 0b	SHORT4	=>	11 00101 0b	SHORT2N	=>	01 00101 1b	SHORT4N	=>	11 00101 1b	USHORT2N	=>	01 00100 1b	USHORT4N	=>	11 00100 1b	UDEC3	=>	10 00110 0b
Float1	=>	00 00001 0b																																											
Float2	=>	01 00001 0b																																											
Float3	=>	10 00001 0b																																											
Float4	=>	11 00001 0b																																											
D3DColor	=>	11 01000 1b																																											
UBYTE4	=>	11 00011 0b																																											
UBYTE4N	=>	11 00011 1b																																											
SHORT2	=>	01 00101 0b																																											
SHORT4	=>	11 00101 0b																																											
SHORT2N	=>	01 00101 1b																																											
SHORT4N	=>	11 00101 1b																																											
USHORT2N	=>	01 00100 1b																																											
USHORT4N	=>	11 00100 1b																																											
UDEC3	=>	10 00110 0b																																											

			DEC3N	=>	10 00111 1b
			Float16_2	=>	01 00010 0b
			Float16_4	=>	11 00010 0b

HParaType = 04h, Sub-Address = 02h
Flexible Vertex Format and Multiple Streams 3

Bits [23:0]	Attribute	Default	Description
23:20	WO	xxh	Vertex Buffer ID of Vertex Data 1
19:12	WO	xxh	Offset for D1 to Related Base In unit of 4 bytes and max 255*4 bytes.
11:8	WO	xxh	Indicate which "Input Register" for the VB's D1 (2 nd Vertex Data)
7:0	WO	xxh	Format of VB's D1 (2 nd Data)

HParaType = 04h, Sub-Address = 03h
Flexible Vertex Format and Multiple Streams 4

Bits [23:0]	Attribute	Default	Description
23:20	WO	xxh	Vertex Buffer ID of Vertex Data 2
19:12	WO	xxh	Offset for D2 to Related Base In unit of 4 bytes and max 255*4 bytes.
11:8	WO	xxh	Indicate which "Input Register" for the VB's D2 (3 rd Vertex Data)
7:0	WO	xxh	Format of VB's D2 (3 rd Data)

HParaType = 04h, Sub-Address = 04h
Flexible Vertex Format and Multiple Streams 5

Bits [23:0]	Attribute	Default	Description
23:20	WO	xxh	Vertex Buffer ID of Vertex Data 3
19:12	WO	xxh	Offset for D3 to Related Base In unit of 4 bytes and max 255*4 bytes.
11:8	WO	xxh	Indicate which "Input Register" for the VB's D3 (4 th Vertex Data)
7:0	WO	xxh	Format of VB's D3 (4 th Data)

HParaType = 04h, Sub-Address = 05h
Flexible Vertex Format and Multiple Streams 6

Bits [23:0]	Attribute	Default	Description
23:20	WO	xxh	Vertex Buffer ID of Vertex Data 4
19:12	WO	xxh	Offset for D4 to Related Base In unit of 4 bytes and max 255*4 bytes.
11:8	WO	xxh	Indicate which "Input Register" for the VB's D4 (5 th Vertex Data)
7:0	WO	xxh	Format of VB's D4 (5 th Data)

HParaType = 04h, Sub-Address = 06h
Flexible Vertex Format and Multiple Streams 7

Bits [23:0]	Attribute	Default	Description
23:20	WO	xxh	Vertex Buffer ID of Vertex Data 5
19:12	WO	xxh	Offset for D5 to Related Base In unit of 4 bytes and max 255*4 bytes.
11:8	WO	xxh	Indicate which "Input Register" for the VB's D5 (6 th Vertex Data)
7:0	WO	xxh	Format of VB's D5 (6 th Data)

HParaType = 04h, Sub-Address = 07h
Flexible Vertex Format and Multiple Streams 8

Bits [23:0]	Attribute	Default	Description
23:20	WO	xxh	Vertex Buffer ID of Vertex Data 6
19:12	WO	xxh	Offset for D6 to Related Base In unit of 4 bytes and max 255*4 bytes.
11:8	WO	xxh	Indicate which "Input Register" for the VB's D6 (7 th Vertex Data)
7:0	WO	xxh	Format of VB's D6 (7 th Data)

HParaType = 04h, Sub-Address = 08h
Flexible Vertex Format and Multiple Streams 9

Bits [23:0]	Attribute	Default	Description
23:20	WO	xxh	Vertex Buffer ID of Vertex Data 7
19:12	WO	xxh	Offset for D7 to Related Base In unit of 4 bytes and max 255*4 bytes.
11:8	WO	xxh	Indicate which "Input Register" for the VB's D7 (8 th Vertex Data)
7:0	WO	xxh	Format of VB's D7 (8 th Data)

HParaType = 04h, Sub-Address = 09h
Flexible Vertex Format and Multiple Streams 10

Bits [23:0]	Attribute	Default	Description
23:20	WO	xxh	Vertex Buffer ID of Vertex Data 8
19:12	WO	xxh	Offset for D8 to Related Base In unit of 4 bytes and max 255*4 bytes.
11:8	WO	xxh	Indicate which "Input Register" for the VB's D8 (9 th Vertex Data)
7:0	WO	xxh	Format of VB's D8 (9 th Data)

HParaType = 04h, Sub-Address = 0Ah
Flexible Vertex Format and Multiple Streams 11

Bits [23:0]	Attribute	Default	Description
23:20	WO	xxh	Vertex Buffer ID of Vertex Data 9
19:12	WO	xxh	Offset for D9 to Related Base In unit of 4 bytes and max 255*4 bytes.
11:8	WO	xxh	Indicate which "Input Register" for the VB's D9 (10 th Vertex Data)
7:0	WO	xxh	Format of VB's D9 (10 th Data)

HParaType = 04h, Sub-Address 0Bh
Flexible Vertex Format and Multiple Streams 12

Bits [23:0]	Attribute	Default	Description
23:20	WO	xxh	Vertex Buffer ID of Vertex Data A
19:12	WO	xxh	Offset for DA to Related Base In unit of 4 bytes and max 255*4 bytes.
11:8	WO	xxh	Indicate which "Input Register" for the VB's DA (11 th Vertex Data)
7:0	WO	xxh	Format of VB's DA (11 th Data)

HParaType = 04h, Sub-Address = 0Ch
Flexible Vertex Format and Multiple Streams 13

Bits [23:0]	Attribute	Default	Description
23:20	WO	xxh	Vertex Buffer ID of Vertex Data B
19:12	WO	xxh	Offset for DB to Related Base In unit of 4 bytes and max 255*4 bytes.
11:8	WO	xxh	Indicate which "Input Register" for the VB's DB (12 th Vertex Data)
7:0	WO	xxh	Format of VB's DB (12 th Data)

HParaType = 04h, Sub-Address = 0Dh
Flexible Vertex Format and Multiple Streams 14

Bits [23:0]	Attribute	Default	Description
23:20	WO	xxh	Vertex Buffer ID of Vertex Data C
19:12	WO	xxh	Offset for DC to Related Base In unit of 4 bytes and max 255*4 bytes.
11:8	WO	xxh	Indicate which "Input Register" for the VB's DC (13 th Vertex Data)
7:0	WO	xxh	Format of VB's DC (13 th Data)

HParaType = 04h, Sub-Address = 0Eh
Flexible Vertex Format and Multiple Streams 15

Bits [23:0]	Attribute	Default	Description
23:20	WO	xxh	Vertex Buffer ID of Vertex Data D
19:12	WO	xxh	Offset for DD to Related Base In unit of 4 bytes and max 255*4 bytes.
11:8	WO	xxh	Indicate which "Input Register" for the VB's DD (14 th Vertex Data)
7:0	WO	xxh	Format of VB's DD (14 th Data)

HParaType = 04h, Sub-Address = 0Fh
Flexible Vertex Format and Multiple Streams 16

Bits [23:0]	Attribute	Default	Description
23:20	WO	xxh	Vertex Buffer ID of Vertex Data E
19:12	WO	xxh	Offset for DE to Related Base In unit of 4 bytes and max 255*4 bytes.
11:8	WO	xxh	Indicate which "Input Register" for the VB's DE (15 th Vertex Data)
7:0	WO	xxh	Format of VB's DE (15 th Data)

HParaType = 04h, Sub-Address = 10h
Flexible Vertex Format and Multiple Streams 17

Bits [23:0]	Attribute	Default	Description
23:20	WO	xxh	Vertex Buffer ID of Vertex Data F
19:12	WO	xxh	Offset for DF to Related Base In unit of 4 bytes and max 255*4 bytes.
11:8	WO	xxh	Indicate which "Input Register" for the VB's DF (16 th Vertex Data)
7:0	WO	xxh	Format of VB's DF (16 th Data)

HParaType = 04h, Sub-Address = 11h: Reserved (Flexible Vertex Format and Multiple Streams 18)

HParaType = 04h, Sub-Address = 12h
Flexible Vertex Format and Multiple Streams 19

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	Reserved
15	WO	xxh	The 16th Input Register(IRf) is filled from Some VB Data 0: The Input Register should be default value (0, 0, 0, 1) 1: The Input Register is filled from VB
14	WO	xxh	The 15th Input Register(IRE) is filled from Some VB Data 0: The Input Register should be default value (0, 0, 0, 1) 1: The Input Register is filled from VB
13	WO	xxh	The 14th Input Register(IRd) is filled from Some VB Data 0: The Input Register should be default value (0, 0, 0, 1) 1: The Input Register is filled from VB
12	WO	xxh	The 13th Input Register(IRC) is filled from Some VB Data 0: The Input Register should be default value (0, 0, 0, 1) 1: The Input Register is filled from VB
11	WO	xxh	The 12th Input Register(IRb) is filled from Some VB Data 0: The Input Register should be default value (0, 0, 0, 1) 1: The Input Register is filled from VB
10	WO	xxh	The 11th Input Register(IRa) is filled from Some VB Data 0: The Input Register should be default value (0, 0, 0, 1) 1: The Input Register is filled from VB
9	WO	xxh	The 10th Input Register(IR9) is filled from Some VB Data 0: The Input Register should be default value (0, 0, 0, 1) 1: The Input Register is filled from VB
8	WO	xxh	The 9th Input Register(IR8) is filled from Some VB Data 0: The Input Register should be default value (0, 0, 0, 1) 1: The Input Register is filled from VB
7	WO	xxh	The 8th Input Register(IR7) is filled from Some VB Data 0: The Input Register should be default value (0, 0, 0, 1) 1: The Input Register is filled from VB
6	WO	xxh	The 7th Input Register(IR6) is filled from Some VB Data 0: The Input Register should be default value (0, 0, 0, 1) 1: The Input Register is filled from VB
5	WO	xxh	The 6th Input Register(IR5) is filled from Some VB Data 0: The Input Register should be default value (0, 0, 0, 1) 1: The Input Register is filled from VB
4	WO	xxh	The 5th Input Register(IR4) is filled from Some VB Data 0: The Input Register should be default value (0, 0, 0, 1) 1: The Input Register is filled from VB
3	WO	xxh	The 4th Input Register(IR3) is filled from Some VB Data 0: The Input Register should be default value (0, 0, 0, 1) 1: The Input Register is filled from VB
2	WO	xxh	The 3rd Input Register(IR2) is filled from Some VB Data 0: The Input Register should be default value (0, 0, 0, 1) 1: The Input Register is filled from VB
1	WO	xxh	The 2nd Input Register(IR1) is filled from Some VB Data 0: The Input Register should be default value (0, 0, 0, 1) 1: The Input Register is filled from VB
0	WO	xxh	The 1st Input Register(IR0) is filled from Some VB Data 0: The Input Register should be default value (0, 0, 0, 1) 1: The Input Register is filled from VB

HParaType = 04h, Sub-Address = 13h-1F: Reserved

HParaType = 04h, Sub-Address = 20h
Vertex Buffer & Primitive Setting 1

Bits [23:0]	Attribute	Default	Description
23:22	WO	xxh	Reserved
21:16	WO	xxh	The Setting of Second or Even One-vertex Triangle <H2nd1VT> <u>Bit [21:20]: Setting of Vertex A</u> This setting is used for both triangle and line rendering. 00: Vertex a is a new input 01: The Vertex a will be replaced by previous Vertex a. 10: The Vertex a will be replaced by previous Vertex b. 11: The Vertex a will be replaced by previous Vertex c. <u>Bit [19:18] Setting of Vertex B</u> This setting is used for both triangle and line rendering. 00: Vertex b is a new input 01: The Vertex b will be replaced by previous Vertex a. 10: The Vertex b will be replaced by previous Vertex b. 11: The Vertex b will be replaced by previous Vertex c. <u>Bit [17:16] Setting of Vertex C</u> This setting is used for both triangle and line rendering. 00: Vertex c is a new input 01: The Vertex c will be replaced by previous Vertex a. 10: The Vertex c will be replaced by previous Vertex b. 11: The Vertex c will be replaced by previous Vertex c.
15:8	WO	xxh	Primitive Render Mode 00000000: Full Vertex Cycle For Triangle Rendering, this is the 3 vertexes cycle. For Line Rendering, this is the 2 vertexes cycle. 10xxxxxx: Reserved x1xxxxxx: Automatic Fast Primitive Vertex Cycle For Triangle Rendering, this is a fast way to render 3111 Mode For Line Rendering, this is a fast way to render 2111 Mode The first or odd single vertex cycle will use the setting of bit [5:0]. The second or even single vertex cycle will use the setting of H2nd1VT. <u>Bit [13:12] Setting of Vertex A</u> This setting is used for both triangle and line rendering. 00: Vertex a is a new input 01: The Vertex a will be replaced by previous Vertex a. 10: The Vertex a will be replaced by previous Vertex b. 11: The Vertex a will be replaced by previous Vertex c. <u>Bit [11:10] Setting of Vertex B</u> This setting is used for both triangle and line rendering. 00: Vertex b is a new input 01: The Vertex b will be replaced by previous Vertex a. 10: The Vertex b will be replaced by previous Vertex b. 11: The Vertex b will be replaced by previous Vertex c. <u>Bit [9:8] Setting of Vertex C</u> This setting is used for both triangle and line rendering. 00: Vertex c is a new input 01: The Vertex c will be replaced by previous Vertex a. 10: The Vertex c will be replaced by previous Vertex b. 11: The Vertex c will be replaced by previous Vertex c.
7:2	WO	xxh	Reserved
1	WO	xxh	Vertex Buffer Index Mode 0: 16-bit index 1: 32-bit index
0	WO	xxh	Vertex Mode 0: Command mode Vertex 1: Index mode Vertex

HParaType = 04h, Sub-Address = 21h-22F: Reserved

HParaType = 04h, Sub-Address = 23h
Vertex Buffer & Primitive Setting 4

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	Disable Clipping for Triangle Point (Just Near Plane) 0: Enable 1: Disable
22	WO	xxh	Enable Clipping By Plane W = 0 0: Enable (Default) 1: Disable Note: Consider a special, a primitive whose vertices' Z are all positive, but Ws are positive and negative. Original design just clip by the plane, Z = 0, can not handle this case. The clip by the plane, W = 0, is added into our design. This register is used to disable this newly added function.
21	WO	0	Enable Clipping Engine ECO on CL2_V0OCLAT (Clipping Engine's Vertex0 Output and Color Window Compare Result) 0: Enable (Default) 1: Disable
20	WO	0	Enable Clipping Engine ECO on T0_X10 (Temp Xb-Xa Result) / T0_Y10 (Temp Yb-Ya Result) 0: Enable (Default) 1: Disable
19	WO	0	Enable 3D ECO on E3IDLE (3D Engine Idle) 0: Enable (Default) 1: Disable
18:16	WO	xxh	Reserved
15	WO	xxh	Last Pixel Control for Drawing Line 0: Discard the last pixel of each line 1: Draw the last pixel of each line
14:12	WO	xxh	Shading Setting 000: Solid shading 001: Flat shading via Vertex a 010: Flat shading via Vertex b 011: Flat shading via Vertex c 100: Gouraud shading
11:9	WO	xxh	Edge Flag Assume the vertex transmission sequence of a triangle is a, b, then c. 000: Render NO Edge for triangle wire-frame or antialiasing 1xx: Render Edge (a, b) for triangle wire-frame or antialiasing x1x: Render Edge (b, c) for triangle wire-frame or antialiasing xx1: Render Edge (c, a) for triangle wire-frame or antialiasing
8	WO	xxh	Back Face Mode for "Culling" 0: If the vertex input is in the order of clockwise, it would be "culled" 1: If the vertex input is in the order of counterclockwise, it would be "culled"
7	WO	xxh	Back Face Mode for VS's Output "oBFD#" 0: If the vertex input is in the order of clockwise, "oBFD#" would be selected as the vertex color 1: If the vertex input is in the order of counterclockwise, "oBFD#" would be selected as the vertex color
6:5	WO	xxh	Primitive Type for Clockwise Triangle 00: Triangle Rendering for Hen2FRender enabled and clockwise primitive 01: Reserved 10: Triangle Wire-frame Rendering for Hen2FRender enabled and clockwise primitive 11: Triangle Point Rendering for Hen2FRender enabled and clockwise primitive
4	WO	xxh	Render Mode (PMTYPE) Is Different for Front-Face and Back-Face Primitive <Hen2FRender> The related PMType is "Triangle", "Triangle Wire-Frame" and "Triangle Point". 0: The PMTypes for both front-face and back-face are the same, or only one kind of face is rendered. 1: The PMType is different for front-face and back-face primitive.
3:0	WO	xxh	Primitive Type 0000: Point Rendering 0001: Line Rendering 0010: Triangle Rendering for "Hen2Frender" is false, or Hen2Frender enabled and counter-clockwise primitive 0011: Reserved 0100: Rectangle 0101: Reserved 0110: Triangle Wire-frame Rendering for "Hen2Frender" is false, or Hen2Frender enabled and counter-clockwise primitive 0111: Triangle Point Rendering for "Hen2Frender" is false, or Hen2Frender enabled and counter-clockwise primitive 1xxx: Reserved

HParaType = 04h, Sub-Address = 24
Vertex Buffer & Primitive Setting 5

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Vertexes Number n: There are n vertexes in current primitive list.

HParaType = 04h, Sub-Address = 25h
Vertex Buffer & Primitive Setting 6

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	<p>Flexible Vertex Format Mask</p> <p><u>Bit [23]: X Parameter Mask</u> 0: Primitive Vertex Parameter does not have X 1: Primitive Vertex Parameter has X</p> <p><u>Bit [22]: Y Parameter Mask</u> 0: Primitive Vertex Parameter does not have Y 1: Primitive Vertex Parameter has Y</p> <p><u>Bit [21]: Z Parameter Mask</u> 0: Primitive Vertex Parameter does not have Z 1: Primitive Vertex Parameter has Z</p> <p><u>Bit [20]: W Parameter Mask</u> 0: Primitive Vertex Parameter does not have W 1: Primitive Vertex Parameter has W</p> <p><u>Bit [19]: Point-Size Parameter Mask</u> 0: Primitive Vertex Parameter does not have Point-Size If the primitive type is point, use HVPointSize. 1: Primitive Vertex Parameter has Point-Size If the primitive type is point, use the value from Vertex Data.</p> <p><u>Bit [18]: Cd(C0) Parameter Mask</u> 0: Primitive Vertex Parameter does not have Diffuse Color, ARGB 1: Primitive Vertex Parameter has Diffuse Color, ARGB</p> <p><u>Bit [17]: Cs(C1) Parameter Mask</u> 0: Primitive Vertex Parameter does not have Specula Color, SR SG SB, and SA 1: Primitive Vertex Parameter has Specula Color, SR SG SB, and SA</p> <p><u>Bit [16]: Fog-Factor Parameter Mask</u> 0: Primitive Vertex Parameter does not have Fog Factor 1: Primitive Vertex Parameter has Fog Factor</p> <p><u>Bit [15]: Texture A's S Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate S 1: Primitive Vertex Parameter has Texture Coordinate S</p> <p><u>Bit [14]: Texture A's T Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate T 1: Primitive Vertex Parameter has Texture Coordinate T</p> <p><u>Bit [13]: Texture A's R Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate R 1: Primitive Vertex Parameter has Texture Coordinate R</p> <p><u>Bit [12]: Texture A's Q Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate Q 1: Primitive Vertex Parameter has Texture Coordinate Q</p> <p><u>Bit [11]: Texture B's S Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate S 1: Primitive Vertex Parameter has Texture Coordinate S</p> <p><u>Bit [10]: Texture B's T Parameter Mask</u></p>

		<p>0: Primitive Vertex Parameter does not have Texture Coordinate T 1: Primitive Vertex Parameter has Texture Coordinate T</p> <p><u>Bit [9]: Texture B's R Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate R 1: Primitive Vertex Parameter has Texture Coordinate R</p> <p><u>Bit [8]: Texture B's Q Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate Q 1: Primitive Vertex Parameter has Texture Coordinate Q</p> <p><u>Bit [7]: Texture C's S Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate S 1: Primitive Vertex Parameter has Texture Coordinate S</p> <p><u>Bit [6]: Texture C's T Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate T 1: Primitive Vertex Parameter has Texture Coordinate T</p> <p><u>Bit [5]: Texture C's R Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate R 1: Primitive Vertex Parameter has Texture Coordinate R</p> <p><u>Bit [4]: Texture C's Q Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate Q 1: Primitive Vertex Parameter has Texture Coordinate Q</p> <p><u>Bit [3]: Texture D's S Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate S 1: Primitive Vertex Parameter has Texture Coordinate S</p> <p><u>Bit [2]: Texture D's T Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate T 1: Primitive Vertex Parameter has Texture Coordinate T</p> <p><u>Bit [1]: Texture D's R Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate R 1: Primitive Vertex Parameter has Texture Coordinate R</p> <p><u>Bit [0]: Texture D's Q Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate Q 1: Primitive Vertex Parameter has Texture Coordinate Q</p>
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HParaType = 04h, Sub-Address = 26h
Vertex Buffer & Primitive Setting 7

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	Flexible Vertex Format Mask Bit [23]: Texture I's S Parameter Mask 0: Primitive Vertex Parameter does not have Texture Coordinate S 1: Primitive Vertex Parameter has Texture Coordinate S Bit [22]: Texture I's T Parameter Mask 0: Primitive Vertex Parameter does not have Texture Coordinate T 1: Primitive Vertex Parameter has Texture Coordinate T Bit [21]: Texture I's R Parameter Mask 0: Primitive Vertex Parameter does not have Texture Coordinate R 1: Primitive Vertex Parameter has Texture Coordinate R Bit [20]: Texture I's Q Parameter Mask 0: Primitive Vertex Parameter does not have Texture Coordinate Q 1: Primitive Vertex Parameter has Texture Coordinate Q Bit [19]: Texture J's S Parameter Mask 0: Primitive Vertex Parameter does not have Texture Coordinate S 1: Primitive Vertex Parameter has Texture Coordinate S Bit [18]: Texture J's T Parameter Mask 0: Primitive Vertex Parameter does not have Texture Coordinate T 1: Primitive Vertex Parameter has Texture Coordinate T Bit [17]: Texture J's R Parameter Mask 0: Primitive Vertex Parameter does not have Texture Coordinate R 1: Primitive Vertex Parameter has Texture Coordinate R Bit [16]: Texture J's Q Parameter Mask 0: Primitive Vertex Parameter does not have Texture Coordinate Q 1: Primitive Vertex Parameter has Texture Coordinate Q
15:0	WO	xxh	Flexible Vertex Format Mask Bit [15]: Texture E's S Parameter Mask 0: Primitive Vertex Parameter does not have Texture Coordinate S 1: Primitive Vertex Parameter has Texture Coordinate S Bit [14]: Texture E's T Parameter Mask 0: Primitive Vertex Parameter does not have Texture Coordinate T 1: Primitive Vertex Parameter has Texture Coordinate T Bit [13]: Texture E's R Parameter Mask 0: Primitive Vertex Parameter does not have Texture Coordinate R 1: Primitive Vertex Parameter has Texture Coordinate R Bit [12]: Texture E's Q Parameter Mask 0: Primitive Vertex Parameter does not have Texture Coordinate Q 1: Primitive Vertex Parameter has Texture Coordinate Q Bit [11]: Texture F's S Parameter Mask 0: Primitive Vertex Parameter does not have Texture Coordinate S 1: Primitive Vertex Parameter has Texture Coordinate S Bit [10]: Texture F's T Parameter Mask 0: Primitive Vertex Parameter does not have Texture Coordinate T 1: Primitive Vertex Parameter has Texture Coordinate T Bit [9]: Texture F's R Parameter Mask 0: Primitive Vertex Parameter does not have Texture Coordinate R 1: Primitive Vertex Parameter has Texture Coordinate R Bit [8]: Texture F's Q Parameter Mask 0: Primitive Vertex Parameter does not have Texture Coordinate Q

		<p>1: Primitive Vertex Parameter has Texture Coordinate Q</p> <p><u>Bit [7]: Texture G's S Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate S 1: Primitive Vertex Parameter has Texture Coordinate S</p> <p><u>Bit [6]: Texture G's T Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate T 1: Primitive Vertex Parameter has Texture Coordinate T</p> <p><u>Bit [5]: Texture G's R Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate R 1: Primitive Vertex Parameter has Texture Coordinate R</p> <p><u>Bit [4]: Texture G's Q Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate Q 1: Primitive Vertex Parameter has Texture Coordinate Q</p> <p><u>Bit [3]: Texture H's S Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate S 1: Primitive Vertex Parameter has Texture Coordinate S</p> <p><u>Bit [2]: Texture H's T Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate T 1: Primitive Vertex Parameter has Texture Coordinate T</p> <p><u>Bit [1]: Texture H's R Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate R 1: Primitive Vertex Parameter has Texture Coordinate R</p> <p><u>Bit [0]: Texture H's O Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate Q 1: Primitive Vertex Parameter has Texture Coordinate Q</p>
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HParaType = 04h, Sub-Address = 27h
Vertex Buffer & Primitive Setting 8

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Starting Primitive Count

HParaType = 04h, Sub-Address = 28h
Vertex Buffer & Primitive Setting 9

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	<p>Vertex Parameter Mask <i>Note that the “(**)” is controlled by HVPDV_XX’s Setting</i></p> <p>Bit [23]: X Parameter Mask 0: Primitive Vertex Parameter does not have X thus use default value 0.0 1: Primitive Vertex Parameter has X</p> <p>Bit [22]: Y Parameter Mask 0: Primitive Vertex Parameter does not have Y thus use default value 0.0 1: Primitive Vertex Parameter has Y</p> <p>Bit [21]: Z Parameter Mask 0: Primitive Vertex Parameter does not have Z thus use default value (**) 1: Primitive Vertex Parameter has Z</p> <p>Bit [20]: W Parameter Mask 0: Primitive Vertex Parameter does not have W thus use default value (**) 1: Primitive Vertex Parameter has W</p> <p>Bit [19]: Reserved</p> <p>Bit [18]: Cd (C0) Parameter Mask 0: Primitive Vertex Parameter does not have Diffuse Color, ARGB thus use default value (**) 1: Primitive Vertex Parameter has Diffuse Color, ARGB</p> <p>Bit [17]: Cs (C1) Parameter Mask 0: Primitive Vertex Parameter does not have Specula Color, SR SG SB, and SA thus use default value (**) 1: Primitive Vertex Parameter has Specula Color, SR SG SB, and SA</p> <p>Bit [16]: Fog-Factor Parameter Mask 0: Primitive Vertex Parameter does not have Fog Factor thus use default value (**) 1: Primitive Vertex Parameter has Fog Factor</p> <p>Bit [15]: Texture 0’s S Parameter Mask 0: Primitive Vertex Parameter does not have Texture Coordinate S thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate S</p> <p>Bit [14]: Texture 0’s T Parameter Mask 0: Primitive Vertex Parameter does not have Texture Coordinate T thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate T</p> <p>Bit [13]: Texture 0’s R Parameter Mask 0: Primitive Vertex Parameter does not have Texture Coordinate R thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate R</p> <p>Bit [12]: Texture 0’s Q Parameter Mask 0: Primitive Vertex Parameter does not have Texture Coordinate Q thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate Q</p> <p>Bit [11]: Texture 1’s S Parameter Mask 0: Primitive Vertex Parameter does not have Texture Coordinate S thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate S</p> <p>Bit [10]: Texture 1’s T Parameter Mask 0: Primitive Vertex Parameter does not have Texture Coordinate T thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate T</p>

		<p><u>Bit [9]: Texture 1's R Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate R thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate R</p> <p><u>Bit [8]: Texture 1's Q Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate Q thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate Q</p> <p><u>Bit [7]: Texture 2's S Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate S thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate S</p> <p><u>Bit [6]: Texture 2's T Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate T thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate T</p> <p><u>Bit [5]: Texture 2's R Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate R thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate R</p> <p><u>Bit [4]: Texture 2's Q Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate Q thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate Q</p> <p><u>Bit [3]: Texture 3's S Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate S thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate S</p> <p><u>Bit [2]: Texture 3's T Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate T thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate T</p> <p><u>Bit [1]: Texture 3's R Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate R thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate R</p> <p><u>Bit [0]: Texture 3's Q Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate Q thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate Q</p>
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HParaType = 04h, Sub-Address = 29h
Vertex Buffer & Primitive Setting 10

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	Reserved
15:0	WO	xxh	<p>Vertex Parameter Mask <i>Note that the “(**)” is controlled by HVPDV_XX’s Setting</i></p> <p><u>Bit [15]: Texture 4’s S Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate S thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate S</p> <p><u>Bit [14]: Texture 4’s T Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate T thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate T</p> <p><u>Bit [13]: Texture 4’s R Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate R thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate R</p> <p><u>Bit [12]: Texture 4’s Q Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate Q thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate Q</p> <p><u>Bit [11]: Texture 5’s S Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate S thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate S</p> <p><u>Bit [10]: Texture 5’s T Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate T thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate T</p> <p><u>Bit [9]: Texture 5’s R Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate R thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate R</p> <p><u>Bit [8]: Texture 5’s Q Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate Q thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate Q</p> <p><u>Bit [7]: Texture 6’s S Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate S thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate S</p> <p><u>Bit [6]: Texture 6’s T Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate T thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate T</p> <p><u>Bit [5]: Texture 6’s R Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate R thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate R</p> <p><u>Bit [4]: Texture 6’s Q Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate Q thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate Q</p> <p><u>Bit [3]: Texture 7’s S Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate S thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate S</p> <p><u>Bit [2]: Texture 7’s T Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate T thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate T</p> <p><u>Bit [1]: Texture 7’s R Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate R thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate R</p> <p><u>Bit [0]: Texture 7’s Q Parameter Mask</u> 0: Primitive Vertex Parameter does not have Texture Coordinate Q thus use default value (**)</p>

			1: Primitive Vertex Parameter has Texture Coordinate Q
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HParaType = 04h, Sub-Address = 2Ah
Vertex Buffer & Primitive Setting 11

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Point's Default Width as Floating s[8].15 When point size comes from FVF, this setting is as the maximum value of point size. Point Sprite is not only useful for 3D AP, but also for 2D and video AP. This can be considered as just filled a rectangle and make use of all those 3D features at the same time. The maximum value is 2048.0. The minimum value is 1.0. If (HFVFMask of "point size" is "0", and primitive type is point) Point_width = HVPointW Else Point_width = max(HVPointH, min(HVPointW, value from Primitive Vertex data's "point_size"))

HParaType = 04h, Sub-Address = 2Bh
Vertex Buffer & Primitive Setting 12

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Point's Default Hight as Floating s[8].15 When point size comes from FVF, this setting is as the minimum value of point size. The maximum value is 2048.0. The minimum value is 1.0.

HParaType = 04h, Sub-Address = 2Ch
Vertex Buffer & Primitive Setting 13

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Lower 24 Bits for Maximum Value of Vertex Buffer's Index

HParaType = 04h, Sub-Address = 2Dh
Vertex Buffer & Primitive Setting 14

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Lower 24 Bits for Minimum Value of Vertex Buffer's Index

HParaType = 04h, Sub-Address = 2Eh
Vertex Buffer & Primitive Setting 15

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	Reserved
15:8	WO	xxh	Higher 8 Bits for Maximum Value of Vertex Buffer's Index
7:0	WO	xxh	Higher 8 Bits for Minimum Value of Vertex Buffer's Index If (index of vertex > HVBIndexMax index of vertex < HVBIndexMin) Ignore this and the followed indices

HParaType = 04h, Sub-Address = 2Fh
Vertex Buffer & Primitive Setting 16

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	Default Value for Vertex Parameter Z 0: Default value is 0.0 1: Default value is 1.0
22	WO	xxh	Default Value for Vertex Parameter W 0: Default value is 0.0 1: Default value is 1.0
21	WO	xxh	Default Value for Vertex Parameter Fog 0: Default value is 0.0 1: Default value is 1.0
20	WO	xxh	Default Value for Vertex Parameter Color 0 0: Default value is 0.0 1: Default value is 1.0
19	WO	xxh	Default Value for Vertex Parameter Alpha 0 0: Default value is 0.0 1: Default value is 1.0
18	WO	xxh	Default Value for Vertex Parameter Color 1 0: Default value is 0.0 1: Default value is 1.0
17	WO	xxh	Default Value for Vertex Parameter Alpha 1 0: Default value is 0.0 1: Default value is 1.0
16	WO	xxh	Default Value for Vertex Parameter Texture Coordinate S 0: Default value is 0.0 1: Default value is 1.0
15	WO	xxh	Default Value for Vertex Parameter Texture Coordinate T 0: Default value is 0.0 1: Default value is 1.0
14	WO	xxh	Default Value for Vertex Parameter Texture Coordinate R 0: Default value is 0.0 1: Default value is 1.0
13	WO	xxh	Default Value for Vertex Parameter Texture Coordinate Q 0: Default value is 0.0 1: Default value is 1.0
12:10	WO	xxh	Reserved
9	WO	xxh	Point Sprite Enable for Texture J 0: Disable 1: Enable
8	WO	xxh	Point Sprite Enable for Texture I 0: Disable 1: Enable
7	WO	xxh	Point Sprite Enable for Texture H 0: Disable 1: Enable
6	WO	xxh	Point Sprite Enable for Texture G 0: Disable 1: Enable
5	WO	xxh	Point Sprite Enable for Texture F 0: Disable 1: Enable
4	WO	xxh	Point Sprite Enable for Texture E 0: Disable 1: Enable
3	WO	xxh	Point Sprite Enable for Texture D 0: Disable 1: Enable
2	WO	xxh	Point Sprite Enable for Texture C 0: Disable 1: Enable
1	WO	xxh	Point Sprite Enable for Texture B 0: Disable 1: Enable
0	WO	xxh	Point Sprite Enable for Texture A 0: Disable 1: Enable

HParaType = 04h, Sub-Address = 30-3Fh: Reserved (for Vertex Buffer & Primitive Setting)

HParaType = 04h, Sub-Address = 40-52h: Clipping Window to Screen Window Transformation Setting

All the transforming coefficients are 32-bit floating-point.

Notes to Driver:

1. Driver has to set the C-to-S transform scaling factor to both "HC2SxScale"(where x is X, Y & Z) and HVSCnstReg's c256. HVSCnstReg's c256 is used in VS and "HC2SxScale" is used in Clipping Engine.
2. Driver has to set the C-to-S transform offset factor to both "HC2SxOffset"(where x is X, Y & Z) and HVSCnstReg's c257. HVSCnstReg's c257 is used in VS and "HC2SxOffset" is used in Clipping Engine.

HParaType = 04h, Sub-Address = 40h

Clipping Window to Screen Window Transformation Setting 1

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Lower 3 Bytes of Scaling for X Transform

HParaType = 04h, Sub-Address = 41h

Clipping Window to Screen Window Transformation Setting 2

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Lower 3 Bytes of Offset for X Transform

HParaType = 04h, Sub-Address = 42h

Clipping Window to Screen Window Transformation Setting 3

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	Reserved
15:8	WO	xxh	Higher Byte of Offset for X Transform
7:0	WO	xxh	Higher Byte of Scaling for X Transform

HParaType = 04h, Sub-Address = 43h

Clipping Window to Screen Window Transformation Setting 4

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Lower 3 Bytes of Scaling for Y Transform

HParaType = 04h, Sub-Address = 44h:

Clipping Window to Screen Window Transformation Setting 5

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Lower 3 Bytes of Offset for Y Transform

HParaType = 04h, Sub-Address = 45h

Clipping Window to Screen Window Transformation Setting 6

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	Reserved
15:8	WO	xxh	Higher Byte of Offset for Y Transform
7:0	WO	xxh	Higher Byte of Scaling for Y Transform

HParaType = 04h, Sub-Address = 46h
Clipping Window to Screen Window Transformation Setting 7

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Lower 3 Bytes of Scaling for Z Transform

HParaType = 04h, Sub-Address = 47h
Clipping Window to Screen Window Transformation Setting 8

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Lower 3 Bytes of Offset for Z Transform

HParaType = 04h, Sub-Address = 48h
Clipping Window to Screen Window Transformation Setting 9

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	A Threshold Value For More Accurate Area Calculating <HC2SXYEmax4Area > A threshold value of screen coordinate's Exponential part for more accurate area calculation. If any screen coordinate's expomntial is over "HC2SXYEmax4Area", the area calculating equation would be $XbYc - XbYa - XaYc - XcYb + XcYa + XaYb$. And add each term in the order from absolute largest to the absolute smallest.
15:8	WO	xxh	Higher Byte of Offset for Z Transform
7:0	WO	xxh	Higher Byte of Scaling for Z Transform

HParaType = 04h, Sub-Address = 49-4Fh: Reserved (for Clipping Window to Screen Window Transformation Setting)

HParaType = 04h, Sub-Address = 50h
Clipping Window to Screen Window Transformation Setting 10

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Lower 3 Bytes of Upper Clamping Value for Screen Coordinate

HParaType = 04h, Sub-Address = 51h
Clipping Window to Screen Window Transformation Setting 11

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Lower 3 Bytes of Down Clamping Value for Screen Coordinate

HParaType = 04h, Sub-Address = 52h
Clipping Window to Screen Window Transformation Setting 12

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	Maximum Exponential Value Clipped Screen Coordinate <HC2SXYE _{max4CL} > If the clipped new vertex's screen coordinate is over $\pm 2^{\wedge} \text{HC2SXYE}_{\text{max4CL}}$, re-generate this clipped vertex to a smaller screen coordinate.
15:8	WO	xxh	Higher Byte of Upper Clamping Value for Screen Coordinate
7:0	WO	xxh	Higher Byte of Down Clamping Value for Screen Coordinate If ($X_s \geq \text{HC2SXYUClamp}$) $X_s = \text{HC2SXYUClamp}$ Else if ($X_s \leq \text{HC2SXYDClamp}$) $X_s = * \text{HC2SXYDClamp}$ If ($Y_s \geq \text{HC2SXYUClamp}$) $Y_s = \text{HC2SXYUClamp}$ Else if ($Y_s \leq \text{HC2SXYDClamp}$) $Y_s = \text{HC2SXYDClamp}$

HParaType = 04h, Sub-Address = 53-62h: Reserved
HParaType = 04h, Sub-Address AAh
Software Inspection

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	Reserved
15:0	WO	xxh	Flag Number for SW Inspection

HParaType 08h: CDC and PPC Settings

Sub-Address (Bits [31:24]): 00-03h

HParaType = 08h, Sub-Address = 00h

CDC Setting

Bits [23:0]	Attribute	Default	Description
23:1	WO	xxh	Reserved
0	WO	xxh	HW CDC Solution Enable Backdoor 0: Disable (default) 1: Enable

HParaType = 08h, Sub-Address = 01h

PPC (Performance Profile Counter) Setting 1

Bits [23:0]	Attribute	Default	Description
23:5	WO	xxh	Reserved
4:0	WO	xxh	PPC Type that Driver Wants to Write Back to Memory 00h: <HRPPC_vertice> Total number of received vertices. VP counts it. 01h: <HRPPC_VChit> Hit number of vertice cache. VP counts it. 02h: <HRPPC_VSInst> Total number of executed VS instructions. VS counts it. 03h: <HRPPC_PM> Total number of primitives including the dropped primitives. VC counts it. 04h: <HRPPC_PM_valid> Total number of available primitives. VC counts it. 05h: <HRPPC_Pixel> Total number of pixels including the dropped pixel. RZ counts it. 06h: <HRPPC_Pixel_valid> Total number of available pixels. BE counts it (Zvalid Cvalid STvalid). 07h: <HRPPC_PSTAU> Total number of executed PS TAU instructions. PS counts it. 08h: <HRPPC_PSalu> Total number of executed PS ALU instructions. PS counts it. 09h: <HRPPC_RVB> Total number of reading Vertex Buffer in unit of 2QW. GEMI counts it. 0Ah: <HRPPC_RCZ> Total number of reading Coarse Z buffer in unit of 2QW. GEMI counts it. 0Bh: <HRPPC_WCZ> Total number of writing Coarse Z buffer in unit of 2QW. GEMI counts it. 0Ch: <HRPPC_RZ> Total number of reading Z buffer in unit of 2QW. GEMI counts it. 0Dh: <HRPPC_WZ> Total number of writing Z buffer in unit of 2QW. GEMI counts it. 0Eh: <HRPPC_RC> Total number of reading Color buffer in unit of 2QW. GEMI counts it. 0Fh: <HRPPC_WC> Total number of writing Color buffer in unit of 2QW. GEMI counts it. 10h: <HRPPC_RTX_SL> Total number of reading texture from SL in unit of 2QW. GEMI counts it. 11h: <HRPPC_RTX_SF> Total number of reading texture from SF in unit of 2QW. GEMI counts it. 12h: <HRPPC_R_SL> Total number of reading from SL in unit of 2QW. GEMI counts it. 13h: <HRPPC_W_SL> Total number of writing to SL in unit of 2QW. GEMI counts it. 14h: <HRPPC_R_SF> Total number of reading from SF in unit of 2QW. GEMI counts it. 15h: <HRPPC_W_SF> Total number of writing to SF in unit of 2QW. GEMI counts it. 1_0110: <HRPPC_WK_CNT> Working counter enabled by HenWK_CNT. VP counts it. 1_0111: <HZOcclusionCNT> Occlusion Count of both Z test and Stencil test result.

HParaType = 08h, Sub-Address = 02h
PPC (Performance Profile Counter) Setting 2

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	Low 24-Bit Memory Address of HRPPCTYPE In unit of 4 bytes.

HParaType = 08h, Sub-Address = 03h
PPC (Performance Profile Counter) Setting 3

Bits [23:0]	Attribute	Default	Description
23:22	WO	xxh	Location Setting of Write Back PPC 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: Reserved (System Memory) 11: Reserved (Local Memory Local Frame Buffer (L.L.))
21:9	WO	xxh	Reserved
8	WO	xxh	PPC Write Back to Memory Fire Signal 0: Not fire (default) 1: Fire
7:0	WO	xxh	High 8-Bit Memory Address of HRPPCTYPE In unity of 4 bytes.

HParaType 10h: Commands for Command Regulator

Refer to CR Chapter's "HParaType 10h: Commands for Command Regulator" for more details

HParaType 11h: Commands for Frame Buffer Swapping and CR's Miscellaneous Setting

Refer to CR Chapter's "HParaType 11h: Commands for Frame Buffer Swapping and CR's Miscellaneous Setting" for more detail