Open Graphics Programming Manual

UniChrome Pro II Graphics Processor

CX700 / VX700 Series

Part I: Graphics Core / 2D

Preliminary Revision 1.08
November 19, 2008

VIA TECHNOLOGIES, INC.

Copyright Notice:

Trademark Notice:

Disclaimer Notice:

Offices:

VIA Technologies Incorporated
Taiwan Office:
1st Floor, No. 531
Chung-Cheng Road, Hsin-Tien
Taipei, Taiwan ROC
Tel: 886-2-2218-5452
FAX: 886-2-2218-5453
Home page: http://www.via.com.tw

VIA Technologies Incorporated
USA Office:
940 Mission Court
Fremont, CA 94539
USA
Tel: 510-683-3300
FAX: 510-683-3301 or 510-687-4654
Home Page: http://www.viatech.com

REVISION HISTORY

Document Release	Date	Revision	Initials
1.08	11/19/08	Initial public release	LW

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

INTRODUCTION

This document contains detailed graphics registers descriptions and other general information for the UniChrome Pro II graphic engine. The graphics registers for the UniChrome Pro II main features and its underlying subsystems are described explicitly in the following chapters.

About This Programming Guide

The programming manual is organized into 2 volumes (Part I & Part II). A brief description of each chapter is given below:

Part I:

Introduction.
An overview of the UniChrome Pro II design features is given in this chapter, along with block diagram and reference list.

Register Overview
Register specifications for register addressing and I/O space division are shown in this chapter.

PCI Interface Register Descriptions
PCI interface summary table is presented in this chapter.

VGA I/O Register Descriptions
This chapter provides detailed VGA-related register summary and descriptions. The various video modes support by the UniChrome Pro II controller are also included in the configuration section.

2D Engine Register Descriptions
In this chapter provides detailed 2D engine register summary and descriptions.

DMA Register Descriptions
In this chapter provides detailed DMA register summary and descriptions.

CBU Rotation Register Descriptions
In this chapter provides detailed CBU rotation register summary and descriptions.

Integrated TV Encoder Register Descriptions
In this chapter provides detailed Integrated TV Encoder register summary and descriptions.

Part II:

Video Register Descriptions
This chapter provides detailed video register summary and descriptions.

3D Engine Register Descriptions
In this chapter provides detailed 3D engine register summary and descriptions.

REGISTER OVERVIEW

In the register descriptions, column “Default” indicates the default value of register bit. While column “Attribute” indicates access type of register bit.

Abbreviation

Attribute Definitions

Read / Write Attributes: read / write attributes may be used together to specify combined attributes

- **RO:** Read Only.
- **RZ:** Read as Zero.
- **R1:** Read as 1.
- **IW:** Ignore Write.
- **MW:** Must Write back what is read.
- **XW:** Backdoor Write.
- **W:** Write Only. (register value can not be read by the software)
- **WO/W1:** Write Once then Read Only after that.
- **RW**: Read / Write.
- **RW1C**: Read / Write of “1” clears bit to zero.

Sticky Attributes: adding a “S” in tail to indicate a sticky register, which means that register will not be set or altered by hot reset.
Ex. RWS: Sticky-Read/Write. **ROS**: Sticky-Read Only. **RW1CS**: Sticky-Write-1-to-Clear.

Default Value Definitions

- **Dip**: means the default value is set by dip switch or strapping.
- **HwInit**: Hardware initialized; bit default value is set by hardware.

I/O Address Space

The I/O space of the UniChrome Pro II processor is divided into the following subspaces for various functions of the processor:

- PCI Interface: PCI/AGP/Power Management configuration space
- VGA space
- Extended I/O space
- Secondary Display Engine / LCD Display
- 2D engine space
- 3D engine space
- Video Playback / Blending engines space
- HQV space
- DMA engine space

Table 1 lists the various I/O space categories and their corresponding I/O addresses for the UniChrome Pro II processor. Please note that in the monochrome mode, the "X" contained within the I/O addresses stands for **"B",** and in the color mode the "X" stands for **"D".**

Table 1. UniChrome Pro II I/O Space

Categories	I/O Address
PCI Interface	PCI Configuration Space
VGA Space	Standard VGA Space
Extended I/O Space	3C5.10 ~ 3C5.FF / 3CF.20 ~ 3CF.2F / 3X5.30 ~ 3X5.4F
Secondary Display Engine / LCD Display	3X5.50 ~ 3X5.D2

Memory Address Space

There are two memory spaces implemented in the UniChrome Pro II graphics processor:

1. Starting from PCI Memory Base 0, **MB0**, there is a 128M-Byte memory space reserved as the graphics and video playback buffer.
2. Starting from PCI Memory Base 1**, MB1**, there is a 16M-Byte memory space reserved for memory-mapped I/O, 2D Host BitBLT space and burst command area.

MB0 is declared in the register with offset address 10h in the PCI configuration space.

MB1 is declared in the register with offset address 14h in the PCI configuration space.

Memory Mapped I/O Register Address Spaces

Table 2. Memory Mapped I/O Address Space Partition Table

Memory Range (Note)	Usage
0 ~ 2M-1:	
0x00000000 ~ 0x000001FF	2D Engine Register Space
0x00000200 ~ 0x000003FF	Video Related Engines Register Space 1
0x00000400 ~ 0x000007FF	3D Engine Register Space
0x00000800 ~ 0x00000BFF	Burst Command Area
0x00000C00 ~ 0x00000DFF	MPEG Register Space
0x00000E00 ~ 0x00000FFF	DMA(AGP) Register Space
0x00001200 ~ 0x000013FF	Video Related Engines Register Space 2
0x00001E00 ~ 0x00001FFF	CBU Rotate Related
0x00002200 ~ 0x000023FF	Extended Video Engines Register Space 1
0x00003200 ~ 0x000033FF	Extended Video Engines Register Space 2
0x000083CX ~ 0x000083DX	VGA memory mapped IO Space
2M ~ 4M-1	**2D Host BitBLT Space**
4M ~ 8M-1	**Burst Command Area**
8M ~ 16M-1	**Reserved**

Notes These addresses are offset address from MB1.

PCI INTERFACE

This section provides a complete PCI register overview. Table 3 shows the supported PCI commands in UniChrome Pro II and Table 4 is a PCI register summary table.

PCI Commands

Table 3 shows the PCI commands supported by the UniChrome Pro II graphic processor. The UniChrome Pro II processor complies with the PCI bus interface protocol, Rev. 2.2. The design clock rate is 66 MHz and both master and slave modes are supported.

Table 3. PCI Command

Command Code	Command
0000	**Interrupt Acknowledge**
0001	**Special**
0010	I/O Read
0011	I/O Write
0100	**Reserved**
0101	**Reserved**
0110	Memory Read
0111	Memory Write
1000	**Reserved**
1001	**Reserved**
1010	Configuration Read
1011	Configuration Write
1100	Memory Read Multiple; treated as 0110 memory read
1101	**Dual Address**
1110	Memory Read Line; treated as 0110 memory read
1111	Memory Write and Invalid; treated as 0111 memory write

Note: The command codes in **bold** are not supported in UniChrome Pro II.

PCI Configuration Registers

The following table summarizes PCI configuration registers of UniChrome Pro II processor. This table also documents the power-on default value ("Default") and attribute ("Attribute") for each register. Access type definitions used are RW (Read/Write), RO (Read/Only) and RWC (or just WC) (Read / Write 1's to Clear individual bits). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions for details).

All offset and default values are shown in hexadecimal unless otherwise indicated. For detailed PCI register descriptions, please refer to the VIA North Bridge Datasheet.

Table 4. PCI Configuration Registers (AGP GFX)

Offset Address	Registers Name	Default Value	Attribute
01-00	Vendor ID	1106	RO
03-02	Device ID	3157	RO
05-04	Command	0000	RW
07-06	Status	0230	RW
08	Revision ID	00	RO
0B-09	Class Code	030000	RO
13-10	Memory Base 0	00000008	RW
17-14	Memory Base 1	00000000	RW
2D-2C	Subsystem Vendor ID	1106	RO
2F-2E	Subsystem ID	3157	RO
33-30	ROM Base	00000000	RW
34	Capabilities Pointer	60	RO
3C	Interrupt Line	00	RW
3D	Interrupt Pin	01	RW

Offset Address	Power Management Configuration Registers	Default Value	Attribute
60	Capability ID (01h)	01	RO
61	Next Item Pointer	70	RO
63-62	Power Management Capability	0622	RO
65-64	Power Management Control / Status	0000	RO / RW
67-66	Data+PMCSR_BSE	0000	RO

Offset Address	AGP 2.0 Configuration Register	Default Value	Attribute
70	Capability ID (02h)	02	RO
71	Next Item Pointer	00	RO
73-72	Revision Number	0020	RO
77-74	AGP Status	1F000207	RO
7B-78	AGP Command	00000000	RW

Offset Address	AGP 3.0 Configuration Area	Default	Attribute
70	Capability ID (02h)	02h	RO
71	Next Item Pointer	00	RO
73-72	Revision Number	0030	RO
77-74	AGP Status	FF001E0B	RO
7B-78	AGP Command	00000000	RW

Table 5. PCI Configuration Registers

Offset Address	Registers Name	Default Value	Attribute
01-00	Vendor ID	1106	RO
03-02	Device ID	3157	RO
05-04	Command	0000	RW
07-06	Status	0230	RW
08	Revision ID	00	RO
0B-09	Class Code	030000	RO
13-10	Memory Base 0	00000008	RW
17-14	Memory Base 1	00000000	RW
1B-18	Memory Base 2	00000008	RW
2D-2C	Subsystem Vendor ID	1106	RO
2F-2E	Subsystem ID	3157	RO
33-30	ROM Base	00000000	RW
34	Capabilities Pointer	60	RO
3C	Interrupt Line	00	RW
3D	Interrupt Pin	01	RW

Offset Address	Power Management Configuration Registers	Default Value	Attribute
60	Capability ID (01h)	01	RO
61	Next Item Pointer	70	RO
63-62	Power Management Capability	0622	RO
65-64	Power Management Control / Status	0000	RO / RW
67-66	Data+PMCSR_BSE	0000	RO

PCI REGISTER DESCRIPTIONS

This chapter provides PCI register summary table and detailed register descriptions are followed in the subsequent sections.

PCI Configuration Registers (AGP GFX)

Header Registers (0-3h)

Offset Address: 1-0h

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technologies ID Code**

Offset Address: 3-2h

Device ID **Default Value: 3157h**

Bit	Attribute	Default	Description
15:0	RO	3157h	**Device ID Code**

PCI Configuration Registers (5-3Dh)

Offset Address: 5-4h

Command Register **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10	RW	0	**Interrupt Disable** 0 Disable 1 Enable
9	RW	0	**Fast Back-to-Back Enable** 0 Disable 1 Enable
8	RW	0	**SERR# Enable** 0 Disable 1 Enable
7	RW	0	**Wait Cycle Control** 0 Disable 1 Enable
6	RW	0	**Parity Error Response** 0 Disable 1 Enable
5	RW	0	**VGA Palette Snoop** 0 Disable 1 Enable
4	RW	0	**Memory Write and Invalidate Enable** 0 Disable 1 Enable
3	RW	0	**Special Cycle** 0 Disable 1 Enable
2	RW	0	**Bus Master** 0 Disable 1 Enable
1	RW	0	**Memory Space** 0 Disable 1 Enable
0	RW	0	**IO Space** 0 Disable 1 Enable

Offset Address: 7-6h

Status Register **Default Value: 0230h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** This bit is set whenever a parity error is detected, even if parity error handling is disabled (as controlled by bit 6 in the Command register).
14	RO	Hardwired to 0	**Signaled System Error** (Not implemented)
13	RW1C	0	**Received Master Abort** For bus master only 0: If normal operation 1: When there is a master abort detected
12	RW1C	0	**Received Target Abort** For bus master only 0: If normal operation 1: When a target abort is detected
11	RW	0	**Signaled Target Abort** Not implemented.
10:9	RO	01b	**DEVSEL# Timing** 01: Medium (Read only).
8	RO	Hardwired to 0	**Data Parity Error Detected** For bus master only
7	RO	Hardwired to 0	**Fast Back-to-back Capable**
6	RO	Hardwired to 0	**UDF Supported**
5	RO	Hardwired to 1	**66MHz Capable**
4	RO	Hardwired to 1	**Capabilities List**
3	RW	0	**Interrupt Status**
2:0	RO	Hardwired to 0	**Reserved**

Note: Access property of Bit 15, 13-12 is write 1 to clear

Offset Address: 8h

Revision ID **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Revision ID**

Offset Address: 0B-9h

Class Code **Default Value: 030000h**

Bit	Attribute	Default	Description
23:0	RO	030000h	**Class Code**

Offset Address: 13-10h

Memory Base 0 **Default Value: 0000 0008h**

Bit	Attribute	Default	Description
31:0	RW	0000 0008h	**Memory Base 0**

Offset Address: 17-14h

Memory Base 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Memory Base 1**

Offset Address: 2D-2Ch
Subsystem Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Subsystem Vendor ID**

Offset Address: 2F-2Eh
Subsystem ID **Default Value: 3157h**

Bit	Attribute	Default	Description
15:0	RO	3157h	**Subsystem ID**

Offset Address: 33-30h
ROM Base **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**ROM Base**

Offset Address: 34h
Capabilities Pointer **Default Value: 60h**

Bit	Attribute	Default	Description
7:0	RO	60h	**Capabilities Pointer**

Offset Address: 3Ch
Interrupt Line **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Interrupt Line**

Offset Address: 3Dh
Interrupt Pin **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RW	01h	**Interrupt Pin**

Power Management Configuration Registers (60-67h)

Offset Address: 60h
Capability ID (01h) **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Capability ID (01h)**

Offset Address: 61h
Next Item Pointer **Default Value: 70h**

Bit	Attribute	Default	Description
7:0	RO	70h	**Next Item Pointer**

Offset Address: 63-62h
Power Management Capability **Default Value: 0622h**

Bit	Attribute	Default	Description
15:11	RO	Hardwired to 0	**Power Management Event (PME) Support**
10	RO	Hardwired to 1	**D2 Support**
9	RO	Hardwired to 1	**D1 Support**
8:6	RO	Hardwired to 0	**3.3 Vaux Auxiliary Current**
5	RO	Hardwired to 1	**DSI Device Specific Initialization**
4	RO	0	**Reserved**
3	RO	Hardwired to 0	**Power Management Event (PME) Clock**
2:0	RO	Hardwired to 010b	**Version** Complies with version 1.1

Offset Address: 65-64h
Power Management Control and Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RO	Hardwired to 0	**Power Management Event (PME) Status**
14:13	RO	Hardwired to 0	**Data Scale**
9	RO	Hardwired to 0	**D1 Select**
8	RO	Hardwired to 0	**PME Enable**
7:2	RO	0	**Reserved**
1:0	RW	0	**Power State** 00: D0 State 01: D1 State 10: D2 State 11: D3 State

Offset Address: 67-66h
Data + PMCSR_BSE **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0	**Data + PMCSR_BSE**

AGP 2.0 Configuration Registers (70-7Bh)

Offset Address: 70h
Capability ID (02h) **Default Value: 02h**

Bit	Attribute	Default	Description
7:0	RO	02h	**Capability ID (02h)**

Offset Address: 71h
Next Item Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Next Item Pointer**

Offset Address: 73-72h
Revision Number **Default Value: 0020h**

Bit	Attribute	Default	Description
15:0	RO	0020h	**Revision Number**

Offset Address: 77-74h
AGP Status **Default Value: 1F00 0207h**

Bit	Attribute	Default	Description
31:0	RO	1F00 0207h	**AGP Status**

Offset Address: 7B-78h
AGP Command **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**AGP Command**

AGP 3.0 Configuration Registers (70-7Bh)

Offset Address: 70h
Capability ID (02h) **Default Value: 02h**

Bit	Attribute	Default	Description
7:0	RO	02h	**Capability ID (02h)**

Offset Address: 71h
Next Item Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Next Item Pointer**

Offset Address: 73-72h
Revision Number **Default Value: 0030h**

Bit	Attribute	Default	Description
15:0	RO	0030h	**Revision Number**

Offset Address: 77-74h
AGP Status **Default Value: FF00 1E0Bh**

Bit	Attribute	Default	Description
31:0	RO	FF00 1E0Bh	**AGP Status**

Offset Address: 7B-78h
AGP Command **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**AGP Command**

PCI Configuration Registers

Header Registers (0-3h)

Offset Address: 1-0h

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technologies ID Code**

Offset Address: 3-2h

Device ID **Default Value: 3157h**

Bit	Attribute	Default	Description
15:0	RO	3157h	**Device ID Code**

PCI Configuration Registers (5-3Dh)

Offset Address: 5-4h

Command Register **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10	RW	0	**Interrupt Disable** 0 Disable 1 Enable
9	RW	0	**Fast Back-to-Back Enable** 0 Disable 1 Enable
8	RW	0	**SERR# Enable** 0 Disable 1 Enable
7	RW	0	**Wait Cycle Control** 0 Disable 1 Enable
6	RW	0	**Parity Error Response** 0 Disable 1 Enable
5	RW	0	**VGA Palette Snoop** 0 Disable 1 Enable
4	RW	0	**Memory Write and Invalidate Enable** 0 Disable 1 Enable
3	RW	0	**Special Cycle** 0 Disable 1 Enable
2	RW	0	**Bus Master** 0 Disable 1 Enable
1	RW	0	**Memory Space** 0 Disable 1 Enable
0	RW	0	**IO Space** 0 Disable 1 Enable

Offset Address: 7-6h

Status Register **Default Value: 0230h**

Bit	Attribute	Default	Description
15	RW	0	**Detected Parity Error** This bit is set whenever a parity error is detected, even if parity error handling is disabled (as controlled by bit 6 in the Command register).
14	RO	Hardwired to 0	**Signaled System Error** (Not implemented)
13	RW	0	**Received Master Abort** For bus master only 0 if normal operation 1 when there is a master abort detected
12	RW	0	**Received Target Abort** For bus master only 0 if normal operation 1 When a target abort is detected
11	RW	0	**Signaled Target Abort** Not implemented.
10:9	RO	01b	**DEVSEL# Timing** 01: Medium
8	RO	Hardwired to 0	**Data Parity Error Detected** For bus master only
7	RO	Hardwired to 0	**Fast Back-to-back Capable**
6	RO	Hardwired to 0	**UDF Supported**
5	RO	Hardwired to 1	**66MHz Capable**
4	RO	Hardwired to 1	**Capabilities List**
3	RW	0	**Interrupt Status**
2:0	RO	Hardwired to 0	**Reserved**

Note: Access property of Bit 15, 13-12 is write 1 to clear

Offset Address: 8h

Revision ID **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Revision ID**

Offset Address: 0B-9h

Class Code **Default Value: 030000h**

Bit	Attribute	Default	Description
23:0	RO	030000h	**Class Code**

Offset Address: 13-10h

Memory Base 0 **Default Value: 0000 0008h**

Bit	Attribute	Default	Description
31:0	RW	0000 0008h	**Memory Base 0**

Offset Address: 17-14h

Memory Base 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Memory Base 1**

Offset Address: 1B-18h
Memory Base 2 **Default Value: 0000 0008h**

Bit	Attribute	Default	Description
31:0	RW	0000 0008h	**Memory Base 2**

Offset Address: 2D-2Ch
Subsystem Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Subsystem Vendor ID**

Offset Address: 2F-2Eh
Subsystem ID **Default Value: 3157h**

Bit	Attribute	Default	Description
15:0	RO	3157h	**Subsystem ID**

Offset Address: 33-30h
ROM Base **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**ROM Base**

Offset Address: 34h
Capabilities Pointer **Default Value: 60h**

Bit	Attribute	Default	Description
7:0	RO	60h	**Capabilities Pointer**

Offset Address: 3Ch
Interrupt Line **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Interrupt Line**

Offset Address: 3Dh
Interrupt Pin **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RW	01h	**Interrupt Pin**

Power Management Configuration Registers (60-67h)

Offset Address: 60h
Capability ID (01h) **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Capability ID (01h)**

Offset Address: 61h
Next Item Pointer **Default Value: 70h**

Bit	Attribute	Default	Description
7:0	RO	70h	**Next Item Pointer**

Offset Address: 63-62h
Power Management Capability **Default Value: 0622h**

Bit	Attribute	Default	Description
15:11	RO	Hardwired to 0	**Power Management Event (PME) Support**
10	RO	Hardwired to 1	**D2 Support**
9	RO	Hardwired to 1	**D1 Support**
8:6	RO	Hardwired to 0	**3.3 Vaux Auxiliary Current**
5	RO	Hardwired to 1	**DSI Device Specific Initialization**
4	RO	0	**Reserved**
3	RO	Hardwired to 0	**Power Management Event (PME) Clock**
2:0	RO	Hardwired to 010b	**Version** Complies with version 1.1

Offset Address: 65-64h
Power Management Control and Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RO	Hardwired to 0	**Power Management Event (PME) Status**
14:13	RO	Hardwired to 0	**Data Scale**
9	RO	Hardwired to 0	**D1 Select**
8	RO	Hardwired to 0	**PME Enable**
7:2	RO	0	**Reserved**
1:0	RO	0	**Power State** 00: D0 State 01: D1 State 10: D2 State 11: D3 State

Offset Address: 67-66h
Data + PMCSR_BSE **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0	**Data + PMCSR_BSE**

PCI Express Configuration Area (70-7Bh)

Offset Address: 70h
PCI Express Capability ID (10h) **Default Value: 10h**

Bit	Attribute	Default	Description
7:0	RO	10h	**PCI Express Capability ID (10h)**

Offset Address: 71h
Next Item Pointer **Default Value: 90h**

Bit	Attribute	Default	Description
7:0	RO	90h	**Next Item Pointer**

Offset Address: 73-72h
PCI Express Capabilities **Default Value: 0011h**

Bit	Attribute	Default	Description
15:0	RO	0011h	**PCI Express Capabilities**

Offset Address: 77-74h
Device Capabilities **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Device Capabilities**

Offset Address: 79-78h

Device Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Device Control**

Offset Address: 7B-7Ah

Device Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0	**Device Status**

MSI Configuration Area (90-98h)

Offset Address: 90h

MSI Capability ID (05h) **Default Value: 05h**

Bit	Attribute	Default	Description
7:0	RO	05h	**MSI Capability ID (05h)**

f

Offset Address: 91h

Next Item Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Next Item Pointer**

Offset Address: 93-92h

Message Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Message Control**

Offset Address: 97-94h

Message Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Message Control**

Offset Address: 99-98h

Message Data **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Message Data**

VGA REGISTERS DESCRIPTIONS

This chapter provides VGA register summary table and detailed register descriptions.

VGA I/O Registers

These VGA register tables document the I/O port, I/O index and attribute ("Attribute") for each register. Attribute definitions being used are RW (Read/Write), RO (Read/Only) and RWC (or just WC) (Read / Write 1's to Clear individual bits). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions for details). All offset and default values are shown in hexadecimal unless otherwise indicated.

Table 6. VGA I/O Registers

I/O Port	I/O Index	Attribute Control Register	Attribute
3C0	-	Address	RW
3C1	00 – 0F	Palette	RW
3C1	10	Mode Control	RW
3C1	11	Overscan Color	RW
3C1	12	Color Plane Enable	RW
3C1	13	Horizontal Pixel Panning	RW
3C1	14	Color Select	RW

I/O Port	I/O Index	General Register	Attribute
3C2	-	Miscellaneous Output	WO
3CC	-	Miscellaneous Output	RO
3C2	-	Input Status 0	RO
3XA	-	Input Status 1	RO
3C3	-	Video Subsystem Enable	RW
46E8	-	Video Adapter Enable	RW

I/O Port	I/O Index	Sequencer Register	Attribute
3C4	-	Address	RW
3C5	00	Reset	RW
3C5	01	Clocking Mode	RW
3C5	02	Map Mask	RW
3C5	03	Character Map Select	RW
3C5	04	Memory Mode	RW

I/O Port	I/O Index	Graphic Controller Register	Attribute
3CE	-	Address	RW
3CF	00	Set / Reset	RW
3CF	01	Enable Set / Reset	RW
3CF	02	Color Compare	RW
3CF	03	Data Rotate	RW
3CF	04	Read Map Select	RW
3CF	05	Mode	RW
3CF	06	Miscellaneous	RW
3CF	07	Color Don't Care	RW
3CF	08	Bit Mask	RW

I/O Port	I/O Index	CRTC Controller Register	Attribute
3X4	-	Address	RW
3X5	00	Horizontal Total	RW
3X5	01	Horizontal Dipslay End	RW
3X5	02	Start Horizontal Blank	RW
3X5	03	End Horizontal Blank	RW
3X5	04	Start Horizontal Retrace	RW
3X5	05	End Horizontal Retrace	RW
3X5	06	Vertical Total	RW
3X5	07	Overflow	RW
3X5	08	Preset Row Scan	RW
3X5	09	Max Scan Line	RW
3X5	0A	Cursor Start	RW
3X5	0B	Cursor End	RW
3X5	0C	Start Address High	RW
3X5	0D	Start Address Low	RW
3X5	0E	Cursor Location High	RW
3X5	0F	Cursor Location Low	RW
3X5	10	Vertical Retrace Start	RW
3X5	11	Vertical Retrace End	RW
3X5	12	Vertical Display End	RW
3X5	13	Offset	RW
3X5	14	Underline Location	RW
3X5	15	Start Vertical Blank	RW
3X5	16	End Vertical Blank	RW
3X5	17	CRTC Mode Control	RW
3X5	18	Line Compare	RW

Table 7. Extended I/O Registers

I/O Port	I/O Index	Sequencer Extended Register	Attribute
3C5	10	Extended Register Unlock	RW
3C5	11	Configuration Register 0	RO
3C5	12	Configuration Register 1	RO
3C5	13	Configuration Register 2	RO
3C5	14	Reserved	RO
3C5	15	Display Mode Control	RW
3C5	16	Display FIFO Threshold Control	RW
3C5	17	Display FIFO Control	RW
3C5	18	Display Arbiter Control 0	RW
3C5	19	Power Management	RW
3C5	1A	PCI Bus Control	RW
3C5	1B	Power Management Control 0	RW
3C5	1C	Horizontal Display Fetch Count Data	RW
3C5	1D	Horizontal Display Fetch Count Control	RW
3C5	1E	Power Management Control	RW
3C5	1F	Memory Control 0	RW
3C5	20	Typical Arbiter Control 0	RW
3C5	21	Typical Arbiter Control 1	RW
3C5	22	Display Arbiter Control 1	RW
3C5	23	Memory Control 1	RW
3C5	24	Memory Control 2	RW
3C5	25	General Purpose I/O Port	RW
3C5	26	IIC Serial Port Control 0	RW
3C5	27	Memory Control 3	RW
3C5	28	Memory Control 4	RW
3C5	29	Memory Control 5	RW
3C5	2A	Power Management Control 5	RW
3C5	2B	MCK De-skew Control 1	RW
3C5	2C	General Purpose I/O Port	RW
3C5	2D	Power Management Control 1	RW
3C5	2E	Power Management Control 2	RW
3C5	2F	PCI Configuration Memory Base Shadow 0	RO
3C5	30	PCI Configuration Memory Base Shadow 1	RO
3C5	31	IIC Serial Port Control 1	RW
3C5	34-32	Reserved	-
3C5	36-35	Subsystem Vender ID	RW
3C5	38-37	Subsystem ID	RW
3C5	3A-39	BIOS Reserved Register 1-0	RW
3C5	3B	PCI Revision ID Back Door	RW
3C5	3C	Miscellaneous	RW
3C5	3D	General Purpose I/O Port	RW
3C5	3E	Miscellaneous Register for AGP Mux	RW
3C5	3F	Power Management Control 2	RW
3C5	40	PLL Control	RW
3C5	41	Typical Arbiter Control 1	RW
3C5	42	Typical Arbiter Control 2	RW
3C5	43	Graphics Bonding Option	RO

I/O Port	I/O Index	Clock Synthesizer Register	Attribute
3C5	44	VCK Clock Synthesizer Value 0	RW
3C5	45	VCK Clock Synthesizer Value 1	RW
3C5	46	VCK Clock Synthesizer Value 2	RW
3C5	47	ECK Clock Synthesizer Value 0	RW
3C5	48	ECK Clock Synthesizer Value 1	RW
3C5	49	ECK Clock Synthesizer Value 2	RW
3C5	4A	Secondary Display (LCDCK) Clock Synthesizer Value 0	RW
3C5	4B	Secondary Display (LCDCK) Clock Synthesizer Value 1	RW
3C5	4C	Secondary Display (LCDCK) Clock Synthesizer Value 2	RW
3C5	4D	Dual Channel Memory Control	RW
3C5	4E	Software Reset Control	RW
3C5	4F	CR Gating Clock Control	RW
3C5	50	AGP Control Register	RW
3C5	51	P4/K8 Control Register 1	RW
3C5	52	Integrated TV shadow Register Control	RW
3C5	53	DAC Sense Control Register 1	RW
3C5	54	DAC Sense Control Register 2	RW
3C5	55	DAC Sense Control Register 3	RW
3C5	56	DAC Sense Control Register 4	RW
3C5	57	P4/K8 Control Register 2	RW
3C5	58	GFX Power Control Register 1	RW
3C5	59	GFX Power Control Register 2	RW
3C5	5A	PCI Bus Control 2	RW
3C5	5B	Device Used Status 0	RO
3C5	5C	Device Used Status 1	RO
3C5	5D	Timer Control Register	RW
3C5	5E	DAC Control Register 2	RW
3C5	60	I2C Mode Control	RW
3C5	61	I2C Host Address	RW
3C5	62	I2C Host Data	RW
3C5	63	I2C Host Control	RW
3C5	64	I2C Status	RW
3C5	65	Power Management Control 6	RW

I/O Port	I/O Index	Graphics Controller Extended Register	Attribute
3CF	20	Offset Register Control	RW
3CF	21	Offset Register A	RW
3CF	22	Offset Register B	RW

I/O Port	I/O Index	CRT Controller Extended Register	Attribute
3X5	30	Display Fetch Blocking Control	RW
3X5	31	Half Line Position	RW
3X5	32	Mode Control	RW
3X5	33	HSYNC Adjuster	RW
3X5	34	Starting Address Overflow	RW
3X5	35	Extended Overflow	RW
3X5	36	Power Management Control 3 (Monitor Control)	RW
3X5	37	DAC control Register	RW
3X5	38	Signature Data B0	RW
3X5	39	Signature Data B1	RW
3X5	3A	Signature Data B2	RW
3C5	3F-3B	BIOS Reserved Register 6-2	RW
3X5	40	Test Mode Control 0	RW
3X5	41	Power Now Indicator Control 1	RW
3X5	42	Power Now Indicator Control 2	RW
3X5	43	IGA1 Display Control	RW
3X5	45	Power Now Indicator Control 3	RW
3X5	46	Test Mode Control 1	RW
3X5	47	Test Mode Control 2	RW
3X5	48	Starting Address Overflow	RW
3X5	49-4F	Reserved	RW

Note: In monochrome mode, the “X” in the above table stands for **“B”**
In color mode, the “X” in the above table stands for **“D”.**

Table 8. Secondary Display I/O Registers

I/O Port	I/O Index	Sequencer Extended Registers	Attribute
3X5	50	Second CRTC Horizontal Total Period	RW
3X5	51	Second CRTC Horizontal Active Data Period	RW
3X5	52	Second CRTC Horizontal Blanking Start	RW
3X5	53	Second CRTC Horizontal Blanking End	RW
3X5	54	Second CRTC Horizontal Blanking Overflow	RW
3X5	55	Second CRTC Horizontal Period Overflow	RW
3X5	56	Second CRTC Horizontal Retrace Start	RW
3X5	57	Second CRTC Horizontal Retrace End	RW
3X5	58	Second CRTC Vertical Total Period	RW
3X5	59	Second CRTC Vertical Active Data Period	RW
3X5	5A	Second CRTC Vertical Blanking Start	RW
3X5	5B	Second CRTC Vertical Blanking End	RW
3X5	5C	Second CRTC Vertical Blanking Overflow	RW
3X5	5D	Second CRTC Vertical Period Overflow	RW
3X5	5E	Second CRTC Vertical Retrace Start	RW
3X5	5F	Second CRTC Vertical Retrace End	RW
3X5	60	Second CRTC Vertical Status 1	RO
3X5	61	Second CRTC Vertical Status 2	RO
3X5	62	Second Display Starting Address Low	RW
3X5	63	Second Display Starting Address Middle	RW
3X5	64	Second Display Starting Address High	RW
3X5	65	Second Display Horizontal Quadword Count Data	RW
3X5	66	Second Display Horizontal Offset	RW
3X5	67	Second Display Color Depth and Horizontal Overflow	RW
3X5	68	Second Display Queue Depth and Read Threshold	RW
3X5	69	Second Display Interrupt Enable and Status	RW
3X5	6A	Second Display Channel and LCD Enable	RW
3X5	6B	Channel 1 and 2 Clock Mode Selection	RW
3X5	6C	TV Clock Control	RW
3X5	6D	Horizontal Total Shadow	RW
3X5	6E	End Horizontal Blanking Shadow	RW
3X5	6F	Vertical Total Shadow	RW
3X5	70	Vertical Display Enable End Shadow	RW
3X5	71	Vertical Display Overflow Shadow	RW
3X5	72	Start Vertical Blank Shadow	RW
3X5	73	End Vertical Blank Shadow	RW
3X5	74	Vertical Blank Overflow Shadow	RW
3X5	75	Vertical Retrace Start Shadow	RW
3X5	76	Vertical Retrace End Shadow	RW
3X5	77	LCD Horizontal Scaling Factor	RW
3X5	78	LCD Vertical Scaling Factor	RW
3X5	79	LCD Scaling Control	RW
3X5	7A	LCD Scaling Parameter 1	RW
3X5	7B	LCD Scaling Parameter 2	RW
3X5	7C	LCD Scaling Parameter 3	RW
3X5	7D	LCD Scaling Parameter 4	RW
3X5	7E	LCD Scaling Parameter 5	RW
3X5	7F	LCD Scaling Parameter 6	RW
3X5	80	LCD Scaling Parameter 7	RW
3X5	81	LCD Scaling Parameter 8	RW

I/O Port	I/O Index	Sequencer Extended Registers	Attribute
3X5	82	LCD Scaling Parameter 9	RW
3X5	83	LCD Scaling Parameter 10	RW
3X5	84	LCD Scaling Parameter 11	RW
3X5	85	LCD Scaling Parameter 12	RW
3X5	86	LCD Scaling Parameter 13	RW
3X5	87	LCD Scaling Parameter 14	RW
3X5	88	LCD Panel Type	RW
3X5	89	Reserved	RO
3X5	8A	LCD Timing Control 1	RW
3X5	8B	LCD Power Sequence Control 0	RW
3X5	8C	LCD Power Sequence Control 1	RW
3X5	8D	LCD Power Sequence Control 2	RW
3X5	8E	LCD Power Sequence Control 3	RW
3X5	8F	LCD Power Sequence Control 4	RW
3X5	90	LCD Power Sequence Control 5	RW
3X5	91	Software Control Power Sequence	RW
3X5	92	Read Threshold 2	RW
3X5	93	Reserved	RO
3X5	94	Expire Number and Display Queue Extend Bit	RW
3X5	95	Extend Threshold Bit	RW
3X5	96	Digital Video Port 0 Function Select	RW
3X5	97	LVDS Channel 2 Function Select 0	RW
3X5	98	LVDS Channel 2 Function Select 1	RW
3X5	99	LVDS Channel 1 Function Select 0	RW
3X5	9A	LVDS Channel 1 Function Select 1	RW
3X5	9B	Digital Video Port 1 Function Select 0	RW
3X5	9C	Digital Video l Port 1 Function Select 1	RW
3X5	9D	Power Now Control 2	RW
3X5	9E	Power Now Control 3	RW
3X5	9F	Power Now Control 4	RW
3X5	A0	Horizontal Scaling Initial Value	RW
3X5	A1	Vertical Scaling Initial Value	RW
3X5	A2	Horizontal and Vertical Scaling Enable Bit	RW
3X5	A3	Second Display Starting Address Extended	RW
3X5	A4	Spectrum FIFO Control register	RW
3X5	A5	Second LCD Vertical scaling Factor	RW
3X5	A6	Second LCD Vertical scaling Factor	RW
3X5	A7	Expected IGA1 Vertical Display End	RW
3X5	A8	Expected IGA1 Vertical Display End	RW
3X5	A9	Hardware Gamma Control Register	RW
3X5	AA	FIFO Depth & Threshold Overflow bit	RW
3X5	AB	IGA2 Interlace Half Line Register	RW
3X5	AC	IGA2 Interlace Half Line Register	RW
3X5	D0	LVDS PLL Control Register	RW
3X5	D1	DVI PLL Control Register	RW
3X5	D2	LVDS / DVI Control Register	RW
3X5	D3	Second Power Sequence Control Register 0	RW
3X5	D4	Second Power Sequence Control Register 1	RW
3X5	D5	LVDS Testing Mode Control Register	RW
3X5	D6	DCVI Control Register 0	RW
3X5	D7	DCVI Control Register 1	RW

Extended I/O Space Register Descriptions

Sequencer Extended Registers

IO Port / Index: 3C5.10
Extended Register Unlock **Default Value: 01h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	1b	Write 1 to this bit to unlock accessing of I/O space.

IO Port / Index: 3C5.11
Configuration Register 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**VGA Port Select** 0: 3C3 1: 46E8
6	RO	0	**PC AT Space Disable** 0: Disable VGA & memory space: A0000h-BFFFFh 1: IBM VGA standard space
5	RO	0	**Reserved**
4:3	RO	0	**Bus Type** 00: Reserved 01: Reserved 10: Reserved 11: 1x, 2x, 4x (8x) side band AGP Bus
2:0	RO	0	**Reserved**

IO Port / Index: 3C5.12
Configuration Register 1 (3C5.5A[0]=0) **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RO	0	**Panel Type (VCP0D3/2/1/0)**

IO Port / Index: 3C5.13
Configuration Register 2 (3C5.5A[0]=0) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RO	0	**DVP1 Output Status (VCP1D5)**
5:3	RO	0	**Reserved**
2:1	RO	0	**DVP1 Output Status (VCP1D4/ VCP1D3)** {[6], [2:1]} 00x: DVP-TV output 01x: DVP with alpha output 100: DCVI 10-bit data output 101: DCVI 8-bit data output 110: DCVI 20-bit data output 111: DCVI 16-bit data output
0	RO	0	**Reserved**

IO Port / Index: 3C5.12

Shadow Configuration Register 1 (3C5.5A[0]=1) **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**VCP1 Status (DVP1D7/6/5/4)** 0000: CAP 8 bit CCIR656 0001: CAP 8 bit CCIR601 0010: CAP 8 bit VIP 1.1 0011: CAP 8 bit VIP 2.0 0100: CAP 16 bit CCIR656 0101: CAP 16 bit CCIR601 0110: CAP 16 bit VIP 1.1 0111: CAP 16 bit VIP 2.0 1xxx: TS 8 bit
3:0	RO	0	**VCP0 Type Select (DVP1D07/6/5/4)** 0000: CAP 8 bit CCIR656 0001: CAP 8 bit CCIR601 0010: CAP 8 bit VIP 1.1 0011: CAP 8 bit VIP 2.0 0100: CAP 16 bit CCIR656 0101: CAP 16 bit CCIR601 0110: CAP 16 bit VIP 1.1 0111: CAP 16 bit VIP 2.0 1xxx: TS 8 bit

IO Port / Index: 3C5.13

Configuration Register 2 (3C5.5A[0]=1) **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Integrated LVDS / DVI Mode Select (DVP1D15/14) -** ***Refer to LVDS / DVI chapter for details***
5:3	RO	0	**Reserved (DVP1D13/12/11)**
2:0	RO	0	**DAC (CRT/TV) Output Mode Select (DVP1D10/09/08)** 0xx: DAC A/B/C = R/G/B for CRT 100: DAC A/B/C = C/Y/CVBS for TV 101: DAC A/B/C = C/Y/Y for TV 110: DAC A/B/C = R/G/B for TV 111: DAC A/B/C = Pr/Y/Pb for TV

IO Port / Index: 3C5.15

Display Mode Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**8/6 Bits LUT** 0: 6-bit 1: 8-bit
6	RW	0	**Text Column Control** 0: 80 column 1: 132 column
5	RW	0	**Wrap Around Disable** 0: Disable (For Mode 0-13) 1: Enable
4	RW	0	**Hi Color Mode Select** 0: 555 1: 565
3:2	RW	0	**Display Color Depth Select** 00: 8bpp 01: 16bpp 10: 30bpp 11: 32bpp
1	RW	0	**Extended Display Mode Enable** 0: Disable 1: Enable
0	RO	0	**Reserved**

IO Port / Index: 3C5.16
Display FIFO Threshold Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Move to 3B/D5.33** Display FIFO threshold select bit[6]
6	RW	0	**CRT Display Source** 0: Primary Display Stream 1: Secondary Display Stream
5:0	RW	0	**Display FIFO Threshold Select** Display FIFO threshold select. (see Rx3C5.51[2])

IO Port / Index: 3C5.17
Display FIFO Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Display FIFO Depth Select** Display FIFO Depth select. (see Rx3C5.51[2])

IO Port / Index: 3C5.18
Display Arbiter Control 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Display FIFO Fetch Datum Threshold Value Bit[6]**
6	RW	0	**Force The PREQ Always Higher Than TREQ** 0: Disable 1: Enable
5:0	RW	0	**Graphics PREQ Threshold**

IO Port / Index: 3C5.19
Power Management **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**MIU/AGP Interface Clock Control** 0: Clocks always on 1: Enable clock gating
5	RW	0	**P-Arbiter Interface Clock Control** 0: Clocks always on 1: Enable clock gating
4	RW	0	**AGP Interface Clock Control** 0: Clocks always on 1: Enable clock gating
3	RW	0	**Typical Arbiter Interface Clock Control** 0: Clocks always on 1: Enable clock gating
2	RW	0	**MC Interface Clock Control** 0: Clocks always on 1: Enable clock gating
1	RW	0	**Display Interface Clock Control** 0: Clocks always on 1: Enable clock gating
0	RW	0	**CPU Interface Clock Control** 0: Clocks always on 1: Enable clock gating

IO Port / Index: 3C5.1A
PCI Bus Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Read Cache Enable** 0: Disable 1: Enable
6	RW	0	**Software Reset** 0: Default value 1: Reset
5	RW	0	**DVI Sense** 0: No connect 1: Connected
4	RW	0	**Second DVI Sense** 0: No connect 1: Connected
3	RW	0	**Extended Mode Memory Access Enable** 0: Disable 1: Enable
2	RW	0	**PCI Burst Write Wait State Select** 0: 0 Wait state 1: 1 Wait state
1	RO	0	**Reserved**
0	RW	0	**LUT Shadow Access** 0: 3C6/3C7/3C8/3C9 addresses map to Primary Display's LUT 1: 3C6/3C7/3C8/3C9 addresses map to Secondary Display's LUT

IO Port / Index: 3C5.1B
Power Management Control 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Secondary Display Engine (Gated Clock <LCK>)** 0x: Clock always off 10: Clock always on 11: Clock on/off according to the Power Management Status (PMS)
5:4	RW	0	**Primary Display Engine (Gated Clock <VCK>)** 0x: Clock always off 10: Clock always on 11: Clock on/off according to the PMS
3:1	RO	0	**Reserved**
0	RW	0	**Primary Display's LUT On/Off** 0: On 1: Off

IO Port / Index: 3C5.1C
Horizontal Display Fetch Count Data **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Horizontal Display Fetch Count Data [7:0]** Unit: 16 bytes

IO Port / Index: 3C5.1C
Horizontal Display Fetch Count Data **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1:0	RW	0	**Horizontal Display Fetch Count Data Bit [9:8]** Used in conjunction with Rx3C5.1C register.

IO Port / Index: 3C5.1E
Power Management Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Video Capture Port Power Control** 0x: Pad always off 10: Depend on the other control signal 11: Pad on/off according to the PMS
5:4	RW	0	**Digital Video Port 1 Power Control** 0x: Pad always off 10: Depend on the other control signal 11: Pad on/off according to the PMS
3	RW	0	**Spread Spectrum On/Off** 0: Off 1: On
2	RO	0	**Reserved**
1	RW	0	**Replace ECK by MCK** For BIST purpose.
0	RW	0	**On/Off ROC ECK** 0: Off 1: On

IO Port / Index: 3C5.20
Typical Arbiter Control 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Typical Request Kill Number**

IO Port / Index: 3C5.21
Typical Arbiter Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**3D Request Kill Number**

IO Port / Index: 3C5.22
Display Arbiter Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Display Queue Request Expire Number** Hardware multiples this register value by 4 to handle the FIFO control

IO Port / Index: 3C5.26
IIC Serial Port Control 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	0	**SPCLK2 Pin Control** 0: Driven low 1: Tri-Stated
4	RW	0	**SPCLK2 Pin Control** 0: Driven low 1: Tri-Stated
3	RO	0	**SPCLK2 Pin Status**
2	RO	0	**SPCLK2 Pin Status**
1	RW	0	**SPCLK2 Wait State Enable** 0: Disable 1: Enable (Drive DDCSCL low upon receipt of serial port start).
0	RW	0	**Serial Port Enable** 0: Disable 1: Enable

IO Port / Index: 3C5.2A

Power Management Control 5 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**The Spread Spectrum Type Control** 0: Original Type 1: FIFO Type
5:4	RO	0	**Reserved**
3:2	RW	0	**LVDS Channel 2 I/O Pad Control** 0x: Pad always off 10: Depend on the other control signal 11: Pad on/off according to the PMS
1:0	RW	0	**LVDS Channel 1 and DVI I/O Pad Control** 0x: Pad always off 10: Depend on the other control signal 11: Pad on/off according to the PMS

IO Port / Index: 3C5.2B

DVI and LVDS Interrupt Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DVI Sense Interrupt Enable -** ***Refer to LVDS / DVI chapter for details***
6	RW1C	0	**DVI Sense Interrupt Status -** ***Refer to LVDS / DVI chapter for details***
5	RW	0	**LVDS Sense Interrupt Enable -** ***Refer to LVDS / DVI chapter for details***
4	RW1C	0	**LVDS Sense Interrupt Status -** ***Refer to LVDS / DVI chapter for details***
3	RW	0	**CRT Sense Interrupt Enable** 0: Disable 1: Enable
2	RW1C	0	**CRT Sense Interrupt Status**
1	RW	0	**CRT Hot Plug Detection Function Enable** 0: Disable 1: Enable Please wait at least 2 frames to enable interrupt, when this function is enabled.
0	RW1C	0	**MSI Pending Interrupt Re-trigger Bit** When SW wants to exit interrupt service, please clear the bit. HW may send out interrupt again if pending interrupt exists. The funciton is enable when MSI Enable = 1'b1.

IO Port / Index: 3C5.2C

General Purpose I/O Port **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**GPIO_2 Output Enable** 0: Disable 1: Enable
6	RW	0	**GPIO_3 Output Enable** 0: Disable 1: Enable
5	RW	0	**GPIO_2 Output Data**
4	RW	0	**GPIO_3 Output Data**
3	RO	0	**GPIO_2 Pin Status**
2	RO	0	**GPIO_3 Pin Status**
1	RW	0	**GPIO Port Enable** 0: HW controlled 1: SW controlled
0	RW	0	**Spectrum IO Selected** 0: GPIO port 1: GPIO_2 as DISPCLKI1, GPIO_3 as DISPCLKO1

IO Port / Index: 3C5.2D

Power Management Control 1 **Default Value: 2Ah**

Bit	Attribute	Default	Description
7:6	RW	0	**E3_ECK_N Selection** 00: E3_ECK_N 01: E3_ECK 10: delayed E3_ECK_N 11: delayed E3_ECK
5:4	RW	10b	**VCK (Primary Display Clock) PLL Power Control** 0x: PLL power-off 10: PLL always on 11: PLL on/off according to the PMS
3:2	RW	10b	**LCK (Secondary Display Clock) PLL Power Control** 0x: PLL power-off 10: PLL always on 11: PLL on/off according to the PMS
1:0	RW	10b	**ECK (Engine Clock) PLL Power Control** 0x: PLL power-off 10: PLL always on 11: PLL on/off according to the PMS

IO Port / Index: 3C5.2E

Power Management Control 2 **Default Value: 2Ah**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5:4	RW	10b	**Video Processor (Gated Clock <ECK>)** 0x: Clock off 10: Clock always on 11: Clock on/off according to the engine IDLE status
3:2	RW	10b	**PCI Master/DMA (Gated Clock <ECK/CPUCK>)** 0x: Clock off 10: Clock always on 11: Clock on/off according to the engine IDLE status
1:0	RW	10b	**Video Playback Engine (V3/V4 Gated Clock <VCK>)** 0x: Clock off 10: Clock always on 11: Clock on/off according to the engine IDLE status

IO Port / Index: 3C5.2F

PCI Configuration Memory Base Shadow 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**PCI Configuration Register 14, bits [31:24]**

IO Port / Index: 3C5.30

PCI Configuration Memory Base Shadow 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**PCI Configuration Register 10, bits [31:24]**

IO Port / Index: 3C5.31
IIC Serial Port Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	0	**SPCLCK1 Pin Control** 0: SPCLCK driven low 1: SPCLCK tri-stated
4	RW	0	**SDATA1 Pin Control** 0: SDATA driven low 1: SDATA tri-stated
3	RO	0	**SDPCLCK1 Pin Status** 0: SPCLCK driven low 1: SPCLCK tri-stated
2	RO	0	**SDATA1 Pin Status** 0: SDATA driven low 1: SDATA tri-stated
1	RW	0	**SPCLCK1 Wait State Enable** 1: Enable (Drive SPCLCK low upon receipt of serial port start).
0	RW	0	**Serial Port Enable** 0: Disable 1: Enable

IO Port / Index: 3C5.35
Subsystem Vendor ID0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Subsystem Vendor ID [7:0]**

IO Port / Index: 3C5.36
Subsystem Vendor ID1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Subsystem Vendor ID [15:8]**

IO Port / Index: 3C5.37
Subsystem ID0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Subsystem ID [7:0]**

IO Port / Index: 3C5.38
Subsystem ID1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Subsystem ID [15:8]**

IO Port / Index: 3C5.39
BIOS Reserved Register 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**BIOS Reserved Register 0**

IO Port / Index: 3C5.3A
BIOS Reserved Register 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**BIOS Reserved Register 1**

IO Port / Index: 3C5.3B
Revision ID **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Internal Revision ID**

IO Port / Index: 3C5.3C
Miscellaneous **Default Value: 01h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RO	0	**ECK PLL Locked Detect** 0: Unlock 1: Locked
3	RO	0	**VCK PLL Locked Detect** 0: Unlock 1: Locked
2	RO	0	**LCDCK PLL Locked Detect** 0: Unlock 1: Locked
1	RW	0	**Switch 3 PLLs to Prime Output** 0: Disable 1: Enable
0	RW	1b	**AGP Bus Back Door** 0: ACP2.0 Spec 1: ACP3.0 Spec

IO Port / Index: 3C5.3D
General Purpose I/O Port **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**GPIO_4 Output Enable** 0: Disable 1: Enable
6	RW	0	**GPIO_5 Output Enable** 0: Disable 1: Enable
5	RW	0	**GPIO_4 Output Data**
4	RW	0	**GPIO_5 Output Data**
3	RO	0	**GPIO_4 Pin Status**
2	RO	0	**GPIO_5 Pin Status**
1	RO	0	**Reserved**
0	RW	0	**Spectrum IO Selected** 0: GPIO Port 1: GPIO_4 as DISPCLKI2, GPIO_5 as DISPCLKO2

IO Port / Index: 3C5.3E
Miscellaneous Register for AGP Mux **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved for AGP Mux**
1	RW	0	**Multi-function Selection** 0: Emulate I2C and DDC Bus by GPIO2/3/4 1: Direct ENPVDD/ ENPVEE / ENBLT signals through AGP Bus
0	RW	0	**Second DVIDET Sense Signal Source** 0: From DFP high-half 1: From DVP 1

IO Port / Index: 3C5.3F

Power Management Control 2 **Default Value: AAh**

Bit	Attribute	Default	Description
7:6	RW	10b	**CR Clock Control (Gated Clock <ECK>)** 0x: Clock off 10: Clock always on 11: Clock on/off according to the engine IDLE status
5:4	RW	10b	**3D Clock Control (Gated Clock <ECK>)** 0x: Clock off 10: Clock always on 11: Clock on/off according to the engine IDLE status
3:2	RW	10b	**2D Clock Control (Gated Clock <ECK/CPUCK>)** 0x: Clock off 10: Clock always on 11: Clock on/off according to the engine IDLE status
1:0	RW	10b	**Video Clock Control (Gated Clock <ECK>)** 0x: Clock off 10: Clock always on 11: Clock on/off according to each engine IDLE status

IO Port / Index: 3C5.40

PLL Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**CRT Sense Enable** Hardware sends constant value to DAC for sense. 0: Disable 1: Enable When enable, we send pattern 24'h555555 to DAC
6	RW	0	**CAP_ON**
5:4	RW	0	**Free Run ECK Frequency Within the Idle Mode** 00: No change 01: 1/2 ECK 10: 1/4 ECK 11: 1/8 ECK
3	RW	0	**LVDS and DVI Interrupt Method** - ***Refer to LVDS / DVI chapter for details***
2	RW	0	**Reset LCDCK PLL**
1	RW	0	**Reset VCK PLL**
0	RW	0	**Reset ECK PLL**

IO Port / Index: 3C5.41

Typical Arbiter Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Typical Request T-Hold**
3:0	RO	0	**Typical Request Pre-T-Hold**

IO Port / Index: 3C5.42

Typical Arbiter Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Linear Addressing Mode Enable** 0: Force all engine use linear addressing mode 1: The addressing mode is decided by engine itself
6	RO	0	**P_ARB Request Attribute** 1: Supports Fetch Cycle With Length (2) Capability
5	RO	0	**P_ARB Arbitration Type** 0: Run-robin Like 1: Fix
4:0	RO	0	**Typical Request Max. Queuing Number**

IO Port / Index: 3C5.43

Graphics Bonding Option **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Advance Video Enable Flag** 0: Disable 1: Enable
6	RO	0	**Windows Media Video Enable Flag** 0: Disable 1: Enable
5	RW1C	0	**IGA2 Display FIFO Underflow Flag**
4	RW1C	0	**IGA1 Display FIFO Underflow Flag**
3	RW1C	0	**Typical Channel 0 Arbiter Read Back Data Overwrite Flag**
2	RW1C	0	**Typical Channel 1 Arbiter Read Back Data Overwrite Flag**
1	RO	0	**Reserved**
0	RO	0	**Notebook Used Flag** 1: Notebook 0: Desktop

Clock Synthesizer Registers

IO Port / Index: 3C5.44
Primary Display (VCK) Clock Synthesizer Value 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**DM[7:0]**

IO Port / Index: 3C5.45
Primary Display (VCK) Clock Synthesizer Value 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**{DTZ[0], 2'b00, DR[2:0], DM[9:8]}**

IO Port / Index: 3C5.46
Primary Display (VCK) Clock Synthesizer Value 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**{DTZ[1], DN[6:0]}**

IO Port / Index: 3C5.47
ECK Clock Synthesizer Value 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**DM[7:0]**

IO Port / Index: 3C5.48
ECK Clock Synthesizer Value 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**{DTZ[0], 2'b00, DR[2:0], DM[9:8]}**

IO Port / Index: 3C5.49
ECK Clock Synthesizer Value 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**{DTZ[1], 1'b0, DN[5:0]}**

IO Port / Index: 3C5.4A
Secondary Display (LCDCK) Clock Synthesizer 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**DM[7:0]**

IO Port / Index: 3C5.4B
Secondary Display (LCDCK) Synthesizer Value 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**{DTZ[0], 2'b00, DR[2:0], DM[9:8]}**

IO Port / Index: 3C5.4C

Secondary Display (LCDCK) Synthesizer Value 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**{DTZ[1], DN[6:0]}**

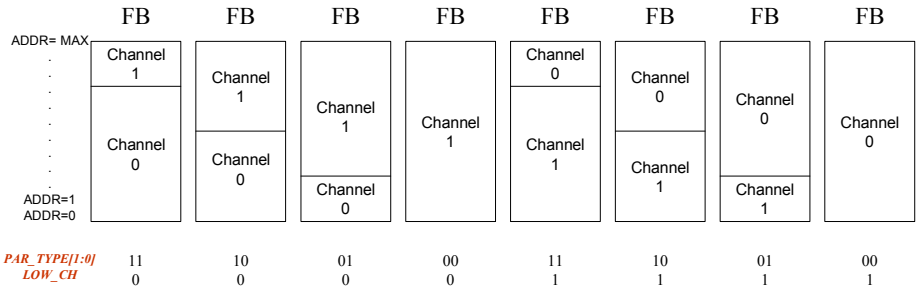
Note:

1. DTZ[1:0]: Select charge-pump current. Default value = 00b.
2. DGAIN[1:0] is for testing purpose and must be 00b in normal mode.
3. Frequency equations: the following two equations must be asserted
   a) Internal Working Frequency
      Fvco = Fref * (DM+2) / (DN+2) and 300MHz <= Fvco <= 600MHz
   b) True Output Frequency
      Fout = Fref * (DM+2) / [(DN+2) (2DR)]

IO Port / Index: 3C5.4D

Dual Channel Memory Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Ypical Arbiter Tracking FIFO Type** 0: 64 level 1: 128 level (only single channel can use)
6	RO	0	**Reserved**
5:4	RW	0	**Partition Type** 00: 4/4, 0/4 01: 3/4, 1/4 10: 2/4, 2/4 11: 1/4, ¾
3	RW	0	**Low Address Channel Indicator** 0: Channel 0 at low address 1: Channel 1 at low address
2:0	RW	0	**Frame Buffer Size Indicator** 000: Reserved 001: 8MB 010: 16MB 011: 32MB 100: 64MB 101: 128MB 110: 256MB 111: 512MB



IO Port / Index: 3C5.4E
Software Reset Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5:4	RW	0	**3D Reset Control** 01: Engine reset (high active) 10: Register reset (high active)
3:2	RW	0	**2D Reset Control** 01: Engine reset (high active) 10: Reserved
1:0	RW	0	**HQV/Video/Capture Reset Control** 01: Engine reset (high active) 10: Register reset (high active)

IO Port / Index: 3C5.4F
CR Gating Clock Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Threshold value of engine idle for gating engine clock**

IO Port / Index: 3C5.50
AGP Control Register **Default Value: 3Fh**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**AGP Request Attribute** 0: Only support length 1 1: Support length 2
5:0	RW	111111b	**AGP Track FIFO Number** The default value is 63.

IO Port / Index: 3C5.51
P4 / K8 Control Register 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**NB FIFO Clock Control** 0: Disable 1: Enable
6	RW	0	**IGA1 Request Using New Method** 0: Original method 1: New method
5	RW	0	**GFIFO1_SRC for Text Mode** 0: Original method 1: Write out font and attribute to NB FIFO
4	RW	0	**K8_MODE for GMINT Data Bus Mux Select** 0: For P4 1: For K8
3	RW	0	**ARB_TYP Software Reset** 1: Reset (high active)
2	RW	0	**IGA1_FIFO_VAL_TYPE** 0: THD/DEPTH/HighTHD : x2/x1/x2 1: THD/DEPTH/HighTHD : x4/x2/x4
1	RW	0	**P_ARB and NB FIFO Software Reset** 1: Reset (high active)
0	RW	0	**NB FIFO Enable** 0: Disable 1: Enable

IO Port / Index: 3C5.52
Integrated TV Shadow Register Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:1	RW	0	**Integrated TV Shadow Memory Window** 00: A0000 01: A8000 10: B0000 11: B8000
0	RW	0	**Integrated TV Shadow Register Enable** 0: Disable 1: Enable

IO Port / Index: 3C5.53
DAC Sense Control Register 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Vertical Line Count for Sense** Programming which line that HW can assert HW_SENSE

IO Port / Index: 3C5.54
DAC Sense Control Register 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Horizontal Pixel Count for Sense Start** Programming which pixel that HW asserts HW_SENSE

IO Port / Index: 3C5.55
DAC Sense Control Register 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Horizontal Pixel Count for Sense End** Programming which pixel that HW asserts HW_SENSE

IO Port / Index: 3C5.56
DAC Sense Control Register 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Reserved**
4	RW	0	**HCNT_SENSE_CLR[8]**
3	RW	0	**HCNT_SENSE_SET[8]**
2:0	RW	0	**VCNT_SENSE[10:8]**

IO Port / Index: 3C5.57
P4 / K8 Control Register 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Display Queue Request Expire Number [5]**
5	RW	0	**NB FIFO Delay Mode** 0: Original 1: Delay 1 Cycle
4	RW	0	**Display FIFO Threshold Select Bit [7]**
3	RW	0	**Display FIFO Depth Select Bit [8]**
2	RW	0	**Display FIFO Threshold High Select Bit [7]**
1	RW	0	**NB FIFO Extended Source Select** 0: IGA1 1: IGA2
0	RW	0	**NB FIFO Length Extended Control** 0: Disable 1: Enable

IO Port / Index: 3C5.58
GFX Power Control Register 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Display FIFO Low Threshold Select** HW will multiples the value by 4 to handle

IO Port / Index: 3C5.59
GFX Power Control Register 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**IGA1 Enable** When IGA1 engine is active, this bit need to set to 1
6	RO	0	**Reserved**
5	RW	0	**IGA Low Threshold Enable** 0: Disable 1: Enable
4	RW	0	**GFX-NB IGA Vertical Blanking Enable** 0: Disable 1: Enable
3	RW	0	**GFX-NB PCIC Dynamic Clock Enable** 0: Disable 1: Enable
2	RW	0	**GFX-NB GMINT Channel 1 Dynamic Clock Enable** 0: Disable 1: Enable
1	RW	0	**GFX-NB GMINT Channel 0 Dynamic Clock Enable** 0: Disable 1: Enable
0	RW	0	**GFX-NB AGP Dynamic Clock Enable** 0: Disable 1: Enable

IO Port / Index: 3C5.5A
PCI Bus Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**Scratch Pad Register Shadow Access** 0: For Rx3C5.32/33/34, Rx3X5.49-4F, Rx3C5.39/3A, Rx3X5.3B-3F (total 17) addresses map to original registers 1: For Rx3C5.32/33/34, Rx3X5.49-4F, Rx3C5.39/3A, Rx3X5.3B-3F (total 17) addresses map to secondary registers

IO Port / Index: 3C5.5B

Device Used Status 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**DCVI Source Selection Flag** 0:Graphic 1:TV
6	RO	0	**DAC0 User Flag** 0: Graphic 1: TV
5	RO	0	**DAC0 Used IGA1 Source Flag** 0: No use 1: Use
4	RO	0	**DAC0 Used IGA2 Source Flag** 0: No use 1: Use
3	RO	0	**LVDS0 Used IGA1 Source Flag** - ***Refer to LVDS / DVI chapter for details***
2	RO	0	**LVDS0 Used IGA2 Source Flag** - ***Refer to LVDS / DVI chapter for details***
1	RO	0	**LVDS1 Used IGA1 Source Flag** - ***Refer to LVDS / DVI chapter for details***
0	RO	0	**LVDS1 Used IGA2 Source Flag**- ***Refer to LVDS / DVI chapter for details***

IO Port / Index: 3C5.5C

Device Used Status 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RO	0	**DVP1 Used IGA1 Source Flag** 0: No use 1: Use
0	RO	0	**DVP1 Used IGA2 Source Flag** 0: No use 1: Use

IO Port / Index: 3C5.5D

Timer Control Register **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Timer Status** When the bit is asserted, it means the timer is reached.
6:0	RW	0	**Timer Step Setting** Countdown step value for timer. (one step is about 10us (8.9us))

IO Port / Index: 3C5.5E
DAC Control Register 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**DAC3 OFF for TV (B / CVBS)** This bit is ignored when TVREG.6C[12] = 0
2	RW	0	**DAC2 OFF for TV (G / Luma)** This bit is ignored when TVREG.6C[12] = 0
1	RW	0	**DAC1 OFF for TV (R / Chroma)** This bit is ignored when TVREG.6C[12] = 0
0	RW	0	**CRT DACOFF Setting** When this bit is 1, CRT DACOFF signal will be controlled by screen off register (Rx3C5.01[5]).

IO Port / Index: 3C5.60
I2C Mode Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**I2C Byte Count** This field is programmed with the data transfer count (a value between 0 and 15)
3	RW	0	**Internal Timer Count using Clock Divided by 2** 0: Counter using original clock 1: Counter using clock divided by 2
2	RW	0	**NO STOP Command Generation** When this bit is enable, master controller finishes the transaction without STOP
1	RW	0	**I2C Mode** 0: Standard mode 1: Fast mode
0	RW	0	**I2C Master Interrupt Enable** 0: Disable interrupt generation 1: Enable generation of interrupts on completion of the current transaction

IO Port / Index: 3C5.61
I2C Host Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RW	0	**I2C Host Address** This field contains the 7 bit address of the targeted slave device
0	RW	0	**I2C Write or Read** 0: Write 1: Read

IO Port / Index: 3C5.62
I2C Host Data **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**I2C Host Data** Hardware supports the queue of 2-byte data. Reads and writes to this register are used to access the 2-byte data queue. An internal index pointer is used to address the queue. It is reset to 0 by reads of the I2C Host Control register and incremented automatically by each access to this register.

IO Port / Index: 3C5.63

Device Used Status 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Software Reset** 0: Normal function 1: Reset I2C master controller
6	RW	0	**No Active Driving to High before Release the Bus** 0: Driving to high 1: No driving to high
5	RW	0	**Which Port I2C Master Process** 0: 31h 1: 2Ch
4	RW	0	**I2C Master Clock Control** 0: Disable 1: Enable
3:2	RO	0	**Reserved**
1	RW	0	**Kill Transaction in Progress** 0: Normal master controller operation 1: Stop transaction currently in progress
0	RW	0	**Fire** 0: No effect 1: Writing one to this bit causes master controller to start transaction

IO Port / Index: 3C5.64

I2C Status **Default Value: 40h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	1	**Queue Empty Status** When this bit is one, it means hardware queue is empty.
4	R/WC	0	**I2C Data Transferred Status**
3	R/WC	0	**I2C Transaction Done Status**
2	R/WC	0	**I2C Abnormal Status**
1	RW	0	**Queue Full Status** When this bit is one, it means hardware queue is full.
0	RW	0	**Master Busy Status** When this bit is one, it means master controller is busy processing a command

IO Port / Index: 3C5.65

Power Management Control 6 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:2	RW	0	**DVP1 Clock Pads Driving Select** 00 (Low) ←→ 11 (high)
1:0	RW	0	**DVP1 Data Pads Driving Select** 00 (Low) ←→ 11 (high)

IO Port / Index: 3C5.66

DVI Interrupt Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DVI Sense Interrupt Enable** 0: Disable 1: Enable
6	RW1C	0	**DVI Sense Interrupt Status**
5	RW	0	**Inside DVI Sense** 0: No connect 1: Connected
4:0	RO	0	**Reserved**

Graphics Controller Extended Register

This section describes the graphics controller extended register definitions in detail.

IO Port / Index: 3CF.20
Offset Register Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Offset Register A Overflow Bit 9**
5	RW	0	**Offset Register A Overflow Bit 8**
4	RW	0	**Offset Register B Overflow Bit 8**
3:2	RO	0	**Reserved**
1	RW	0	**Offset Read/Write Control** 0: Offset A (Rx3CF.21) and B (Rx3CF.22) as read/write 1: Offset A as write and offset B as read
0	RW	0	**Offset Configuration** 0: Offset A and B configured as 64KB 1: Offset A and B configured as 16KB

IO Port / Index: 3CF.21
Offset Register A **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Offset A**

IO Port / Index: 3CF.22
Offset Register B **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Offset B**

CRT Controller Extended Registers

This section provides detail CRT controller extended register bit definitions. The "X" contained within the I/O port address stands for **"B"** during monochrome mode and is changed to **"D"** in color mode. For example, the I/O index for Mode Control register will be **Rx3B5.32** in monochrome mode and **Rx3D5.32** in color mode.

IO Port / Index: 3X5.30

Display Fetch Blocking Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**IGA1 Digital Interface Test Enable** 0: Disable 1: Enable
6	RW	0	**Convert Primary Display Data From RGB TO YcbCr** 0: Disable 1: Enable
5	RW	0	**FTTYPE1. DAC Vref Select**
4:3	RW	0	**DR. DAC Speed Enhancement**
2	RW	0	**On / Off Power Now Signals in Primary Path** 0: Disable 1: Enable
1:0	RW	0	**Block T_REQ Path** 0x: Disable 10: Block request within the vertical & horizontal display area 11: Block request within the vertical display area

IO Port / Index: 3X5.32

Display Fetch Blocking Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**HSYNC Delay Number by VCLK** 000: No delay 001: Delay + 4 VCKs 010: Delay + 8 VCKs 011: Delay + 12 VCKs 100: Delay + 16 VCKs 101: Delay + 20 VCKs Others: Undefined
4	RO	0	**Reserved**
3	RW	0	**CRT SYNC Driving Selection** 0: Low 1: High
2	RW	0	**Display End Blanking Enable** 0: Disable 1: Enable
1	RW	0	**Digital Video Port (DVP) Grammar Correction** If the Grammar correction of primary display is turned on, the grammar correction in DVP can be enabled/disabled by this bit. 0: Disable 1: Enable
0	RW	0	**Real-Time Flipping** 0: Flip by the frame 1: Flip by each scan line

IO Port / Index: 3X5.33
HSYNCH Adjuster **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Primary Display Gamma Correction** 0: Disable 1: Enable
6	RW	0	**Primary Display Interlace Mode**
5	RW	0	**Horizontal Blanking End Bit [6]**
4	RW	0	**HSYNC Start Bit [8]**
3	RW	0	**Prefetch Mode** 0: Disable 1: Enable
2:0	RW	0	**The value will shift the HSYNC to be early than planned** 000: Shift to early time by 3 character (VGA mode sugested value; default value) 001: Shift to early time by 4 character 010: Shift to early time by 5 character 011: Shift to early time by 6 character 100: Shift to early time by 7 character 101: Shift to early time by 0 character (Non-VGA mode sugested value) 110: Shift to early time by 1 character 111: Shift to early time by 2 character

IO Port / Index: 3X5.34
Starting Address Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Starting Address Overflow Bits [23:16]**

IO Port / Index: 3X5.35
Extended Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Offset Bits [10:8]**
4	RW	0	**Line Compare Bit [10]**
3	RW	0	**Vertical Blanking Start Bit [10]**
2	RW	0	**Vertical Display End Bit [10]**
1	RW	0	**Vertical Retrace Start Bit [10]**
0	RW	0	**Vertical Total Bit [10]**

IO Port / Index: 3X5.36
Power Management 3 (Monitor Control) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DPMS VSYNC Output**
6	RW	0	**DPMS HSYNC Output**
5:4	RW	0	**DPMS Control** 00: On 01: Stand-by 10: Suspend 11: Off When the DPMS state is off, both HSYNC and VSYNC are grounded, saving monitor power consumption.
3	RW	0	**Horizontal Total Bit [8]**
2:1	RO	0	**Reserved**
0	RW	0	**PCI Power Management Control** 0: Disable 1: Enable

IO Port / Index: 3X5.37
DAC Control Register **Default Value: 04h**

Bit	Attribute	Default	Description
7	RW	0	**DAC Power Save Control 1** 0: Depend on Rx3X5.37[5:4] setting 1: DAC always goes into power save mode
6	RW	0	**DAC Power Down Control** 0: Depend on Rx3X5.47[2] setting 1: DAC never goes to power down mode
5:4	RW	0	**DAC Power Save Control 2** 00: DAC never goes to power save mode 01: DAC goes to power save mode by line 10: DAC goes to power save mode by frame 11: DAC goes to power save mode by line and frame
3	RW	0	**DAC PEDESTAL Control**
2:0	RW	100b	**DAC Factor**

IO Port / Index: 3X5.38
Signature Data Register B0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Signature Data Register B0**

IO Port / Index: 3X5.39
Signature Data Register B1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Signature Data Register B1**

IO Port / Index: 3X5.3A
Signature Data Register B2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Signature Data Register B2**

IO Port / Index: 3X5.3B
Scratch Pad Register 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Scratch Pad Register 2**

IO Port / Index: 3X5.3C
Scratch Pad Register 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Scratch Pad Register 3**

IO Port / Index: 3X5.3D
Scratch Pad Register 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Scratch Pad Register 4**

IO Port / Index: 3X5.3E
Scratch Pad Register 5 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Scratch Pad Register 5**

IO Port / Index: 3X5.3F
Scratch Pad Register 6 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Scratch Pad Register 6**

IO Port / Index: 3X5.40
Test Mode Control 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Test Group Select**
3	RW	0	**Test Mode Control** 0: Disable 1: Enable
2	RW	0	**Signature Test Source** 0: Primary display 1: Secondary display
1	RW	0	**Signature Test Enable** 0: Disable 1: Enable
0	RW	0	**DAC Test Mode Control Enable** 0: Disable 1: Enable Data come from MDI[23:0].

IO Port / Index: 3X5.43
IGA1 Display Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**IGA1 10 Bit Gamma Algorithm LUT256 Index 0 for Color 0** 0: Color 0 always output 10'b0 1: Color 0 output value from index 0' data
2	RW	0	**IGA1 Address Mode Selection** 0: Linear 1: Tile
1	RW	0	**IGA1 Hardware 10 bit Gamma Enable** 0: Disable 1: Enable
0	RW	0	**IGA1 Extend 10 bit Mode LSB Selection** 0: Always 00b 1: MSB bits

IO Port / Index: 3X5.45
Power Now Indicator Control 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**Display FIFO Threshold for Power Now Indicator bit [7]**

IO Port / Index: 3X5.46
Test Mode Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Load a value to the Vertical Counter**

IO Port / Index: 3X5.47
Test Mode Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**IGA1 Timing Plus 2 VCK**
6	RW	0	**IGA1 Timing Plus 4 VCK**
5	RW	0	**Peep at the PCI-bus** 0: Disable 1: Enable
4	RO	0	**Reserved**
3	RW	0	**IGA1 Timing Plus 6 VCK**
2	RW	0	**DACOFF Backdoor Register**
1	RW	0	**LCD Simultaneous Mode Backdoor Register for 8/9 Dot Clocks**
0	RW	0	**LCD Simultaneous Mode Backdoor Register for Clock Select and CRTC Register Protect**

IO Port / Index: 3X5.48
Starting Address Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Starting Address Overflow Bits[28:24]**

Secondary Display Registers

This section describes the secondary display I/O register bit definitions. The "X" contained within the I/O port address stands for **"B"** during monochrome mode and is changed to **"D"** in color mode. For example, the I/O index for the Second CRTC horizontal Total Period register will be **Rx3B5.50** in monochrome mode and **Rx3D5.50** in color mode.

IO Port / Index: 3X5.50
Second CRTC Horizontal Total Period **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Second CRTC Horizontal Total Period**

IO Port / Index: 3X5.51
Second CRTC Horizontal Active Data Period **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Second CRTC Horizontal Active Data Period**

IO Port / Index: 3X5.52
Second CRTC Horizontal Blanking Start **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Second CRTC Horizontal Blanking Start**

IO Port / Index: 3X5.53
Second CRTC Horizontal Blanking End **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Second CRTC Horizontal Blanking End**

IO Port / Index: 3X5.54
Second CRTC Horizontal Blanking Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Horizontal Retrace Start Bit [9:8]**
5:3	RW	0	**Horizontal Blanking End Bit [10:8]**
2:0	RW	0	**Horizontal Blanking Start Bit [10:8]**

IO Port / Index: 3X5.55
Second CRTC Horizontal Period Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	0	**Horizontal Blanking End Bit [10:8]**
3:0	RW	0	**Horizontal Blanking Start Bit [10:8]**

IO Port / Index: 3X5.56
Second CRTC Horizontal Retrace Start **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Horizontal Retrace Start Bit [7:0]**

IO Port / Index: 3X5.57
Second CRTC Horizontal Retrace End **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Horizontal Retrace End**

IO Port / Index: 3X5.58
Second CRTC Vertical Total Period **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Vertical Total Period [7:0]

IO Port / Index: 3X5.59
Second CRTC Vertical Active Data Period **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Vertical Active Data Period Bit [7:0]

IO Port / Index: 3X5.5A
Second CRTC Vertical Blanking Start **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Vertical Blanking Start Bit [7:0]

IO Port / Index: 3X5.5B
Second CRTC Vertical Blanking End **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Vertical Blanking End Bit [7:0]

IO Port / Index: 3X5.5C
Second CRTC Vertical Blanking Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	Horizontal Retrace Bit [10]
6	RW	0	Horizontal Retrace End Bit [8]
5:3	RW	0	Vertical Blanking End Bit [10:8]
2:0	RW	0	Vertical Blanking Start Bit [10:8]

IO Port / Index: 3X5.5D
Second CRTC Vertical Period Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	Horizontal Retrace Start bit[11]
6	RW	0	Horizontal Blanking End bit[11]
5:3	RW	0	Vertical Active Data Period Bit [10:8]
2:0	RW	0	Vertical Total Period bit [10:8]

IO Port / Index: 3X5.5E
Second CRTC Vertical Retrace Start **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Vertical Retrace Start Bit [7:0]

IO Port / Index: 3X5.5F
Second CRTC Vertical Retrace End **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	Vertical Retrace Start Bit [10:8]
4:0	RW	0	Vertical Retrace End

IO Port / Index: 3X5.60
Second CRTC Vertical Status 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Vertical Count Number [7:0]**

IO Port / Index: 3X5.61
Second CRTC Vertical Status 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Vertical Retrace Status** 1: Retrace Period
6	RO	0	**Vertical Active Data Status** 1: Active Data Period
5	RO	0	**Flip Flag**
4	RO	0	**Power Sequence Flag 0** 0: Invalid 1: Valid
3	RO	0	**Power Sequence Flag 1** 0: Invalid 1: Valid
2:0	RO	0	**Vertical Count Number [10:8]**

IO Port / Index: 3X5.62
Second Display Starting Address Low **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RW	0	**Second Display Starting Address Bit [9:3]** This is quadword boundary.
0	RW	0	**Second Display Address Mode Selection** 0: Linear mode 1: Tile mode

IO Port / Index: 3X5.63
Second Display Starting Address Middle **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Second Display Starting Address Bit [17:10]**

IO Port / Index: 3X5.64
Second Display Starting Address High **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Second Display Starting Address Bit [25:18]**

IO Port / Index: 3X5.65
Second Display Horizontal Quadword Count Data **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Second Display Horizontal Quadword Count Data Bit [25:18]**

IO Port / Index: 3X5.66
Second Display Horizontal Offset **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Second Display Horizontal Offset Bit [10:3] or** **Horizontal Synchronous Point**

IO Port / Index: 3X5.67
Second Display Color Depth and Horizontal Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Color Depth** 00: 8bpp 01: 16bpp 10: 30bpp 11: 32bpp
5	RW	0	**Second Display Interlace Mode**
4	RW	0	**IGA2 Extend 10 Bit Mode LSB Selection** 0: 2'b00 1: MSB[7:6]
3:2	RW	0	**Second Display Horizontal Quadword Count Data Bit [9:8]**
1:0	RW	0	**Second Display Horizontal Offset Bit [12:11]**

IO Port / Index: 3X5.68
Second Display Queue Depth and Read Threshold **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Display Queue Depth [3:0]** Unit 8 level ([5:4] on Rx3X5..95[7] and Rx3X5..94[7])
3:0	RW	0	**Display Queue Read Threshold 1** Unit 4 level ([6:4] on Rx3X5.95[6:4])

IO Port / Index: 3X5.69
Second Display Interrupt Enable and Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**For Write:** **Interrupt Clear** 1: Clear
6	RW	0	**Interrupt Enable** 0: Disable 1: Enable
5:0	RO	0	**Reserved**

IO Port / Index: 3X5.6A
Second Display Channel and LCD Enable **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Second Display Channel Enable** 0: Disable 1: Enable
6	RW	0	**Second Display Channel Reset** 0: Reset
5	RW	0	**Second Display 8/6 Bits LUT** 0: 6-bit 1: 8-bit
4	RW	0	**Horizontal Count by 2** 0: Disable 1: Enable
3	RW	0	**First Hardware Power Sequence** - ***Refer to LVDS / DVI chapter for details***
2	RW	0	**Second Display Channel Vertical Clear** 1: Clear
1	RW	0	**LCD Gamma Enable** 0: Disable 1: Enable
0	RW	0	**LCD Pre-fetch Mode Enable** 0: Disable 1: Enable

IO Port / Index: 3X5.6B

Channel 1 and 2 Clock Mode Selection **Default Value: 00h**

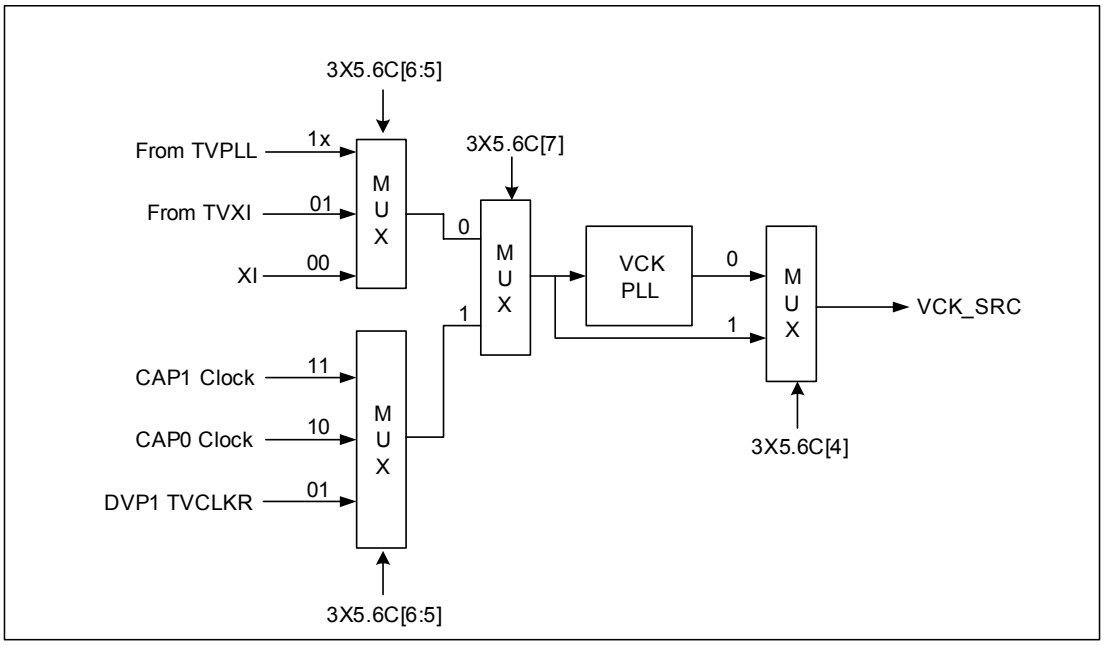
Bit	Attribute	Default	Description
7:6	RW	0	**First Display Channel Clock Mode Selection** 0x: Normal 1x: Division by 2
5:4	RW	0	**Second Display Channel Clock Mode Selection** 0x: Normal 1x: Division by 2
3	RW	0	**Simultaneous Display Enable** 0: Disable 1: Enable
2	RW	0	**IGA2 Screen Off** 0: Normal 1: Screen off
1	RW	0	**IGA2 Screen Off Selection Method** 0: IGA2 Screen off 1: IGA1 Screen off
0	RO	0	**Reserved**

IO Port / Index: 3X5.6C

TV CLK Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**VCK PLL Reference Clock Source Selection** 000: From XI pin 001: From TVXI 01x: From TVPLL 100: Reserved 101: DVP1TVCLKR 110: CAP0 Clock 111: CAP1 Clock
4	RW	0	**VCK Source Selection** 0: VCK PLL output clock 1: VCK PLL reference clock
3:1	RW	0	**LCDCK PLL Reference Clock Source Selection** 000: From XI pin 001: From TVXI 01x: From TVPLL 100: Reserved 101: DVP1TVCLKR 110: CAP0 Clock 111: CAP1 Clock
0	RW	0	**LCDCK Source Selection** 0: LCDCK PLL output clock 1: LCDCK PLL reference clock

VCK Example:



IO Port / Index: 3X5.6D
Horizontal Total Shadow **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Horizontal Total Bit [7:0]**

IO Port / Index: 3X5.6E
End Horizontal Blanking Shadow **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**End Horizontal Blanking Bit [7:0]**

IO Port / Index: 3X5.6F
Vertical Total Shadow **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Vertical Total Bit [7:0]**

IO Port / Index: 3X5.70
Vertical Display Enable End Shadow **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Vertical Display Enable End Bit [7:0]**

IO Port / Index: 3X5.71
Vertical Display Overflow Shadow **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	0	**Vertical Display Enable End Bit [10:8]**
3	RW	0	**Horizontal Total Bit [8]**
2:0	RW	0	**Vertical Total Bit [10:8]**

IO Port / Index: 3X5.72
Start Vertical Blank Shadow **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Start Vertical Blanking Bit [7:0]

IO Port / Index: 3X5.73
End Vertical Blank Shadow **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	End Vertical Blanking Bit [7:0]

IO Port / Index: 3X5.74
Vertical Blank Overflow Shadow **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	Reserved
6:4	RW	0	Start Vertical Blanking Bit [10:8]
3	RO	0	Reserved
2:0	RW	0	End Vertical Blanking Bit [10:8]

IO Port / Index: 3X5.75
Vertical Retrace Start Shadow **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Vertical Retrace Start Bit [7:0]

IO Port / Index: 3X5.76
Vertical Retrace End Shadow **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	Reserved
6:4	RW	0	Vertical Retrace Start Bit [10:8]
3:0	RW	0	Vertical Retrace End

IO Port / Index: 3X5.77
LCD Horizontal Scaling Factor **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Horizontal Scaling Factor Bit [9:2]

IO Port / Index: 3X5.78
LCD Vertical Scaling Factor **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Vertical Scaling Factor Bit [8:1]

IO Port / Index: 3X5.79
LCD Scaling Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Vertical Scaling Factor Bit [10:9]**
5:4	RW	0	**Horizontal Scaling Factor Bit [11:10]**
3	RW	0	**Vertical Scaling Factor Bit [0]**
2	RO	0	**Reserved**
1	RW	0	**Horizontal Scaling Selection** 0: Duplication 1: Interpolation
0	RW	0	**LCD Scaling Enable** 0: Disable 1: Enable

IO Port / Index: 3X5.7A
LCD Scaling Parameter 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 1**

IO Port / Index: 3X5.7B
LCD Scaling Parameter 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 2**

IO Port / Index: 3X5.7C
LCD Scaling Parameter 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 3**

IO Port / Index: 3X5.7D
LCD Scaling Parameter 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 4**

IO Port / Index: 3X5.7E
LCD Scaling Parameter 5 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 4**

IO Port / Index: 3X5.7F
LCD Scaling Parameter 6 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 6**

IO Port / Index: 3X5.80
LCD Scaling Parameter 7 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 7**

IO Port / Index: 3X5.7F
LCD Scaling Parameter 6 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 6**

IO Port / Index: 3X5.81
LCD Scaling Parameter 8 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 8**

IO Port / Index: 3X5.82
LCD Scaling Parameter 9 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 9**

IO Port / Index: 3X5.83
LCD Scaling Parameter 10 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 10**

IO Port / Index: 3X5.84
LCD Scaling Parameter 11 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 11**

IO Port / Index: 3X5.85
LCD Scaling Parameter 12 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 12**

IO Port / Index: 3X5.86
LCD Scaling Parameter 13 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 13**

IO Port / Index: 3X5.87
LCD Scaling Parameter 14 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 14**

IO Port / Index: 3X5.88
LCD Panel Type **Default Value: 00h**
Refer to LVDS / DVI chapter for more details

IO Port / Index: 3X5.8A
LCD Timing Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	0	**Adjust FLM**
3	RO	0	**Reserved**
2:0	RW	0	**Adjust LP**

IO Port / Index: 3X5.8B
LCD Power Sequence Control 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**TD0 Timer Bit [7:0] (default 32ms)**

IO Port / Index: 3X5.8C
LCD Power Sequence Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**TD1 Timer Bit [7:0] (default 32ms)**

IO Port / Index: 3X5.8D
LCD Power Sequence Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**TD2 Timer Bit [7:0] (default 32ms)**

IO Port / Index: 3X5.8E
LCD Power Sequence Control 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**TD3 Timer Bit [7:0] (default 32ms)**

IO Port / Index: 3X5.8F
LCD Power Sequence Control 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**TD1 Timer [11:8]**
3:0	RW	0	**TD0 Timer [11:8]**

IO Port / Index: 3X5.90
LCD Power Sequence Control 5 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**TD3 Timer [11:8]**
3:0	RW	0	**TD2 Timer [11:8]**

IO Port / Index: 3X5.91
Software Control Power Sequence **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Software Direct On / Off Display Period in the Panel Path** 0: On 1: Off
6	RW	0	**Software On / Off Back Light Directly** 0: On 1: Off
5	RO	0	**Reserved**
4	RW	0	**Software VDD On**
3	RW	0	**Software Data On**
2	RW	0	**Software VEE On**
1	RW	0	**Software Back Light On**
0	RW	0	**Hardware or Software Control Power Sequence** 1: Software Control

IO Port / Index: 3X5.92
Read Threshold 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0	**Read Threshold 2**

IO Port / Index: 3X5.94
Expire Number and Display Queue Extend Bit **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Display Queue Depth [4]**
6:0	RW	0	**Display2 Expire_ Number [6:0]**

IO Port / Index: 3X5.95
Extend Threshold Bit **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Display Queue Depth [5]**
6:4	RW	0	**Read Threshold 1 [6:4]**
3	RO	0	**Reserved**
2:0	RW	0	**Read Threshold 2 [6:4]**

IO Port / Index: 3X5.97
LVDS Channel 2 Function Select 0 **Default Value: 00h**
Refer to LVDS / DVI chapter for more details

IO Port / Index: 3X5.98
LVDS Channel 2 Function Select 1 **Default Value: 00h**
Refer to LVDS / DVI chapter for more details

IO Port / Index: 3X5.99
LVDS Channel 1 Function Select 0 **Default Value: 00h**
Refer to LVDS / DVI chapter for more details

IO Port / Index: 3X5.9A
LVDS Channel 1 Function Select 1 **Default Value: 00h**
Refer to LVDS / DVI chapter for more details

IO Port / Index: 3X5.9B

Digital Video Port 1 Function Select 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DVP1 ALPHA Enable** 0: Disable 1: Enable
6	RW	0	**DVP1 VSYNC Polarity** 0: Positive 1: Negative
5	RW	0	**DVP1 HSYNC Polarity** 0: Positive 1: Negative
4	RW	0	**DVP1 Data Source Selection 0** 0: Primary Display 1: Secondary Display
3	RW	0	**DVP1 Clock Polarity**
2:0	RW	0	**DVP1 Clock Adjust**

IO Port / Index: 3X5.9C

Digital Video Port 1 Function Select 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Reserved**

IO Port / Index: 3X5.9D

Power Now Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Specifies the Indicator Ending Reference Point in the Vertical Blanking Period** 0: Use vertical retrace starting position 1: Use bit[6:0] of this register
6:3	RO	0	**Reserved**
2:0	RW	0	**Ending Position of Power Now Indicator**

IO Port / Index: 3X5.9E

Power Now Control 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Use Which Condition As The Power Now Indicator** 0: Active in the vertical blanking area 1: Active while display FIFO is almost full (refer bit[6:0])or vertical blanking period
6:0	RW	0	**Display FIFO Threshold for Power Now Indicator** The value must be divided by 4

IO Port / Index: 3X5.9F
Power Now Control 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable the Power Now Indicator** 0: Disable 1: Enable
6:2	RO	0	**Reserved**
1:0	RW	0	**Horizontal Scaling Factor Bit [1:0]**

IO Port / Index: 3X5.A0
Horizontal Scaling Initial Value **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Horizontal Scaling Initial Value** Add on scaling factor high 8 bit

IO Port / Index: 3X5.A1
Vertical Scaling Initial Value **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Vertical Scaling Initial Value** Add on scaling factor high 8 bit

IO Port / Index: 3X5.A2
Scaling Enable Bit **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Horizontal Scaling Enable Bit**
6	RW	0	**Horizontal Scaling Factor Selection** 0: Original 1: Linear Mode
5:4	RO	0	**Reserved**
3	RW	0	**Vertical; Scaling Enable Bit**
2:0	RO	0	**Reserved**

IO Port / Index: 3X5.A3
Second Display Starting Address Extended **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RW	0	**Second Display Starting Address Bit [28:26]**

IO Port / Index: 3X5.A4
Spectrum FIFO Control Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**Spectrum FIFO Line Reset in vertical Active Region**
2	RW	0	**Spectrum FIFO Line Reset in vertical Blanking Region**
1:0	RO	0	**Reserved**

IO Port / Index: 3X5.A5
Second LCD Vertical Scaling Factor **Default Value: 00h**

Bit	Attribute	Default	Description
1:0	RO	0	**Second LCD Vertical Scaling Factor [8:1]**

IO Port / Index: 3X5.A6
Second LCD Vertical Scaling Factor **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2	RW	0	**Second Vertical Scaling Factor[0]**
1:0	RW	0	**Second Vertical Scaling Factor[10:9]**

IO Port / Index: 3X5.A7
Expected IGA1 Vertical Display End **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Expected IGA1 Vertical Display End [7:0]**

IO Port / Index: 3X5.A8
Expected IGA1 Vertical Display End **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RW	0	**Expected IGA1 Vertical Display End [10:8]**

IO Port / Index: 3X5.A9
Hardware Gamma Control Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RW	0	**Hardware 10 bit Gamma Enable**
0	RW	0	**10 Bit Gamma Algorithm LUT256 Index 0 for Color0** 0: Color0 always output 10'b0

IO Port / Index: 3X5.AA
FIFO Depth & Threshold Overflow Bit **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Reserved**

IO Port / Index: 3X5.AB
IGA2 Interlace Half Line Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**IGA2 Interlace Half Line Register [7:0]**

IO Port / Index: 3X5.AC
IGA2 Interlace Half Line Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RW	0	**IGA2 Interlace Half Line Register [10:8]**

IO Port / Index: 3X5.D0
LVDS PLL Control Register **Default Value: 00h**
Refer to LVDS / DVI chapter for more details

IO Port / Index: 3X5.D1
DVI PLL Control Register **Default Value: 00h**
Refer to LVDS / DVI chapter for more details

IO Port / Index: 3X5.D2
LVDS / DVI Control Register **Default Value: 00h**
Refer to LVDS / DVI chapter for more details

IO Port / Index: 3X5.D3
Second Power Sequence Control Register 0 **Default Value: 00h**
Refer to LVDS / DVI chapter for more details

IO Port / Index: 3X5.D4
Second Power Sequence Control Register 1 **Default Value: 00h**
Refer to LVDS / DVI chapter for more details

IO Port / Index: 3X5.D5
LVDS Setting Mode Control Register **Default Value: 00h**
Refer to LVDS / DVI chapter for more details

IO Port / Index: 3X5.D6
DCVI Control Register 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DCVI Data Testing Mode** 0: Disable 1: Enable
6	RW	0	**DCVI Format Selection** 0: 656 or 601 output 1: 20 bit output
5	RW	0	**DVCI Format Source Selection High Bit** 0: Reference Rx3X5.9B[4] 1: P2I mode
4	RO	0	**Reserved**
3	RW	0	**DCVI Output Format Selection** 0: Original 1: TV5 mode
2	RW	0	**DCVI Dither Enable**
1:0	RW	0	**DCVI Color Space Convert Enable**

IO Port / Index: 3X5.D7
DCVI Control Register 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**DCVI Output Field Polarity** 0: Original 1: Invert
2:0	RW	0	**DCVI Field Delay Lines After Vertical Blank Start**

2D ENGINE REGISTER SPACE

This chapter provides 2D register summary table and detailed graphics engine register descriptions.

2D Engine Registers

These 2D engine register table documents the I/O port, I/O index and attribute ("Attribute") for each register. Attribute definitions being used are RW (Read/Write), RO (Read/Only), and RWC (or just WC) (Read / Write 1's to Clear individual bits). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions for details). All offset and default values are shown in hexadecimal unless otherwise indicated.

Table 9. Graphics Engine Registers

Offset	2D Engine Registers	Attribute
000	GE Command	RW
004	GE Mode and Status	RW
008	BitBLT Source Address	RW
00C	BitBLT Destination Address	RW
010	Dimension	RW
014	Pattern Address	RW
018	Foreground Color or Destination Color Key	RW
01C	Background Color or Source Color key	RW
020	Scissors Top and Left Limit	RW
024	Scissors Bottom and Right Limit	RW
028	Offset	RW
02C	Direct3D Control	RW
030	Source Map Base Address	RW
034	Destination Map Base Address	RW
038	Pitch	RW
03C	Mono Pattern Data Port 0	WO
040	Mono Pattern Data Port 1	WO
044	Rotation Temporary Memory Base Address **(Only for Group A)**	RW
048	Resolution of Rotation Source **(Only for Group A)**	RW
04C	Pitch of Rotation Temporary Memory **(Only for Group A)**	RW
050	Resolution of Rotation Destination **(Only for Group A)**	RW
054	Foreground Color of Pattern **(Only for Group A)**	WO
060	3D / 2D ID Control **(Only for Group A)**	RW
06C	3D / 2D Wait Control **(Only for Group A)**	RW
1FC-100	Color Pattern RAM Port0~63	WO
400	Engine Status	WO
43C	Transmission Setting	WO
440	Transmission Space **(For Virtue Queue)**	WO

Note: Port Address: MB1 + Offset Address

Graphics Engine Register Descriptions

This section provides detailed register descriptions for the 2D graphics engine.

Offset Address: 000h

GE Command **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RW	0	**Raster Operation Code**
23	RW	0	**Quick Start Enable** 0: Disable 1: Enable When enabled, a command will be kicked off when a command writes to register 10h, saving one command write instruction.
22	RW	0	**Pattern Source** 0: Must get somewhere (Bitmap pattern register or frame buffer) to pattern RAM 1: Current pattern RAM (Directly use pattern RAM data without fill it again)
21	RW	0	**Line Draw Major** 0: X Major 1: Y Major
20	RW	0	**Line Draw Last Pixel Turn On Enable** 0: Enable 1: Disable
19:18	RW	0	**Monochrome Data Next Line Alignment Type** 00: Byte 01: Word 10: Dword 11: Qword
17	RW	0	**Monochrome Data Alignment Enable** 0: Disable 1: Enable
16	RW	0	**Monochrome Pattern Transparency** 0: opaque 1: Transparency
15	RW	0	**Destination X-direction Select** 0: Increment 1: Decrement
14	RW	0	**Destination Y-direction Select** 0: Increment 1: Decrement
13	RW	0	**Fix Color Pattern** 0: Normal 1: Fix Color
12	RW	0	**Clipping Select** 0: Disable 1: Enable
11	RW	0	**Pattern Source Select** 0: Pattern from frame buffer 1: Pattern from pattern register
10	RW	0	**Monochrome Source Transparency** 0: Opaque 1: Transparency
9	RW	0	**Pattern Data Format** 0: Color 1: Monochrome
8	RW	0	**Source Data Format** 0: Color 1: Monochrome
7	RO	0	**Reserved**
6	RW	0	**Source Select** 0: Frame Buffer 1: System Memory
5	RW	0	**Destination Address Type Select** 0: X-Y Address 1: Line Address
4	RW	0	**Source Address Type Select** 0: X-Y Address 1: Linear Address

3:0	RW	0	**GE Command Select** 0000: No operation 0001: Bit BLT 0010: Text (Mono, ROP == CC) 0101: Bresenham Line Draw 1001: Bitblt then rotate 1010: Text (Mono, ROP == CC) then rotate Others: Reserved

Offset Address: 004h

GE Mode and Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:10	RO	0	**Reserved**
9:8	RW	0	**Color Depth Select** 00: 8bpp 01: 16bpp (Could be 555 or 565 format) 10: Reserved 11: 32bpp
7:2	RO	0	**Reserved**
1:0	RW	0	**Rotation Angle** 00: Rotate 0 degree 01: Rotate anticlockwise 90 degree 10: Rotate anticlockwise 180 degree 11: Rotate anticlockwise 270 degree

Offset Address: 008h

BitBLT Source Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RO	0	**Reserved**
29:16	RW	0	**BitBILT Source Address** These bits are used for three different commands: 1. For color or mono BitBLT, [27:16] specify the source y-position (XY based). 2. For linear address BitBLT, [28:16] specify the upper 10 bits of source address. 3. For line draw, [29:16] specify the axial step (K1 term of Bresenham line draw).
15:0	RW	0	**BitBILT Source Address** These bits are used for four different commands: 1. For color BitBLT, [11:0] specify the source x-position (XY based). 2. For mono BitBLT, [14:0] specify the source x-position. 3. For linear address BitBLT, [15:0] specify the lower 16 bits of source address. 4. For line draw, [13:0] specify the diagonal step (K2 term of Bresenham line draw).

Offset Address: 00Ch

BitBLT Destination Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:16	RW	0	**BitBILT Destination Address** These bits are used for two different commands: 1. For BitBLT, [27:16] specify the destination of y-position. 2. For linear address BitBLT, [28:16] specify the upper 7 bits of destination address.
15:0	RW	0	**BitBILT Destination Address** These bits are used for two different commands: 1. For BitBLT, [11:0] specify the destination x-position. 2. For linear address BitBLT, [15:0] specify the lower 16 bits of destination address.

Offset Address: 010h

Dimension **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:16	RW	0	These bits specify the rectangle height (value = height–1) for the BitBLT operation.
15:12	RO	0	**Reserved**
11:0	RW	0	These bits specify the rectangle width (value = width-1) for the BitBLT operation.

Offset Address: 014h

Pattern Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RW	0	**Pattern Offset** [31:29]: Start line location (0~7) [28:26]: Start location in a line (0~7)
25:0	RW	0	**Pattern Base Address** These bits are used for the following purpose: For 8x8 pattern, [22:0] specify the 8x8 pattern address stored in the off-screen frame buffer, Qword alignment.

Offset Address: 018h

Foreground Color or Destination Color Key **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**For 256 Color Mode:** Bits [7:0] specify foreground color or destination color key. **For 555 Hi Color Mode:** Bits [14:0] specify foreground color or destination color key. **For 565 Hi Color Mode:** Bits [15:0] specify foreground color or destination color key. **For 32-bit True Color Mode:** Bits [31:0] specify foreground color or destination color key.

Offset Address: 01Ch

Background Color or Source Color Key **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**For 256 Color Mode:** Bits [7:0] specify background color or destination color key. **For 555 Hi Color Mode:** Bits [14:0] specify background color or destination color key. **For 565 Hi Color Mode:** Bits [15:0] specify background color or destination color key. **For 32-bit True Color Mode:** Bits [31:0] specify background color or destination color key.

Offset Address: 020h

Scissors Top and Left Limit **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:16	RW	0	For clipping operation, these bits specify the top limit.
15:12	RO	0	**Reserved**
11:0	RW	0	For clipping operation, these bits specify the left limit.

Offset Address: 024h

Scissors Bottom and Right Limit **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:16	RW	0	For clipping operation, these bits specify the bottom limit.
15:12	RO	0	**Reserved**
11:0	RW	0	For clipping operation, these bits specify the right limit.

Offset Address: 028h

Offset **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RW	0	**These bits are used for two different commands** 1. For linear address BitBLT, [29:16], specify the destination offset (pitch and byte address). 2. For line draw, [31:16] specify the error term for textured line.
15	RO	0	**Reserved**
14	RW	0	**Line Drawing Repeat Counter Control** 0: Always reset 1: Keep the current value
13:0	RW	0	**These bits are used for two different commands** 1. For linear address BitBLT, [13:0] specify the source offset (pitch and byte address). 2. For line draw, [13:0] specify the error term.

Offset Address: 02Ch

Direct 3D Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RW	0	**The Byte Mask of 32bpp** 0: Write 1: Not write
27:16	RO	0	**Reserved**
15	RW	0	**Destination Color Key Select** 0: Disable 1: Enable
14	RW	0	**Source Color Key Select** 0: Disable 1: Enable
13	RW	0	**Color Key Type** 0: Write if different 1: Write if the same
12:0	RO	0	**Reserved**

Offset Address: 030h

Source Map Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RO	0	**Reserved**
25:0	RW	0	**Source Map Base Address and Qword Address** Must be 128-bit alignment

Offset Address: 034h

Destination Map Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RO	0	**Reserved**
25:0	RW	0	**Destination Map Base Address and Qword Address** Must be 128-bit alignment

Offset Address: 038h

Pitch **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**Destination Pitch, Byte Address and 64-bit Address** Must be 128-bit.
15:11	RO	0	**Reserved**
10:0	RW	0	**Source Pith, Byte Address and 64-bit Address** Must be 128-bit.

Offset Address: 03Ch

Mono Pattern Data Port 0 / Style Line **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	WO	0	**Pattern 0**

Offset Address: 040h

Mono Pattern Data Port 1 / Style Line **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	WO	0	**Pattern 1**

Offset Address: 044h

Rotation Temporary Memory Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RO	0	**Reserved**
25:0	RW	0	**Rotation Temporary Memory Base Address** Qword Address

Offset Address: 048h

Resolution X, Y of Rotation Source Service **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:16	RW	0	**Y Resolution-1**
15:12	RO	0	**Reserved**
11:0	RW	0	**X Resolution-1**

Offset Address: 4Ch

Pitch of Rotation Temporary Memory **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:11	RO	0	**Reserved**
10:0	RW	0	**Rotation Tem Pitch** Qword Address

Offset Address: 50h

Resolution X, Y of Rotation Destination **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:16	RW	0	**Y Resolution-1**
15:12	RO	0	**Reserved**
11:0	RW	0	**X Resolution-1**

Offset Address: 54h

Foreground Color of Pattern **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Foreground Color of Mono Pattern**

Offset Address: 60h

3D / 2D ID Control (Only For Group A) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**Reserved**
30	WO	0	**3D/2D Command Force Start. (Software must fill zero)**
29:28	WO	0	**3D/2D Command Status** 00: 3D/2D command start 01: 3D/2D command end 10: 3D/2D command end and wait 3D idle 11: 3D/3D command end and wait 2D idle
27	WO	0	**3D/2D Command Stream Kinds**
26:24	WO	0	**3D/2D Working Buffer Number**
23:16	WO	0	**Reserved for Hardware Use**
15:0	WO	0	**3D/2D Working ID**

Offset Address: 6Ch

3D / 2D Wait Control (Only For Group A) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:14	RO	0	**Reserved**
13	WO	0	**Command wait later IGA VBLK interval to start to work**
12	WO	0	**Command wait former IGA VBLK interval to start to work**
11	WO	0	**Command wait later IGA VBLK end pulse to start to work**
10	WO	0	**Command wait former IGA VBLK end pulse to start to work**
9	WO		**Command wait later IGA VBLK start pulse to start to work**
8	WO	0	**Command wait former IGA VBLK start pulse to start to work**
7:6	RO	0	**Reserved**
5	WO	0	**Command wait LCD VBLK interval to start to work**
4	WO	0	**Command wait CRT VBLK interval to start to work**
3	WO	0	**Command wait LCD VBLK end pulse to start to work**
2	WO	0	**Command wait CRT VBLK end pulse to start to work**
1	WO	0	**Command wait LCD VBLK start pulse to start to work**
0	WO	0	**Command wait CRT VBLK start pulse to start to work**

Offset Address: 1FC-100h

Color Pattern RAM Prot 0 - 63 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	WO	0	**Pattern Data**

Offset Address: 400h

Engine Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
17	WO	0	**Virtue Queue Status** 0: Non-empty 1: Empty
7	WO	0	**Command Regulator Status** 0: Idle 1: Busy
1	WO	0	**2D Engine Status** 0: Idle 1: Busy
0	WO	0	**3D Engine Status** 0: Idle 1: Busy
Others	WO	0	**Status for 3D Engine**

Offset Address: 43Ch

Transmission Setting **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	WO	0	**Parameter Type Sub-code**
23:16	WO	0	**Parameter Type**
16:8	WO	0	**Offset Setting for Some Special Parameter Types**
7:0	WO	0	**The Beginning of Internal Address for Parameter Programming** For Virtual Queue setting, set 00FE 0000h in OF-Address 43Ch first and then set the registers' values in OF-Address 440h.

Offset Address: 440h

Transmission Space (For Virtue Queue) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	WO	0	**Sub-address=00h**
23:0	WO	0	**Register Value**
31:24	WO	0	**Sub-address=00h**
23:0	WO	0	**Virtue Queue Enable** 0: Disable 1: Enable
31:24	WO	0	**Sub-address=50h**
23:0	WO	0	**Lower 3 bytes of Virtue Queue Start Address**
31:24	WO	0	**Sub-address=51h**
23:0	WO	0	**Lower 3 bytes of Virtue Queue End Address**
31:24	WO	0	**Sub-address=52h**
23:16	RO	0	**Reserved**
15:8	WO	0	**The highest bye of Virtue Queue End Address**
7:0	WO	0	**The highest byte of Virtue Queue Start Address**
31:24	WO	0	**Sub-address=53h**
23:0	WO	0	**Length of Virtue Queue**
Bit	WO	0	**Description**
31:24	WO	0	**Sub-adress**
23:16	WO	0	**Parameter Type**
15:8	WO	0	**Offset Setting for Some Special Parameter Types**
7:0	WO	0	**The Beginning of Internal Address for Parameter Programming** For Virtual Queue setting, set 00FE 0000h in OF-Address 43Ch first and then set the registers' values in OF-Address 440h.

DMA REGISTERS

This chapter provides detailed DMA register summary table and register descriptions are followed in the sequent section.

DMA Registers

These DMA register tables document the I/O port, I/O index and attribute ("Attribute") for each register. Attribute definitions being used are RW (Read/Write), RO (Read/Only) and RWC (or just WC) (Read / Write 1's to Clear individual bits). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions for details). All offset and default values are shown in hexadecimal unless otherwise indicated.

Table 10. DMA Controller Operation Registers

Offset	DMA Controller Operation Registers	Attribute
040	Channel 0 Memory Address (MAR0)	RW
044	Channel 0 Device Address (DAR0)	RW
048	Channel 0 Byte Count (BCR0)	RW
04C	Channel 0 Descriptor Pointer (DPR0)	RW
050	Channel 1 Memory Address (MAR1)	RW
054	Channel 1 Device Address (DAR1)	RW
058	Channel 1 Byte Count (BCR1)	RW
05C	Channel 1 Descriptor Pointer (DPR1)	RW
060	Channel 2 Memory Address (MAR2)	RW
064	Channel 2 Device Address (DAR2)	RW
068	Channel 2 Byte Count (BCR2)	RW
06C	Channel 2 Descriptor Pointer (DPR2)	RW
070	Channel 3 Memory Address (MAR3)	RW
074	Channel 3 Device Address (DAR3)	RW
078	Channel 3 Byte Count (BCR3)	RW
07C	Channel 3 Descriptor Pointer (DPR3)	RW
080	Channel 0 Mode (MR0)	RW
084	Channel 1 Mode (MR1)	RW
088	Channel 2 Mode (MR2)	RW
08C	Channel 3 Mode (MR3)	RW
090	Channel 0 Command / Status (CSR0)	RW
094	Channel 1 Command / Status (CSR1)	RW
098	Channel 2 Command / Status (CSR2)	RW
09C	Channel 3 Command / Status (CSR3)	RW
0A0	Priority Type Register (PTR)	RW

1. The offset address for all registers is 0x0E00 and these registers can be re-allocated by changing the base address registers.
2. R/W Attribute Definition

RO	**Read Only**	If a register is read only, write to this register will have no effect
R/W	**Read / Write**	A register with this attribute can be read and written
R/WC	**Read / Write**	A register bit with this attribute can be read and written. However, a write of 1 clears the corresponding bit and a write of 0 has no effects.

3. DMA Controller Access Attribute Abbreviation List

Note 1 Bit 0 and Bit 3 in the register are read only. Other bits are read / write. Bit 3 is fixed as 1 for DPR0 and is fixed as 0 for DPR1.

Note 2 Bits 8 - 31 in the register are read only. Bit 7 is read/write for MR0 and is read only for MR1. Bits 2 – 6 are read only. Other bits are read/write.

Note 3 Bits 3 - 4 in the register are read / write clear. Bits 5 - 31 in the register are read only. Other bits are read / write.

Note4 Bits 8 - 31 in the register are read only. Bit 2 - 7 are read/write. Bit 1 is read only. Bit 0 is read/write.

DMA Operation Registers Description

Following registers are the DMA Operation registers used to control the operation of the DMA controller. Address space mentioned in the following registers (expect MAR) is PCI address space.

Channel n Memory Address (MARn)

Offset Address: **Attribute: RW**

MAR0 0x 40
MAR1 0x 50
MAR2 0x 60
MAR3 0x 70

Bit	Attribute	Default	Description
31:0	RW	0	**Memory Address (MA)** This field indicates the starting memory address of a DMA transfer. In unit of byte

Note: A 32-bit memory-space address (not PCI-space address) is expected in this register. In addition, when the device address is located within the PCI Memory space, the last two bits (bit 1 and bit 0) of memory address and device address must be the same.

Channel n Device Address (MARn)

Offset Address: **Attribute: RW**

MAR0 0x 44
MAR1 0x 54
MAR2 0x 64
MAR3 0x 74

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:2	RW	0	**Device Address (DA)** This field indicates the starting device address of a DMA transfer.
1:0	RO	0	**Reserved**

Channel n Byte Count (BCRn)

Offset Address: **Attribute: RW**

BCR0 0x 48
BCR1 0x 58
BCR2 0x 68
BCR3 0x 78

Bit	Attribute	Default	Description
31:0	RW	0	**Byte Count (BC)** This field indicates the number of bytes to be transferred during a DMA transfer. It will be cleared when the transfer is done by hardware.

Channel n Description Pointer (DRPn)

Offset Address: **Attribute: RW**

DPR0 0x 4C
DPR1 0x 5C
DPR2 0x 6C
DPR3 0x 7C

Bit	Attribute	Default	Description
31:4	RW	0	**Next Descriptor Address (NDA)** This field indicates the double word aligned address (Bit3-0 = 0000) of next descriptor.
3	RW	0	**Direction of Transfer (DT)** A value of 1 indicates transfers from Memory to PCI Device. A value of 0 indicates transfers from PCI Device to Memory. Channel0 and Channel2 are fixed as 1 hus transfers data from system to PCI device. Channel1 and Channel3 are fixed as 0 hus transfers data from PCI device to system.
:2	RW	0	**Descriptor Done Interrupt Enable (DDIE)** A value of 1 cause an interrupt to be generated after the terminal count for this descriptor is reached. A value of 0 disables interrupts from being generated.
1	RW	0	**End of Chain (EC)** A value of 1 indicates the end of chain.
0	RO	0	**Reserved**

Channel n Mode (MRn)

Offset Address: **Attribute: RW**

MR0 0x 80
MR1 0x 84
MR2 0x 88
MR3 0x 8C

Bit	Attribute	Default	Description
31:7	RO	0	**Reserved**
6	RW	0	**HTSDMA_FB** Mothod3
5	RW	0	**HTSDMA_NOFB** Mothod4
4:2	RO	0	**Reserved**
1	RW	0	**Transfer Done Interrupt Enable (TDIE)** A value of 1 enables the interrupt to be generated when transfer is done.
0	RW	0	**Chaining Mode (CM)** A value of 1 causes the DMA controller to operate in Chaining mode.

Channel n Command / Status (CSRn)

Offset Address: **Attribute: RW**

CSR0 0x 90
CSR1 0x 94
CSR2 0x 98
CSR3 0x 9C

Bit	Attribute	Default	Description
31:5	RO	0	**Reserved**
4	RW	0	**Descriptor Done (DD)** A value of 1 indicates the transfer of current descriptor is complete. Writing 1 will clear this bit and the interrupt due to this event when DDIE is set to 1
3	RW	0	**Transfer Done (TD)** A value of 1 indicates the transfer of this channel is complete. Writing 1 will clear this bit and the interrupt due to this event when TDIE is set to 1.
2	RW	0	**Transfer Abort (TA)** Writing 1 to this bit causes the channel to abort the current transfer. The channel enable bit must be cleared. This channel transfer done bit is set when the abort is complete. Reading this bit always gets 0.
1	RW	0	**Transfer Start (TS)** Writing 1 to this bit causes the channel to start transferring data if the channel is enabled. Reading this bit always gets 0.
0	RW	0	**DMA Enable (DE)** A value of 1 enables this DMA channel.

Priority Type Registers (PTR)

Offset Address: A0h **Attribute: RW**

Bit	Attribute	Default	Description
31:8	RO	0	**Reserved**
7:4	RW	0	**Clock Dynamic Control** 0: Disable 1: Enable (ch0, ch1, ch2, ch3)
3:1	RO	0	**Reserved**
0	RW	0	**Priority Type (PT)** A value of 1 indicates the priority type is rotating type. A value of 0 indicates the priority type is fixed type. When the fixed type is selected, channel 0 has the highest priority.

CBU ROTATION REGISTERS

This chapter provides detailed CBU register summary table and detailed register descriptions are followed in the sequent sections.

CBU Registers

These CBU Rotation register tables document the I/O port, I/O index and attribute ("Attribute") for each register. Attribute definitions being used are RW (Read/Write), RO (Read/Only) and RWC (or just WC) (Read / Write 1's to Clear individual bits). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions for details). All offset and default values are shown in hexadecimal unless otherwise indicated.

Table 11. CBU Rotation Function Registers

Offset	DMA Controller Operation Registers	Attribute
1E00	Rotate Control 0	RW
1E04	Rotate Base Address 0	RW
1E08	Rotate End Address 0	RW
1E0C	Rotate Source Pitch 1 0	RW
1E10	Rotate Pitch 0	RW
1E14	Rotate Height and Width 0	RW
1E18	Reserved	RW
1E1C	Reserved	RW
1E3C-1E20	Rotate Window Register 1	RW
1E5C-1E40	Rotate Window Register 2	RW
1E7C-1E60	Rotate Window Register 3	RW
1E80-1E9C	Rotate Window Register 4	RW
1EBC-1EA0	Rotate Window Register 5	RW
1EDC-1EC0	Rotate Window Register 6	RW
1EFC-1EE0	Rotate Window Register 7	RW
1F1C-1F00	Rotate Window Register 8	RW
1F3C-1F20	Rotate Window Register 9	RW
1F5C-1F40	Rotate Window Register 10	RW
1F7C-1F60	Rotate Window Register 11	RW
1F9C-1F80	Rotate Window Register 12	RW
1FAC-1FA0	Rotate Window Register 13	RW
1FCC-1FC0	Rotate Window Register 14	RW
1FFC-1FE0	Rotate Window Register 15	RW

Note: Rotation Base Address[28:16], Rotation End Address[28:16] and Rotation Source Pitch[21:0] are write-only. Read these bits always get 0.

CBU Rotation Registers Description

Offset Address: 1E00h

Rotate Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:7	RO	0	**Reserved**
6	RW	0	**Rotate Function With Tile** When this bit is set to 1, translated linear address to tiling address within rotation mode is supported.
5	RW	0	**Tile Function Flag** When Rotate Function Enable is set to 1, this bit show which function supported. 0: Rotate function 1: Tile function
4:3	RW	0	**Rotate Type** 00: No Support 01: 90 degree 10: 180 degree 11: 270 degree
2:1	RW	0	**Rotate Bpp** 00: 8 bpp 01: 16 bpp 1x: 32 bpp
0	RW	0	**Rotate Function Enable** 0: Disable 1: Enable

Offset Address: 1E04h

Rotate Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:2	RW	0	**Rotate Base Address** Address [28:0] Unit: Byte
1:0	RO	0	**Reserved**

Offset Address: 1E08h

Rotate End Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:2	RW	0	**Rotate End Address** Address [28:0] Unit: Byte
1:0	RO	0	**Reserved**

Offset Address: 1E0Ch

Rotate Source Pitch 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:22	RO	0	**Reserved**
21:0	RW	0	**Rotate Source Pitch Reciprocal** 22bit(1/source pitch, source pitch unit: pixel) (1/sp = 0.x, for ex. Source pitch = 256d, x = 004000h)

Offset Address: 1E10h

Rotate Pitch **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**Rotate Destination Pitch** (Unit: pixel, scope: 1 ~ 2047)
15:11	RO	0	**Reserved**
10:0	RW	0	**Rotate Source Pitch** (Unit: pixel, scope: 1 ~ 2047)

Offset Address: 1E14h

Rotate High and Width **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**Rotate Window Height** (Unit: pixel, scope: 1 ~ 2047)
15:11	RO	0	**Reserved**
10:0	RW	0	**Rotate Window Width** (Unit: pixel, scope: 1 ~ 2047)

INTEGRATED TV ENCODER REGISTERS

This chapter provides detailed Integrated TV Encoder register summary table and detailed register descriptions are followed in the sequent sections.

Integrated TV Encoder Registers Summary

These Integrated TV Encoder register tables document the I/O port, I/O index and attribute ("Attribute") for each register. Attribute definitions being used are RW (Read/Write), RO (Read/Only) and RWC (or just WC) (Read / Write 1's to Clear individual bits). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions for details). All offset and default values are shown in hexadecimal unless otherwise indicated.

All these registers are controlled by 3C5.52[2:0]. 3C5.52[2:1] is the selection of mapping to A0000~B8000. 3C5.52[0] is the selection of mapping to these TV registers or the real memory. If 3C5.52[0]=1'b1, we can write/read these TV registers.

Table 12. Integrated TV Encoder Registers

I/O Port	I/O Index	TV Register	Attribute
A0000	00	TV Encoder Control Register	RW
A0000	04	Source Buffer 0 Base Address	RW
A0000	08	Source Buffer 1 Base Address	RW
A0000	0C	Source Buffer 2 Base Address	RW
A0000	10	Source Buffer 3 Base Address	RW
A0000	14	Source Buffer Line Pitch	RW
A0000	18	Source Image Size	RW
A0000	1C	Source Image Starting Position	RW
A0000	20	Source Image Ending Position	RW
A0000	24	Scaling Factor & De-Flicker Control	RW
A0000	28	Destination Image Size	RW
A0000	2C	Destination Even Buffer Base Address	RW
A0000	30	Destination Odd Buffer Base Address	RW
A0000	34	Destination Buffer Line Pitch & DQWord	RW
A0000	38	Encoder Control Register	RW
A0000	3C	Encoder CRTC Register 0	RW
A0000	40	Encoder CRTC Register 1	RW
A0000	44	Encoder CRTC Register 2	RW
A0000	48	Encoder CRTC Register 3	RW
A0000	4C	Encoder CRTC Register 4	RW
A0000	50	Encoder Chroma Data Control	RW
A0000	54	Encoder Luma Data Control	RW
A0000	58	Encoder FSCI	RW
A0000	5C	Encoder Burst and Sync Shape control	RW
A0000	60	Encoder Hue & Sub-Carrier Adjustment	RW
A0000	64	Encoder Filter Control Register	RW
A0000	68	Second CRT Sense Register	RW
A0000	6C	TV DAC Register and Second CRT Power Management	RW
A0000	70~BC	Reserved	—
A0000	C0	Closed Caption Data Register	RW
A0000	C4~D8	Reserved	—
A0000	DC	TVCLK PLL Register 0	RW
A0000	E0	TVCLK PLL Register 1	RW
A0000	E4	TV Status Register	RO
A0000	E8	TV Blank Level and Sense Register	RW

Integrated TV Encoder Registers Description

I/O Index: 00h

TV Encoder Control Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Scaler and Deflicker Enable**
30	RW	0	**Synchronous Mode and Use Less than One Buffer Size**
29	RW	0	**Memory Data Dither Enable**
28:27	RO	0	**Reserved**
26	RW	0	**Pack Field ID Polarity**
25	RW	0	**SD Sync TV Mode**
24:23	RW	0	**Bypass Mode** x0: Do not bypass 01: P2I bypass mode 11: P2P or I2I bypass mode
22	RW	0	**Memory Data Compress Enable**
21	RW	0	**Source Image Data Type** 0: RGB 1: YCbCr
20	RW	0	**Software Reset** 1: Reset
19	RW	0	**444 to 422 Filter Type** 0:11 1:1331
18	RW	0	**TV Source Selection** 0: From IGA1 1: From IGA2
17	RW	0	**Tile Mode or Linear Mode**
16	RW	0	**FLIP_TYPE** 0: Field base flip mode 1: Frame base flip mode
15:11	RW	0	**Request Signal Threshold Value**
10:6	RW	0	**High Priority Request Threshold Value**
5:1	RW	0	**Request Expire Number**
0	RW	0	**Pack Circuit Enable**

I/O Index: 04h

TV Encoder Control Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:4	RW	0	**Source Buffer 0 Base Address [28:4]**
3:0	RO	0	**Reserved**

I/O Index: 08h

Source Buffer 1 Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:4	RW	0	**Source Buffer 1 Base Address [28:4]**
3:0	RO	0	**Reserved**

I/O Index: 0Ch

Source Buffer 2 Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:4	RW	0	**Source Buffer 2 Base Address [28:4]**
3:0	RO	0	**Reserved**

I/O Index: 10h

Source Buffer 3 Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:4	RW	0	**Source Buffer 3 Base Address [28:4]**
3:0	RO	0	**Reserved**

I/O Index: 14h

Source Buffer Line Pitch **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**Source Buffer Line** How many lines of source buffer we want to use (only for sync buffer mode)
15	RO	0	**Reserved**
14:4	RW	0	**Source Buffer Line Pitch [14:4]**
3:0	RO	0	**Reserved**

I/O Index: 18h

Source Image Size **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:22	RW	0	**SD Engine Segment Line Count** How many lines of SD engine will partition the buffer (only for sync buffer mode)
22:11	RW	0	**Source Image Horizontal Pixels**
10:0	RW	0	**Source Image Vertical Lines**

I/O Index: 1Ch

Source Image Starting Position **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**Reserved**
30	RW	0	**Vertical Scaling Enable**
29	RO	0	**Reserved**
28	RW	0	**Vertical Pre-scaling Enable**
27	RW	0	**Scaling Down Method** 0: Bilinear interpolation 1: Adaptive accumulation
26:16	RW	0	**Source Image Start X Position** The msb is the sign bit
15:11	RO	0	**Reserved**
10:0	RW	0	**Source Image Start Y Position** The msb is the sign bit

I/O Index: 20h

Source Image Ending Position **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RW	0	**De-flicker Threshold Value** Threshold to decide as a high contras edge, bit9~bit5
26:16	RW	0	**Source Image End X Position** Has no sign bit
15:11	RW	0	**De-flicker Threshold Value** Threshold to decide as a high contras edge, bit4~bit0
10:0	RW	0	**Source Image End Y Position** Has no sign bit

I/O Index: 24h

Source Image Starting Position **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Scaler and Deflicker Pre-filter Enable** 0: Disable 1: Enable
30	RW	0	**Non-interlaced to Interlaced Conversion Enable**
29	RW	0	**De-flicker Enable**
28:16	RW	0	**Horizontal Scaling Factor** The msb 2 bits is the integer part
15	RW	0	**Deflicker Type Selection** 0: Normal 1: IIR
14	RW	0	**De-Flicker Weighting Selection** 0: 121 1: 161
13	RW	0	**Measure Points to Determine De-flickering or not** 0: Filtering on whole image 1: One point
12:0	RW	0	**Vertical Scaling Factor** The msb 2 bits is the integer part

I/O Index: 28h

Destination Image Size **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**Reserved**
30:22	RW	0	**Destination Double Quad-Word Number** How many double quad-words at the destination buffer
21:11	RW	0	**Destination Image Horizontal Pixels**
10:0	RW	0	**Destination Image Vertical Lines**

I/O Index: 2Ch

Destination Even Buffer Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:4	RW	0	**Destination Even Buffer Base Address [28:4]**
3:0	RO	0	**Reserved**

I/O Index: 30h

Destination Odd Buffer Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:4	RW	0	**Destination Odd Buffer Base Address [28:4]**
3:0	RO	0	**Reserved**

I/O Index: 34h

Destination Buffer Line Pitch & DQWord **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**Destination Buffer Line Count** How many lines of destination buffer want to be used
15	RO	0	**Reserved**
14:4	RW	0	**Destination Buffer Line Pitch [14:4]**
3:0	RO	0	**Reserved**

I/O Index: 38h

Encoder Control Register **Default Value: 0100 0001h**

Bit	Attribute	Default	Description
31:30	RW	0	**Input Source Selection** 00: Color bar, 01: Capture port 1x: From FB data
29:28	RW	0	**TV DAC1 Output Selection** (CRT & TV shared DAC1, CRT is set as the default) 00: DAC1 A/B/C = C/Y/CVBS 01: DAC1 A/B/C = C/Y/Y 10: DAC1 A/B/C = R/G/B 11: DAC1 A/B/C = Pr/Y/Pb
27:26	RW	0	**TV DAC2 Output Selection** (CRT & TV shared DAC2, TV is set as the default) 00: DAC2 D/E/F = C/Y/CVBS 01: DAC2 D/E/F = C/Y/C 10: DAC2 D/E/F = R/G/B 11: DAC2 D/E/F = Pr/Y/Pb
27:26	RW	0	**TV DAC Output Selection** 00: DAC A/B/C/D = CVBS/C/Y/CVBS 01: DAC A/B/C/D = Y/C/Y/C 10: DAC A/B/C/D = CVBS/R/G/B 11: DAC A/B/C/D = CVBS/Pr/Y/Pb
25	RO	0	**Reserved**
24	RW	1b	**TV Asynchronous Mode Enable**
23:22	RW	0	**TV Output Standard** 00: NTSC, 01: PAL 10: SDTV, 11: HDTV
21:19	RW	0	**TV Line Selection** 000: 525, 001: 625 010: 1125, 011: 1250 1xx: 750
18:17	RW	0	**NTSC or PAL Variation Type** For TV_STAND = 00: 0x: normal NTSC 1x: NTSC 443 For TV_STAND = 01: 0x: normal PAL 10: PAL N, 11: PAL Nc
16	RW	0	**TV Horizontal Scaling Mode** 0: Bi-linear 1: Duplicate
15:11	RW	0	**Request Signal Threshold Value**
10:6	RW	0	**High Priority Request Threshold Value**
5:1	RW	0	**Request Expire Number**
0	RW	1b	**Integrated TV Encoder Enable**

I/O Index: 3Ch

Encoder CRTC Register 0 **Default Value: 007F 06B3h**

Bit	Attribute	Default	Description
31:24	RW	0	**TV Sense Data** When sense enable, this 8-bit data will send to the TV DAC
23:16	RW	7Fh	**TV Horizontal Sync Width**
15:14	RW	0	**TV Sense Enable** 0x: No sense 10: Manual sense enable 11: Auto sense enable
13:12	RO	0	**Reserved**
11:0	RW	0	**TV Horizontal Total Pixels -1**

I/O Index: 40h

Encoder CRTC Register 1 **Default Value: 00EA 00A8h**

Bit	Attribute	Default	Description
31:25	RO	0	**Reserved**
24:16	RW	EAh	**TV Burst End**
15:8	RO	0	**Reserved**
7:0	RW	A8h	**TV Burst Start**

I/O Index: 44h

Encoder CRTC Register 2 **Default Value: 0686 00F9h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:16	RW	86h	**TV Active Video End**
15:9	RO	0	**Reserved**
8:0	RW	F9h	**TV Active Video Start**

I/O Index: 48h

Encoder CRTC Register 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**Reserved**
30:21	RW	0	**TV Horizontal Start Display**
20:9	RW	0	**HDTV Broad Pulse End**
8:0	RW	0	**HDTV Broad Pulse Start**

I/O Index: 4Ch

Encoder CRTC Register 4 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:23	RW	0	**TV Vertical Start Display**
22:11	RW	0	**TV Image Horizontal Position**
10:0	RW	0	**TV Image Vertical Position**

I/O Index: 50h

Encoder Chroma Data Control **Default Value: 0100 0100h**

Bit	Attribute	Default	Description
31	RW	0	**Input Luma Data Shift 64**
30	RW	0	**Input Chroma Data Shift 512**
29	RO	0	**Reserved**
28	RW	0	**TV Component Output Sync on R or B Enable (RGB)**
27:25	RW	0	**U or B Data Delay Depth**
24:16	RW	100b	**U or B Gain Value**
15:13	RO	0	**Reserved**
12	RW	0	**TV Component Output Sync on PB or PR Enable (YPbPr)**
11:9	RW	0	**V or R Data Delay Depth**
8:0	RW	100b	**V or R Gain Value**

I/O Index: 54h

Encoder Luma Data Control **Default Value: 0020 0100h**

Bit	Attribute	Default	Description
31	RW	0	**TV_CSO_HSO Output Port Selection** 1: CSYNC 0: HSYNC
30:23	RW	0	**TV Black Level from Blank Level**
22:14	RW	80h	**TV Blank Level**
13	RW	0	**TV Component Output Sync on Y or G Enable**
12:9	RW	0	**Y or G Data Delay Depth**
8:0	RW	100h	**Y or G Gain Value**

I/O Index: 58h

Encoder FSCI **Default Value: 21F0 2016h**

Bit	Attribute	Default	Description
31:0	RW	21F0 2016h	**TV Sub-carrier Value**

I/O Index: 5Ch

Encoder Burst and Sync Shape Control **Default Value: 0128 1010h**

Bit	Attribute	Default	Description
31	RO	0	**Reserved**
30:23	RW	0	**TV Burst Reset Mode** 000: 1 frame 001: 2 frame 010: 4 frame 011: 8 frame 1xx: Free run
22:14	RO	0	**Reserved**
13	RW	4Ah	**TV Burst Amplitude**
12:9	RW	08h	**TV Burst Step** Control the slop/shape of the burst
8:0	RW	10h	**TV Sync Step** Control the slop/shape of the sync

I/O Index: 60h

Encoder Hue & Sub-Carrier Adjustment **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RW	0	**TV Auto-generate FSCI Mode** 0x: Auto not enabled 10: Auto enabled 11: Auto enabled and fine tune
29:27	RO	0	**Reserved**
26:16	RW	0	**TV Sub-carrier Phase Adjustment**
15:11	RO	0	**Reserved**
10:0	RW	0	**TV Hue Adjustment**

I/O Index: 64h

Encoder Filter Control Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:7	RO	0	**Reserved**
6:4	RW	0	**TV Composite Luma Signal Filter Selection** 000: 3.0 M (L) 001: 4.2 M (L) 010: 4.8 M (L) 011: 6.0 M (L) 100: 3.58 M (N) 101: 4.43 M (N) 110: 8.4 M (L) 111: 9.6 M (L)
3:2	RW	0	**TV Progressive Signal Y Filter Selection** 00: 6.0 M (L) 01: 10 M (L) 10: 24 M (L) 11: 30 M (L)
1:0	RW	0	**TV Composite Signal Chroma Filter Selection** 00: 0.65 M (L) 01: 1.3 M (L) 10: 2.6 M (L) 11: 5.2 M (L)

I/O Index: 68h

Second CRT SENSE Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RO	0	**Reserved**
29	RW	0	**TV Sense Mode Selection** 0: First active line sense 1: According to VCNT_SENSE sense
28:18	RW	0	**Vertical Line Count for Sense** Programming which line that HW can assert HW_SENSE.
17:9	RW	0	**Horizontal Pixel Count for Sense End** Programming which pixel that HW de-asserts HW_SENSE.
8:0	RW	0	**Horizontal Pixel Count for Sense Start** Programming which pixel that HW asserts HW_SENSE

I/O Index: 6Ch

TV DAC Register and Second CRT Power Management Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:13	RO	0	**Reserved**
12	RW	0	**Primary DAC** 0:CRT 1:TV
11:0	RO	0	**Reserved**

I/O Index: C0h

Closed Caption Data Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RW	0	**Second Closed Caption Data Byte of Line 284(335)**
23:16	RW	0	**First Closed Caption Data Byte of Line 284(335)**
15:8	RW	0	**Second Closed Caption Data Byte of Line 21(22)**
7:0	RW	0	**First Closed Caption Data Byte of Line 21(22)**

I/O Index: DCh

TVCLK PLL Register 0 **Default Value: 8000 0000h**

Bit	Attribute	Default	Description
31:30	RW	0	**SD Clock Mode Selection** 0x: Clock always off 10: Clock always on 11: Depend on SD Engine
29:28	RW	0	**TVCK PLL Power Control** 0x: PLL power-off 10: PLL always on 11: PLL on/off according to the PMS
27	RW	0	**Reset TVCK PLL** 1: Reset
26:6	RO	0	**Reserved**
5	RW	0	**Bypass TV Oscillator** Using the external clock generator through XI
3	RW	0	**Double the frequency of TV DAC clock** 1: Double the frequency
3:2	RW	0	**Capture Clock Bypass to TVCLK** 0x: Do not bypass, use the internal TVPLL 10: Capture 0 clock bypass to TVCLK 11: Capture 1 clock bypass to TVCLK
1	RW	0	**Reference Clock Bypass to TVCLK**
0	RW	0	**PLL Output Frequency x 2**

I/O Index: E0h

TVCLK PLL Register 1 **Default Value: 0063 1809h**

Bit	Attribute	Default	Description
31:29	RW	000b	**Loop Filter Resistance Value Selection** 000: R=19K 001: R= 25K 010: R=28K 011: R= 32K 100: R=35K 101: R= 38K 110: R=40K 111: R= 46K
28:26	RW	000b	**Charge Pump Current Selection** 000: Ip= 10.5uA 100: Ip= 15uA 001: Ip= 42nA 110: Ip= 22.5uA
25:21	RW	03h	**PLL Post Divider Value: 3~31**
20:16	RW	03h	**PLL Post Divider-2 Value: 3~31**
15:10	RW	06h	**PLL Pre-divider Value: 1.5~31.5**
9:0	RW	09h	**PLL Feedback Divider Value: 3~1023**

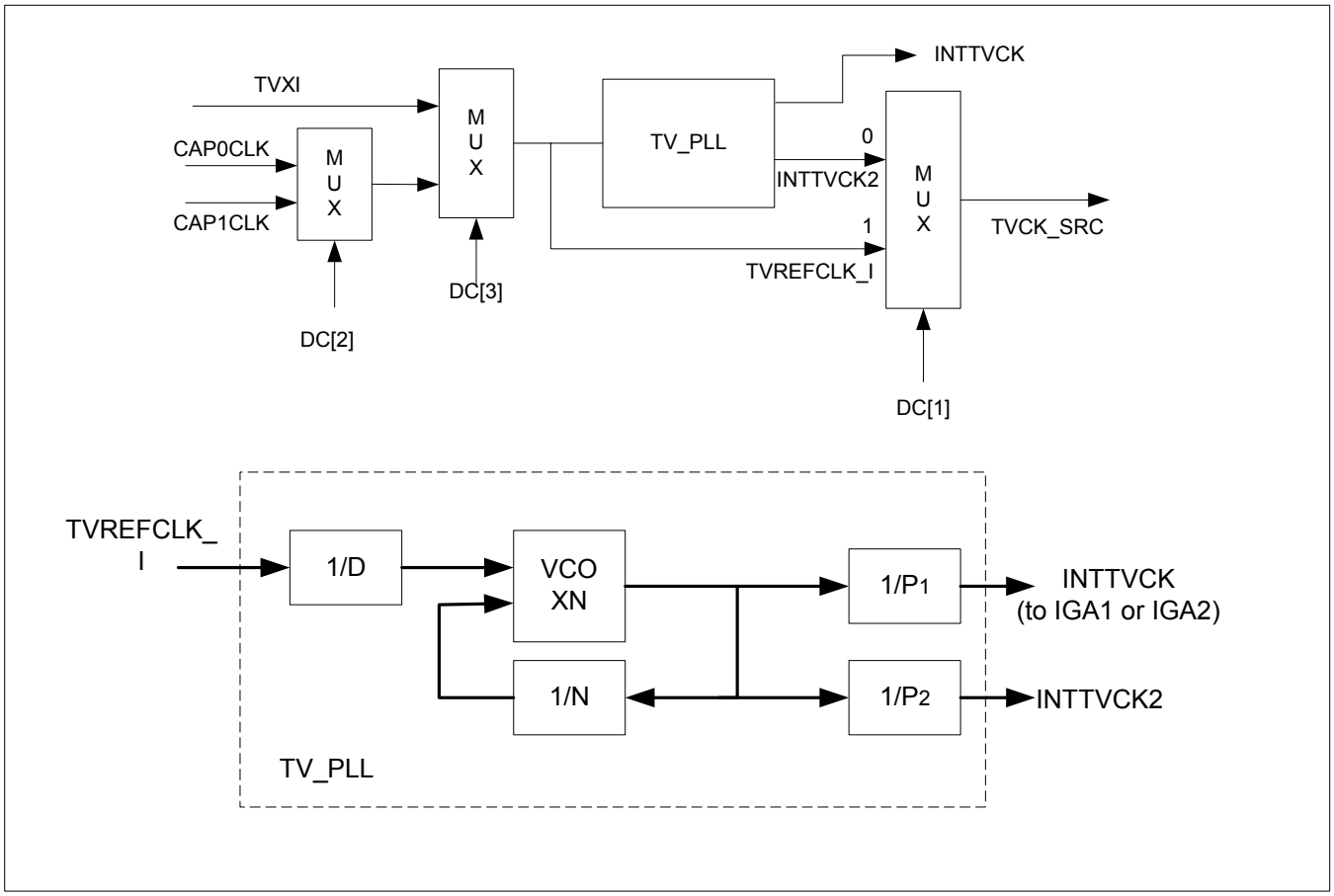


Figure 1. TV PLL Internal Clock Scheme

I/O Index: E4h

TV Status Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:3	RO	0	**Reserved**
2	RO	0	**TV Sense Status**
1	RO	0	**The Status of CCDR2 and CCDR3** 0: Cleared 1: Busy
0	RO	0	**The Status of CCDR0 and CCDR1** 0: Cleared 1: Busy

I/O Index: E8h

TV Blank Level and Sense Register **Default Value: 0000 0000h**

Cl3	Attribute	Default	Description
31	RO	0	**Reserved**
30	RW	0	**Sense R Status**
29	RW	0	**Sense G Status**
28	RW	0	**Sense B Status**
27:9	RO	0	**Reserved**
8:0	RW	0	**Blank Level for Pb and Pr**

LVDS / DVI REGISTERS

This chapter provides detailed LVDS and DVI register descriptions.

IO Port / Index: 3C5.13 [7:6]
Configuration Register 2 (3C5.5A[0]=1) **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Integrated LVDS / DVI Mode Select (DVP1D15/14)** 00: LVDS1 + LVDS2 01: DVI + LVDS2 10: One Dual LVDS Channel (High Resolution Pannel) 11: One DVI only (decrease the clock jitter)

IO Port / Index: 3C5.2B [7:4]
DVI and LVDS Interrupt Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DVI Sense Interrupt Enable** 0: Disable 1: Enable
6	RW1C	0	**DVI Sense Interrupt Status**
5	RW		**LVDS Sense Interrupt Enable** 0: Disable 1: Enable
4	RW1C	0	**LVDS Sense Interrupt Status**

IO Port / Index: 3C5.40 [3]
PLL Control **Default Value: 00h**

Bit	Attribute	Default	Description
3	RW	0	**LVDS and DVI Interrupt Method** 0: New method (bypass and low active) 1: Old method

IO Port / Index: 3C5.5B [3:0]
Device Used Status 0 **Default Value: 00h**

Bit	Attribute	Default	Description
3	RO	0	**LVDS0 Used IGA1 Source Flag** 0: No use 1: Use
2	RO	0	**LVDS0 Used IGA2 Source Flag** 0: No use 1: Use
1	RO	0	**LVDS1 Used IGA1 Source Flag** 0: No use 1: Use
0	RO	0	**LVDS1 Used IGA2 Source Flag** 0: No use 1: Use

IO Port / Index: 3X5.6A [3]

Second Display Channel and LCD Enable **Default Value: 00h**

Bit	Attribute	Default	Description
3	RW	0	**First Hardware Power Sequence Enable** 0: Off 1: On

IO Port / Index: 3X5.88

LCD Panel Type **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**LVDS First Channel1 Output Format** 0: Rotation 1: Sequential
5	RW	0	**Flip Strategy** 0: By Frame 1: By Line
4:1	RO	0	**Reserved**
0	RW	0	**LVDS Second Channel1 Output Bits** 0: 24 bits 1: 18 bits

IO Port / Index: 3X5.97

LVDS Channel 2 Function Select 0 / DVI Function Select **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RO	0	**DVI (TMDS) VSYNC Polarity** 0: Positive 1: Negetive
5	RO	0	**DVI (TMDS) HSYNC Polarity** 0: Positive 1: Negetive
4	RW	0	**LVDS Channel2 Data Source Selection** 0: Primary Display 1: Secondary Display
3:0	RO	0	**Reserved**

IO Port / Index: 3X5.98

LVDS Channel 2 Function Select 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**LVDS Channel 2 DE Mask to Zero Enable**
6:4	RW	0	**12-bit Output Format Rotation** 000:R G B 001:R B G 010:G R B 011:G B R 100:B R G 101:B G R Others: R G B
3:0	RO	0	**Reserved**

IO Port / Index: 3X5.99
LVDS Channel 1 Function Select 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**LVDS Channel 2 VSYNC Mask to Zero Enable**
6:5	RO	0	**Reserved**
4	RW	0	**LVDS Channel1 Data Source Selection** 0: Primary Display 1: Secondary Display
3:0	RO	0	**Reserved**

IO Port / Index: 3X5.9A
LVDS Channel 1 Function Select 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**LVDS Channel 1 DE Mask to Zero Enable**
6	RW	0	**LVDS Channel 1 VSYNC Mask to Zero Enable**
5	RW	0	**LVDS Channel 1 HSYNC Mask to Zero Enable**
4	RW	0	**LVDS Channel 2 HSYNC Mask to Zero Enable**
3:0	RO	0	**Reserved**

IO Port / Index: 3X5.D0
LVDS PLL Control Register **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**PLL1 Reference Clock Edge Select Bit** 0: PLLCK lock to rising edge of reference clock 1: PLLCK lock to falling edge of reference clock
6:5	RW	0	**PLL1 Charge Pump Current Set Bits** 00: ICH = 12.5 uA 01: ICH = 25.0 uA 10: ICH = 37.5 uA 11: ICH = 50.0 Ua
4:3	RO	0	**Reserved**
2:0	RW	0	**PLL1 Output Clock (PLLCK) Delay Select Bits** 000: T_{DLY} = 0.82 nS 001: T_{DLY} = 0.1T + 0.82 nS 010: T_{DLY} = 0.2T + 0.82 nS 011: T_{DLY} = 0.3T + 0.82 nS 100: T_{DLY} = 0.4T + 0.82 nS

IO Port / Index: 3X5.D1
DVI PLL Control Register **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**PLL2 Reference Clock Edge Select Bit** 0: PLLCK lock to rising edge of reference clock 1: PLLCK lock to falling edge of reference clock
6:5	RW	0	**PLL2 Charge Pump Current Set Bits** 00: ICH = 12.5 uA 01: ICH = 25.0 uA 10: ICH = 37.5 uA 11: ICH = 50.0 Ua
4:1	RO	0	**Reserved**
0	RW	0	**PLL2 Control Voltage Measurement Enable Bit**

IO Port / Index: 3X5.D2
LVDS / DVI Control Register **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Power Down (Active High) for Channel 1 LVDS**
6	RW	0	**Power Down (Active High) for Channel 2 LVDS**

5:4	RW	0	**Display Channel Select** **00: LVDS1 Channel + LVDS2 Channel** **01: Reserved** **10: One Dual LVDS Channel (High Resolution Pannel)** **11: Single Channel DVI**
3	RW	0	**Power Down (Active High) for DVI**
2	RO	0	**Reserved**
1	RW	0	**LVDS Channel 1 Format Selection** 0: SPWG Mode 1: OPENLDI Mode
0	RW	0	**LVDS Channel 2 Format Selection** 0: SPWG Mode 1: OPENLDI Mode

IO Port / Index: 3X5.D3

Second Power Sequence Control Register 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Software Direct On / Off Display Period in the Panel Path** 0: On 1: Off
6	RW	0	**Software On / Off Back Light Directly** 0: On 1: Off
5	RW	0	**Software Direct On / Of Display Period on DVP1 Port** 0: On 1: Off
4	RW	0	**Software VDD On**
3	RW	0	**Software Data On**
2	RW	0	**Software VEE On**
1	RW	0	**Software Back Light On**
0	RW	0	**Hardware or Software Control Power Sequence** 1: Software Control

IO Port / Index: 3X5.D4

Second Power Sequence Control Register 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**LVDS Second Channel2 Output Format** 0: Rotation 1: Sequential
6	RW	0	**LVDS Second Channel2 Output Bits** 0: 24 bits 1: 18 bits
5:2	RO	0	**Reserved**
1	RW	0	**Secondary Power Hardware Power Sequence Enable** 0: Off 1: On
0	RW	0	**Power Sequence Timer Selection** 0: First 1: Second

IO Port / Index: 3X5.D5

LVDS Setting Mode Control Register **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**PD1 Enable Selection** 1: Select by power flag
6	RW	0	**PD2 Enable Selection** 0: By register 1: Select by power flag
5	RW	0	**DVI Testing Mode Enable**
4	RW	0	**DVI Testing Format Selection** 0: Half cycle 1: LFSR mode
3	RO	0	**Reserved**
2	RW	0	**LVDS Testing Mode Enable**
1:0	RW	0	**LVDS Testing Format Selection** 00: Always 0 01: Always 1 1x: 0,1 toggle