Open Graphics Programming Manual

UniChrome Pro II Graphics Processor

CX700 / VX700 Series

Part II: 3D / Video

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REVISION HISTORY

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TABLE OF CONTENTS

LIST OF TABLES

INTRODUCTION

This document contains detailed graphics registers descriptions and other general information for the UniChrome Pro II graphic engine. The graphics registers for the UniChrome Pro II main features and its underlying subsystems are described explicitly in the following chapters.

About This Programming Guide

The programming manual is organized into 2 volumes (Part I & Part II). A brief description of each chapter is given below:

Part I:

Introduction.
An overview of the UniChrome Pro II design features is given in this chapter, along with block diagram and reference list.

Register Overview
Register specifications for register addressing and I/O space division are shown in this chapter.

PCI Interface Register Descriptions
PCI interface summary table is presented in this chapter.

VGA I/O Register Descriptions
This chapter provides detailed VGA-related register summary and descriptions. The various video modes support by the UniChrome Pro II controller are also included in the configuration section.

2D Engine Register Descriptions
In this chapter provides detailed 2D engine register summary and descriptions.

DMA Register Descriptions
In this chapter provides detailed DMA register summary and descriptions.

CBU Rotation Register Descriptions
In this chapter provides detailed CBU rotation register summary and descriptions.

Integrated TV Encoder Register Descriptions
In this chapter provides detailed Integrated TV Encoder register summary and descriptions.

Part II:

Video Register Descriptions
This chapter provides detailed video register summary and descriptions.

3D Engine Register Descriptions
In this chapter provides detailed 3D engine register summary and descriptions.

VIDEO REGISTERS

This chapter provides detailed video register summary table. Register descriptions on video play back, blending, engine capture and high quality video registers are provided in the sequent sections.

Video Registers

The UniChrome Pro II Graphic Engine has an integrated video playback and blending engine. The video playback engine can simultaneously support up to three live video windows, and each video window can be independently scaled. Two blending engines support the graphics-to-video blending, followed by video-to-video blending effect. The blending factor is from constant, alpha stream or is combined with graphics data. Table 1 summarizes the video playback and blending engine registers. Detail register description follows.

These video register tables document the I/O port, I/O index and attribute ("Attribute") for each register. Attribute definitions being used are RW (Read/Write), RO (Read/Only), and RWC (or just WC) (Read / Write 1's to Clear individual bits). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions for details). All offset and default values are shown in hexadecimal unless otherwise indicated.

Table 1. Video Display Engine Registers

Offset	Register Name	Attribute
200	Interrupt Flags & Masks Control	RW
204	Address Flip Status	RO
208	Alpha Window / HI (For Second Display) Horizontal and Vertical Start	RW
20C	Alpha Window Horizontal and Vertical End & HI (For Second Display) Center Offset	RW
210	Alpha Window Control	RW
214	CRT Starting Address	RW
218	The Second Display Starting Address	RW
21C	Alpha Stream Frame Buffer Stride	RW
220	Primary Display Color Key	RW
224	Alpha Window & HI (For Second Display) Frame Buffer Starting Address	RW
228	Chroma Key Lower Bound	RW
22C	Chroma Key Upper Bound	RW
230	Video Stream 1 Control	RW
234	Video Window 1 Fetch Count	RW
238	Video Window 1 Frame Buffer Y Starting Address 1	RW
23C	Video Window 1 Frame Buffer Stride	RW
240	Video Window 1 Horizontal and Vertical Start Location	RW
244	Video Window 1 Horizontal and Vertical Ending Location	RW
248	Video Window 1 Frame Buffer Y Starting Address 2	RW
24C	Video Window 1 Display Zoom Control	RW
250	Video Window 1 Minify and Interpolation Control	RW
254	Video Window 1 Frame Buffer Y Starting Address 0	RW
258	Video 1 FIFO Depth and Threshold Control	RW
25C	Video Window 1 Position Offset	RW
260	HI Control For Second Display	RW
264	The Second Display Color Key	RW
268	V3 and Alpha Window FIFO Pre-threshold Control	RW
26C	V1 Source Image Line Count	RW
270	HI Transparent Color For Second Display	RW

Offset	Register Name	Attribute
274	HI Inverse Color For Second Display	RW
278	V3 and Alpha Window FIFO Depth and Threshold Control	RW
27C	V3 Display Count On Screen Control	RW
280	Primary Display Second Color Key	RW
284	V1 Color Space Conversion & Enhancement Control (1)	RW
288	V1 Color Space Conversion & Enhancement Control (2)	RW
28C	P Signature Adder Result 1	RW
290	Alpha Window / HI (For Primary Display) Ending Position	RW
294	3D AGP Pause Address MMIO Port	WO
298	Compose Output Modes Select	RW
29C	V3 Frame Buffer Starting Address 2	RW
2A0	V3 Control	RW
2A4	V3 Frame Buffer Starting Address 0	RW
2A8	V3 Frame Buffer Starting Address 1	RW
2AC	V3 Frame Buffer Stride	RW
2B0	V3 Horizontal and Vertical Start	RW
2B4	V3 Horizontal and Vertical End	RW
2B8	V3 and Alpha Window Fetch Count	RW
2BC	V3 Display Zoom Control	RW
2C0	V3 Minify & Interpolation Control	RW
2C4	V3 Color Space Conversion & Enhancement Control (1)	RW
2C8	V3 Color Space Conversion & Enhancement Control (2)	RW
2CC	T Signature Adder Result 1.	RW
2D0	Graphics Hardware Cursor Mode Control	RW
2D4	Graphics Hardware Cursor Position	RW
2D8	Graphics Hardware Cursor Origin	RW
2DC	Graphics Hardware Cursor Background Color	RW
2E0	Graphics Hardware Cursor Foreground Color	RW
2E4	T Signature Data Result 1	RW
2E8	HI for Primary Display FIFO Control Signal	RW
2EC	HI for Primary Display Transparent color	RW
2F0	HI for Primary Display Control Signal	RW
2F4	HI for Primary Display Frame Buffer Starting Address	RW
2F8	HI for Primary Display Horizontal and Vertical Start	RW
2FC	HI for Primary Display Center Offset	RW
1200	Video 1Gamma R Correction Control	RW
1204	Video 1Gamma G Correction Control	RW
1208	Video 1Gamma B Correction Control	RW
120C	HI for Primary Display Inverse Color	RW
1220	Video 3Gamma R Correction Control	RW
1224	Video 3Gamma G Correction Control	RW
1228	Video 3Gamma B Correction Control	RW
122C	Video 3 Position OFFSET	RW
127C-1230	Reserved	RO
1280	Interrupt Flags and Masks Control	RW
1284	Logic Signature Setting	RW
1288	P Logic Signature Address Result0	RW
128C	T Logic Signature Address Result0	RW
1290	IGA1 Display Position Counter 0	RO
1294	IGA1 Display Position Counter 1	RO
1298	IGA1 Display Position Counter 2	RW

Offset	Register Name	Attribute
129C	T Logic Signature Data Result0	RW
12A0	IGA2 Display Position Counter 0	RO
12A4	IGA2 Display Position Counter 1	RO
12A8	IGA2 Display Position Counter 2	RW
12AC	IGA1 Translation	RW
12B0	Primary Display Data Color Space Conversion and Enhancement Control (1)	RW
12B4	Primary Display Data Color Space Conversion and Enhancement Control (2)	RW
12B8	Primary Display Data Color Space Conversion and Enhancement Control (3)	RW
12BC	Primary Display Data Color Space Conversion and Enhancement Control (4)	RW
12F0-12C0	Reserved	RO
3260	Video ID Control	RW
326C	Video Wait Control Register	RW

Note: 1) Port Address: MB1 + Offset Address

2) Group A includes PM800, PM880, PN800 and CN400 products
Group B includes K8M800 Version CD / CE and K8N800 Version CD / CE products

3) For Group A, there is additional register space to match the above register definition. When write a register to this space, it will be sent to “command regulator” first and then pass to video display engine. However, register read will be same as the original action.
The relationship between the additional register space and original register space is **(the additional register address) = (the original register address) + 16’h2000**.

Table 2. Video Capture Engine and High Quality Video Registers

Offset	Register Name	Attribute
First Capture Engine register		
300	Capture Interrupt Control and Flags	RW
304	Reserved	RO
308	Transport Stream Control	RW
30C	Reserved	RO
310	Capture Interface Control	RW
314	Active Video Horizontal Range (CCIR601 only)	RW
318	Active Video Vertical Range (CCIR601 only)	RW
31C	Active Video Scaling Control	RW
320	VBI Data Horizontal Range	RW
324	VBI Data Vertical Range	RW
328	First VBI Buffer Starting Address	RW
32C	VBI Buffer Stride	RW
330	Ancillary Data Count Setting	RW
334	Maximum Data Count of Active Video	RW
338	Maximum Data Count of VBI or ANC	RW
33C	Capture Data Count	RO
340	First Active Video Frame Buffer Starting Address	RW
344	Second Active Video Frame Buffer Starting Address	RW
348	Third Active Video Frame Buffer Starting Address	RW
34C	Second VBI Buffer Starting Address	RW
350	Stride of Active Video Buffer and Coring Function Control	RW
354	TS Buffer0 Error Packet Indicator	RO
358	TS Buffer1 Error Packet Indicator	RO
35C	TS Buffer2 Error Packet Indicator	RO
360-37C	Reserved	RO
First HQV Engine Registers		
380-3B8	Reserved	RO
3BC	De-blocking Factor	RW
3C0	Subpicture Frame Buffer Stride and Control	RW
3C4	Subpicture Frame Buffer Starting Address	RW
3C8	Subpicture 4 X 16 RAM Table Write Control	RW
3CC	HQV Source Data Offset Control	RW
3D0	HQV Stream Control and Status	RW
3D4	HQV SW Source Data –Luma or Packed Starting Address	RW
3D8	HQV SW Source Data – Chroma Starting Address	RW
3DC	HQV Linear / Tile address mode and Color Space Conversion First Control	RW
3E0	HQV Source Data Line Count and Fetch Count Per Line	RW
3E4	HQV Motion Adaptive De-interlace control & Threshold	RW
3E8	HQV Scale Control	RW
3EC	HQV Destination Data Starting Address 0	RW
3F0	HQV Destination Data Starting Address 1	RW
3F4	HQV Destination Frame Buffer Stride	RW
3F8	HQV Source Frame Buffer Stride	RW
3FC	HQV Destination Data Starting Address 2.	RW
Second Capture Engine register		
1300	Capture Interrupt Control and Flags	RW
1304	Reserved	RO

1308	Transport Stream Control	RW
130C	Reserved	RO
1310	Capture Interface Control	RW
1314	Active Video Horizontal Range (CCIR601 only)	RW
1318	Active Video Vertical Range (CCIR601 only)	RW
131C	Active Video Scaling Control	RW
1320	VBI Data Horizontal Range	RW
1324	VBI Data Vertical Range	RW
1328	First VBI Buffer Starting Address	RW
132C	VBI Buffer Stride	RW
1330	Ancillary Data Count Setting	RW
1334	Maximum Data Count of Active Video	RW
1338	Maximum Data Count of VBI or ANC	RW
133C	Capture Data Count	RO
1340	First Active Video Frame Buffer Starting Address	RW
1344	Second Active Video Frame Buffer Starting Address	RW
1348	Third Active Video Frame Buffer Starting Address	RW
134C	Second VBI Buffer Starting Address	RW
1350	Stride of Active Video Buffer and Coring Function Control	RW
1354	TS Buffer0 Error Packet Indicator	RO
1358	TS Buffer1 Error Packet Indicator	RO
135C	TS Buffer2 Error Packet Indicator	RO
1360-137C	Reserved	RO
Second HQV Engine register		
1380-13B8	Reserved	RO
13BC	De-blocking Factor	RW
13C0	Subpicture Frame Buffer Stride and Control	RW
13C4	Subpicture Frame Buffer Starting Address	RW
13C8	Subpicture 4 X 16 RAM Table Write Control	RW
13CC	HQV Source Data Offset Control	RW
13D0	HQV Stream Control and Status	RW
13D4	HQV SW Source Data –Luma or Packed Starting Address	RW
13D8	HQV SW Source Data – Chroma Starting Address	RW
13DC	HQV Linear / Tile Address Mode and Color Space Conversion First Control	RW
13E0	HQV Source Data Line Count and Fetch Count Per Line	RW
13E4	HQV Motion Adaptive De-interlace Control and Threshold	RW
13E8	HQV Scale Control	RW
13EC	HQV Destination Data Starting Address 0	RW
13F0	HQV Destination Data Starting Address 1	RW
13F4	HQV Destination Frame Buffer Stride	RW
13F8	HQV Source Frame Buffer Stride	RW
13FC	HQV Destination Data Starting Address 2.	RW

Note:1) Port Address: MB1 + Offset Address

2) There is additional register space to match the above register definition. When write a register to this space, it will be sent to “command regulator” first and then pass to video display engine. However, register read will be same as the original action. The relationship between the additional register space and original register space is

(The additional register address) = (The original register address) + 16’h2000

Video Display Engine Register Descriptions

Offset Address: 200h

Interrupt Flags and Masks Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Interrupt Enable** 0: Disable 1: Enable
30	RW	0	**LVDS Sense Interrupt Enable** 0: Disable 1: Enable
29	RW	0	**Capture0 VBI Capture End Interrupt Enable** 0: Disable 1: Enable
28	RW	0	**Capture0 Active Video Data Capture End Enable** 0: Disable 1: Enable
27	RW1C	0	**LVDS Sense Interrupt Status**
26	RW	0	**Capture1 VBI Capture End Interrupt Enable** 0: Disable 1: Enable
25	RW	0	**First HQV Engine Interrupt Enable** 0: Disable 1: Enable (Refer to 03D0h)
24	RW	0	**Capture1 Active Video Data Capture End Enable** 0: Disable 1: Enable
23	RW	0	**DMA1 Transfer Done Interrupt Enable** 0: Disable 1: Enable
22	RW	0	**DMA1 Descriptor Done Interrupt Enable** 0: Disable 1: Enable
21	RW	0	**DMA0 Transfer Done Interrupt Enable** 0: Disable 1: Enable
20	RW	0	**DMA0 Descriptor Done Interrupt Enable** 0: Disable 1: Enable
19	RW	0	**VGA VSYNC Interrupt Mask Enable** 0: Disable 1: Enable
18	RW	0	**MC Complete Frame Interrupt Mask Enable** 1: Enable
17	RW	0	**Secondary Display VSYNC Interrupt Enable** 0: Disable 1: Enable
16	RW	0	**DVI Sense Interrupt Enable** 0: Disable 1: Enable
15	RW1C	0	**Secondary Display VSYNC Interrupts Status**
14	RW1C	0	**Capture1 VBI Capture end Interrupt Status**
13	RW1C	0	**Capture0 VBI Capture end Interrupt Status**
12	RW1C	0	**Capture0 Active Video Data Capture End Interrupt Status**
11	RW	0	**Second HQV Engine Interrupt Enable** 0: Disable 1: Enable (Reference 13D0h)
10	RW	0	**Second HQV Engine Interrupt Status** (Refer to 13D0h)
9	RW1C	0	**First HQV Engine Interrupt Status** (Refer to 03D0h)
8	RW1C	0	**Capture1 Active Video Data Capture End Interrupt Status**
7	RW1C	0	**DMA1 Transfer Done Interrupt Status**
6	RW1C	0	**DMA1 Descriptor Done Interrupt Status**
5	RW1C	0	**DMA0 Transfer Done Interrupt Status**
4	RW1C	0	**DMA0 Descriptor Done Interrupt Status**
3	RW1C	0	**VGA VSYNC Interrupt Status**
2	RW1C	0	**MC Complete Frame Interrupt Status**
1	RO	0	**Vertical Blanking Status**
0	RW1C	0	**DVI Sense Interrupt Status**

Offset Address: 204h

Address Flip Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RO	0	**Reserved**
11	RO	0	**Video Window 1 SW flip status (R); write B0+254'h port to clear this bit.**
10	RO	0	**Video Window 3 SW flip status (R); write B0+2A4'h port to clear this bit.**
9:5	RO	0	**Reserved**
4	RO	0	**Alpha Window Starting Address Update Status** 0: Updated 1: Not yet updated It will be set as writes Rx224, and be clear as starting address is updated
3	RO	0	**Video Window 3 Starting Address Update Status** 0: Updated 1: Not yet updated It will be set as writes Rx2A4, and be clear as starting address is updated
2	RO	0	**Reserved**
1	RO	0	**Graphics Starting Address Update Status** 0: Updated 1: Not yet updated It will be set as writes Rx214, and be clear as starting address is updated
0	RO	0	**Video Window 1 Starting Address Update Status** 0: Updated 1: Not yet updated (It will be set as writes Rx254, and be clear as starting address is updated)

Offset Address: 208h

Alpha Window / Hardware Icon (HI) Horizontal and Vertical Location Start **Default Value: 0000 0000h**

Bit	Attribute	Default	Description	
31:27	RO	0	**Reserved**	
26:16	WO	0	**Depend on Hardware Icon Enable (Rx260[0])** 0: Alpha window horizontal (X) starting location 1: Hardware icon horizontal (X) starting location Unit: Pixel	
15:11	RO	0	**Reserved**	
10:0	WO	0	**Write** **Depend on Hardware Icon Enable (Rx260[0])** 0: Alpha window vertical (Y) starting location 1: Hardware icon vertical (Y) starting location Unit: Line	**Read** **Graphic Display Vertical Line Number** Unit: Line

Offset Address: 20Ch

Alpha Window Horizontal and Vertical Location End / Hardware Icon (HI) Center Offset **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RW	0	**Parameter Type Sub-code**
26:16	RW	0	**Depend on Hardware Icon Enable (Rx260[0])** 0: [26:16] Alpha window horizontal (X) ending location 1: [22:16] Hardware icon horizontal (X) center offset Unit: Pixel
15:11	RO	0	**Reserved**
10:0	RW	0	**Depend on Hardware Icon Enable (Rx260[0])** 0: [10:0] Alpha window vertical (Y) ending location 1: [6:0] Hardware icon vertical (Y) enter offset Unit: Line

Offset Address: 210h

Alpha Window Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:21	RO	0	**Reserved**
20:16	RW	0	**Alpha Stream Request Expire Number** Unit: 4 Requests
15:8	RW	0	**Constant Alpha Factor Setting For Graphics Blending** Default: 8'Hf
7:2	RO	0	**Reserved**
1:0	RW	0	**Graphics Blending Alpha Select (Alpha*VID+(1-Alpha)*GRA)** 00: Blending using constant alpha factor [15:8] 01: Alpha is from alpha stream 10: Alpha is from graphics stream 11: Reserved (Default: 2'b0)

Offset Address: 214h

CRT Starting Address Shadow **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:0	RW	0	**Primary Display Starting Address** Address equivalent to: 3X5.48 [4:0] 3X5.34 [7:0] 3X5.0C [7:0] 3X5.0D [7:0]

Note: In monochrome mode, the "X" in the above table stands for **"B".** In color mode, the "X" in the above table stands for **"D".**

Offset Address: 218h

The Second Display Starting Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:3	RW	0	**The Second Display Starting Address** Unit: 8 bytes
2:0	RO	0	**Reserved**

Note: This register should be the same with 3X5.5E, 5D and 5C registers.

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Offset Address: 21Ch

Alpha Stream Frame Buffer Stride **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:13	RO	0	**Reserved**
12:4	RW	0	**Alpha Stream Frame Buffer Stride** Unit: 16 bytes
3:0	RO	0	**Reserved**

Offset Address: 220h

Primary Display Color Key **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**CRT Color key : For RGB10 color mode [29].**
30	RW	0	**CRT Color Key Enable** 0: Disable 1: Enable
29	RW	0	**CRT Color Key Inverse Control** 0: Display video if color key match 1: Display video if not color key match
28:0	RW	0	**CRT Color Key** [28:0] For RGB10 color mode [28:0] [23:0] For 32-bit true color mode [15:0] For 565 Hi color mode [14:0] For 555 Hi color mode [7:0] For 256 color mode

Offset Address: 224h

Alpha Window / Hardware Icon Frame Buffer Starting Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RO	0	**Reserved**
25:4	RW	0	**Depend On Hardware Icon Enable (Rx260[0])** 0: Frame buffer starting address for alpha window 1: Frame buffer starting address for hardware icon Unit: 16 bytes
3:0	RO	0	**Reserved**

Offset Address: 228h

Chroma Key Lower Bound **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Chroma Key Lower for Y/G bit [1]**
30	RW	0	**Chroma Key Enable** 0: Disable 1: Enable
29	RW	0	**Chroma Key Inverse Control** 0: Display video if chroma key not match 1: Display video if chroma key match
28:0	RW	0	**Chroma Key Lower** {[23:16],[31],[28]}: Y/G {[15:8],[27:26]}: U/R {[7:0],[25:24]}: V/B

Offset Address: 22Ch

Chroma Key Upper Bound **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**Reserved**
30	RW	0	**Chroma Key Select** 1 : Select Video 3 0 : Select Video 1
29:0	RO	0	**Chroma Key Upper** {[23:16],[29:28]} Y/G {[15:8],[27:26]}: U/R {[7:0],[25:24]}: V/B

Offset Address: 230h

Video Stream 1 Control (Only For Group A) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**V1 Display to CRT or the Second Display** 0: CRT 1: Second Display
30	RW	0	**V1 Window Pre-fetch Enable**
29	RW	0	**V1 Window Gamma Function Enable**
28	RW	0	**V1 Window De-Gamma Function Enable**
27	RW	0	**V1 Window Adder Tile Mode Enable**
26:25	RW	0	**V1 Flip Control (default : 2'b0)** 00: SW Flip 01: HW Flip and triggle by the HQV engine 10: HW Flip and triggle by the Capture Port 0 11: HW Flip and triggle by the Capture Port 1.
24	RW	0	**V1 Frame to Field Enable** 0: Disable 1: Enable. If enabled, the stride will 2 times of original values. This bit is valid at Software flip. HQV flip. Capture frame mode flip. MC frame mode flip.
23	RW	0	**V1 Buffer in Field mode**
22	RW	0	**V1 De-interlace Mode** If enabled Hardware will add one line to the top of odd (bottom) field 0: Disable 1: Enable
21	RW	0	**V1 Line Flip Only in Non Video Active Period Enable** 0: Disable 1: Enable
20:16	RW	0	**V1 Request Expire Number (Unit: 4 requests)**
15:10	RO	0	**Reserved**
9	RW	0	**Divided V1 Flip for HQV Engine VSYNC Number to Half Enable** 0: Disable 1: Enable
8	RW	0	**V1 Color Space Conversion Disable** 0: Enable 1: Disable
7	RW	0	**V1 Color Space Conversion Chroma Sign Bits Conversion**
6:5	RO	0	**Reserved**
4:2	RW	000b	**V1 Stream Data Format** 000: YUV422; 001: RGB32; 010: RGB15; 011: RGB16; 100: YUV10; 101: RGB10; Other : reserved
1	RO	0	**Reserved**
0	RW	0	**V1 Enable** 0: Disable 1: Enable

Offset Address: 234h

Video Window 1 Fetch Count **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RO	0	**Reserved**
29:20	RW	0	**V1 Per Line Fetch Count** It is equal, no-sizing line fetch count / minify times (Unit : 16 bytes)
19:0	RO	0	**Reserved**

Offset Address: 238h

Video Window 1 Fetch Buffer Y Starting Address 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RO	0	**Reserved**
25:4	RW	0	**V1 Packed Mode** The second frame buffer starting address. (Unit : 16 bytes)
3:0	RO	0	**Reserved**

Offset Address: 23Ch

Video Window 1 Frame Buffer Stride **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RO	0	**Reserved**
25:4	RW	0	**V1 Packed Mode** Frame buffer stride (Unit : 16 bytes)
3:0	RO	0	**Reserved**

Offset Address: 240h

Video Window 1 Horizontal and Vertical Starting Location **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**Video Window 1 Horizontal (X) Starting Location (-1)**. (Unit: pixel)
15:11	RO	0	**Reserved**
10:0	RW	0	**Video Window 1 Vertical (Y) Starting Location (-1)**. (Unit: Line)

Offset Address: 244h

Video Window 1 Horizontal and Vertical Ending Location **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**Video Window 1 Horizontal (X) Ending Location (-1)**. (Unit: pixel)
15:11	RO	0	**Reserved**
10:0	RW	0	**Video Window 1 Vertical (Y) Ending Location (-1)**. (Unit: Line)

Offset Address: 248h

Video Window 1 Frame Buffer Y Starting Address 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RO	0	**Reserved**
25:4	RW	0	**V1 Packed Mode** The third frame buffer starting address (Unit : 16 bytes)
3:0	RO	0	**Reserved**

Offset Address: 24Ch

Video Window 1 Display Zoom Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RW	0	**Video Window 1 Horizontal (X) Zoom Enable** 0: Disable 1: Enable
30:27	RO	0	**Reserved**
26:16	RW	0	**Video window 1 Horizontal(X) Zoom Factor**
15	RW	0	**Video window 1 Vertical (Y) Zoom Enable** 0: Disable 1: Enable
14:10	RO	0	**Reserved**
9:0	RW	0	**Video Window 1 Vertical(Y) Zoom Factor**

Offset Address: 250h

Video Window 1 Minify & Interpolation Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:24	RW	0	**V1 Horizontal (X) Minify Control** 000: No minify; 001: Minify by a factor of 2 010: Reserved 011: Minify by a factor of 4 101: Minify by a factor of 8 111: Minify by a factor of 16 Other cases: reserved
23:19	RO	0	**Reserved**
19:16	RW		**V1 Vertical (Y) Minify Control** 000: No minify 001: Minify by a factor of 2 010: Reserved 011: Minify by a factor of 4 101: Minify by a factor of 8 111: Minify by a factor of 16 Other cases: reserved
15:3	RO	0	**Reserved**
2	RW		**V1 Luma-only Interpolation when the Vertical Interpolation is Enabled** 0: Only luma values interpolated. 1: All YUV/YcbCr values interpolated.
1	RW	0	**V1 Horizontal (X) Interpolation Mode Select** 0: Pixel is replicated 1: Enable interpolation
0	RW	0	**V1 Vertical (Y) Interpolation Mode Select** 0: Pixel is replicated 1: Enable interpolation

Offset Address: 254h

Video Window 1 Frame Buffer Y Starting Address 0 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**V1 play odd(1) / even(0) field when SW playback and field base picture are selected** 1: Odd field.
30:29	RO	0	**Reserved**
28:2	RO	0	**V1 Packed Mode** The first frame buffer starting address. (unit : 4 bytes)
1:0	RO	0	**Reserved**

Note: In packed mode, we could use Rx254[3:2] to get

1.No minify: 4 bytes alignment. a Rx254[3:2] are valid

2. (Minify == 2): 8 bytes alignment. a Rx254[3] is valid, and Rx254[2] is omitted.

3. (Minify > 2): 16 bytes alignment. a Rx254[3:2] are omitted.

Offset Address: 258h

Video 1 FIFO Depth and Threshold Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RW	0	**V1 FIFO Pre-threshold** Let V1 to issue request early. Normally, this value is more or equal than V1 FIFO threshold (Rx258[15:8]). (unit : level)
23:26	RO	0	**Reserved**
15:8	RW	0	**V1 FIFO Threshold** Let V1 request priority from low to high (Unit: level)
7:0	RW	0	**V1 FIFO Depth (- 1)** (Unit : level)

Note: One level is equal to 16 bytes.

Offset Address: 25Ch

Video Window 1 Horizontal and Vertical Starting Location Offset **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**Video Window 1 Horizontal(X) Starting Location Offset** (Unit : 16 bytes)
15:11	RO	0	**Reserved**
10:0	RW	0	**Video Window 1 Vertical(Y) Starting Location Offset** (Unit: Line)

Offset Address: 260h

Hardware Icon (HI) Control (Only for Second Display) **Default Value: 000F 00F0h**

Bit	Attribute	Default	Description
31	RW	0	**V4 Displays to CRT (0) or Secondary Display (1)** 0: CRT 1: Secondary Display
30	RW	0	**V4 Window Pre-fetch Enable** Default: 1'b0
29	RW	0	**HWI + (1-aplha)*Graphics Mode** 0 Disable 1 Enable
28	RW	0	**Alpha Value Come From Where** (Only for the true color Hardware icon) 0: From bit [23:16] 1: From the bit [31:24] of Hardware icon
27:26	RW	0	**HI Window Size** 00: 32x32 01: 64x64 1x: 128x128 Unit: Pixel X line
25:24	RW	0	**HI Data Stream Format** 00: RGB555 01: RGB565 10: RGB32 11: RGB10
23:20	RO	0	**Reserved**
19:16	RW	Fh	**HI Constant Alpha [3:0] (HIAPA)**
15:12	RW	0	**Alpha Changed Value (HICV)** per frame as HI fan in/out turn on Rx260[8]. ALPHAn[7:0] = ALPHAn-1[7:0] +/- HICV[3:0], where just ALPHAn[7:4] is valid alpha value and ALPHA0 = {HIAPA}.
11:10	RW	0	**DMA1 Descriptor Done Interrupt Enable** 0: Disable 1: Enable
9	RW	0	**HI Fan In / Out Selector** 0: Default 1: Fan in (+)
8	RW	0	**HI Fan In / Out Enable** 0: Disable 1: Enable
7:4	RW	Fh	**HI Constant Alpha[7:4] (HIAPA)** The Rest Bits are put on [19:16]
3	RO	0	**Reserved**
2	RW	0	**HI Blending Enable** 0: Default 1: Enable
1	RO	0	**Reserved**
0	RW	0	**HI Enable** 0: Default 1: Enable

Offset Address: 264h

The Second Display Color Key **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**The Second Display Color Key Bit [29] For RGB10 True Color Mode**
30	RW	0	**Second Display Color Key Enable** 0: Disable 1:Enable
29	RW	0	**Second Display Color Key Inverse Control** 0: Display video if color key match 1: Display video if not color key match
28:0	RW	0	**The Second Display Color Key** [31],[28:0]: For RGB10 true color mode [23:0]: For 32-bit true color mode [15:0]: For 565 Hi color mode [14:0]: For 555 Hi color mode [7:0]: For 256 color mode

Offset Address: 268h

Alpha Window FIFO Pre-Threshold Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:23	RO	0	**Reserved**
22:16	RW	0	**Alpha Window FIFO Pre-threshold** Let alpha engine issues request early. This value is normally more or equal than the alpha engine FIFO threshold(Rx278[30:24]). Unit : Level
15:7	RO	0	**Reserved**
7:0	RW	0	**V3 FIFO Pre-threshold** Let V3 issues request early. This value is normally more or equal than V3 FIFO threshold (Rx278[15:8]). Unit: Level

Offset Address: 26Ch

Video Window 1 Display Count On Screen Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:26	RW	0	**V1 Vertical Line Count That Shows On Screen** (Unit: Line)
15:12	RO	0	**Reserved**
11:0	RW	0	**V1 Horizontal Pixel Count That Shows On Screen(-1)** (Unit: pixel)

Offset Address: 270h

Hardware Icon (HI) Transparent Color (Only For Second Display) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RO	0	**Reserved**
29:0	RW	0	**HI Transparent Color** [29:0]: For RGB10 [23:0]: For RGB32 [15:0]: For RGB565 [14:0]: For RGB555

Offset Address: 274h

Hardware Icon (HI) Inverse Color (Only For Second Display) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RO	0	**Reserved**
29:0	RW	0	**HI Inverse Color** [29:0]: For RGB10 [23:0]: For RGB32 [15:0]: For RGB565 [14:0]: For RGB555

Offset Address: 278h

V3 and Alpha Window FIFO Depth and Threshold Contorl **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**Reserved**
30:24	RW	0	**Alpha Window FIFO Threshold** Unit: Level
23	RO	0	**Reserved**
22:16	RW	0	**Alpha Window FIFO Depth (-1)** Unit: Level
15:8	RW	0	**Video Window 3 FIFO Threshold** Unit: Level
7:0	RW	0	**Video Window 3 FIFO Depth (-1)** Unit: Level

Note: (1) One level is equal to 16 bytes.

Offset Address: 27Ch

Video Window 3 Display Count On Screen Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:26	RW	0	**V3 Vertical Line Count That Shows On Screen** (Unit: Line)
15:12	RO	0	**Reserved**
11:0	RW	0	**V1 Horizontal Pixel Count That Shows On Screen(-1)** (unit: pixel)

Offset Address: 280h

Primary Display Second Color Key **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**Reserved**
30	RW	0	**CRT Color Key Enable** 0: Disable 1: Enable
29	RW	0	**CRT Color Key Inverse Control** 0: Display video if color key match 1: Display video if not color key match
28:24	RO	0	**Reserved**
23:0	RW	0	**Primary Display Color Key** [23:0] For 32-bit true color mode [15:0] For 565 Hi color mode [14:0] For 555 Hi color mode [7:0] For 256 color mode

Offset Address: 284h

Video Window 1 Color Space Conversion and Enhancement Control (1) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**SDTV(BT601) Coefficient Enable** 0: Disable 1: Enable
30	RW	0	**HDTV(BT709) Coefficient Enable** 0: Disable 1: Enable
29	RO	0	**Reserved**
28:24	RW	0	**Coefficient A:** **X.XXXX** From 0 to 1.9375
23:22	RO	0	**Reserved**
21:16	RW	0	**Coefficient B1:** **SXX.XXX** S=1 negative S=0 positive, from –2.125 to 2.125
15:14	RO	0	**Reserved**
13:8	RW	0	**Coefficient C1:** **SXX.XXX** S=1 negative S=0 positive, from –2.125 to 2.125
7:0	RW	0	**Coefficient D:** 2's complement integer from -128 to 127

Note: $R = AY+B_1Cb+C_1C_r+D$

Offset Address: 288h

Video Window 1 Color Space Conversion and Enhancement Control (2) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:24	RW	0	**Coefficient B2:** SX.XXX S=1 negative S=0 positive, from –1.875 to 1.875
23:21	RO	0	**Reserved**
20:16	RW	0	**Coefficient C2:** SX.XXX S=1 negative S=0 positive, from –1.875 to 1.875
15:14	RO	0	**Reserved**
13:8	RW	0	**Coefficient B3:** SXX.XXX S=1 negative S=0 positive, from –3.875 to 3.875
7:6	RO	0	**Reserved**
5:0	RW	0	**Coefficient C3:** SXX.XXX S=1 negative S=0 positive, from –3.875 to 3.875

Note: $G = AY+B_2Cb+C_2C_r+D$
$B = AY+B_3Cb+C_3C_r+D$

Offset Address: 28Ch

P Logic Adder Result 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**P Logic Adder Result 1**

Offset Address: 290h

Alpha Window / Color Cursor Ending (Only For Primary Display) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:16	RW	0	**Hardware Icon Horizontal (X) Ending Position**
15:11	RO	0	**Reserved**
10:0	RW	0	**Hardware Icon Vertical (Y) Ending Position** Unit: Line

Offset Address: 294h

3D AGP Pause Address MMIO Port **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**3D AGP Address MMIO Port**

Offset Address: 298h

Compose Output Mode Select **Default Value: 0300 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Video 1 Command End, V1 Load New Register Setting** 1: Fire. If registers are updated to engine, this bit will be cleared to 0 and the deafault is set at 0.
30	RW	0	**Video 3 Command End, V3 Load New Register Setting** 1: Fire. If registers are updated to engine, this bit will be cleared to 0 and the deafault is set at 0.
29	RW	0	**Video Register Always Loaded** For hardware simulation and the default is set at 0.
28	RW	0	**Video Register Loaded at Vertical Blanking Without Waiting Source Flip** Need to write [31] or [30] and default is set at 0.
27	RW	0	**Video 3 Register Always Loaded** For hardware simulation and the default is set at 0.
26	RW	0	**Video 3 Register Loaded at Vertical Blanking Without Waiting Source Flip** Need to write [31] or [30] and default is set at 0.
25:24	RW	11b	**Interpolation FIFO Clock Select** 00 : Not in use 01 : V1 HDTV 10 : V3 HDTV 11 : V1 SDTV and V3 SDTV
23:21	RO	0	**Reserved**
20	RW	0	**Video Output Overlap Control** 0: V1 is on top 1: V3 is on top
19:8	RO	0	**Reserved**
7	RW	0	**MCK Bypass Enable** 0: Disable 1: Enable
6	RO	0	**Reserved**
5	RW	0	**Bypass LCD Horizontal Magnify Function**
4	RW	0	**Bypass LCD Vertical Magnify Function**
3	RO	0	**Video 3 Line Flip Enable** 0: Disable 1: Enable
2	RW	0	**Video 1 Line Flip Enable** 0: Disable 1: Enable
1	RO	0	**Reserved**
0	RW	0	**Video 1 Round Control Enable** 0: Disable 1: Enable

Offset Address: 29Ch

Video Window 3 Frame Buffer Starting Address 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:4	RW	0	**The Third Frame Buffer Starting Address of V3** Unit : 16 bytes
3:0	RO	0	**Reserved**

Offset Address: 2A0h

Video Stream 3 Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**Reserved**
30	RW	0	**V3 Window Pre-fetch Enable** 0: Disable 1: Enable
29	RW	0	**V3 Window Gamma Function Enable** 0: Disable 1: Enable
28:27	RO	0	**Reserved**
26:25	RW	0	**V3 Flip Control** 00: SW Flip 01: HW Flip and triggle by the HQV engine 10: Reserved (For Group B) 10: HW Flip and triggle by the Capture Port 0 (For Group A) 11: Reserved (For Group B) 11: HW Flip and triggle by the Capture Port 1. (For Group A)
24	RW	0	**V3 Frame to Field Enable** 0: Disable 1: Enable If enabled, the stride will be 2 times of original values. This bit is valid at: Software flip, HQV flip.
23	RO	0	**Reserved**
22	RW	0	**V3 De-interlace Mode** 0: Disable 1: Enable If enabled, hardware will add one line to the top of odd (bottom) field
21	RW	0	**V3 Line Flip Only in Non Video Active Period Enable** 0: Disable 1: Enable
20:16	RW	0	**V3 Request Expire Number** Unit: 4 requests
15:10	RO	0	**Reserved**
9	RW	0	**Divided V3 Flip for HQV Engine VSYNC Number to Half Enable** 0: Disable 1: Enable
8	RW	0	**V3 Color Space Conversion Disable** 0: Enable 1: Disable
7	RW	0	**V3 Color Space Conversion Chroma Sign Bits Conversion** 1: Inverse
6:5	RO	0	**Reserved**
4:2	RW	0	**V3 Stream Data Format** X00: YUV422 001: RGB32 X10: RGB15 011: RGB16
1	RO	0	**Reserved**
0	RW	0	**V3 Enable** 0: Disable 1: Enable

Offset Address: 2A4h

Video Window 3 Frame Buffer Starting Address 0 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Play odd(1)/even(0) field when SW playback and field base picture are selected**
30:29	RO	0	**Reserved**
28:2	RW	0	**The First Frame Buffer Starting Address of V3** Unit: 4 bytes
1:0	RO	0	**Reserved**

Offset Address: 2A8h

Video Window 3 Frame Buffer Starting Address 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:4	RW	0	**The Second Frame Buffer Starting Address of V3** Unit: 16 bytes
3:0	RO	0	**Reserved**

Offset Address: 2ACh

Video Window 3 Frame Buffer Stride **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:14	RO	0	**Reserved**
13:4	RW	0	**V3 Frame Buffer Stride** Unit: 16 bytes
3:0	RO	0	**Reserved**

Offset Address: 2B0h

Video Window 3 Horizontal and Vertical Start **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**Reserved**
30:29	RW	0	**V3 Horizontal (X) Starting Location** Unit: Pixel
28:2	RO	0	**Reserved**
1:0	RW	0	**V3 Vertical (Y) Starting Location** Unit: Line

Offset Address: 2B4h

Video Window 3 Horizontal and Vertical End **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**V3 Horizontal (X) Ending Location** Unit: Pixel
15:11	RO	0	**Reserved**
10:0	RW	0	**V3 Vertical (Y) Ending Location** Unit: Line

Offset Address: 2B8h

Video Window 3 and Alpha Window Fetch Count **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RO	0	**Reserved**
29:20	RW	0	**V3 Per Line Fetch Count** Unit: Pixel
19:10	RO	0	**Reserved**
9:0	RW	0	**Alpha Window Per Line Fetch Count** Unit: Line

Offset Address: 2BCh

Video Window 3 Display Zoom Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**V3 Horizontal (X) Zoom Enable** 0: Disable 1: Enable
20:27	RO	0	**Reserved**
26:16	RW	0	**V3 Horizontal (X) Zoom Factor**
15	RO	0	**V3 Vertical (Y) Zoom Enable** 0: Disable 1: Enable
14:10	RO	0	**Reserved**
9:0	RW	0	**V3 Vertical (Y) Zoom Factor**

Offset Address: 2C0h

Video Window 3 Minify and Interpolation Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RW	0	**Reserved**
26:24	RW	0	**V3 Horizontal (X) Minify Control** 000: No minify 001: Minify by a factor of 2 010: Reserved 011: Minify by a factor of 4 101: Minify by a factor of 8 111: Minify by a factor of 16 Other cases are reserved.
23:19	RO	0	**Reserved**
18:16	RW	0	**V3 Vertical (Y) Minify Control** 000: No minify 001: Minify by a factor of 2 010: Reserved 011: Minify by a factor of 4 101: Minify by a factor of 8 111: Minify by a factor of 16 Other cases are reserved.
15:3	RO	0	**Reserved**
2	RW	0	**V3 luma-only interpolation when the vertical interpolation is enabled** 0: Only luma values interpolated 1: All YUV/YcbCr values interpolated
1	RW	0	**V3 Horizontal (X) Interpolation Mode Select** 0: Pixel is replicated 1: Enable interpolation
0	RW	0	**V3 Vertical(Y) Interpolation Mode Select** 0 Pixel is replicated 1 Enable interpolation Note: V1 and V3 can support interpolation simultaneously when both video source resolutions are lower than 800x600. If anyone exceeds the 800x600 resolution, only one of them can support interpolation. The control bit is defined at 0x298[25:24].

Offset Address: 2C4h

Video Window 3 Color Space Conversion and Enhancement Control 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**Reserved**
30	RW	0	**SDTV(BT601) Coefficient Enable** 0: Disable 1: Enable
29	RW	0	**HDTV (BT709) Coefficient Enable** 0: Disable 1: Enable
28:24	RO	0	**Reserved**
23:22	RW	0	**Coefficient A:** X.XXXX from 0 to 1.9375
21:16	RO	0	**Reserved**
15:14	RW	0	**Coefficient B1:** SXX.XXX S=1 negative S=0 positive From – 2.125 to 2.125
13:8	RO	0	**Reserved**
0	RW	0	**Coefficient C1:** SXX.XXX S=1 negative S=0 positive From – 2.125 to 2.125

Note: R=AY+B1Cb+C1Cr+D

Offset Address: 2C8h

Video Window 3 Color Space Conversion and Enhancement Control 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Coefficient D[2:0]:** 2's complement integer from -128 to 127
28:24	RW	0	**Coefficient B2:** SX.XXX S=1 negative S=0 positive, from –1.875 to 1.875
23:21	RO	0	**Reserved**
20:16	RW	0	**Coefficient C2:** SX.XXX S=1 negative S=0 positive, from –1.875 to 1.875
15:14	RO	0	**Reserved**
13:8	RW	0	**Coefficient B3:** SXX.XX S=1 negative S=0 positive, from 0 to 3.75
7:6	RO	0	**Reserved**
5:0	RW	0	**Coefficient C3:** SX.XX S=1 negative S=0 positive, from –3.875 to 3.875

Note: G=AY+B2Cb+C2Cr+D, B=AY+B3Cb+C3Cr+D

Offset Address: 2CCh

T Logic Adder Result1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**T Logic Adder Result1**

Offset Address: 2D0h

Graphic Hardware Cursor Mode Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Show mono cursor on which display path** 0: Primary 1: Secondary
30:26	RO	0	**Reserved**
25:8	RW	0	**Hardware Cursor Base Address** Up to 64M bytes For 32x32x2 pattern: [25:8] define the base address For 64x64x2 pattern: [25:10] define the base address
7:2	RO	0	**Reserved**
1	RW	0	**Hardware Cursor Size** 0: 64x64x2 1: 32x32x2
0	RW	0	**Hardware Cursor Enable** 0: Disable 1: Enable

Offset Address: 2D4h

Graphic Hardware Cursor Position **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**Hardware Cursor Position in the X-coordinate**
15:11	RO	0	**Reserved**
10:0	RW	0	**Hardware Cursor Position in the Y-coordinate**

Offset Address: 2D8h

Graphic Hardware Cursor Origin **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**Hardware Cursor Origin in the X-coordinate**
15:11	RO	0	**Reserved**
10:0	RW	0	**Hardware Cursor Origin in the Y-coordinate**

Offset Address: 2DCh

Graphic Hardware Cursor Background **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Reserved**
23:0	RW	0	For 256 color mode, bits [7:0] specify hardware cursor background color For 555 Hi color mode, bits [14:0] specify hardware cursor background color For 565 Hi color mode, bits [15:0] specify hardware cursor background color For 32-bit True color mode, bits [23:0] specify hardware cursor background color

Offset Address: 2DCh

Graphic Hardware Cursor Background **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Reserved**
23:0	RW	0	**For 256 Color Mode:** Bits [7:0] specify hardware cursor foreground color **For 555 Hi Color Mode:** Bits [14:0] specify hardware cursor foreground color **For 565 Hi Color Mode:** Bits [15:0] specify hardware cursor foreground color **For 32-bit True Color Mode** Bits [23:0] specify hardware cursor foreground color

Table 3 below shows the hardware color cursor operation. Please be noted this table is only applicable to the graphics modes. For the text modes, the VGA registers control the hardware color cursor.

Table 3. Graphics Hardware Color Cursor Operation

Pixel Operation	AND Plane	XOR Plane
Choose graphics hardware color cursor background color	0	0
Choose graphics hardware color cursor foreground color	0	1
Transparent	1	0
VGA data is inverted	1	1

Offset Address: 2E4h

T Logic Data Result1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**T Logic Data Result1**

Offset Address: 2E8h

HI FIFO Depth and Threshold Control (Only For Primary Display) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RW	0	**HI FIFO Pre-threshold** Let HI to issue request early. Normally, this value is more or equal than HI FIFO threshold (Rx2E8[14:8]). (unit : level)
23:16	RO	0	**Reserved**
15:8	RW	0	**HI FIFO Threshold** Let HI request priority from low to high (unit: level)
7:0	RO	0	**HI FIFO Depth (- 1) (unit : level)**

Offset Address: 2ECh

Hardware Icon (HI) Transparent Color (Only For Primary Display) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RO	0	**Reserved**
29:0	RW	0	**HI Transparent Color** [29:0]: For RGB10 [23:0]: For RGB32 [15:0]: For RGB565 [14:0]: For RGB555

Offset Address: 2F0h

Hardware Icon (HI) Control (Only for Primary Display) **Default Value: 000F 00F0h**

Bit	Attribute	Default	Description
31	RO	0	**Reserved**
30	RW	0	**HI Window Pre-fetch Enable**
29	RW	0	**HWI + (1-aplha)*Graphics Mode** 0 Disable 1 Enable
28	RW	0	**Alpha Value Come From Where** Only for the true color Hardware icon 0: From bit [23:16] 1: From the bit [31:24] of Hardware icon
27:26	RW	0	**HI Window Size** 00: 32x32 01: 64x64 1x: 128x128 Unit: Pixel X line
25:24	RW	0	**HI Data Stream Format** 00: RGB555 01: RGB565 10: RGB32 11: RGB10
23:20	RO	0	**Reserved**
19:16	RW	Fh	**HI Constant Alpha [3:0] (HIAPA)**
15:12	RW	0	**Alpha Changed Value** (HICV) per frame as HI fan in/out turn on Rx260[8]. ALPHAn[7:0] = ALPHAn-1[7:0] +/- HICV[3:0], where just ALPHAn[7:4] is valid alpha value and ALPHA0 = {HIAPA}.
11:10	RO	0	**Reserved**
9	RW	0	**HI Fan In / Out Selector** 0: Default 1: Fan in (+)
8	RW	0	**HI Fan In / Out Enable** 0: Disable 1: Enable
7:4	RW	Fh	**HI Constant Alpha[7:4] (HIAPA)** The Rest Bits are put on [19:16]
3	RO	0	**Reserved**
2	RW	0	**HI Blending Enable** 0: Default 1: Enable
1	RO	0	**Reserved**
0	RW	0	**HI Enable** 0: Default 1: Enable

Offset Address: 2F4h

Hardware Icon Frame Buffer Starting Address (Only For Primary Display) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RO	0	**Reserved**
25:4	RW	0	Frame buffer starting address for hardware icon Unit: 16 bytes
3:0	RO	0	**Reserved**

Offset Address: 2F8h

Hardware Icon (HI) Horizontal and Vertical Location Start (Only For Primary Display) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**Hardware Icon Horizontal (X) Starting Location** Unit: Pixel
15:11	RO	0	**Reserved**
10:0	RW	0	**Hardware Icon Vertical (Y) Starting Location** Unit: Line

Offset Address: 2FCh

Hardware Icon (HI) Center Offset (Only For Primary Display) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:23	RO	0	**Reserved**
22:16	RW	0	**Hardware Icon Horizontal (X) Center Offset** Unit: Pixel
15:7	RO	0	**Reserved**
6:0	RW	0	**Hardware Icon Horizontal (Y) Center Offset** Unit: Line

Offset Address: 1200h

Video Gamma Color R Register for Video 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RO	0	**Reserved**
25:16	RW	0	**Color Value After Gamma Function**
15:5	RO	0	**Reserved**
4:0	RW	0	**Color Index Number for Gamma Function Division**

Offset Address: 1204h

Video Gamma Color G Register for Video 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RO	0	**Reserved**
25:16	RW	0	**Color Value After Gamma Function**
15:5	RO	0	**Reserved**
4:0	RW	0	**Color Index Number for Gamma Function Division**

Offset Address: 1208h

Video Gamma Color B Register for Video 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RO	0	**Reserved**
25:16	RW	0	**Color Value After Gamma Function**
15:5	RO	0	**Reserved**
4:0	RW	0	**Color Index Number for Gamma Function Division**

Offset Address: 120Ch

Hardware Icon (HI) Inverse Color (Only For Primary Display) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RO	0	**Reserved**
29:0	RW	0	**HI Inverse Color** [29:0]: For RGB10 [23:0]: For RGB32 [15:0]: For RGB565 [14:0]: For RGB555

Offset Address: 1220h

Video Gamma Color R Register for Video 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RO	0	**Reserved**
25:16	RW	0	**Color Value After Gamma Function**
15:5	RO	0	**Reserved**
4:0	RW	0	**Color Index Number for Gamma Function Division**

Offset Address: 1224h

Video Gamma Color G Register for Video 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RO	0	**Reserved**
25:16	RW	0	**Color Value After Gamma Function**
15:5	RO	0	**Reserved**
4:0	RW	0	**Color Index Number for Gamma Function Division**

Offset Address: 1228h

Video Gamma Color B Register for Video 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RO	0	**Reserved**
25:16	RW	0	**Color Value After Gamma Function**
15:5	RO	0	**Reserved**
4:0	RW	0	**Color Index Number for Gamma Function Division**

Offset Address: 122Ch

Video Window 3 Horizontal and Vertical Starting Location Offset **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**Video Window 3 Horizontal (X) Starting Location Offset** (unit : 16 bytes)
15:11	RO	0	**Reserved**
10:0	RW	0	**Video Window 3 Vertical (Y) Starting Location Offset** (Unit: Line)

Offset Address: 1280h

Interrupt Flags and Masks Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW1C	0	**MSI Pending Interrupt Re-trigger Bit** When SW wants to exit interrupt service, please clear the bit. HW may send out interrupt again if pending interrupt exists. The function is enable when MSI Enable = 1'b1.
30:23	RO	0	**Reserved**
22	RW	0	**Secondary CRT Sense Interrupt Enable** 0: Disable 1: Enable
21	RW	0	**I2C Interrupt Enable** 0: Disable 1: Enable
20	RW	0	**CRT Sense Interrupt Enable** 0: Disable 1: Enable
19	RW	0	**DMA3 Transfer Done Interrupt Enable** 0: Disable 1: Enable
18	RW	0	**DMA3 Descriptor Done Interrupt Enable** 0: Disable 1: Enable
17	RW	0	**DMA2 Transfer Done Interrupt Enable** 0: Disable 1: Enable
16	RW	0	**DMA2 Descriptor Done Interrupt Enable** 0: Disable 1: Enable
15:9	RO	0	**Reserved**
8	RO	0	**Secondary CRT Sense Interrupt Status**
7	RO	0	**I2C Data Transferred Status**
6	RO	0	**I2C Transaction Done Status**
5	RO	0	**I2C Abnormal Status**
4	RO	0	**CRT Sense Interrupt Status**
3	RO	0	**DMA3 Transfer Done Interrupt Status**
2	RO	0	**DMA3 Descriptor Done Interrupt Status**
1	RO	0	**DMA2 Transfer Done Interrupt Status**
0	RO	0	**DMA2 Descriptor Done Interrupt Status**

Note: Write 1 to bit [8:0] to clear bits

Offset Address: 1284h

Logic Signature Setting **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RO	0	**Reserved**
7	RW	0	**T Signature RD Disable 1e**
6	RW	0	**P & T Select Signal1 :**
5	RW	0	**T Signature Enable1**
4	RW	0	**P Signature Enbale1**
3	RW	0	**T Signature RD Disable 0**
2	RW	0	**P & T Select Signal0**
1	RW	0	**T Signature Enable0**
0	RW	0	**P Signature Enbale0**

Offset Address: 1288h
P Logic Adder Result0 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**P Logic Adder Result0**

Offset Address: 128Ch
T Logic Adder Result0 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**T Logic Adder Result0**

Offset Address: 1290h
IGA1 Display Position Counter 0 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RO	0	**IGA1 Display Line Counter**
15:0	RO	0	**IGA1 Display Frame Counter**

Offset Address: 1294h
IGA1 Display Position Counter 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:0	RO	0	**IGA1 Display Frame Counter**

Offset Address: 1298h
IGA1 Display Position Counter 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:0	RO	0	**IGA1 Display Frame Counter Enable** 0: Disable 1: Enable When this bit is disabled, Frame Counter always get 16'h0.

Offset Address: 129Ch
T Logic Data Result0 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**T Logic Data Result0**

Offset Address: 12A0h
IGA2 Display Position Counter 0 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RO	0	**IGA2 Display Line Counter**
15:0	RO	0	**IGA2 Display Frame Counter**

Offset Address: 12A4h
IGA2 Display Position Counter 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:0	RO	0	**IGA2 Display Frame Counter**

Offset Address: 12A8h

IGA2 Display Position Counter 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:0	RW	0	**IGA2 Display Frame Counter Enable** 0: Disable 1: Enable When this bit is disabled, Frame Counter always get 16'h0.

Offset Address: 12B0h

Primary Display Data Color Space Conversion and Enhancement Control 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RO	0	**Reserved**
29:20	RW	0	**A1 <= XXXXXXXXXX**
19:10	RW	0	**B1 <= XXXXXXXXXX**
9:0	RW	0	**C1 <= XXXXXXXXXX**

Note: Y = A1R+B1G+C1B+D

Coefficient A1, B1, C1: 10 bits, 0.XXXXXXXX from 0 to 0.99903 Coefficient D: 8 bit positive integer from 16 to 255

Offset Address: 12B4h

Primary Display Data Color Space Conversion and Enhancement Control 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RO	0	**Reserved**
29:20	RW	0	**A2[9:0] <= XXXXXXXXXX**
19:10	RW	0	**B2[9:0] <= XXXXXXXXXX**
9:0	RW	0	**C2[9:0] <= XXXXXXXXXX**

Note: Cr= A2R+B2G+C2B +128

Coefficient A2, B2, C2: 11 bits S.XXXXXXXX 2's complement from -0.99903 to 0.99903

Offset Address: 12B8h

Primary Display Data Color Space Conversion and Enhancement Control 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RO	0	**Reserved**
29:20	RW	0	**A3[9:0] <= XXXXXXXXXX**
19:10	RW	0	**B3[9:0] <= XXXXXXXXXX**
9:0	RW	0	**C3[9:0] <= XXXXXXXXXX**

Note: Cr= A3R+B3G+C3B +128

Coefficient A3, B3, C3: 11 bits. S.XXXXXXXX 2's complement from -0.99903 to 0.99903,

Offset Address: 12BCh

Primary Display Data Color Space Conversion and Enhancement Control 4 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:14	RO	0	**Reserved**
13	RW	0	**A2[10] <= S**
12	RW	0	**B2[10] <= S**
11	RW	0	**C2[10] <= S**
10	RW	0	**A3[10] <= S**
9	RW	0	**B3[10] <= S**
8	RW	0	**C3[10] <= S**
7:0	RW	0	**D**

Offset Address: 3260h

Video ID Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**Reserved**
30	WO	0	**Video Command Force Start (SW must fill zero)**
29:28	WO	0	**Video Command Status** **00: Video command start** **01: Video command end** **10: Video command end and wait VIDEO idle** **11: Video command end and wait HQV idle**
27	WO	0	**Video Command Stream Kinds**
26:24	WO	0	**Video Working Buffer Number**
23:16	WO	0	**Reserved (HW Use)**
15:0	WO	0	**Video Working ID**

Offset Address: 326Ch

Video Wait Control Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	WO	0	**Wait 3D IDLE – For Video Command Path**
30	WO	0	**Wait 2D IDLE – For Video Command Path**
29:25	WO	0	**Wait Idle Count**
24:22	RO	0	**Reserved**
21	WO	0	**Wait V3 Starting Address Load**
20	WO	0	**Wait V3 Fire Bit**
19	WO	0	**For V3 path, wait HQV HW flip FIFO full**
18	WO	0	**For V3 path, wait HQV Subpicture / Update Overlay Flip**
17	WO	0	**For V3 path, wait HQV SW flip**
16	WO	0	**For V3 path, wait HQV finish a frame**
15:6	RO	0	**Reserved**
5	WO	0	**Wait V1 Starting Address Load**
4	WO	0	**Wait V1 Fire Bit**
3	WO	0	**For V1 path, wait HQV HW flip FIFO full**
2	WO	0	**For V1 path, wait HQV Subpicture / Update Overlay Flip**
1	WO	0	**For V1 path, wait HQV SW flip**
0	WO	0	**For V1 path, wait HQV finish a frame**

Video Capture Engine and HQV Register Descriptions

Video Capture Control Registers (Only For Group A)

Offset Address: 300h

Capture Interrupt Control and Flags **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:11	RO	0	**Reserved**
10	RW	0	**Current Writing VBI Buffer ID**
9	RW	0	**End of VBI Interrupt Enable**
8	RW	0	**End of Active Video Interrupt Enable** If TS(Transport Stream) is enabled, it defines as TS data over a buffer interrupt enable
7	RO	0	**Video Capture Port Internal FIFO Full Status**
6	RO	0	**Current Active Video Input Field Status** 0: Top field 1: Bottom field
5	RO	0	**Current Input Vsync Status** 0: Vertical blanking 1: Active video
4:3	RO	0	**Current Writing Active Video (or TS data) Frame Buffer ID**
2	RO	0	**Flipping Active Video Field Status** 0: Top field 1: Bottom field
1	RO	0	**Video Capture End-of-VBI Status**
0	RO	0	**Video Capture End-of-Active Video Status** If TS is enabled, it defines as TS data over a buffer status

Note: Write 1 to clear bits [1:0] and [7]

Offset Address: 308h

Transport Stream Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:19	RO	0	**Reserved**
18:4	RW	0	**Packet_Number_Minus_One** There are (Packet_Number_Minus_One + 1) packets per buffer
3:2	RW	0	**Method to Move Received TS Data** 0x: Capture engine write data to FB. After fill a buffer, trigger an interrupt to driver. 10: Capture engine write data to FB. After fill a buffer, trigger an interrupt to DMA. 11: Capture engine control DMA to move data. (not via frame buffer) (In mode=2'b11, set FIFO Threshold Rx310[27:24] to 1)
1	RW	0	**Drop Error Packet** This bit is only valid at TS_DERR pin is available 0: Write all received data out. 1: Drop the data of error packet
0	RW	0	**Transport Stream Input Enable** 0: Disable 1:enable Turn on this bit before enable Capture Engine Rx310[0]

Offset Address: 310h

Capture Interface Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Capture CLK Enable** 0: Disable 1: Enable This bit should turn on before Rx310[0]
30	RW	0	**Capture FIELD Signal Output Inverted Select** 1: Inverted
29	RW	0	**Vertical Count Starting Reference** 0: Negative edge of VREF 1: Positive edge of VREF
28	RW	0	**Horizontal Count Starting Reference** 0: Negative edge of HREF 1: Positive edge of HREF
27:24	RW	0	**Capture FIFO Threshold (Unit: level)** Once the queuing captured data more than the threshold, it starts to write data out. Unit of 1st Capture Engine is 4-level, the FIFO size is 64level x 64bit Unit of 2nd Capture Engine is 2-level, the FIFO size is 32level x 64bit
23	RW	0	**Switch Capture Clock Source** Since there are two Capture clock sources, use this bit to switch it. In VIP2.0 while using task bit to differentiate video stream, it need to switch the clock source as the same one. For 1st Capture engine: 0: clock from 1st Capture CLK pin 1: clock from 2nd Capture CLK pin For 2nd Capture engine: 0: clock from 2nd Capture CLK pin 1: clock from 1st Capture CLK pin
22	RW	0	**Capture FIELD Input Inverted Select** 1: Inverted
21	RW	0	**Capture HREF Input Inverted Select** 1: Inverted
20	RW	0	**Capture VREF Input Inverted Select** 1: Inverted
19	RW	0	**Capture CLK Input Inverted Select** 1: Inverted
18:16	RW	0	**Capture Horizontal Filter Mode Select. (2P)** 000: No filtering 001: 2 tap (1,1)/2 010: 3 tap (1,2,1)/4 011: 4 tap (1,3,3,1)/8 100: 5 tap (1,2,2,2,1)/8 101~111:Reserved
15	RW	0	**Capture Flipping Control at Rx310[13:12] set to 2'b11** 0: Capture engine flip to HQV or Video engine after captured a frame. 1: Capture engine flip to HQV or Video engine after captured a field (HQV or Video should set to frame_to_field)
14	RW	0	**4:2:2 to 4:4:4 Cb, Cr Type Select** 0: Duplication 1: Interpolation
13:12	RW	0	**Capture De-interlace Mode Select** 00: Capture odd field only, 30fps 01: Capture even field only, 30fps 10: Capture odd/even field, 60fps; place on the same location 11: Capture odd/even field, 30fps; place in interlace fashion doubling the storage space
11	RW	0	**Input FIELD Signal Enable** If TS enable, it defines as TS_DERR signal enable 0: Disable 1: Enable
10	RW	0	**VIP Type** 0: VIP1.1, VBI data region specify by task bit. 1: VIP2, VBI data region specify by SAV/EAV during vertical blanking period
9:8	RW	0	**Byte Swapping Control** 00: 0123 (no swap: YUYV) 01: 1032 (C, Y swap: UYVY) 10: 0321 (Cr, Cb swap: YVYU) 11: 3012 (Cr, Cb swap and Y swap: VYUY)

7	RW	0	**16 Bit Input Low/High Swap** 1: Low / high byte inverted
6	RW	0	**CCIR656-16 Bit Header Decode Mode** 0: Low 8bit 1: 16bit all
5:4	RW	0	**Input Stream Type** 00: CCIR601-8bit; 01: CCIR656-8bit; 10: CCIR601-16bit; 11: CCIR656-16bit.
3	RW	0	**VIP Enable** 0: Disable 1: Enable
2	RW	0	**Buffer Mode** 0: Double buffers, use starting address 1 and 2; 1: Triple buffers, use starting address 1, 2 and 3.
1	RW	0	**Bit Stream Selection of VIP2.0** In VIP2.0, task bit to differentiate video stream. For 1st Capture engine: 0: Capture the data of task bit is 0 1: Capture the data of task bit is 1 For 2nd Capture engine: 0: Capture the data of task bit is 1 1: Capture the data of task bit is 0
0	RW	0	**Capture Enable** 0: Disable 1: Enable

Offset Address: 314h

Active Video Horizontal Range **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RO	0	**Reserved**
27:16	RW	0	**Horizontal Ending Line** (CCIR601 only). (Unit: Line)
15:12	RO	0	**Reserved**
11:0	RW	0	**Horizontal Starting Line** (CCIR601 only). (Unit: Line)

Offset Address: 318h

Active Video Vertical Range **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RO	0	**Reserved**
27:16	RW	0	**Vertical Ending Line** (CCIR601 only). (Unit: Line)
15:11	RO	0	**Reserved**
10:0	RW	0	**Vertical Starting Line** (CCIR601 only). (Unit: Line)

Offset Address: 31Ch

Active Video Scaling Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
26	RW	0	**Vertical Minify Enable** 0: Disable 1: Enable
25:16	RW	0	**Vertical Minify Factor**
15:12	RO	0	**Reserved**
11	RW	0	**Horizontal Minify Enable** 0: Disable 1: Enable
10:0	RW	0	**Horizontal Minify Factor**

Offset Address: 320h
VBI Data Horizontal Range **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:16	RW	0	**Horizontal Ending Line** (Unit: Line)
15:12	RO	0	**Reserved**
11:0	RW	0	**Horizontal Starting Line** (Unit: Line)

Offset Address: 324h
VBI Data Vertical Range **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RO	0	**Reserved**
27:16	RW	0	**Vertical Ending Line** (Unit: Line)
15:11	RO	0	**Reserved**
10:0	RW	0	**Vertical Starting Line** (Unit: Line)

Offset Address: 328h
First VBI Buffer Starting Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**VBI Data Enable** 0: Disable 1: Enable
30	RW	0	**VBI Mode Select** 0: Range depend on SAV/EAV 1: Capture by specify range (define by register 320h, 324h) If VIP enable (Rx310.[3]=1), this bit setting would be ignored, capture VBI data defined as VIP spec.
29	RO	0	**Reserved**
28:23	RW	0	**VBI or ANC Buffer 0 Starting Address** (Unit: 8 bytes)
2:0	RO	0	**Reserved**

Offset Address: 32Ch
VBI Buffer Stride **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:14	RO	0	**Reserved**
13	RW	0	**VBI Data Placement Method** 0: Linear, no stride needed 1: With stride
12:3	RW	0	**VBI Buffer Stride** (Unit: 8 bytes)
2:0	RO	0	**Reserved**

Offset Address: 330h
Ancillary Data Count Setting **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:15	RO	0	**Reserved**
14	RW	0	**Ancillary Data.Type** 0 : Type2 – 00-FF-FF-DID-SDID-NN-….-….-CheckSumByte-FillBytes. Total captured data are (8Bytes + NN*4Bytes). 1: Type1 – 00-FF-FF-DID-DBN-NN-….-….-CheckSumByte-FillBytes. Total captured data are (8Bytes + (DBN+NN)*4Bytes).
13	RW	0	**Ancillary Data Enable** 0: Disable 1: Enable.
12	RW	0	**Ancillary Data Count Reference Select** 0: By header decoder 1: By register (define by Rx330[11:0]).
11:0	RW	0	**Ancillary data should be capture length** (Unit: Double-word)

Offset Address: 334h

Maximum Data Count of Active Video **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RO	0	**Reserved**
26:16	RW	0	**Maximum Active Video Line Count in a field** (Unit: Line). If TS enable, it defines as the maximum TS data count of a packet (Unit: Byte)
15:9	RO	0	**Reserved**
8:0	RW	0	**Maximum Active Video QW Count in a line** (Unit: 8 bytes).

Offset Address: 338h

Maximum Data Count of VBI or ANC **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RO	0	**Reserved**
26:16	RW	0	**Maximum VBI or ANC Line Count in a field** (Unit: Line).
15:9	RO	0	**Reserved**
8:0	RW	0	**Maximum VBI or ANC QW Count in a line** (Unit: 8 bytes).

Offset Address: 33Ch

Capture Data Count **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**Current Active Video Line Counter**. (Unit: Line)
15:13	RO	0	**Reserved**
12:0	RW	0	**VBI or ANC Data has been captured length**. (Unit: 8 bytes)

Offset Address: 340h

First Active Video Frame Buffer Starting Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:3	RW	0	**Active Video Frame Buffer 0 Starting Address** (Unit: 8 bytes) If TS enable, it defines as frame buffer 0 starting address for TS data
2:0	RO	0	**Reserved**

Offset Address: 344h

Second Active Video Frame Buffer Starting Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:3	RW	0	**Active Video Frame Buffer 1 Starting Address** (Unit: 8 bytes) If TS enable, it defines as frame buffer 1 starting address for TS data
2:0	RO	0	**Reserved**

Offset Address: 348h

Third Active Video Frame Buffer Starting Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:3	RW	0	**Active Video Frame Buffer 2 Starting Address** (Unit: 8 bytes) If TS enable, it defines as frame buffer 2 starting address for TS data
2:0	RO	0	**Reserved**

Offset Address: 34Ch

Second VBI Buffer Starting Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:3	RW	0	**VBI or ANC Buffer 1 Starting Address** (Unit: 8 bytes) If TS enable, it defines as frame buffer 0 starting address for TS data
2:0	RO	0	**Reserved**

Offset Address: 350h

Stride of Active Video Buffer & Coring Function Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Reserved**
23	RW	0	**Coring Function Enable**
22:16	RW	0	**Coring Function Compare Data (CCD)** (If coring function enable(Rx350[23]) and (-(CCD+1) <= U, V <= CCD), then all of these U and V will be truncated to zero)
15:13	RO	0	**Reserved**
12:3	RW	0	Stride of Active Video Buffer (Unit: 8 bytes)
2:0	RO	0	**Reserved**

Offset Address: 354h

TS Buffer0 Error Packet Indicator **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Last Error Packet Indicator** 0: Less than one error packet in this buffer, defined at [15:0] 1: More than two error packets, the last error packet ID defined at [30:16]
30:16	RW	0	**Last Error Packet ID**
15	RW	0	**First Error Packet Indicator** 0: No error packet in this buffer 1: More than one error packet, the first error packet ID defined at [14:0]
14:0	RW	0	**First Error Packet ID**

Offset Address: 358h

TS Buffer1 Error Packet Indicator **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Last Error Packet Indicator** 0: Less than one error packet in this buffer, defined at [15:0] 1: More than two error packets, the last error packet ID defined at [30:16]
30:16	RW	0	**Last Error Packet ID**
15	RW	0	**First Error Packet Indicator** 0: No error packet in this buffer 1: More than one error packet, the first error packet ID defined at [14:0]
14:0	RW	0	**First Error Packet ID**

Offset Address: 35Ch

TS Buffer2 Error Packet Indicator **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Last Error Packet Indicator** 0: Less than one error packet in this buffer, defined at [15:0] 1: More than two error packets, the last error packet ID defined at [30:16]
30:16	RW	0	**Last Error Packet ID**
15	RW	0	**First Error Packet Indicator** 0: No error packet in this buffer 1: More than one error packet, the first error packet ID defined at [14:0]
14:0	RW	0	**First Error Packet ID**

Note: Capture supports 2 input interface; therefore, an additional register space is provided to match the above registers definition.

Writing a register to this space, it will write to the second Capture Engine.

The relationship between the additional register space and original register space is

(The additional register address) = (The original register address) + 16'h1000.

Video Processor Registers

Offset Address: 3BCh

De-blocking Factor **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:20	RO	0	**Reserved**
19:18	RO	0	**HQV Current Process Destination Buffer ID**
17	RW	0	**HQV Output Field** 1: Bottom field
16	RW	0	**HQV Current Process Field** 1: Bottom field
15	RW	0	**Bob De-interlacing Method** 0: Line average 1: Line duplication (for TV output)
14:10	RW	0	**De-blocking Factor2 (0.xxxxx)** Recommend value: 19
9:5	RW	0	**De-blocking Factor1 (0.xxxxx)** Recommend value: 6
4:0	RW	0	**De-blocking Factor0 (0.xxxxx)** Recommend value: 10

Offset Address: 3C0h

Subpicture Frame Buffer Stride and Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RW	0	**MC Flipping Count** HQV update read out register data at the beginning of HQV processing a frame.
23:20	RO	0	**Reserved**
19	RW	0	**Subpicture Format** 0: AI44 or IA44 1: AYUV (MSB A(8)-Y(8)-U(8)-V(8) LSB)
18	RW	0	**Inverse Alpha Value in AI44 Mode** 1: Inverse (One's Complement)
17	RW	0	**Alpha, Index Exchange in AI44 Mode** 0: AI44 1: IA44
16	RW	0	**HQV Subpicture Enable** 1: Enable Only active at HQV source format is YUV; default:0)
15:14	RO	0	**Reserved**
13:4	RW	0	**Subpicture Frame Buffer Stride** Unit: 16 bytes
3:0	RO	0	**Reserved**

Offset Address: 3C4h

Subpicture Frame Buffer Starting Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:3	RW	0	**Subpicture Frame Buffer Starting Address** (Unit: 16 bytes)
2:0	RO	0	**Reserved**

Offset Address: 3C8h

Subpicture 4x16 RAM Table Write Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RW	0	**RAM Table Write Data** V: [31:24] U: [23:16] Y: [15:8]
7:4	RW	0	**RAM Table Read / Write Address** Indicate which entry of palette table will be written or read. Palette table contains 16 entries of palette data. (HQV3C8[7:4]=0x0000 ~ HQV3C8[7:4]=0x1111) Need to program HQV3C8[31:8] and HQV3C8[7:4] 16 times to fill the subpicture palette table.
3	RO	0	**Reserved**
2	RW	0	**V Write Enable** 0: Disable 1: Enable
1	RW	0	**U Write Enable** 0: Disable 1: Enable
0	RW	0	**Y Write Enable** 0: Disable 1: Enable

Offset Address: 3CCh

HQV Source Data Offset Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:16	RW	0	**Video Source Data Horizontal Offset** (Unit: Byte) (2P)
15:11	RO	0	**Reserved**
10:0	RW	0	**Video Source Data Vertical Offset** (Unit: Line) (2P)

Offset Address: 3D0h

HQV Stream Control and Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RW	0	**Video Data Stream Format [3:0]** 0000: RGB32 – (X8R8G8B8) 0010: RGB16 – (R5G6B5) 0011: RGB15 – (X1R5G5B5) 1000: YUV422 – ($V8Y_1 8U8Y_0 8$) 1100: YUV420 – (NV12; planar mode) others:reserved
27	RW	0	**High Quality Video Enable** 0: Disable 1: Enable
26	RW	0	**Buffer Mode** 0: Double destination buffers 1: Triple destination buffers
25:24	RW	0	**Video Stream Source [1:0]** 00: SW 01: MC 10: Capture 0 11: Capture 1
23	RW	0	**Advanced De-interlace Mode Enable**
22:21	RW	0	**Vertical Low Pass Filter** 00: No filtering. 01: (2,12,2)/16 1x: (4,8,4)/16
20	RW	0	**Planar Mode Chrominance Source Data Format** 0: Source Chrominance is saved by frame picture 1: Source Chrominance is saved by field picture
19	RW	0	**Inverse Input Field** 1: Inversed
18	RW	0	**Frame To Field** 1: Frame base source, field display If this bit is set to 1, then Rx3D0[7] must be 1.
17	RW	0	**Field To Frame** 1: Field source, fetch each line twice to display
16	RW	0	**Bob Mode (De-Interlace Mode)** 1: First line will be repeated once in bottom field
15	RW	0	**Subpicture Flip** Software writes 1 to this bit indicates a new subpicture need to blending. After blending completed, Hardware clears it to 0. Software can read this bit to check the status if Hardware completed blending.
14	RO	0	**Reserved**
13	RO	0	**HQV Current Process Field** 0: Top 1: Bottom
12	RO	0	**HQV Flip FIFO Full Status** The FIFO depth defined in Rx3F8 [18:16]
11	RO	0	Status of "HQV has completed processing but waiting a Vsync pulse to flip"
10	RO	0	**Reserved**
9:8	RW	0	**HQV Current Process ID[1:0] (RO)** HQV'S destination buffer ID.
7	RW	0	**HQV Interrupt Enable** 0: Disable HQV interrupt. 1: HQV send interrupt signal after done a frame. Relative setting: Rx3D0[0].
6	RW	0	**Single Destination Buffer** 1: Single buffer used Rx3D0[26] would be ignored.
5	RW	0	**Field of Software Source Input** 0: Top 1: Bottom
4	RW	0	**Software Source Flip** Software write 1 to flip a image to HQV. (Rx3D0[25:24] should be 00b) After processing completed, Hardware clears it to 0. Software read this bit to check flip status.
3	RO	0	**HQV Engine Idle State** 1: Idle
2:1	RO	0	**HQV Output Buffer ID** HQV destination buffer ID

0	RW	0	**HQV End of Frame Status** 1:HQV has been output an image. (Software write 1 to clear this bit) After HQV done an image, this bit will be pulled high, and it will be pulled down only at software write 1b to it.

Offset Address: 3D4h

HQV SW Source Data – Luma or Packed Starting Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:4	RW	0	**SW Source Data Y or Packed Mode Starting Address** (Unit: 16 bytes)
3:0	RO	0	**Reserved**

Offset Address: 3D8h

HQV SW Source Data – Chroma Starting Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:4	RW	0	**SW Source Data U, V Starting Addresses** (Unit: 16 bytes)
3:0	RO	0	**Reserved**

Offset Address: 3DCh

HQV Linear / Tile Address Mode, Color Space Conversion, Gamma, De-blocking Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RW	0	**Linear / Tile Address Mode Control** (Tile address only enable at source data from MC, 3D0[25:24]=2'b01) 00: Linear 01: Reserved 10: 256 bits tile mode (Addr = SA + (Y[10:4]*PTH*16) + {X[10:1],Y[3:0],X[0]}), 11: 512 bits tile mode (Addr = SA + (Y[10:4]*PTH*16) + {X[10:2], Y[3:0],X[1:0]}). Where unti of X is 128-bit; unit of Y is line.
29	RW	0	**HQV Output Data Pack In 32bit Mode.** 0:16bit(RGB565). 1:32 bit (RGB888) (Only valid at source is YUV and color space conversion enable.)
28	RW	0	**Color Space Conversion Enable** 0: Disable 1: Enable
27	RW	0	**De-blocking Enable**
26	RW	0	**Enable Low Pass Filter in Both Vertical / Horizontal Direction while de-blocking.** 1: Enable
25	RO	0	**Reserved**
24:20	RW	0	**HQV Output FIFO Threshold for Write Request Control** (Unit: level) HQV output FIFO has 64 levels, once the data in output FIFO touch the threshold (32+3DC.[23:20]), the write request would be triggered.
19:16	RO	0	**Reserved**
15	RW	0	**The Value of the MSB of RGB32 Format** 0: 00 1: FF
14	RW	0	**Enable Synchronization Flipping Field with Interlaced IGA** 1: Enable
13	RW	0	**IGA Field Inverse** 1: Inverse
12:11	RO	0	**Reserved**
10:0	RW	0	**Image Size / 1024** Pull-down detection use.

Offset Address: 3E0h

HQV Source Data Line Cont and Fetch Count Per Line **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:16	RW	0	**Video Source Data Fetch Count Per Line (-1)** Unit: Bytes
15:11	RO	0	**Reserved**
10:0	RW	0	**Video Source Data Line Number (-1)** Unit: Line

Offset Address: 3E4h

HQV Motion Adaptive De-interlace Control & Threshold **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**2:2 Pull Down Sequence Detection Enable** 0: Disable 1: Enable Relative setting: Rx3E4[30:28], Rx 3E4[26:25], Rx 3DC[10:0] and Rx3E4[19:14].
30:28	RW	0	**Threshold of Inter-field Complexity for Pull Down Detection (x4).** Recommend value Rx3E4[30:28] : 4. Calculate the difference between current (fn) & previous field (fn-1).
27	RW	0	**3:2 Pull Down Sequence Detection Enable** 0: Disable 1: Enable Relative setting: Rx 3E4[30:28], Rx 3E4[26:25], Rx 3DC[10:0] and Rx3E4[19:14].
26:25	RW	0	**Factor of Calculating Threshold of Intra-field Complexity** 00: Threshold = 3E4[30:28]*4 + 3E4[30:28]*1; 01: Threshold = 3E4[30:28]*4 + 3E4[30:28]*2; 10: Threshold = 3E4[30:28]*4 + 3E4[30:28]*3; 11: Threshold = 3E4[30:28]*4 + 3E4[30:28]*4; (Recommended)
24:20	RO	0	**Reserved**
19:18	RW	0	**Pull-down Factor2** Apply this factor while pull-down detected 00: 3/8 01: 4/8 (Recommended) 10: 5/8 11: 6/8
17:16	RW	0	**Pull-down Factor1** Apply this factor while pull-down not yet detected. 00: 2/8 (Recommended) 01: 3/8 10: 4/8 11: 5/8
15:14	RW	0	**Threshold for Pull Down Detection** Recommend value Rx3E4[15:14]: 2. (Rx3DC[10:0] << Rx3E4[15:14]) as the minimum threshold for valid pull down detection
13:8	RO	0	**Reserved**
7	RO	0	**2:2 Pull Down Detection Status**
6	RO	0	**3:2 Pull Down Detection Status**
5	RO	0	**Reserved**
4:1	RW	0	**Edge Detection Threshold: for Degree 90 (x2).** Recommend value for Rx3E4[4:1]: 8
0	RW	0	**Edge Detection Enable** 0: Disable 1: Enable Relative setting: Rx3E4[4:1].

Offset Address: 3E8h

HQV Scale Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28	RW	0	**Vertical Scale Function** 0: Up 1: Down. (2P)
27	RW	0	**Vertical Scale Enable** 1: Enable (2P)
26:16	RW	0	**Vertical Scale Factor [10:0](2P)**
15:13	RO	0	**Reserved**
12	RW	0	**Horizontal Scale Function** 0: Up 1: Down (2P)
11	RW	0	**Horizontal Scale Enable** 1: Enable (2P)
10:0	RW	0	**Horizontal Scale Factor [10:0] (2P)**

Offset Address: 3ECh

HQV Destination Data Starting Address 0 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**Reserved**
30	RW	0	**Enable Output In Tile Mode** 1:Enable. Addr = ST_ADDR[28:4] + Y[10:3]*{PITCH[10:0], 3'b0} + {X[10:1], Y[2:0], X[0]}
29	RO	0	**Reserved**
28:4	RW	0	**Destination Data Starting Address 0** Unit: 16 bytes
3:0	RO	0	**Reserved**

Offset Address: 3F0h

HQV Destination Data Starting Address 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:4	RW	0	**Destination Data Starting Address 1** Unit: 16 bytes
3:0	RO	0	**Reserved**

Offset Address: 3F4h

HQV Destination Frame Buffer Stride **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:14	RO	0	**Reserved**
13:4	RW	0	**Destination Frame Buffer Stride** Unit: 16 bytes
3:0	RO	0	**Reserved**

Offset Address: 3F8h

HQV Source Frame Buffer Stride **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RW	0	**Load Starting Address 3D4[25:4], 3D8[25:4] for Advanced De-interlacing.** 00: No used. -- Hardware keep starting address 01: Reserved 10: Load starting address to previous field. F(n-1) 11: Load starting address to current field. F(n) Note: command sequence First load to F(n-1): Rx3F8[31:30]=2'b10 then Rx3D4, Rx 3D8 Second load to F(n) : Rx3F8[31:30]=2'b11 then Rx 3D4, Rx 3D8
29:21	RW	0	**For fixing bug: Spare register.**
20	RW	0	**Software Flip Queue Enable** 0: Pull Rx 3D0[4] low at frame done. 1: Pull Rx 3D0[4] low at beginning of processing frame
19	RW	0	**Read Debugging Register.**
18	RO	0	**Reserved**
17:16	RW	0	**FIFO Depth of HQV Flip Control Engine** Only supports 2 stages FIFO queuing MC flipping address. 00: Pull "FIFO full status Rx 3D0[12]" high, while both two stage are queuing. Drop current processing frame while both two stage are queuing. 01: Pull "FIFO full status Rx 3D0[12]" high, while one stage is queuing. Drop current processing frame while both two stage are queuing. 10: Pull "FIFO full status Rx 3D0[12]" high, while both two stage are queuing. Never drop current processing frame. 11: Pull "FIFO full status Rx 3D0[12]" high, while one stage is queuing. Never drop current processing frame.
15:14	RO	0	**Reserved**
13:4	RW	0	**Source Frame Buffer Stride** (Unit: 16 bytes)
3:0	RO	0	**Reserved**

Offset Address: 3FCh

HQV Destination Data Starting Address 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:4	RW	0	**Destination Data Starting Address 2** Unit: 16 bytes
3:0	RO	0	**Reserved**

Note: HQV supports 2 Video Streams; therefore, an additional register space is provided to match the above registers definition. Writing a register to this space, it will write to the second HQV, which output to V3, but the second HQV don't support Hardware flip from MC engine.
The relationship between the additional register space and original register space is
(The additional register address) = (The original register address) + 16'h1000.

3D ENGINE REGISTERS

This chapter provides detailed 3D engine register descriptions which are followed in the sequent sections.

Definition of I/O Register

The I/O Register Base Address for UniChrome Pro II 3D GFX is 400h.

For Write Mode

<table>
<tr><th>Scope</th><th>Offset</th><th>Description</th><th>Mnemonic</th></tr>
<tr><td>Explicit 3D Engine Fire</td><td>03h-00h</td><td>Dedicated 3D Engine Fire Register. Any write to this register will cause a 3D Engine Fire.</td><td>HE3Fire</td></tr>
<tr><td></td><td>3B-04h</td><td>Reserved</td><td></td></tr>
<tr><td rowspan="4">Transmission Setting</td><td>3Ch</td><td>The Beginning of Internal Address for Parameter Programming</td><td>HParaAdr</td></tr>
<tr><td>3Dh</td><td>Offset Setting for Some Special Parameter Types</td><td>HParaOS</td></tr>
<tr><td>3Eh</td><td>Parameter Type

<table>
<tr><th>HParaType</th><th>Description</th></tr>
<tr><td>0000 0000</td><td>Command and Primitive Vertex Data</td></tr>
<tr><td>0000 0001</td><td>Attribute Other Than Texture</td></tr>
<tr><td>0000 0010</td><td>Attribute of Texture n
n is the number stored in HparaSubType (Rx3F):
0000 0000 = Texture 0
0000 0001 = Texture 1
1111 1110 = General Texture Setting

The use of 1111 1111 is prohibited.
Others = Reserved</td></tr>
<tr><td>0000 0011</td><td>Palette
HParaSubType (Rx3F) shows the palette type:
0000 0000 = Texture Palette 0
0000 0001 ~ 0000 0111 (Reserved)
0000 1xxx = Reserved
0001 0000 = Fog Palette
0001 0100 = Stipple Palette</td></tr>
<tr><td>0000 1111 ~ 1111 1111</td><td>Reserved</td></tr>
</table>

For more details for the parameters, please refer to Definition of Parameter section.</td><td>HParaType</td></tr>
<tr><td>3Fh</td><td>Parameter Type Sub-code</td><td>HParaSubType</td></tr>
<tr><td rowspan="10">Transmission Space</td><td>43h-40h</td><td>Parameter 0</td><td>Hpara0</td></tr>
<tr><td>47h-44h</td><td>Parameter 1</td><td>Hpara1</td></tr>
<tr><td>4Bh-48h</td><td>Parameter 2</td><td>Hpara2</td></tr>
<tr><td>…….</td><td>…….</td><td></td></tr>
<tr><td>1F7h-1F4h</td><td>Parameter 109</td><td>Hpara6D</td></tr>
<tr><td>1FBh-1F8h</td><td>Parameter 110</td><td>Hpara6E</td></tr>
<tr><td>1FFh-1FCh</td><td>Parameter 111</td><td>Hpara6F</td></tr>
<tr><td>……</td><td>…….</td><td></td></tr>
<tr><td>2FFh-2FCh</td><td>Parameter 175</td><td>HparaAF</td></tr>
</table>

For Read Mode

Offset Address: 03-00h
Engine Status (HREngSt)

Bit	Description	Mnemonic
31:19	**Reserved**	
18	**RC Status** 0: Idle 1: Busy	**HRRCst**
17	**Command Queue is Empty** 0: Not Empty 1: Empty	**HCMDQEMPTY**
16:2	**Reserved**	
1	**2D Engine Status** 0: Idle 1: Busy	**HRE2st**
0	**3D Engine Status** 0: Idle 1: Busy	**HRE3st**

Offset Address: 0B-04h: Reserved

Offset Address: 0F-0Ch
Error Flag (HRErr)

Bit	Description	Mnemonic
31	**Error Flag for AGP Command Decoding** 0: No illegal Command detected 1: There is at least one illegal Command detected Definition of Error Command: TBD	**HRAGPCMErr**
30	**Un-expected Command Header Error** 0: No Un-expected Command Header 1: Un-expected Command Header Happened AGP Command Header 1, 2, 3, and 4 mush follow on data. Only Header 0 can be used for command A and B. After Command A, it must be vertex data. Thus, any command header happened which violate the previous rule. CR will report this error. (However, CR cannot detect if any command header happen in the vertex transmission sequence. A header may be defined as part of the vertex data.)	**HRAGPNHErr**
29	**Data Number Down to Zero Error** 0: No Such Error 1: In AGP Command Header 3, if the transmission data count down to zero, we must have another command header. If it is not, this error is reported.	**HRAGPDOErr**
28	**Data Number Overflow Error** 0: No Such Error 1: In AGP Command Header1, only one data is following on the command header. If the data is more than one, this error is reported.	**HRAGPDOErr**
27:0	**Reserved**	

Offset Address: 13-10h

Bit	Description	Mnemonic
31	**Summary of FIFO Auto Testing Result** 0: All FIFO pass auto testing 1: At least one FIFO does not pass the auto testing	**HRFIFOATall**
30:0	**Reserved**	

Offset Address: 1B-14h: Reserved

Offset Address: 1F-1Ch

Bit	Description	Mnemonic
31	**CR read AGP command cycle is in pause status** 0: Not in pause status 1: In pause status	**HRAGPCYCpause**
30	**CR read AGP command cycle is finished** 0: Not finished 1: Finished	**HRAGPCYCidle**
29:0	**Reserved**	

Offset Address: 20-47h: Reserved

Offset Address: 4B-48h

Bit	Description	Mnemonic
31	**CR is in CMDQ Cycle**	**HRCMDQ_CYC**
30	**CMDQ Full**	**HRCMDQFULL**
29:6	**CMDQ Data Count**	**HRCMDQ_CNT**
5	**CR is in AGP Cycle**	**HRCRAGP_CYC**
4:0	**Issued AGP Command Count**	**HRCRAGP_CNT**

Offset Address: 4F-4Ch

Data	Description	Mnemonic
31:8	**Reserved**	
7	**The Idle Signal for PS to XE**	**PS2XE_IDLE**
6	**The Idle Signal for CR fire Unlock**	**RZPRIDLE**
5:4	**CR Data Status (=>SPT_ADR[11:0])**	**HRCR_STATUS**
3	**2D Command Lock Signal**	**E2CMD_LOCK**
2	**3D Command Lock Signal**	**E3CMD_LOCK**
1	**Frame Buffer Swap Lock signal**	**FBSW_LOCKCMD**
0	**Fire Lock Signal**	**FFRE_LOCK**

Offset Address: 53-50h

Bit	Description	Mnemonic
31:14	**Reserved**	
13	**The Idle Signal for RC's De-Packing to BE**	**HRRCDPKBEidle**
12:10	**The State of RC's De-Packing to BE**	**HRRCDPKBEstate**
9	**The Idle Signal for RC's FIFO**	**HRRCFIFOidle**
8	**The Idle Signal for RC's PIPE**	**HRRCPIPEidle**
7	**The Idle Signal for RC's Request MI**	**HRRCREQMIidle**
6:4	**The State of RC's De-Packing to XE**	**HRRCDPKXEstate**
3:2	**The Ready Signal of RC's Data FIFO**	**HRRCRAMready**
1:0	**The State of RC's Packing Module**	**HRRCPACKstate**

Offset Address: 63-60h

Bit	Description	Mnemonic
31:25	**Reserved**	
24	**The Ready Signal to the Bubble between XE and PE**	**HRXE0_XPEREADY**
23:20	**The Ready Signals of the 4 Stages of XE1_AP** D[23]: Stage 3 D[22]: Stage 2 D[21]: Stage 1 D[20]: Stage 0	**HRXE0_XACTRLREADY**
19:18	**State when Operation Bump-mapping** 010: "Decrease" state when operating normal texture 001: "Increase" state when operating bunp-mapping texture 000: "Initial" state when operating bump-mapping txxture	**HRXE0_BUMP_STATE**
17:12	**Number of Data when Operating Bump-mapping**	**HRXE0_COUNT_IN**
11	**If A-channel Operates as 2-cycle per 1-pixel** 0: 1Cycle/1P 1: 2Cycle/1P	**HRXE0_TWO_A**
10	**If B-channel Operates as 2-cycle per 1-pixel** 0: 1Cycle/1P 1: 2Cycle/1P	**HRXE0_TWO_B**
9	**Full or not of Fraction-FIFO** 0: Not full 1: Full	**HRXE0_FIFOFULL34**
8	**Full or not of ARGB-FIFO** 0: Not full 1: Full	**HRXE0_FIFOFULL84**
7	**Empty or not of Fraction-FIFO** 0: Not empty 1: Empty	**HRXE0_FIFOENPTY34**
6	**Empty of not of ARG-FIFO** 0: Not empty 1: Empty	**HRXE0_FIFOEMPTY84**
5	**The full Signal of AP (XE1_AP)** 0: Not full 1: Full	**HRXE0_XAP_FULL**
4	**The Ready Signal to ARGB-FIFO**	**HRXE0_ARGB_RDY**
3	**The Acknowledge Signal to PE**	**HRXE0_XEACK**
2	**The Ready Signal to AP**	**HRXE0_XPEREADY**
1	**The Acknowledge Signal to Bubble between XE and PERZ**	**HRXE0_XXEACK_NXT**
0	**The Acknowledge Signal of Z-FIFO**	**HRXE0_BE_ZACK**

Offset Address: 67-64h

Signals of The Path When Operating Normal Texture Mapping (HRX1_TXMP)

Bit	Description	Mnemonic
31	XE to XC Pip Full	
30	XE1 to XE0 Color FIFO Read Acknowledge	
29	XE1 to XE0 Fraction FIFO Read Acknowledge	
28	XE1 to XE0 Z FIFO Read Acknowledge	
27	Transparency Test Pipe 0 Enable	
26	Texture Filtering Pipe 0 Enable	
25	Texture Filtering Pipe 1 Enable	
24	Texture Filtering Pipe 2 Enable	
23	Texture Blending pipe Enable	
22	Texture Blending (one texture) Pipe 0 Enable	
21	Texture Blending (one texture) Pipe 1 Enable	
20	Texture Blending (two texture) Pipe 0 Enable	
19	Texture Blending (two texture) Pipe 1 Enable	
18	Texture Blending (two texture) Pipe 2 Enable	
17	Texture Blending (two texture) Pipe 3 Enable	
16	Texture Blending (two texture) Pipe 4 Enable	
15	Fog and Alpha Test Pipe 0 Enable	
14	Fog and Alpha Test Pipe1 Enable	
13	Transparency Test Pipe 0 Ready	
12	Texture Filtering Pipe 0 Ready	
11	Texture Filtering Pipe 1 Ready	
10	Texture Filtering Pipe 2 Ready	
9	Texture Blending (one texture) Pipe 0 Ready	
8	Texture Blending (one texture) Pipe 1 Ready	
7	Texture Blending (two texture) Pipe 0 Ready	
6	Texture Blending (two texture) Pipe 1 Ready	
5	Texture Blending (two texture) Pipe 2 Ready	
4	Texture Blending (two texture) Pipe 3 Ready	
3	Texture Blending (two texture) Pipe 4 Ready	
2	Reserved	
1	XE Ready	
0	XE Internal Signal of BE Acknowledge	

Offset Address: 73-70h

Bit	Description	Mnemonic
31:24	Reserved	
23	Force 1 pipe instead of 2 pipes	HRenForce1P
22	Reserved	
21	Enable Environment Map Texture	HRenTXEnvMap
20	Reserved	
19	Reserved	
18	Reserved	
17	Enable BackFace Culling	HRenBFCull
16	Enable Color Write	HRenCW
15	Enable Anti-Aliasing	HRenAA
14	Enable Stencil Test	HRenST
13	Enable Z Test	HRenZT
12	Enable Z Write	HRenZW
11	Enable Alpha Test	HRenAT
10	Enable Alpha Write	HRenAW
9	Enable Stipple Pattern	HRenSP
8	Enable Line Pattern	HRenLP
7	Enable Texture Cache	HRenTXCH
6	Enable Texture Mapping	HRenTXMP
5	Enable Texture Perspective Correction	HRenTXPP
4	Enable Texture Transparency	HRenTXTR
3	Enable Specula Color	HRenCS
2	Enable Fog	HRenFOG
1	Enable Alpha Blending	HRenABL
0	Enable Dither	HRenDT

Offset Address: 77-74h

Bit	Description	Mnemonic
31:0	Current Command A	HRCMDA

Offset Address: 7B-78h

Bit	Description	Mnemonic
31:0	Current Command B	HRCMDB

Offset Address: 7F-7Ch

Bit	Description	Mnemonic
31:0	Starting Address of current Display Buffer	HRDisplayBst

Offset Address: 83-80h

Bit	Description	Mnemonic
31:0	Current Downer 32-bit Command to Graphic Engine	HRCurrentCMDD

Offset Address: 87-84h

Bit	Description	Mnemonic
31:0	Current Upper 32-bit Command to Graphic Engine	HRCurrentCMDU

Offset Address: 8B-88h

Bit	Description	Mnemonic
31:0	Status of Command Regulator 0	HRCRState0

Offset Address: 8F-8Ch

Bit	Description	Mnemonic
31:0	Status of Command Regulator 1	HRCRState1

Offset Address: 93-90h

Bit	Description	Mnemonic
31:0	Low 32 Bits of the Input of CR's 1st FIFO	HRCRFIFOIL

Offset Address: 97-94h

Bit	Description	Mnemonic
31:0	High 32 bits of the Input of CR's 1st FIFO	HRCRFIFOIH

Offset Address: 9B-98h

Bit	Description	Mnemonic
31:0	The Flag Number in AGP Command 2 16-bit Flag Number	HRCRFlagNum

Offset Address: 9F-9Ch: Reserved

Note: Please note from Rx74 to Rx9F, the read data is meanless, but the read access will cause AGP Control circuit flush.

Offset Address: A3-A0h

Bit	Description	Mnemonic
31:24	Reserved	
23:0	Write Register at ParaType 10h with SubAddress 00h	HRPType10Adr00

Offset Address: A7-A4h

Bit	Description	Mnemonic
31:24	Reserved	
23:0	Write Register at ParaType 10h with SubAddress 10h	HRPType10Adr10

Offset Address: AB-A8h

Bit	Description	Mnemonic
31:24	Reserved	
23:0	Write Register at ParaType 10h with SubAddress 60h	HRPType10Adr60

Offset Address: AF-ACh

Bit	Description	Mnemonic
31:24	Reserved	
23:0	Write Register at ParaType 10h with SubAddress 61h	HRPType10Adr61

Offset Address: B3-B0h

Bit	Description	Mnemonic
31:24	Reserved	
23:0	Write Register at ParaType 10h with SubAddress 62h	HRPType10Adr62

Offset Address: B7-B4h

Bit	Description	Mnemonic
31:24	Reserved	
23:0	Write Register at ParaType 10h with SubAddress 63h	HRPType10Adr63

Offset Address: BB-B8h

Bit	Description	Mnemonic
31:24	Reserved	
23:0	Write Register at ParaType 10h with SubAddress 64h	HRPType10Adr64

Offset Address: C3-C0h

Bit	Description	Mnemonic
31:24	Reserved	
23:0	Write Register at ParaType FEh with SubAddress 00h	HRPTypeFEAdr00

Offset Address: C7-C4h

Bit	Description	Mnemonic
31:24	Reserved	
23:0	Write Register at ParaType FEh with SubAddress 04h	HRPTypeFEAdr04

Offset Address: CB-C8h

Bit	Description	Mnemonic
31:24	Reserved	
23:0	Write Register at ParaType FEh with SubAddress 05h	HRPTypeFEAdr05

Offset Address: CF-CCh

Bit	Description	Mnemonic
31:24	Reserved	
23:0	Write Register at ParaType FEh with SubAddress 08h	HRPTypeFEAdr08

Offset Address: D3-D0h

Bit	Description	Mnemonic
31:24	Reserved	
23:0	Write Register at ParaType FEh with SubAddress 0Ah	HRPTypeFEAdr0A

Offset Address: D7-D4h

Bit	Description	Mnemonic
31:24	Reserved	
23:0	Write Register at ParaType FEh with SubAddress 0Bh	HRPTypeFEAdr0B

Offset Address: DD-D8h

Bit	Description	Mnemonic
31:24	Reserved	
23:0	Write Register at ParaType FEh with SubAddress 0Ch	HRPTypeFEAdr0C

Offset Address: DF-DCh

Bit	Description	Mnemonic
31:24	Reserved	
23:0	Write Register at ParaType FEh with SubAddress 0Dh	HRPTypeFEAdr0D

Offset Address: E3-E0h

Bit	Description	Mnemonic
31:24	Reserved	
23:0	Write Register at ParaType FEh with SubAddress 0Eh	HRPTypeFEAdr0E

Offset Address: E7-E4h

Bit	Description	Mnemonic
31:24	Reserved	
23:0	Write Register at ParaType FEh with SubAddress 0Fh	HRPTypeFEAdr0F

Offset Address: EB-E8h

Bit	Description	Mnemonic
31:24	Reserved	
23:0	Write Register at ParaType FEh with SubAddress 10h	HRPTypeFEAdr10

Offset Address: EF-ECh

Bit	Description	Mnemonic
31:24	Reserved	
23:0	Write Register at ParaType FEh with SubAddress 20h	HRPTypeFEAdr20

Definition of Parameter

Command and Primitive Vertex Data (HParaType = 00h)

- If Parameter is used for Command and Vertex Data Programming, the setting of HParaOS is ignored.
- The HCmdA must be the last programmed command register before any programming of primitive vertex data.
- The word with light color is not published. (No Publish)

Command

HParaType = 00h

Command Register A (HCmdA)

Bit	Description	Mnemonic
31:25	**Command Header. Must be '1110 111'**	**HCmdHeader**
24:22	**Reserved**	
21	**Vertex Cycle Update** 0: Render primitive as the original setting of the HVCycle 1: Render primitive as the new setting of the HVCycle This Register is only for Full-Vertex(3-3-3…cycle) Triangle rendering. We can insert a Command A to update the setting of HVCycle by setting this register in a primitive list. Thus we can use the vertexes of previous primitive in current primitive flexibly even in a full-cycle primitive list.	**HVCycleUpd**
20	**Reserved**	
19:16	**Primitive Type** 0000: Point Rendering 0001: Line Rendering 0010: Triangle Rendering 0011: Rectangle	**HPMType**
15:13	**Edge Flag** 000: Do not do antialiasing 1xx: Do antialiasing on Edge(a,b) x1x: Do antialiasing on Edge(b,c) xx1: Do antialiasing on Edge(c,a) Where we assume the vertex transmission sequence of a triangle is a, b, then c.	**HEFlag**
12:10	**Shading Setting** 000: Solid Shading 001: Flat Shading Via Vertex a 010: Flat Shading Via Vertex b 011: Flat Shading Via Vertex c 100: Gouraud Shading 101: (Advance) Phone Shading 110: (Advance) AI Shading 111: Reserved Where we assume the vertex transmission sequence of a triangle is a, b, then c.	**HShading**
9	**Primitive Invalid** 0: Primitive is Valid 1: Primitive Is Invalid	**HPMValidN**
8	**Primitive List End** 0: The definition is not true 1: The input primitive is the last primitive input of a primitive list.	**HPLEND**

7:0	**Vertex Cycle** 0000 0000: Full Vertex Cycle. 1. For Triangle Rendering, this is the 3 vertexes cycle 2. For Line Rendering, this is the 2 vertexes cycle 01xx xxxx: Automatic Fast Primitive Vertex Cycle 3. For Triangle Rendering this is a fast way to render 3111 Mode 4. For Line Rendering, this is a fast way to render 2111 Mode 5. The first or odd single vertex cycle will use the setting of D[6:0] 6. The second or even single vertex cycle will use the setting of H2nd1VT 10xx xxxx: Reserved 11xx xxxx: One Vertex Cycle The setting of one vertex triangle or line is as follow: D[5:4] Setting of Vertex a. This setting is used for both triangle and line rendering 00: Vertex a is a new input 01: The Vertex a will be replaced by previous Vertex a 10: The Vertex a will be replaced by previous Vertex b 11: The Vertex a will be replaced by previous Vertex c D[3:2] Setting of Vertex b. This setting is used for both triangle and line rendering 00: Vertex b is a new input 01: The Vertex b will be replaced by previous Vertex a 10: The Vertex b will be replaced by previous Vertex b 11: The Vertex b will be replaced by previous Vertex c D[1:0] Setting of Vertex c. This setting is only used for triangle rendering 00: Vertex c is a new input 01: The Vertex c will be replaced by previous Vertex a 10: The Vertex b will be replaced by previous Vertex b 11: The Vertex c will be replaced by previous Vertex c	**HVCycle**

Note for Driver [19:16]:
1. For this kind of primitive, only “rectangle list” is available. The stipple and fan can not adopt for rectangle.
2. Back face culling must be disabled.
3. Z bias per primitive is not available
4. No wrap correction
5. Up-left corner: vertex A Up-right corner: vertex B Down-left corner: vertex C

HParaType = 00h

Command Register B (HCmdB)

Bit	Description	Mnemonic
31:25	**Command ID 1. Must be '1110 110'**	**HCmdHeader**
24:17	**Reserved**	
16	**Line Pattern Reset** 0: No Line Pattern Reset When we draw the first pixel of a line, we do not always reference the first line pattern bit. Instead, we use the following line pattern bit after the last used linepattern bit of the previous line. 1: Reset Line Pattern When we draw the first pixel of a line, we always reference the first line pattern bit.	**HLPrst**
15	**Last Pixel Control in Line Drawing** 0: Do not draw the last pixel of the input line 1: Draw the last pixel of the input line	**HLLastP**
14:7	**Vertex Parameter Mask** D[14]: X parameter mask 0: Primitive Vertex Parameter does not have X 1: Primitive Vertex Parameter has X D[13]: Y parameter mask 0: Primitive Vertex Parameter does not have Y 1: Primitive Vertex Parameter has Y D[12]: Z parameter mask 0: Primitive Vertex Parameter does not have Z 1: Primitive Vertex Parameter has Z D[11]: W parameter mask 0: Primitive Vertex Parameter does not have W 1: Primitive Vertex Parameter has W D[10]: Cd parameter mask 0: Primitive Vertex Parameter does not have Diffuse Color, ARGB 1: Primitive Vertex Parameter has Diffuse Color, ARGB D[9]: Cs parameter mask 0: Primitive Vertex Parameter does not have Specula Color, SR SG SB, and Fog Factor 1: Primitive Vertex Parameter has Specula Color, SR SG SB, and Fog Factor D[8]: S parameter mask 0: Primitive Vertex Parameter does not have Texture Coordinate S 1: Primitive Vertex Parameter has Texture Coordinate S D[7]: T parameter mask 0: Primitive Vertex Parameter does not have Texture Coordinate T 1: Primitive Vertex Parameter has Texture Coordinate T	**HVPMSK**
6	**Back Face** 0: If the vertex input is in the order of clockwise, this is a back face primitive 1: If the vertex input is in the order of counter clockwise, this is a back face primitive	**HBFace**
5:0	**The Setting of Second or Even One-vertex Triangle** The setting is the same as in HVCycle[5:0]	**H2nd1VT**

HParaType = 00h

Vertex Data

UniChrome Pro II 3D GFX supports maximum 10 32-bit data in a vertex. They are: X, Y, Z, W, Cd, Cs, S0, T0, S1, T1. The programming sequence is fixed as previous writing order. If the command is sent via AGP bus, one of the X, Y, Z, or W must be programmed in a vertex. There is no such limitation if command is sent via PCI bus. To inform HW about which vertex parameter will be programmed is set via Command Register B (HCmdB) [14:7].

Attribute Other Than Texture (HParaType = 01h)

(Using FFh as sub-address is prohibited)

HParaType = 01h

Z Setting

Bit [31:24] Sub-Address	Bit	Description	Mnemonic
01h	23	**Force 1 Pipe Instead of 2 Pipes** 0: 2 Pipes 1: 1 Pipe	**HenForce1P**
	22	**Reserved**	
	21	**Enable Environment Map Texture** 0: Disable 1: Enable (Do Environment Map if HenTXMP=1)	**HenTXEnvMap**
	20:18	**Reserved**	
	17	**Enable BackFace Culling** 0: Disable 1: Enable	**HenBFCull**
	16	**Enable Color Write** 0: Disable 1: Enable	**HenCW**
	15	**Enable Anti-Aliasing** 0: Disable 1: Enable	**HenAA**
	14	**Enable Stencil Test** 0: Disable 1: Enable	**HenST**
	13	**Enable Z Test** 0: Disable 1: Enable	**HenZT**
	12	**Enable Z Write** 0: Disable 1: Enable	**HenZW**
	11	**Enable Alpha Test** 0: Disable 1: Enable	**HenAT**
	10	**Enable Alpha Write** 0: Disable 1: Enable	**HenAW**
	9	**Enable Stipple Pattern** 0: Disable 1: Enable	**HenSP**
	8	**Enable Line Pattern** 0: Disable 1: Enable	**HenLP**
	7	**Enable Texture Cache** 0: Disable & Clear Texture Cache 1: Enable	**HenTXCH**
	6	**Enable Texture Mapping** 0: Disable 1: Enable	**HenTXMP**
	5	**Enable Texture Perspective Correction** 0: Disable 1: Enable	**HenTXPP**
	4	**Enable Texture Transparency** 0: Disable 1: Enable	**HenTXTR**
	3	**Enable Specula Color** 0: Disable 1: Enable	**HenCS**
	2	**Enable Fog** 0: Disable 1: Enable	**HenFOG**
	1	**Enable Alpha Blending** 0: Disable 1: Enable	**HenABL**
	0	**Enable Dither** 0: Disable 1: Enable	**HenDT**
10h	23:0	**Lower 3 Bytes of ZW Buffer Base Address** This is A23 to A0.	**HZWBBasL**
11h	23:8	**Reserved**	
	7:0	**Highest Byte of ZW Buffer Base Address** This is A31 to A24.	**HZWBBasH**
12h	23	**ZW Buffer Type** 0: ZW buffer stores Z value 1: ZW buffer stores W value	**HZWBType**
	22	**Z Bias Write Back Setting** 0: Write original Z to Z buffer 1: Write biased Z to Z buffer	**HZBiasedWB**
	21	**Force the Z Value from 1.0 to 1.0- (from 1.00000000h to 0.FFFFFFFFh)** 0: Keep the original 1.0 1: Force to 1.0- whenever Z equal to 1.0	**HZONEasFF**
	20	**Clamp the Z Value is over 1.0 to 1.0- (from 1.xxxxxxxxh to 0.FFFFFFFFh)** 0: Keep the original value over 1.0 1: Clamp to 1.0- whenever Z is over 1.0	**HZOONEasFF**
	19:18	**Reserved**	

	17:16	**ZW Buffer Format** For Z Buffer 00: 16-bit fix point format, 0.0 ≤ Z < 1.0 01: Reserved 10: 32-bit fix point format, 0.0 ≤ Z < 1.0 11: 24-bit fix point format Z, 0.0 ≤ Z < 1.0, and Stencil Z is located in D[31:8], Stencil is located in D[7:0] For W Buffer 00: 16-bit floating point format: [4].12 If the 4 exponential bits is x, it represents 2^0. Where x is programmable via the setting of HWBEBias. The maximum exponential is 15 and minimum is 0. Any value outside this range will be clamped to 15 or 0. 01: Reserved 10: 32-bit floating point format: s[8].23 Since W is always positive, the sign bit is no use. However, the storage is still keep as IEEE single precision floating point format. 11: 24-bit floating point format W and 8-bit Stencil 24-bit floating point format of W is [5].19 If the 5 exponential bits is x, it represent 2^0. Where x is programmable via the setting of HWBEBias. The maximum exponential is 63 and minimum is 0. Any value outside this range will be clamped to 63 or 0. W located in D[31:8], Stencil located in D[7:0]	**HZWBFM**
	15:14	**ZW Buffer Location** 00: ZW Buffer is located in Local Memory 01: ZW Buffer is located in System Memory 1x: Reserved	**HZWBLoc**
	13:0	**ZW Buffer Pitch**	**HZWBPit**
13h	23:0	**Lower 3 Bytes of Z Bias**	**HZBiasL**
14h	23:16	**Bias Scale With 32-bit Floating Format**	**HZBiasScaleH**
	15:8	**Reserved**	
	7:0	**Highest Byte of Z Bias** SEZbias = max(Zdx, Zdy) * HZBiasScale + HZBias	**HZBiasH**
15h	23:19	**Reserved**	
	18:16	**ZW Test Mode** 000: Z or W Test Never Pass 001: Z or W Test Pass if Znew < Zdst 010: Z or W Test Pass if Znew = Zdst 011: Z or W Test Pass if Znew ≤ Zdst 100: Z or W Test Pass if Znew > Zdst 101: Z or W Test Pass if Znew ≠ Zdst 110: Z or W Test Pass if Znew ≥ Zdst 111: Z or W Test Always Pass Where Znew is the calculated Z value and Zdst is the Z stored in the Z buffer.	**HZWTMD**
	15	**Reserved**	
	14:8	**Exponential Bias for 16 or 24 bpp W Buffer Format** In 16-bpp, D[11:8] represents the exponential value for 2^0. In 24-bpp, D[12:8] represents the exponential value for 2^0. Currently, D[14:13] is reserved	**HWBEBias**
	7:0	**Z Normalization Factor** We define that Z can be divided by a value of power of 2. Thus, it allows the input Z free from the constrain of Z < 1. Z Normalization is $Z = Zin / 2^{HZNF}$	**HZNF**
16h	23:0	**Lower 3 Bytes of ZW Clear Data**	**HZWCDL**
17h	23:16	**Total Amount of ZWC Tag Bit Used**	**HZWCTAGnum**
	15:8	**Reserved**	
	7:0	**Highest Byte of ZW Clear Data**	**HZWCDH**
18h	23:0	**Z Bias Scale With 32-bit Floating Format**	**HZBiasScaleL**
19h	23:0	**Low 23 Bits of Low Boundary to Clamp the Z Bias**	**HZBiasLClampL**
20h	23:0	**Low 23 Bits of High Boundary to Clamp the Z Bias**	**HZBiasHClampL**
21h	23:20	**Reserved**	
	19:10	**High 10 Bits of High Boundary to Clamp the Z Bias**	**HZBiasHClampH**
	9:0	**High 10 Bits of Low Boundary to Clamp the Z Bias**	**HZBiasLClampH**

HParaType = 01h

Stencil Setting

Bit [31:24] Sub-Address	Bit	Description	Mnemonic
23h	23:16	**Stencil Test Reference Value** A positive 8-bit fix point number with range from 0 to 255. We will use this value for Stencil Test: A comparison between Stencil and HSTREF.	**HSTREF**
	15:8	**Stencil Test Operation Mask** The usage is a comparison between (Stencil & HSTOPMSK) and (HSTREF & HSTMSK)	**HSTOPMSK**
	7:0	**Stencil Buffer Bit Mask** If a bit = 0, the relative bit in the stencil buffer cannot be changed. Otherwise, it can be changed.	**HSTBMSK**
24h	23:19	**Reserved**	
	18:16	**Stencil Test Mode** 000: Stencil Test Never Pass 001: Stencil Test Pass if (HSTREF & HSTOPMSK) < (Stencil & HSTOPMSK) 010: Stencil Test Pass if (HSTREF & HSTOPMSK) = (Stencil & HSTOPMSK) 011: Stencil Test Pass if (HSTREF & HSTOPMSK) ≤ (Stencil & HSTOPMSK) 100: Stencil Test Pass if (HSTREF & HSTOPMSK) > (Stencil & HSTOPMSK) 101: Stencil Test Pass if (HSTREF & HSTOPMSK) ≠ (Stencil & HSTOPMSK) 110: Stencil Test Pass if (HSTREF & HSTOPMSK) ≥ (Stencil & HSTOPMSK) 111: Stencil Test Always Pass	**HSTMD**
	15:9	**Reserved**	
	8:6	**Stencil Operation for Stencil Test Fail** 000: KEEP 001: ZERO 010: REPLACE 011: INCRSAT 100: DECRSAT 101: INVERT 110: INCR 111: DECR	**HSTOPSF**
	5:3	**Stencil Operation for Stencil Test Pass and Z Test Fail** 000: KEEP 001: ZERO 010: REPLACE 011: INCRSAT 100: DECRSAT 101: INVERT 110: INCR 111: DECR	**HSTOPSPZF**
	2:0	**Stencil Operation for Stencil Test Pass and Z Test Pass** 000: KEEP 001: ZERO 010: REPLACE 011: INCRSAT 100: DECRSAT 101: INVERT 110: INCR 111: DECR	**HSTOPSPZP**

HParaType = 01h

Setting for Z-Dirty Check Function

Bit [31:24] Sub-Address	Bit	Description	Mnemonic
28h	23	**Reset the Z-Dirty Bits** 0: Normal 1: Reset	**HenZDRST**
	22:13	**Reserved**	
	12:8	**The Number of Pixels per Z-dirty Bit in Y-direction** 01100: 16 =1x16 11011: 24 = 3x8 01101: 32 = 1x32 01110: 64 = 1x64 Others: Reserved	**HZDYNum**
	7:6	**Reserved**	
	5:0	**The Number of Pixels per Z-dirty Bit in X-direction** 101010: 20 = 5x4 001101: 32 = 1x32 101011: 40 = 5x8 001110: 64 = 1x64 Others: Reserved	**HZDXNum**

HParaType = 01h

Alpha Setting

Bit [31:24] Sub-Address	Bit	Description	Mnemonic
33h	23:11	**Reserved**	
	10:8	**Alpha Test Mode** 000: Alpha Test Never Pass 001: Alpha Test Pass if Anew < HATREF 010: Alpha Test Pass if Anew = HATREF 011:A lpha Test Pass if Anew ≤ HATREF 100: Alpha Test Pass if Anew > HATREF 101: Alpha Test Pass if Anew ≠ HATREF 110: Alpha Test Pass if Anew ≥ HATREF 111: Alpha Test Always Pass	**HATMD**
	7:0	**Alpha Test Reference Value** Range from 0 to 255.	**HATREF**

34h		Alpha Blending Equation of RGB: Equation of RGB:
		Equation of RGB:
		If (AB_FCa = FFh)
		CA_Temp = AB_Ca
		Else
		CA_temp = (AB_Ca * AB_FCa)
		
		If (AB_FCb = FFh)
		CB_temp = AB_Cb
		Else
		CB_temp = (AB_Cb * AB_FCb)
		
		Cout = ((CA_temp) AB_Cop (CB_temp))	

	23:17	**Reserved**	
	16	**RGB Saturation Control of Alpha Blending Calculation** 0: Cout will be clamp to 0.0 ~ 1.0 1: Cout will not be clamp to 0.0 ~ 1.0	**HABLCsat**
	15:10	**Ca of Alpha Blending Equation** **HABLCa[4:3]** / **R of AB_Ca** / **G of AB_Ca** / **B of AB_Ca** **00** Reserved / Reserved / Reserved **01** Reserved / Reserved / Reserved **10** Reserved / Reserved / Reserved **11** Reserved / Reserved / Reserved **HABLCa[3:0]** / **R_of_OPCa** / **G_of_OPCa** / **B_of_OPCa** **0001** Rsrc / Gsrc / Bsrc **0001** Rdst / Gdst / Bdst **0010** Reserved / Reserved / Reserved **0011** Reserved / Reserved / Reserved **0100** Reserved / Reserved / Reserved **0101** R of Rx38h / G of Rx38h / B of Rx38h **0110** Min (Rsrc, Rdst) / Min (Gsrc, Gdst) / Min (Bsrc, Bdst) **0111** Max (Rsrc, Rdst) / Max (Gsrc, Gdst) / Max (Bsrc, Bdst) **1xxx** Reserved / Reserved / Reserved	**HABLCa**
	9:4	**FCa of Alpha Blending Equation** **HABLFCa[5:4]** / **R of AB_Fca** / **G of AB_FCa** / **B of AB_FCa** **00** R_of_OPFCa / G_of_OPFCa / B_of_OPFCa **01** Inv (R_of_OPFCa) / Inv (G_of_OPFCa) / Inv (B_of_OPFCa) **10** Reserved / Reserved / Reserved **11** Reserved / Reserved / Reserved **HABLFCa[3:0]** / **R_of_OPFCa** / **G_of_OPFCa** / **B_of_OPFCa** **0000** Rsrc / Gsrc / Bsrc **0001** Rdst / Gdst / Bdst **0010** Asrc / Asrc / Asrc **0011** Adst / Adst / Adst **0100** Reserved / Reserved / Reserved **0101** R of Rx39h / G of Rx39h / B of Rx39h **0110** Reserved / Reserved / Reserved **0111** Reserved / Reserved / Reserved **1000** Min (Asrc, 1-Adst) / Min (Asrc, 1-Adst) / Min (Asrc, 1-Adst) **1111-1001** Reserved / Reserved / Reserved	**HABLFCa**
	3:0	**Reserved**	

Bit [31:24] Sub-Address	Bit	Description	Mnemonic
35h	23:15	**Reserved**	
	14	**Cop of Alpha Blending Equation** HABLCop Cop 0: + 1: -	**HABLCop**
	13:8	**Cb of Alpha Blending Equation** **HABLCb[5:4] / R of AB_Cb / G of AB_Cb / B of AB_Cb** **00** Reserved Reserved Reserved **01** Reserved Reserved Reserved **10** Reserved Reserved Reserved **11** Reserved Reserved Reserved **HABLCb[3:0] / R_of_OPCb / G_of_OPCb / B_of_OPCb** **0000** Rsrc Gsrc Bsrc **0001** Rdst Gdst Bdst **0010** Reserved Reserved Reserved **0011** Reserved Reserved Reserved **0100** Reserved Reserved Reserved **0101** R of Rx3Bh G of Rx3Bh B of Rx3Bh **0110** Reserved Reserved Reserved **0111** Reserved Reserved Reserved **1xxx** Reserved Reserved Reserved	**HABLCb**
	7:2	**FCb of Alpha Blending Equation** **HAB_FCb[5:4] / R of AB_FCb / G of AB_FCb / B of AB_FCb** **00** R_of_OPFCb G_of_OPFCb B_of_OPFCb **01** Inv (R_of_OPFCb) Inv (G_of_OPFCb) Inv (B_of_OPFCb) **10** Reserved Reserved Reserved **11** Reserved Reserved Reserved **HAB_FCb[3:0] / R_of_OPFCb / G_of_OPFCb / B_of_OPFCb** **0000** Rsrc Gsrc Bsrc **0001** Rdst Gdst Bdst **0010** Asrc Asrc Asrc **0011** Adst Adst Adst **0100** Reserved Reserved Reserved **0101** R of Rx3Ch G of Rx3Ch B of Rx3Ch **0110** Reserved Reserved Reserved **0111** Reserved Reserved Reserved **1000** Min (Asrc, 1-Adst) Min (Asrc, 1-Adst) Min (Asrc, 1-Adst) **1111-1001** Reserved Reserved Reserved	**HABLFCb**
	1:0	**Reserved**	**HABLCshift**

36h		**Equation of A:**
		
		If (AB_FAa = FFh)
		AA_Temp = AB_Aa
		Else
		AA_temp = (AB_Aa * AB_FAa)
		
		If (AB_FAb = FFh)
		AB_temp = AB_Ab
		Else
		AB_temp = (AB_Ab * AB_FAb)
		
		Aout = ((AA_temp) AB_Cop (AB_temp))
		Equation of Dot Product is Reserved	

	23:17	**Reserved**	
	16	**Alpha Saturation Control of Alpha Blending Calculation** 0: Aout will be clamped to 0.0 ~ 1.0 1: Aout will not be clamped to 0.0 ~ 1.0	**HABLAsat**

	15:10	**Aa of Alpha Blending Equation** **HABLAa[5:4]** 00 – 11: Reserved **HABLAa[3:0]** 0000: 0 0001: Asrc 0010: Adst 0011 – 0100: Reserved 0101: Min (Asrc, Adst) 0110: Reserved 0111: Max (Asrc, Adst) 1000: HABLRAa 1111 – 1001: Reserved	**HABLAa**
	9:4	**FAa of Alpha Blending Equation** **HABLFAa[5:4]** 00: OPFAa 01: Inv (OPFAa) 1x: Reserved **HABLFAa[3:0]** 0000: 0 0001: Asrc 0010: Adst 0011 – 0111: Reserved 1000: Min (Asrc, 1-Adst) 1001: HABLRFAa 1111 – 1101: Reserved	**HABLFAa**
	3:0	**Reserved**	
37h	23:15	**Reserved**	
	14	**Aop of Alpha Blending Equation** **HAB_Aop** **AB_Aop** 0 + 1 -	**HABLAop**
	13:8	**Ab of Alpha Blending Equation**	**HABLAb**
	7:2	**FAb of Alpha Blending Equation** **HABLFAb[3:0]** 0000: 0 0001: Asrc 0010: Adst 0011 - 0111: Reserved 1000: Min (Asrc, 1-Adst) 1001: HABLRFAb 1111 – 1010: Reserved	**HABLFAb**
	1:0	**Reserved**	
38h	23:0	**Constant Register of Ca** D[23:16]: This is a 8-bit integer number in 2's complement format range from -128 to 127. D[15:8]: This is a 8-bit integer number in 2's complement format range from -128 to 127 D[7:0]: This is a 8-bit integer number in 2's complement format range from -128 to 127.	**HABLRCa**
39h	23:0	**Constant Register of Fca** D[23:16]: This is a 8-bit integer number in 2's complement format range from -128 to 127. D[15:8]: This is a 8-bit integer number in 2's complement format range from -128 to 127. D[7:0]: This is a 8-bit integer number in 2's complement format range from -128 to 127.	**HABLRFCa**

3Ah	23:0	**Constant Register of Cbias** D[23:16]: This is a 8-bit integer number in 2's complement format range from -128 to 127. D[15:8]: This is a 8-bit integer number in 2's complement format range from -128 to 127. D[7:0]: This is a 8-bit integer number in 2's complement format range from -128 to 127.	**HABLRCbias**
3Bh	23:0	**Constant Register of Cb** D[23:16]: This is a 8-bit integer number in 2's complement format range from -128 to 127. D[15:8]: This is a 8-bit integer number in 2's complement format range from -128 to 127. D[7:0]: This is a 8-bit integer number in 2's complement format range from -128 to 127.	**HABLRCb**
3Ch	23:0	**Constant Register of FCb** D[23:16]: This is a 8-bit integer number in 2's complement format range from -128 to 127. D[15:8]: This is a 8-bit integer number in 2's complement format range from -128 to 127. D[7:0]: This is a 8-bit integer number in 2's complement format range from -128 to 127.	**HABLRFCb**
3Dh	23:16	**Constant Register of Aa** This is a 8-bit integer number in 2's complement format range from -128 to 127.	**HABLRAa**
	15:8	**Constant Register of Faa** This is a 8-bit integer number in 2's complement format range from -128 to 127..	**HABLRFAa**
	7:0	**Constant Register of Abias** This is a 8-bit integer number in 2's complement format range from -128 to 127.	**HABLRAbias**
3Eh	23:16	**Reserved**	
	15:8	**Constant Register of Ab** This is a 8-bit integer number in 2's complement format range from -128 to 127.	**HABLRAb**
	7:0	**Constant Register of Fab** This is a 8-bit integer number in 2's complement format range from -128 to 127.	**HABLRFAb**

HParaType = 01h

Destination Setting

Bit [31:24] Sub-Address	Bit	Description	Mnemonic
40h	23:0	**Lower 3 Bytes of Destination Buffer Base Address** This is A23 to A0.	**HDBBasL**
41h	23:8	**Reserved**	
	7:0	**Highest Byte of Destination Buffer Base Address** This is A31 to A24.	**HDBBasH**
42h	23	**Reserved**	
	22:16	**Destination Buffer Format** D[22]: Deal RGB565 as RGB666 or BGR565 as BGR666 0: Normal 1: Extend R4R3R2R1R0 to R4R3R2R1R0G0 Extend B4B3B2B1B0 to B4B3B2B1B0G0 D[21]: Extend 16bpp to 24bpp by filling zero or high color bit 0: Fill high color bit For example of RGB565: R4R3R2R1R0R4R3R2 G5G4G3G2G1G0G5G4 B4B3B2B1B0B4B3B2 1: Fill zero For example of RGB565: R4R3R2R1R0 000 G5G4G3G2G1G0 00 B4B3B2B1B0 000 D[20]: Deal RGB565 as RGB555 or BGR565 as BGR555 0: Normal 1: Ignore G0 bit To sum up D[22:20] 000: R4R3R2R1R0R4R3R2 G5G4G3G2G1G0G5G4 B4B3B2B1B0B4B3B2 001: R4R3R2R1R0R4R3R2 G5G4G3G2G1G5G4G3 B4B3B2B1B0B4B3B2 100: R4R3R2R1R0G0R4R3 G5G4G3G2G1G0G5G4 B4B3B2B1B0G0B4B3 010: R4R3R2R1R0 000 G5G4G3G2G1G0 00 B4B3B2B1B0 000 011: R4R3R2R1R0 000 G5G4G3G2G1 000 B4B3B2B1B0 000 110: R4R3R2R1R0G0 00 G5G4G3G2G1G0 00 B4B3B2B1B0G0 00 1x1: Never Happen D[19] 0: ARGB 16 bpp Format 1: ARGB 32 bpp Format D[18:16] For ARGB16_bpp Format 000: RGB555 (Bit[14:10] = R, Bit[9:5] = G, Bit[4:0] = B) 001: RGB565 (Bit[15:11] = R, Bit[10:5] = G, Bit[4:0] = B) 010: ARGB4444 (Bit[15:12] = A, Bit[11:8] = R, Bit[7:4] = G, Bit[3:0] = B) 011: ARGB1555 (Bit[15] = A, Bit[14:10] = R, Bit[9:5] = G, Bit[4:0] = B) 100: BGR555 (Bit[14:10] = B, Bit[9:5] = G, Bit[4:0] = R) 101: BGR565 (Bit[15:11] = B, Bit[10:5] = G, Bit[4:0] = R) 110: ABGR4444 (Bit[15:12] = A, Bit[11:8] = B, Bit[7:4] = G, Bit[3:0] = R) 111: ABGR1555 (Bit[15] = A, Bit[14:10] = B, Bit[9:5] = G, Bit[4:0] = R) For ARGB32_bpp Format 000: ARGB0888 (Bit[23:16] = R, Bit[15:8] = G, Bit[7:0] = B) 001: ARGB8888 (Bit[31:24] = A, Bit[23:16] = R, Bit[15:8] = G, Bit[7:0] = B) 010: ABGR0888 (Bit[23:16] = B, Bit[15:8] = G, Bit[7:0] = R) 011: ABGR8888 (Bit[31:24] = A, Bit[23:16] = B, Bit[15:8] = G, Bit[7:0] = R) 10x: Reserved 110: Reserved 111: Video Texture Package mode(YUY2) (Bit[31:24] = V or Cr, Bit[23:16] = Y1, Bit[15:8] = U or Cb, Bit[7:0] = Y0) For reading color, **consider the 8-bit Y as positive 8-bit R, 8-bit U as positive 8-bit G, and 8-bit V as positive 8-bit B**. For writing color, the adjacent 2 pixel are combinen into 32-bit and share same 8-bit U and V. Consider the even pixel with R0, G0 & B0(dithered 8-bit color), and the next odd pixel with R1, G1& B1(dithered 8-bit color) the packed result is {(B0 + B1)/2, R1, (G0+G1)/2, R0}. Note the (B0+B1)/2 and (R0+R1)/2 are the result of rounding	**HDBFM**

	15:14	**Destination Buffer Location** 00: Destination Buffer is located in the Local Memory 01: Destination Buffer is located in System Memory 1x: Reserved	**HDBLoc**
	13:0	**Destination Buffer Pitch**	**HDBPit**
43h	23:0	**Lower 3 Bytes of Frame Buffer Bit Mask** 0: The relative data bit will remain the same value in Frame Buffer. 1: The relative data bit will be updated by a new calculated number. D[23:16] = D[7:0] for 16-bpp FB = D[23:16] for 32-bpp FB D[15:0] = No use for 16-bpp FB = D[15:0] for 32-bpp FB	**HFBBMSKL**
44h	23	**Y Inverse for Dither** 0: Not inverse 1: Inverse	**HDTYInverse**
	22:21	**Y Bias for Dither**	**HDTYBias**
	20	**X Inverse for Dither** 0: Not inverse 1: Inverse	**HDTXInverse**
	19:18	**X Bias for Dither**	**HDTXBias**
	17	**Reserved**	
	16	**Dither Mode** 0: Dither Table 1: Rounding	**HDTMode**
	15:12	**Reserved**	
	11:8	**Raster Operation** 0000: BLACK 0 0001: NOT_MERGE_PEN DPon 0010: MASK_NOT_PEN DPna 0011: NOT_COPY_PEN Pn 0100: MASK_PEN_NOT PDna 0101: NOT Dn 0110: XOR_PEN DPx 0111: NOT_MASK_PEN DPan 1000: MASK_PEN DPa 1001: NOT_XOR_PEN DPxn 1010: NOP D 1011: MERGE_NOT_PEN DPno 1100: COPY_PEN P 1101: MERGE_PEN_NOT PDno 1110: MERGE_PEN DPo 1111: WHITE 1	**HROP**
	7:0	**Highest Byte of Frame Buffer Bit Mask** = D[15:8] for 16-bpp FB = D[15:8] for 16-bpp FB	**HFBBMSKH**

HParaType = 01h

Fog Setting

Bit [31:24] Sub-Address	Bit	Description	Mnemonic
50h	23:5	**Reserved**	
	4	**Linear Fog Calculation Factor Setting** 0: Use W to calculate Linear Fog 1: Use Z to calculate Linear Fog	**HFogLF**
	3	**Fog Equation** Fog Equation 0: Cout = f * (Cin + Csepc) + (1-f) * HCFog Fog Equation 1: Cout = (1-f) * (Cin + Cspec) + f * HCFog 0: Use Fog Equation 0 1: Use Fog Equation 1	**HFogEq**
	2:0	**Fog Mode** 000: Local Fog 001: Reserved Global Fog 010: Linear Fog 011: Reserved 1xx: Non-linear Fog (Using Fog Table) 100: Exponential Fog 101: Exponential_2 Fog 11x: Reserved	**HFogMD**
51h	23:16	**Lower 3 Bytes of Fog Color Register** R of HCFogCL	**FCFogR**
	15:8	**Lower 3 Bytes of Fog Color Register** G of HCFogCL	**FCFogG**
	7:0	**Lower 3 Bytes of Fog Color Register** B of HCFogCL	**FCFogB**
52h	23:8	**Reserved**	
	7:0	**Alpha of Fog Color**	**HCFogA**
53h	23:0	**Lower 3 Bytes of Fog Start** When Z is used to calculate fog factor, the format of HFogSt is fixed-point .32. When W is used to calculate fog factor, the format of HFogSt is floating-point [8].7.	**HFogStL**
54h	23:8	**Reserved**	
	7:0	**Highest Byte of Fog Start**	**HFogStH**
55h	23:4	**Reserved**	
	3:0	**Mantissa part of the One Over (Fog End - Fog Start)** **Note that not contain leading one.**	**HFogOOdMF**
56h	23:8	**Reserved**	
	7:0	**Exponential part of the One Over (Fog End - Fog Start) and as IEEE's floating presentation. The value of 1/(Fog End – Fog Start) is (1.HfogOOdMF[3:0] * 2^(HfogOOdEF – 127))**	**HFogOOdEF**
57h	23:0	**Lower 3 Bytes of Fog End** When Z is used to calculate fog factor, the format of HFogSt is fixed-point .32. When W is used to calculate fog factor, the format of HFogSt is floating-point [8].7.	**HFogEndL**
58h	23:21	**Reserved**	
	20:8	**Fog Density with Positive Floating Format [8].5**	**HfogDenst**
	7:0	**Highest Byte of Fog End and only available when Z is used to calculate fog factor**	**HFogEndH**

HParaType = 01h

AGP Command Setting

Bit [31:24] Sub-Address	Bit	Description	Mnemonic
60h	23:0	**Lower 3 bytes of AGP Buffer Start Address** It is A[23:0] which A[1:0] is useless.	**HAGPBstL**
61h	23:0	**Lower 3 bytes of AGP Buffer End Address** It is A[23:0] which A[1:0] is useless.	**HAGPBendL**
62h	23	**Start to Fetch AGP Command Block on Next Clock** This is a trigger setting. Thus, whenever we program the value to 1, we do not have to program it back to 0. 0: Negative meaning from our definition 1: Start to Fetch AGP Command Block on Next Clock	**HAGPCMNT**
	22	**Clear AGP Command Error Flag** 0: The AGP Command Error Flag will not be cleared. 1: The AGP Command Error Flag will be cleared.	**HCmdErrClr**
	21:16	**Reserved**	
	15:8	**Highest Byte of AGP Buffer End Address. A[31:24]**	**HAGPBendH**
	7:0	**Highest Byte of AGP Buffer Start Address. A[31:24]**	**HAGPBstH**
63h	23:2	**Lower 3 Bytes of AGP Command Pause Address. A[23:2]**	**HAGPBpL**
	1:0	**ID of HAGPBp** 00: HAGPBp is the Pause Address of AGP Command Fetch. If AGP Command Fetcher wants to continuely fetch AGP Command again, he will start on the next address after HAGPBp. 01: HAGPBp is the End Address of a portion of AGP Command Block. When AGP Command Fetcher reach this address, he will start to fetch next AGP Command addressed by HAGPBst. No waiting or pause at this time. 10: HAGPBp is the AGP Command Stop Address. Whenever, AGP Command Fetcher reach this address, the AGP Command Fetching is finished. If we want to do another AGP Command Fetching, we have to set HAGPCMNT as 1. 11: Reserved	**HAGPBpID**
64h	23:8	**Reserved**	
	7:0	**Highest Byte of AGP Command Pause Address. A[31:24]**	**HAGPBpH**

HParaType = 01h
Miscellenous Setting

Bit [31:24] Sub-Address	Bit	Description	Mnemonic
70h	23	**Reserved**	
	22:12	**Top Clipping Value in the range from 0 to 2047**	**HClipT**
	11	**Reserved**	
	10:0	**Bottom Clipping Value in the range from 0 to 2047**	**HClipB**
71h	23	**Reserved**	
	22:12	**Left Clipping Value**	**HClipL**
	11	**Reserved**	
	10:0	**Right Clipping Value**	**HClipR**
72h	23:0	**Reserved**	
78h	23:16	**Reserved**	
	15:0	**Line Pattern** The Line Pattern bit is start from the LSB.	**HLP**
79h	23:16	**Reserved**	
	15:0	**Line Pattern Repeat Factor** This number denotes how many times that a line pattern bit will be used for several line pixels.	**HLPRF**
7Ah	23:16	**Lower 3 Bytes of Solid Shading Color** **R of Solid Shading Color**	**HSolidCL** **HsolidR**
	15:8	**Lower 3 Bytes of Solid Shading Color** **G of Solid Shading Color**	**HsolidG**
	7:0	**Lower 3 Bytes of Solid Shading Color** **B of Solid Shading Color**	**HsolidB**
7Bh	23	**Pixel Grid Center** 0: The pixel grid center is located in (x.5, x.5) of a 3D coordinates. 1: The pixel grid center is located in (x.0, x.0) of a 3D coordinates.	**HPixGC**
	22:8	**Reserved**	
	7:0	**Highest Byte of Solid Shading Color**	**HSolidCH**
7Ch	23:17	**Reserved**	
	16:12	**Stipple X Offset Value**	**HSPXOS**
	11:5	**Reserved**	
	4:0	**Stipple Y Offset Value** Therefore, the actually referenced stipple pattern bit is (5 LSB of (X + HSPXOS), 5 LSB of (Y + HSPYOS))	**HSPYOS**
7Dh	23:16	**Reserved**	
	15:0	**Vertex Count** This counter indicates the number of vertex in a input primitive list.	**HVertexCNT**

HParaType = 01h
SW Inspection

Bit [31:24] Sub-Address	Bit	Description	Mnemonic
AAh	23:16	**Reserved**	
	15:0	**Flag Number for SW Inspection**	**HCRFlagNum**

Attribute of Texture n (HParaType = 02h)

HparaSubType: 00h For Texture 0

Attribute of Texture n (HParaType = 02h)

HparaSubType: 01h For Texture 1

Using FFh as sub-address is prohibited

Bit [31:24] Sub-Address	Bit	Description	Mnemonic
00h	23:0	**Lower 3 Bytes of Level 0 Base Address.** This is A23 to A0. Lower 3 bytes of Y Buffer Base Address for Plannar mode (Y-Cb-Cr) Video Texture for Level 0. Lower 3 bytes of Y Buffer Base Address for Plannar mode (Y-Crb) Video Texture for Level 0.	**HTXnL0BasL**
01h	23:0	**Lower 3 Bytes of Level 1 Base Address.** This is A23 to A0. Lower 3 bytes of U Buffer Base Address for Plannar mode (Y-Cb-Cr) Video Texture for Level 0. Lower 3 bytes of Crb Buffer Base Address for Plannar mode (Y-Crb) Video Texture for Level 0.	**HTXnL1BasL**
02h	23:0	**Lower 3 Bytes of Level 2 Base Address.** This is A23 to A0. Lower 3 bytes of V Buffer Base Address for Plannar mode (Y-Cb-Cr) Video Texture for Level 0. Lower 3 bytes of Y Buffer Base Address for Plannar mode (Y-Crb) Video Texture for Level 1.	**HTXnL2BasL**
03h	23:0	**Lower 3 Bytes of Level 3 Base Address.** This is A23 to A0. Lower 3 bytes of Y Buffer Base Address for Plannar mode (Y-Cb-Cr) Video Texture for Level 1. Lower 3 bytes of Crb Buffer Base Address for Plannar mode (Y-Crb) Video Texture for Level 1.	**HTXnL3BasL**
04h	23:0	**Lower 3 Bytes of Level 4 Base Address.** This is A23 to A0. Lower 3 bytes of U Buffer Base Address for Plannar mode (Y-Cb-Cr) Video Texture for Level 1. Lower 3 bytes of Y Buffer Base Address for Plannar mode (Y-Crb) Video Texture for Level 2.	**HTXnL4BasL**
05h	23:0	**Lower 3 Bytes of Level 5 Base Address.** This is A23 to A0. Lower 3 bytes of V Buffer Base Address for Plannar mode (Y-Cb-Cr) Video Texture for Level 1. Lower 3 bytes of Crb Buffer Base Address for Plannar mode (Y-Crb) Video Texture for Level 2.	**HTXnL5BasL**
06h	23:0	**Lower 3 Bytes of Level 6 Base Address.** This is A23 to A0. Lower 3 bytes of Y Buffer Base Address for Plannar mode (Y-Cb-Cr) Video Texture for Level 2. Lower 3 bytes of Y Buffer Base Address for Plannar mode (Y-Crb) Video Texture for Level 3.	**HTXnL6BasL**
07h	23:0	**Lower 3 Bytes of Level 7 Base Address.** This is A23 to A0. Lower 3 bytes of U Buffer Base Address for Plannar mode (Y-Cb-Cr) Video Texture for Level 2. Lower 3 bytes of Crb Buffer Base Address for Plannar mode (Y-Crb) Video Texture for Level 3.	**HTXnL7BasL**
08h	23:0	**Lower 3 Bytes of Level 8 Base Address.** This is A23 to A0. Lower 3 bytes of V Buffer Base Address for Plannar mode (Y-Cb-Cr) Video Texture for Level 2. Lower 3 bytes of Y Buffer Base Address for Plannar mode (Y-Crb) Video Texture for Level 4.	**HTXnL8BasL**
09h	23:0	**Lower 3 Bytes of Level 9 Base Address.** This is A23 to A0. Lower 3 bytes of Crb Buffer Base Address for Plannar mode (Y-Crb) Video Texture for Level 4.	**HTXnL9BasL**
20h	23:16	**Highest Byte of Level 2 Base Address.** This is A31 to A24. Highest byte of V Buffer Base Address for Plannar mode (Y-Cb-Cr) Video Texture for Level 0. Highest byte of Y Buffer Base Address for Plannar mode (Y-Crb) Video Texture for Level 1.	**HTXnL2BasH**
	15:8	**Highest Byte of Level 1 Base Address.** This is A31 to A24. Highest byte of U Buffer Base Address for Plannar mode (Y-Cb-Cr) Video Texture for Level 0. Highest byte of Crb Buffer Base Address for Plannar mode (Y-Crb) Video Texture for Level 0.	**HTXnL1BasH**
	7:0	**Highest Byte of Level 0 Base Address.** This is A31 to A24. Highest byte of Y Buffer Base Address for Plannar mode (Y-Cb-Cr) Video Texture for Level 0. Highest byte of Y Buffer Base Address for Plannar mode (Y-Crb) Video Texture for Level 0	**HTXnL0BasH**
21h	23:16	**Highest Byte of Level 5 Base Address.** This is A31 to A24. Highest byte of V Buffer Base Address for Plannar mode (Y-Cb-Cr) Video Texture for Level 1. Highest byte of Crb Buffer Base Address for Plannar mode (Y-Crb) Video Texture for Level 2	**HTXnL5BasH**
	15:8	**Highest Byte of Level 4 Base Address.** This is A31 to A24. Highest byte of U Buffer Base Address for Plannar mode (Y-Cb-Cr) Video Texture for Level 1. Highest byte of Y Buffer Base Address for Plannar mode (Y-Crb) Video Texture for Level 2	**HTXnL4BasH**
	7:0	**Highest Byte of Level 3 Base Address.** This is A31 to A24. Highest byte of Y Buffer Base Address for Plannar mode (Y-Cb-Cr) Video Texture for Level 1 Highest byte of Crb Buffer Base Address for Plannar mode (Y-Crb) Video Texture for Level 1	**HTXnL3BasH**
22h	23:16	**Highest Byte of Level 8 Base Address.** This is A31 to A24. Highest byte of V Buffer Base Address for Plannar mode (Y-Cb-Cr) Video Texture for Level 2. Highest byte of Y Buffer Base Address for Plannar mode (Y-Crb) Video Texture for Level 4	**HTXnL8BasH**
	15:8	**Highest Byte of Level 7 Base Address.** This is A31 to A24. Highest byte of U Buffer Base Address for Plannar mode (Y-Cb-Cr) Video Texture for Level 2. Highest byte of Crb Buffer Base Address for Plannar mode (Y-Crb) Video Texture for Level 3	**HTXnL7BasH**

	7:0	**Highest Byte of Level 6 Base Address.** This is A31 to A24. Highest byte of Y Buffer Base Address for Plannar mode (Y-Cb-Cr) Video Texture for Level 2. Highest byte of Y Buffer Base Address for Plannar mode (Y-Crb) Video Texture for Level 3	**HTXnL6BasH**
23h	23:16	**Highest Byte of Level B Base Address**	**HTXnLBBasH**
	15:8	**Highest Byte of Level A Base Address**	**HTXnLABasH**
	7:0	**Highest Byte of Level 9 Base Address.** This is A31 to A24. Highest byte of Crb Buffer Base Address for Plannar mode (Y-Crb) Video Texture for Level 4	**HTXnL9BasH**
2Bh	23:20	**Exponential of Pitch of Texture Level 0 (in unit of byte)** 0000: Pitch = 1 byte 0001: Pitch = 2 bytes 0010: Pitch = 4 bytes 0011: Pitch = 8 bytes 0100: Pitch = 16 bytes 0101: Pitch = 32 bytes 0110: Pitch = 64 bytes 0111: Pitch = 128 bytes 1000: Pitch = 256 bytes 1001: Pitch = 512 bytes 1010: Pitch = 1024 bytes 1011: Pitch = 2048 bytes 1100: Pitch = 4096 bytes 1101: Pitch = 8192 bytes 111x: Reserved	**HTXnL0PITE**
	19	**Enable Using HTXnLmPit instead if HTXnLmWE to calculate the texture address**	**HTXnEnPit**
	18:14	**Reserved**	
	13:0	**Pitch of Texture Level 0 (in unit of byte)** Pitch of Y buffer for Plannar mode (Y-Cb-Cr) Video Texture for Level 0. Pitch of Y buffer for Plannar mode (Y-Crb) Video Texture for Level 0.	**HTXnL0PIT**
2Ch	23:20	**Exponential of Pitch of Texture Level 1 (in unit of byte)** The bit definitions are listed in HTXnL0PITE.	**HTXnL1PITE**
	19:14	**Reserved**	
	13:0	**Pitch of Texture Level 1 (in unit of byte)** Pitch of U buffer for Plannar mode (Y-Cb-Cr) Video Texture for Level 0. Pitch of Crb buffer for Plannar mode (Y-Crb) Video Texture for Level 0.	**HTXnL1PIT**
2Dh	23:20	**Exponential of Pitch of Texture Level 2 (in unit of byte)** The bit definitions are listed in HTXnL0PITE.	**HTXnL2PITE**
	19:14	**Reserved**	
	13:0	**Pitch of Texture Level 2 (in unit of byte)** Pitch of V buffer for Plannar mode (Y-Cb-Cr) Video Texture for Level 0. Pitch of Y buffer for Plannar mode (Y-Crb) Video Texture for Level 1.	**HTXnL2PIT**
2Eh	23:20	**Exponential of Pitch of Texture Level 3 (in unit of byte)** The bit definitions are listed in HTXnL0PITE.	**HTXnL3PITE**
	19:14	**Reserved**	
	13:0	**Pitch of Texture Level 3 (in unit of byte)** Pitch of Y buffer for Plannar mode (Y-Cb-Cr) Video Texture for Level 1. Pitch of Crb buffer for Plannar mode (Y-Crb) Video Texture for Level 1.	**HTXnL3PIT**
2Fh	23:20	**Exponential of Pitch of Texture Level 4 (in unit of byte)** The bit definitions are listed in HTXnL0PITE.	**HTXnL4PITE**
	19:14	**Reserved**	
	13:0	**Pitch of Texture Level 4 (in unit of byte)** Pitch of U buffer for Plannar mode (Y-Cb-Cr) Video Texture for Level 1. Pitch of Y buffer for Plannar mode (Y-Crb) Video Texture for Level 2.	**HTXnL4PIT**

Bit [31:24] Sub-Address	Bit	Description	Mnemonic
30h	23:20	**Exponential of Pitch of Texture Level 5 (in unit of byte)** The bit definitions are listed in HTXnL0PITE.	**HTXnL5PITE**
	19:14	**Reserved**	
	13:0	**Pitch of Texture Level 5 (in unit of byte)** Pitch of V buffer for Plannar mode (Y-Cb-Cr) Video Texture for Level 1. Pitch of Crb buffer for Plannar mode (Y-Crb) Video Texture for Level 2.	**HTXnL5PIT**
31h	23:20	**Exponential of Pitch of Texture Level 6 (in unit of byte)** The bit definitions are listed in HTXnL0PITE.	**HTXnL6PITE**
	19:14	**Reserved**	
	13:0	**Pitch of Texture Level 6 (in unit of byte)** Pitch of Y buffer for Plannar mode (Y-Cb-Cr) Video Texture for Level 2. Pitch of Y buffer for Plannar mode (Y-Crb) Video Texture for Level 3.	**HTXnL6PIT**
32h	23:20	**Exponential of Pitch of Texture Level 7 (in unit of byte)** The bit definitions are listed in HTXnL0PITE.	**HTXnL7PITE**
	19:14	**Reserved**	
	13:0	**Pitch of Texture Level 7 (in unit of byte)** Pitch of U buffer for Plannar mode (Y-Cb-Cr) Video Texture for Level 2. Pitch of Crb buffer for Plannar mode (Y-Crb) Video Texture for Level 3.	**HTXnL7PIT**
33h	23:20	**Exponential of Pitch of Texture Level 8 (in unit of byte)** The bit definitions are listed in HTXnL0PITE.	**HTXnL8PITE**
	19:14	**Reserved**	
	13:0	**Pitch of Texture Level 8 (in unit of byte)** Pitch of V buffer for Plannar mode (Y-Cb-Cr) Video Texture for Level 2. Pitch of Y buffer for Plannar mode (Y-Crb) Video Texture for Level 4.	**HTXnL8PIT**
34h	23:20	**Exponential of Pitch of Texture Level 9 (in unit of byte)** The bit definitions are listed in HTXnL0PITE.	**HTXnL9PITE**
	19:14	**Reserved**	
	13:0	**Pitch of Texture Level 9 (in unit of byte)** Pitch of Crb buffer for Plannar mode (Y-Crb) Video Texture for Level 4.	**HTXnL9PIT**
35h	23:20	**Exponential of Pitch of Texture Level A**	**HTXnLAPITE**
	19:14	**Reserved**	
	13:0	**Pitch of Texture Level A (in unit of byte)**	**HTXnLAPIT**
36h	23:20	**Exponential of Pitch of Texture Level B**	**HTXnLBPITE**
	19:14	**Reserved**	**Reserved**
	13:0	**Pitch of Texture Level B (in unit of byte)**	**HTXnLBPIT**
4Bh	23:20	**Width Exponential of Texture Level 5 (range from 0 to 11)**	**HTXnL5WE**
	19:16	**Width Exponential of Texture Level 4 (range from 0 to 11)**	**HTXnL4WE**
	15:12	**Width Exponential of Texture Level 3 (range from 0 to 11)**	**HTXnL3WE**
	11:8	**Width Exponential of Texture Level 2 (range from 0 to 11)**	**HTXnL2WE**
	7:4	**Width Exponential of Texture Level 1 (range from 0 to 11)**	**HTXnL1WE**
	3:0	**Width Exponential of Texture Level 0 (range from 0 to 11)**	**HTXnL0WE**
4Ch	23:20	**Width Exponential of Texture Level B (range from 0 to 11)**	**HTXnLBWE**
	19:16	**Width Exponential of Texture Level A (range from 0 to 11)**	**HTXnLAWE**
	15:12	**Width Exponential of Texture Level 9 (range from 0 to 11)**	**HTXnL9WE**
	11:8	**Width Exponential of Texture Level 8 (range from 0 to 11)**	**HTXnL8WE**
	7:4	**Width Exponential of Texture Level 7 (range from 0 to 11)**	**HTXnL7WE**
	3:0	**Width Exponential of Texture Level 6 (range from 0 to 11)**	**HTXnL6WE**
51h	23:20	**Height Exponential of Texture Level 5**	**HTXnL5HE**
	19:16	**Height Exponential of Texture Level 4**	**HTXnL4HE**
	15:12	**Height Exponential of Texture Level 3**	**HTXnL3HE**
	11:8	**Height Exponential of Texture Level 2**	**HTXnL2HE**
	7:4	**Height Exponential of Texture Level 1**	**HTXnL1HE**
	3:0	**Height Exponential of Texture Level 0**	**HTXnL0HE**
52h	23:20	**Height Exponential of Texture Level B**	**HTXnLBHE**
	19:16	**Height Exponential of Texture Level A**	**HTXnLAHE**
	15:12	**Height Exponential of Texture Level 9**	**HTXnL9HE**
	11:8	**Height Exponential of Texture Level 8**	**HTXnL8HE**
	7:4	**Height Exponential of Texture Level 7**	**HTXnL7HE**
	3:0	**Height Exponential of Texture Level 6**	**HTXnL6HE**

Bit [31:24] Sub-Address	Bit	Description	Mnemonic
77h	23:22	**Reserved**	
	21:12	**Texture Level 0 Offset** Format: 2's Complement Fix Point Number with 5 bits integer and 5 bits fraction The real Level 0 is (Texture Minimum Level + HTXnL0OS). D[21:17]: 5 bits integer of Texture n Level 0 D[16:12]: 5 bits fraction of Texture n Level 0	**HTXnL0OS**
	11:6	**Maximum Texture Level** 00000: Texture n Maximum Level = 0 00001: Texture n Maximum Level = 1 00010: Texture n Maximum Level = 2 00011: Texture n Maximum Level = 3 00100: Texture n Maximum Level = 4 00101: Texture n Maximum Level = 5 00110: Texture n Maximum Level = 6 00111: Texture n Maximum Level = 7 01000: Texture n Maximum Level = 8 01001: Texture n Maximum Level = 9 01010: Texture n Maximum Level = A 01011: Texture n Maximum Level = B 01100 - 11111: reserved	**HTXnLVmax**
	5:0	**Minimum Texture Level** 00000: Texture n Minimum Level = 0 00001: Texture n Minimum Level = 1 00010: Texture n Minimum Level = 2 00011: Texture n Minimum Level = 3 00100: Texture n Minimum Level = 4 00101: Texture n Minimum Level = 5 00110: Texture n Minimum Level = 6 00111: Texture n Minimum Level = 7 01000: Texture n Minimum Level = 8 01001: Texture n Minimum Level = 9 01010: Texture n Minimum Level = A 01011: Texture n Minimum Level = B 01100 - 11111: reserved	**HTXnLVmin**

Bit [31:24] Sub-Address	Bit	Description	Mnemonic
78h	23:20	**Texture Border** 0000: Neither Texture Border nor Texture Border Color is supported xxx1: Support Texture Border Color in S axis xx1x: Support Texture Border Color in T axis x1xx: Support Texture Border in S axis 1xxx: Support Texture Border in T axis	**HTXnTB**
	19:16	**Reserved**	
	15:13	**Texture Filter Setting in S Direction for Texture Enlargement** 000: Nearest 001: Linear 01x: Reserved 10x: Reserved 110: Flat Cubic or Gausian Cubic (Reserved) 111: Reserved	**HTXnFLSe**
	12:10	**Texture Filter Setting in S Direction for Texture Shrinking** 000: Nearest 001: Linear 010: Reserved 011 - 101: Reserved 110: Flat Cubic or Gausian Cubic (Reserved) 111: Reserved	**HTXnFLSs**
	9:7	**Texture Filter Setting in T Direction for Texture Enlargement** 000: Nearest 001: Linear 01x: Reserved 100: Reserved 101: Reserved 110: Flat Cubic or Gausian Cubic(Reserved) 111: Reserved	**HTXnFLTe**
	6:4	**Texture Filter Setting in T Direction for Texture Shrinking** 000: Nearest 001: Linear 010: Reserved 011: Reserved 101: Reserved 110: Flat Cubic or Gausian Cubic(Reserved) 111: Reserved	**HTXnFLTs**
	3:0	**Texture Filter Setting in D Direction for Texture Shrinking** 0000: Always uses Texture Level 0 0001: Nearest 0010: Linear 0011: Non-linear (Gausine, Advance: Triangle, Sine, Cosine, Round, Trapezoid, Diamond) 0100: Dither 0101: Constant LOD 0110: Anisotropy (The filter setting of S and T is ignored for this mode) 0111: Anisotropy Dither (The filter setting of S and T is ignored for this mode) 1xxx: Reserved	**HTXnFLDs**

Bit [31:24] Sub-Address	Bit	Description	Mnemonic
79h	23:16	**Texture Mapping Mode** D[23:22] Reserved D[21:19] T Axis Setting 000: Single 001: Clamp 010: Repeat 011: Mirror 100: Warp 111-101: Reserved 111: Mirror Once D[18:16] S axis setting 000: Single 001: Clamp 010: Repeat 011: Mirror 100: Warp 111-101: Reserved 111: Mirror Once	**HTXnMPMD**
	15:4	**Reserved**	
	3	**Use Pixel Coordinates (X, Y) as Texture Coordinates (S, T)** 0: :Use Texture Coordinates (S, T) 1: Use Pixel Coordinates (X, Y)	**HTXnXY2ST**
	2:0	**Reserved**	
7A	23:20	**Exponential of the Dividing Factor for dS and dT** 0000: PEdSn = PEdSn / 1, PEdTn = PEdTn / 1 0001: PEdSn = PEdSn / 2, PEdTn = PEdTn / 2 0010: PEdSn = PEdSn / 4, PEdTn = PEdTn / 4 0011: PEdSn = PEdSn / 8, PEdTn = PEdTn / 8 0100: PEdSn = PEdSn / 16, PEdTn = PEdTn / 16 0101: PEdSn = PEdSn / 32, PEdTn = PEdTn / 32 Others: Reserved	**HTXnEFdST**
	19:10	**Constant LOD for Upper Level of MIP Texture** D[19:15]: 5 integer bits of LOD D[14:10]: 5 fraction bits of LOD	**HTXnCLODu**
	9:0	**Constant LOD for Down Level of MIP Texture** D[9:5]: 5 integer bits of LOD D[4:0]: 5 fraction bits of LOD	**HTXnCLODd**

Bit [31:24] Sub-Address	Bit	Description	Mnemonic
7Bh	23:16	**Texture Format** D[23:19] 00000: Index Format 00001: Intensity Format 00010: Luminance Format 00011: Alpha Format 00101: Compressed Texture 00110: YUV(Video Texture) Format 00111: Format for BumpMaping 10001: ARGB_16bpp Format 10011: ARGB_32bpp Format 10101: ABGR_16bpp Format 10111: ABGR_32bpp Format 11001: RGBA_16bpp Format 11011: RGBA_32bpp Format 11101: BGRA_16bpp Format 11111: BGRA_32bpp Format Others: reserved D[18:16] For Index Format 000: Index 1 Format 001: Index 2 Format 010: Index 4 Format Others: reserved For Intensity Format 000: T1 (Bit = T) 001: T2 (Bit[1:0] = TT) 010: T4 (Bit[3:0] = T) 011: T8 (Bit[7:0] = T) 1xx: Reserved For Luminance Format 000: L1 (Bit = L) 001: L2 (Bit[1:0] = L) 010: L4 (Bit[3:0] = L) 011: L8 (Bit[7:0] = L) 100: AL44 (Bit[7:4] = A, Bit[3:0] = L) 101: AL88 (Bit[15:8] = A, Bit[7:0] = L) 11x: Reserved For Alpha Format 000: A1 (Bit = A) 001: A2 (Bit[1:0] = A) 010: A4 (Bit[3:0] = A) 011: A8 (Bit[7:0] = A) 1xx: Reserved For Compressed Format 000: Reserved 001: DXT1, 16-bpp format 010: DXT2, DXT3, 4-bit Alpha format 011: DXT4, DXT5, 3-bit Alpha format 1xx: Reserved	**HTXnFM**

For YUV format(Video Texture)

For YUV format(Video Texture)

000: Package mode (Bit[31:24] = V or Cr, Bit[23:16] = Y1, Bit[15:8] = U or Cb, Bit[7:0] = Y0)
001: AYUV (Bit[31:24] = A, Bit[23:16] = Y, Bit[15:8] = U, Bit[7:0] = V)
010: IA44 (Bit[7:4] = I as a 16 entries index to get a Y(R)8U(G)8V(B)8 texel, Bit[3:0] = A. A does not come from palette)
011: AI44 (Bit[7:4] = A. A does not come from palette, Bit[3:0] = I as a 16 entries index to get a Y(R)8U(G)8V(B)8 texel)
100: Plannar mode (Y in Y buffer, U(Cb) in U buffer and V(Cr) in V buffer)
101: Plannar Y-Crb mode (Y in Y buffer), and V(Cr)U(Cb) in U buffer
The V(Cr)U(Cb) is packet per 128bit from MSB to LSB as V7V6V5V4V3V2V1V0U7U6U5U4U3U2U1U0
111: Reserved

For BumpMapping Format (Reserved)

000: VU88 (Bit[15:8] = dV, Bit[7:0] = dU)
001: LVU655 (Bit[15:10] = L, Bit[9:5] = dV, Bit[4:0] = dU)
010: LVU888 (Bit[23:16] = L, Bit[15:8] = dV, Bit[7:0] = dU)
111– 011: Reserved

For ARGB_16bpp Format

000: RGB555 (Bit[14:10] = R, Bit[9:5] = G, Bit[4:0] = B)
001: RGB565 (Bit[15:11] = R, Bit[10:5] = G, Bit[4:0] = B)
010: ARGB1555 (Bit[15] = A, Bit[14:10] = R, Bit[9:5] = G, Bit[4:0] = B)
011: ARGB4444 (Bit[15:12] = A, Bit[11:8] = R, Bit[7:4] = G, Bit[3:0] = B)
1xx: Reserved

For ARGB_32bpp Format

000: ARGB0888 (Bit[23:16] = R, Bit[15:8] = G, Bit[7:0] = B)
001: ARGB8888 (Bit[31:24] = A, Bit[23:16] = R, Bit[15:8] = G, Bit[7:0] = B)
01x: Reserved
1xx: Reserved

For ABGR_16bpp Format

000: BGR555 (Bit[14:10] = B, Bit[9:5] = G, Bit[4:0] = R)
001: BGR565 (Bit[15:11] = B, Bit[10:5] = G, Bit[4:0] = R)
010: ABGR1555 (Bit[15] = A, Bit[14:10] = B, Bit[9:5] = G, Bit[4:0] = R)
011: ABGR4444 (Bit[15:12] = A, Bit[11:8] = B, Bit[7:4] = G, Bit[3:0] = R)
1xx: Reserved

For ABGR_32bpp Format

000: ABGR0888 (Bit[23:16] = B, Bit[15:8] = G, Bit[7:0] = R)
001: ABGR8888 (Bit[31:24] = A, Bit[23:16] = B, Bit[15:8] = G, bit[7:0] = R)
1xx-01x: Reserved

For RGBA_16bpp Format

000: RGBA5550 (Bit[15:11] = R, Bit[10:6] = G, Bit[5:1] = B)
001: Reserved
010: RGBA5551 (Bit[15:11] = R, Bit[10:6] = G, Bit[5:1] = B, Bit[0] = A)
011: RGBA4444 (Bit[15:12] = R, Bit[11:8] = G, Bit[7:4] = B, Bit[3:0] = A)
1xx:Reserve

For RGBA_32bpp Format

000: RGBA8880 (Bit[31:24] = R, Bit[23:16] = G, Bit[15:8] = B)
001: RGBA8888 (Bit[31:24] = R, Bit[23:16] = G, Bit[15:8] = B, Bit[7:0] = A)
01x: Reserved
1xx: Reserved

For BGRA_16bpp Format

000: BGRA5550 (Bit[15:11] = B, Bit[10:6] = G, Bit[5:1] = R)
001: Reserved
010: BGRA5551 (Bit[15:11] = B, Bit[10:6] = G, Bit[5:1] = R, Bit[0] = A)
011: BGRA4444 (Bit[15:12] = B, Bit[11:8] = G, Bit[7:4] = R, Bit[3:0] = A)
1xx: Reserved

For BGRA_32bpp Format

000: BGRA8880 (Bit[31:24] = B, Bit[23:16] = G, Bit[15:8] = R)
001: BGRA8888 (Bit[31:24] = B, Bit[23:16] = G, Bit[15:8] = R, Bit[7:0] = A)
01x: Reserved
1xx: Reserved

	15	**Texture Color Extending Mode(Excluding Alpha)** 0: Extending with high color bit considering RGB565 as example R4R3R2R1R0R4R3R2 G5G4G3G2G1G0G5G4 B4B3B2B1B0B4B3B2 1: Extending with zero considering RGB565 as example R4R3R2R1R0 000 G5G4G3G2G1G0 00 B4B3B2B1B0 000	**HTXnCExtend**
	14	**Inverse the texel order in one byte for those texture with 1bpp, 2bpp or 3bpp** 0: Normal Consider Index 1: bit[7] for tex[8n+7], bit[6] for tex[8n+6]……..bit[0] for tex[8n] Consider Index 2: bit[7:6] for tex[4n+3], bit[5:4] for tex[4n+2]……..bit[1:0] for tex[4n] Consider Index 4: bit[7:4] for tex[2n+1], bit[3:0] for tex[2n] 1: Inverse Consider Index 1: bit[7] for tex[8n], bit[6] for tex[8n+1]……..bit[0] for tex[8n+7] Consider Index 2: bit[7:6] for tex[4n], bit[5:4] for tex[4n+1]……..bit[1:0] for tex[4n+3] Consider Index 4: bit[7:4] for tex[2n], bit[3:0] for tex[2n+1]	**HTXnInv124bpp**
	13:2	**Reserved**	
	1:0	**Texture Location** Texture n is located in Local Memory 01: Reserved 10: Texture n is located in System Memory 11: Texture n is located in AGP Memory	**HTXnLoc**
7Ch	23:0	**High Color Value of Transparency Test** D[23:16]: The High Value of Texture Transparency Test Red Color or Y Component D[15:8]: The High Value of Texture Transparency Test Green Color or U Component D[7:0]: The High Value of Texture Transparency Test Blue Color or V Component	**HTXnTRCH**
7Dh	23:0	**Low Color Value of Transparency Test** D[23:16]: The Low Value of Texture Transparency Test Red Color or Y Component D[15:8]: The Low Value of Texture Transparency Test Green Color or U Component D[7:0]: The Low Value of Texture Transparency Test Blue Color or V Component	**HTXnTRCL**
7Eh	23:0	**Texture Border Color** D[23:16]: Red Color or Y Component of Texture Border D[15:8]: Green Color or U Component of Texture Border D[7:0]: Blue Color or V Component of Texture Border	**HTXnTBC**
7Fh	23:16	**High Alpha Value of Transparency Test**	**HTXnTRAH**
	15:8	**Low Alpha Value of Transparency Test**	**HTXnTRAL**
	7:0	**Texture Border Alpha**	**HTXnTBA**

Bit [31:24] Sub-Address	Bit	Description	Mnemonic

80h		// Texture Blending
		Equation of RGB: Cout = (Ca * (Cb Cop Cc) + Cbias) << Cshift
		Equation of A: Aout = (Aa * (Ab Aop Ac) + Abias) << Ashift
		
		// The dot product is not supported in single pass texture combine. This feature only supported in multiple pass texture combine.
		If (HTXnTBLCshift == Dot Product) then
		Cout = ((Aa * FAa + Abias) Aop (Ab * FAb))
		+ ((R of Ca * R of FCa + R of Cbias) Cop (R of Cb * R of FCb))
		+ ((G of Ca * G of FCa + G of Cbias) Cop (G of Cb * G of FCb))
		+ ((B of Ca * B of FCa + B of Cbias) Cop (B of Cb * B of FCb))
		If (HTXnTBLCshift == HTXnTBLAshift == Dot Product) then
		Aout = ((Aa * FAa + Abias) Aop (Ab * FAb))
		+ ((R of Ca * R of FCa + R of Cbias) Cop (R of Cb * R of FCb))
		+ ((G of Ca * G of FCa + G of Cbias) Cop (G of Cb * G of FCb))
		+ ((B of Ca * B of FCa + B of Cbias) Cop (B of Cb * B of FCb))
		If (HTXnTBLAshift == Dot Product & HTXnTBLCshift != Dot Product) then
		Aout is undefined.	

	23	**RGB Saturation Control for Texture Blending Calculation** 0: Do not clamp the output of Texture Blending to 0.0 ~ 1.0 1: Clamp the output of Texture Blending to 0.0 ~ 1.0	**HTXnTBLCsat**
	22:20	**Reserved**	
	19:14	**Ca of Texture Blending Equation** **HTXnTBLCa[5:4]** / **R of Ca** / **G of Ca** / **B of Ca** **00** R_of_TOPCa / G_of_TOPCa / B_of_TOPCa **01** Inv (R_of_TOPCa) / Inv (G_of_TOPCa) / Inv (B_of_TOPCa) **10** (R_of_TOPCa) - 0.5 / (G_of_TOPCa) - 0.5 / (B_of_TOPCa) - 0.5 **11** Reserved / Reserved / Reserved **HTXnTBLCa[3:0]** / **R_of_TOPCa** / **G_of_TOPCa** / **B_of_TOPCa** **0000** 0 / 0 / 0 **0001** Rdif / Gdif / Bdif **0010** Rspec / Gspec / Bspec **0011** Rtex / Gtex / Btex **0100** Rcur / Gcur / Bcur **0101** Adif / Adif / Adif **0110** Fog / Fog / Fog **0111** Atex / Atex / Atex **1000** Acur / Acur / Acur **1001** R of HTXnTBLRCa / G of HTXnTBLRCa / B of HTXnTBLRCa **1010** Rtex_next / Gtex_next / Btex_next **1111-1011** Reserved / Reserved / Reserved Note: Currently, HTXnTBLCa[3:0] == 1010 is only used for texture 0. For Texture 1, the setting is reserved.	**HTXnTBLCa**
	13	**Reserved**	
	12:7	**Cb of Texture Blending Equation** **HTXnTBLCb[5:4]** / **R of Cb** / **G of Cb** / **B of Cb** **00** R_of_TOPCb / G_of_TOPCb / B_of_TOPCb **01** Inv (R_of_TOPCb) / Inv (G_of_TOPCb) / Inv (B_of_TOPCb) **10** (R_of_TOPCb) - 0.5 / (G_of_TOPCb) - 0.5 / (B_of_TOPCb) - 0.5 **11** Reserved / Reserved / Reserved **HTXnTBLCb[3:0]** / **R_of_TOPCb** / **G_of_TOPCb** / **B_of_TOPCb** **0000** 0 / 0 / 0 **0001** Rdif / Gdif / Bdif **0010** Rspec / Gspec / Bspec **0011** Rtex / Gtex / Btex **0100** Rcur / Gcur / Bcur **0101** Adif / Adif / Adif **0110** Fog / Fog / Fog **0111** Atex / Atex / Atex **1000** Acur / Acur / Acur **1001** R of HTXnTBLRCb / G of HTXnTBLRCb / B of HTXnTBLRCb **1010** Rtex_next / Gtex_next / Btex_next **1111-1010** Reserved / Reserved / Reserved Note: Currently, HTXnTBLCb[3:0] == 1010 is only used for texture 0. For Texture 1, the setting is reserved.	**HTXnTBLCb**

	6	**Reserved**	
	5:0	**Cc of Texture Blending Equation** The format of Cc is s8.	**HTXnTBLCc**

HTXnTBLCc[5:4]	**R of Cc**	**G of Cc**	**B of Cc**
00	R_of_TOPCc	G_of_TOPCc	B_of_TOPCc
01	Inv (R_of_TOPCc)	Inv (G_of_TOPCc)	Inv (B_of_TOPCc)
10	(R_of_TOPCc) - 0.5	(G_of_TOPCc) - 0.5	(B_of_TOPCc) - 0.5
11	Reserved	Reserved	Reserved

HTXnTBLCc[3:0]	**R_of_TOPCc**	**G_of_TOPCc**	**B_of_TOPCc**
0000	0	0	0
0001	Rdif	Gdif	Bdif
0010	Rspec	Gspec	Bspec
0011	Rtex	Gtex	Btex
0100	Rcur	Gcur	Bcur
0101	Adif	Adif	Adif
0110	Fog	Fog	Fog
0111	Atex	Atex	Atex
1000	Acur	Acur	Acur
1001	R of HTXnTBLRCc	G of HTXnTBLRCc	B of HTXnTBLRCc
1010	Rtex_next	Gtex_next	Btex_next
1111-1010	Reserved	Reserved	Reserved

Note:
Currently, HTXnTBLCc[3:0] == 1010 is only used for texture 0. For Texture 1, the setting is reserved.

Bit [31:24] Sub-Address	Bit	Description	Mnemonic
81h	23:22	**Enable Dot Production for Texture Blending** 0x: No Dot Production used in Texture Blending 10: Use Dot3 Production in Texture Blending 11: Use Dot4 Production in Texture Blending	HTXnTBLdot
	21:19	**Cop of Texture Blending Equation** **HTXnTBLCop[2:0] — Cop** 000 — + 001 — - 010 — Min(Ca, Cb) 011 — Max(Ca, Cb) 100 — Mask Operation If (n^{th} bit of Atex == 1) then Cout = Ca * Cb, else Cout = Cc Others — Reserved Please note that the Min and Max operation will modify the equation as Min(Ca, Cb) << Cshift or Min(Ca, Cb) designer please picks up one of them for less gates.	HTXnTBLCop
	18:14	**Cbias of Texture Blending Equation** The format of Cbias is s8. **HTBLCbias[4] — R of Cbias — G of Cbias — B of Cbias** 0 — R_of_Cbias — G_of_Cbais — B_of_Cbias 1 — Inv(R_of_Cbias) — Inv(G_of_Cbias) — Inv(B_of_Cbias) HTBLCbias[3:0] — R_of_Cbias — G_of_Cbias — B_of_Cbias 0000 — 0 — 0 — 0 0001 — Rdif — Gdif — Bdif 0010 — Rspec — Gspec — Bspec 0011 — Rtex — Gtex — Btex 0100 — Rcur — Gcur — Bcur 0101 — Adif — Adif — Adif 0110 — Fog — Fog — Fog 0111 — Atex — Atex — Atex 1000 — Acur — Acur — Acur 1001 — R of HTXnTBLRCbias — G of HTXnTBLRCbias — B of HTXnTBLRCbias 1111-1010 — Reserved — Reserved — Reserved where HTXnTBLRCbias is a register with a format s7.	HTXnTBLCbias
	13	**Reserved**	
	12:11	**Cshift of Texture Blending Equation** **HTXnTBLCshift[1:0] — Cshift** 00 — Shift Left 1 Bit 01 — Shift Left 2 Bit 10 — No Shift 11 — Reserved	HTXnTBLCshift
	10	**Reserved**	
	9:7	**Aop of Texture Blending Equation** **HTXnTBLAop[1:0] — Aop** 000 — + 001 — - 010 — Min (Aa, Ab) 011 — Max (Aa, Ab) 100 — Mask Operation If (n^{th} bit of Atex == 1) then Aout = Aa * Ab else Aout = Ac Others — Reserved Note that the Min and Max operation will modify the equation as Min(Aa, Ab) << Ashift or Min(Aa, Ab) designer please picks up one of them for less gates.	HTXnTBLAop

	6:3	**Abias of Texture Blending Equation** The format of Abias is s8. **HTXnTBLAbias[3]** — **Abias** 0 — AbiasSel 1 — Inv (AbiasSel) **HTXnTBLAbias[2:0]** — **AbiasSel** 000 — Adif 001 — Fog 010 — Acur 011 — HTXnTBLRAbias 100 — Atex Others — Reserved Where HTXnTBLRAbias is a register with a format s7. Note: For Texture 0, Acur = Adif	**HTXnTBLAbias**
	2	**Reserved**	
	1:0	**Ashift of Texture Blending Equation** **HTXnTBLAshift[1:0]** — **Ashift** 00 — Shift Left 1 Bit 01 — Shift Left 2 Bit 10 — No Shift 11 — Reserved	**HTXnTBLAshift**
82h	23:21	**Texture Blending Setting for Multiple Pass Rendering on Additional Alpha Channel** In multiple pass rendering, we use the fog color for additional alpha channel. **HTXnTBLMPFog[23:21]** — **Fog** 000 — 0 001 — Adif 010 — Fog 011 — Atex 100 — Acur 101 — G of HTXnTBLRFog 111-110 — Reserved Note: For Texture 0, Acur = Adif	**HTXnTBLMPfog[2:0]**
	20:0	**Reserved**	

Bit [31:24] Sub-Address	Bit	Description	Mnemonic
83h	23	**Alpha Saturation Control for Texture Blending Calculation** **HTXnTBLAsat** **Saturation Control on Alpha** 0 Do not clamp the output of Texture Blending to 0.0 ~ 1.0 1 Clamp the output of Texture Blending to 0.0 ~ 1.0 Where 0.0 is 'b00000000, 1.0 is 'b11111111	**HTXnTBLAsat**
	22:20	**Texture Alpha Mask Bit Position of Texture Blending Mask Operation** 000: Use Atex[0] for Texture Blending Mask Operation 001: Use Atex[1] for Texture Blending Mask Operation 010: Use Atex[2] for Texture Blending Mask Operation 011: Use Atex[3] for Texture Blending Mask Operation 100: Use Atex[4] for Texture Blending Mask Operation 101: Use Atex[5] for Texture Blending Mask Operation 110: Use Atex[6] for Texture Blending Mask Operation 111: Use Atex[7] for Texture Blending Mask Operation	**HTXnTBLAMB**
	19	**Reserved**	
	18:14	**Aa of Texture Blending Equation** The format of Aa is s8. **HTXnTBLAa[4:3]** **Aa** 00 TOPAa 01 Inv (TOPAa) 10 (TOPAa) - 0.5 11 Reserved **HTXnTBLAa[2:0]** **TOPAa** 000 Adif 001 Fog 010 Acur 011 HTXnTBLRAa 100 Atex 101 Atex_next Others Reserved Note: Currently, HTXnTBLAa[2:0] ==101 is only used for texture 0. For texture 1, the setting is reserved. For Texture 0, Acur = Adif	**HTXnTBLAa**
	13:12	**Reserved**	
	11:7	**Ab of Texture Blending Equation** The format of Ab is s8. **HTXnTBLAb[4:3]** **Ab** 00 TOPAb 01 Inv (TOPAb) 10 (TOPAb) - 0.5 11 Reserved **HTXnTBLAb[2:0]** **TOPAb** 000 Adif 001 Fog 010 Acur 011 HTXnTBLRAb 100 Atex 101 Atex_next Others Reserved Note: Currently, HTXnTBLAb[2:0] == 101 is only used for texture 0. For texture 1, the setting is reserved. For Texture 0, Acur = Adif	**HTXnTBLAb**
	6:5	**Reserved**	

	4:0	**Ac of Texture Blending Equation** The format of Ac is s8. **HTXnTBLAc[4:3] — Ac** 00 — TOPAc 01 — Inv (TOPAc) 10 — (TOPAc) - 0.5 11 — Reserved **HTXnTBLAc[2:0] — TOPAc** 000 — Adif 001 — Fog 010 — Acur 011 — HTXnTBLRAc 100 — Atex 101 — Atex_next Others — Reserved Note: Currently, HTXnTBLAc[2:0] == 101 is only used for texture 0. For texture 1, the setting is reserved. For Texture 0, Acur = Adif	**HTXnTBLAc**
85h	23:0	**Constant Register of Ca** D[23:16]: R of HTXnTBLRCa D[15:8]: G of HTXnTBLGCa D[7:0]: B of HTXnTBLBCa	**HTXnTBLRCa** **HTXnTBLRCaR** **HTXnTBLRCaG** **HTXnTBLRCaB**
86h	23:0	**Constant Register of Cb** D[23:16]: R of HTXnTBLRCb D[15:8]: G of HTXnTBLGCb D[7:0]: B of HTXnTBLBCb	**HTXnTBLRCb** **HTXnTBLRCbR** **HTXnTBLRCbG** **HTXnTBLRCbB**
87h	23:0	**Constant Register of Cc** D[23:16]: R of HTXnTBLRCc D[15:8]: G of HTXnTBLGCc D[7:0]: B of HTXnTBLBCc	**HTXnTBLRCc** **HTXnTBLRCcR** **HTXnTBLRCcG** **HTXnTBLRCcB**
88h	23:0	**Constant Register of Cbias** D[23:16]: R of HTXnTBLCbias D[15:8]: G of HTXnTBLCbias D[7:0]: B of HTXnTBLCbias	**HTXnTBLRCbias** **HTXnTBLRCbiasR** **HTXnTBLRCbiasG** **HTXnTBLRCbiasB**
89h	23:16	**Constant Register of Aa**	**HTXnTBLRAa**
	15:8	**Constant Register of Ab**	**HTXnTBLRAb**
	7:0	**Constant Register of Ac**	**HTXnTBLRAc**
8Ah	23:16	**Reserved**	
	15:8	**The Constant Register for Additional Alpha Channel of Multiple Pass Alpha Blending** In multiple pass alpha blending, we use fog color for the additional alpha channel	**HTXnTBLRFog**
	7:0	**Constant Register of Abias**	**HTXnTBLRAbiasL**
90h	23:0	**Reserved**	
91h	23:0	**Reserved**	
92h	23:0	**Reserved**	
93h	23:0	**Reserved**	
94h	23:19	**Reserved**	
	18:10	**Scaling Factor of the Bump Mapping Texture's Luminance**	**HTXnLScale**
	9	**Reserved**	
	8:0	**Offset Factor of the Bump Mapping Texture's Luminance**	**HTXnLOff**

HparaSubType: FEh For General Texture Setting

Bit [31:24] Sub-Address	Bit	Description	Mnemonic
00h	23:11	**Reserved**	
	10:8	**The Exponential of the Length of FIFO for Texture Requesting** 000: 1-stage FIFO 001: 2-stage FIFO 010: 4-stage FIFO 011: 8-stage FIFO 100: 16-stage FIFO 101: 32-stage FIFO 11x: Reserved Note: Please set "HTXDFIFOLEN_E[2:0]" to 101b as default value for performance issue.	**HTXDFIFOLEN_E**
	7	**Texture S Coordinate Input Mode** 0: Un-normalized 1: Normalized	**HTXSMD**
	6	**Texture T Coordinate Input Mode** 0: Un-normalized 1: Normalized	**HTXTMD**
	5:3	**Number of Texture** n: n+1 Texture	**HTXNum**
	2:1	**Texture Transparency Mode** 0: Order Dependent Transparency (Very Good Quality, Lower Performance) 1: Order Independent Transparency (Good Quality, Higher Performance)	**HTXTRMD**
	0	**Clear Texture Cache** 0: Do not Care 1: Clear Texture Cache	**HTXCHCLR**
01h	23	**Video Texture is as BT601 (SDTV)**	**HTXYUV2RGB4BT601**
	22	**Video Texture is as BT709 (HDTV)**	**HTXYUV2RGB4BT709**
	21	**Video Texture's YUV is just Mapped to RGB Directly** Y as R, U as G & V as B	**HTXYUVasRGB**
	20:16	**Coefficient A of VUV to RGB Conversion** Format as fixed point 1.4 (x.xxxx) from 0 to 1.9375	**HTXYUV2RGBA**
	15:14	**Reserved**	
	13:8	**Coefficient B1 of VUV to RGB Conversion** Format is a sign cascaded with absolute value (sxx.xxx) from –2.125 to 2.125	**HTXYUV2RGBB1**
	7:6	**Reserved**	
	5:0	**Coefficient C1 of YUV to RGB Conversion** Format is a sign cascaded with absolute value (sxx.xxx) from –2.125 to 2.125	**HTXYUV2RGBC1**

Bit [31:24] Sub-Address	Bit	Description	Mnemonic
02h	23:16	**Integer Part of Coefficient D of YUV to RGB Conversion** Format as 2's complement integer from -127 to 127	HTXYUV2RGBDi
	15:13	**Reserved**	
	12:8	**Coefficient B2 of VUV to RGB Conversion** Format is a sign cascaded with absolute value (sx.xxx) from –1.875 to 1.875	HTXYUV2RGBB2
	7:5	**Reserved**	
	4:0	**Coefficient C2 of YUV to RGB Conversion** Format is a sign cascaded with absolute value (sx.xxx) from –1.875 to 1.875	HTXYUV2RGBC2
03h	23:20	**Reserved**	
	19:17	**Fractional Part of Coefficient D of YUV to RGB Conversion**	HTXYUV2RGBDf
	16	**Chroma Sign Bits Conversation for YUV to RGB Conversation** 0: U(Cb) and V(Cr) are already 2's complement and sent to YVU to RGB conversation directly 1: U(Cb) and V(Cr) have to be subtracted 128 before the YUV to RGB conversation U' = U-128, U is originally positive and thus U' become 2's complement V' = U-128, V is originally positive and thus V' become 2's complement	HTXYUVChrmS
	15:13	**Reserved**	
	12:8	**Coefficient B3 of VUV to RGB Conversion** Format is a sign cascaded with absolute value (sxx.xxx) from –3.875 to 3.875	HTXYUV2RGBB3
	7:6	**Reserved**	
	5:0	**Coefficient C3 of YUV to RGB Conversion** Format is a sign cascaded with absolute value (sxx.xxx) from –3.875 to 3.875	HTXYUV2RGBC3

HParaType = 01h
SW Inspection

Bit [31:24] Sub-Address	Bit	Description	Mnemonic
AAh	23:16	**Reserved**	
	15:0	**Flag Number for SW Inspection**	HCRFlagNum

Texture Palette n (HParaType = 03h)

HParaSubType: 0xh For TexturePalette 0

Bit	Description	Mnemonic
31:24	**Alpha of Texture Palette n Data**	HTPnA
23:16	**R of Texture Palette n Data**	HTPnR
15:8	**G of Texture Palette n Data**	HTPnG
7:0	**B of Texture Palette n Data**	HTPnB

HParaSubType: 10h For Fog Palette

Bit	Description	Mnemonic
31:24	**The (n+3)th Fog Factor**	HFPn3
23:16	**The (n+2)th Fog Factor**	HFPn2
15:8	**The (n+1)th Fog Factor**	HFPn1
7:0	**The (n)th Fog Factor**	HFPn

HParaSubType: 11h For Stipple Palette

Bit	Description	Mnemonic
31:0	**32-bit Stipple Palette Data**	HSP