Intel® Open Source HD Graphics Programmers' Reference Manual (PRM)

Volume 11: Graphics Interface

For the 2014 Intel Atom™ Processors, Celeron™ Processors, and Pentium™ Processors based on the "BayTrail" Platform (ValleyView graphics)

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Notices and Disclaimers

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GenLC Registers

The figure below shows the different types of registers that reside within the GenLC block.

Figure: High-level GenLC Registers

Memory Map

The diagram below shows the memory map for Gfx Device 2.

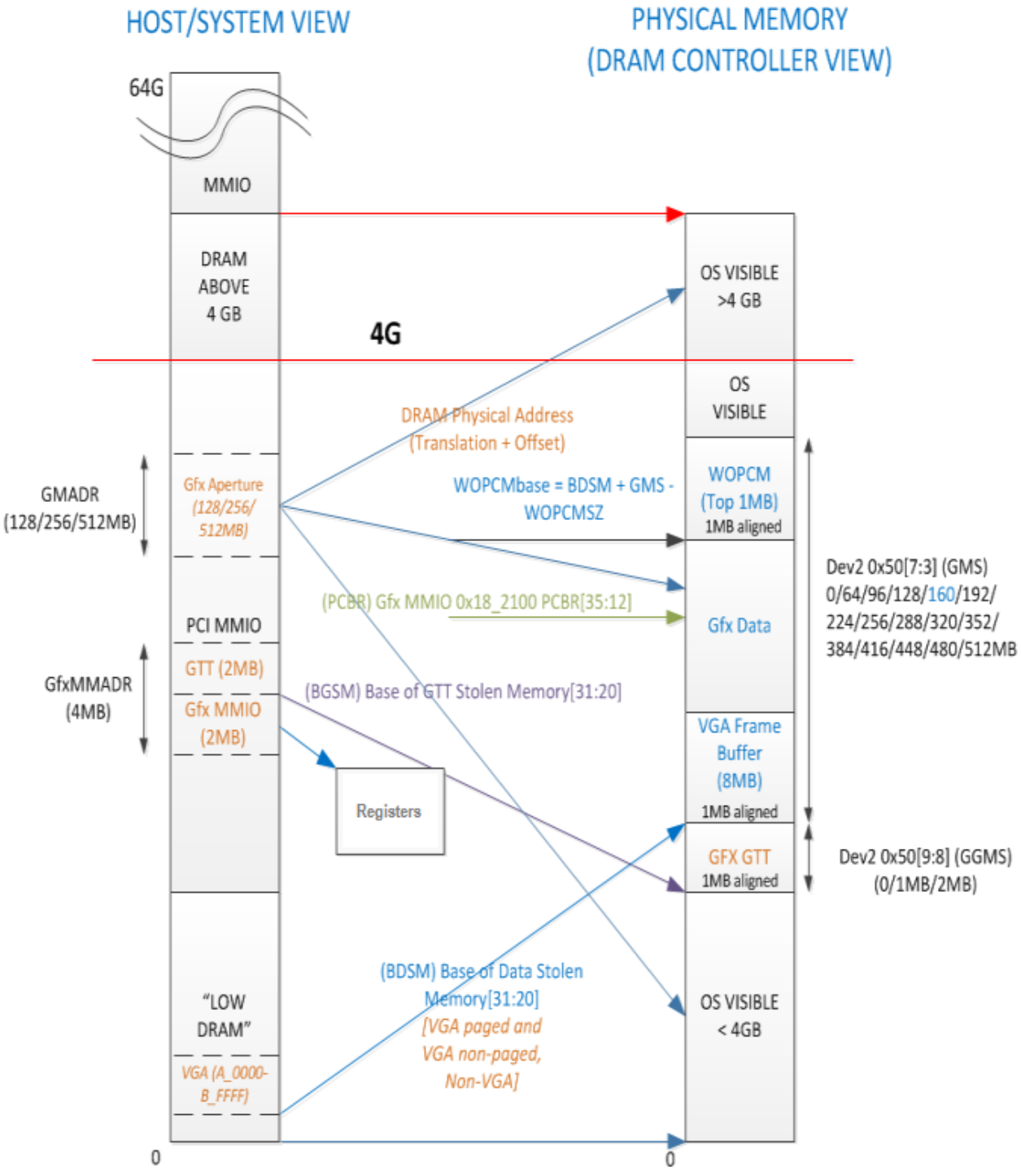

Figure: Device 2 Memory Map

Relocatable Address Ranges

Bus 0, Device 2, Function 0:

1. **IOBAR** – IO access window for internal graphics. Though this window address/data register pair, using I/O semantics, the IGD and internal graphics instruction port registers can be accessed. Note, this allows accessing the same registers as GTTMMADR. The IOBAR can be used to issue writes to the GTTMMADR or the GTT table.
2. **GMADR** – Internal graphics translation window (128MB, 256MB, 512MB window).
3. **GTTMMADR** – This register requests a 4MB allocation for combined Graphics Translation Table Modification Range and Memory Mapped Range. GTTADR will be at GTTMMADR + 2MB while the MMIO base address will be the same as GTTMMADR.
4. **GGC.GMS** – Graphics Mode Select. Used to select the amount of main memory that is pre-allocated to support the internal graphics device in VGA (non-linear) and Native (linear) modes.
5. **GGC.GGMS** – GTT Graphics Memory Size. Used to select the amount of main memory that is pre-allocated to support the Internal Graphics Translation Table. (0-2MB options).

VGA memory and VGA IO addresses are also supported.

Legacy Video Area (A_0000h – B_FFFFh)

The legacy 128KB VGA memory range, frame buffer, (000A_0000h – 000B_FFFFh) can be mapped to Device #2. The VGA memory space is a 128KB space. The space's virtual address range, as seen on the IOSF bus, is A0000h-BFFFFh. The space's starting physical address is given by the Base of Data Stolen Memory register value (Dev 2 register BDSM[31:20]).

Table: Frame Buffer Accesses (VGA Memory Map Mode Register)

VRH_HT_GR06[3:2]	A0000h - AFFFFh	B0000h - B7FFFh	B8000h - BFFFFh
00	X	X	X
01	X		
10		X	
11			X

VGA Paged

The VGA frame buffer is 8MB (similar to client). The space's virtual address range, as seen on the IOSF bus, is A0000h-AFFFFh.

GTT Stolen Memory (GSM)

The base of the GTT table memory is contained in register BGSM. GSM is allocated to store the GFX translation table entries. This space is allocated to store accesses as page table entries get updated through virtual GTTMMADR range. Hardware is responsible to map PTEs into this physical space.

Direct accesses to GSM are not allowed. The memory map programming and North Cluster IMR programming prevents direct GSM accesses. Only hardware translations and fetches can be directed to GSM.

ValleyView North Cluster has IMR registers that define stolen memory regions. The GSM will be mapped into an IMR region. The SAI attribute, driven on PFI, ensures the North Cluster does not invalidate GSM directed translations or fetches.

GTT Table Format Change

The GTT entry will be redefined to use bit 2 to indicate whether a page is snooped or not.

Only the Graphics-initiated accesses need this field; IOSF Host initiated cycles are already coherent, so the aperture translation path can ignore this GTT entry bit.

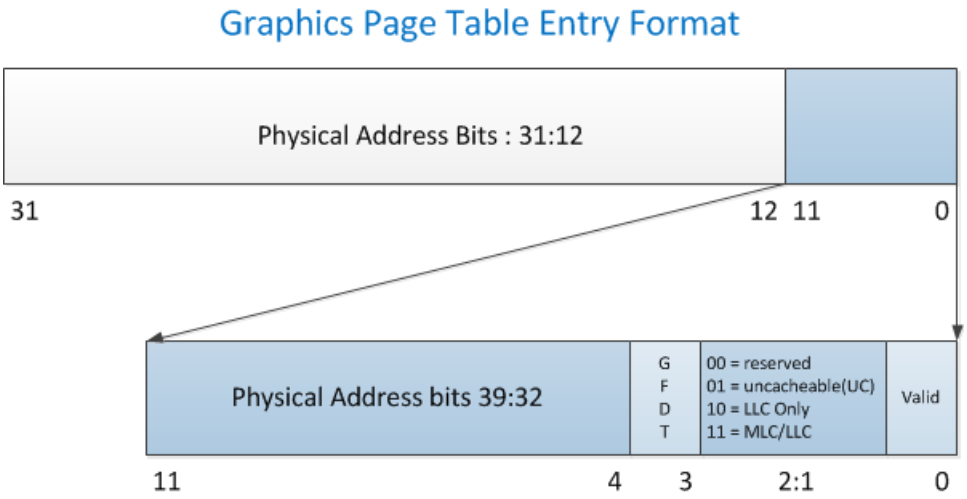

Figure: GTT Table Format

Table: GTT Table Entry Description

Bit	Description
31: 12	**Physical Page Address 31:12:** If the Valid bit is set, This field provides the page number of the physical memory page backing the corresponding Graphics Memory page.
11:4	Physical Start Address Extension: This field specified Bits 39:32 of the page table entry. This field must be zero for 32 bit addresses.
3	Graphics Data Type (GFDT) This field contains the GFDT bit for this surface when writes occur. GFDT can also be set by various state commands and indirect objects. The effective GFDT is the logical OR of the GTT entry with this field. This field is ignored for reads. Format = U1 0: No GFDT (default) 1: GFDT

Bit	Description
2:1	Coherency Control (when GT is a non-caching agent – VLV LCIA) This field controls coherency with the CPU core caches 0x: data in this page is not coherent with the CPU caches 1x: data accesses in this page must be snooped in the CPU caches
0	**Valid PTE:** This field indicates whether the mapping of the corresponding Graphics Memory page is valid. 1: Valid 0: Invalid. An access (other than a CPU Read) through an invalid PTE will result in Page Table Error (Invalid PTE).

Graphics Stolen Memory

The Gen graphics engine relies on a sections of memory that are accessible to graphics but not to CPU software. This is called *stolen memory* or sometimes just *graphics memory*. This consists of 2 ranges, set up by BIOS:

1. GTT stolen memory: Programmable 1MB or 2MB space, used to store virtual->physical graphics translation tables. CPU software cannot access this directly; a section of the GTTMMADR BAR accessible to the Device 2 driver is mapped to this range.
    a. TLB fetch requests are mapped to this range
2. Data stolen memory: Programmable 32MB-512MB space, used for general graphics data (including frame buffers and other local structures). This range will be the target of some of the virtual address pages via the GTT.
    a. Lower 8MB – VGA frame buffer. VGA client can only access this region

For VLV, the Northbridge "IMR" mechanism will be used to reserve these 2 spaces for graphics hidden from the OS.

BAR1 – GTTMMADR (GTT and Regs)

This range will be marked as UC (Un-cacheable). This BAR is split in half. The bottom portion is registers while the top portion is the window to the GTT (Graphics Translation Table).

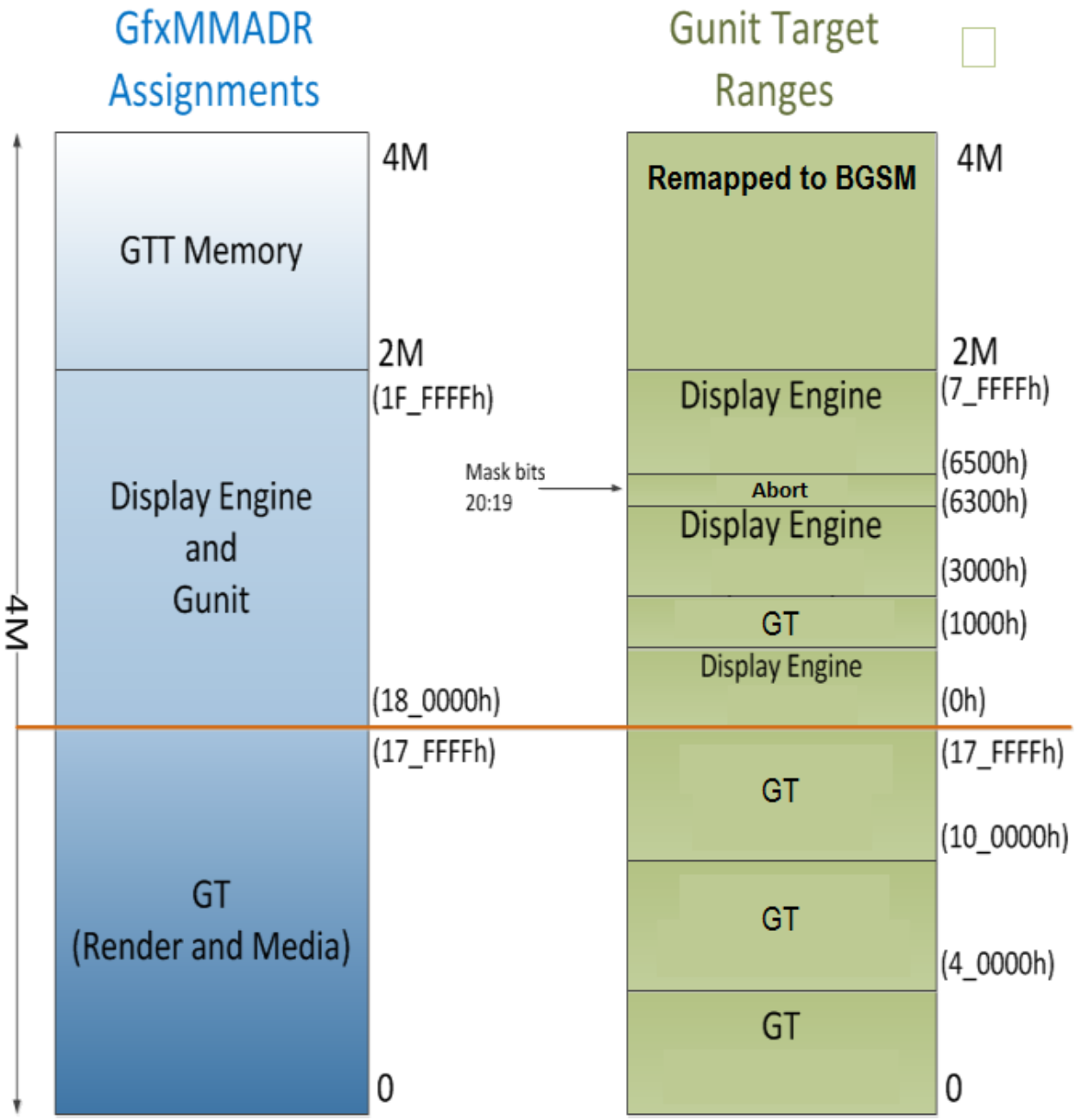

Figure: GTTMMADR Map

BAR2 – GMADR (Gfx Aperture Memory)

IOSF primary accesses targeting GMADR range are translated using the GTT translation table. The resulting physical addressed request is then sent to system memory. The GMADR range can be subdivided using the fence registers within Gfx MMIO space. TileY, TileX, and linear formats will be supported.

IOBAR Indirect MMIO or GTT access

The graphics interface (Device 2) contains an IOBAR register. If Device 2 is enabled, then IGD registers or the GTT table can be accessed using this IOBAR. The IOBAR is composed of an index register and a data register.

MMIO_Index: MMIO_INDEX is a 32 bit register. An IO write to this port loads the offset of the MMIO register or offset into the GTT that needs to be accessed. An IO Read returns the current value of this register. See IOBAR rules for detailed information.

MMIO_Data: MMIO_DATA is a 32 bit register. An IO write to this port is re-directed to the MMIO register pointed to by the MMIO-index register. An IO read to this port is re-directed to the MMIO register pointed to by the MMIO-index register.

The result of accesses through IOBAR can be:

a. Accesses directed to the GTT table. (i.e. route to DRAM)
b. Accesses to Graphics MMIO registers.

Note: GTT table space writes (GTTADR) are supported through this mapping mechanism.

This mechanism to access internal graphics MMIO registers must not be used to access VGA IO registers which are mapped through the MMIO space. VGA registers must be accessed directly through the dedicated VGA IO ports.

Register Range Assignments

- Gfx registers:
  - PCI Configuration registers (housed in Gfx)
  - Gfx "MIR" MMIO registers
    - Gfx related registers
    - Display "MIR" MMIO registers
      1. Housed in Gfx as a service to Display.
  - Gfx "GTLC" MMIO registers
    - SA,
    - GTLC interrupt registers
- GTLC MMIO registers
- Display MMIO registers

Register Clock Domains

This topic is still under development.

Domain Registers

PCI Configuration Registers

Table: PCI Configuration Register Summary

Name	Address	Functionality	Notes
DID	0x0000	PCI Device and Vendor ID Register	
PCICMD	0x0004	PCI Command and Status Register	
PCISTS	0x0006		
RIDCC	0x0008	Revision Identification and Class Codes	
HDR	0x000C	Header Type	
GTTMMADR	0x0010	BAR for Memory Mapped Registers and GTT Table	
GMADR	0x0018	BAR for Gfx Aperture	
IOBAR	0x0020	I/O BAR, BAR for the MMIO_INDEX and MMIO_DATA registers	Used only by SBIOS
SSID	0x002C	Subsystem Identifiers.	Only the BIOS can write this register, and only once after reset. After the first write, this register becomes read-only

Name	Address	Functionality	Notes
CAPPOINT	0x0034	Capabilities Pointer	
INTR	0x003C	Interrupt	This register is programmed by SBIOS. It is not used by the graphics/display driver
MGGC	0x0050	Graphics Control	Used to select the amount of memory pre-allocated to support the graphics device in VGA (non-linear) and Native (linear) modes
BDSM	0x005c	Base of Gfx Data Stolen Memory	Contains the VGA frame buffer and other Gfx data and command structures.
MSAC	0x0062	Multi-Size Aperture Control	
BGSM	0x0070	Base of GTT Stolen Memory	
MSI_CAPID	0x0090	Message Signaled Interrupts Capability ID and Control Register	
MA	0x0094	Message Address	Used for upstream IOSF Primary messages
MD	0x0098	Message Data	Data used for upstream IOSF Primary MSI messages
VCID	0x00B0	Vendor Capability ID	
VC	0x00B4	Vendor Capabilities	
FD	0x00C4	Functional Disable	Used by SBIOS, not by driver
PMCAP	0x00D0	Power Management Capabilities	
PMCS	0x00D4	Power Management Control/Status	Driver and SBIOS don't use this register
SWSMISCI	0x00E0	Software SMI or SCI	The graphics driver writes to this register as a means to interrupt the SBIOS
ASLE	0x00E4	System Display Event Register	SBIOS writes this register to generate an interrupt to the graphics/display driver
ASLS	0x00FC	ASL Storage	

Vendor ID and Device ID

PCI Address: 00h

Description: D2: PCI Device ID and Vendor ID Register

Field Name	Bit	Access	Reset Value	Description
DEVICE_IDENTIFICATION_NUMBER	31:16	RO	0F31	DID: Identifier assigned to the Device 2 Graphics PCI device.
VENDOR_IDENTIFICATION_NUMBER	15:0	RO	8086h	VID: PCI standard identification for Intel

PCICMD

PCI Address: 04h

Description: PCI Command Register

Field Name	Bit	Access	Reset Value	Description
Reserved	15:11	RO	00h	Reserved
INTERRUPT_DISABLE	10	RW	0b	**ID:** 0: Legacy interrupt message is enabled. 1: Disables legacy interrupt message generation on IOSF Sideband. **Note:** The interrupt status is not blocked from being reflected in PCISTS.IS. **Note:** MSI interrupt generation :(PCISTS.IS & PCICMD.BME & MSI_CAPID.MSIE) changes from 0 to 1. **Note:** Message bus interrupt assert is sent: (PCISTS.IS & ~PCICMD.ID & ~MSI_CAPID.MSIE) changes from 0 to 1. **Note:** Message bus interrupt de-assert is sent: (PCISTS.IS & ~PCICMD.ID & ~MSI_CAPID.MSIE) changes from 1 to 0
Reserved	9:3	RO	00h	Reserved
BUS_MASTER_ENABLE	2	RW	0b	**BME:**(BME & MAE are observed. But context save/restore can occur.) 0: Blocks the sending of MSI interrupts. 1: Permits the sending of MSI interrupts
Reserved	1	RW	0b	Reserved
IO_SPACE_ENABLE	0	RW	0b	**IOSE:** 0: I/O space is disabled. IORD and IOWr cycles will not be claimed. 1: I/O space is enabled. VGA_IO and Gfx_IOBAR are checked. If an IORD/IOWR matches (VGA IO address range or GFX_IOBAR), the cycle will be claimed. Care should be taken in setting up GFX_IOBAR that more than 1 match is not made as this will result in unpredictable behavior. VGA_IO: Address[15:0] is checked to determine if it falls in the VGA IO range. (The VGA IO range is 03B0h –03BBh and 03C0h – 03DFh.) Gfx_IOBAR: Address[15:3] is compared to GFX_IOBAR[15:3].

PCISTS

PCI Address: 06h

Description: PCI Status Register

Field Name	Bit	Access	Reset Value	Description
Reserved	15:5	RO	000h	Reserved
CAPABILITY_LIST	4	RO	1b	CAP: Indicates that the CAPPOINT register at 34h provides an offset into PCI Configuration Space containing a pointer to the location of the first item in the list
INTERRUPT_STATUS	3	RO	0b	IS: Reflects the state of the interrupt in the graphics device. 1: Determined by IIR and IER memory interface registers. Indicates a device 2 (Display/Media/Render) interrupt request. 0: No interrupt pending. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the assert_IntX message be sent.
Reserved	2:0	RO	000b	Reserved

Revision ID (RID)

PCI Address: 08h

Description: Revision Identification

Field Name	Bit	Access	Reset Value	Description
REVISION_ID	7:0	RO	From metal straps	RID: The value in this field reflects the value of Revision ID. This register is read-able by any agent.

Class Codes (CC)

PCI Address: 09h

Description: Class Codes

Field Name	Bit	Access	Reset Value	Description
BASE_CLASS_CODE	23:16	RO	03h	**BCC:** This is an 8-bit value that indicates the base class code. When MGGC0[VAMEN] is 0 this code has the value 03h, indicating a Display Controller. When MGGC0[VAMEN] is 1 this code has the value 04h, indicating a Multimedia Device.
SUB_CLASS_CODE	15:8	RO	00h	When MGGC0[VAMEN] is 1, this value is 80h, indicating other multimedia device. When MGGC0[VAMEN] is 0 this value will be determined based on GGC register, GMS and IVD fields. When cfg_MGGC[17] = 1 or cfg_MGGC[22:20] = 3'b000 this value is 80h, otherwise its 00h 00h: VGA compatible 80h: Non VGA (GMS = "00h" or IVD = "1b")
PROGRAMMING_INTERFACE	7:0	RO	00h	**PI:** When MGGC0[VAMEN] is 0 this value is 00h, indicating a Display Controller. When MGGC0[VAMEN] is 1 this value is 00h, indicating a NOP.

HDR

PCI Address: 0Ch

Description: Header Type

Field Name	Bit	Access	Reset Value	Description
Reserved	31:24	RO	00h	Reserved
MULTI_FUNCTION_STATUS	23	RO	0b	MFUNC: Integrated graphics is a single function
HEADER_CODE	22:16	RO	00h	HDR: Indicates a type 0 configuration space header format
Reserved	15:0	RO	0000h	Reserved

GTTMMADR

PCI Address: 10-17h

Description: Gfx Memory Mapped Address Range. This is the base address for all memory mapped registers and GTT table.

This register requests allocation for the combined Graphics Translation Table Modification Range and Memory Mapped Range. The range requires 4 MB combined for MMIO and Global GTT aperture, with 512K of that used by MMIO and 2MB used by GTT. GTTADR will begin at (GTTMMADR + 2 MB) while the MMIO base address will be the same as GTTMMADR.

For the Global GTT, this range is defined as a memory BAR in graphics device config space. It is an alias into which software is required to write Page Table Entry values (PTEs). Software may read PTE values from the global Graphics Translation Table (GTT). PTEs cannot be written directly into the global GTT memory area.

The allocation is for 4MB and the base address is defined by bits [31:22].

Field Name	Bit	Access	Reset Value	Description
Reserved	63:36	RO	000000h	**Reserved for Memory Base Address (RSVD):** Must be set to 0 since addressing above 64GB is not supported.
Reserved	35:32	RO	0h	**Reserved – since 32 bit BAR.**
MBA	31:22	RW	0000h	**Memory Base Address (MBA):** 4MB combined for MMIO and Global GTT table aperture (2MB for MMIO and 2 MB for GTT).
Reserved	21:4	RO	00000h	**Reserved (RSVD):** Hardwired to 0's to indicate at least 4MB address range.
Reserved	3	RO	0b	**Prefetchable Memory (PREFMEM):** Hardwired to 0 to prevent prefetching.
MEMTYP	2:1	RO	00b	**Memory Type (MEMTYP):** 00: To indicate 32 bit base address 01: Reserved 10: To indicate 64 bit base address
Reserved	0	RO	0b	**Memory/IO Space (MIOS):** Hardwired to 0 to indicate memory space.

GMADR – Gfx Memory Address Range (ie. Gfx Aperture)

PCI Address: 18-1Fh

Description: Gfx Aperture location.

GMADR is a Prefetchable range in order to apply USWC attribute (from the processor point of view) to that range. The USWC attribute is used by the processor for write combining.

Accesses to this range will be translated to DRAM Physical memory addresses. Fence registers may be used to sub-divide this range and allow tiled surfaces (determined by fence registers).

The following sizes are supported: 128MB, 256MB, 512MB. (Determined by the MSAC register).

Field Name	Bit	Access	Reset Value	Description
Reserved	63:36	RO	00000000h	**Memory Base Address (MBA2):** Memory Base Address (MBA): Set by the OS, these bits correspond to address signals [63:36].
Reserved	35:32	RO	0h	**Reserved – 32 bit BAR supported**
MBA	31:29	RW	0000000b	**Memory Base Address (MBA):** Memory Base Address (MBA): Set by the OS, these bits correspond to address signals [31:29].
ADMSK512	28	RW-L	0b	**512MB Address Mask (512ADMSK):** This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO), depending on the value of MSAC[2:1]. See MSAC (Dev2, Func 0, offset 62h) for details.
ADMSK256	27	RW-L	0b	**256 MB Address Mask (256ADMSK):** This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO), depending on the value of MSAC[2:1]. See MSAC (Dev 2, Func 0, offset 62h) for details.
Reserved	26:4	RO	0000000h	**Address Mask (ADM):** Hardwired to 0s to indicate at least 128MB address range.
PREFMEM	3	RO	1b	**Prefetchable Memory (PREFMEM):** Hardwired to 1 to enable prefetching.
MEMTYP	2:1	RO	00b	**Memory Type (MEMTYP):** 00: To indicate 32 bit base address 01: Reserved 10: To indicate 64 bit base address
Reserved	0	RO	0b	**Memory/IO Space (MIOS):** Hardwired to 0 to indicate memory space.

IOBAR

PCI Address: 20-23h

Description: I/O Base Address. This is used only by SBIOS. This register is the base address for the MMIO_INDEX and MMIO_DATA registers

This register provides the Base offset of the I/O registers within Device #2. Access to the 8Bs of IO space is allowed in PM state D0 when IO Enable (PCICMD bit 0) set. Access is disallowed:

- in PM states D1-D3 or
- if IO Enable is clear or
- if Device #2 is turned off or
- if Internal graphics is disabled thru the fuse or fuse override mechanisms.

Note that access to this IO BAR is independent of VGA functionality within Device #2.

If accesses to this IO bar is allowed then the GMCH claims all 8, 16 or 32 bit IO cycles from the CPU that falls within the 8B claimed.

Field Name	Bit	Access	Reset Value	Description
Reserved	31:16	RO	0000h	Reserved
BASE_ADDRESS	15:3	RW	0000h	**BA:** Set by the OS, these bits correspond to address signals [15:3]. The IOBAR is to be used for both GTLC register programming and GTT table programming. This is an indirect access method.
Reserved	2:1	RO	0h	Reserved
RESOURCE_TYPE_RTE	0	RO	1b	Indicates a request for I/O space

Subsystem Vendor Identification (SSID)

PCI Address: 2C-2Dh

Description: This register is used to uniquely identify the subsystem where the PCI device resides.

Field Name	Bit	Access	Reset Value	Description
SUBVID	15:0	RW-O	0000h	This value is used to identify the vendor of the subsystem. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.

Subsystem Identification (SID)

PCI Address: 2E-2Fh

Description: This register is used to uniquely identify the subsystem where the PCI device resides.

Field Name	Bit	Access	Reset Value	Description
SUBID	15:0	RW-O	0000h	This value is used to identify the vendor of the subsystem. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.

CAPPOINT

PCI Address: 34-37h

Description: This register points to a linked list of capabilities implemented by this device.

The capability linked list is :

(Head-34, PMCAP-D0, MSI-90, VID-B0, … End)

Field Name	Bit	Access	Reset Value	Description
Reserved	31:8	RO	000000h	Reserved
CAPABILITIES_POINTER	7:0	RW-O	D0h	The first item in the capabilities list is at address D0h (PMCS). This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.

Interrupt Line Register (INTRLINE)

PCI Address: 3Ch

Description: Interrupt. This register is programmed by SBIOS. It is not used by the graphics/display driver. This 8-bit register is used to communicate interrupt line routing information. It is read/write and must be implemented by the device. POST software will write the routing information into this register as it initializes and configures the system.

The value in this register tells which input of the system interrupt controller(s) the device's interrupt pin is connected to. The device itself does not use this value, rather it is used by device drivers and operating systems to determine priority and vector information.

Field Name	Bit	Access	Reset Value	Description
INTRLINE	7:0	RW	00h	ILIN: BIOS written value to communicate interrupt line routing information to the device driver Used to communicate interrupt line routing information. POST software writes the routing information into this register as it initializes and configures the system. The value in this register indicates to which input of the system interrupt controller the device's interrupt pin is connected.

INTR

PCI Address: 3Dh

Description: Interrupt. This register is programmed by SBIOS. It is not used by the graphics/display driver

Field Name	Bit	Access	*Reset Value*	Description
INTERRUPT_PIN	7:0	RO	01h	IPIN: Value indicates which interrupt pin this device uses. This field is hard coded to 1h since Valleyview Device 2 is a single function device. The PCI spec requires that it use INTA#. 01h: INTA#.

GGC

PCI Address: 50-51h

Description: GMCH Graphics Control Register

Field Name	Bit	Access	Reset Value	Description
Reserved	15	RO	0b	Reserved
VAMEN	14	RW-L	0b	Enables the use of the iGFX engines for Versatile Acceleration. 1 – iGFX engines are in Versatile Acceleration Mode. Device 2 Class Code is 048000h. 0 – iGFX engines are in iGFX Mode. Device 2 Class Code is 030000h.
Reserved	13:10	RO	0h	Reserved
GGMS	9:8	RW-L	00b	GTT Graphics Memory Size (GGMS): This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. GSM is assumed to be a contiguous physical DRAM space with DSM, and BIOS needs to allocate a contiguous memory chunk. Hardware will drive the base of GSM from DSM only using the GSM size programmed in the register. 0h: No memory pre-allocated. GTT cycles (Mem and IO) are not claimed. 1h: 1 MB of memory pre-allocated for GTT. 2h: 2 MB of memory pre-allocated for GTT. 3h: Reserved. All unspecified encodings of this register field are reserved,

Field Name	Bit	Access	Reset Value	Description
				hardware functionality is not guaranteed if used.
GMS	7:3	RW-L	00101b	Graphics Mode Select (GMS). This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled. BIOS Requirement: BIOS must not set this field to 0h if IVD (bit 1 of this register) is 0. 0h = 0MB 10h = 512MB 1h = Reserved (32 MB – encoding is only valid for steppings C0 and beyond.) 2h = 64MB 3h = 96MB 4h = 128MB 5h = 160MB 6h = 192MB 7h = 224MB 8h = 256MB 9h = 288MB Ah = 320MB Bh = 352MB Ch = 384MB Dh = 416MB

Field Name	Bit	Access	Reset Value	Description
				Eh = 448MB Fh = 480MB Other = Reserved When GMS != 000 (and VD=0): When GMS == 000 : No address compare will occur against VGA memory range or the VGA IO register range. Also, CC[15:8] is changed to 8'h80 from 8'h00
Reserved	2	RO	0b	Reserved ():
VGA_DISABLE	1	RW-L	0b	**VGA Disable (VD):** 0: Enable. Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00. 1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub- Class Code field within Device 2 function 0 Class Code register is 80. BIOS Requirement: BIOS must not set this bit to 0 if the GMS field pre-allocates no memory. This bit MUST be set to 1 if Device 2 is disabled either via a fuse or fuse override (CAPID0[38] = 1) or via a register (DEVEN[3] = 0).
GGCLCK	0	RW-L	0b	When set to 1b, this bit will lock all bits in this register.

BDSM – Base of Data Stolen Memory

PCI Address: 5C-5Fh

Description: This register contains the base address of Graphics Data Stolen DRAM memory.

Graphics Stolen Memory is within DRAM space. The base of stolen memory will always be below 4G.

Field Name	Bit	Access	Reset Value	Description
BDSM	31:20	RW-L	000h	**BDSM:** BASE_OF_Data_STOLEN_MEMORY This register contains bits 31 to 20 of

Field Name	Bit	Access	Reset Value	Description
				the base address of Data stolen DRAM memory. For certain GTLC generated accesses, this base register will be added to the GTLC provided offset address, forming the full physical address for the PFI fabric. This is also used as a base for VGA paged accesses. The display engine also uses the register.
Reserved	19:1	RO	00000h	Reserved
Lock	0	RW-L	0b	This bit will lock all writeable settings in this register, including itself.

MSAC – Multi-Size Aperture Control

PCI Address: 62h

Description: This register determines the size of the graphics memory aperture. Only the system BIOS will write this register based on pre- boot address allocation efforts. Graphics may read this register to determine the correct aperture size. System BIOS needs to save this value on boot so that it can reset it correctly during S3 resume.

The size of the aperture must not be modified by software after its location is written into GMADR (offset 18h).

Field Name	Bit	Access	Reset Value	Description
Reserved	7:3	RO	00000b	Reserved
LHSAS	2:1	RW	01b	**Untrusted Aperture Size (LHSAS):** 00: bits [28:27] of GMADR register are made R/W allowing **128MB** of GMADR 01: bit [28] of GMADR is made R/W and bit [27] of GMADR is forced to zero allowing **256MB** of GMADR 10: Illegal programming. 11: bits [28:27] of GMADR register are made Read only and forced to zero, allowing only **512MB** of GMADR
Reserved	0	RO	0b	Reserved

BGSM – Base of GTT Stolen Memory

PCI Address: 70-73h

Description: Base of GTT table in Gfx Stolen Memory

The GTT table is located within Graphics Stolen Memory in DRAM space. The base of stolen memory will always be below 4G.

Field Name	Bit	Access	Reset Value	Description
BGSM	31:20	RW-L	000h	**BGSM:** Gfx Base of GTT Stolen Memory This register contains bits 31 to 20 of the base address of GTT Table in stolen DRAM memory. BIOS determines the base of GTT stolen memory by subtracting the GTT graphics stolen memory size (PCI Device 2 offset 50 bits 9:8) from the Graphics Base of Data Stolen Memory (PCI Device 2 offset 5C bits 31:20).
Reserved	19:1	RO	00000h	Reserved
Lock	0	RW-L	0b	This bit will lock all writeable settings in this register, including itself.

MSI_CAPID

PCI Address: 90-91h

Description: Message Signaled Interrupts Capability ID

Field Name	Bit	Access	Reset Value	Description
POINTER_TO_NEXT_CAPABILITY	15:8	RW-O	B0h	Points to the next item in the list (B0=VCID support). Next pointer changed with HSD#259253. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.
CAPABILITY_ID	7:0	RO	05h	CAPID: Indicates an MSI capability

Message Control (MC)

PCI Address: 92-93h

Description: Message Signaled Control Register

Field Name	Bit	Access	Reset Value	Description
Reserved	15:8	RO	00h	Reserved
64_BIT_ADDRESS_CAPABLE	7	RO	0b	**C64:** 32-bit capable only
MULTIPLE_MESSAGE_ENABLE	6:4	RW	000b	**MME:** This field is RW for software compatibility, but only a single message is ever generated System software programs this field to indicate the actual number of messages allocated to this device. This number will be equal to or less than the number actually requested. The encoding is the same as for the MMC field below.
MULTIPLE_MESSAGE_CAPABLE	3:1	RO	000b	**MMC:** This device is only single message capable System Software reads this field to determine the number of messages being requested by this device. Value: Number of requests 000: 1 001- 111: Reserved
MSI_ENABLE	0	RW	0b	**MSIE:** If set, MSI is enabled and traditional interrupts are not used to generate interrupts. PCICMDSTS.BME must be set for an MSI to be generated. 0: MSI interrupts are disabled. 1: MSI interrupts are enabled. Permits sending an MSI interrupt.

MA

PCI Address: 94-97h

Description: Message Address

Field Name	Bit	Access	Reset Value	Description
ADDRESS	31:2	RW	00000000h	**MA:** Lower 32-bits of the system specified message address, always DW aligned. When the GVD issues an MSI interrupt as a MEMWR on the SCL, the memory address corresponds to the value of this field
Reserved	1:0	RO	00b	Reserved

MD

PCI Address: 98-99h

Description: Message Data

Field Name	Bit	Access	Reset Value	Description
Reserved	31:16	RO	0000h	Reserved
DATA	15:0	RW	0000h	**MD:** This 16-bit field is programmed by system software. This is forms the lower word of data for the MSI write transaction.

VCID

PCI Address: B0h

Description: Vendor Capability ID

Field Name	Bit	Access	Reset Value	Description
VERSION	31:24	RO	01h	VS: Identifies this as the first revision of the CAPID register definition
LENGTH	23:16	RO	07h	LEN: This field has the value 07h to indicate the structure length (8 bytes)
NEXT_CAPABILITY_POINTER	15:8	RW-O	00h	00 indicates capability list ends here. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset. Write-once allowing the capability list to be changed.
CAPABILITY_ID_CID	7:0	RO	09h	Identifies this as a vendor dependent capability pointers

VC

PCI Address: B4h

Description: Vendor Capabilities

Any sku related fuses would be added here.

Field Name	Bit	Access	Reset Value	Description
Reserved	31:1	RO	0000000h	Reserved
Reserved	0	RO	0b	Placeholder for sku related fusing. Valleyview has no need for this.

FD

PCI Address: C4h

Description: Functional Disable. This register is used by SBIOS, not by driver

Field Name	Bit	Access	Reset Value	Description
Reserved	31:1	RO	00000000h	Reserved
FUNCTION_DISABLE	0	RW	0b	**FD:** 0: Default – normal operation. 1: When set, the function is disabled (configuration space is disabled).All new requests on the IOSF Primary bus, including any new configuration cycle requests are not claimed on IOSF Primary. This bit as no effect register accessibility via IOSF SB. Once programmed to '1', the only way to re-enable device 2 is via an IOSF SB write of '0' to this register.

PM Capabilities ID

PCI Address: D0-D1h

Description: Power Management Capabilities ID

Field Name	Bit	Access	Reset Value	Description
NEXT_POINTER	15:8	RW-O	90h	Indicates the next item in the capabilities list (90=MSI). This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset. Write once allowing changing of the capabilities list.
CAPABILITIES_ID	7:0	RO	01h	CAPID: SIG defines this ID is 01h for power management

PM Capabilities

PCI Address: D2-D3h

Description: Power Management Capabilities

Field Name	Bit	Access	Reset Value	Description
PME_SUPPORT	15:11	RO	00h	PMES The graphics controller does not generate PME#
D2_SUPPORT	10	RO	0b	D2S: The D2 power management state is not supported
D1_SUPPORT	9	RO	0b	D1S: The D1 power management state is not supported
Reserved	8:6	RO	000b	Reserved
DEVICE_SPECIFIC_INITIALIZATION	5	RO	1b	Hardwired to 1 to indicate that special initialization of the graphics controller is required before generic class device driver is to use it
Reserved	4:3	RO	00b	Reserved
VERSION	2:0	RO	010b	VS: Indicates compliance with revision 1.1 of the PCI Power Management Specification

PMCS

PCI Address: D4-D5h

Description: Power Management Control/Status. Driver doesn't use this register. SBIOS doesn't use this register

Field Name	Bit	Access	Reset Value	Description
Reserved	31:2	RO	00000000h	Reserved
POWER_STATE_PS	1:0	RW	00b	This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. On a transition from D3 to D0 the graphics controller is optionally reset to initial values. Behavior of the graphics controller in supported states is detailed in the power management section of the Bspec. **Bits[1:0] Power state** 00: D0 Default 01: D1 Not Supported 10: D2 Not Supported 11: D3

SWSMISCI

PCI Address: E0-E1h

Description: Software SMI or SCI

The SCI mechanism for driver / BIOS communication. SMI is a system wide lock interrupt (halts the all the cores) as opposed to SCI. Vista and Win7 recommend to use the SCI. The SMI is slowly being phased out.

This register serves 2 purposes:

1. Support selection of SMI or SCI event source (SMISCISEL – bit15)
2. Event trigger (bit 0).

To generate a SW SCI event, software (System BIOS/Graphics driver) should program bit 15 (SMISCISEL) to 1. This is typically programmed once (assuming SMIs are never triggered). On a "0" to "1" subsequent transition in bit 0 of this register (caused by a software write operation), GMCH sends a single SCI message. The SCI will set the DMISCI bit in its TCO1_STS register and TCOSCI_STS bit in its GPE0 register upon receiving this message from DMI.

Once written as 1, software must write a "0" to this bit to clear it, and all other write transitions (1->0, 0->0, 1->1) or if bit 15 is "0" will not cause GMCH to send SCI message to DMI link.

To generate a SW SMI event, software should program bit 15 to 0 and trigger an SMI.

Field Name	Bit	Access	Reset Value	Description
Reserved	31:16	RO	0000h	Reserved
SMI_OR_SCI_EVENT_SELECT	15	RW	0b	MCS: SMI or SCI event select. 0 = SMI 1 = SCI
SOFTWARE_SCRATCH_BITS	14:1	RW	0000h	Used by driver to communicate information to SBIOS. No hardware functionality
SMI_OR_SCI_EVENT	0	RW	0b	**MCE:** MCS=1, setting this bit causes an SCI. MCS=0, setting this bit causes an SMI. A 1 to 0, 0 to 0 or 1 to 1 transition of this bit does not trigger any events. The graphics driver writes to this register as a means to interrupt the SBIOS

ASLE

PCI Address: E4-E7h

Description: System Display Event Register. SBIOS writes this register to generate an interrupt to the graphics/display driver

Field Name	Bit	Access	Reset Value	Description
ASLE_SCRATCH_TRIGGER_3	31:24	RW	00h	AST3: The writing of this by field (byte) – even if just writing back the original contents – will trigger a display controller interrupt (when the memory interface register bits IER[0] = 1 and IMR[0] = 0). If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common
ASLE_SCRATCH_TRIGGER_2	23:16	RW	00h	AST2: The writing of this by field (byte) – even if just writing back the original contents – will trigger a display controller interrupt (when the memory interface register bits IER[0] = 1 and IMR[0] = 0). If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common
ASLE_SCRATCH_TRIGGER_1	15:8	RW	00h	AST1: The writing of this by field (byte) – even if just writing back the original contents – will trigger a display controller interrupt (when the memory interface register bits IER[0] = 1 and IMR[0] = 0). If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common
ASLE_SCRATCH_TRIGGER_0	7:0	RW	00h	AST0: The writing of this by field (byte) – even if just writing back the original contents – will trigger a display controller interrupt (when the memory interface register bits IER[0] = 1 and IMR[0] = 0). If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common

ASLS

PCI Address: FCh

Description: ASL Storage. The Valleyview display driver does not need this register since memory Operational Region (OpRegion) is available. This register is kept for use as scratch space.

This software scratch register only needs to be read/write accessible. The exact bit register usage must be worked out in common between System BIOS and driver software, but storage for switching/indicating up to 6 devices is possible with this amount.

For each device, the ASL control method with require two bits for _DOD (BIOS detectable yes or no, VGA/NonVGA), one bit for _DGS (enable/disable requested), and two bits for _DCS (enabled now/disabled now, connected or not).

Field Name	Bit	Access	Reset Value	Description
SCRATCH	31:0	RW	00000000h	This register provides a means for the BIOS to communicate with the driver. This definition of this scratch register is worked out in common between System BIOS and driver software. Storage for up to 6 devices is possible. For each device, the ASL control method requires two bits for _DOD (BIOS detectable yes or no, VGA/NonVGA), one bit for _DGS (enable/disable requested), and two bits for DCS (enabled now/disabled now, connected or not).

Memory Interface Registers (MIR)

The graphics interface will claim GTTMMADR display offset range: 0x18_1000h to 0x18_2FFFh.

Table: Memory Interface Registers

Name	Address	Functionality	Notes
IIR_RW	0x18_2084	Alternate means to access the IIR register	Provides software RW access to the IIR register. Write/Restore to the IIR register using this address will not trigger an interrupt to the CPU.
SCPD0	0x18_209C	Scratch Pad 0 Register	
IER	0x18_20A0	Interrupt Enable Register	Contains an interrupt enable bit for each interrupt bit in the Interrupt Identity Register (IIR) register. A disabled interrupt will still appear in the Interrupt Identity Register to allow polling of interrupt sources. The bits in this register enable a CPU interrupt to be generated whenever the corresponding bit in the Interrupt Identity Register becomes set.
IIR	0x18_20A4	Interrupt Identity	Contains the persistent values of the interrupt bits that are unmasked by

Name	Address	Functionality	Notes
		Register	the IMR and thus can generate a CPU interrupt (if enabled via the IER). When a CPU interrupt is generated, this should be the first register to be interrogated to determine the source of the interrupt. Bits set in this register will remain set until the interrupt condition is cleared by software. Writing a 1 into the appropriate bit position within this register clears interrupts.
IMR	0x18_20A8	Interrupt Mask	Used by software to control which ISR bits are masked or unmasked. Unmasked bits will be reported in the IIR, possibly triggering a CPU interrupt, and will persist in the IIR until cleared by software. Masked bits will not be reported in the IIR and therefore cannot generate CPU interrupts.
ISR	0x18_20AC	Interrupt Status	Contains the non-persistent value of all interrupt status bits. The IMR register selects which of these interrupt conditions are reported in the persistent IIR (i.e., set bits must be cleared by software). Bits in the IER are used to selectively enable IIR bits to cause CPU interrupts. The User Interrupt bit in this register is a short pulse therefore software should not expect to use this register to sample these conditions.
EIR	0x18_20B0	Error Identity	This register contains the persistent values of ESR error status bits that are unmasked via the EMR register. The logical OR of all (defined) bits in this register is reported in the Master Error bit of the Interrupt Status Register (ISR). In order to clear an error condition, software must first clear the error by writing a 1 to the appropriate bit(s) in this field. If required, software should then proceed to clear the Master Error bit of the IIR.
EMR	0x18_20B4	Error Mask	This register contains a bit mask that selects which error condition bits (from the ESR) are reported in the EIR.
ESR	0x18_20B8	Error Status	This register contains the non-persistent values of all hardware-detected error condition bits.
PCBR	0x18_2120	Power Context Base Register	

IIR_RW – Alternate IIR Access

MMIO Address Offset: 18_2084oh

Description: Alternate means to access the IIR register. This address provides software RW access to the IIR register. Write/Restore to the IIR register using this address will not trigger an interrupt to the CPU.

Field Name	Bit	Access	Reset Value	Description
VED_Power_Interrupt	31	RW	0b	See IIR register for definition of this bit.
Reserved	30:24	RW	0000000b	Reserved
VED_Block_Interrupt	23	RW	0b	See IIR register for definition of this bit.
ISP_Interrupt	22	RW	0b	See IIR register for definition of this bit.
LPE_PIPEB_Interrupt	21	RW	0b	See IIR register for definition of this bit.
LPE_PIPEA_Interrupt	20	RW	0b	See IIR register for definition of this bit.
MIPIB_INTERRUPT	19	RW	0b	See IIR register for definition of this bit.
MIPIA_INTERRUPT	18	RW	0b	See IIR register for definition of this bit.
DISPLAY_HOTSYNC_INTERRUPT	17	RW	0b	See IIR register for definition of this bit.
Reserved	16	RW	0b	Reserved
MASTER_ERROR	15	RW	0b	See IIR register for definition of this bit.
Reserved	14:8	RW	0000000b	Reserved
DISPLAY_PIPE_A_VBLANK	7	RW	0b	See IIR register for definition of this bit.
DISPLAY_PIPE_A_EVENT	6	RW	0b	See IIR register for definition of this bit.
DISPLAY_PIPE_B_VBLANK	5	RW	0b	See IIR register for definition of this bit.
DISPLAY_PIPE_B_EVENT	4	RW	0b	See IIR register for definition of this bit.
DISPLAY_A_DPBM	3	RW	0b	See IIR register for definition of this bit.
DISPLAY_B_DPBM	2	RW	0b	See IIR register for definition of this bit.
GAM_Write_Invalid	1	RW	0b	See IIR register for definition of this bit.
ASLE	0	RW	0b	See IIR register for definition of this bit.

SCPD0 – Scratch Pad 0 Register

MMIO Address Offset: 18_209Coh

Description: Scratch Pad 0 Register

Field Name	Bit	Access	Reset Value	Description
SCPD0	31:0	RW	00000000h	Software scratch pad

IER – Interrupt Enable Register

MMIO Address Offset: 18_20A0oh

Description: IER: Interrupt Enable Register. The IER register contains an interrupt enable bit for each interrupt bit in the Interrupt Identity Register (IIR) register. A disabled interrupt will still appear in the Interrupt Identity Register to allow polling of interrupt sources. The bits in this register enable a CPU interrupt to be generated whenever the corresponding bit in the Interrupt Identity Register becomes set.

Note: The MSI enable and PCICMD "Interrupt disable bit" are additional conditioning that occurs before an actual MSI or INTA message is generated.

Field Name	Bit	Access	Reset Value	Description
VED_Power_Interrupt	31	RW	0b	1 = Generate a CPU interrupt when associated IIR bit and this bit are both set indicating a VED power interrupt. 0 = Do not generate a CPU interrupt when associated IIR bit is set.
Reserved	30:24	RW	0000000b	Reserved
VED_Block_Interrupt	23	RW	0b	1 = Generate a CPU interrupt when associated IIR bit and this bit are both set indicating a VED hardware block interrupt. 0 = Do not generate a CPU interrupt when associated IIR bit is set.
ISP_Interrupt	22	RW	0b	1 = Generate a CPU interrupt when associated IIR bit and this bit are both set indicating an ISP hardware block interrupt. 0 = Do not generate a CPU interrupt when associated IIR bit is set.
LPE_PIPEB_Interrupt	21	RW	0b	1 = Generate a CPU interrupt when the associated IIR bit and this bit are both set indicating a MIPIB event. 0 = Do not generate a CPU interrupt when associated IIR bit is set.
LPE_PIPEA_Interrupt	20	RW	0b	1 = Generate a CPU interrupt when the associated IIR bit and this bit are both set indicating a MIPIB event. 0 = Do not generate a CPU interrupt when associated IIR bit is set.
MIPIB_INTERRUPT	19	RW	0b	1 = Generate a CPU interrupt when the associated IIR bit and this bit are both set indicating a MIPIB event. 0 = Do not generate a CPU interrupt

Field Name	Bit	Access	Reset Value	Description
				when associated IIR bit is set.
MIPIA_INTERRUPT	18	RW	0b	1 = Generate a CPU interrupt when the associated IIR bit and this bit are both set indicating a MIPIA event. 0 = Do not generate a CPU interrupt when associated IIR bit is set.
DISPLAY_HOTSYNC_INTERRUPT	17	RW	0b	1 = Generate a CPU interrupt when the associated IIR bit and this bit are both set indicating a HOT Plug event. 0 = Do not generate a CPU interrupt when associated IIR bit is set.
Reserved	16	RW	0b	Reserved
MASTER_ERROR	15	RW	0b	1 = Generate a CPU interrupt when a master error occurs. A master error condition occurs if any of the bits in the Error Identity Register (EIR) are set. 0 = Do not generate a CPU interrupt when a master error occurs.
Reserved	14:8	RW	0000000b	Reserved
DISPLAY_PIPE_A_VBLANK	7	RW	0b	1 = Generate a CPU interrupt when the associated IIR bit and this bit are both set. 0 = Do not generate a CPU interrupt when associated IIR bit is set.
DISPLAY_PIPE_A_EVENT	6	RW	0b	1 = Generate a CPU interrupt when the associated IIR bit and this bit are both set. 0 = Do not generate a CPU interrupt when associated IIR bit is set.
DISPLAY_PIPE_B_VBLANK	5	RW	0b	1 = Generate a CPU interrupt when the associated IIR bit and this bit are both set. 0 = Do not generate a CPU interrupt when associated IIR bit is set.
DISPLAY_PIPE_B_EVENT	4	RW	0b	1 = Generate a CPU interrupt when the associated IIR bit and this bit are both set. 0 = Do not generate a CPU interrupt when associated IIR bit is set.
DISPLAY_A_DPBM	3	RW	0b	1 = Generate a CPU interrupt when the associated IIR bit and this bit are both set. 0 = Do not generate a CPU interrupt when associated IIR bit is set.

Field Name	Bit	Access	Reset Value	Description
DISPLAY_B_DPBM	2	RW	0b	1 = Generate a CPU interrupt when the associated IIR bit and this bit are both set. 0 = Do not generate a CPU interrupt when associated IIR bit is set.
GAM_Write_Invalid	1	RW	0b	1 = Generate a CPU interrupt when the associated IIR bit and this bit are both set. 0 = Do not generate a CPU interrupt when associated IIR bit is set.
ASLE	0	RW	0b	1 = Generate a CPU interrupt when the ASLE register in the PCI Device 2 configuration space is written. 0 = Do not generate a CPU interrupt when the ASLE register is written.

IIR – Interrupt Identity Register

MMIO Address Offset: 18_20A4oh

Description: The IIR register contains the persistent values of the interrupt bits that are unmasked by the IMR and thus can generate a CPU interrupt (if enabled via the IER). When a CPU interrupt is generated, this should be the first register to be interrogated to determine the source of the interrupt. Bits set in this register will remain set until the interrupt condition is cleared by software. Writing a 1 into the appropriate bit position within this register clears interrupts.

Programming Note: Prior to clearing a Display Pipe-sourced interrupt (e.g., Display Pipe A VBLANK) in the IIR, the corresponding interrupt (source) status in the PIPEASTAT register (e.g., Pipe A VBLANK Interrupt Status bit of PIPEASTAT) must first be cleared.

Note: Bits in this register can be written to '1' by software via a write to 0x18_2084.

A direct write of '1' to any set bit will clear the bit.

Field Name	Bit	Access	Reset Value	Description
VED_Power_Interrupt	31	RW1C	0b	1 = If associated ISR bit asserts and is not IMR masked. 0 = This interrupt condition has either not occurred, or was masked.
Reserved	30:24	RW1C	0000000b	Reserved
VED_Block_Interrupt	23	RW1C	0b	1 = If associated ISR bit asserts and is not IMR masked. 0 = This interrupt condition has either not occurred, or was masked.
ISP_Interrupt	22	RW1C	0b	1 = If associated ISR bit asserts and is not IMR masked.

Field Name	Bit	Access	Reset Value	Description
				0 = This interrupt condition has either not occurred, or was masked.
LPE_PIPEB_Interrupt	21	RW1C	0b	1 = If associated ISR bit asserts and is not IMR masked. This occurs when a MIPIB interrupt event has been detected. The specific trigger of this interrupt can be read in the associated status register. 0 = This interrupt condition has either not occurred, or was masked.
LPE_PIPEA_Interrupt	20	RW1C	-b	1 = If associated ISR bit asserts and is not IMR masked. This occurs when a MIPIB interrupt event has been detected. The specific trigger of this interrupt can be read in the associated status register. 0 = This interrupt condition has either not occurred, or was masked.
MIPIB_INTERRUPT	19	RW1C	0b	1 = If associated ISR bit asserts and is not IMR masked. This occurs when a MIPIB interrupt event has been detected. The specific trigger of this interrupt can be read in the associated status register. 0 = This interrupt condition has either not occurred, or was masked.
MIPIA_INTERRUPT	18	RW1C	0b	1 = If associated ISR bit asserts and is not IMR masked. This occurs when a MIPIA interrupt event has been detected. The specific trigger of this interrupt can be read in the associated status register. 0 = This interrupt condition has either not occurred, or was masked.
DISPLAY_HOTSYNC_INTERRUPT	17	RW1C	0b	1 = If associated ISR bit asserts and is not IMR masked. This occurs when a port hotplug/unplug event has been detected. The specific trigger of this interrupt can be read in the port hotplug status register. 0 = This interrupt condition has either not occurred, or was masked.
Reserved	16	RW1C	0b	Reserved
MASTER_ERROR	15	RW1C	0b	1 = A master error has occurred. A master error condition occurs if any of

Field Name	Bit	Access	Reset Value	Description
				the bits in the Error Identity Register (EIR) are set. 0 = This interrupt condition has either not occurred, or was masked. "OR" of EIR bits.
Reserved	14:8	RW1C	0000000b	Reserved
DISPLAY_PIPE_A_VBLANK	7	RW1C	0b	1 = If associated ISR bit asserts and is not IMR masked. 0 = This interrupt condition has either not occurred, or was masked.
DISPLAY_PIPE_A_EVENT	6	RW1C	0b	1 = If associated ISR bit asserts and is not IMR masked. 0 = This interrupt condition has either not occurred, or was masked.
DISPLAY_PIPE_B_VBLANK	5	RW1C	0b	1 = If associated ISR bit asserts and is not IMR masked. 0 = This interrupt condition has either not occurred, or was masked.
DISPLAY_PIPE_B_EVENT	4	RW1C	0b	1 = If associated ISR bit asserts and is not IMR masked. 0 = This interrupt condition has either not occurred, or was masked.
DISPLAY_A_DPBM	3	RW1C	0b	1 = If associated ISR bit asserts and is not IMR masked. 0 = This interrupt condition has either not occurred, or was masked.
DISPLAY_B_DPBM	2	RW1C	0b	1 = If associated ISR bit asserts and is not IMR masked. 0 = This interrupt condition has either not occurred, or was masked.
GAM_Write_Invalid	1	RW1C	0b	1 = If associated ISR bit asserts and is not IMR masked. 0 = This interrupt condition has either not occurred, or was masked.
ASLE	0	RW1C	0b	1 = If associated ISR bit asserts and is not IMR masked. 0 = This interrupt condition has either not occurred, or was masked.

IMR – Interrupt Mask Register

MMIO Address Offset: 18_20A8oh

Description: The IMR register is used by software to control which ISR bits are masked or unmasked. Unmasked bits will be reported in the IIR, possibly triggering a CPU interrupt, and will persist in the IIR until cleared by software. Masked bits will not be reported in the IIR and therefore cannot generate CPU interrupts

Field Name	Bit	Access	Reset Value	Description
VED_Power_Interrupt	31	RW	1b	1 = Masked. This interrupt will neither be reported in the IIR, nor generate a CPU interrupt. 0 = Unmasked. This interrupt will be reported in the IIR. It will generate a CPU interrupt if the corresponding bit in the IER register is set.
Reserved	30:24	RW	1111111b	Reserved
VED_Block_Interrupt	23	RW	1b	1 = Masked. This interrupt will neither be reported in the IIR, nor generate a CPU interrupt. 0 = Unmasked. This interrupt will be reported in the IIR. It will generate a CPU interrupt if the corresponding bit in the IER register is set.
ISP_Interrupt	22	RW	1b	1 = Masked. This interrupt will neither be reported in the IIR, nor generate a CPU interrupt. 0 = Unmasked. This interrupt will be reported in the IIR. It will generate a CPU interrupt if the corresponding bit in the IER register is set.
LPE_PIPEB_Interrupt	21	RW	1b	1 = Masked. This interrupt will neither be reported in the IIR, nor generate a CPU interrupt. 0 = Unmasked. This interrupt will be reported in the IIR. It will generate a CPU interrupt if the corresponding bit in the IER register is set.
LPE_PIPEA_Interrupt	20	RW	1b	1 = Masked. This interrupt will neither be reported in the IIR, nor generate a CPU interrupt. 0 = Unmasked. This interrupt will be reported in the IIR. It will generate a CPU interrupt if the corresponding bit in the IER register is set.

Field Name	Bit	Access	Reset Value	Description
MIPIB_INTERRUPT	19	RW	1b	1 = Masked. This interrupt will neither be reported in the IIR, nor generate a CPU interrupt. 0 = Unmasked. This interrupt will be reported in the IIR. It will generate a CPU interrupt if the corresponding bit in the IER register is set.
MIPIA_INTERRUPT	18	RW	1b	1 = Masked. This interrupt will neither be reported in the IIR, nor generate a CPU interrupt. 0 = Unmasked. This interrupt will be reported in the IIR. It will generate a CPU interrupt if the corresponding bit in the IER register is set.
DISPLAY_HOTSYNC_INTERRUPT	17	RW	1b	1 = Masked. This interrupt will neither be reported in the IIR, nor generate a CPU interrupt. 0 = Unmasked. This interrupt will be reported in the IIR. It will generate a CPU interrupt if the corresponding bit in the IER register is set.
Reserved	16	RW	1h	Reserved
MASTER_ERROR	15	RW	1b	1 = Masked. This interrupt will neither be reported in the IIR, nor generate a CPU interrupt. 0 = Unmasked. This interrupt will be reported in the IIR. It will generate a CPU interrupt if the corresponding bit in the IER register is set.
Reserved	14:8	RW	1111111b	Reserved
DISPLAY_PIPE_A_VBLANK	7	RW	1b	1 = Masked. This interrupt will neither be reported in the IIR, nor generate a CPU interrupt. 0 = Unmasked. This interrupt will be reported in the IIR. It will generate a CPU interrupt if the corresponding bit in the IER register is set.
DISPLAY_PIPE_A_EVENT	6	RW	1b	1 = Masked. This interrupt will neither be reported in the IIR, nor generate a CPU interrupt. 0 = Unmasked. This interrupt will be reported in the IIR. It will generate a CPU interrupt if the corresponding bit in the IER register is set.

Field Name	Bit	Access	Reset Value	Description
DISPLAY_PIPE_B_VBLANK	5	RW	1b	1 = Masked. This interrupt will neither be reported in the IIR, nor generate a CPU interrupt. 0 = Unmasked. This interrupt will be reported in the IIR. It will generate a CPU interrupt if the corresponding bit in the IER register is set.
DISPLAY_PIPE_B_EVENT	4	RW	1b	1 = Masked. This interrupt will neither be reported in the IIR, nor generate a CPU interrupt. 0 = Unmasked. This interrupt will be reported in the IIR. It will generate a CPU interrupt if the corresponding bit in the IER register is set.
DISPLAY_A_DPBM	3	RW	1b	1 = Masked. This interrupt will neither be reported in the IIR, nor generate a CPU interrupt. 0 = Unmasked. This interrupt will be reported in the IIR. It will generate a CPU interrupt if the corresponding bit in the IER register is set.
DISPLAY_B_DPBM	2	RW	1b	1 = Masked. This interrupt will neither be reported in the IIR, nor generate a CPU interrupt. 0 = Unmasked. This interrupt will be reported in the IIR. It will generate a CPU interrupt if the corresponding bit in the IER register is set.
GAM_Write_Invalid	1	RW	1b	1 = Masked. This interrupt will neither be reported in the IIR, nor generate a CPU interrupt. 0 = Unmasked. This interrupt will be reported in the IIR. It will generate a CPU interrupt if the corresponding bit in the IER register is set.
ASLE	0	RW	1b	1 = Masked. This interrupt will neither be reported in the IIR, nor generate a CPU interrupt. 0 = Unmasked. This interrupt will be reported in the IIR. It will generate a CPU interrupt if the corresponding bit in the IER register is set.

ISR – Interrupt Status Register

MMIO Address Offset: 18_20Acoh

Description: The ISR (Interrupt Status register) contains the non-persistent value of all interrupt status bits. The IMR register selects which of these interrupt conditions are reported in the persistent IIR (i.e., set bits must be cleared by software). Bits in the IER are used to selectively enable IIR bits to cause CPU interrupts. The User Interrupt bit in this register is a short pulse therefore software should not expect to use this register to sample these conditions

Field Name	Bit	Access	Reset Value	Description
VED_Power_Interrupt	31	RW1S	0b	A write of '1' indications this interrupt condition currently exists. Once written '1', hardware will clear this bit the next clock. In other words, a write to this bit mimics a wire pulse.
Reserved	30:24	RO	0000000b	Reserved
VED_Block_Interrupt	23	RO	0b	1 = This interrupt condition currently exists. 0 = This interrupt condition currently does not exist.
ISP_Interrupt	22	RO	0b	1 = This interrupt condition currently exists. 0 = This interrupt condition currently does not exist.
LPE_PIPEB_Interrupt	21	RO	0b	1 = This interrupt condition currently exists. 0 = This interrupt condition currently does not exist.
LPE_PIPEA_Interrupt	20	RO	0b	1 = This interrupt condition currently exists. 0 = This interrupt condition currently does not exist.
MIPIB_INTERRUPT	19	RO	0b	1 = This interrupt condition currently exists. 0 = This interrupt condition currently does not exist.
MIPIA_INTERRUPT	18	RO	0b	1 = This interrupt condition currently exists. 0 = This interrupt condition currently does not exist.
DISPLAY_HOTSYNC_INTERRUPT	17	RO	0b	1 = This interrupt condition currently exists. 0 = This interrupt condition currently does not exist.

Field Name	Bit	Access	Reset Value	Description
Reserved	16	RO	0h	Reserved
MASTER_ERROR	15	RO	0b	1 = This interrupt condition currently exists. 0 = This interrupt condition currently does not exist.
Reserved	14:8	RO	0h	Reserved
DISPLAY_PIPE_A_VBLANK	7	RO	0b	1 = This interrupt condition currently exists. 0 = This interrupt condition currently does not exist.
DISPLAY_PIPE_A_EVENT	6	RO	0b	1 = This interrupt condition currently exists. 0 = This interrupt condition currently does not exist.
DISPLAY_PIPE_B_VBLANK	5	RO	0b	1 = This interrupt condition currently exists. 0 = This interrupt condition currently does not exist.
DISPLAY_PIPE_B_EVENT	4	RO	0b	1 = This interrupt condition currently exists. 0 = This interrupt condition currently does not exist.
DISPLAY_A_DPBM	3	RO	0b	1 = This interrupt condition currently exists. 0 = This interrupt condition currently does not exist.
DISPLAY_B_DPBM	2	RO	0b	1 = This interrupt condition currently exists. 0 = This interrupt condition currently does not exist.
GAM_Write_Invalid	1	RO	0b	1 = This interrupt condition currently exists. 0 = This interrupt condition currently does not exist.
ASLE	0	RO	0b	1 = This interrupt condition currently exists. 0 = This interrupt condition currently does not exist.

EIR – Error Identity Register

MMIO Address Offset: 18_20B0oh

Description: Error Identity. This register contains the persistent values of ESR error status bits that are unmasked via the EMR register. The logical OR of all (defined) bits in this register is reported in the Master Error bit of the Interrupt Status Register (ISR). In order to clear an error condition, software must first clear the error by writing a 1 to the appropriate bit(s) in this field. If required, software should then proceed to clear the Master Error bit of the IIR

Field Name	Bit	Access	Reset Value	Description
Reserved	31:7	RO	0000000h	Reserved
TLB_DataE	6	RW1C	0b	Set if TLB has a data valid error.
Gunit_TLB_PTE	5	RW1C	0b	Set if TLB has a PTE translation error.
PAGE_TABLE_ERROR	4	RW1C	0b	PTE: This bit is set when a Graphics Memory Mapping Error is detected and it's not EMR masked. The cause of the error is indicated (to some extent) in the PGTBL_ER register. This error condition cannot be cleared except by reset (i.e., it is a fatal error).
Reserved	3:1	RO	0h	Reserved
CLAIM_ERROR	0	RW1C	0b	If EMR[0]=1, this bit is set when an address within the address space is accessed, but no memory mapped register exists in this address. This error condition can be cleared by writing 1b to this bit.

EMR – Error Mask Register

MMIO Address Offset: 18_20B4oh

Description: Error Mask. This register contains a bit mask that selects which error condition bits (from the ESR) are reported in the EIR.

Field Name	Bit	Access	Reset Value	Description
Reserved	31:7	RO	0000000h	Reserved
TLB_DataE	6	RW	1b	1 = Masked. This error will neither be reported in the EIR, nor set the master error condition in the IIR. 0 = Unmasked. This interrupt will be reported in the EIR and will set the master error condition in the IIR.
TLB_PTE	5	RW	1b	1 = Masked. This error will neither be reported in the EIR, nor set the master error condition in the IIR. 0 = Unmasked. This interrupt will be reported in the EIR and will set the master error condition in the IIR.
PAGE_TABLE_ERROR	4	RW	1b	1 = Masked. This error will neither be reported in the EIR, nor set the master error condition in the IIR. 0 = Unmasked. This interrupt will be reported in the EIR and will set the master error condition in the IIR.
Reserved	3:1	RO	0h	Reserved
CLAIM_ERROR	0	RW	1b	1 = Masked. This error will neither be reported in the EIR, nor set the master error condition in the IIR. 0 = Unmasked. This interrupt will be reported in the EIR and will set the master error condition in the IIR.

ESR – Error Status Register

MMIO Address Offset: 18_20B8oh

Description: Error Status. This register contains the non-persistent values of all hardware-detected error condition bits.

Field Name	Bit	Access	Reset Value	Description
Reserved	31:7	RO	0000000h	Reserved
TLB_DataE	6	RO	0b	1 = This error condition currently exists. 0 = This error condition currently does not exist.
TLB_PTE	5	RO	0b	1 = This error condition currently exists. 0 = This error condition currently does not exist.
PAGE_TABLE_ERROR	4	RO	0b	1 = This error condition currently exists. 0 = This error condition currently does not exist.
Reserved	3:1	RO	0h	Reserved
CLAIM_ERROR	0	RO	0b	No RMbus claim occurred. Logging the error. 1 = This error condition currently exists. 0 = This error condition currently does not exist.

Power Context Base Register (PCBR)

MMIO Offset Address: 18_2120oh

Description: This provides an base address for context save/restore of GT and Media power context to DRAM.

The BIOS is expected to program this register and ensure proper allocation within Gfx stolen memory.

Field Name	Bit	Access	Reset Value	Description
Reserved	63:32	RO	000000h	Reserved
Power Context Address	31:12	RW-L	0000000h	4KB aligned address Locked with bit 0
Reserved	11:1	RO	000h	Reserved
Power Context Register Lock	0	RW-L	0b	Writing a '1' to this register locks this bit – preventing further updates. The Power Context Address bits are also locked.

GTLC: SA MMIO Registers

For Valleyview, the graphics interface will contain these registers.

This is range: 10_0000 to 17_FFFFh.

Table: GTLC SA MMIO registers

Name	Address	Functionality	Notes
Fence Registers	0x10_0000 to 0x10_007Fh	Fence Registers	Determine whether GMADR subregion is linear/TileX/TileY.
Gfx Flush Control	0x10_1008h	Invalidates TLB	Invalidates the TLB.
GTFIFOCTL	0x12_0008	GT FIFO Control	
GTLC Wake Control	0x13_0090	GTLC Wake Control	
GTLC Power Well Status	0x13_0094	GTLC Power Well Status	
Render Force Wake Req	0x13_00B0		
Render Force Wake Ack	0x13_00B4		
Media Force Wake Req	0x13_00B8		
Media Force Wake Ack	0x13_00BC		
Render RC6 (Standby) counter	0x13_8108		
Media RC6 (Standby) counter	0x13_810C		

Fence Registers

MMIO Address Offset: 10_0000h

Description: Fence Registers

Fence0 Register: 10_0000h

Fence1 Register: 10_0008h

....

Fence15 Register: 10_0078h

Field Name	Bit	Access	Reset Value	Description
FENCEUP	63:44	RW	00000000h	Bits 31:12 of the ending Graphics Address of the fence region. Fence regions must be aligned to a 4KB page. This address represents the last 4KB page of the fence region (Upper Bound is included in the fence region). Graphics Address is the offset within GMADR space.
Reserved	43	RO	0b	Reserved
Pitch	42:32	RW	000h	This field specifies the width (pitch) of the fence region in multiple of "tile widths". For Tile X this field must be programmed to a multiple of 512B ("003" is the minimum value) and for Tile Y this field must be programmed to a multiple of 128B ("000" is the minimum value). 000h = 128B 001h = 256B 002h = 384B 003h = 512B 004h = 640B 005h = 768B 006h = 896B 007h = 1024B ... 3FFh = 128KB

Field Name	Bit	Access	Reset Value	Description
				4FFh = 160KB 5FFh = 192KB 6FFh = 224KB 7FFh = 256KB
FENCELO	31:12	RW	000000h	Bits 31:12 of the starting Graphics Address of the fence region. Fence regions must be aligned to 4KB. This address represents the first 4KB page of the fence region (Lower Bound is included in the fence region). Graphics Address is the offset within GMADR.
Reserved	11:2	RO	000h	Reserved.
TILE	1	RW	0b	**This field specifies the spatial ordering of QW within tiles.** 0b - Consecutive SWords (32B) sequenced in the X direction 1b - Consecutive OWords (16B) sequenced in the Y direction
FENCEVAL	0	RW	0b	This field specifies whether or not this fence register defines a fence region. 0b - FENCE INVALID 1b - FENCE VALID

Gfx_FLSH_CNTL

MMIO Address Offset: 10_1008Description:

Description: Used to flush the TLB.

Field Name	Bit	Access	Reset Value	Description
Reserved	31:1	RO	00000000h	Reserved
GfxFlshCntl	0	WO	0b	A write to this bit flushes the GFX TLB in the graphics interface. The data associated with the write is discarded and a read returns all 0s.

GTFIFOCTL

MMIO Address Offset: 12_0008h

Description: GT FIFO Control. Number of free Wake FIFO entries.

Field Name	Bit	Access	Reset Value	Description
Reserved	31:7	RW	0b	Reserved (should not be changed)
GT_FIFO_FREE_ENTRIES	6:0	RO	40h	This value indicate the number of entries that are free within the GT FIFO. The free entries may be used for IA accesses and IO accesses to GT. The Wake FIFO depth is 64 entries. Zero entries free = "threshold has been hit" condition.

GTLC Wake Control

MMIO Address Offset: 13_0090h

Description: GT Wake Control. This register is used as a way to control the GTLC Render and Media Power wells.

Writing bit 0 during normal operation may result in a hang.

Field Name	Bit	Access	*Reset Value*	Description
Reserved	31:26	RO	00h	Reserved
RenderContextExists	25	RW	0b	• SW can only write a one to this bit. The usage is for support of s0ix, where the Driver would restore the value in this bit no later than the time a '1' is written to ALLOWWAKEREQ (bit 0 of this register) during s0ix exit. SW should not write '1' to this bit during a cold boot exit or warm reset exit. • CZ reset is the only thing that can clear this bit. • This bit is set by HW after the first Render context save after cold boot or warm reset. • SW can only write a one to this bit. If SW tries to write a zero, the previous value will be

Field Name	Bit	Access	*Reset Value*	Description
				maintained.
MediaContextExists	24	RW	0b	• SW can only write a one to this bit. The usage is for support of s0ix, where the Driver would restore the value in this bit no later than the time a '1' is written to ALLOWWAKEREQ (bit 0 of this register) during s0ix exit. SW should not write '1' to this bit during a cold boot exit or warm reset exit. • CZ reset is the only thing that can clear this bit. • This bit is set by HW after the first Media context save after cold boot or warm reset. • SW can only write a one to this bit. If SW tries to write a zero, the previous value will be maintained.
Reserved	23:17	RO	00h	Reserved
Reserved	16	RW	0b	Reserved
Reserved	15:9	RO	00h	Reserved
Reserved	8	RW	0b	Reserved
Reserved	7:1	RO	00h	Reserved
ALLOWWAKEREQ	0	RW	0	This bit is used as a way for the driver to make sure GTLC Render AND MEDIA engines do not wake while powered down. The usage is specifically with s0ix, where the driver wants to access the message channel common well (GSclk domain) and does not want the render/media wells to wake up. To remove ambiguity, this bit should be set to '1' and the ALLOWWAKEACK should be observed to the '1' before the FWAKEMEDIAREQ/FWAKERENDERREQ are set. Care must be taken to ONLY use this register prior to powering down the graphics interface for S0ix or after registers have been initialized.

GTLC Power Well Status

MMIO Address Offset: 13_0094h

Description: This register contains Ack and status information for power well requests.

Field Name	Bit	Access	Reset Value	Description
Reserved	31:8	RO	000000h	Reserved
Reserved	7	RO	0b	Reserved
Reserved	6	RO	0b	Reserved
Reserved	5	RO	0b	Reserved
Reserved	4	RO	0b	Reserved
Reserved	3:2	RO	00b	Reserved
ALLOWWAKEERR	1	RW1C	0b	HW set, SW cleared. When access to media or render is observed when ALLOWWAKE=0, the ALLOWWAKERR bit will be set. It will be up to SW or a power cycle to clear the ALLOWWAKEERR bit.
ALLOWWAKEACK	0	RO	0b	Indicates that the allow wake request has been completed.

Render Force wake req

MMIO Address Offset: 13_00B0h

Description: This register contains per thread force wake request bits for the Render power Well.. The upper 16 bits act as masks for the lower 16 bits. bit-31 masks bit-15 and bit 16 masks bit 0.

1. Driver writes to GPM force wake request bit. (VV will have a Render(13_00B0(15:0)) and a Media (13_00B8(15:0)) bits)
2. The GPM responds by writing (via PLINK) to 1300B4[15:0] or 1300BC[15:0] register.
3. Driver polls (1300B4[15:0] and/or 1300BC[15:0])status until 1 ... indicating that that well has completed wake sequence.

Since the registers are per thread, only the specific bit that was forced should be checked for status.

Field Name	Bit	Access	Reset Value	Description
FWAKERENDERREQMSK	31:16	RO	0000h	Mask bits for lower 16 bits to avoid a read modify/write. If '0', the corresponding bit in [15:0] is not changed. If '1', the corresponding bit in [15:0] is changed to the value in [15:0].
FWAKERENDERREQ	15:0	RW	0000h	Force Wake Render request bits.

Render Force wake ack

MMIO Address Offset: 13_00B4h

Description: This register contains the per thread force wake acknowledge bits for the Render power well.

Field Name	Bit	Access	Reset Value	Description
Reserved	31:16	RO	0000h	Reserved
FWAKERENDERACK	15:0	RW	0000h	Force Wake Render request bits. Driver must poll on the corresponding bit to confirm that the well has woken. For example, if 13_00B0[0] is written to a '1' (along with 13_00B0[16]='1'), then bit0 of this register indicates when the force wake request has been completed.

Media Force wake req

MMIO Address Offset: 13_00B8h

Description: This register contains per thread force wake request bits for the Media power Well. The upper 16 bits act as masks for the lower 16 bits. bit-31 masks bit-15 and bit 16 masks bit 0.

Field Name	Bit	Access	Reset Value	Description
FWAKEMEDIAREQMSK	31:16	RO	0000h	Mask bits for lower 16 bits to avoid a read modify/write. If '0', the corresponding bit in [15:0] is not changed. If '1', the corresponding bit in [15:0] is changed to the value in [15:0]
FWAKEMEDIAREQ	15:0	RW	0000h	Force Wake Media request bits

Media Force wake ack

MMIO Address Offset: 13_00BCh

Description: This register contains the per thread force wake acknowledge bits for the Media power well.

Field Name	Bit	Access	Reset Value	Description
Reserved	31:16	RO	0000h	Reserved
FWAKEMEDIAACK	15:0	RW	0000h	Force Wake Media request bits. Driver must poll on the corresponding bit to confirm that the well has woken. For example, if 13_00B0[0] is written to a '1' (along with 13_00B0[16]='1'), then bit0 of this register indicates when the force wake request has been completed.

Render RC6 (Standby) counter

MMIO Address Offset: 13_8108h

Description: This register contains the total RC6 residency (Render power gated and clock gated) time that Render power well was in since boot. The counter will wrap around. The time is given in units of 1.28 uSec.The 40-bit HW counter will wrap around. The only clear condition is reset. When 0x13_8104[15] is set to zero, bits 31:0 of the 40-bit counter are reported. When 0x13_8104[15] is set to one, bits 39:8 of the 40-bit counter are reported. The units are CZ clock cycles.

It is up to SW to periodically read this register and do a difference from the last time it was read. The primary usage for this register is for power characterization.

0x13_8104[0] controls if this register should count or if it should be gated: 0= clear, 1=count

Field Name	Bit	Access	Reset Value	Description
RENDERRC6TIME	31:0	RO	00000000h	Render Residency Counter

Media RC6 (Standby) counter

MMIO Address Offset: 13_810Ch

Description: This register contains the total RC6 residency (Media power gated and clock gated) time that Media was in since boot. The counter will wrap around. The time is given in units of cz clock cycles.

The 40-bit HW counter will wrap around. The only clear condition is CZ reset. When 0x13_8104[15] is set to zero, bits 31:0 of the 40-bit counter are reported. When 0x13_8104[15] is set to one, bits 39:8 of the 40-bit counter are reported. The units are CZ clock cycles.

It is up to SW to periodically read this register and do a difference from the last time it was read. The primary usage for this register is for power characterization.

0x13_8104[1] controls if this register should count or if it should be gated: 0= clear, 1=count

Field Name	Bit	Access	Reset Value	Description
MEDIARC6TIME	31:0	RO	00000000h	Media Residency Counter

GTLC: "Render/Media/PM" Interrupt Architecture

GTLC can send status messages for Render/Media and for Power Management. There are separate sets of IIR/IMR/IER/ISR registers for Render/Media and for Power Management.

The graphics interface will house these registers.

Table: GTLC "Display" MMIO registers

Name	Address	Functionality	Notes
GTLC MIR	0x4_400Ch		GTLC Master Interrupt Enable
GTLC ISR	0x4_4010h		
GTLC IMR	0x4_4014h		
GTLC IIR	0x4_4018h		
GTLC IER	0x4_401Ch		
PM ISR	0x4_4020h		
PM IMR	0x4_4024h		
PM IIR	0x4_4028h		
PM IER	0x4_402Ch		
SWF	0x4_F000h to 0x4_F08Fh		Software Flag registers. Used by software
GTSCRATCH	0x4_F100h to 0x4_F11Fh		GT Scratch pad registers. Used by software.

GTLC: Master Interrupt Register

MMIO Address Offset: 4400Ch

Description: GTLC Master Interrupt Control Register.

For VLV, the display engine has its own interrupt registers. As a result, only the GTLC Master interrupt bit remains. The graphics interface will house these registers.

GTLC Master Interrupt Register	
Register Type:	MMIO
Project:	All
Default Value:	00000000h
Access Type:	Read Only, R/W
Size (in bits):	32

For VV, this register simply controls GTLC (Render/Media/PM) ability to generate interrupts.

Bit	Description
31	**Read-Write. GTLC Master_Interrupt_Control** Project: / Format: All / MB1 for GTLC interrupts This is the master control for the GTLC to CPU interrupts. This bit must be set to 1 for any GTLC interrupts to propagate to the system.
30:0	Read-only. *Reserved for VV*

GTLC: "Render/Media" Interrupts

Bit Definition for Interrupt Control Registers. All following interrupts are originated from GT in message format. DE needs to convert the message bits to events mapping one to one to following register.

Bit	Description
Blitter Interrupts (BCS bit31-bit22)	
31:30	*Reserved for Blitter Command Streamer*
29	**Blitter page directory faults:** This is a write of logic1 via interrupt message from GT via 0x50200 bit29
28	*Reserved for Blitter Command Streamer*
27	*Reserved for Blitter Command Streamer*
26	**Blitter MI_FLUSH_DW notify:** This is a write of logic1 via interrupt message from GT via 0x50200 bit26
25	**Blitter Command Streamererror interrupt:** This is a write of logic1 via interrupt message from GT via 0x50200 bit25
24	**Billter MMIO sync flush status:** This is a write of logic1 via interrupt message from GT via 0x50200 bit24
23	*Reserved for Blitter Command Streamer*
22	**Blitter Command Streamer MI_USER_INTERRUPT:** This is a write of logic1 via interrupt message from GT via 0x50200 bit22
Media Interrupts (VCS bit21-bit12)	
21	*Reserved for Video Command Streamer*
19	**Video page directory faults:** This is a write of logic1 via interrupt message from GT via 0x50200 bit19
18	**Video Command Streamer Watchdog counter exceeded:** This is a write of logic1 via interrupt message from GT via 0x50200 bit18
16	**Video MI_FLUSH_DW notify:** This is a write of logic1 via interrupt message from GT via 0x50200 bit16
15	**Video Command Streamer error interrupt:** This is a write of logic1 via interrupt message from GT via 0x50200 bit15
14	**Video MMIO sync flush status:** This is a write of logic1 via interrupt message from GT via 0x50200 bit14
12	**Video Command Streamer MI_USER_INTERRUPT:** This is a write of logic1 via interrupt message from GT via 0x50200 bit12
Render Interrupts (CS bit11-bit0)	
11:9	*Reserved for Main Command Streamer*
7	**Render page directory faults:** This is a write of logic1 via interrupt message from GT via 0x50200 bit7
6	**Render Command Streamer Watchdog counter exceeded:** This is a write of logic1 via interrupt message from GT via 0x50200 bit6
5	**L3 Parity Error Interrupt**
4	**Render PIPE_CONTROL notify:** This is a write of logic1 via interrupt message from GT via 0x50200 bit4
3	**Render Command Streamer error interrupt:** This is a write of logic1 via interrupt message from GT via 0x50200 bit3
2	**Render MMIO sync flush status:** This is a write of logic1 via interrupt message from GT via 0x50200 bit2
1	
0	**Render Command Streamer MI_USER_INTERRUPT:** This is a write of logic1 via interrupt message from GT via 0x50200 bit0

ISR – Interrupt Status Register

MMIO Address Offset: 4_4010h

Description: Interrupt Status

ISR	
Register Type:	MMIO
Project:	All
Default Value:	00000000h
Access Type:	Read Only
Size (in bits):	32

See the interrupt bit definition tables to find the source event for each interrupt bit.

Bit	Description
31:0	**Interrupt_Status_Bits**

Project:	All
This field contains the non-persistent values of all interrupt status bits. The IMR register selects which of these interrupt conditions are reported in the persistent IIR.	

Value	Name	Description	Project
0b	Condition Doesn't exist	Interrupt Condition currently does not exist	All
1b	Condition Exists	Interrupt Condition currently exists	All

Programming Notes
Some inputs to this register are short pulses; therefore software should not expect to use this register to sample these conditions.

IMR – Interrupt Mask Register

MMIO Address Offset: 4_4014h

Description: Interrupt Mask Register

IMR	
Register Type:	MMIO
Project:	All
Default Value:	FFFFFFFFh
Access Type:	R/W
Size (in bits):	32

For GT command streamer interrupts DO NOT use this register to mask interrupt events. Instead use the individual GT command streamer MASK bits.
For PM interrupts DO NOT use this register to mask interrupt events. Instead use the individual PM MASK bits in the corresponding PMunit register space.
See the interrupt bit definition tables to find the source event for each interrupt bit.

Bit	Description
31:0	**Interrupt_Mask_Bits** Project: All This field contains a bit mask which selects which interrupt bits from the ISR are reported in the IIR.

Value	Name	Description	Project
0b	Not Masked	Not Masked – will be reported in the IIR	All
1b	Masked	Masked – will not be reported in the IIR	All

IIR

MMIO Address Offset: 4_4018h

Description: Interrupt Identity Register

IIR	
Register Type:	MMIO
Project:	All
Default Value:	00000000h
Access Type:	R/W Clear
Size (in bits):	32

See the interrupt bit definition tables to find the source event for each interrupt bit.

Bit	Description
31:0	**Interrupt_Identity_Bits** Project: All This field holds the persistent values of the interrupt bits from the ISR which are unmasked by the IMR. If enabled by the IER, bits set in this register will generate a CPU interrupt. Bits set in this register will remain set (persist) until the interrupt condition is cleared by writing a '1' to the appropriate bits. For each bit, the IIR can store a second pending interrupt if two or more of the same interrupt conditions occur before the first condition is cleared. Upon clearing the interrupt, the IIR bit will momentarily go low, then return high to indicate there is another interrupt pending

Value	Name	Description	Project
0b	Condition Not Detected	Interrupt Condition Not Detected	All
1b	Condition Detected	Interrupt Condition Detected (may or may not have generated a CPU interrupt)	All

IER – Interrupt Enable Register

MMIO Address Offset: 4_401Ch

Description: Interrupt Enable Register

IER	
Register Type:	MMIO
Project:	All
Default Value:	00000000h
Access Type:	R/W
Size (in bits):	32

See the interrupt bit definition tables to find the source event for each interrupt bit.

Bit	Description
31:0	**Interrupt_Enable_Bits** Project: All The bits in this register enable a CPU interrupt to be generated whenever the corresponding bit in the IIR becomes set. A disabled interrupt will still appear in the IIR register to allow polling of interrupt sources. The DE_IER master interrupt control bit must be set to 1 for any interrupts to propagate to the system.

Value	Name	Description	Project
0b	Disable	Disable	All
1b	Enable	Enable	All

GTLC: "Power Management" Interrupts

The graphics interface routes the GTLC PM writes to the appropriate ISR/IIR registers. The bit assignments are below.

<table>
<tr><th colspan="3">Power Management Interrupt Bit Definition</th></tr>
<tr><td colspan="2">Project:</td><td>All</td></tr>
<tr><td colspan="2">Size (in bits):</td><td>32</td></tr>
<tr><td colspan="3">Power Management interrupt bits come to the graphics interface via direct wires. The GT_IIR and PM_IIR are ORed together to generate the CPU interrupt. The Power Management Interrupt Control Registers all share the same bit definitions from this table.</td></tr>
<tr><th>Bit</th><th colspan="2">Description</th></tr>
<tr><td>31:7</td><td colspan="2">Reserved<table><tr><td>Project:</td><td>Format:</td></tr><tr><td>All</td><td>MBZ</td></tr></table></td></tr>
<tr><td>6</td><td colspan="2">Render Frequency Downward Timeout During RC6 interrupt: This is a write of logic1 via interrupt message from GT via 0x50210 bit6</td></tr>
<tr><td>5</td><td colspan="2">RP UP threshold interrupt: This is a write of logic1 via interrupt message from GT via 0x50210 bit5</td></tr>
<tr><td>4</td><td colspan="2">RP DOWN threshold interrupt: This is a write of logic1 via interrupt message from GT via 0x50210 bit4</td></tr>
<tr><td>3</td><td colspan="2">Reserved<table><tr><td>Project:</td><td>Format:</td></tr><tr><td>All</td><td>MBZ</td></tr></table></td></tr>
<tr><td>2</td><td colspan="2">Render geyserville UP evaluation interval interrupt: This is a write of logic1 via interrupt message from GT via 0x50210 bit2</td></tr>
<tr><td>1</td><td colspan="2">Render geyserville Down evaluation interval interrupt: This is a write of logic1 via interrupt message from GT via 0x50210 bit1</td></tr>
<tr><td>0</td><td colspan="2">Reserved for GT PM unit</td></tr>
</table>

ISR – Interrupt Status Register

MMIO Address Offset: 4_4020h

Description: Interrupt Status Register

ISR	
Register Type:	MMIO
Project:	All
Default Value:	00000000h
Access Type:	Read Only
Size (in bits):	32

See the interrupt bit definition tables to find the source event for each interrupt bit.

Bit	Description
31:0	**Interrupt_Status_Bits** Project: All This field contains the non-persistent values of all interrupt status bits. The IMR register selects which of these interrupt conditions are reported in the persistent IIR.

Value	Name	Description	Project
0b	Condition Doesn't exist	Interrupt Condition currently does not exist	All
1b	Condition Exists	Interrupt Condition currently exists	All

Programming Notes

Some inputs to this register are short pulses; therefore software should not expect to use this register to sample these conditions.

IMR – Interrupt Mask Register

MMIO Address Offset: 4_4024h

Description: Interrupt Mask Register

IMR	
Register Type:	MMIO
Project:	All
Default Value:	FFFFFFFFh
Access Type:	R/W
Size (in bits):	32

For GT command streamer interrupts DO NOT use this register to mask interrupt events. Instead use the individual GT command streamer MASK bits.
For PM interrupts DO NOT use this register to mask interrupt events. Instead use the individual PM MASK bits in the corresponding PMunit register space.
See the interrupt bit definition tables to find the source event for each interrupt bit.

Bit	Description
31:0	**Interrupt_Mask_Bits** Project: All This field contains a bit mask which selects which interrupt bits from the ISR are reported in the IIR.

Value	Name	Description	Project
0b	Not Masked	Not Masked – will be reported in the IIR	All
1b	Masked	Masked – will not be reported in the IIR	All

IIR – Interrupt Identity Register

MMIO Address Offset: 4_4028h

Description: Interrupt Identity Register

IIR	
Register Type:	MMIO
Project:	All
Default Value:	00000000h
Access Type:	R/W Clear
Size (in bits):	32

See the interrupt bit definition tables to find the source event for each interrupt bit.

Bit	Description
31:0	**Interrupt_Identity_Bits** Project: All This field holds the persistent values of the interrupt bits from the ISR which are unmasked by the IMR. If enabled by the IER, bits set in this register will generate a CPU interrupt. Bits set in this register will remain set (persist) until the interrupt condition is cleared by writing a '1' to the appropriate bits. For each bit, the IIR can store a second pending interrupt if two or more of the same interrupt conditions occur before the first condition is cleared. Upon clearing the interrupt, the IIR bit will momentarily go low, then return high to indicate there is another interrupt pending

Value	Name	Description	Project
0b	Condition Not Detected	Interrupt Condition Not Detected	All
1b	Condition Detected	Interrupt Condition Detected (may or may not have generated a CPU interrupt)	All

IER – Interrupt Enable Register

MMIO Address Offset: 4_402Ch

Description: Interrupt Enable Register

IER	
Register Type:	MMIO
Project:	All
Default Value:	00000000h
Access Type:	R/W
Size (in bits):	32

See the interrupt bit definition tables to find the source event for each interrupt bit.

Bit	Description
31:0	**Interrupt_Enable_Bits** Project: All The bits in this register enable a CPU interrupt to be generated whenever the corresponding bit in the IIR becomes set. A disabled interrupt will still appear in the IIR register to allow polling of interrupt sources. The DE_IER master interrupt control bit must be set to 1 for any interrupts to propagate to the system.

Value	Name	Description	Project
0b	Disable	Disable	All
1b	Enable	Enable	All

GTLC: Scratch Registers

The GTLC engine can target these registers with information. The driver is then able to read the registers.

SWF – Software Flags

MMIO Address Offset: 0x4_F000 – 0x4_F08C

Description: These (36 Dword) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

SWF		
Register Type:	MMIO	
Project:	All	
Default Value:	00000000h	
Access Type:	R/W	
Size (in bits):	36x32	
These registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.		
Dword	**Bit**	**Description**
0..35	31:0	**Software_Flags** Project: All

GTSCRATCH – GT Scratch registers

MMIO Address Offset: 0x4_F100 – 0x4_F11F

Description: These (8 Dword) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

GTSCRATCH		
Register Type:	MMIO	
Project:	All	
Default Value:	00000000h	
Access Type:	R/W	
Size (in bits):	8x32	
These registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.		
Dword	**Bit**	**Description**
0..7	31:0	**GT_Scratchpad** Project: All