Intel® Open Source HD Graphics Programmers' Reference Manual (PRM)

Volume 14: Observability Performance Counters

For the 2014-2015 Intel Atom™ Processors, Celeron™ Processors and Pentium™ Processors based on the "Cherry Trail/Braswell" Platform (Cherryview/Braswell graphics)

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Notices and Disclaimers

Table of Contents

Trace

This section contains the following contents:

- Performance Visibility

Performance Visibility

Motivation For Hardware-Assisted Performance Visibility

As the focus on GFX performance and programmability has increased over time, the need for hardware (HW) support to rapidly identify bottlenecks in HW and efficiently tune the work sent to same has become correspondingly important. This part of the PRM describes the HW support for Performance Visibility.

HW Support

This section contains various reporting counters and registers for hardware support for Performance Visibility.

Performance Counter Registers

The following Performance Statistics registers must be part of the power context:

OAPERF_A0 - Aggregate Perf Counter A0

OAPERF_A0_UPPER - Aggregate Perf Counter A0 Upper DWord

OAPERF_A1 - Aggregate Perf Counter A1

OAPERF_A1_UPPER - Aggregate Perf Counter A1 Upper DWord

OAPERF_A2 - Aggregate Perf Counter 2

OAPERF_A2_UPPER - Aggregate Perf Counter A2 Upper DWord

OAPERF_A3 - Aggregate Perf Counter A3

OAPERF_A3_UPPER - Aggregate Perf Counter A3 Upper DWord

OAPERF_A4 - Aggregate Perf Counter A4

OAPERF_A4_UPPER - Aggregate Perf Counter A4 Upper DWord

OAPERF_A5 - Aggregate Perf Counter A5

OAPERF_A5_UPPER - Aggregate Perf Counter A5 Upper DWord

OAPERF_A6 - Aggregate Perf Counter A6

OAPERF_A6_UPPER - Aggregate Perf Counter A6 Upper DWord

OAPERF_A7 - Aggregate Perf Counter A7

OAPERF_A8 - Aggregate Perf Counter A8

OAPERF_A8_UPPER - Aggregate Perf Counter A8 Upper DWord

OAPERF_A9 - Aggregate Perf Counter A9

OAPERF_A9_UPPER - Aggregate Perf Counter A9 Upper DWord

OAPERF_A10 - Aggregate Perf Counter A10

OAPERF_A10_UPPER - Aggregate Perf Counter A10 Upper DWord

OAPERF_A11 - Aggregate Perf Counter A11

OAPERF_A11_UPPER - Aggregate Perf Counter A11 Upper DWord

OAPERF_A12 - Aggregate Perf Counter A12

OAPERF_A12_UPPER - Aggregate Perf Counter A12 Upper DWord

OAPERF_A13 - Aggregate Perf Counter A13

OAPERF_A13_UPPER - Aggregate Perf Counter A13 Upper DWord

OAPERF_A14 - Aggregate Perf Counter A14

OAPERF_A14_UPPER - Aggregate Perf Counter A14 Upper DWord

OAPERF_A15 - Aggregate Perf Counter A15

OAPERF_A15_UPPER - Aggregate Perf Counter A15 Upper DWord

OAPERF_A16 - Aggregate Perf Counter A16

OAPERF_A16_UPPER - Aggregate Perf Counter A16 Upper DWord

OAPERF_A17 - Aggregate Perf Counter A17

OAPERF_A17_UPPER - Aggregate Perf Counter A17 Upper DWord

OAPERF_A18 - Aggregate Perf Counter A18

OAPERF_A18_UPPER - Aggregate Perf Counter A18 Upper DWord

OAPERF_A19 - Aggregate Perf Counter A19

OAPERF_A19_UPPER - Aggregate Perf Counter A19 Upper DWord

OAPERF_A20 - Aggregate Perf Counter A20

OAPERF_A20_UPPER - Aggregate Perf Counter A20 Upper DWord

OAPERF_A21 - Aggregate Perf Counter A21

OAPERF_A21_UPPER - Aggregate Perf Counter A21 Upper DWord

OAPERF_A22 - Aggregate Perf Counter A22

OAPERF_A22_UPPER - Aggregate Perf Counter A22 Upper DWord

OAPERF_A23 - Aggregate Perf Counter A23

OAPERF_A23_UPPER - Aggregate Perf Counter A23 Upper DWord

OAPERF_A24 - Aggregate Perf Counter A24

OAPERF_A24_UPPER - Aggregate Perf Counter A24 Upper DWord

OAPERF_A25 - Aggregate Perf Counter A25

OAPERF_A25_UPPER - Aggregate Perf Counter A25 Upper DWord

OAPERF_A26 - Aggregate Perf Counter A26

OAPERF_A26_UPPER - Aggregate Perf Counter A26 Upper DWord

OAPERF_A27 - Aggregate Perf Counter A27

OAPERF_A27_UPPER - Aggregate Perf Counter A27 Upper DWord

OAPERF_A28 - Aggregate Perf Counter A28

OAPERF_A28_UPPER - Aggregate Perf Counter A28 Upper DWord

OAPERF_A29 - Aggregate Perf Counter A29

OAPERF_A29_UPPER - Aggregate Perf Counter A29 Upper DWord

OAPERF_A30 - Aggregate Perf Counter A30

OAPERF_A30_UPPER - Aggregate Perf Counter A30 Upper DWord

OAPERF_A31 - Aggregate_Perf_Counter_A31

OAPERF_A31_UPPER - Aggregate Perf Counter A31 Upper DWord

OAPERF_A32 - Aggregate_Perf_Counter_A32

OAPERF_A33 - Aggregate_Perf_Counter_A33

OAPERF_A34 - Aggregate_Perf_Counter_A34

OAPERF_A35 - Aggregate_Perf_Counter_A35

OAPERF_B0 - Boolean_Counter_B0

OAPERF_B1 - Boolean_Counter_B1

OAPERF_B2 - Boolean_Counter_B2

OAPERF_B3 - Boolean_Counter_B3

OAPERF_B4 - Boolean_Counter_B4

OAPERF_B5 - Boolean_Counter_B5

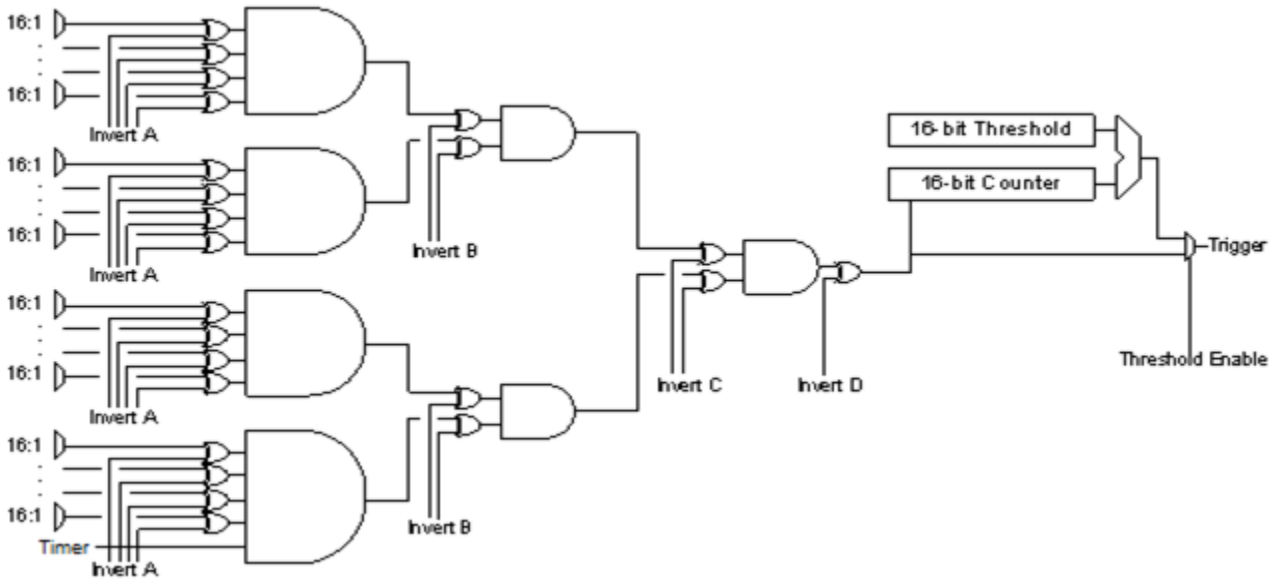
OAPERF_B6 - Boolean_Counter_B6

OAPERF_B7 - Boolean_Counter_B7

Performance Counter Reporting

When either the MI_REPORT_PERF_COUNT command is received or the internal report trigger logic fires, a snapshot of the performance counter values is written to memory. The format used by HW for such reports is selected using the Counter Select field within the OACONTROL register. The organization and number of report formats vary per project and are detailed in the following section. In the following layouts, the RPT_ID is always stored in the lowest addressed DWORD.

OA contains logic to control when performance counter values are reported to memory. This functionality is controlled using the OA report trigger and OA start trigger registers. More detailed register descriptions are included in the Hardware Programming interface. The block diagram below illustrates the logic these registers control.



Note that counters which are 40 bits wide are split in the report format into low DWORD and high byte chunks for simplicity of HW implementation as well as SW-friendly alignment of report data. The performance counter read logically done before writing out report data for these 40-bit counters is guaranteed to be an atomic operation, the counter data is simply swizzled as it is being packed into the report.

MI_REPORT_PERF_COUNT

MI_REPORT_PERF_Count

Aggregating Counters

The table below described the desired high-level functionality from each of the aggregating counters.

Note that there is no counter of 2x2s sent to pixel shader, this is based on the assumption that the pixel shader invocation pipeline statistics counter increments for partially lit 2x2s as well and hence does not require a duplicate performance counter.

Counter #	Event	Description
A0	Render Engine Busy	Render engine is not idle. GPU Busy aggregate counter doesn't increment under the following conditions: 1. Context Switch in Progress. 2. GPU stalled on executing MI_WAIT_FOR_EVENT. 3. GPU stalled on execution MI_SEMAPHORE_MBOX. 4. RCS idle but other parts of GPU active (e.g. only media engines active)
A1	# of Vertex Shader Threads Dispatched	Count of VS threads dispatched to EUs
A2	# of Hull Shader Threads Dispatched	Count of HS threads dispatched to EUs
A3	# of Domain Shader Threads Dispatched	Count of DS threads dispatched to EUs
A4	# of GPGPU Threads Dispatched	Count of GPGPU threads dispatched to EUs
A5	# of Geometry Shader Threads Dispatched	Count of GS threads dispatched to EUs
A6	# of Pixel Shader Threads Dispatched	Count of PS threads dispatched to EUs
A7	Aggregating EU counter 0	User-defined (details in Flexible EU Event Counters section)
A8	Aggregating EU counter 1	User-defined (details in Flexible EU Event Counters section)
A9	Aggregating EU counter 2	User-defined (details in Flexible EU Event Counters section)
A10	Aggregating EU counter 3	User-defined (details in Flexible EU Event Counters section)
A11	Aggregating EU counter 4	User-defined (details in Flexible EU Event Counters section)

Counter #	Event	Description
A12	Aggregating EU counter 5	User-defined (details in Flexible EU Event Counters section)
A13	Aggregating EU counter 6	User-defined (details in Flexible EU Event Counters section)
A14	Aggregating EU counter 7	User-defined (details in Flexible EU Event Counters section)
A15	Aggregating EU counter 8	User-defined (details in Flexible EU Event Counters section)
A16	Aggregating EU counter 9	User-defined (details in Flexible EU Event Counters section)
A17	Aggregating EU counter 10	User-defined (details in Flexible EU Event Counters section)
A18	Aggregating EU counter 11	User-defined (details in Flexible EU Event Counters section)
A19	Aggregating EU counter 12	User-defined (details in Flexible EU Event Counters section)
A20	Aggregating EU counter 13	User-defined (details in Flexible EU Event Counters section)
A21	2x2s Rasterized	Count of the number of samples of 2x2 pixel blocks generated from the input geometry before any pixel-level tests have been applied. (Please note that 2x2s may be in terms of pixels or in terms of samples depending on project but are consistent between A21-A27.)
A22	2x2s Failing Fast pre-PS Tests	Count of the number of samples failing fast "early" (i.e. before pixel shader execution) tests (counted at 2x2 granularity). (Please note that 2x2s may be in terms of pixels or in terms of samples depending on project but are consistent between A21-A27.)
A23	2x2s Failing Slow pre-PS Tests	Count of the number of samples of failing slow "early" (i.e. before pixel shader execution) tests (counted at 2x2 granularity). (Please note that 2x2s may be in terms of pixels or in terms of samples depending on project but are consistent between A21-A27.) If a 2x2 sample partially fails the Z/STC test (i.e some pixels fail and some pixels pass), the OA slow fail counter value will be incorrect.
A24	2x2s Killed in PS	Number of samples entirely killed in the pixel shader as a result of explicit instructions in the kernel (counted in 2x2 granularity). (Please note that 2x2s may be in terms of pixels or in terms of samples depending on project but are consistent between A21-A27.) Behavior of this counter changes when MSAA is enabled based on PS dispatch mode (per-sample versus per-pixel). This leads to discrepancies in how A24/A25 increment versus how A21-A23 and A26/A27 increment when both MSAA and per-pixel PS dispatch are enabled. Counter may be inaccurate when pixel shader outputs output mask (e.g. DX11 oMask declaration)

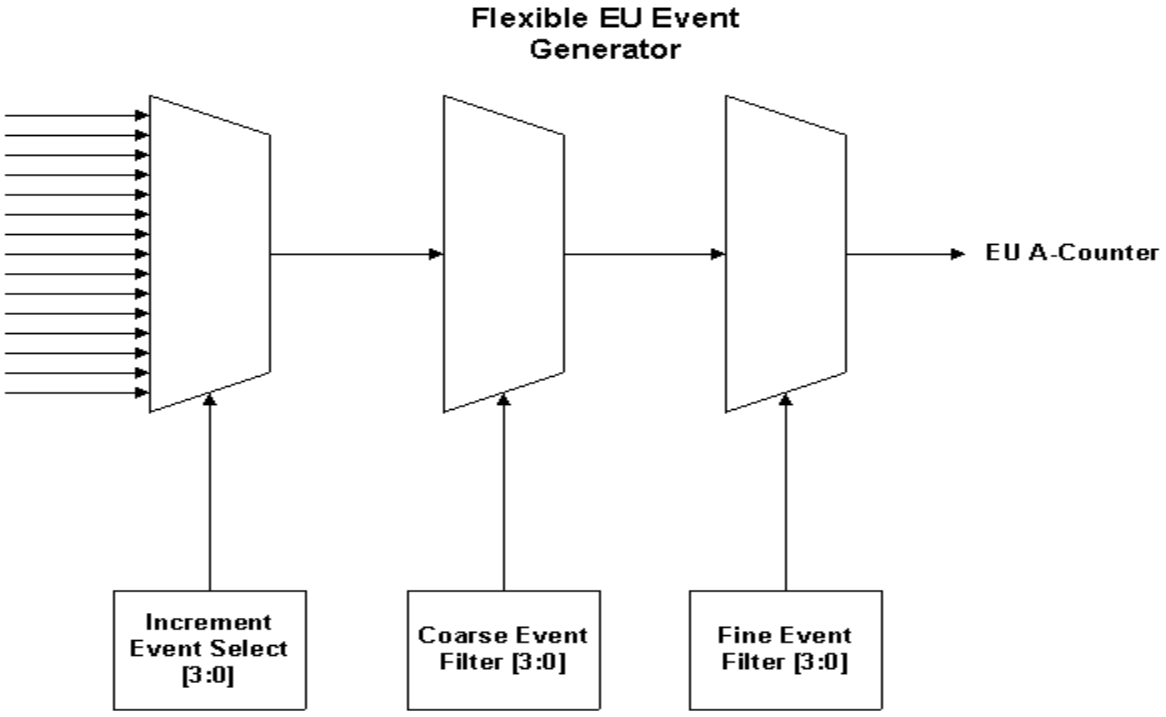
Counter #	Event	Description
A25	2x2s Failing post-PS Tests	Number of samples that entirely fail "late" tests (i.e. tests that can only be performed after pixel shader execution). Counted at 2x2 granularity. (Please note that 2x2s may be in terms of pixels or in terms of samples depending on project but are consistent between A21-A27.) Counter may be inaccurate when pixel shader is allowed to modify output mask (e.g. DX11 oMask declaration) Behavior of this counter changes when MSAA is enabled based on PS dispatch mode (per-sample versus per-pixel). This leads to discrepancies in how A24/A25 increment versus how A21-A23 and A26/A27 increment when both MSAA and per-pixel PS dispatch are enabled.
A26	2x2s Written To Render Target	Number of samples that are written to render target.(counted at 2x2 granularity). MRT case will report multiple writes per 2x2 processed by the pixel shader. (Please note that 2x2s may be in terms of pixels or in terms of samples depending on project but are consistent between A21-A27.)
A27	Blended 2x2s Written to Render Target	Number of samples of blendable that are written to render target.(counted at 2x2 granularity). MRT case will report multiple writes per 2x2 processed by the pixel shader. (Please note that 2x2s may be in terms of pixels or in terms of samples depending on project but are consistent between A21-A27.)
A28	2x2s Requested from Sampler	Aggregated total 2x2 texel blocks requested from all EUs to all instances of sampler logic.
A29	Sampler L1 Misses	Aggregated misses from all sampler L1 caches. Please note that the number of L1 accesses varies with requested filtering mode and in other implementation specific ways. Hence it is not possible in general to draw a direct relationship between A28 and A29. However, a high number of sampler L1 misses relative to texel 2x2s requested frequently degrades sampler performance.
A30	SLM Reads	Total read requests from an EU to SLM (including reads generated by atomic operations).
A31	SLM Writes	Total write requests from an EU to SLM (including writes generated by atomic operations).
A32	Other Shader Memory Accesses	Reserved, can generate per HDC version by looking at (hdc_cput == 1) && (hdc_dest[2:0] == 0b000 || hdc_dest[2:0] == 0b010).
A32	Other Shader Memory Accesses	Aggregated total requests from all EUs to memory surfaces other than render target or texture surfaces (e.g. shader constants).
A34	Atomic Accesses	Aggregated total atomic accesses from all EUs. This counter increments on atomic accesses to both SLM and URB.
A35	Barrier Messages	Aggregated total completed barriers (one per barrier).
A35	Barrier Messages	Aggregated total kernel barrier messages from all Eus (one per thread in barrier).

Flexible EU Event Counters

Since EU performance events are most interesting in many cases when aggregated across all EUs and many interesting EU performance events are limited to certain APIs (e.g. hull shader kernel stats only applicable when running a DX11+ workload), CHV, BSW adds some additional flexibility to the aggregated counters coming from the EU array.

The following block diagram shows the high-level flow that generates each flexible EU event.

Note that no support is provided for differences between flexible EU event programming between EUs because the resulting output from each EU is eventually merged into a single OA counter anyway.



Supported Increment Events

Increment Event	Encoding	Notes
EU FPU0 Pipeline Active	0b0000	Signal that is high on every EU clock where the EU FPU0 pipeline is actively executing a Gen ISA instruction.
		Please note that FPU0 in this EU is the closest match to previous Gen EU's FPU pipe.
EU FPU1 Pipeline Active	0b0001	Signal that is high on every EU clock where the EU FPU1 pipeline is actively executing a Gen ISA instruction.
		Please note that FPU1 in this EU is the closest match to previous Gen EU's EM pipe.
EU SEND Pipeline Active	0b0010	Signal that is high on every EU clock where the EU send pipeline is actively executing a Gen ISA instruction. Only fine event filters 0b0000,0b0101, 0b0110, 0b0111, 0b1000, 0b1001, and 0b1010 are supported with this increment event.
EU FPU0 & FPU1 Pipelines Concurrently Active	0b0011	Signal that is high on every EU clock where the EU FPU0 and FPU1 pipelines are both actively executing a Gen ISA instruction. Only coarse event filters 0b0000, 0b0111, and 0b1000 are supported with this increment event. Only fine event filters 0b0000, 0b0111, 0b1000, 0b1001, and 0b1010 are supported with this increment event.
Some EU Pipeline Active	0b0100	Signal that is high on every EU clock where at least one EU pipeline is actively executing a Gen ISA instruction. Only coarse event filters 0b0000, 0b0111, and 0b1000 are supported with this increment event. Only fine event filters 0b0000,0b0101, 0b0110, 0b0111, 0b1000, 0b1001, and 0b1010 are supported with this increment event.
At Least 1 Thread Loaded But No EU Pipeline Active	0b0101	Signal that is high on every EU clock where at least one thread is loaded but no EU pipeline is actively executing a Gen ISA instruction. Only coarse event filters 0b0000, 0b0111, and 0b1000 are supported with this increment event. Only fine event filters 0b0000, 0b0111, 0b1000, 0b1001, and 0b1010 are supported with this increment event.
Threads loaded integrator == max threads for current HW SKU	0b1000	Implies an accumulator which increases every EU clock by the number of loaded threads, signal pulses high for one clock when the accumulator exceeds a multiple of the number of thread slots (e.g. for a 8-thread EU, signal pulses high every clock where the increment causes a 3-bit accumulator to overflow). Only coarse event filters 0b0000, 0b0111, and 0b1000 are supported with this increment event. Only fine event filters 0b0000, 0b0111, 0b1000, 0b1001, and 0b1010 are supported with this increment event.

Supported Coarse Event Filters

Coarse Event Filter	Encoding	Notes
No mask	0b0000	Never masks increment event.
Currently executing thread came from VS	0b0001	Masks increment event unless the FFID which dispatched the currently executing thread equals FFID of VS.
Currently executing thread came from HS	0b0010	Masks increment event unless the FFID which dispatched the currently executing thread equals FFID of HS.
Currently executing thread came from DS	0b0011	Masks increment event unless the FFID which dispatched the currently executing thread equals FFID of DS.
Currently executing thread came from GS	0b0100	Masks increment event unless the FFID which dispatched the currently executing thread equals FFID of GS.
Currently executing thread came from PS	0b0101	Masks increment event unless the FFID which dispatched the currently executing thread equals FFID of PS.
Currently executing thread came from TS	0b0110	Masks increment event unless the FFID which dispatched the currently executing thread equals FFID of TS.
Row = 0	0b0111	Masks increment event unless the row ID for this EU is 0 (control register is in TDL so only have to check within quarter-slice).
Row = 1	0b1000	Masks increment event unless the row ID for this EU is 1 (control register is in TDL so only have to check within quarter-slice).

Fine Event Filters

Fine Event Filter	Encoding	Notes
None	0b0000	Never mask increment event.
Cycles where hybrid instructions are being executed	0b0001	Masks increment event unless the instruction(s) being executed on the pipeline(s) selected by the increment event are hybrid instructions.
		Filter behaves unreliably when shader ISA uses 64-bit immediate values.
Cycles where ternary instructions are being executed	0b0010	Masks increment event unless the instruction(s) being executed on the pipeline(s) selected by the increment event are ternary instructions.
Cycles where binary instructions are being executed	0b0011	Masks increment event unless the instruction(s) being executed on the pipeline(s) selected by the increment event are binary instructions.
Cycles where mov instructions are being executed	0b0100	Masks increment event unless the instruction(s) being executed on the pipeline(s) selected by the increment event are mov instructions.
Cycles where sends start being executed	0b0101	Masks increment event unless the instruction(s) being executed on the pipeline(s) selected by the increment event are send start of dispatch. Note that if this fine event filter is used in combination with increment events not related to the EU send pipeline (e.g. FPU0 active), the associated flexible event counter will increment in an implementation-specific manner.
EU# = 0b00	0b0111	Masks increment event unless the EU number for this EU is 0b00.
EU# = 0b01	0b1000	Masks increment event unless the EU number for this EU is 0b01.
EU# = 0b10	0b1001	Masks increment event unless the EU number for this EU is 0b10.
EU# = 0b11	0b1010	Masks increment event unless the EU number for this EU is 0b11.