Intel® Iris® Plus Graphics and UHD Graphics Open Source

Programmer's Reference Manual

For the 2019 10th Generation Intel Core™ Processors based on the "Ice Lake" Platform

Volume 2c: Command Reference: Registers
Part 1 – Registers A through L

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Table of Contents

Active Head Pointer Register

ACTHD - Active Head Pointer Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	02074h-02077h
Name:	Active Head Pointer Register
ShortName:	ACTHD_RCSUNIT
Address:	18074h-18077h
Name:	Active Head Pointer Register
ShortName:	ACTHD_POCSUNIT
Address:	22074h-22077h
Name:	Active Head Pointer Register
ShortName:	ACTHD_BCSUNIT
Address:	1C0074h-1C0077h
Name:	Active Head Pointer Register
ShortName:	ACTHD_VCSUNIT0
Address:	1C4074h-1C4077h
Name:	Active Head Pointer Register
ShortName:	ACTHD_VCSUNIT1
Address:	1C8074h-1C8077h
Name:	Active Head Pointer Register
ShortName:	ACTHD_VECSUNIT0
Address:	1D0074h-1D0077h
Name:	Active Head Pointer Register
ShortName:	ACTHD_VCSUNIT2
Address:	1D4074h-1D4077h
Name:	Active Head Pointer Register
ShortName:	ACTHD_VCSUNIT3
Address:	1D8074h-1D8077h
Name:	Active Head Pointer Register
ShortName:	ACTHD_VECSUNIT1
Address:	1E0074h-1E0077h
Name:	Active Head Pointer Register

ACTHD - Active Head Pointer Register

ShortName:	ACTHD_VCSUNIT4
Address:	1E4074h-1E4077h
Name:	Active Head Pointer Register
ShortName:	ACTHD_VCSUNIT5
Address:	1E8074h-1E8077h
Name:	Active Head Pointer Register
ShortName:	ACTHD_VECSUNIT2
Address:	1F0074h-1F0077h
Name:	Active Head Pointer Register
ShortName:	ACTHD_VCSUNIT6
Address:	1F4074h-1F4077h
Name:	Active Head Pointer Register
ShortName:	ACTHD_VCSUNIT7
Address:	1F8074h-1F8077h
Name:	Active Head Pointer Register
ShortName:	ACTHD_VECSUNIT3

This register contains the address details of the data dword being parsed by command streamer.

- When the commands are being executed from a batch buffer this register contains the Dword aligned Graphics Memory Address.
- When the commands are being executed from a ring buffer this register contains the Dword aligned offset in to the ring buffer (offset from Ring Buffer start address).

DWord	Bit	Description
0	31:2	**Head Pointer** Format: GraphicsAddress[31:2] • When the commands are being executed from a batch buffer this register contains the Dword aligned Graphics Memory Address. • When the commands are being executed from a ring buffer this register contains the Dword aligned offset in to the ring buffer (offset from Ring Buffer start address).
	1:0	**Reserved** Format: MBZ

Aggregate_Perf_Counter_A31

OAPERF_A31 - Aggregate_Perf_Counter_A31	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	028F8h

This register reflects the count value of the OA Performance counter A31

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate_Perf_Counter_A32

OAPERF_A32 - Aggregate_Perf_Counter_A32	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02900h

This register reflects the count value of the OA Performance counter A32

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate_Perf_Counter_A33

OAPERF_A33 - Aggregate_Perf_Counter_A33	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02904h

This register reflects the count value of the OA Performance counter A33

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate_Perf_Counter_A34

OAPERF_A34 - Aggregate_Perf_Counter_A34

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02908h

This register reflects the count value of the OA Performance counter A34

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate_Perf_Counter_A35

OAPERF_A35 - Aggregate_Perf_Counter_A35	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0290Ch

This register reflects the count value of the OA Performance counter A35

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A0

OAPERF_A0 - Aggregate Perf Counter A0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Access:	R/W	
Size (in bits):	32	
Address:	02800h	
DWord	**Bit**	**Description**
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Value	Name
0x00000000	**[Default]**
[0x00000001-0xFFFFFFFF]	

Aggregate Perf Counter A0 Upper DWord

OAPERF_A0_UPPER - Aggregate Perf Counter A0 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02804h

This register enables the current live value of performance counter A0 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A1

OAPERF_A1 - Aggregate Perf Counter A1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02808h

This register reflects the count value of the OA Performance counter A1. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A1 Upper DWord

OAPERF_A1_UPPER - Aggregate Perf Counter A1 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0280Ch

This register enables the current live value of performance counter A1 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A2

OAPERF_A2 - Aggregate Perf Counter A2	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02810h

This register reflects the count value of the OA Performance counter A2. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A2 Upper DWord

OAPERF_A2_UPPER - Aggregate Perf Counter A2 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02814h

This register enables the current live value of performance counter A2 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A3

OAPERF_A3 - Aggregate Perf Counter A3	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02818h

This register reflects the count value of the OA Performance counter A3. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A3 Upper DWord

OAPERF_A3_UPPER - Aggregate Perf Counter A3 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0281Ch

This register enables the current live value of performance counter A3 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A4

OAPERF_A4 - Aggregate Perf Counter A4	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02820h

This register reflects the count value of the OA Performance counter A4. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A4 Lower DWord Free

OAPERF_A4_LOWER_FREE - Aggregate Perf Counter A4 Lower DWord Free	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02960h

This register counts the same event as counter A4 however is not affected by context ID or other conditions that prevent A4 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted used this register.

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A4 Upper DWord

OAPERF_A4_UPPER - Aggregate Perf Counter A4 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02824h

This register enables the current live value of performance counter A4 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A4 Upper DWord Free

OAPERF_A4_UPPER_FREE - Aggregate Perf Counter A4 Upper DWord Free	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02964h

This register counts the same event as counter A4 however is not affected by context ID or other conditions that prevent A4 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted using this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A5

OAPERF_A5 - Aggregate Perf Counter A5	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02828h

This register reflects the count value of the OA Performance counter A5. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A5 Upper DWord

OAPERF_A5_UPPER - Aggregate Perf Counter A5 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0282Ch

This register enables the current live value of performance counter A5 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A6

OAPERF_A6 - Aggregate Perf Counter A6	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02830h

This register reflects the count value of the OA Performance counter A6. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A6 Lower DWord Free

OAPERF_A6_LOWER_FREE - Aggregate Perf Counter A6 Lower DWord Free	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02968h

This register counts the same event as counter A6 however is not affected by context ID or other conditions that prevent A6 from incrementing. his counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted used this register.

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A6 Upper DWord

OAPERF_A6_UPPER - Aggregate Perf Counter A6 Upper DWord	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02834h

This register enables the current live value of performance counter A6 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A6 Upper DWord Free

OAPERF_A6_UPPER_FREE - Aggregate Perf Counter A6 Upper DWord Free	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0296Ch

This register counts the same event as counter A6 however is not affected by context ID or other conditions that prevent A6 from incrementing. his counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted using this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A7

OAPERF_A7 - Aggregate Perf Counter A7	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02838h

This register reflects the count value of the OA Performance counter A7. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A7 Upper DWord

OAPERF_A7_UPPER - Aggregate Perf Counter A7 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0283Ch

This register enables the current live value of performance counter A7 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A8

OAPERF_A8 - Aggregate Perf Counter A8	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02840h

This register reflects the count value of the OA Performance counter A8. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A8 Upper DWord

OAPERF_A8_UPPER - Aggregate Perf Counter A8 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02844h

This register enables the current live value of performance counter A8 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A9

OAPERF_A9 - Aggregate Perf Counter A9	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02848h

This register reflects the count value of the OA Performance counter A9. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A9 Upper DWord

OAPERF_A9_UPPER - Aggregate Perf Counter A9 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0284Ch

This register enables the current live value of performance counter A9 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A10

OAPERF_A10 - Aggregate Perf Counter A10	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02850h

This register reflects the count value of the OA Performance counter A10. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A10 Upper DWord

OAPERF_A10_UPPER - Aggregate Perf Counter A10 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02854h

This register enables the current live value of performance counter A10 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A11

OAPERF_A11 - Aggregate Perf Counter A11	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02858h

This register reflects the count value of the OA Performance counter A11. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A11 Upper DWord

OAPERF_A11_UPPER - Aggregate Perf Counter A11 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0285Ch

This register enables the current live value of performance counter A11 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A12

OAPERF_A12 - Aggregate Perf Counter A12	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02860h

This register reflects the count value of the OA Performance counter A12. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A12 Upper DWord

OAPERF_A12_UPPER - Aggregate Perf Counter A12 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02864h

This register enables the current live value of performance counter A12 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A13

OAPERF_A13 - Aggregate Perf Counter A13	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02868h

This register reflects the count value of the OA Performance counter A13. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A13 Upper DWord

OAPERF_A13_UPPER - Aggregate Perf Counter A13 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0286Ch

This register enables the current live value of performance counter A13 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A14

OAPERF_A14 - Aggregate Perf Counter A14	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02870h

This register reflects the count value of the OA Performance counter A14. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A14 Upper DWord

OAPERF_A14_UPPER - Aggregate Perf Counter A14 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02874h

This register enables the current live value of performance counter A14 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A15

OAPERF_A15 - Aggregate Perf Counter A15	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02878h

This register reflects the count value of the OA Performance counter A15. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A15 Upper DWord

OAPERF_A15_UPPER - Aggregate Perf Counter A15 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0287Ch

This register enables the current live value of performance counter A15 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A16

OAPERF_A16 - Aggregate Perf Counter A16	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02880h

This register reflects the count value of the OA Performance counter A16. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A16 Upper DWord

OAPERF_A16_UPPER - Aggregate Perf Counter A16 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02884h

This register enables the current live value of performance counter A16 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A17

OAPERF_A17 - Aggregate Perf Counter A17	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02888h

This register reflects the count value of the OA Performance counter A17. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A17 Upper DWord

OAPERF_A17_UPPER - Aggregate Perf Counter A17 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0288Ch

This register enables the current live value of performance counter A17 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A18

OAPERF_A18 - Aggregate Perf Counter A18	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02890h

This register reflects the count value of the OA Performance counter A9. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A18 Upper DWord

OAPERF_A18_UPPER - Aggregate Perf Counter A18 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02894h

This register enables the current live value of performance counter A18 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A19

OAPERF_A19 - Aggregate Perf Counter A19	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02898h

This register reflects the count value of the OA Performance counter A19. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A19 Lower DWord Free

OAPERF_A19_LOWER_FREE - Aggregate Perf Counter A19 Lower DWord Free	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02970h

This register counts the same event as counter A19 however is not affected by context ID or other conditions that prevent A19 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted used this register.

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A19 Upper DWord

OAPERF_A19_UPPER - Aggregate Perf Counter A19 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0289Ch

This register enables the current live value of performance counter A19 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A19 Upper DWord Free

OAPERF_A19_UPPER_FREE - Aggregate Perf Counter A19 Upper DWord Free

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02974h

This register counts the same event as counter A19 however is not affected by context ID or other conditions that prevent A19 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted using this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A20

OAPERF_A20 - Aggregate Perf Counter A20	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	028A0h

This register reflects the count value of the OA Performance counter A20. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A20 Lower DWord Free

OAPERF_A20_LOWER_FREE - Aggregate Perf Counter A20 Lower DWord Free	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02978h

This register counts the same event as counter A20 however is not affected by context ID or other conditions that prevent A20 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted used this register.

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A20 Upper DWord

OAPERF_A20_UPPER - Aggregate Perf Counter A20 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	028A4h

This register enables the current live value of performance counter A20 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A20 Upper DWord Free

OAPERF_A20_UPPER_FREE - Aggregate Perf Counter A20 Upper DWord Free

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0297Ch

This register counts the same event as counter A20 however is not affected by context ID or other conditions that prevent A20 from incrementing. his counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted using this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A21

OAPERF_A21 - Aggregate Perf Counter A21	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	028A8h

This register reflects the count value of the OA Performance counter A21. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A21 Upper DWord

OAPERF_A21_UPPER - Aggregate Perf Counter A21 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	028ACh

This register enables the current live value of performance counter A21 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A22

OAPERF_A22 - Aggregate Perf Counter A22	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	028B0h

This register reflects the count value of the OA Performance counter A22. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A22 Upper DWord

OAPERF_A22_UPPER - Aggregate Perf Counter A22 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	028B4h

This register enables the current live value of performance counter A22 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A23

OAPERF_A23 - Aggregate Perf Counter A23	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	028B8h

This register reflects the count value of the OA Performance counter A23. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A23 Upper DWord

OAPERF_A23_UPPER - Aggregate Perf Counter A23 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	028BCh

This register enables the current live value of performance counter A23 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A24

OAPERF_A24 - Aggregate Perf Counter A24	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	028C0h

This register reflects the count value of the OA Performance counter A24. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A24 Upper DWord

OAPERF_A24_UPPER - Aggregate Perf Counter A24 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	028C4h

This register enables the current live value of performance counter A24 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A25

OAPERF_A25 - Aggregate Perf Counter A25	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	028C8h

This register reflects the count value of the OA Performance counter A25. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A25 Upper DWord

OAPERF_A25_UPPER - Aggregate Perf Counter A25 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	028CCh

This register enables the current live value of performance counter A25 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A26

OAPERF_A26 - Aggregate Perf Counter A26	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	028D0h

This register reflects the count value of the OA Performance counter A26. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A26 Upper DWord

OAPERF_A26_UPPER - Aggregate Perf Counter A26 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	028D4h

This register enables the current live value of performance counter A26 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A27

OAPERF_A27 - Aggregate Perf Counter A27	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	028D8h

This register reflects the count value of the OA Performance counter A27. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A27 Upper DWord

OAPERF_A27_UPPER - Aggregate Perf Counter A27 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	028DCh

This register enables the current live value of performance counter A27 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A28

OAPERF_A28 - Aggregate Perf Counter A28	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	028E0h

This register reflects the count value of the OA Performance counter A28. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A28 Upper DWord

OAPERF_A28_UPPER - Aggregate Perf Counter A28 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	028E4h

This register enables the current live value of performance counter A28 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A29

OAPERF_A29 - Aggregate Perf Counter A29	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	028E8h

This register reflects the count value of the OA Performance counter A29. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A29 Upper DWord

OAPERF_A29_UPPER - Aggregate Perf Counter A29 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	028ECh

This register enables the current live value of performance counter A29 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A30

OAPERF_A30 - Aggregate Perf Counter A30	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	028F0h

This register reflects the count value of the OA Performance counter A30. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A30 Upper DWord

OAPERF_A30_UPPER - Aggregate Perf Counter A30 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	028F4h

This register enables the current live value of performance counter A30 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A31 Upper DWord

OAPERF_A31_UPPER - Aggregate Perf Counter A31 Upper DWord

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	028FCh

This register enables the current live value of performance counter A31 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:8	**Reserved** Format: PBC
	7:0	**Upper Value** Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

All Engine Fault Register

FAULT_REG - All Engine Fault Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	04094h

DWord	Bit	Description
0	31:1	**All Engine Fault Reg** Default Value: 00000000000000000000000000000000b Access: R/W Bit[31:17]: Reserved. Bit[16:12]: Engine ID: 00000b - GFX. 00001b - MFX0. 00010b - MFX1. 00011b - VEBX. 00100b - BLT. 00110b - WIDI. 00111b - GAM. 01001b - VDBOX2 : For faulted VA, Read 0x5038 / 0x503C (Gen11 Only) 01010b - VDBOX3 : For faulted VA, Read 0x5038 / 0x503C(Gen11 Only) 01011b - VEBOX1 : For faulted VA, Read 0x5038 / 0x503C(Gen11 Only) 10001b - VDBOX4 : Not supported in Gen11 10010b - VDBOX5 : Not supported in Gen11 10011b - VEBOX2 : Not supported in Gen11 11001b - VDBOX6 : Not supported in Gen11 11010b - VDBOX7 : Not supported in Gen11 11011b - VEBOX3 : Not supported in Gen11 01000b - KCR. Bit[11]: Reserved. Bit[10:3]: SRCID of Fault. This is the Source ID of the unit that requested the cycle that generated the First Page fault for this engine. This value is locked and not updated on subsequent faults, until the valid bit of this register is cleared by SW. Bit[2:1]: Fault Type (GFX_FT): Type of Fault recorded: 00b - Invalid PTE Fault. 01b - Invalid PDE Fault. 10b - Invalid PDPE Fault.

FAULT_REG - All Engine Fault Register

		11b - Invalid PML4E Fault. This value is locked and not updated on subsequent faults, until the valid bit of this register is cleared by SW. All bits are only valid with bit[0]=1.
	0	**Valid Bit** Default Value: 0b Access: R/W This bit indicates that the first fault for this engine has been recorded. It can only be cleared by SW, which also clears the other fields.

ARAT C6 Disallow Threshold

ARAT_C6DIS - ARAT C6 Disallow Threshold		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	0A178h	
DWord	**Bit**	**Description**
0	31:0	**C6 Disallow Threshold for ARAT** Access: R/W Threshold, in 10ns increments to prevent short C6.

ARAT Delta (LSB)

ARAT_TDELTA_LOW - ARAT Delta (LSB)		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	0A174h	
DWord	**Bit**	**Description**
0	31:2	**Lower Bits of Delta Time for ARAT** Access: R/W Bits [31:2] of Delta Time, in 10ns increments. Bits 1:0 dropped. This means the granularity is 40ns increments. For example, [31:2]=b1 means the delta time is 40ns.
	1	**ARAT Mode** Access: R/W 0b: One-Shot Mode (default). 1b: Periodic Mode.
	0	**ARAT Enable** Access: R/W 0b: ARAT Disabled (default). 1b: ARAT Enabled.

ARB_CTL

ARB_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	45000h-45003h
Name:	Display Arbitration Control 1
ShortName:	ARB_CTL
Power:	PG0
Reset:	soft

DWord	Bit	Description
0	31	**FBC Memory Wake** Setting this bit allows FBC compressed write requests to wake memory. Value: 1b — Name: Wake On **[Default]** Value: 0b — Name: Wake Off
	30	**Reserved**
	29	**Reserved**
	28:26	**HP Queue Watermark** The value in this register indicates the number of entries the high priority queue should have before it can be read. The value is zero based. Program the values as N-1, where 3'b011 indicates 4 entries. Value: 011b — Name: 4 entries **[Default]** Value: [0,7] — Name:
	25:24	**LP Write Request Limit** The value in this register indicates the maximum number of back to back LP write requests that will be accepted from a single client before re-arbitrating. Value: 00b — Name: 1 Value: 01b — Name: 2 Value: 10b — Name: 4 **[Default]** Value: 11b — Name: 8
	23:20	**TLB Request Limit** The value in this register indicates the maximum number of TLB requests that can be made in an arbitration loop. Zero is not a valid programming.

ARB_CTL

Value	Name
0110b	6 **[Default]**
[1,15]	

19:16 **TLB Request InFlight Limit**

The value in this register indicates the maximum number of TLB (or VTd) requests that can be in flight at any given time. Zero is not a valid programming.

Value	Name
0110b	6 **[Default]**
[1,15]	

15 **FBC Watermark Disable**

Setting this bit disables the FBC watermarks.

Value	Name
0b	Enable
1b	Disable

14:13 **Tiled Address Swizzling**

DRAM configuration registers show if memory address swizzling is needed.

Value	Name	Description
00b	No Display	No display request address swizzling
01b	Reserved	Address bit[6] swizzling for tiled surfaces is not used
10b	Reserved	
11b	Reserved	

12:8 **HP Page Break Limit**

The value in this register represents the maximum number of page breaks allowed in a HP request chain. Zero is not a valid programming.

Value	Name
10000b	16 **[Default]**
[1,31]	

7 **Reserved**

6:0 **HP Data Request Limit**

The value in this register represents the maximum number of cachelines allowed in a HP request chain.

Value	Name
1010110b	86 **[Default]**
[1,127]	

Restriction
This value must always be programmed greater than 8.

ARB_CTL2

ARB_CTL2

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	45004h-45007h
Name:	Display Arbitration Control 2
ShortName:	ARB_CTL2
Power:	PG0
Reset:	soft

DWord	Bit	Description
0	31	**Reserved**
	30	**Reserved** Format: MBZ
	29:28	**LP WD Write Request Limit** The value in this register indicates the maximum number of back to back LP write requests that will be accepted from WD before re-arbitrating. Value / Name: 00b: 1 01b: 2 10b: 4 **[Default]** 11b: 8
	27:25	**Reserved** Format: MBZ
	24:20	**Reserved** Format: MBZ
	19:18	**Par5 Request Limit** This field sets the maximum number of par5 requests before arbitration switches to another client. Value / Name: 00b: 1 01b: 2 10b: 4 **[Default]** 11b: 16
	17:16	**FBC Request Limit**

ARB_CTL2

This field sets the maximum number of FBC requests before arbitration switches to another client.

Value	Name
00b	1
01b	2 **[Default]**
10b	4
11b	8

15 **Reserved**

Format:	MBZ

14 **Reserved**

Format:	MBZ

13 **Reserved**

12 **Arbiter Trickle Feed Allow On HP Request**

If enabled, Arbiter will allow trickle feed request from all clients if any of the client sends a high priority request

Value	Name
0b	Disable **[Default]**
1b	Enable

11 **Reserved**

10:9 **Inflight LP Read Request Limit**

The value in this register represents the maximum number of LP read request transactions that can be inflight at any given time.

Value	Name
00b	1 LP
01b	2 LP
10b	3 LP
11b	4 LP **[Default]**

8 **Reserved**

Format:	MBZ

7 **Reserved**

Format:	MBZ

6 **Reserved**

Format:	MBZ

5:4 **Inflight HP Read Request Limit**

The value in this register represents the maximum number of HP read request transactions that can be inflight at any given time.

Value	Name

ARB_CTL2

	00b	128 HP
	01b	64 HP
	10b	32 HP
	11b	16 HP

3 Enable IPC

Enables the Isochronous Priority Control. If enabled, Display sends demoted requests once the transition watermark is reached. If transition watermark is not enabled, Display sends demoted requests when the display buffer is full.

Value	Name
0b	Disable
1b	Enable

2 Reserved

Format:	MBZ

1:0 RTID FIFO Watermark

The value in this register represents the watermark value for the RTID FIFO. HP transactions will start only when the FIFO level is above or equal the watermark.

Value	Name
00b	8 RTIDs
01b	16 RTIDs
10b	32 RTIDs
11b	Reserved

AUD_CONFIG_2

AUD_CONFIG_2	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	65004h-65007h
Name:	Audio Configuration Register 2 Transcoder A
ShortName:	AUD_TCA_CONFIG_2
Power:	off/on
Reset:	soft
Address:	65104h-65107h
Name:	Audio Configuration Register 2 Transcoder B
ShortName:	AUD_TCB_CONFIG_2
Power:	off/on
Reset:	soft
Address:	65204h-65207h
Name:	Audio Configuration Register 2 Transcoder C
ShortName:	AUD_TCC_CONFIG_2
Power:	off/on
Reset:	soft

This is a new register to add 297 and 584MHz frequencies support for HDMI TMDS clocks. These are programmed along with the other lower bits of the N and CTS values in the Audio Config register. There is one instance of this register per transcoder A/B/C. Each Transcoder is independent of the other.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:12	**Reserved**
	11:8	**Upper bits for N value** These are bits are concatenated as the upper 4 bits to the N value in the AUD_CONFIG register. Please note that the transcoder to which audio is attached must be disabled when changing this field. See bit 29 description for default values
	7:4	**Reserved**
	3:0	**Upper bits for MCTS value** These are the upper 4bits concatenated to CTS or M generation for CTM modes.

AUD_CONFIG

AUD_CONFIG	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	65000h-65003h
Name:	Audio Configuration Transcoder A
ShortName:	AUD_TCA_CONFIG
Power:	off/on
Reset:	soft
Address:	65100h-65103h
Name:	Audio Configuration Transcoder B
ShortName:	AUD_TCB_CONFIG
Power:	off/on
Reset:	soft
Address:	65200h-65203h
Name:	Audio Configuration Transcoder C
ShortName:	AUD_TCC_CONFIG
Power:	off/on
Reset:	soft

This register configures the audio output. There is one instance of this register per transcoder A/B/C. Each Transcoder is independent of the other.

DWord	Bit	Description
0	31:30	**Reserved**
	29	**N value Index** Value / Name / Description 0b / HDMI **[Default]** / N value read on bits 27:20 and 15:4 reflects HDMI N value. Bits 27:20 and 15:4 are programmable to any N value. Default h7FA6 when bit 28 is not set. 1b / DisplayPort / N value read on bits 27:20 and 15:4 reflects DisplayPort N value. Set this bit to 1 before programming N value register. When this bit is set to 1, 27:20 and 15:4 will reflect the current N value. Default is h8000 when bit 28 is not set.
	28	**N programming enable** This bit enables programming of N values for non-CEA modes. Please note that the transcoder to which audio is attached must be disabled when changing this field.
	27:20	**Upper N value**

		Default Value: 00000111b These are bits [19:12] of programmable N values for non-CEA modes. Bit 29 of this register must also be written in order to enable programming. Please note that the transcoder to which audio is attached must be disabled when changing this field. See bit 29 description for default values.
	19:16	**Pixel Clock HDMI** This is the target frequency of the CEA/HDMI video mode to which the audio stream is added. This value is used for generating N_CTS packets. This refers to only HDMI Pixel clock and does not refer to DisplayPort Link clock. DisplayPort Link clock does not require this programming. Note: The transcoder on which audio is attached must be disabled when changing this field.

Value	Name	Description
0b	**[Default]**	
0000b	25.2 / 1.001 MHz	25.2 / 1.001 MHz
0001b	25.2 MHz	25.2 MHz (Program this value for pixel clocks not listed in this field)
0010b	27 MHz	27 MHz
0011b	27 * 1.001 MHz	27 * 1.001 MHz
0100b	54 MHz	54 MHz
0101b	54 * 1.001 MHz	54 * 1.001 MHz
0110b	74.25 / 1.001 MHz	74.25 / 1.001 MHz
0111b	74.25 MHz	74.25 MHz
1000b	148.5 / 1.001 MHz	148.5 / 1.001 MHz
1001b	148.5 MHz	148.5 MHz
Others	Reserved	Reserved

	15:4	**Lower N value** Default Value: 111110100110b These are bits [11:0] of programmable N values for non-CEA modes. Bit 29 of this register must also be written in order to enable programming. Please note that the transcoder to which audio is attached must be disabled when changing this field. See bit 29 description for default values
	3	**Reserved**
	2:0	**Reserved**

AUD_CONFIG_BE

AUD_CONFIG_BE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	65EF0h-65EF3h
Name:	Audio Config Register for Dacbeunit
ShortName:	AUD_CONFIG_BE
Power:	off/on
Reset:	soft

DWord	Bit	Description
0	31:25	**Spare Bits** Access: R/W
	24	**Delay sample count latch Pipe A** Access: R/W Pipe A Hblank SM arc delay for samplecount. Value / Name / Description: 0b / Delay by 16 clocks **[Default]** / When set to 0, sample count latch is delayed by 16 clocks after Hblank starts. 1b / Delay by 32 clocks / When set to 1, sample count latch is delayed by 32 clocks after Hblank starts.
	23	**Delay sample count latch Pipe B** Access: R/W Pipe B Hblank SM arc delay for samplecount. Value / Name / Description: 0b / Delay by 16 clocks **[Default]** / When set to 0, sample count latch is delayed by 16 clocks after Hblank starts. 1b / Delay by 32 clocks / When set to 1, sample count latch is delayed by 32 clocks after Hblank starts.
	22	**Delay sample count latch Pipe C** Access: R/W Pipe C Hblank SM arc delay for samplecount. Value / Name / Description: 0b / Delay by 16 clocks **[Default]** / When set to 0, sample count latch is delayed by 16 clocks after Hblank starts. 1b / Delay by 32 clocks / When set to 1, sample count latch is delayed by 32 clocks

AUD_CONFIG_BE

			after Hblank starts.	

21:18 Reserved

17:15 HBlank_start count for Pipe C

Access:	R/W

The number of tcclk cycles that Hblank early is generated.

Value	Name	Description
000b	Delay of 8 tccclks	Hblank is generated 8 tcclks early.
001b	Delay of 16 tccclks	Hblank is generated 16 tcclks early.
010b	Delay of 32 tccclks **[Default]**	Hblank is generated 32 tcclks early.
011b	Delay of 64 tccclks	Hblank is generated 64 tcclks early.
100b	Delay of 96 tccclks	Hblank is generated 96 tcclks early.
101b	Delay of 128 tccclks	Hblank is generated 128 tcclks early.

14 DP Mixer Mainstream priority enable for Pipe C

Access:	R/W

When set, this will prioritize sending of mainstream data. No Timestamps/DIPs can be sent when there is mainstream data to send except in lines 2-7 of the vblank..

13:12 Number of samples per line for Pipe C

Access:	R/W

When prorgammed to non zero value, this field determines how many samples are sent per line. This is to avoid the audio overflow for high resolutions with small hblanks regions.

Value	Name	Description
00b	All Samples available in buffer **[Default]**	When set to this value, all the collected samples in the buffer are unloaded on the line in the hblank region.
01b	1 sample per line	When set to this value, maximum of one sample(each sample has 2 channels data for layout0 and 8 channels data in layout 1 mode) in the buffer is unloaded on the line in the hblank region.
10b	2 sample per line	When set to this value, maximum of two samples(each sample has 2 channels data for layout0 and 8 channels data in layout 1 mode) in the buffer are unloaded on the line in the hblank region.

11:9 HBlank_start count for Pipe B

Access:	R/W

The number of tcclk cycles that Hblank early is generated.

Value	Name	Description
000b	Delay of 8 tcbclks	Hblank is generated 8 tcclks early.
001b	Delay of 16 tcbclks	Hblank is generated 16 tcclks early.
010b	Delay of 32 tcbclks **[Default]**	Hblank is generated 32 tcclks early.
011b	Delay of 64 tcbclks	Hblank is generated 64 tcclks early.

AUD_CONFIG_BE

	100b	Delay of 96 tcbclks	Hblank is generated 96 tcclks early.
	101b	Delay of 128 tcbclks	Hblank is generated 128 tcclks early.

8 — DP Mixer Mainstream priority enable for Pipe B

Access:	R/W

When set, this will prioritize sending of mainstream data. No Timestamps/DIPs can be sent when there is mainstream data to send except in lines 2-7 of the vblank..

7:6 — Number of samples per line for Pipe B

Access:	R/W

When prorgammed to non zero value, this field determines how many samples are sent per line. This is to avoid the audio overflow for high resolutions with small hblanks regions.

Value	Name	Description
00b	All Samples available in buffer **[Default]**	When set to this value, all the collected samples in the buffer are unloaded on the line in the hblank region.
01b	1 sample per line	When set to this value, maximum of one sample(each sample has 2 channels data for layout0 and 8 channels data in layout 1 mode) in the buffer is unloaded on the line in the hblank region.
10b	2 sample per line	When set to this value, maximum of two samples(each sample has 2 channels data for layout0 and 8 channels data in layout 1 mode) in the buffer are unloaded on the line in the hblank region.

5:3 — HBlank_start count for Pipe A

Access:	R/W

The number of tcclk cycles that Hblank early is generated.

Value	Name	Description
000b	Delay of 8 tcaclks	Hblank is generated 8 tcclks early.
001b	Delay of 16 tcaclks	Hblank is generated 16 tcclks early.
010b	Delay of 32 tcaclks **[Default]**	Hblank is generated 32 tcclks early.
011b	Delay of 64 tcaclks	Hblank is generated 64 tcclks early.
100b	Delay of 96 tcaclks	Hblank is generated 96 tcclks early.
101b	Delay of 128 tcaclks	Hblank is generated 128 tcclks early.

2 — DP Mixer Mainstream priority enable for Pipe A

Access:	R/W

When set, this will prioritize sending of mainstream data. No Timestamps/DIPs can be sent when there is mainstream data to send except in lines 2-7 of the vblank..

1:0 — Number of samples per line for Pipe A

Access:	R/W

When prorgammed to non zero value, this field determines how many samples are sent per line. This is to avoid the audio overflow for high resolutions with small hblanks regions.

AUD_CONFIG_BE

Value	Name	Description
00b	All Samples available in buffer **[Default]**	When set to this value, all the collected samples in the buffer are unloaded on the line in the hblank region.
01b	1 sample per line	When set to this value, maximum of one sample(each sample has 2 channels data for layout0 and 8 channels data in layout 1 mode) in the buffer is unloaded on the line in the hblank region.
10b	2 sample per line	When set to this value, maximum of two samples(each sample has 2 channels data for layout0 and 8 channels data in layout 1 mode) in the buffer are unloaded on the line in the hblank region.

AUD_DIP_ELD_CTRL_ST

AUD_DIP_ELD_CTRL_ST	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	650B4h-650B7h
Name:	Audio Control State for DIP and ELD Transcoder A
ShortName:	AUD_TCA_DIP_ELD_CTRL_ST
Power:	off/on
Reset:	soft
Address:	651B4h-651B7h
Name:	Audio Control State for DIP and ELD Transcoder B
ShortName:	AUD_TCB_DIP_ELD_CTRL_ST
Power:	off/on
Reset:	soft
Address:	652B4h-652B7h
Name:	Audio Control State for DIP and ELD Transcoder C
ShortName:	AUD_TCC_DIP_ELD_CTRL_ST
Power:	off/on
Reset:	soft

There is one instance of this register per transcoder A/B/C.

DWord	Bit	Description
0	31:29	**DIP Port Select** Access: RO This read-only bit reflects which port is used to transmit the DIP data. This can only change when DIP is disabled. If one or more audio-related DIP packets is enabled and audio is enabled on a digital port, these bits will reflect the digital port to which audio is directed. For DP MST, this is the device select/pipe select.

Value	Name	Description
000b	Reserved **[Default]**	Reserved
001b	Digital Port B	Digital Port B
010b	Digital Port C	Digital Port C
011b	Digital Port D	Digital Port D
100b	Digital Port E	Digital Port E
101b	Digital Port F	Digital Port F

AUD_DIP_ELD_CTRL_ST

28:25 **Reserved**

Format:	MBZ

24:21 **DIP type enable status**

Access:	RO

These bits reflect the DIP types enabled. It can be updated while the port is enabled. Within 2 vblank periods, the DIP is guaranteed to have been transmitted. Disabling a DIP type results in setting the contents of that DIP buffer to zero. A reserved setting reflects a disabled DIP.

Value	Name	Description
0000b	**[Default]**	
XXX0b	DIP Disable	Audio DIP disabled
XXX1b	DIP Enable	Audio DIP enabled
XX0Xb	ACP Disable	Generic 1 (ACP) DIP disabled
XX1Xb	ACP Enable	Generic 1 (ACP) DIP enabled
X0XXb	Generic 2 Disable	Generic 2 DIP disabled
X1XXb	Generic 2 Enable	Generic 2 DIP enabled, can be used by ISRC1 or ISRC2
1XXXb	Reserved	Reserved

20:18 **DIP buffer index**

This field is used during read of different DIPs, and during read or write of ELD data. These bits are used as an index to their respective DIP or ELD buffers. When the index is not valid, the contents of the DIP will return all 0s.

Value	Name	Description
000b	Audio **[Default]**	Audio DIP (31 bytes of address space, 31 bytes of data)
001b	Gen 1	Generic 1 (ACP) Data Island Packet (31 bytes of address space, 31 bytes of data)
010b	Gen 2	Generic 2 (ISRC1) Data Island Packet (31 bytes of address space, 31 bytes of data)
011b	Gen 3	Generic 3 (ISRC2) Data Island Packet (31 bytes of address space, 31 bytes of data)
Others	Reserved	Reserved

17:16 **DIP transmission frequency**

Access:	RO

These bits reflect the frequency of DIP transmission for the DIP buffer type designated in bits 20:18. When writing DIP data, this value is also latched when the first DW of the DIP is written. When read, this value reflects the DIP transmission frequency for the DIP buffer designated in bits 20:18.

Value	Name	Description
00b	Disable **[Default]**	Disabled

AUD_DIP_ELD_CTRL_ST

01b	Reserved	Reserved
10b	Send Once	Send Once
11b	Best Effort	Best effort (Send at least every other vsync)

15 Reserved

Format:	MBZ

14:10 ELD buffer size

Default Value:	10101b
Access:	RO

This field reflects the size of the ELD buffer in DWORDs (84 Bytes of ELD)

9:5 ELD access address

Selects the DWORD address for access to the ELD buffer (84 bytes). The value wraps back to zero when incremented past the max addressing value 0x1F. This field change takes effect immediately after being written. The read value indicates the current access address.

4 ELD ACK

Acknowledgement from the audio driver that ELD read has been completed

3:0 DIP access address

Selects the DWORD address for access to the DIP buffers. The value wraps back to zero when it incremented past the max addressing value of 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.

AUD_EDID_DATA

AUD_EDID_DATA	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	65050h-65053h
Name:	Audio EDID Data Block Transcoder A
ShortName:	AUD_TCA_EDID_DATA
Power:	off/on
Reset:	soft
Address:	65150h-65153h
Name:	Audio EDID Data Block Transcoder B
ShortName:	AUD_TCB_EDID_DATA
Power:	off/on
Reset:	soft
Address:	65250h-65253h
Name:	Audio EDID Data Block Transcoder C
ShortName:	AUD_TCC_EDID_DATA
Power:	off/on
Reset:	soft

These registers contain the HDMI/DP data block from the EDID. The graphics driver reads the EDID and writes the structure to these registers. The vendor specific data block may be longer than 8 bytes, but the driver must not write more than 48 bytes to the buffer. The EDID format is Version 3 within the CEA-861B specification. The HDMI/DP Vendor Specific Data Block is described in version 1.1 of the HDMI specification. These values are returned from the device as the HDMI/DP Vendor Specific Data Block response to a Get HDMI/DP Widget command. Writing sequence:

- Video software sets ELD invalid, and sets the ELD access address to 0, or to the desired DWORD to be written.
- Video software writes ELD data 1 DWORD at a time. The ELD access address autoincrements with each DWORD write, wrapping around to address 0 when the max buffer address size of 0xF has been reached.
- Please note that software must write an entire DWORD at a time.
- Please note that the audio driver checks the valid bit with each byte read of the ELD. This means that the video driver can unilaterally write ELD irrespective of audio driver ELD read status.

Reading sequence:

- Video software sets the ELD access address to 0, or to the desired DWORD to be read.
- Video software reads ELD data 1 DWORD at a time. The ELD access address autoincrements with each

AUD_EDID_DATA

DWORD read, wrapping around to address 0 when the max buffer address size of 0xF has been reached.

There is one instance of this register per transcoder A/B/C.

DWord	Bit	Description
0	31:0	**EDID Data Block** Please note that the contents of this buffer are not cleared when ELD is disabled. The contents of this buffer are cleared during FLR.

AUD_FREQ_CNTRL

AUD_FREQ_CNTRL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	65900h-65903h
Name:	Audio BCLK Frequency Control
ShortName:	AUD_FREQ_CNTRL
Power:	off/on
Reset:	soft

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:14	**T-Mode** Indicates the T mode SDI is operating in. BIOS or System Software must pre-program the T-mode register. a. before the iDISPLAY Audio Link is brought out from Link Reset, b. to a value which is consistent with the value of the its counterpart T-mode bit in the Audio Controller. c. to a value which is within the electrical capabilities of the platform. Note that even T modes are prohibited from being used with any BCLK frequency which has an odd number of bit cells. Example, 2T mode is incompatible with BCLK=6MHz (125 bit cells).

Value	Name	Description
00b	4T Default **[Default]**	4T mode with sdi data held for 4 bit clks.
01b	2T	2T Mode with sdi data held for 2 bit clocks. To use 2T mode, the bclk has to be 48MHz and flop in the IO needs to bypass by setting bit 13 of this register. BIOS has to program 48MHz in the controller also to use this mode.
10b	8T	8T Mode with sdi data held for 8 bit clocks.
11b	16T	16T Mode with sdi data held for 16 bit clocks.

	13	**Bypass Flop** Setting this bit will bypass the flop in the IO in the Audout path.

Value	Name	Description
0b	No bypass **[Default]**	Flop in the AUDIO OUT IO is not bypassed.
1b	Bypass	Flop in the AUDIO OUT IO is bypassed.

	12:11	**Detect Frame sync early** These bits are used to pullin the frame sync detection logic earlier to compensate for PV issues if

any. Audio codec starts driving the SDI pin earlier by the number of clocks programmed by this register.

Value	Name	Description
00b	Pull in by 0 bclks	Frame sync is detected at bclk = 1998.
01b	Pull in by 1 bclks	Frame sync is detected at bclk = 1997.
10b	Pull in by 2 bclks	Frame sync is detected at bclk = 1996.
11b	Pull in by 3 bclks	Frame sync is detected at bclk = 1995.

10:5 **Reserved**

Format:	MBZ

4 **96MHz BCLK**

Default Value:	1b

Indicates that iDISPLAY Audio Link will run at 96MHz. This bit is defaulted to 1. BIOS or System Software must pre-program B96 before the iDISPLAY Audio Link is brought out from reset.

3 **48MHz BCLK**

Default Value:	0b

Indicates that iDISPLAY Audio Link will run at 48MHz. This bit is defaulted to 0. BIOS or System Software must pre-program B96 before the iDISPLAY Audio Link is brought out from reset.

2:0 **Reserved**

Format:	MBZ

AUD_INFOFR

AUD_INFOFR	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	65054h-65057h
Name:	Audio Widget Data Island Packet Transcoder A
ShortName:	AUD_TCA_INFOFR
Power:	off/on
Reset:	soft
Address:	65154h-65157h
Name:	Audio Widget Data Island Packet Transcoder B
ShortName:	AUD_TCB_INFOFR
Power:	off/on
Reset:	soft
Address:	65254h-65257h
Name:	Audio Widget Data Island Packet Transcoder C
ShortName:	AUD_TCC_INFOFR
Power:	off/on
Reset:	soft

When the IF type or dword index is not valid, the contents of the DIP will return all 0s.
These values are programmed by the audio driver in an HDMI/DP Widget Set command. They are returned one byte at a time from the device on the HD audio bus as the HDMI/DP DIP response to a Get HDMI/DP Widget command. To fetch a specific byte, the audio driver should send an HDMI/DP Widget HDMI/DP DIP Index Pointer Set command to set the index, then fetch the indexed byte using the HDMI/DP DIP get.

DWord	Bit	Description
0	31:0	**Data Island Packet Data** This reflects the contents of the DIP indexed by the DIP access address. The contents of this buffer are cleared during function reset or HD audio link reset.

AUD_M_CTS_ENABLE

AUD_M_CTS_ENABLE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	65028h-6502Bh
Name:	Audio M and CTS Programming Enable Transcoder A
ShortName:	AUD_TCA_M_CTS_ENABLE
Power:	off/on
Reset:	soft
Address:	65128h-6512Bh
Name:	Audio M and CTS Programming Enable Transcoder B
ShortName:	AUD_TCB_M_CTS_ENABLE
Power:	off/on
Reset:	soft
Address:	65228h-6522Bh
Name:	Audio M and CTS Programming Enable Transcoder C
ShortName:	AUD_TCC_M_CTS_ENABLE
Power:	off/on
Reset:	soft

There is one instance of this register per transcoder A/B/C.

DWord	Bit	Description
0	31:22	**Reserved**
	21	**CTS M value Index** Value / Name / Description 0b / CTS **[Default]** / CTS value read on bits 19:0 reflects CTS value. Bit 19:0 is programmable to any CTS value. default is 0 1b / M / M value read on bits 19:0 reflects DisplayPort M value. Set this bit to 1 before programming M value register. When this is set to 1 19:0 will reflect the current M value
	20	**Enable CTS or M prog** When set will enable CTS or M programming.
	19:0	**CTS programming** These are bits [19:0] of programmable CTS values for non-CEA modes. Bit 21 of this register must also be written in order to enable programming. Please note that the transcoder to which audio is attached must be disabled when changing this field.

AUD_MISC_CTRL

AUD_MISC_CTRL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	65010h-65013h
Name:	Audio Converter 1 Misc Control
ShortName:	AUD_C1_MISC_CTRL
Power:	off/on
Reset:	soft
Address:	65110h-65113h
Name:	Audio Converter 2 Misc Control
ShortName:	AUD_C2_MISC_CTRL
Power:	off/on
Reset:	soft
Address:	65210h-65213h
Name:	Audio Converter 3 Misc Control
ShortName:	AUD_C3_MISC_CTRL
Power:	off/on
Reset:	soft
Address:	65310h-65313h
Name:	Audio Converter 4 Misc Control
ShortName:	AUD_C4_MISC_CTRL
Power:	off/on
Reset:	soft

There is one instance of this register per audio converter 1/2/3.

DWord	Bit	Description
0	31:9	**Reserved** Format: MBZ
	8	**Reserved**
	7:4	**Output Delay** Default Value: 0100b The number of samples between when the sample is received from the HD Audio link and when it appears as an analog signal at the pin.
	3	**Reserved**

AUD_MISC_CTRL

	Format:	MBZ

2 Sample Fabrication EN bit

Access:	R/W

This bit indicates whether internal fabrication of audio samples is enabled during a link underrun.

Value	Name	Description
0b	Disable	Audio fabrication disabled
1b	Enable **[Default]**	Audio fabrication enabled

1 Pro Allowed

Access:	R/W

By default, the audio device is configured to consumer mode and does not allow the mode to be changed to professional mode by an HD Audio verb. When Pro is allowed by setting this configuration bit, the HD Audio codec allows a verb to set the device into professional mode.
Note: Setting this configuration bit does not change the default Pro bit value to be 1. Pro must be set to 1 through the normal process, using a verb.

Value	Name	Description
0b	Consumer **[Default]**	Consumer use only
1b	Professional	Professional use allowed

0 Reserved

Format:	MBZ

AUD_PIN_ELD_CP_VLD

AUD_PIN_ELD_CP_VLD

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	650C0h-650C3h
Name:	Audio Pin ELD and CP Ready Status
ShortName:	AUD_PIN_ELD_CP_VLD
Power:	off/on
Reset:	soft

DWord	Bit	Description
0	31:16	**Reserved**
	15	**Audio InactiveD** Inactive: When this bit is set, a digital display sink device has been attached but not active for streaming audio. **Value** / **Name** / **Description** 0b / Disable / Device is active for streaming audio data 1b / Enable / Device is connected but not active
	14	**Audio Output EnableD** This bit directs audio to the device connected to this transcoder. When enabled along with Inactive set to 0 and audio data is available, the audio data will be combined with the video data and sent over this transcoder. The audio unit uses the status of this bit to indicate presence of the HDMI/DP output to the audio driver. **Value** / **Name** / **Description** 0b / Disable / No Audio output 1b / Valid / Audio is enabled
	13	**CP ReadyD** This R/W bit reflects the state of CP request from the audio unit. When an audio CP request has been serviced, it must be reset to 1 by the video software to indicate that the CP request has been serviced. This is transcoder based. Software should add a delay of 1ms before updating the CP ready bit. This is needed to make sure that all the pending unsolicited responses are cleared (transmitted to HD audio) before CP ready unsolicited responses is generated. This is needed in case of DP MST is enabled and when many changes to PD, ELDV and CP ready bits are done during mode set. **Value** / **Name** / **Description** 0b / Pending or Not Ready / CP request pending or not ready to receive requests.

AUD_PIN_ELD_CP_VLD

	1b	Ready	CP request ready

12	**ELD validD** This R/W bit reflects the state of the ELD data written to the ELD RAM. After writing the ELD data, the video software must set this bit to 1 to indicate that the ELD data is valid. At audio codec initialization, or on a hotplug event, this bit is set to 0 by the video software. This bit is reflected in the audio pin complex widget as the ELD valid status bit. This is transcoder based.

Value	Name	Description
0b	Invalid	ELD data invalid (default, when writing ELD data, set 0 by software)
1b	Valid	ELD data valid (Set by video software only)

11	**Audio InactiveC** Inactive: When this bit is set, a digital display sink device has been attached but not active for streaming audio.

Value	Name	Description
0b	Disable	Device is active for streaming audio data
1b	Enable	Device is connected but not active

10	**Audio Output EnableC** This bit directs audio to the device connected to this transcoder. When enabled along with Inactive set to 0 and audio data is available, the audio data will be combined with the video data and sent over this transcoder. The audio unit uses the status of this bit to indicate presence of the HDMI/DP output to the audio driver.

Value	Name	Description
0b	Disable	No Audio output
1b	Valid	Audio is enabled

9	**CP ReadyC** This R/W bit reflects the state of CP request from the audio unit. When an audio CP request has been serviced, it must be reset to 1 by the video software to indicate that the CP request has been serviced. This is transcoder based. Software should add a delay of 1ms before updating the CP ready bit. This is needed to make sure that all the pending unsolicited responses are cleared (transmitted to HD audio) before CP ready unsolicited responses is generated. This is needed in case of DP MST is enabled and when many changes to PD, ELDV and CP ready bits are done during mode set.

Value	Name	Description
0b	Pending or Not Ready	CP request pending or not ready to receive requests
1b	Ready	CP request ready

8	**ELD validC** This R/W bit reflects the state of the ELD data written to the ELD RAM. After writing the ELD data, the video software must set this bit to 1 to indicate that the ELD data is valid. At audio codec initialization, or on a hotplug event, this bit is set to 0 by the video software. This bit is reflected in the audio pin complex widget as the ELD valid status bit. This is transcoder based.

Value	Name	Description

AUD_PIN_ELD_CP_VLD

0b	Invalid	ELD data invalid (default, when writing ELD data, set 0 by software)
1b	Valid	ELD data valid (Set by video software only)

7 Audio InactiveB

Inactive: When this bit is set, a digital display sink device has been attached but not active for streaming audio.

Value	Name	Description
0b	Disable	Device is active for streaming audio data
1b	Enable	Device is connected but not active

6 Audio Output EnableB

This bit directs audio to the device connected to this transcoder. When enabled along with Inactive set to 0 and audio data is available, the audio data will be combined with the video data and sent over this transcoder. The audio unit uses the status of this bit to indicate presence of the HDMI/DP output to the audio driver. This is transcoder based.

Value	Name	Description
0b	Disable	No audio output
1b	Enable	Audio is enabled

5 CP ReadyB

See CP_ReadyC description.

Value	Name	Description
0b	Not Ready	CP request pending or not ready to receive requests
1b	Ready	CP request ready

4 ELD validB

See ELD_validC descripion.

Value	Name	Description
0b	Invalid	ELD data invalid (default, when writing ELD data, set 0 by software)
1b	Valid	ELD data valid (Set by video software only)

3 Audio InactiveA

Inactive: When this bit is set, a digital display sink device has been attached but not active for streaming audio.

Value	Name	Description
0b	Disable	Device is active for streaming audio data
1b	Enable	Device is connected but not active

2 Audio Output EnableA

This bit directs audio to the device connected to this transcoder. When enabled along with Inactive set to 0 and audio data is available, the audio data will be combined with the video data and sent over this transcoder. The audio unit uses the status of this bit to indicate presence of the HDMI/DP output to the audio driver. This is transcoder based.

Value	Name	Description

AUD_PIN_ELD_CP_VLD

0b	Disable	No audio output
1b	Enable	Audio is enabled

1 — CP ReadyA

See CP_ReadyC description.

Value	Name	Description
0b	Not Ready	CP request pending or not ready to receive requests
1b	Ready	CP request ready

0 — ELD validA

See ELD_validC descripion.

Value	Name	Description
0b	Invalid	ELD data invalid (default, when writing ELD data, set 0 by software)
1b	Valid	ELD data valid (Set by video software only)

AUD_PIN_PIPE_CONN_ENTRY_LNGTH

AUD_PIN_PIPE_CONN_ENTRY_LNGTH	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	650A8h-650ABh
Name:	Audio Connection List Entry and Length Transcoder A
ShortName:	AUD_TCA_PIN_PIPE_CONN_ENTRY_LNGTH_RO
Power:	off/on
Reset:	soft
Address:	651A8h-651ABh
Name:	Audio Connection List Entry and Length Transcoder B
ShortName:	AUD_TCB_PIN_PIPE_CONN_ENTRY_LNGTH_RO
Power:	off/on
Reset:	soft
Address:	652A8h-652ABh
Name:	Audio Connection List Entry and Length Transcoder C
ShortName:	AUD_TCC_PIN_PIPE_CONN_ENTRY_LNGTH_RO
Power:	off/on
Reset:	soft

These values are returned from the device as the Connection List Length response to a Get Pin Widget command or Get Device Widget command if DP MST. There is one instance of this register per transcoder A/B/C.

DWord	Bit	Description
0	31:16	**Reserved**
	15:8	**Connection List Entry** Connection to Convertor Widget Node 0x03
	7	**Long Form** This bit indicates whether the items in the connection list are long form or short form. This bit is hardwired to 0 (items in connection list are short form)
	6:0	**Connection List Length** Default Value: 0000001b This field indicates the number of items in the connection list. If this field is 2, there is only one hardwired input possible, which is read from the Connection List, and there is no Connection Select Control.

AUD_PIPE_CONN_SEL_CTRL

AUD_PIPE_CONN_SEL_CTRL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	650ACh-650AFh
Name:	Audio Pipe Connection Select Control
ShortName:	AUD_PIN_PIPE_CONN_SEL_CTRL_RO
Power:	off/on
Reset:	soft

These values are returned from the device as the Connection List Length response to a Get Pin Widget command or Get Device Widget command for DP MST.

DWord	Bit	Description
0	31:24	**Connection select Control F** Default Value: 0Fh Connection Index Currently Set [Default 0x00], Port F Widget is set to 0x03
	23:16	**Connection select Control D** Connection Index Currently Set [Default 0x00], Port D Widget is set to 0x02 Value: 0Fh — Name: **[Default]**
	15:8	**Connection select Control C** Connection Index Currently Set [Default 0x00], Port C Widget is set to 0x01 Value: 0Fh — Name: **[Default]**
	7:0	**Connection select Control B** Connection Index Currently Set [Default 0x00], Port B Widget is set to 0x00 Value: 0Fh — Name: **[Default]**

AUD_PWRST

AUD_PWRST	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	6504Ch-6504Fh
Name:	Audio Power State Read Only
ShortName:	AUD_PWRST_RO
Power:	off/on
Reset:	soft

These values are returned from the device as the Power State response to a Get Audio Function Group command.

DWord	Bit	Description
0	31:30	**Converter4 Widget PwrSt Curr** Format: **Audio Power State Format** Converter4 Widget current power state Value: 11b — Name:
	29:28	**Converter4 Widget PwrSt Req** Format: **Audio Power State Format** Converter4 Widget power state that was requested by audio software Value: 11b — Name:
	27:26	**Func Grp Dev PwrSt Curr** Format: **Audio Power State Format** Function Group Device current power state Value: 11b — Name:
	25:24	**Func Grp Dev PwrSt Set** Format: **Audio Power State Format** Function Group Device power state that was set Value: 11b — Name:
	23:22	**Converter3 Widget PwrSt Curr** Format: **Audio Power State Format**

AUD_PWRST

		Converter3 Widget current power state **Value** | **Name** 11b |
	21:20	**Converter3 Widget PwrSt Req** Format: **Audio Power State Format** Converter3 Widget power state that was requested by audio software **Value** | **Name** 11b |
	19:18	**Convertor2 Widget PwrSt Curr** Format: **Audio Power State Format** Converor2 Widget current power state **Value** | **Name** 11b |
	17:16	**Convertor2 Widget PwrSt Req** Format: **Audio Power State Format** Converter2 Widget power state that was requested by audio software **Value** | **Name** 11b |
	15:14	**Convertor1 Widget PwrSt Curr** Format: **Audio Power State Format** Converter1 Widget current power state **Value** | **Name** 11b |
	13:12	**Convertor1 Widget PwrSt Req** Format: **Audio Power State Format** Converter1 Widget power state that was requested by audio software **Value** | **Name** 11b |
	11:10	**PinD Widget PwrSt Curr** Format: **Audio Power State Format** PinD Widget current power stateFor DP MST this represents Device3 power state **Value** | **Name** 11b |
	9:8	**PinD Widget PwrSt Set** Format: **Audio Power State Format** PinD Widget power state that was setFor DP MST this represents Device3 power state **Value** | **Name**

AUD_PWRST

	11b	

7:6 PinC Widget PwrSt Curr

Format: **Audio Power State Format**

PinC Widget current power stateFor DP MST this represents Device2 power state

Value	Name
11b	

5:4 PinC Widget PwrSt Set

Format: **Audio Power State Format**

PinC Widget power state that was setFor DP MST this represents Device2 power state

Value	Name
11b	

3:2 PinB Widget PwrSt Curr

Format: **Audio Power State Format**

PinB Widget current power stateFor DP MST this represents Device1 power state

Value	Name
11b	

1:0 PinB Widget PwrSt Set

Format: **Audio Power State Format**

PinB Widget power state that was setFor DP MST this represents Device1 power state

Value	Name
11b	

AUD_RID

AUD_RID	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	65024h-65027h
Name:	Audio Revision ID Read Only
ShortName:	AUD_RID_RO
Power:	off/on
Reset:	soft

These values are returned from the device as the Revision ID response to a Get Root Node command.

DWord	Bit	Description
0	31:24	**Reserved**
	23:20	**Major Revision** Default Value: 1h The major revision number (left of the decimal) of the HD Audio Spec to which the codec is fully compliant. This field is hardwired within the device.
	19:16	**Minor Revision** Default Value: 0h The minor revision number (rights of the decimal) or dot number of the HD Audio Spec to which the codec is fully compliant. This field is hardwired within the device.
	15:8	**Revision ID** Default Value: 00h The vendor revision number for this given Device ID. This field is hardwired within the device.
	7:0	**Stepping ID** Default Value: 00h An optional vendor stepping number within the given Revision ID. This field is hardwired within the device.

AUD_VID_DID

AUD_VID_DID	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	65020h-65023h
Name:	Audio Vendor ID / Device ID Read Only
ShortName:	AUD_VID_DID_RO
Power:	off/on
Reset:	soft

These values are returned from the device as the Vendor ID/ Device ID response to a Get Root Node command.

DWord	Bit	Description
0	31:16	**Vendor ID** Default Value: 8086h Used to identify the codec within the PnP system. This field is hardwired within the device.
	15:8	**Device ID Upper byte** Default Value: 28h Constant used to identify the codec within the PnP system. This field is set by the device hardware.
	7:0	**Device ID Lower byte** Description: Constant used to identify the codec within the PnP system. This field is set by fuse download.

AUDIO_PIN_BUF_CTL

AUDIO_PIN_BUF_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	48414h-48417h
Name:	Audio Pins Buffer Control
ShortName:	AUDIO_PIN_BUF_CTL
Power:	PG0
Reset:	soft

This register controls the display audio pins I/O buffers.

DWord	Bit	Description
0	31	**Enable** This field enables the audio buffer. Value: 0b – Disable; 1b – Enable
	30	**Reserved**
	29:28	**Hysteresis**
	27	**Reserved**
	26:24	**Spare**
	23:21	**Reserved**
	20:16	**Pulldown Strength**
	15:12	**Pulldown Slew**
	11:9	**Reserved**
	8:4	**Pullup Strength**
	3:0	**Pullup Slew**

Audio Codec Interrupt Definition

Audio Codec Interrupt Definition

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	44480h-4448Fh
Name:	Audio Codec Interrupts
ShortName:	AUD_INTERRUPT
Power:	PG0
Reset:	soft

This table indicates which events are mapped to each bit of the Audio Codec Interrupt registers.
0x44480 = ISR
0x44484 = IMR
0x44488 = IIR
0x4448C = IER

DWord	Bit	Description
0	31	**Audio_Power_State_change_DDI_D** The ISR is an active high pulse when there is a power state change for audio for DDI D.
	30	**Audio_Power_State_change_DDI_C** The ISR is an active high pulse when there is a power state change for audio for DDI C.
	29	**Audio_Power_State_change_DDI_B** The ISR is an active high pulse when there is a power state change for audio for DDI B.
	28	**Audio_Power_State_change_WD_0** Description: The ISR is an active high pulse when there is a power state change for audio for WD 0.
	27	**Audio_Power_State_change_WD_1** The ISR is an active high pulse when there is a power state change for audio for WD 1.
	26	**Audio_Function_Group_Power_State_change** The ISR is an active high pulse when there is a power state change for audio of function group widget.
	25	**Audio_Conv1_Power_State_change** The ISR is an active high pulse when there is a power state change for audio of Converter 1 widget.

Audio Codec Interrupt Definition		
	24	**Audio_Conv2_Power_State_change** The ISR is an active high pulse when there is a power state change for audio of Converter 2 widget.
	23	**Audio_Conv3_Power_State_change** The ISR is an active high pulse when there is a power state change for audio of Converter 3 widget.
	22	**Audio_Conv4_Power_State_change** The ISR is an active high pulse when there is a power state change for audio of Converter 4 widget.
	21	**Spare 21**
	20	**Spare 20**
	19	**Spare 19**
	18	**Audio_Ramfull_error_WD_1** The ISR is an active high level indicating an overflow in the Audio Wireless slice 1 RAM.
	17	**Audio_Ramfull_error_WD_0** The ISR is an active high level indicating an overflow in the Audio Wireless slice 0 RAM.
	16	**Reserved**
	15	**Reserved**
	14	**Reserved**
	13	**Reserved**
	12	**Audio_Power_State_change_DDI_E** The ISR is an active high pulse when there is a power state change for audio for DDI E.
	11	**Audio_Power_State_change_DDI_F** The ISR is an active high pulse when there is a power state change for audio for DDI F.
	10:9	**Unused_Int_10_9** These interrupts are currently unused.
	8	**Reserved**
	7	**Reserved**

Audio Codec Interrupt Definition		
	6	**Reserved**
	5	**Reserved**
	4:3	**Unused_Int_4_3** These interrupts are currently unused.
	2	**Reserved**
	1	**Reserved**
	0	**Audio_Mailbox_Write** The ISR is an active high pulse when there is a write to any of the four Audio Mail box verbs in vendor defined node ID 8

Auto Draw End Offset

3DPRIM_END_OFFSET - Auto Draw End Offset	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	32
Address:	02420h-02423h
Name:	Auto Draw End Offset
ShortName:	3DPRIM_END_OFFSET_RCSUNIT_BE_GEOMETRY
Address:	18420h-18423h
Name:	Auto Draw End Offset
ShortName:	3DPRIM_END_OFFSET_POCSUNIT_BE_GEOMETRY
Address:	02420h-02423h
Name:	Auto Draw End Offset
ShortName:	3DPRIM_END_OFFSET_RCSUNIT_BE
Address:	18420h-18423h
Name:	Auto Draw End Offset
ShortName:	3DPRIM_END_OFFSET_POCSUNIT_BE

DWord	Bit	Description
0	31:0	**End Offset** Format: U32 This register is used to store the end offset value used by the Vertex Fetch to determine when to stop processing the 3D_PRIMITIVE command. This register is valid when the End Offset Enable is set in the 3D_PRIMITIVE command.

Auxiliary Table Base Address Higher

AUX_TABLE_BASE_ADDR_HIGH - Auxiliary Table Base Address Higher		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Specified the Upper 32 bits of the Aux table Base address for Memory Compression.;		
DWord	**Bit**	**Description**
0	31:0	**Aux Table Base Address Higher** Default Value: 0000000000000000b

Auxiliary Table Base Address Lower

AUX_TABLE_BASE_ADDR_LOW - Auxiliary Table Base Address Lower		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Specified the Lower 32 bits of the Aux table Base address for Memory Compression.;		
DWord	**Bit**	**Description**
0	31:0	**Aux Table Base Address Lower** Default Value: 0000000000000000b

Batch Address Difference Register

BB_ADDR_DIFF - Batch Address Difference Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02154h-02157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_RCSUNIT
Address:	18154h-18157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_POCSUNIT
Address:	22154h-22157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_BCSUNIT
Address:	1C0154h-1C0157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_VCSUNIT0
Address:	1C4154h-1C4157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_VCSUNIT1
Address:	1C8154h-1C8157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_VECSUNIT0
Address:	1D0154h-1D0157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_VCSUNIT2
Address:	1D4154h-1D4157h

BB_ADDR_DIFF - Batch Address Difference Register

Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_VCSUNIT3

Address:	1D8154h-1D8157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_VECSUNIT1

Address:	1E0154h-1E0157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_VCSUNIT4

Address:	1E4154h-1E4157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_VCSUNIT5

Address:	1E8154h-1E8157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_VECSUNIT2

Address:	1F0154h-1F0157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_VCSUNIT6

Address:	1F4154h-1F4157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_VCSUNIT7

Address:	1F8154h-1F8157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_VECSUNIT3

This register contains the difference between the start of the last batch and where the last initiated Batch Buffer is currently fetching commands.

Programming Notes
Programming Restriction:

BB_ADDR_DIFF - Batch Address Difference Register

This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description
0	31:2	**Batch Buffer Address Difference** Format: GraphicsAddress[31:2] This field specifies the DWord-aligned difference between the starting address of the batch buffer and where the last initiated Batch Buffer is currently fetching commands.
	1:0	**Reserved** Format: MBZ

Batch Buffer Head Pointer Preemption Register

BB_PREEMPT_ADDR - Batch Buffer Head Pointer Preemption Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02148h-0214Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_RCSUNIT
Address:	18148h-1814Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_POCSUNIT
Address:	22148h-2214Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_BCSUNIT
Address:	1C0148h-1C014Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_VCSUNIT0
Address:	1C4148h-1C414Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_VCSUNIT1
Address:	1C8148h-1C814Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_VECSUNIT0
Address:	1D0148h-1D014Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_VCSUNIT2

BB_PREEMPT_ADDR - Batch Buffer Head Pointer Preemption Register

Address:	1D4148h-1D414Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_VCSUNIT3

Address:	1D8148h-1D814Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_VECSUNIT1

Address:	1E0148h-1E014Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_VCSUNIT4

Address:	1E4148h-1E414Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_VCSUNIT5

Address:	1E8148h-1E814Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_VECSUNIT2

Address:	1F0148h-1F014Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_VCSUNIT6

Address:	1F4148h-1F414Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_VCSUNIT7

Address:	1F8148h-1F814Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_VECSUNIT3

Description
This register gets updated with the DWord-aligned graphics memory address of the PREEMPTABLE command

BB_PREEMPT_ADDR - Batch Buffer Head Pointer Preemption Register

in the batch buffer on which preemption has occurred.
This register gets updated with the DWord-aligned graphics memory address of the command following the MI_BATCH_START corresponding to the second level batch buffer, when the preemption has occurred in the second level batch buffer.
This register value should be looked at only when the preemption has occurred in the batch buffer. This is indicated by "Ring/Batch Indicator" in "RING_BUFFER_HEAD_PREEMPT_REG". This register value retains its previous value and doesn't change when the preemption occurs on a preemptable command in ring buffer.
Preemption is triggered by valid UHPTR in ring buffer mode of scheduling and by a pending execlist in Exec-List mode of scheduling. This is a global register and context save/restored as part of power context image.

Preemptable Commands	Source
MI_ARB_CHECK 3D_PRIMITIVE GPGPU_WALKER MEDIA_STATE_FLUSH PIPE_CONTROL (Only in GPGPU mode of pipeline selection) MI_ATOMIC (Post Sync Operation set in GPGPU mode of pipeline selection) MI_SEMAPHORE_SIGNAL (Post Sync Operation set in GPGPU mode of pipeline selection)	RenderCS

Preemptable Commands	Source
MI_ARB_CHECK	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS

Programming Notes
Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description
0	31:2	**Batch Buffer Head Pointer** Format: GraphicsAddress[31:2] This field specifies the DWord-aligned Graphics Memory Address of the PREEMPTABLE command in a batch buffer where the Preemption has occurred.
	1:0	**Reserved** Format: MBZ

Batch Buffer Head Pointer Register

BB_ADDR - Batch Buffer Head Pointer Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	02140h-02143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_RCSUNIT
Address:	18140h-18143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_POCSUNIT
Address:	22140h-22143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_BCSUNIT
Address:	1C0140h-1C0143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_VCSUNIT0
Address:	1C4140h-1C4143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_VCSUNIT1
Address:	1C8140h-1C8143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_VECSUNIT0
Address:	1D0140h-1D0143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_VCSUNIT2
Address:	1D4140h-1D4143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_VCSUNIT3
Address:	1D8140h-1D8143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_VECSUNIT1
Address:	1E0140h-1E0143h

BB_ADDR - Batch Buffer Head Pointer Register

Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_VCSUNIT4

Address:	1E4140h-1E4143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_VCSUNIT5

Address:	1E8140h-1E8143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_VECSUNIT2

Address:	1F0140h-1F0143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_VCSUNIT6

Address:	1F4140h-1F4143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_VCSUNIT7

Address:	1F8140h-1F8143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_VECSUNIT3

Description

This field specifies the DWord-aligned Graphics Memory Address of commands being fetched from the first level batch buffer. This register have valid values only when the “Valid” bit is set to‘0’.

Programming Notes

Programming Restriction: This register should NEVER be programmed by driver. This is for HW internal use only.

DWord	Bit	Description
0	31:2	**Batch Buffer Head Pointer** Format: GraphicsAddress[31:2] **Description** This field specifies the DWord-aligned Graphics Memory Address of commands being fetched from the first level batch buffer. “Valid” bit will be ‘0’ when there is no active batch buffer and this field has no significance. This field specifies the DWord-aligned Graphics Memory Address of commands being fetched for the most recently initiated batch buffer. This register have valid values only when the “Valid” bit is set to‘0’. Level of the batch buffer is indicated based on the Batch Buffer Stack Pointer value in BB_STATE register. • Stack Pointer holding a value ‘0’ indicates First Level batch buffer.

BB_ADDR - Batch Buffer Head Pointer Register

- Stack Pointer holding a value ‘1’ indicates Second Level batch buffer.
- Stack Pointer holding a value ‘2’ indicates Third Level batch buffer.

1	**Reserved**
	Format: MBZ
0	**Valid**
	Format: U1

Value	Name	Description
0h	Invalid **[Default]**	Batch buffer Invalid
1h	Valid	Batch buffer Valid

Batch Buffer Per Context Pointer

BB_PER_CTX_PTR - Batch Buffer Per Context Pointer	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	021C0h-021C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_RCSUNIT
Address:	181C0h-181C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_POCSUNIT
Address:	221C0h-221C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_BCSUNIT
Address:	1C01C0h-1C01C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_VCSUNIT0
Address:	1C41C0h-1C41C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_VCSUNIT1
Address:	1C81C0h-1C81C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_VECSUNIT0
Address:	1D01C0h-1D01C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_VCSUNIT2
Address:	1D41C0h-1D41C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_VCSUNIT3
Address:	1D81C0h-1D81C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_VECSUNIT1

BB_PER_CTX_PTR - Batch Buffer Per Context Pointer

Address:	1E01C0h-1E01C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_VCSUNIT4

Address:	1E41C0h-1E41C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_VCSUNIT5

Address:	1E81C0h-1E81C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_VECSUNIT2

Address:	1F01C0h-1F01C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_VCSUNIT6

Address:	1F41C0h-1F41C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_VCSUNIT7

Address:	1F81C0h-1F81C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_VECSUNIT3

This register is used to program the batch buffer address to be executed between context restore and execution of ring/execution list if enabled. This will only get executed due to regular context save/restore and not during power restore. This register is part of the execution list context and will be executed per context. Only supported if execution list is enabled. There is no preempting workloads within the Per Context Batch Buffer.

Programming Notes	Source
BlitterCS/VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be programmed for these command streamers.	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS
Render CS: Per Context Batch Buffer execution must not look at the MI_RS_CONTROL or Wait For Event status that are restored for the corresponding context. Ex: A context with MI_RS_CONTROL status with RS disabled doesn't stop Render CS from triggering Resource Streamer to execute Per Context Batch Buffer when "**RS Enabled Batch Buffer Per Context**" is set.	RenderCS
RenderCS: The following commands are not supported within a Per Context Batch Buffer: **Command Name** MI_WAIT_FOR_EVENT MI_ARB_CHECK	RenderCS

BB_PER_CTX_PTR - Batch Buffer Per Context Pointer

MI_REPORT_HEAD
MI_URB_ATOMIC_ALLOC
MI_SUSPEND_FLUSH
MI_TOPOLOGY_FILTER
MI_SET_CONTEXT
MI_URB_CLEAR
MI_SEMAPHORE_WAIT (Memory Poll Mode). Note: MI_SEMAPHORE_WAIT in register poll mode is supported.
MI_SEMAPHORE_SIGNAL
MI_BATCH_BUFFER_START
MI_CONDITIONAL_BATCH_BUFFER_END
MEDIA_OBJECT_WALKER
GPGPU_WALKER
3DPRIMITIVE
3DSTATE_BINDING_TABLE_POINTERS_VS
3DSTATE_BINDING_TABLE_POINTERS_HS
3DSTATE_BINDING_TABLE_POINTERS_DS
3DSTATE_BINDING_TABLE_POINTERS_GS
3DSTATE_BINDING_TABLE_POINTERS_PS
3DSTATE_CONSTANT_VS
3DSTATE_CONSTANT_GS
3DSTATE_CONSTANT_PS
3DSTATE_CONSTANT_HS
3DSTATE_CONSTANT_DS
PIPECONTROL

DWord	Bit	Description
0	31:12	**Batch Buffer Per Context Address** Format: U20 Pointer to the Context in memory to be executed as a batch.
	11:3	**Reserved** Format: MBZ
	2	**FORCE BB_PER_CTX_PTR** On detecting a context restore (not lite restore) with head pointer equals to tail pointer, command stream optimizes context switch process by not doing engine context restore and context save for the corresponding context. As part of this optimization command stream doesn't execute batch buffer per context pointer

BB_PER_CTX_PTR - Batch Buffer Per Context Pointer

(BB_PER_CTX_PTR). Setting this bit allows command stream to execute BB_PER_CTX_PT even on context restore flows with head pointer equals to tail pointer.

Value	Name	Description
0	**[Default]**	Command stream does not execute BB_PER_CTX_PTR on context restore with head pointer equals to tail pointer.
1		Command stream does execute BB_PER_CTX_PTR on context restore with head pointer equals to tail pointer.

1 **Reserved**

0 **Batch Buffer Per Context Valid**

Format:	U1

If set, the command stream will execute the context from the **Batch Buffer Per Context Address** prior to the execution of actual submitted workloads.

Batch Buffer Start Head Pointer Register

BB_START_ADDR - Batch Buffer Start Head Pointer Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02150h-02153h
Name:	Batch Buffer Start Head Pointer Register
ShortName:	BB_START_ADDR_RCSUNIT
Address:	18150h-18153h
Name:	Batch Buffer Start Head Pointer Register
ShortName:	BB_START_ADDR_POCSUNIT
Address:	22150h-22153h
Name:	Batch Buffer Start Head Pointer Register
ShortName:	BB_START_ADDR_BCSUNIT
Address:	1C0150h-1C0153h
Name:	Batch Buffer Start Head Pointer Register
ShortName:	BB_START_ADDR_VCSUNIT0
Address:	1C4150h-1C4153h
Name:	Batch Buffer Start Head Pointer Register
ShortName:	BB_START_ADDR_VCSUNIT1
Address:	1C8150h-1C8153h
Name:	Batch Buffer Start Head Pointer Register
ShortName:	BB_START_ADDR_VECSUNIT0
Address:	1D0150h-1D0153h
Name:	Batch Buffer Start Head Pointer Register
ShortName:	BB_START_ADDR_VCSUNIT2
Address:	1D4150h-1D4153h

BB_START_ADDR - Batch Buffer Start Head Pointer Register

Name:	Batch Buffer Start Head Pointer Register
ShortName:	BB_START_ADDR_VCSUNIT3

Address:	1D8150h-1D8153h
Name:	Batch Buffer Start Head Pointer Register
ShortName:	BB_START_ADDR_VECSUNIT1

Address:	1E0150h-1E0153h
Name:	Batch Buffer Start Head Pointer Register
ShortName:	BB_START_ADDR_VCSUNIT4

Address:	1E4150h-1E4153h
Name:	Batch Buffer Start Head Pointer Register
ShortName:	BB_START_ADDR_VCSUNIT5

Address:	1E8150h-1E8153h
Name:	Batch Buffer Start Head Pointer Register
ShortName:	BB_START_ADDR_VECSUNIT2

Address:	1F0150h-1F0153h
Name:	Batch Buffer Start Head Pointer Register
ShortName:	BB_START_ADDR_VCSUNIT6

Address:	1F4150h-1F4153h
Name:	Batch Buffer Start Head Pointer Register
ShortName:	BB_START_ADDR_VCSUNIT7

Address:	1F8150h-1F8153h
Name:	Batch Buffer Start Head Pointer Register
ShortName:	BB_START_ADDR_VECSUNIT3

This register contains the address specified in the last MI_BATCH_BUFFER_START command executed for the first level batch buffer or chained first level batch buffer.

Programming Notes

Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use

BB_START_ADDR - Batch Buffer Start Head Pointer Register

only.

DWord	Bit	Description
0	31:2	**Batch Buffer Start Head Pointer** Format: GraphicsAddress[31:2] This field specifies the DWord-aligned Graphics Memory Address where the last initiated Batch Buffer starting address.
	1:0	**Reserved** Format: MBZ

Batch Buffer Start Upper Head Pointer Register

BB_START_ADDR_UDW - Batch Buffer Start Upper Head Pointer Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02170h-02173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_RCSUNIT
Address:	18170h-18173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_POCSUNIT
Address:	22170h-22173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_BCSUNIT
Address:	1C0170h-1C0173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_VCSUNIT0
Address:	1C4170h-1C4173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_VCSUNIT1
Address:	1C8170h-1C8173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_VECSUNIT0
Address:	1D0170h-1D0173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_VCSUNIT2

BB_START_ADDR_UDW - Batch Buffer Start Upper Head Pointer Register

Address:	1D4170h-1D4173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_VCSUNIT3

Address:	1D8170h-1D8173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_VECSUNIT1

Address:	1E0170h-1E0173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_VCSUNIT4

Address:	1E4170h-1E4173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_VCSUNIT5

Address:	1E8170h-1E8173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_VECSUNIT2

Address:	1F0170h-1F0173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_VCSUNIT6

Address:	1F4170h-1F4173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_VCSUNIT7

Address:	1F8170h-1F8173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_VECSUNIT3

This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space specified in the last MI_START_BATCH_BUFFER command.

BB_START_ADDR_UDW - Batch Buffer Start Upper Head Pointer Register

Programming Notes
Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**Head Pointer Upper DWORD** Format: GraphicsAddress[47:32]

Batch Buffer State Register

BB_STATE - Batch Buffer State Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	02110h-02113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_RCSUNIT
Address:	18110h-18113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_POCSUNIT
Address:	22110h-22113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_BCSUNIT
Address:	1C0110h-1C0113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_VCSUNIT0
Address:	1C4110h-1C4113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_VCSUNIT1
Address:	1C8110h-1C8113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_VECSUNIT0
Address:	1D0110h-1D0113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_VCSUNIT2
Address:	1D4110h-1D4113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_VCSUNIT3
Address:	1D8110h-1D8113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_VECSUNIT1
Address:	1E0110h-1E0113h

BB_STATE - Batch Buffer State Register

Name:	Batch Buffer State Register
ShortName:	BB_STATE_VCSUNIT4

Address:	1E4110h-1E4113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_VCSUNIT5

Address:	1E8110h-1E8113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_VECSUNIT2

Address:	1F0110h-1F0113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_VCSUNIT6

Address:	1F4110h-1F4113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_VCSUNIT7

Address:	1F8110h-1F8113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_VECSUNIT3

Description

This register contains the attributes of the current batch buffer initiated from the Ring Buffer.

This register should not be written by software. These fields should only get written by a context restore. Software should always set these fields via the MI_BATCH_BUFFER_START command when initiating a batch buffer. This register is saved and restored with context.

Programming Notes

Contents of this register are valid only when "Valid" bit in BB_ADDR register is set.

DWord	Bit	Description
0	31:10	**Reserved** Format: MBZ
	9	**POSH Start** Exists If: //RCS, POCS This bit reflects the POSH Start value programmed by the active first level MI_BATCH_BUFFER_START command.
	8	**POSH Enable** Exists If: //RCS, POCS This bit reflects the POSH Enable value programmed by the active first level MI_BATCH_BUFFER_START command.

BB_STATE - Batch Buffer State Register

	7	**Reserved** Format: MBZ
	6	**Clear Command Buffer Enable** Source: RenderCS Format: U1 If set the batch buffer is getting executed from the Write Once area. The address of the batch buffer is an offset into the WOPCM area.
	6	**Reserved** Source: BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS Format: MBZ
	5	**Address Space Indicator** Note: This field reflects the effective address space indicator security level and may not be the same as the Address Space Indicator written using MI_BATCH_BUFFER_START.

Value	Name	Description
0h	GGTT **[Default]**	This Batch buffer is located in GGTT memory and is privileged
1h	PPGTT	This Batch buffer is located in PPGTT memory and is non-privileged.

	4	**Reserved**
	4	**Reserved** Source: BlitterCS Exists If: //BCS Format: MBZ
	3:2	**Reserved** Format: MBZ
	1:0	**Reserved**

Batch Buffer Upper Head Pointer Preemption Register

BB_PREEMPT_ADDR_UDW - Batch Buffer Upper Head Pointer Preemption Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0216Ch-0216Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_RCSUNIT
Address:	1816Ch-1816Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_POCSUNIT
Address:	2216Ch-2216Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_BCSUNIT
Address:	1C016Ch-1C016Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_VCSUNIT0
Address:	1C416Ch-1C416Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_VCSUNIT1
Address:	1C816Ch-1C816Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_VECSUNIT0
Address:	1D016Ch-1D016Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_VCSUNIT2

BB_PREEMPT_ADDR_UDW - Batch Buffer Upper Head Pointer Preemption Register

Address:	1D416Ch-1D416Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_VCSUNIT3

Address:	1D816Ch-1D816Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_VECSUNIT1

Address:	1E016Ch-1E016Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_VCSUNIT4

Address:	1E416Ch-1E416Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_VCSUNIT5

Address:	1E816Ch-1E816Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_VECSUNIT2

Address:	1F016Ch-1F016Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_VCSUNIT6

Address:	1F416Ch-1F416Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_VCSUNIT7

Address:	1F816Ch-1F816Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_VECSUNIT3

This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the last preempted batch buffer. This register follows the same rules as the

BB_PREEMPT_ADDR_UDW - Batch Buffer Upper Head Pointer Preemption Register

BB_PREEMPT_ADDR register.

Programming Notes
Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**Batch Buffer Head Pointer Upper DWORD** Format: GraphicsAddress[47:32] This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the last preempted batch buffer.

Batch Buffer Upper Head Pointer Register

BB_ADDR_UDW - Batch Buffer Upper Head Pointer Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	02168h-0216Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_RCSUNIT
Address:	18168h-1816Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_POCSUNIT
Address:	22168h-2216Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_BCSUNIT
Address:	1C0168h-1C016Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_VCSUNIT0
Address:	1C4168h-1C416Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_VCSUNIT1
Address:	1C8168h-1C816Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_VECSUNIT0
Address:	1D0168h-1D016Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_VCSUNIT2
Address:	1D4168h-1D416Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_VCSUNIT3
Address:	1D8168h-1D816Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_VECSUNIT1
Address:	1E0168h-1E016Bh

BB_ADDR_UDW - Batch Buffer Upper Head Pointer Register

Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_VCSUNIT4

Address:	1E4168h-1E416Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_VCSUNIT5

Address:	1E8168h-1E816Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_VECSUNIT2

Address:	1F0168h-1F016Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_VCSUNIT6

Address:	1F4168h-1F416Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_VCSUNIT7

Address:	1F8168h-1F816Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_VECSUNIT3

Description

This register specifies the upper 32 bits of the 4GB aligned base address, within the 64-bit host virtual address space of the commands being fetched from the first level batch buffer. This register has valid values only when the “Valid” bit in BB_ADDR is set to “1’.
GraphicsAddress is 64-bit value [63:0], but only a portion of it is used by hardware. The uppermost reserved bits are ignored and MBZ.

Programming Notes

This register should NEVER be programmed by driver. This is for HW internal use only.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**Batch Buffer Head Pointer Upper DWORD** Format: GraphicsAddress[47:32]

Batch Offset Register

BB_OFFSET - Batch Offset Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02158h-0215Bh
Name:	Batch Offset Register
ShortName:	BB_OFFSET_RCSUNIT
Address:	18158h-1815Bh
Name:	Batch Offset Register
ShortName:	BB_OFFSET_POCSUNIT
Address:	22158h-2215Bh
Name:	Batch Offset Register
ShortName:	BB_OFFSET_BCSUNIT
Address:	1C0158h-1C015Bh
Name:	Batch Offset Register
ShortName:	BB_OFFSET_VCSUNIT0
Address:	1C4158h-1C415Bh
Name:	Batch Offset Register
ShortName:	BB_OFFSET_VCSUNIT1
Address:	1C8158h-1C815Bh
Name:	Batch Offset Register
ShortName:	BB_OFFSET_VECSUNIT0
Address:	1D0158h-1D015Bh
Name:	Batch Offset Register
ShortName:	BB_OFFSET_VCSUNIT2
Address:	1D4158h-1D415Bh

BB_OFFSET - Batch Offset Register

Name: Batch Offset Register
ShortName: BB_OFFSET_VCSUNIT3

Address: 1D8158h-1D815Bh
Name: Batch Offset Register
ShortName: BB_OFFSET_VECSUNIT1

Address: 1E0158h-1E015Bh
Name: Batch Offset Register
ShortName: BB_OFFSET_VCSUNIT4

Address: 1E4158h-1E415Bh
Name: Batch Offset Register
ShortName: BB_OFFSET_VCSUNIT5

Address: 1E8158h-1E815Bh
Name: Batch Offset Register
ShortName: BB_OFFSET_VECSUNIT2

Address: 1F0158h-1F015Bh
Name: Batch Offset Register
ShortName: BB_OFFSET_VCSUNIT6

Address: 1F4158h-1F415Bh
Name: Batch Offset Register
ShortName: BB_OFFSET_VCSUNIT7

Address: 1F8158h-1F815Bh
Name: Batch Offset Register
ShortName: BB_OFFSET_VECSUNIT3

Description	Source
This register contains the offset value to be added to the Batch Buffer Start Address in the MI_BATCH_BUFFER_START command when the Enable Offset bit in MI_BATCH_BUFFER_START command is set.	

BB_OFFSET - Batch Offset Register

Preemptable Commands	Source
• MI_ARB_CHECK • 3D_PRIMITIVE • GPGPU_WALKER • MEDIA_STATE_FLUSH • PIPE_CONTROL (Only in GPGPU mode of pipeline selection) • MI_ATOMIC (Post Sync Operation set in GPGPU mode of pipeline selection) • MI_SEMAPHORE_SIGNAL (Post Sync Operation set in GPGPU mode of pipeline selection)	RenderCS

RenderCS

Preemptable Commands	Source
MI_ARB_CHECK	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS

BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS

Programming Notes

On preemption occurring within a primary/chain batch buffer this register is loaded with the offset value of the preempted command header from the batch start address when the Enable Load is set. Preemption of 3D or GP_GPU workloads can only occur on preemptable commands. Batch buffer offset always points to the preemptable command if preempted on preemption or the immediate command following it if not preempted on preemption. EX: Preemption occurs on 3D_PRIMITVE command

- If the 3D_PRIMTIVE command is completely processed by render pipe then the BB_OFFSET points to the command following 3D_PRIMITIVE
- If the 3D_PRIMTIVE command is not completely processed by render pipe then the BB_OFFSET points to the 3D_PRIMITIVE command.

DWord	Bit	Description
0	31:2	**Batch Buffer Offset** Format: GraphicsAddress[31:2] This field specifies the DWord-aligned offset between the starting address of the batch buffer and where the last initiated Batch Buffer is currently fetching commands.
	1	**Reserved** Format: MBZ
	0	**Enable Load** Default Value: 1 Format: Enable

BB_OFFSET - Batch Offset Register		
		Description
		If this bit is set then the Batch Buffer Offset is loaded with the preempted command offset or the following command whenever a batch buffer is ended due to a Preemptable command.

BCS Context Sizes

BCS_CXT_SIZE - BCS Context Sizes	
Register Space:	MMIO: 0/2/0
Source:	BlitterCS
Access:	Read/32 bit Write Only
Size (in bits):	32
Address:	221A8h

DWord	Bit	Description
0	31:13	**Reserved** Format: MBZ
	12:8	**BCS Context Size** Format: U5
	7:5	**Reserved** Format: MBZ
	4:0	**Execlist Context Size** Format: U5

BCS Ring Buffer Next Context ID Register

BCS_RNCID - BCS Ring Buffer Next Context ID Register	
Register Space:	MMIO: 0/2/0
Source:	BlitterCS
Access:	R/W
Size (in bits):	64
Address:	22198h-2219Fh

This register contains the *next* ring context ID associated with the ring buffer.

Programming Notes

The current context (RCCID) register can be updated indirectly from this register on a context switch event. Note that the only time a context switch can occur is when MI_ARB_CHECK enables preemption or the current context runs dry (head pointer becomes equal to tail pointer).

DWord	Bit	Description
0	63:0	**Unnamed** See Context Descriptor for BCS

BCS SW Control

BCS_SWCTRL - BCS SW Control

Register Space:	MMIO: 0/2/0
Source:	BlitterCS
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	22200h

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask
	15:4	**Reserved** Format: MBZ
	3	**Shrink Blitter Cache** Format: U1 This bit is primarily used for validation purposes to speed up the test time. The full cache depth of 128 CLs should be used for production. This bit is part of the context save/restore. This bit only applies to the XY_FAST_COPY_BLT command. **Value** / **Name** / **Description** 0 / **[Default]** / Blitter/BCS flush will flush and invalidate all cachelines in the Blitter/BLB cache (default). 1 / / Blitter Cache depth will be shortened from 128 CLs to 16 CLs.
	2	**Not Invalidate Blitter Cache on BCS Flush** Format: U1 Programming this bit allows optimal/maximal cache hit usage, when the destination surface of a Fast Copy Blit, is to be used as the Source for a follow on Fast Copy blit, even if the destination surface is flushed out for Display coherency reasons (where the destination surface is also needed to be Displayed). Such a flush with clean cacheline state is suggested when the intermediate blit operation results are being required to maintain memory coherency. The legacy method of cache invalidation on flush can be still pursued at the end of all blit operations or when switching happens due to other prescribed legacy reasons, or when switching from the new Fast Copy Engine blit, to legacy Engine blits. This bit should be programmed set only when used with Fast Copy Blit commands. This bit is part of the context save/restore. This bit only applies to the XY_FAST_COPY_BLT command. **Value** / **Name** / **Description** 0 / **[Default]** / Blitter/BLB Cache will be 128 cache lines in depth (default). 1 / / BCS flush will put all dirty CL in the Blitter cache in the clean state. Any CL

BCS_SWCTRL - BCS SW Control

		already in the clean state will remain clean.
	1	**Tile Y Destination** Format: U1 Programming this bit makes the HW treat all destination surfaces as Tile Y. This bit over-rides the setting of the destination format in the packet provided to the blitter command streamer. SW is required to flush the HW before changing the polarity of this bit. This bit is part of the context save/restore. This bit does not impact the operations of the XY_FAST_COPY_BLT command
	0	**Tile Y Source** Format: U1 Programming this bit makes the HW treat all source surfaces as Tile Y. This bit over-rides the setting of the source format in the packet provided to the blitter command streamer. SW is required to flush the HW before changing the polarity of this bit. This bit is part of the context save/restore. This bit does not impact the operations of the XY_FAST_COPY_BLT command

Bitstream Output Bit Count for the last Syntax Element Report Register

MFC_BITSTREAM_SE_BITCOUNT_SLICE - Bitstream Output Bit Count for the last Syntax Element Report Register	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	128D4h
Name:	SE Output Bit Count

This register stores the count of number of bits in the bitstream for the last syntax element before padding. The bit count is before the byte-aligned alignment padding insertion, but includes the stop-one-bit. This register is part of the context save and restore.

DWord	Bit	Description
0	31:0	**MFC Bitstream Syntax Element Bit Count** Total number of bits in the bitstream output before padding. This count is updated each time the internal counter is incremented.

Bitstream Output Byte Count Per Slice Report Register

MFC_BITSTREAM_BYTECOUNT_SLICE - Bitstream Output Byte Count Per Slice Report Register	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	128D0h

This register stores the count of bytes of the bitstream output. This register is part of the context save and restore.

DWord	Bit	Description
0	31:0	**MFC Bitstream Byte Count** Total number of bytes in the bitstream output from the encoder. This count is updated for every time the internal bitstream counter is incremented.

Bitstream Output Minimal Size Padding Count Report Register

MFC_AVC_MINSIZE_PADDING_COUNT - Bitstream Output Minimal Size Padding Count Report Register

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12814h
Name:	Minimal Size Padding

This register stores the count in bytes of **minimal size padding insertion. It is primarily provided for statistical data gathering.** This register is part of the context save and restore.

DWord	Bit	Description
0	31:0	**MFC AVC MinSize Padding Count** Total number of bytes in the bitstream output contributing to minimal size padding operation. This count is updated each time when the padding count is incremented.

BLC_PWM_CTL

BLC_PWM_CTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	48250h-48253h
Name:	Backlight PWM Control
ShortName:	BLC_PWM_CTL
Power:	PG0
Reset:	soft

This register controls the backlight PWM logic going to the display utility pin on the CPU.

DWord	Bit	Description
0	31	**PWM Enable** This bit enables the PWM logic. Value / Name / Description: 0b / Disable / PWM disabled 1b / Enable / PWM enabled Restriction: The display utility pin must be configured correctly to output the PWM. Program the frequency and duty cycle before enabling PWM.
	30:29	**Pipe Select** This field selects which vertical blank will be used for backlight blinking. Value / Name / Description: 00b / Pipe A / Use Pipe A 01b / Pipe B / Use Pipe B 10b / Pipe C / Use Pipe C
	28	**Blinking Enable** This bit enables backlight blinking. When enabled, the backlight will be driven on at the programmed brightness during vertical blank and driven off during vertical active. Value / Name: 0b / Disable 1b / Enable
	27	**PWM Granularity** This field controls the granularity (minimum increment) of the PWM backlight control counter.

BLC_PWM_CTL

		Value	Name	Description
		0b	128	PWM frequency adjustment on 128 clock increments
		1b	8	PWM frequency adjustment on 8 clock increments
	26:0	**Reserved**		

BLC_PWM_DATA

BLC_PWM_DATA	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	48254h-48257h
Name:	Backlight PWM Data
ShortName:	BLC_PWM_DATA
Power:	PG0
Reset:	soft

DWord	Bit	Description
0	31:16	**Backlight Frequency** This field determines the number of time base events in total for a complete cycle of modulated backlight control. This field is programmed based on the frequency of the clock that is being used and the desired PWM frequency. This value represents the period of the PWM stream in CD clocks multiplied by 128 (default increment) or 8 (alternate increment selected by BLC_PWM_CTL PWM_Granularity).
	15:0	**Backlight Duty Cycle** This field determines the number of time base events for the active portion of the PWM backlight control. A value of zero will turn the backlight off. A value equal to the backlight modulation frequency field will be full on. Updates will take affect at the end of the current PWM cycle. This value represents the active time of the PWM stream in CD clock periods multiplied by 128 (default increment) or 8 (alternate increment selected by BLC_PWM_CTL PWM_Granularity). **Restriction** This should never be larger than the frequency field.

Blitter MOCS LECC 00 TC 00 Register

BLT_MOCS_LECC_00_TC_00 - Blitter MOCS LECC 00 TC 00 Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CC00h
Name:	Blitter MOCS 0
ShortName:	BLT_MOCS_0
Address:	0CC40h
Name:	Blitter MOCS 16
ShortName:	BLT_MOCS_16
Address:	0CC80h
Name:	Blitter MOCS 32
ShortName:	BLT_MOCS_32
Address:	0CCC0h
Name:	Blitter MOCS 48
ShortName:	BLT_MOCS_48

Blitter MOCS register

DWord	Bit	Description
0	31:19	**Reserved** Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service** Default Value: 00b Access: R/W This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in.The allocation of certain LLC ways to different class of service settings is

a project dependent decision and listed in the Bspec.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3

14 **Snoop Control Field**

Default Value:	0b
Access:	R/W

Description
Not used in ICL.

13:11 **Page Faulting Mode**

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8 **Skip Caching control**

Default Value:	000b
Access:	R/W

Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface.
If "0" - than corresponding address bit value is do not care
Bit[8]=1: address bit[9] needs to be "0" to cache in target
Bit[9]=1: address bit[10] needs to be "0" to cache in target
Bit[10]=1: address bit[11] needs to be "0" to cache in target

7 **Enable Reverse Skip Caching**

Default Value:	0b
Access:	R/W

Enable for the Skip cache mechanism
0: Not enabled
1: Enabled for LLC

6 **Dont allocate on miss**

Default Value:	0b
Access:	R/W

Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM).

BLT_MOCS_LECC_00_TC_00 - Blitter MOCS LECC 00 TC 00 Register

		0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based contr ols have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

Blitter MOCS LECC 00 TC 01 Register

BLT_MOCS_LECC_00_TC_01 - Blitter MOCS LECC 00 TC 01 Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CC04h
Name:	Blitter MOCS 1
ShortName:	BLT_MOCS_1
Address:	0CC44h
Name:	Blitter MOCS 17
ShortName:	BLT_MOCS_17
Address:	0CC84h
Name:	Blitter MOCS 33
ShortName:	BLT_MOCS_33
Address:	0CCC4h
Name:	Blitter MOCS 49
ShortName:	BLT_MOCS_49

Blitter MOCS register

DWord	Bit	Description
0	31:19	**Reserved** Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service** Default Value: 00b Access: R/W This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is

a project dependent decision and listed in the Bspec.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3

14 **Snoop Control Field**

Default Value:	0b
Access:	R/W

Description
Not used in ICL.

13:11 **Page Faulting Mode**

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8 **Skip Caching control**

Default Value:	000b
Access:	R/W

Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface.
If "0" - than corresponding address bit value is do not care
Bit[8]=1: address bit[9] needs to be "0" to cache in target
Bit[9]=1: address bit[10] needs to be "0" to cache in target
Bit[10]=1: address bit[11] needs to be "0" to cache in target

7 **Enable Reverse Skip Caching**

Default Value:	0b
Access:	R/W

Enable for the Skip cache mechanism
0: Not enabled
1: Enabled for LLC

6 **Dont allocate on miss**

Default Value:	0b
Access:	R/W

Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM).

BLT_MOCS_LECC_00_TC_01 - Blitter MOCS LECC 00 TC 01 Register

		0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based contr ols have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

Blitter MOCS LECC 00 TC 10 Register

BLT_MOCS_LECC_00_TC_10 - Blitter MOCS LECC 00 TC 10 Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CC08h
Name:	Blitter MOCS 2
ShortName:	BLT_MOCS_2
Address:	0CC48h
Name:	Blitter MOCS 18
ShortName:	BLT_MOCS_18
Address:	0CC88h
Name:	Blitter MOCS 34
ShortName:	BLT_MOCS_34
Address:	0CCC8h
Name:	Blitter MOCS 50
ShortName:	BLT_MOCS_50

Blitter MOCS register

DWord	Bit	Description
0	31:19	**Reserved** Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service** Default Value: 00b Access: R/W This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is

a project dependent decision and listed in the Bspec.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3

14 **Snoop Control Field**

Default Value:	0b
Access:	R/W

Description
Not used in ICL.

13:11 **Page Faulting Mode**

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8 **Skip Caching control**

Default Value:	000b
Access:	R/W

Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface.
If "0" - than corresponding address bit value is do not care
Bit[8]=1: address bit[9] needs to be "0" to cache in target
Bit[9]=1: address bit[10] needs to be "0" to cache in target
Bit[10]=1: address bit[11] needs to be "0" to cache in target

7 **Enable Reverse Skip Caching**

Default Value:	0b
Access:	R/W

Enable for the Skip cache mechanism
0: Not enabled
1: Enabled for LLC

6 **Dont allocate on miss**

Default Value:	0b
Access:	R/W

Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM).

BLT_MOCS_LECC_00_TC_10 - Blitter MOCS LECC 00 TC 10 Register

		0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based contr ols have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

Blitter MOCS LECC 01 TC 00 Register

BLT_MOCS_LECC_01_TC_00 - Blitter MOCS LECC 01 TC 00 Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CC0Ch
Name:	Blitter MOCS 3
ShortName:	BLT_MOCS_3
Address:	0CC4Ch
Name:	Blitter MOCS 19
ShortName:	BLT_MOCS_19
Address:	0CC8Ch
Name:	Blitter MOCS 35
ShortName:	BLT_MOCS_35
Address:	0CCCCh
Name:	Blitter MOCS 51
ShortName:	BLT_MOCS_51

Blitter MOCS register

DWord	Bit	Description
0	31:19	**Reserved** Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service** Default Value: 00b Access: R/W This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in.The allocation of certain LLC ways to different class of service settings is

a project dependent decision and listed in the Bspec.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3

14 **Snoop Control Field**

Default Value:	0b
Access:	R/W

Description
Not used in ICL.

13:11 **Page Faulting Mode**

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8 **Skip Caching control**

Default Value:	000b
Access:	R/W

Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface.
If "0" - than corresponding address bit value is do not care
Bit[8]=1: address bit[9] needs to be "0" to cache in target
Bit[9]=1: address bit[10] needs to be "0" to cache in target
Bit[10]=1: address bit[11] needs to be "0" to cache in target

7 **Enable Reverse Skip Caching**

Default Value:	0b
Access:	R/W

Enable for the Skip cache mechanism
0: Not enabled
1: Enabled for LLC

6 **Dont allocate on miss**

Default Value:	0b
Access:	R/W

Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM).

		0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based contr ols have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

Blitter MOCS LECC 10 TC 00 Register

DWord	Bit
0	31:19
	18:17
	16:15
	14
	13:11
	10:8
	7
	6
	5:4
	3:2
	1:0

Blitter MOCS LECC 10 TC 01 Register

DWord	Bit
0	31:19
	18:17
	16:15
	14
	13:11
	10:8
	7
	6
	5:4
	3:2
	1:0

Blitter MOCS LECC 10 TC 10 Register

BLT_MOCS_LECC_10_TC_10 - Blitter MOCS LECC 10 TC 10 Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CC18h
Name:	Blitter MOCS 6
ShortName:	BLT_MOCS_6
Address:	0CC30h
Name:	Blitter MOCS 12
ShortName:	BLT_MOCS_12
Address:	0CC58h
Name:	Blitter MOCS 22
ShortName:	BLT_MOCS_22
Address:	0CC70h
Name:	Blitter MOCS 28
ShortName:	BLT_MOCS_28
Address:	0CC98h
Name:	Blitter MOCS 38
ShortName:	BLT_MOCS_38
Address:	0CCB0h
Name:	Blitter MOCS 44
ShortName:	BLT_MOCS_44
Address:	0CCD8h
Name:	Blitter MOCS 54
ShortName:	BLT_MOCS_54
Address:	0CCF0h
Name:	Blitter MOCS 60
ShortName:	BLT_MOCS_60

Blitter MOCS register

DWord	Bit	Description	
0	31:19	**Reserved**	
		Default Value:	0000000000000b

BLT_MOCS_LECC_10_TC_10 - Blitter MOCS LECC 10 TC 10 Register

	Access:	RO

18:17 Self Snoop Enable

Default Value:	00b
Access:	R/W

00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic
01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface
11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface

16:15 Class of Service

Default Value:	00b
Access:	R/W

This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3

14 Snoop Control Field

Default Value:	0b
Access:	R/W

Description
Not used in ICL.

13:11 Page Faulting Mode

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8 Skip Caching control

Default Value:	000b

BLT_MOCS_LECC_10_TC_10 - Blitter MOCS LECC 10 TC 10 Register

		Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is do not care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching

BLT_MOCS_LECC_10_TC_10 - Blitter MOCS LECC 10 TC 10 Register

		00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based contr ols have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

Blitter MOCS LECC 11 TC 00 Register

BLT_MOCS_LECC_11_TC_00 - Blitter MOCS LECC 11 TC 00 Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CC1Ch
Name:	Blitter MOCS 7
ShortName:	BLT_MOCS_7
Address:	0CC34h
Name:	Blitter MOCS 13
ShortName:	BLT_MOCS_13
Address:	0CC5Ch
Name:	Blitter MOCS 23
ShortName:	BLT_MOCS_23
Address:	0CC74h
Name:	Blitter MOCS 29
ShortName:	BLT_MOCS_29
Address:	0CC9Ch
Name:	Blitter MOCS 39
ShortName:	BLT_MOCS_39
Address:	0CCB4h
Name:	Blitter MOCS 45
ShortName:	BLT_MOCS_45
Address:	0CCDCh
Name:	Blitter MOCS 55
ShortName:	BLT_MOCS_55
Address:	0CCF4h
Name:	Blitter MOCS 61
ShortName:	BLT_MOCS_61

Blitter MOCS register

DWord	Bit	Description	
0	31:19	**Reserved**	
		Default Value:	0000000000000b

BLT_MOCS_LECC_11_TC_00 - Blitter MOCS LECC 11 TC 00 Register

	Access:	RO

18:17 Self Snoop Enable

Default Value:	00b
Access:	R/W

00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic
01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface
11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface

16:15 Class of Service

Default Value:	00b
Access:	R/W

This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3

14 Snoop Control Field

Default Value:	0b
Access:	R/W

Description
Not used in ICL.

13:11 Page Faulting Mode

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8 Skip Caching control

Default Value:	000b

BLT_MOCS_LECC_11_TC_00 - Blitter MOCS LECC 11 TC 00 Register

		Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is do not care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching

BLT_MOCS_LECC_11_TC_00 - Blitter MOCS LECC 11 TC 00 Register

		00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based contr ols have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

Blitter MOCS LECC 11 TC 01 Register

BLT_MOCS_LECC_11_TC_01 - Blitter MOCS LECC 11 TC 01 Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CC20h
Name:	Blitter MOCS 8
ShortName:	BLT_MOCS_8
Address:	0CC38h
Name:	Blitter MOCS 14
ShortName:	BLT_MOCS_14
Address:	0CC60h
Name:	Blitter MOCS 24
ShortName:	BLT_MOCS_24
Address:	0CC78h
Name:	Blitter MOCS 30
ShortName:	BLT_MOCS_30
Address:	0CCA0h
Name:	Blitter MOCS 40
ShortName:	BLT_MOCS_40
Address:	0CCB8h
Name:	Blitter MOCS 46
ShortName:	BLT_MOCS_46
Address:	0CCE0h
Name:	Blitter MOCS 56
ShortName:	BLT_MOCS_56
Address:	0CCF8h
Name:	Blitter MOCS 62
ShortName:	BLT_MOCS_62

Blitter MOCS register

DWord	Bit	Description	
0	31:19	**Reserved**	
		Default Value:	0000000000000b

BLT_MOCS_LECC_11_TC_01 - Blitter MOCS LECC 11 TC 01 Register

	Access:	RO

18:17 Self Snoop Enable

Default Value:	00b
Access:	R/W

00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic
01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface
11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface

16:15 Class of Service

Default Value:	00b
Access:	R/W

This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3

14 Snoop Control Field

Default Value:	0b
Access:	R/W

Description
Not used in ICL.

13:11 Page Faulting Mode

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8 Skip Caching control

Default Value:	000b

BLT_MOCS_LECC_11_TC_01 - Blitter MOCS LECC 11 TC 01 Register

		Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is do not care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching

BLT_MOCS_LECC_11_TC_01 - Blitter MOCS LECC 11 TC 01 Register

		00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based contr ols have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

Blitter MOCS LECC 11 TC 10 Register

BLT_MOCS_LECC_11_TC_10 - Blitter MOCS LECC 11 TC 10 Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CC24h
Name:	Blitter MOCS 9
ShortName:	BLT_MOCS_9
Address:	0CC3Ch
Name:	Blitter MOCS 15
ShortName:	BLT_MOCS_15
Address:	0CC64h
Name:	Blitter MOCS 25
ShortName:	BLT_MOCS_25
Address:	0CC7Ch
Name:	Blitter MOCS 31
ShortName:	BLT_MOCS_31
Address:	0CCA4h
Name:	Blitter MOCS 41
ShortName:	BLT_MOCS_41
Address:	0CCBCh
Name:	Blitter MOCS 47
ShortName:	BLT_MOCS_47
Address:	0CCE4h
Name:	Blitter MOCS 57
ShortName:	BLT_MOCS_57
Address:	0CCFCh
Name:	Blitter MOCS 63
ShortName:	BLT_MOCS_63

Blitter MOCS register

DWord	Bit	Description	
0	31:19	**Reserved**	
		Default Value:	0000000000000b

BLT_MOCS_LECC_11_TC_10 - Blitter MOCS LECC 11 TC 10 Register

	Access:	RO

18:17 Self Snoop Enable

Default Value:	00b
Access:	R/W

00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic
01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface
11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface

16:15 Class of Service

Default Value:	00b
Access:	R/W

This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3

14 Snoop Control Field

Default Value:	0b
Access:	R/W

Description
Not used in ICL.

13:11 Page Faulting Mode

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8 Skip Caching control

Default Value:	000b

BLT_MOCS_LECC_11_TC_10 - Blitter MOCS LECC 11 TC 10 Register

		Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is do not care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching

BLT_MOCS_LECC_11_TC_10 - Blitter MOCS LECC 11 TC 10 Register

		00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based contr ols have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

BLT Fault Counter Register

BLT_FAULT_CNTR - BLT Fault Counter Register		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	045B8h	
DWord	**Bit**	**Description**
0	31:0	**BLT Fault Counter** Default Value: 00000000h Access: RO This counter only applies to advance context when fault and stream mode is selected.

BLT Fixed Counter

BLT_FIXED_CNTR - BLT Fixed Counter

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	045BCh

DWord	Bit	Description
0	31:0	**BLT Fixed Counter** Default Value: 00000000h Access: RO This counter only applies to advance context when fault and stream mode is selected.

Boolean_Counter_B0

OAPERF_B0 - Boolean_Counter_B0	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02920h

This register enables the current live value of performance counter B0 to be read. Since what conditions cause B0 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Boolean_Counter_B1

OAPERF_B1 - Boolean_Counter_B1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02924h

This register enables the current live value of performance counter B1 to be read. Since what conditions cause B1 to increment are defined by the programming of CEC1-0/CEC1-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Boolean_Counter_B2

OAPERF_B2 - Boolean_Counter_B2	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02928h

This register enables the current live value of performance counter B2 to be read. Since what conditions cause B2 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Boolean_Counter_B3

OAPERF_B3 - Boolean_Counter_B3	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0292Ch

This register enables the current live value of performance counter B3 to be read. Since what conditions cause B3 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Boolean_Counter_B4

OAPERF_B4 - Boolean_Counter_B4	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02930h

This register enables the current live value of performance counter B4 to be read. Since what conditions cause B4 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Boolean_Counter_B5

OAPERF_B5 - Boolean_Counter_B5	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02934h

This register enables the current live value of performance counter B5 to be read. Since what conditions cause B5 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Boolean_Counter_B6

OAPERF_B6 - Boolean_Counter_B6	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02938h

This register enables the current live value of performance counter B6 to be read. Since what conditions cause B6 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Boolean_Counter_B7

OAPERF_B7 - Boolean_Counter_B7	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0293Ch

This register enables the current live value of performance counter B7 to be read. Since what conditions cause B7 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

BOOT VECTOR

BOOTMSG - BOOT VECTOR

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	08504h

Boot Message Register
This register gets locked by the Hardware once written and is cleared only during the reset. This is extra protection given against Illegal Programming.

DWord	Bit	Description
0	31:0	**Boot Vector Message** Access: R/W Lock Boot vector is pass through. MBC gets the boot message from GPMunit and forwards it to MSQC. Breakdown of message is done in MSQC. Details: if b[26] = 1 C6SliceA = b[20:17]; C6SliceB= d[13:10] C6Way = 0 C6Area = 0 if b[26] = 0 C6Way = b[25:21], C6Slice = d[20:17]; C6Area = d[17:10] Context Restore = b[7] Reset Type = b[6:5] Ring Stop ID = b[4:0]

Cache Mode Register 0

CACHE_MODE_0 - Cache Mode Register 0

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	32
Address:	07000h
Name:	Cache Mode Register 0
ShortName:	CACHE_MODE_0

This register is used to control the operation of the Render and Sampler L2 Caches. All reserved bits are implemented as read/write.
Before changing the value of this register, GFX pipeline must be idle i.e. full flush is required.
This Register is saved and restored as part of Context.

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask[15:0] A 1 in a bit in this field allows the modification of the corresponding bit in Bits 15:0.
	15	**Reserved** Access: R/W Format: PBC
	14:12	**MSAA Compression Plane Number Threshold for eLLC** Access: R/W

Value	Name	Description
0h	threshold0 **[Default]**	Cache only planeID = 0 in eLLC.
1h	threshold1	Cache only planeID = 0, 1 in eLLC.
2h	threshold2	Cache only planeID = 0..2 in eLLC.
3h	threshold3	Cache only planeID = 0..3 in eLLC.
4h	threshold4	Cache only planeID = 0..4 in eLLC.
5h	threshold5	Cache only planeID = 0..5 in eLLC.
6h	threshold6	Cache only planeID = 0..6 in eLLC.
7h	threshold7	Cache only planeID = 0..7 in eLLC.

Programming Notes
This bit-field is programmed based on MSAA. When MSAA compression is enabled, these

CACHE_MODE_0 - Cache Mode Register 0

	settings affect HW, else it is ignored. For 16X MSAA only lower 8 planes can be cached in eLLC.
11	**Reserved** | | | |---|---| | Access: | R/W | | Format: | PBC |
10	**RCZ PMA Not-Promoted Allocation stall optimization Disable due to change in depth parameters** | | | |---|---| | Access: | R/W | | Format: | Disable | Setting this bit will force the RCZ cache to stall at the allocation of a CL if any of the values in {Depth-mode, DTE, DWE, DTF} are different between the old and new requests to the same CL. The default is a smart stall depending on the New request's depth-test and depth write fields. | Value | Name | Description | |---|---|---| | 0h | **[Default]** | Optimization is enabled | | 1h | | Optimization is disabled |
9	**Sampler L2 TLB Prefetch Enable** | Access: | R/W | |---|---| | Value | Name | Description | |---|---|---| | 0h | **[Default]** | TLB Prefetch Disabled | | 1h | | TLB Prefetch Enabled |
8	**Reserved**
7	**Reserved** | | | |---|---| | Access: | R/W | | Format: | PBC |
6	**STC Read-Hit Wonly Optimization Disable** | | | |---|---| | Access: | R/W | | Format: | Disable | Setting this bit will disable the RHWO optimization of STC-cache. The access on encountering a RHWO will wait for the ref-cnt to go, evict the Cache-line and sends a miss-req to memory to fill the Cache-line | Value | Name | |---|---| | 0h | **[Default]** | | 1h | |

CACHE_MODE_0 - Cache Mode Register 0

5 STC PMA Optimization Disable

Access:	R/W
Format:	Disable

Setting this bit will force the STC cache to wait for pending retirement of pixels at the HZ-read stage and do the STC-test for Non-promoted, R-computed and Computed depth modes instead of postponing the STC-test to RCPFE.

Value	Name	Description
0h	Enable **[Default]**	STC PMA optimization is enabled.
1h	Disable	STC PMA optimization is disabled.

4 RCC Eviction Policy

Access:	R/W
Format:	Disable

If this bit is set, RCCunit will have LRA as replacement policy. The default value i.e. (when this bit is reset) indicates that non-LRA eviction policy. This bit must be reset. LRA replacement policy is not supported.

3 Reserved

1 Disable clock gating in the pixel backend

Access:	R/W
Format:	Disable

MCL related clock gating is disabled in the pixel backend. Before setting this bit to 1, the instruction/state caches must be invalidated.

0 Disable Byte sharing for 3D TYF LOD1 surfaces for 32/64/128 bpp

Access:	R/W

Value	Name	Description
1		Enable byte sharing for 3D TYF LOD1 surfaces - 32/64/128 bpp
0	**[Default]**	Disable Byte Sharing for 3D TYF surfaces LOD1 , 32/64/128 bpp

Cache Mode Register 1

CACHE_MODE_1 - Cache Mode Register 1

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	32
Reset:	DEV
Address:	07004h
Name:	Cache Mode Register 1
ShortName:	CACHE_MODE_1

Description
RegisterType: MMIO_SVL
Before changing the value of this register, GFX pipeline must be idle; i.e., full flush is required. This Register is saved and restored as part of Context.

DWord	Bit	Description
0	31:16	**Mask** Access: WO Mask: MASK Format: Mask[15:0] Must be set to modify corresponding data bit. Reads to this field returns zero.
	15	**Color Compression Disable** Access: R/W Setting this bit causes Lossless Render Target Color Compression to be disabled in Classic Clear (1x) Mode of Operation. Default value, i.e. resetting this bit, Enables Color Compression in Classic Clear Mode (1x) when CCS is Enabled. Value / Name / Description: 0h **[Default]** Enables Color Compression in Classic Clear Mode (1x) when CCS is Enabled. 1h Causes Lossless Render Target Color Compression to be disabled in Classic Clear (1x) Mode of Operation **Programming Notes** The Below programming forces Color Compression to be disabled for MSAA modes explicitly as

	a HW WA. When switching from 1x ==> MSAA. Program this bit to 1 When switching from MSAA ==> 1x. Program this bit to 0
14	**Render Target 64B Read Disabled by RCC**

Access:	R/W
Format:	U1

Setting this bit causes RCC to disable 64B reads and switch to legacy 128B Reads per RCC CL

Value	Name
1h	
0h	**[Default]**

13 **NP EARLY Z FAILS DISABLE**

Access:	R/W

Value	Name	Description
0h	**[Default]**	IZ does conservatively fail any NP/R pixels.
1h		Disables IZ to conservatively fail pixels.

12 **Reserved**

Access:	R/W
Format:	PBC

11 **Reserved**

Access:	R/W
Format:	PBC

10 **Reserved**

Access:	R/W
Format:	PBC

9 **MSC RAW Hazard Avoidance Bit**

Access:	R/W
Format:	Enable

When this field is set, MSC will enable RAW Hazard prevention mechanism, when lossless compression is enabled.

Value	Name	Programming Notes

CACHE_MODE_1 - Cache Mode Register 1

	0h	**[Default]**	
	1h		This field should be programmed to 1 only if need arise to avoid RAW hazard when lossless compression is enabled

8:7 Reserved

Format:	PBC

6 Reserved

Access:	R/W
Format:	PBC

5 MCS Cache Disable

Access:	R/W
Format:	Disable

For Programming restrictions please refer to the 3D Pipeline.

Value	Name	Description
0h	**[Default]**	MCS cache enabled. It allows RTs with MCS buffer enabled to be rendered using either MSAA compression for MSRT OR with color clear feature for non MSRT.
1h		MCS cache is disabled. Hence no MSAA compression for MSRT and no color clear for non-MSRT.

4 Reserved

Access:	R/W
Format:	PBC

3 RCZ PMA Promoted 2 Not-Promoted Allocation stall optimization Disable

Access:	R/W

Setting this bit will force the RCZ cache to stall at the allocation of a CL until the old Promoted writes retire in the RCZ$. Default mode is to stall at the IZ-read point until promoted writes are complete.

Value	Name	Description
0h	**[Default]**	[] Optimization is enabled
1h		Optimization is disabled

2 Reserved

CACHE_MODE_1 - Cache Mode Register 1

Access:	R/W	
Format:	Disable	

1 **YCoCg DIsable**

Access:	R/W
Format:	Disable

Value	Name	Description
0h	**[Default]**	YCoCg will be enabled by Default
1h		Setting this bit to 1 will disable YCoCg Compression and only compress using legacy RGB color space

0 **Disable Lossless Compression of partial Evictions on Previous Uncompressed Cache line**

Access:	R/W
Format:	PBC

Value	Name	Description
0h	**[Default]**	Lossless Compression of partial Evictions on Previous Uncompressed Cache line is Enabled
1h		Lossless Compression of partial Evictions on Previous Uncompressed Cache line is Disabled

Cache Mode Subslice Register

CACHE_MODE_SS - Cache Mode Subslice Register

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	0E420h

DWord	Bit	Description
0	31:16	**Mask Bits** Format: Mask[15:0] Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15:12	**Reserved** Format: MBZ
	11	**Per Sample Blend Opt Disable** Format: Enable Value / Name / Programming Notes: 0h **[Default]** Keeping this Field to default 0 will enable Per Sample Blend Optimization in DAPRSS 1h Setting this Field to 1 will disable Per Sample Blend Optimization in DAPRSS
	10:5	**Reserved** Format: MBZ
	4	**Float Blend Optimization Enable** Access: R/W Format: Enable Value / Name / Description: 0h **[Default]** Disables blend optimization for floating point RTs. 1h Enables blend optimization for floating point RTs.
	3:2	**Reserved** Format: MBZ

CACHE_MODE_SS - Cache Mode Subslice Register

	1	**Instruction Level 1 Cache and In-Flight Queue Disable** Format: Disable **Value** / **Name** / **Description** 0h **[Default]** — Cache is enabled. 1h — Cache is disabled and all accesses to this cache are treated as misses and sent to L2 cache. Setting this bit overrides the setting of bit 0.
	0	**Instruction Level 1 Cache Disable** Format: Disable **Value** / **Name** / **Description** 0h **[Default]** — Cache is enabled. 1h — Cache is disabled and all accesses to this cache are treated as misses, but only requests with unique addresses are sent to the L2.

Capabilities A

CAPID0_A_0_2_0_PCI - Capabilities A

Register Space:	PCI: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00044h

Populated by pulling relevant fuses.

DWord	Bit	Description
0	31:11	**Spare Fuses** Default Value: 00000000000000000000b Access: RO Variant
	10:4	**DEVID SKU Fuse** Default Value: 000000b Access: RO Variant
	3	**VGT Enable Fuse** Default Value: 0b Access: RO Variant
	2	**Pinning Capable Fuse** Default Value: 0b Access: RO Variant
	1	**SVM Disable Fuse** Default Value: 0b Access: RO Variant
	0	**Vtd Disable Fuse** Default Value: 0b Access: RO Variant

Capabilities B

CAPID0_B_0_2_0_PCI - Capabilities B		
Register Space:	PCI: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00048h	
Populated by pulling relevant fuses.		
DWord	**Bit**	**Description**
0	31:0	**Reserved Fuses** Default Value: 0b Access: RO

CDCLK_CTL

CDCLK_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	46000h-46003h
Name:	CD Clock Control
ShortName:	CDCLK_CTL
Power:	PG0
Reset:	global

This register is not reset by the device 2 FLR.

Restriction
These fields should only be changed as part of the Display Sequences for Changing CD Clock Frequency.

DWord	Bit	Description
0 **Programming Notes:** Gen11	31:24	**Reserved** Format: MBZ
	23:22	**CD2X Divider Select** Access: Double Buffered Double Buffer Update Point: Pipe off or start of vertical blank This field selects how the CDCLK PLL output is divided before driving the display CD2X clock. This field is double buffered to align with the pipe from CD2X Pipe Select. It will update at the start of vertical blank of the selected pipe, or immediately if the selected pipe is disabled or no pipe is selected. **Value** / **Name** 00b: Divide by 1 10b: Divide by 2 **[Default]** **Restriction** CD2X Divider Select must not be changed while more than one pipe is enabled. When one pipe is enabled, the CD2X Pipe Select must be set to that pipe before changing CD2X Divider Select.
	21:19	**CD2X Pipe Select**

This field selects the pipe enable and vertical blank to be used for double buffering the CD2X Divider Select.

Value	Name	Description
000b	Pipe A	
010b	Pipe B	
110b	Pipe C	
111b	None	Double buffer enable is tied to 1 so that writes to the CD2X Divider Select will take effect immediately.

18 **Reserved**

17 **Reserved**

16 **SSA Precharge Enable**

This field is unused.

Value	Name
0b	Disable

15 **Reserved**

14:11 **Reserved**

Format:	MBZ

10:0 **CD Frequency Decimal**

Format:	U10.1

This field selects the decimal value of the frequency for CD clock, which is used to generate divided down clocks for some display engine timers. This value is represented in a 10.1 format with 10 integer bits and 1 fractional bit.

Program this field to select the pre-defined value that matches the CD frequency chosen by the CDCLK PLL and CD2X Divider. If no value is defined, program this field with the CD frequency, rounded to the closest 0.5, then minus one.

Value	Name	Description
00 1010 0111 0b	168 MHz CD **[Default]**	This value is default, but not valid.
00101011000b	172.8 MHz CD	
0010110 0110b	180 MHz CD	
00101111110b	192 MHz CD	
01001100100b	307.2 MHz CD	

CDCLK_CTL				
		01 0011 0111 0b	312 MHz CD	
		10 0010 0111 0b	552 MHz CD	
		10 0010 1100 0b	556.8 MHz CD	
		10 1000 0111 0b	648 MHz CD	
		10 1000 1100 0b	652.8 MHz CD	

CDCLK_PLL_ENABLE

CDCLK_PLL_ENABLE

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	46070h-46073h
Name:	CDCLK PLL Enable
ShortName:	CDCLK_PLL_ENABLE
Power:	Always on
Reset:	soft

This register is used to control the CDCLK PLL.

DWord	Bit	Description
0	31	**PLL Enable** This field enables or disables the CDCLK PLL. Value / Name: 0b – Disable 1b – Enable
	30	**PLL Lock** Access: RO This fields indicates the status of the CDCLK PLL Lock. Value / Name: 0b – Not locked or not enabled 1b – Locked
	29:28	**Reserved** Format: MBZ
	27:26	**Reserved** Format: MBZ
	25:24	**Reserved** Format: MBZ
	23:22	**Reserved** Format: MBZ

CDCLK_PLL_ENABLE

	21:12	**Reserved** Format: MBZ
	11	**Reserved** Format: MBZ
	10:8	**Reserved** Format: MBZ
	7:0	**PLL Ratio** This field selects the CDCLK PLL divider ratio, controlling the output frequency. Refer to the Clocks page for valid ratios to program.

Value	Name	Description
1Ch	28 default **[Default]**	Default value. Refer to the Clocks page for valid ratios to program.

Restriction
This field must be configured before enabling CDCLK PLL and not changed while it is enabled.

CGE_CTRL

CGE_CTRL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank
Address:	49080h-49083h
Name:	Pipe Color Gamut Enhancement Control
ShortName:	CGE_CTRL_A
Power:	PG1
Reset:	soft
Address:	49180h-49183h
Name:	Pipe Color Gamut Enhancement Control
ShortName:	CGE_CTRL_B
Power:	PG2
Reset:	soft
Address:	49280h-49283h
Name:	Pipe Color Gamut Enhancement Control
ShortName:	CGE_CTRL_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31	**CGE Enable** This bit enables the Color Gamut Enhancement logic. Value: 0b – Disable; 1b – Enable
	30:0	**Reserved** Format: MBZ

CGE_WEIGHT

CGE_WEIGHT	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	160
Address:	49090h-490A3h
Name:	Pipe Color Gamut Enhancement Weights
ShortName:	CGE_WEIGHT_A
Power:	PG1
Reset:	soft
Address:	49190h-491A3h
Name:	Pipe Color Gamut Enhancement Weights
ShortName:	CGE_WEIGHT_B
Power:	PG2
Reset:	soft
Address:	49290h-492A3h
Name:	Pipe Color Gamut Enhancement Weights
ShortName:	CGE_WEIGHT_C
Power:	PG2
Reset:	soft

These are the weights contained in the lookup up table (LUT) used in pipe color gamut enhancement. LUT index 0 contains the weight for the least saturated colors, and LUT index 16 contains the weight for the most saturated colors. Weight values can range from 00000b (100% of the enhanced output color is from the pipe gamma and CSC output corrected color) to 100000b (100% of the enhanced output color is from the pipe gamma and CSC input color).

Restriction
The weight values should only be changed while color gamut enhancement is disabled, otherwise screen artifacts may show temporarily.

DWord	Bit	Description
0	31:30	**Reserved** Format: MBZ
	29:24	**CGE Weight Index 3** This is the weight value for this color gamut enhancement LUT index.
	23:22	**Reserved**

CGE_WEIGHT			
		Format:	MBZ
	21:16	**CGE Weight Index 2** This is the weight value for this color gamut enhancement LUT index.	
	15:14	**Reserved**	
		Format:	MBZ
	13:8	**CGE Weight Index 1** This is the weight value for this color gamut enhancement LUT index.	
	7:6	**Reserved**	
		Format:	MBZ
	5:0	**CGE Weight Index 0** This is the weight value for this color gamut enhancement LUT index.	
1	31:30	**Reserved**	
		Format:	MBZ
	29:24	**CGE Weight Index 7** This is the weight value for this color gamut enhancement LUT index.	
	23:22	**Reserved**	
		Format:	MBZ
	21:16	**CGE Weight Index 6** This is the weight value for this color gamut enhancement LUT index.	
	15:14	**Reserved**	
		Format:	MBZ
	13:8	**CGE Weight Index 5** This is the weight value for this color gamut enhancement LUT index.	
	7:6	**Reserved**	
		Format:	MBZ
	5:0	**CGE Weight Index 4** This is the weight value for this color gamut enhancement LUT index.	
2	31:30	**Reserved**	
		Format:	MBZ
	29:24	**CGE Weight Index 11** This is the weight value for this color gamut enhancement LUT index.	
	23:22	**Reserved**	
		Format:	MBZ
	21:16	**CGE Weight Index 10** This is the weight value for this color gamut enhancement LUT index.	
	15:14	**Reserved**	
		Format:	MBZ

CGE_WEIGHT		
	13:8	**CGE Weight Index 9** This is the weight value for this color gamut enhancement LUT index.
	7:6	**Reserved** Format: MBZ
	5:0	**CGE Weight Index 8** This is the weight value for this color gamut enhancement LUT index.
3	31:30	**Reserved** Format: MBZ
	29:24	**CGE Weight Index 15** This is the weight value for this color gamut enhancement LUT index.
	23:22	**Reserved** Format: MBZ
	21:16	**CGE Weight Index 14** This is the weight value for this color gamut enhancement LUT index.
	15:14	**Reserved** Format: MBZ
	13:8	**CGE Weight Index 13** This is the weight value for this color gamut enhancement LUT index.
	7:6	**Reserved** Format: MBZ
	5:0	**CGE Weight Index 12** This is the weight value for this color gamut enhancement LUT index.
4	31:6	**Reserved** Format: MBZ
	5:0	**CGE Weight Index 16** This is the weight value for this color gamut enhancement LUT index.

Clipper Invocation Counter

CL_INVOCATION_COUNT - Clipper Invocation Counter	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02338h-0233Fh
Name:	Clipper Invocation Counter
ShortName:	CL_INVOCATION_COUNT_RCSUNIT_BE_GEOMETRY
Address:	18338h-1833Fh
Name:	Clipper Invocation Counter
ShortName:	CL_INVOCATION_COUNT_POCSUNIT_BE_GEOMETRY
Address:	02338h-0233Fh
Name:	Clipper Invocation Counter
ShortName:	CL_INVOCATION_COUNT_RCSUNIT_BE
Address:	18338h-1833Fh
Name:	Clipper Invocation Counter
ShortName:	CL_INVOCATION_COUNT_POCSUNIT_BE

This register stores the count of objects entering the Clipper stage. This register is part of the context save and restore.

DWord	Bit	Description
0	63:32	**CL Invocation Count Report UDW** Number of objects entering the clipper stage. Updated only when Statistics Enable is set in CLIP_STATE (see the Clipper Chapter in the 3D Volume.)
	31:0	**CL Invocation Count Report LDW** Number of objects entering the clipper stage. Updated only when Statistics Enable is set in CLIP_STATE (see the Clipper Chapter in the 3D Volume.)

Clipper Primitives Counter

CL_PRIMITIVES_COUNT - Clipper Primitives Counter	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02340h-02347h
Name:	Clipper Primitives Counter
ShortName:	CL_PRIMITIVES_COUNT_RCSUNIT_BE_GEOMETRY
Address:	18340h-18347h
Name:	Clipper Primitives Counter
ShortName:	CL_PRIMITIVES_COUNT_POCSUNIT_BE_GEOMETRY
Address:	02340h-02347h
Name:	Clipper Primitives Counter
ShortName:	CL_PRIMITIVES_COUNT_RCSUNIT_BE
Address:	18340h-18347h
Name:	Clipper Primitives Counter
ShortName:	CL_PRIMITIVES_COUNT_POCSUNIT_BE

This register reflects the total number of primitives that have been output by the clipper. This register is part of the context save and restore.

DWord	Bit	Description
0	63:32	**Clipped Primitives Output Count UDW** Total number of primitives output by the clipper stage. This count is updated for every primitive output by the clipper stage, as long as Statistics Enable is set in SF_STATE (see the Clipper and SF Chapters in the 3D Volume.)
	31:0	**Clipped Primitives Output Count LDW** Total number of primitives output by the clipper stage. This count is updated for every primitive output by the clipper stage, as long as Statistics Enable is set in SF_STATE (see the Clipper and SF Chapters in the 3D Volume.)

Clock Gating Messages

CGMSG - Clock Gating Messages

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	08104h

Clock Gating Messages Register

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:7	**Reserved** Access: RO Reserved
	6	**Posh Clock gating control message** Access: R/W Gate Posh Clock Message : '0' : Clock Un-gate Request (un-gates the scmsclk clock) '1' : Clock Gate Request (gates the scmsclk clock)
	5	**Media sampler Clock gating control message** Access: R/W Gate Media sampler Clock Message : '0' : Clock Un-gate Request (un-gates the scmsclk clock) '1' : Clock Gate Request (gates the scmsclk clock)
	4	**WIDI 1 Clock gating control message** Access: R/W Gate WIDI 1 (2nd Vbox) Clock gate Message : '0' : WIDI 1 Clock Un-gate Request (un-gates the cmclk clock in the 2nd wigig block) '1' : WIDI 1 Clock Gate Request (gates the cmclk clockin the 2nd Media block)
	3	**WIDI 0 CLock Gating control Message**

		Access: R/W Gate WIDI 0 Clock Message : '0' : WIDI 0 Clock Un-gate Request (un-gates the cwclk clock) '1' : WIDI 0 Clock Gate Request (gates the cwclk clock)
	2	**Reserved**
	1	**Fix Function Clock gating Control Message** Access: R/W Gate Fix Clock Message : '0' : Fix Clock Un-gate Request (un-gates the cfclk/cf2xclk clock) '1' : Fix Clock Gate Request (gates the cfclk/cf2xclk clock)
	0	**Row Clock Gating Control Message** Access: R/W Gate Row Clocks Message : '0' : Row Clock Un-gate Request (un-gates the crclk and cr2xclk clocks) '1' : Row Clock Gate Request (gates the crclk and cr2xclk clocks)

Command Buffer Caching Control Register

CMD_BUF_CCTL - Command Buffer Caching Control Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	02084h-02087h
Name:	CMD_BUF_CCTL
ShortName:	CMD_BUF_CCTL_RCSUNIT
Address:	18084h-18087h
Name:	CMD_BUF_CCTL
ShortName:	CMD_BUF_CCTL_POCSUNIT
Address:	22084h-22087h
Name:	CMD_BUF_CCTL
ShortName:	CMD_BUF_CCTL_BCSUNIT
Address:	1C0084h-1C0087h
Name:	CMD_BUF_CCTL
ShortName:	CMD_BUF_CCTL_VCSUNIT0
Address:	1C4084h-1C4087h
Name:	CMD_BUF_CCTL
ShortName:	CMD_BUF_CCTL_VCSUNIT1
Address:	1C8084h-1C8087h
Name:	CMD_BUF_CCTL
ShortName:	CMD_BUF_CCTL_VECSUNIT0
Address:	1D0084h-1D0087h
Name:	CMD_BUF_CCTL
ShortName:	CMD_BUF_CCTL_VCSUNIT2

CMD_BUF_CCTL - Command Buffer Caching Control Register

Address:	1D4084h-1D4087h
Name:	CMD_BUF_CCTL
ShortName:	CMD_BUF_CCTL_VCSUNIT3

Address:	1D8084h-1D8087h
Name:	CMD_BUF_CCTL
ShortName:	CMD_BUF_CCTL_VECSUNIT1

Address:	1E0084h-1E0087h
Name:	CMD_BUF_CCTL
ShortName:	CMD_BUF_CCTL_VCSUNIT4

Address:	1E4084h-1E4087h
Name:	CMD_BUF_CCTL
ShortName:	CMD_BUF_CCTL_VCSUNIT5

Address:	1E8084h-1E8087h
Name:	CMD_BUF_CCTL
ShortName:	CMD_BUF_CCTL_VECSUNIT2

Address:	1F0084h-1F0087h
Name:	CMD_BUF_CCTL
ShortName:	CMD_BUF_CCTL_VCSUNIT6

Address:	1F4084h-1F4087h
Name:	CMD_BUF_CCTL
ShortName:	CMD_BUF_CCTL_VCSUNIT7

Address:	1F8084h-1F8087h
Name:	CMD_BUF_CCTL
ShortName:	CMD_BUF_CCTL_VECSUNIT3

This register informs the size of the command buffer cache allocated in L3 for DMA requests from RenderCS. This register also defines the MOCS index that need be send on command buffer read request to be cached in L3. This register is an non-privileged register and engine context saved and restored.

CMD_BUF_CCTL - Command Buffer Caching Control Register

Programming Notes
This register is only functional on RenderCS and must be only programmed on RenderCS.

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask Mask bits act as write enables for the bits in the lower bits of this register
	15:12	**Reserved**
	11:8	**Command Buffer Cache Size** Format: U4 The value programmed to this field should be less than or equal to the actual physical cache space reserved in L3 for command buffercaching through L3 configuration. Command buffer DMA engine uses the cache size programmed in this field to limit the read requests of a cacheable batch buffer to be cached in L3. DMA engine does this by tracking the amount of read requests made cacheable and stops caching when the read requested data size equals to the size of the command cache allocated. DMA engine resets the command caching tracker on events listed below. This avoids thrashing of cache for Batch Buffers larger in size compared to the command buffer cache allocated in L3. • On an End Of Tile in PTRBR/POSH mode of operation. • On a context save of a context. • On command cache invalidation through PIPE_CONTROL.

Value	Name	Description
0h	Cache Size Zero	Size of the command buffer cache allocated in L3 is 0KB
1h	Cache Size 16 KB	Size of the command buffer cache allocated in L3 is 16KB
2h	Cache Size 32 KB	Size of the command buffer cache allocated in L3 is 32KB
3h	Cache Size 64 KB	Size of the command buffer cache allocated in L3 is 64KB
4h	Cache Size 128 KB	Size of the command buffer cache allocated in L3 is 128KB
5h	Cache Size 256 KB	Size of the command buffer cache allocated in L3 is 256KB
6h	Cache Size 512 KB	Size of the command buffer cache allocated in L3 is 512KB
7h,8h,9h, Ah, Bh, Ch, Dh, Eh, Fh	Reserved	Reserved.

CMD_BUF_CCTL - Command Buffer Caching Control Register		
	7	**Reserved** Format: MBZ
	6:0	**Memory Object Control State (MOCS) for Command Buffer Caching** Format: MEMORY_OBJECT_CONTROL_STATE This field has the standard format defined for MOCS globally. “Index to MOCS Tables” field of MOCS is used for L3 and System cache memory properties. “Index to MOCS Tables” attribute of this field is used for defining the caching properties for requests made for batch buffer command fetches.

Config Access Range Register Base

CARR_BASE - Config Access Range Register Base	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	04150h
Name:	Config Access Range Register 0 Base
ShortName:	CARR0_Base
Address:	04158h
Name:	Config Access Range Register 1 Base
ShortName:	CARR1_Base
Address:	04160h
Name:	Config Access Range Register 2 Base
ShortName:	CARR2_Base
Address:	04168h
Name:	Config Access Range Register 3 Base
ShortName:	CARR3_Base
Address:	04170h
Name:	Config Access Range Register 4 Base
ShortName:	CARR4_Base
Address:	04178h
Name:	Config Access Range Register 5 Base
ShortName:	CARR5_Base
Address:	04180h
Name:	Config Access Range Register 6 Base
ShortName:	CARR6_Base
Address:	04188h

CARR_BASE - Config Access Range Register Base

Name: Config Access Range Register 7 Base

ShortName: CARR7_Base

CS Config access ranger register - Base address and permission

DWord	Bit	Description
0	31	**Lock** Default Value: 0b Access: R/W Lock Lock bit. Expected to be set by BIOS after programming. 0: Register can be accessed from IA or HW accesses 1: Register can only be accessed with HW accesses
	30:23	**Reserved** Default Value: 0000000000000000b Access: RO
	22:2	**Base Address** Default Value: 000000h Access: R/W Lock Base address of the config address range defined by this CARR
	1	**Access** Default Value: 0b Access: R/W Lock Access permissions for the config address range defined by this CARR. 0: Read access only 1: Both Read and Write access
	0	**Valid** Default Value: 0b Access: R/W Lock Config address ranger defined by this CARR is valid, and is compared against incoming CS config accesses. If within range, the access is allowed. If Valid=0, the range register does not participate in range checking. If none of the CARRs are valid, no range checking is done.

Configuration Register0 for RPMunit

CONFIG0 - Configuration Register0 for RPMunit

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00D00h

Lock bit LOCK applies to all RW/L fields in this register. Lock is overridden during context restore.

DWord	Bit	Description
0	31	**Lock for RW/L Fields in this Register** Access: R/W Lock 0 = Bits of CONFIG0 register are R/W. 1 = All bits of CONFIG0 register are RO (including this lock bit). Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). Lock is reset on a restore after context is captured.
	30	**Engineering Sample Indicator** Access: R/W Lock This bit defines whether the part is an engineering sample/Pre-Production part
	29:6	**Placeholder Bits** Access: R/W Lock
	5:3	**Crystal Clock Freq Selector** Access: RO This indicates the crystal clock frequency. BIOS will read this bit and then program the shift parameters, below, appropriately
	2:1	**CTC SHIFT parameter** Default Value: 10b

Value	Name
0	Crystal clock is at 24 MHz **[Default]**
1	Crystal clock is at 19.2 MHz
10	Crystal clock is at 38.4 MHz
11	Crystal clock is at 25 MHz
100	Rsvd for future use

CONFIG0 - Configuration Register0 for RPMunit		
		Access: R/W Lock 00 - use bit 7 as “microsecond”, bit 3 as lowest *CS timestamp 01 - use bit 6 as “microsecond”, bit 2 as lowest *CS timestamp 10 - use bit 5 as “microsecond”, bit 1 as lowest *CS timestamp (default) 11 - use bit 4 as “microsecond”, bit 0 as lowest *CS timestamp
	0	**Disable TSC Synchronization** Access: R/W Lock 'b0 - TSC synchronization enabled in GT (default) 'b1 - TSC synchronization DISABLED in GT

Configuration Register1 for RPMunit

CONFIG1 - Configuration Register1 for RPMunit

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00D04h

Lock bit LOCK applies to all RW/L fields in this register. Lock is overridden during context restore.

DWord	Bit	Description
0	31	**Lock for RW/L Fields in this Register** Access: R/W Lock 0 = Bits of CONFIG0 register are R/W. 1 = All bits of CONFIG0 register are RO (including this lock bit). Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). Lock is reset on a restore after context is captured.
	30:10	**Placeholder Bits** Access: R/W Lock
	9	**Reserved**
	8:0	**RCP L3 FREQ DETECT** Default Value: 000011110b Access: R/W Lock This is control signal needed from clock unit that can be set at 1 when 2X clock frequency is less than or equal to 1GHz. It needs to be at 0 when 2X clock frequency is >1GHz. Without this circuit changes, the GT L3 cache will not be functional at lower frequency due to Vcc is less than Vccmin of 0.9V for the array. default value: low2xthresh=0x01Eh corresponding to a 1x frequency of 500Mhz.

Context Restore Request To TDL

TDL_CONTEXT_RESTORE - Context Restore Request To TDL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	WO
Size (in bits):	32
Address:	0E418h

DWord	Bit	Description
0	31:17	**Reserved** Format: MBZ
	16	**Context Restore Mask** Value: 1 — Name: — Description: Bit 0 and bit 16 both need to be 1 for Context restore request
	15:1	**Reserved** Format: MBZ
	0	**Context Restore** Value: 1 — Name: — Description: Bit 0 and bit 16 both need to be 1 for Context restore request

Context Sizes

CXT_SIZE - Context Sizes

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	021A8h

The actual size of a logical rendering context is the amount of data stored/restored during a context switch and is measured in 64B cache lines.

This register will be power context save/restored. Note that this register will default to the correct value, so software should not have to modify it.

DWord	Bit	Description
0	31:28	**Reserved** Format: MBZ
	27:16	**Render Engine Context Size** This field indicates the size of the render engine context data that needs to be save/restored when extended mode is not enabled for a context; this excludes URB context size. Note that this excludes the ring context image size and the engine context saved by CSFE. Value: 15Eh — Name: **[Default]**
	15:8	**SOL Context Offset** This field indicates the cacheline aligned offset of the SOL context in the render context image starting from Ring Context. Note that in execlist of scheduling Ring context itself is at 4KB offset from LRCA. Value: 66h — Name: **[Default]**
	7:0	**Reserved** Format: MBZ

Context Status Buffer1 Contents

CTXT_ST_BUF1 - Context Status Buffer1 Contents	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	384
Trusted Type:	1
Address:	023C0h-023EFh
Name:	Context Status Buffer1 Contents
ShortName:	CTXT_ST_BUF1_RCSUNIT
Address:	183C0h-183EFh
Name:	Context Status Buffer1 Contents
ShortName:	CTXT_ST_BUF1_POCSUNIT
Address:	223C0h-223EFh
Name:	Context Status Buffer1 Contents
ShortName:	CTXT_ST_BUF1_BCSUNIT
Address:	1C03C0h-1C03EFh
Name:	Context Status Buffer1 Contents
ShortName:	CTXT_ST_BUF1_VCSUNIT0
Address:	1C43C0h-1C43EFh
Name:	Context Status Buffer1 Contents
ShortName:	CTXT_ST_BUF1_VCSUNIT1
Address:	1C83C0h-1C83EFh
Name:	Context Status Buffer1 Contents
ShortName:	CTXT_ST_BUF1_VECSUNIT0
Address:	1D03C0h-1D03EFh
Name:	Context Status Buffer1 Contents
ShortName:	CTXT_ST_BUF1_VCSUNIT2

CTXT_ST_BUF1 - Context Status Buffer1 Contents

Address:	1D43C0h-1D43EFh
Name:	Context Status Buffer1 Contents
ShortName:	CTXT_ST_BUF1_VCSUNIT3

Address:	1D83C0h-1D83EFh
Name:	Context Status Buffer1 Contents
ShortName:	CTXT_ST_BUF1_VECSUNIT1

Address:	1E03C0h-1E03EFh
Name:	Context Status Buffer1 Contents
ShortName:	CTXT_ST_BUF1_VCSUNIT4

Address:	1E43C0h-1E43EFh
Name:	Context Status Buffer1 Contents
ShortName:	CTXT_ST_BUF1_VCSUNIT5

Address:	1E83C0h-1E83EFh
Name:	Context Status Buffer1 Contents
ShortName:	CTXT_ST_BUF1_VECSUNIT2

Address:	1F03C0h-1F03EFh
Name:	Context Status Buffer1 Contents
ShortName:	CTXT_ST_BUF1_VCSUNIT6

Address:	1F43C0h-1F43EFh
Name:	Context Status Buffer1 Contents
ShortName:	CTXT_ST_BUF1_VCSUNIT7

Address:	1F83C0h-1F83EFh
Name:	Context Status Buffer1 Contents
ShortName:	CTXT_ST_BUF1_VECSUNIT3

All "Context Status* LDW" have the format of the Bits[31:0] of the "Context Status" definition.
All "Context Status* UDW" have the format of the Bits[61:32] of the "Context Status" definition.

CTXT_ST_BUF1 - Context Status Buffer1 Contents

Programming Notes
This structure contains the Context Switch status locations Context Status 6 to Context Status 11.

DWord	Bit	Description
0	63:32	**Context Status 6 UDW** Format: U32
	31:0	**Context Status 6 LDW** Format: U32
1	63:32	**Context Status 7 UDW** Format: U32
	31:0	**Context Status 7 LDW** Format: U32
2	63:32	**Context Status 8 UDW** Format: U32
	31:0	**Context Status 8 LDW** Format: U32
3	63:32	**Context Status 9 UDW** Format: U32
	31:0	**Context Status 9 LDW** Format: U32
4	63:32	**Context Status 10 UDW** Format: U32
	31:0	**Context Status 10 LDW** Format: U32
5	63:32	**Context Status 11 UDW** Format: U32
	31:0	**Context Status 11 LDW** Format: U32

Context Status Buffer Contents

CTXT_ST_BUF - Context Status Buffer Contents	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	384
Trusted Type:	1
Address:	02370h-0239Fh
Name:	Context Status Buffer Contents
ShortName:	CTXT_ST_BUF_RCSUNIT
Address:	18370h-1839Fh
Name:	Context Status Buffer Contents
ShortName:	CTXT_ST_BUF_POCSUNIT
Address:	22370h-2239Fh
Name:	Context Status Buffer Contents
ShortName:	CTXT_ST_BUF_BCSUNIT
Address:	1C0370h-1C039Fh
Name:	Context Status Buffer Contents
ShortName:	CTXT_ST_BUF_VCSUNIT0
Address:	1C4370h-1C439Fh
Name:	Context Status Buffer Contents
ShortName:	CTXT_ST_BUF_VCSUNIT1
Address:	1C8370h-1C839Fh
Name:	Context Status Buffer Contents
ShortName:	CTXT_ST_BUF_VECSUNIT0
Address:	1D0370h-1D039Fh
Name:	Context Status Buffer Contents
ShortName:	CTXT_ST_BUF_VCSUNIT2

CTXT_ST_BUF - Context Status Buffer Contents

Address:	1D4370h-1D439Fh
Name:	Context Status Buffer Contents
ShortName:	CTXT_ST_BUF_VCSUNIT3

Address:	1D8370h-1D839Fh
Name:	Context Status Buffer Contents
ShortName:	CTXT_ST_BUF_VECSUNIT1

Address:	1E0370h-1E039Fh
Name:	Context Status Buffer Contents
ShortName:	CTXT_ST_BUF_VCSUNIT4

Address:	1E4370h-1E439Fh
Name:	Context Status Buffer Contents
ShortName:	CTXT_ST_BUF_VCSUNIT5

Address:	1E8370h-1E839Fh
Name:	Context Status Buffer Contents
ShortName:	CTXT_ST_BUF_VECSUNIT2

Address:	1F0370h-1F039Fh
Name:	Context Status Buffer Contents
ShortName:	CTXT_ST_BUF_VCSUNIT6

Address:	1F4370h-1F439Fh
Name:	Context Status Buffer Contents
ShortName:	CTXT_ST_BUF_VCSUNIT7

Address:	1F8370h-1F839Fh
Name:	Context Status Buffer Contents
ShortName:	CTXT_ST_BUF_VECSUNIT3

Contents of the Execlist 0 in HW.

All "Context Status* LDW" have the format of the Bits[31:0] of the "Context Status" definition.

CTXT_ST_BUF - Context Status Buffer Contents

All "Context Status* UDW" have the format of the Bits[61:32] of the "Context Status" definition.

Programming Notes	Source
This structure contains the Context Switch status locations Context Status 0 to Context Status 5.	
This register functionality is not supported and must not be programmed for Position command streamer.	PositionCS

DWord	Bit	Description
0	63:32	**Context Status 0 UDW** Format: U32
	31:0	**Context Status 0 LDW** Format: U32
1	63:32	**Context Status 1 UDW** Format: U32
	31:0	**Context Status 1 LDW** Format: U32
2	63:32	**Context Status 2 UDW** Format: U32
	31:0	**Context Status 2 LDW** Format: U32
3	63:32	**Context Status 3 UDW** Format: U32
	31:0	**Context Status 3 LDW** Format: U32
4	63:32	**Context Status 4 UDW** Format: U32
	31:0	**Context Status 4 LDW** Format: U32
5	63:32	**Context Status 5 UDW** Format: U32
	31:0	**Context Status 5 LDW** Format: U32

Context Status Buffer Interrupt Mask Register

CSB_INTERRUPT_MASK - Context Status Buffer Interrupt Mask Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	02218h-0221Bh
Name:	CSB_INTERRUPT_MASK
ShortName:	CSB_INTERRUPT_MASK_RCSUNIT
Address:	18218h-1821Bh
Name:	CSB_INTERRUPT_MASK
ShortName:	CSB_INTERRUPT_MASK_POCSUNIT
Address:	22218h-2221Bh
Name:	CSB_INTERRUPT_MASK
ShortName:	CSB_INTERRUPT_MASK_BCSUNIT
Address:	1C0218h-1C021Bh
Name:	CSB_INTERRUPT_MASK
ShortName:	CSB_INTERRUPT_MASK_VCSUNIT0
Address:	1C4218h-1C421Bh
Name:	CSB_INTERRUPT_MASK
ShortName:	CSB_INTERRUPT_MASK_VCSUNIT1
Address:	1C8218h-1C821Bh
Name:	CSB_INTERRUPT_MASK
ShortName:	CSB_INTERRUPT_MASK_VECSUNIT0
Address:	1D0218h-1D021Bh
Name:	CSB_INTERRUPT_MASK
ShortName:	CSB_INTERRUPT_MASK_VCSUNIT2

CSB_INTERRUPT_MASK - Context Status Buffer Interrupt Mask Register

Address:	1D4218h-1D421Bh
Name:	CSB_INTERRUPT_MASK
ShortName:	CSB_INTERRUPT_MASK_VCSUNIT3

Address:	1D8218h-1D821Bh
Name:	CSB_INTERRUPT_MASK
ShortName:	CSB_INTERRUPT_MASK_VECSUNIT1

Address:	1E0218h-1E021Bh
Name:	CSB_INTERRUPT_MASK
ShortName:	CSB_INTERRUPT_MASK_VCSUNIT4

Address:	1E4218h-1E421Bh
Name:	CSB_INTERRUPT_MASK
ShortName:	CSB_INTERRUPT_MASK_VCSUNIT5

Address:	1E8218h-1E821Bh
Name:	CSB_INTERRUPT_MASK
ShortName:	CSB_INTERRUPT_MASK_VECSUNIT2

Address:	1F0218h-1F021Bh
Name:	CSB_INTERRUPT_MASK
ShortName:	CSB_INTERRUPT_MASK_VCSUNIT6

Address:	1F4218h-1F421Bh
Name:	CSB_INTERRUPT_MASK
ShortName:	CSB_INTERRUPT_MASK_VCSUNIT7

Address:	1F8218h-1F821Bh
Name:	CSB_INTERRUPT_MASK
ShortName:	CSB_INTERRUPT_MASK_VECSUNIT3

Hardware generates context switch interrupt and the associated context switch status report for the context switch reasons unmasked in this register. By default the context switch interrupts for all context switch reasons

CSB_INTERRUPT_MASK - Context Status Buffer Interrupt Mask Register

are un-masked. This register is privileged and global across all contexts and power context save/restored by hardware.
Note that on a context switch status report even the status of the masked context switch reasons are reported.

Programming Notes
Software must program this register through direct MMIO when hardware is idle and not processing any contexts.

DWord	Bit	Description
0	31:8	**Reserved**
	7	**Active to Idle** This mask bit controls the context switch interrupt generation and the associated context switch status report on a context switch leading hardware to go idle. Active-to-Idle is a special case of element switch due to ring done or un-successful semaphore wait or un-successful display wait for event following which hardware goes idle. **Value** / **Name** / **Description** 0 / **[Default]** / Context switch interrupt and associated context switch status report is generated on a context switch leading hardware to go idle. 1 / / Context switch interrupt and associated context switch status report is not generated on a context switch leading hardware to go idle.
	6	**Preempt to Idle** This mask bit controls the context switch interrupt generation and the associated context switch status report on a context switch due to Preempt-to-Idle. **Value** / **Name** / **Description** 0 / **[Default]** / Context switch interrupt and associated context switch status report is generated on a context switch due to Preempt-to-Idle. 1 / / Context switch interrupt and associated context switch status report is not generated on a context switch due to Preempt-to-Idle.
	5	**Lite Restore** This mask bit controls the context switch interrupt generation and the associated context switch status report on a context switch due to lite restore. **Value** / **Name** / **Description** 0 / **[Default]** / Context switch interrupt and associated context switch status report is generated on a context switch due to lite restore. 1 / / Context switch interrupt and associated context switch status report is not generated on a context switch due to lite restore.
	4	**Preemption** This mask bit controls the context switch interrupt generation and the associated context switch status report on a context switch due to preemption. Preemption of an ongoing context is triggered due to loading of submission queue to execution queue on a "Load".

CSB_INTERRUPT_MASK - Context Status Buffer Interrupt Mask Register

Value	Name	Description
0	**[Default]**	Context switch interrupt and associated context switch status report is generated on a context switch due to preemption.
1		Context switch interrupt and associated context switch status report is not generated on a context switch due to preemption.

3 **Display Wait For Event**

This mask bit controls the context switch interrupt generation and the associated context switch status report on Ring-Done context switch.

Value	Name	Description
0	**[Default]**	Context switch interrupt and associated context switch status report is generated on a context switch due to un-successful display wait for event. Context switch on un-successful display wait for even wait is a part of element switch.
1		Context switch interrupt and associated context switch status report is not generated on a context switch due to un-successful display wait for event.

2 **Semaphore Wait**

This mask bit controls the context switch interrupt generation and the associated context switch status report on Ring-Done context switch.

Value	Name	Description
0	**[Default]**	Context switch interrupt and associated context switch status report is generated on a context switch due to un-successful sempahore wait. Context switch on un-successful semaphore wait is a part of element switch.
1		Context switch interrupt and associated context switch status report is not generated on a context switch un-successful semaphore wait.

1 **Ring Done**

This mask bit controls the context switch interrupt generation and the associated context switch status report on Ring-Done context switch.

Value	Name	Description
0	**[Default]**	Context switch interrupt and associated context switch status report is generated on a context switch reason due to Ring-Done. Context switch on ring done is a part of element switch.
1		Context switch interrupt and associated context switch status report is not generated on a context switch due to Ring-Done.

0 **Idle To Active**

This mask bit controls the context switch interrupt generation and the associated context switch status report on Idle-to-Active context switch.

Value	Name	Description
0	**[Default]**	Context switch interrupt and associated context switch status report is generated on a context switch due to Idle-to-Active. Idle2Active is a special

CSB_INTERRUPT_MASK - Context Status Buffer Interrupt Mask Register				
				case of submission queue acceptance by hardware.
		1		Context switch interrupt and associated context switch status report is not generated on a context switch due to Idle-to-Active.

Context Status Buffer Read Register

CSB_STATUS - Context Status Buffer Read Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	023A4h-023A7h
Name:	Context Status Buffer Read Register
ShortName:	CSB_STATUS_RCSUNIT
Address:	183A4h-183A7h
Name:	Context Status Buffer Read Register
ShortName:	CSB_STATUS_POCSUNIT
Address:	223A4h-223A7h
Name:	Context Status Buffer Read Register
ShortName:	CSB_STATUS_BCSUNIT
Address:	1C03A4h-1C03A7h
Name:	Context Status Buffer Read Register
ShortName:	CSB_STATUS_VCSUNIT0
Address:	1C43A4h-1C43A7h
Name:	Context Status Buffer Read Register
ShortName:	CSB_STATUS_VCSUNIT1
Address:	1C83A4h-1C83A7h
Name:	Context Status Buffer Read Register
ShortName:	CSB_STATUS_VECSUNIT0
Address:	1D03A4h-1D03A7h
Name:	Context Status Buffer Read Register
ShortName:	CSB_STATUS_VCSUNIT2
Address:	1D43A4h-1D43A7h

CSB_STATUS - Context Status Buffer Read Register

Name:	Context Status Buffer Read Register
ShortName:	CSB_STATUS_VCSUNIT3

Address:	1D83A4h-1D83A7h
Name:	Context Status Buffer Read Register
ShortName:	CSB_STATUS_VECSUNIT1

Address:	1E03A4h-1E03A7h
Name:	Context Status Buffer Read Register
ShortName:	CSB_STATUS_VCSUNIT4

Address:	1E43A4h-1E43A7h
Name:	Context Status Buffer Read Register
ShortName:	CSB_STATUS_VCSUNIT5

Address:	1E83A4h-1E83A7h
Name:	Context Status Buffer Read Register
ShortName:	CSB_STATUS_VECSUNIT2

Address:	1F03A4h-1F03A7h
Name:	Context Status Buffer Read Register
ShortName:	CSB_STATUS_VCSUNIT6

Address:	1F43A4h-1F43A7h
Name:	Context Status Buffer Read Register
ShortName:	CSB_STATUS_VCSUNIT7

Address:	1F83A4h-1F83A7h
Name:	Context Status Buffer Read Register
ShortName:	CSB_STATUS_VECSUNIT3

This 32 bit address contains the value of the context status that is next to be read by scheduler.

Programming Notes	Source
This register functionality is not supported and must not be programmed for Position command streamer.	PositionCS

DWord	Bit	Description
0	31:0	**Context Status** Access: RO This field contains the value of the Context Status depending on the value of **Context Status Buffer Read Pointer** in the CTXT_ST_PTR. Read Pointer value of zero will point to context status zero, read pointer value of one will pointer to context status one, and so on. The scheduler must read this register twice to get the full 64b of context status. The first read returns the lower DW of the status and the second read returns the upper DW of the status.

Context Timestamp Count

CTX_TIMESTAMP - Context Timestamp Count	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	023A8h-023ABh
Name:	Context Timestamp Count
ShortName:	CTX_TIMESTAMP_RCSUNIT
Address:	183A8h-183ABh
Name:	Context Timestamp Count
ShortName:	CTX_TIMESTAMP_POCSUNIT
Address:	223A8h-223ABh
Name:	Context Timestamp Count
ShortName:	CTX_TIMESTAMP_BCSUNIT
Address:	1C03A8h-1C03ABh
Name:	Context Timestamp Count
ShortName:	CTX_TIMESTAMP_VCSUNIT0
Address:	1C43A8h-1C43ABh
Name:	Context Timestamp Count
ShortName:	CTX_TIMESTAMP_VCSUNIT1
Address:	1C83A8h-1C83ABh
Name:	Context Timestamp Count
ShortName:	CTX_TIMESTAMP_VECSUNIT0
Address:	1D03A8h-1D03ABh
Name:	Context Timestamp Count
ShortName:	CTX_TIMESTAMP_VCSUNIT2
Address:	1D43A8h-1D43ABh
Name:	Context Timestamp Count
ShortName:	CTX_TIMESTAMP_VCSUNIT3
Address:	1D83A8h-1D83ABh
Name:	Context Timestamp Count
ShortName:	CTX_TIMESTAMP_VECSUNIT1

CTX_TIMESTAMP - Context Timestamp Count

Address:	1E03A8h-1E03ABh
Name:	Context Timestamp Count
ShortName:	CTX_TIMESTAMP_VCSUNIT4

Address:	1E43A8h-1E43ABh
Name:	Context Timestamp Count
ShortName:	CTX_TIMESTAMP_VCSUNIT5

Address:	1E83A8h-1E83ABh
Name:	Context Timestamp Count
ShortName:	CTX_TIMESTAMP_VECSUNIT2

Address:	1F03A8h-1F03ABh
Name:	Context Timestamp Count
ShortName:	CTX_TIMESTAMP_VCSUNIT6

Address:	1F43A8h-1F43ABh
Name:	Context Timestamp Count
ShortName:	CTX_TIMESTAMP_VCSUNIT7

Address:	1F83A8h-1F83ABh
Name:	Context Timestamp Count
ShortName:	CTX_TIMESTAMP_VECSUNIT3

This register provides a mechanism to obtain cumulative run time of a GPU context on HW. This register gets context save/restored on a context switch. SW must reset this register on very first submission of a context to HW, then afterwards gets context save/restored maintaining the cumulative run time of the corresponding context. This register (effectively) counts at a constant frequency by adjusting the increment amount according to the actual reference clock frequency. SW therefore does not need to know the reference clock frequency. This register gets reset on an engine reset.

This register is context save restore on a context switch.

DWord	Bit	Description
0	31:0	**Timestamp Value** Format: U32 The granularity of this toggle is at the rate of the bit 3 in the "Reported Timestamp Count" register(0x2358).. The toggle will be 8 times slower that "Reported Timestamp Count". The granularity of the time stamp base unit for "Reported Timestamp Count" is defined in the “Timestamp Bases” subsection in Power Management chapter.

Control Register for Power Management

WAIT_FOR_RC6_EXIT - Control Register for Power Management	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	020CCh-020CFh
Name:	Control Register for Power Management
ShortName:	WAIT_FOR_RC6_EXIT_RCSUNIT
Address:	180CCh-180CFh
Name:	Control Register for Power Management
ShortName:	WAIT_FOR_RC6_EXIT_POCSUNIT
Address:	220CCh-220CFh
Name:	Control Register for Power Management
ShortName:	WAIT_FOR_RC6_EXIT_BCSUNIT
Address:	1C00CCh-1C00CFh
Name:	Control Register for Power Management
ShortName:	WAIT_FOR_RC6_EXIT_VCSUNIT0
Address:	1C40CCh-1C40CFh
Name:	Control Register for Power Management
ShortName:	WAIT_FOR_RC6_EXIT_VCSUNIT1
Address:	1C80CCh-1C80CFh
Name:	Control Register for Power Management
ShortName:	WAIT_FOR_RC6_EXIT_VECSUNIT0
Address:	1D00CCh-1D00CFh
Name:	Control Register for Power Management
ShortName:	WAIT_FOR_RC6_EXIT_VCSUNIT2
Address:	1D40CCh-1D40CFh
Name:	Control Register for Power Management
ShortName:	WAIT_FOR_RC6_EXIT_VCSUNIT3
Address:	1D80CCh-1D80CFh
Name:	Control Register for Power Management

WAIT_FOR_RC6_EXIT - Control Register for Power Management

ShortName:	WAIT_FOR_RC6_EXIT_VECSUNIT1
Address:	1E00CCh-1E00CFh
Name:	Control Register for Power Management
ShortName:	WAIT_FOR_RC6_EXIT_VCSUNIT4
Address:	1E40CCh-1E40CFh
Name:	Control Register for Power Management
ShortName:	WAIT_FOR_RC6_EXIT_VCSUNIT5
Address:	1E80CCh-1E80CFh
Name:	Control Register for Power Management
ShortName:	WAIT_FOR_RC6_EXIT_VECSUNIT2
Address:	1F00CCh-1F00CFh
Name:	Control Register for Power Management
ShortName:	WAIT_FOR_RC6_EXIT_VCSUNIT6
Address:	1F40CCh-1F40CFh
Name:	Control Register for Power Management
ShortName:	WAIT_FOR_RC6_EXIT_VCSUNIT7
Address:	1F80CCh-1F80CFh
Name:	Control Register for Power Management
ShortName:	WAIT_FOR_RC6_EXIT_VECSUNIT3

This register gets power context save/restored. Bit[0] contents of this register does't get save/restored. Note: Even though this register exists in BlitterCS, VideoCS, VidoeEnhancmentCS, individual bit driven functionality is not supported.

Programming Notes	Source
This register is functional for RenderCS only and must not be programmed for other command streamers.	
This register functionality is not supported and must not be programmed for Position command streamer.	PositionCS

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15	**Selective Read Addressing Enable** Source: RenderCS

This field controls the outbound read request originating from Render Command Streamer. This field enables to read the MMIO register from selected unit in a given slice and sub-slice instead of multicasting the read cycle to all slices/sub-slices.

Value	Name	Description
0h	**[Default]**	Lowest Slice and Lowest Sub-Slice Enabled. Ex: Slice-0, Sub-Slice-0 are the lowest in GT.
1h	Selective Unit Enabled	Unit selected based on **Selective Read Slice Select** and **Selective Read Sub-Slice Select**.

14 **Reserved**

Format:	PBC

13:12 **Selective Read Slice Select**

Source:	RenderCS

This field selects the slice from which the read return data value has to be considered when **Selective Read Addressing Enable** is set. Below value must be programmed with a legal value supported by the GT configuration, one must not program this to a slice that is disabled or not supported by GT.

Value	Name
0h	Slice-0
1h	Slice-1
2h	Slice-2
3h	Slice-3

11:9 **Selective Read Sub-Slice Select**

Source:	RenderCS

This field selects the sub-slice from which the read return data value has to be considered when **Selective Read Addressing Enable** is set. Below value must be programmed with a legal value supported by the GT configuration, one must not program this to a sub-slice that is disabled or not supported by GT.

Value	Name
000b	Sub Slice-0
001b	Sub Slice-1
010b	Sub Slice-2
011b	Sub Slice-3
100b	Sub Slice-4
101b	Sub Slice-5
110b	Sub Slice-6

111b	Sub Slice-7

8 Selective Write Addressing Enable

Source:	RenderCS

This field controls the outbound write request on message channel originating from Render Command Streamer on executing LRI, LRR and LRM commands. Setting this field doesn't affect the execution of LRI commands from context image during context restore. This field enables to select the unit in given slice and sub-slice instead of multicasting the write cycle to all slices/half-slices.

Value	Name	Description
0h	Multi Cast **[Default]**	
1h	Selective Unit Enabled	Unit selected based on **Selective Write Slice Select** and **Selective Write Sub-Slice Select**.

Programming Notes
This field is used to implement per-slice performance counting by limiting which slices receive Flex EU programming. Please refer to Flex EU event topic **here** for more details.

7 Reserved

Source:	RenderCS
Format:	PBC

6:5 Selective Write Slice Select

Source:	RenderCS

This field selects the slice to which the write has to be done when **Selective Write Addressing Enable** is set. Below value must be programmed with a legal value supported by the GT configuration, one must not program this to a slice that is disabled or not supported by GT.

Value	Name
000b	Slice-0
001b	Slice-1
010b	Slice-2
011b	Slice-3

Programming Notes
This field is used to implement per-slice performance counting by limiting which slices receive Flex EU programming. Please refer to Flex EU event topic **here** for more details.

4:2 Selective Write Sub-Slice Select

		Source: RenderCS
		This field selects the Sub-Slice to which the write has to be done when **Selective Write Addressing Enable** is set. Below value must be programmed with a legal value supported by the GT configuration, one must not program this to a sub-slice that is disabled or not supported by GT.

Value	Name
000b	Sub Slice-0
001b	Sub Slice-1
010b	Sub Slice-2
011b	Sub Slice-3
100b	Sub Slice-4
101b	Sub Slice-5
110b	Sub Slice-6
111b	Sub Slice-7

	1	**Reserved**
		Source: RenderCS
		Format: PBC
	0	**Reserved**
		Source: RenderCS
		Format: PBC

Count Active Channels Dispatched

TS_GPGPU_THREADS_DISPATCHED - Count Active Channels Dispatched

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02290h
Name:	Count Active Channels Dispatched
ShortName:	TS_GPGPU_THREADS_DISPATCHED

This register is used to count the number of active channels that TS sends for dispatch. For each dispatch the active bits in the execution mask are summed and added to this register. This register is reset when a write occurs to 2290h

DWord	Bit	Description
0..1	63:32	**GPGPU_THREADS_DISPATCHED UDW** Format: U32 This count is increased by the number of active bits in the execution mask each time the TS sends a GPGPU dispatch.
	31:0	**GPGPU_THREADS_DISPATCHED LDW** Format: U32 This count is increased by the number of active bits in the execution mask each time the TS sends a GPGPU dispatch.

CPS Invocation Counter

CPS_INVOCATION_COUNT - CPS Invocation Counter	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02478h
Name:	CPS Invocation Counter
ShortName:	CPS_INVOCATION_COUNT

This register stores the value of the coarse pixel count shaded. This register is part of the context save and restore.

DWord	Bit	Description
0..1	63:32	**CPS Invocation Count Report UDW** Number of coarse pixels that are dispatched as threads by the PS Stage. Updated only when **Statistics Enable** is set in **3DSTATE_CPS**.
	31:0	**CPS Invocation Count Report LDW** Number of coarse pixels that are dispatched as threads by the PS Stage. Updated only when **Statistics Enable** is set in **3DSTATE_CPS**.

CSC_COEFF

CSC_COEFF	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	192
Double Buffer Update Point:	Start of vertical blank after armed
Double Buffer Armed By:	Write to CSC_MODE
Address:	49010h-49027h
Name:	Pipe CSC Coefficients
ShortName:	CSC_COEFF_A
Power:	PG1
Reset:	soft
Address:	49110h-49127h
Name:	Pipe CSC Coefficients
ShortName:	CSC_COEFF_B
Power:	PG2
Reset:	soft
Address:	49210h-49227h
Name:	Pipe CSC Coefficients
ShortName:	CSC_COEFF_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31:16	**RY** Format: CSC COEFFICIENT FORMAT
	15:0	**GY** Format: CSC COEFFICIENT FORMAT
1	31:16	**BY** Format: CSC COEFFICIENT FORMAT
	15:0	**Reserved** Format: MBZ
2	31:16	**RU**

CSC_COEFF		
		Format: CSC COEFFICIENT FORMAT
	15:0	**GU** Format: CSC COEFFICIENT FORMAT
3	31:16	**BU** Format: CSC COEFFICIENT FORMAT
	15:0	**Reserved** Format: MBZ
4	31:16	**RV** Format: CSC COEFFICIENT FORMAT
	15:0	**GV** Format: CSC COEFFICIENT FORMAT
5	31:16	**BV** Format: CSC COEFFICIENT FORMAT
	15:0	**Reserved** Format: MBZ

CSC_MODE

CSC_MODE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank
Address:	49028h-4902Bh
Name:	Pipe CSC Mode
ShortName:	CSC_MODE_A
Power:	PG1
Reset:	soft
Address:	49128h-4912Bh
Name:	Pipe CSC Mode
ShortName:	CSC_MODE_B
Power:	PG2
Reset:	soft
Address:	49228h-4922Bh
Name:	Pipe CSC Mode
ShortName:	CSC_MODE_C
Power:	PG2
Reset:	soft

Description
Writes to this register arm CSC registers for this pipe.

DWord	Bit	Description
0	31	**Pipe CSC Enable** This bit enables the pipe color space conversion.
	30	**Pipe Output CSC Enable** This bit enables the pipe output color space conversion.
	29:2	**Reserved**

CSC_MODE		
		Format: MBZ
	1	**Reserved** Format: MBZ
	0	**Reserved** Format: MBZ

CSC_POSTOFF

CSC_POSTOFF	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	96
Double Buffer Update Point:	Start of vertical blank after armed
Double Buffer Armed By:	Write to CSC_MODE
Address:	49040h-4904Bh
Name:	Pipe CSC Post-Offsets
ShortName:	CSC_POSTOFF_A
Power:	PG1
Reset:	soft
Address:	49140h-4914Bh
Name:	Pipe CSC Post-Offsets
ShortName:	CSC_POSTOFF_B
Power:	PG2
Reset:	soft
Address:	49240h-4924Bh
Name:	Pipe CSC Post-Offsets
ShortName:	CSC_POSTOFF_C
Power:	PG2
Reset:	soft

The post-offset is intended to add an offset from 0 on the Y or RGB channels and to convert UV channels from 2's complement to excess 0.5 as they exit pipe color space conversion (CSC).

DWord	Bit	Description
0	31:13	**Reserved** Format: MBZ
	12:0	**PostCSC High Offset** This value is used to give an offset to the high color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
1	31:13	**Reserved** Format: MBZ

CSC_POSTOFF		
	12:0	**PostCSC Medium Offset** This value is used to give an offset to the medium color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
2	31:13	**Reserved** Format: MBZ
	12:0	**PostCSC Low Offset** This value is used to give an offset to the low color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).

CSC_PREOFF

CSC_PREOFF	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	96
Double Buffer Update Point:	Start of vertical blank after armed
Double Buffer Armed By:	Write to CSC_MODE
Address:	49030h-4903Bh
Name:	Pipe CSC Pre-Offsets
ShortName:	CSC_PREOFF_A
Power:	PG1
Reset:	soft
Address:	49130h-4913Bh
Name:	Pipe CSC Pre-Offsets
ShortName:	CSC_PREOFF_B
Power:	PG2
Reset:	soft
Address:	49230h-4923Bh
Name:	Pipe CSC Pre-Offsets
ShortName:	CSC_PREOFF_C
Power:	PG2
Reset:	soft

The pre-offset is intended to remove an offset from 0 on the Y or RGB channels and to convert UV channels from excess 0.5 to 2's complement as they enter pipe color space conversion (CSC).

DWord	Bit	Description
0	31:13	**Reserved** Format: MBZ
	12:0	**PreCSC High Offset** This value is used to give an offset to the high color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
1	31:13	**Reserved** Format: MBZ

CSC_PREOFF		
	12:0	**PreCSC Medium Offset** This value is used to give an offset to the medium color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
2	31:13	**Reserved** Format: MBZ
	12:0	**PreCSC Low Offset** This value is used to give an offset to the low color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).

CSFE FSM2

CSFEFSM2 - CSFE FSM2	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	022A4h-022A7h
Name:	CSFE FSM2
ShortName:	CSFEFSM2_RCSUNIT
Address:	182A4h-182A7h
Name:	CSFE FSM2
ShortName:	CSFEFSM2_POCSUNIT
Address:	222A4h-222A7h
Name:	CSFE FSM2
ShortName:	CSFEFSM2_BCSUNIT
Address:	1C02A4h-1C02A7h
Name:	CSFE FSM2
ShortName:	CSFEFSM2_VCSUNIT0
Address:	1C42A4h-1C42A7h
Name:	CSFE FSM2
ShortName:	CSFEFSM2_VCSUNIT1
Address:	1C82A4h-1C82A7h
Name:	CSFE FSM2
ShortName:	CSFEFSM2_VECSUNIT0
Address:	1D02A4h-1D02A7h
Name:	CSFE FSM2
ShortName:	CSFEFSM2_VCSUNIT2
Address:	1D42A4h-1D42A7h
Name:	CSFE FSM2
ShortName:	CSFEFSM2_VCSUNIT3
Address:	1D82A4h-1D82A7h
Name:	CSFE FSM2
ShortName:	CSFEFSM2_VECSUNIT1

CSFEFSM2 - CSFE FSM2

Address:	1E02A4h-1E02A7h
Name:	CSFE FSM2
ShortName:	CSFEFSM2_VCSUNIT4

Address:	1E42A4h-1E42A7h
Name:	CSFE FSM2
ShortName:	CSFEFSM2_VCSUNIT5

Address:	1E82A4h-1E82A7h
Name:	CSFE FSM2
ShortName:	CSFEFSM2_VECSUNIT2

Address:	1F02A4h-1F02A7h
Name:	CSFE FSM2
ShortName:	CSFEFSM2_VCSUNIT6

Address:	1F42A4h-1F42A7h
Name:	CSFE FSM2
ShortName:	CSFEFSM2_VCSUNIT7

Address:	1F82A4h-1F82A7h
Name:	CSFE FSM2
ShortName:	CSFEFSM2_VECSUNIT3

DWord	Bit	Description
0	31:30	**POCSLITERST** Format: MBZ
	29:27	**POCSELSUB** Format: MBZ
	26:23	**CTXSWMASTER** Format: MBZ
	22:20	**CSRL_PREEMPT** Format: MBZ
	19:16	**CSCTXSW_CTXSEQ** Format: MBZ
	15:13	**CSPREP4SWITCH**

CSFEFSM2 - CSFE FSM2

		Format: MBZ
	12:11	**SVWR** Format: MBZ
	10:9	**RRCRD** Format: MBZ
	8:6	**RENDCTX** Format: MBZ
	5:3	**CTXSEQ** Format: MBZ
	2:0	**RINGCTX** Format: MBZ

CSPREEMPT

CSPREEMPT - CSPREEMPT

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	024B0h
Name:	CSPREEMPT
ShortName:	CSPREEMPT
Address:	224B0h
Name:	BCSPREEMPT
ShortName:	BCSPREEMPT
Address:	124B0h
Name:	VCSPREEMPT
ShortName:	VCSPREEMPT
Address:	1A4B0h
Name:	VECSPREEMPT
ShortName:	VECSPREEMPT

Programming Notes

This is for HW internal usage and must not be written by SW.

DWord	Bit	Description
0	31:16	**Mask Bits** Format: Mask[15:0] Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15:1	**Reserved** Format: MBZ
	0	**Unnamed** Format: Disable This is a message bit written by the cross CS in case of GT4-CBR/SFR mode of operation. To set this bit both bit[0] and bit[16] (mask) needs to be set. This bit set indicates CS in other GT has reached a preemption point. This bit gets reset by CS when preemption takes place.

CTX REG 1

CTXREG1 - CTX REG 1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00FF4h-00FF7h	
DWord	**Bit**	**Description**
0	31:0	**CTXSIZE** Default Value: 00000044h Access: RO Register to store value for number of CTX DWORDs, not including the CR 000 mapping entry

CUR_BASE

CUR_BASE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled
Address:	70084h-70087h
Name:	Cursor Base Address
ShortName:	CUR_BASE_A
Power:	PG1
Reset:	soft
Address:	71084h-71087h
Name:	Cursor Base Address
ShortName:	CUR_BASE_B
Power:	PG2
Reset:	soft
Address:	72084h-72087h
Name:	Cursor Base Address
ShortName:	CUR_BASE_C
Power:	PG2
Reset:	soft

Writes to this register arm cursor registers for this pipe.

DWord	Bit	Description
0	31:12	**Cursor Base 31 12** Format: GraphicsAddress[31:12] This field specifies bits 31:12 of the graphics address of the base of the cursor for hi-res mode. When performing 180 degree rotation, this address does not need to change, hardware will internally offset to start from the last pixel of the last line of the cursor. **Workaround** To prevent false VT-d type 6 errors, use 64KB address alignment and allocate an extra 2 Page Table Entries (PTEs) beyond the end of the displayed surface. Only the PTEs will be used, not the pages themselves. **Restriction**

CUR_BASE		
		The cursor surface address must be 4K byte aligned. The cursor must be in linear memory, it cannot be tiled.
	11:7	**Reserved**
	6:4	**Reserved**
	3	**Reserved**
	2	**Reserved**
	1:0	**Reserved**

CUR_COLOR_CTL

CUR_COLOR_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed
Double Buffer Armed By:	Write to CUR_BASE or cursor not enabled

Address:	700C0h-700C3h
Name:	Cursor Color Control
ShortName:	CUR_COLOR_CTL_A
Power:	PG1
Reset:	soft

Address:	710C0h-710C3h
Name:	Cursor Color Control
ShortName:	CUR_COLOR_CTL_B
Power:	PG2
Reset:	soft

Address:	720C0h-720C3h
Name:	Cursor Color Control
ShortName:	CUR_COLOR_CTL_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15	**Tone Mapping Enable** This field enables the tone mapping of cursor pixels using the programmed tone mapping factor. Value / Name

CUR_COLOR_CTL		
		1b: Enable 0b: Disable
	14:10	**Reserved** Format: MBZ
	9:0	**Tone Mapping Factor** This field specifies the tone mapping factor. Each color component gets corrected with this programmed 10 bit fractional value.

CUR_CSC_COEFF

CUR_CSC_COEFF	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	192
Double Buffer Update Point:	Start of vertical blank after armed
Double Buffer Armed By:	Write to CUR_CTL
Address:	700D0h-700E7h
Name:	Cursor CSC Coefficients
ShortName:	CUR_CSC_COEFF_A
Power:	PG1
Reset:	soft
Address:	710D0h-710E7h
Name:	Cursor CSC Coefficients
ShortName:	CUR_CSC_COEFF_B
Power:	PG2
Reset:	soft
Address:	720D0h-720E7h
Name:	Cursor CSC Coefficients
ShortName:	CUR_CSC_COEFF_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31:16	**RY** Format: CSC COEFFICIENT FORMAT
	15:0	**GY** Format: CSC COEFFICIENT FORMAT
1	31:16	**BY** Format: CSC COEFFICIENT FORMAT

CUR_CSC_COEFF		
	15:0	**Reserved** Format: MBZ
2	31:16	**RU** Format: CSC COEFFICIENT FORMAT
	15:0	**GU** Format: CSC COEFFICIENT FORMAT
3	31:16	**BU** Format: CSC COEFFICIENT FORMAT
	15:0	**Reserved** Format: MBZ
4	31:16	**RV** Format: CSC COEFFICIENT FORMAT
	15:0	**GV** Format: CSC COEFFICIENT FORMAT
5	31:16	**BV** Format: CSC COEFFICIENT FORMAT
	15:0	**Reserved** Format: MBZ

CUR_CTL

CUR_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed
Double Buffer Armed By:	Write to CUR_BASE or cursor not enabled
Address:	70080h-70083h
Name:	Cursor Control
ShortName:	CUR_CTL_A
Power:	PG1
Reset:	soft
Address:	71080h-71083h
Name:	Cursor Control
ShortName:	CUR_CTL_B
Power:	PG2
Reset:	soft
Address:	72080h-72083h
Name:	Cursor Control
ShortName:	CUR_CTL_C
Power:	PG2
Reset:	soft

The cursor is enabled by programming a valid cursor mode in the cursor mode select fields. The cursor is disabled by programming all 0s in the cursor mode select fields.

DWord	Bit	Description
0	31	**Reserved** Format: MBZ
	30:28	**Pipe Slice Arbitration Slots** This field specifies the number of slots allocated to cursor in pipe slice request arbitration. This field is ignored when the 'PIPE_SLICE_ARBITRATION_CTL->Use Programmed Slots' is not set. This field is zero based; a programmed value of 0 results in 1 slot allocation.

CUR_CTL

27	**Reserved**
26	**Gamma Enable** This bit enables pipe gamma correction for the cursor pixel data. In VGA pop-up operation, the cursor data will always bypass gamma.

Value	Name
0b	Disable
1b	Enable

25	**Reserved**
24	**Pipe CSC Enable**

Description
This bit enables pipe color space conversion for the cursor pixel data.
Use CSC_MODE.Pipe CSC Enable, GAMMA_MODE.*_GAMMA_ENABLE for enabling pipe color space conversion and gamma respectively across all pixels from all planes. Cursor CSC must be used for cursor specific color space conversion.

Value	Name
0b	Disable
1b	Enable

23	**Allow Double Buffer Update Disable**

Access:	R/W

This field controls whether double buffer updates are allowed to be disabled for this cursor. The DOUBLE_BUFFER_CTL register can be configured to globally disable double buffer updates for resources that allow them to be disabled.

Value	Name
0b	Not Allowed
1b	Allowed

22:19	**Reserved**

Format:	MBZ

18	**Pre CSC Gamma Enable**

This bit enables the cursor pre-CSC gamma for the cursor pixel data. This is generally used with HDR to de-gamma the sRGB cursor pixel data before the RGB2020 conversion.

Value	Name
0b	Disable

CUR_CTL

	1b	Enable

17 Reserved

Format:	MBZ

16 CSC Enable

This bit enables the cursor color space conversion for the cursor pixel data. Hardware uses the coefficients programmed in the CUR_CSC_COEFF regsiters to perform the color space conversion.

Value	Name
0b	Disable
1b	Enable

15 180 Rotation

This mode causes the cursor image to be rotated 180 degrees. In addition to setting this bit, the cursor position must be adjusted to match the physical orientation of the display.

Value	Name
0b	No rotation
1b	180 degree rotation

Restriction
Only 32 bits per pixel cursors can be rotated. This field must be zero when the cursor format is 2 bits per pixel.

14 Trickle Feed Enable

Value	Name
0b	Enable
1b	Disable

Restriction
Do not program this field to 1b.

13:12 Reserved

11:10 Force Alpha Plane Select

This field selects which planes the cursor alpha value will be forced for. It is used together with the Force Alpha Value field.

Value	Name	Description
00b	Disable	Disable alpha forcing

CUR_CTL

01b	Pipe CSC Enabled	Enable alpha forcing where cursor overlaps a plane that has enabled pipe CSC
10b	Pipe CSC Disabled	Enable alpha forcing where cursor overlaps plane that has disabled pipe CSC
11b	Reserved	Reserved

9:8 **Force Alpha Value**

This field controls the behavior of cursor when alpha blending onto certain plane pixels. It is used together with the Force Alpha Plane Select field.

Value	Name	Description
00b	Disable	Cursor pixels alpha blend normally over any plane.
01b	50	Cursor pixels with alpha >= 50% are made fully opaque where they overlap the selected plane(s). Cursor pixels with alpha < 50% are made fully transparent where they overlap the selected plane(s).
10b	75	Cursor pixels with alpha >= 75% are made fully opaque where they overlap the selected plane(s). Cursor pixels with alpha < 75% are made fully transparent where they overlap the selected plane(s).
11b	100	Cursor pixels with alpha = 100% are made fully opaque where they overlap the selected plane(s). Cursor pixels with alpha < 100% are made fully transparent where they overlap the selected plane(s).

Restriction
Force Alpha is only for use with ARGB cursor formats.

7:6 **Reserved**

5:0 **Cursor Mode Select**

This field selects the cursor mode. Cursor is disabled when the selection is 000000b and enabled when the selection is any other value. The cursor vertical size can be overriden by the size reduction mode.

Color channels should be pre-multiplied with alpha by software.

Value	Name	Description
000000b	Disable	Cursor is disabled
000010b	128x128 32bpp AND/INV	128x128 32bpp AND/INVERT
000011b	256x256 32bpp AND/INV	256x256 32bpp AND/INVERT
000100b	64x64 2bpp 3-color	64x64 2bpp Indexed 3-color and transparency
000101b	64x64 2bpp 2-color	64x64 2bpp Indexed AND/XOR 2-color
000110b	64x64 2bpp 4-color	64x64 2bpp Indexed 4-color
000111b	64x64 32bpp AND/INV	64x64 32bpp AND/INVERT
100010b	128x128 32bpp ARGB	128x128 32bpp ARGB (8:8:8:8 MSB-A:R:G:B)
100011b	256x256 32bpp ARGB	256x256 32bpp ARGB (8:8:8:8 MSB-A:R:G:B)
100100b	64x64 32bpp AND/XOR	64x64 32bpp AND/XOR

100101b	128x128 32bpp AND/XOR	128x128 32bpp AND/XOR
100110b	256x256 32bpp AND/XOR	256x256 32bpp AND/XOR
100111b	64x64 32bpp ARGB	64x64 32bpp ARGB (8:8:8:8 MSB-A:R:G:B)
Others	Reserved	Reserved

Programming Notes

INVERT, XOR, and alpha blends may not look as expected when the plane underlying the cursor is YUV or extended range RGB. Out of range RGB values will be clamped prior to alpha blending, INVERT, or XOR with cursor. It is recommended to use Force Alpha when cursor is alpha blending onto an plane of a different color space or extended gamut.

The AND/INVERT format uses the most significant byte (MSB) to control the color. If MSB is 0xFF: Cursor is opaque. Show cursor color from three least significant bytes. If MSB is 0x00: Cursor is transparent. Three least significant bytes must be zero. If MSB is not 0x00 or 0xFF: Cursor inverts the color of the surface underneath.

The AND/XOR format uses the most significant byte (MSB) to control the color. If MSB is 0xFF: Cursor is opaque. Show cursor color from three least significant bytes. If MSB is 0x00: Cursor is transparent. Three least significant bytes must be zero. If MSB is not 0x00 or 0xFF: The three least significant bytes are XOR'd with the color of the surface underneath.

CUR_FBC_CTL

CUR_FBC_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed
Double Buffer Armed By:	Write to CUR_BASE or cursor not enabled
Address:	700A0h-700A3h
Name:	Cursor FBC Control
ShortName:	CUR_FBC_CTL_A
Power:	PG1
Reset:	soft
Address:	710A0h-710A3h
Name:	Cursor FBC Control
ShortName:	CUR_FBC_CTL_B
Power:	PG2
Reset:	soft
Address:	720A0h-720A3h
Name:	Cursor FBC Control
ShortName:	CUR_FBC_CTL_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31	**Size Reduction Enable** This enables cursor size reduction logic. The cursor engine will fetch and display the programmed reduced number of lines, then go transparent for the rest of the frame. Value: 0b — Name: Disable Value: 1b — Name: Enable Restriction

CUR_FBC_CTL		
		Cursor size reduction is not allowed with 2bpp cursor formats or cursor 180 degree rotation. The reduced scan lines field must be programmed with a valid value when cursor size reduction is enabled.
	30:8	**Reserved**
	7:0	**Reduced Scan Lines** This specifies the number of scan lines of cursor data to fetch and display when cursor size reduction is enabled. The value programmed is the size minus one. **Restriction** The minimum size is 8 lines, programmed as 07h. The maximum size can not be greater than the normal size when size reduction is not enabled.

CUR_PAL

CUR_PAL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled
Address:	70090h-7009Fh
Name:	Cursor A Palette
ShortName:	CUR_PAL_A_*
Power:	PG1
Reset:	soft
Address:	71090h-7109Fh
Name:	Cursor B Palette
ShortName:	CUR_PAL_B_*
Power:	PG2
Reset:	soft
Address:	72090h-7209Fh
Name:	Cursor C Palette
ShortName:	CUR_PAL_C_*
Power:	PG2
Reset:	soft

The cursor palette provides color information when using the indexed cursor modes. There are 4 instances of this register format per cursor. The table below describes how the cursor mode and index value will select between the cursor palette colors, AND/XOR, transparency, and destination invert.

Index Value	2 color mode	3 color mode	4 color mode
00	CUR_PAL 0	CUR_PAL 0	CUR_PAL 0
01	CUR_PAL 1	CUR_PAL 1	CUR_PAL 1
10	Transparent	Transparent	CUR_PAL 2
11	Invert Destination	CUR_PAL 3	CUR_PAL 3

DWord	Bit	Description

CUR_PAL		
0	31:24	**Reserved**
	23:16	**Palette Red** This field is the cursor palette red value
	15:8	**Palette Green** This field is the cursor palette green value.
	7:0	**Palette Blue** This field is the cursor palette blue value.

CUR_POS

CUR_POS	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled
Address:	70088h-7008Bh
Name:	Cursor Position
ShortName:	CUR_POS_A
Power:	PG1
Reset:	soft
Address:	71088h-7108Bh
Name:	Cursor Position
ShortName:	CUR_POS_B
Power:	PG2
Reset:	soft
Address:	72088h-7208Bh
Name:	Cursor Position
ShortName:	CUR_POS_C
Power:	PG2
Reset:	soft

This register specifies the screen position of the cursor. The origin of the cursor position is always the upper left corner of the display pipe source image area. When performing 180 degree rotation, the cursor image is rotated by hardware, but the position is not, so it should be adjusted if it is desired to maintain the same apparent position on a physically rotated display.

Restriction
The cursor must have at least a single pixel positioned over the pipe source area.

DWord	Bit	Description
0	31	**Y Position Sign** This specifies the sign of the vertical position of the cursor upper left corner.
	30:29	**Reserved** Format: MBZ

CUR_POS		
	28:16	**Y Position Magnitude** This specifies the magnitude of the vertical position of the cursor upper left corner in lines.
	15	**X Position Sign** This specifies the sign of the horizontal position of the cursor upper left corner.
	14:13	**Reserved** Format: MBZ
	12:0	**X Position Magnitude** This specifies the magnitude of the horizontal position of the cursor upper left corner in pixels.

CUR_PRE_CSC_GAMC_DATA

CUR_PRE_CSC_GAMC_DATA	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	700B4h-700B7h
Name:	Cursor Pre CSC Gamma Data
ShortName:	CUR_PRE_CSC_GAMMA_DATA_A
Power:	PG1
Reset:	soft
Address:	710B4h-710B7h
Name:	Cursor Pre CSC Gamma Data
ShortName:	CUR_PRE_CSC_GAMMA_DATA_B
Power:	PG2
Reset:	soft
Address:	720B4h-720B7h
Name:	Cursor Pre CSC Gamma Data
ShortName:	CUR_PRE_CSC_GAMMA_DATA_C
Power:	PG2
Reset:	soft

CUR_PRE_CSC_GAMC_INDEX and CUR_PRE_CSC_GAMC_DATA registers are used to program the values that determine the characteristics of the gamma correction for the cursor pixel data before Color Space Conversion. Additional gamma correction can be done after the Color Space Conversion if desired.
The gamma correction curve is represented by specifying a set of gamma entry reference points spaced equally along the curve for values between -1 and 1. For extended values there are extended gamma entry reference points. All input values are clamped to the greater than -7.0 and less than 7.0 range before the gamma calculation.
For input values greater than or equal to 0 and less than 1.0, the input value is used to linearly interpolate between two adjacent points of the first 33 gamma entries to create the result value. The first 32 entries are stored as 16 bits per color in an unsigned 0.16 format with 0 integer and 16 fractional. The 33rd, 34th and 35th entries are stored as 19 bits per color in an unsigned 3.16 format with 3 integer and 16 fractional bits.
For input values greater than or equal to 1.0 and less than 3.0, the input value is used to linearly interpolate between the 33rd and 34th gamma entries to create the result value.

CUR_PRE_CSC_GAMC_DATA

For input values greater than or equal to 3.0 and less than 7.0, the input value is used to linearly interpolate between the 34th and 35th gamma entries to create the result value.
For negative input values, gamma is mirrored along the X-axis, giving the same result as positive input values, except for a negative sign. When gamma input may be negative, the first gamma point should be programmed to a value of 0.0 in order to have a symmetric mirroring.
Pre-CSC Gamma correction gets enabled or disabled based on the "Pre CSC Enable" bit in the CUR_CTL register.

Programming Notes

To program the gamma correction entries, calculate the desired gamma curve for inputs from 0 to 7.0. For inputs of 0 to 1.0, multiply the input value by 32 to find the gamma entry number, then store the desired gamma result in that entry. For inputs greater than 1.0 and less than or equal to 3.0, store the result for an input of 3.0 in the 34th gamma entry. For inputs greater than 3.0 and less than or equal to 7.0, store the result for an input of 7.0 in the 35th gamma entry.

Restriction

The gamma curve must be flat or increasing, never decreasing. The gamma correction registers should only be updated when the plane is off, otherwise screen artifacts may show temporarily.

DWord	Bit	Description	
0	31:19	**Reserved**	
		Format:	MBZ
	18:0	**Gamma Value**	
		Default Value:	00000000000000000b
		Format:	U3.16

CUR_PRE_CSC_GAMC_INDEX

CUR_PRE_CSC_GAMC_INDEX

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	700B0h-700B3h
Name:	Cursor Pre CSC Gamma Index
ShortName:	CUR_PRE_CSC_GAMMA_INDEX_A
Power:	PG1
Reset:	soft
Address:	710B0h-710B3h
Name:	Cursor Pre CSC Gamma Index
ShortName:	CUR_PRE_CSC_GAMMA_INDEX_B
Power:	PG2
Reset:	soft
Address:	720B0h-720B3h
Name:	Cursor Pre CSC Gamma Index
ShortName:	CUR_PRE_CSC_GAMMA_INDEX_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31:11	**Reserved** Format: MBZ
	10	**Index Auto Increment** This field enables the index auto increment. Value / Name / Description 0b / No Increment / Do not automatically increment the index value. 1b / Auto Increment **[Default]** / Increment the index value with each read or write to the data register.
	9:6	**Reserved** Format: MBZ

CUR_PRE_CSC_GAMC_INDEX

	5:0	**Index Value** Access: Write/Read Status This index controls access to the array of pipe pre color space conversion gamma values. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set. When automatically incrementing, the index will roll over to 0 after writing or reading the entire allowed range. While in auto increment mode, after performing reads or writes to only part of the range, the auto increment bit must be cleared before resetting the index value. **Value**: [0,34] **Name**:

CUR_SURFLIVE

CUR_SURFLIVE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	700ACh-700AFh
Name:	Cursor Live Base Address
ShortName:	CUR_SURFLIVE_A
Power:	PG1
Reset:	soft
Address:	710ACh-710AFh
Name:	Cursor Live Base Address
ShortName:	CUR_SURFLIVE_B
Power:	PG2
Reset:	soft
Address:	720ACh-720AFh
Name:	Cursor Live Base Address
ShortName:	CUR_SURFLIVE_C
Power:	PG2
Reset:	soft

There is one instance of this register for each pipe.

DWord	Bit	Description
0	31:12	**Live Surface Base Address** This gives the live value of the surface base address as being currently used for the cursor.
	11:0	**Reserved** Format: MBZ

Customizable Event Creation 0-0

CEC0-0 - Customizable Event Creation 0-0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02770h

This register is used to define custom counter event 0, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Format: U11 The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. **Value** / **Name** / **Description** / **Programming Notes** 0b / Pass-through / Input bit is passed through to comparator as is / 1b / Negated / Input bit is negated before passing to comparator / [] If the input bit is negated using any bit in this field, then the corresponding Consderations bit in the CEC0-1 register must also be set.
	20:19	**Source Select** Format: U2 Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). **Value** / **Name** / **Description** 01b / Prev Event / Selects the conditioned/flopped input from the last CEC block as the input bus to CEC0 block 11b / Reserved /
	18:3	**Compare Value** Format: U16 The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the

signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

2:0 **Compare Function**

Format:	U3

This field selects the function used by the CEC0 comparator when comparing the compare value to the value active on the CEC0 conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

Customizable Event Creation 1-0

CEC1-0 - Customizable Event Creation 1-0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02778h

This register is used to define custom counter event 1, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Format: U11 The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. **Value** / **Name** / **Description** / **Programming Notes** 0b / Pass-through / Input bit is passed through to comparator as is / 1b / Negated / Input bit is negated before passing to comparator / [] If the input bit is negated using any bit in this field, then the corresponding Considerations bit in the CEC1-1 register must also be set.
	20:19	**Source Select** Format: U2 Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). **Value** / **Name** / **Description** 01b / Prev Event / Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block 11b / Reserved /
	18:3	**Compare Value** Format: U16 The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the

CEC1-0 - Customizable Event Creation 1-0

signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

2:0 **Compare Function**

Format:	U3

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

Customizable Event Creation 1-1

CEC1-1 - Customizable Event Creation 1-1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0277Ch

This register configures the input conditioning portion of CEC (custom event creation) block 1, bit definitions in this register refer to the CEC block diagram.

DWord	Bit	Description
0	31:16	**Considerations** This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.

Value	Name	Description
0b	Live	Input bit is not delayed by 1 clock before event calculation
1b	Delayed	Input bit is delayed by 1 clock before event calculation

DWord	Bit	Description
	15:0	**Mask** This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used.

Value	Name	Description
0b	Unmasked	Input bit is considered in event calculation
1b	Masked	Input bit is ignored in event calculation

Customizable Event Creation 2-0

CEC2-0 - Customizable Event Creation 2-0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02780h

This register is used to define custom counter event 2, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Format: U11 The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. **Value** / **Name** / **Description** / **Programming Notes** 0b / Pass-through / Input bit is passed through to comparator as is / 1b / Negated / Input bit is negated before passing to comparator / [] If the input bit is negated using any bit in this field, then the corresponding Consderations bit in the CEC2-1 register must also be set.
	20:19	**Source Select** Format: U2 Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). **Value** / **Name** / **Description** 01b / Prev Event / Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block 11b / Reserved /
	18:3	**Compare Value** Format: U16 The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the

signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

2:0 **Compare Function**

Format:	U3

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

Customizable Event Creation 2-1

CEC2-1 - Customizable Event Creation 2-1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02784h

This register configures the input conditioning portion of CEC (custom event creation) block 2, bit definitions in this register refer to the CEC block diagram.

DWord	Bit	Description
0	31:16	**Considerations** This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.

Value	Name	Description
0b	Live	Input bit is not delayed by 1 clock before event calculation
1b	Delayed	Input bit is delayed by 1 clock before event calculation

Bit	Description
15:0	**Mask** This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used.

Value	Name	Description
0b	Unmasked	Input bit is considered in event calculation
1b	Masked	Input bit is ignored in event calculation

Customizable Event Creation 3-0

CEC3-0 - Customizable Event Creation 3-0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02788h

This register is used to define custom counter event 3, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Format: U11 The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. **Value** / **Name** / **Description** / **Programming Notes** 0b / Pass-through / Input bit is passed through to comparator as is / 1b / Negated / Input bit is negated before passing to comparator / [] If the input bit is negated using any bit in this field, then the corresponding Considerations bit in the CEC3-1 register must also be set.
	20:19	**Source Select** Format: U2 Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). **Value** / **Name** / **Description** 01b / Prev Event / Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block 11b / Reserved /
	18:3	**Compare Value** Format: U16 The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the

CEC3-0 - Customizable Event Creation 3-0

signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

2:0 **Compare Function**

Format:	U3

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

Customizable Event Creation 3-1

CEC3-1 - Customizable Event Creation 3-1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0278Ch

This register configures the input conditioning portion of CEC (custom event creation) block 3, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:16	**Considerations** This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.
	15:0	**Mask** This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used.

Bit 31:16 — Considerations

Value	Name	Description
0b	Live	Input bit is not delayed by 1 clock before event calculation
1b	Delayed	Input bit is delayed by 1 clock before event calculation

Bit 15:0 — Mask

Value	Name	Description
0b	Unmasked	Input bit is considered in event calculation
1b	Masked	Input bit is ignored in event calculation

Customizable Event Creation 4-0

CEC4-0 - Customizable Event Creation 4-0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02790h

This register is used to define custom counter event 4, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Format: U11 The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. **Value** / **Name** / **Description** / **Programming Notes** 0b / Pass-through / Input bit is passed through to comparator as is / 1b / Negated / Input bit is negated before passing to comparator / [] If the input bit is negated using any bit in this field, then the corresponding Considerations bit in the CEC4-1 register must also be set.
	20:19	**Source Select** Format: U2 Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). **Value** / **Name** / **Description** 01b / Prev Event / Selects the conditioned/flopped input from the last CEC block as the input bus to CEC0 block 11b / Reserved /
	18:3	**Compare Value** Format: U16 The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance

counter or fed into other CEC blocks.

2:0 **Compare Function**

Format:	U3

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

Customizable Event Creation 5-0

CEC5-0 - Customizable Event Creation 5-0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02798h

This register is used to define custom counter event 5, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Format: U11 The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. **Value** / **Name** / **Description** / **Programming Notes** 0b / Pass-through / Input bit is passed through to comparator as is / 1b / Negated / Input bit is negated before passing to comparator / [] If the input bit is negated using any bit in this field, then the corresponding Considerations bit in the CEC5-1 register must also be set.
	20:19	**Source Select** Format: U2 Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). **Value** / **Name** / **Description** 01b / Prev Event / Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block 11b / Reserved /
	18:3	**Compare Value** Format: U16 The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance

counter or fed into other CEC blocks.

2:0 **Compare Function**

Format:	U3

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

Customizable Event Creation 5-1

CEC5-1 - Customizable Event Creation 5-1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0279Ch

This register configures the input conditioning portion of CEC (custom event creation) block 5, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:16	**Considerations** This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.

Value	Name	Description
0b	Live	Input bit is not delayed by 1 clock before event calculation
1b	Delayed	Input bit is delayed by 1 clock before event calculation

DWord	Bit	Description
0	15:0	**Mask** This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used.

Value	Name	Description
0b	Unmasked	Input bit is considered in event calculation
1b	Masked	Input bit is ignored in event calculation

Customizable Event Creation 6-0

CEC6-0 - Customizable Event Creation 6-0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	027A0h

This register is used to define custom counter event 6, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

<table>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td>0</td><td>31:21</td><td>Negate
<table>
<tr><td></td><td></td></tr>
<tr><td>Format:</td><td>U11</td></tr>
</table>
The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th><th>Programming Notes</th></tr>
<tr><td>0b</td><td>Pass-through</td><td>Input bit is passed through to comparator as is</td><td></td></tr>
<tr><td>1b</td><td>Negated</td><td>Input bit is negated before passing to comparator</td><td>[] If the input bit is negated using any bit in this field, then the corresponding Considerations bit in the CEC6-1 register must also be set.</td></tr>
</table></td></tr>
<tr><td></td><td>20:19</td><td>Source Select
<table>
<tr><td>Format:</td><td>U2</td></tr>
</table>
Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).
<table>
<tr><th>Value</th><th>Name</th><th>Description</th></tr>
<tr><td>01b</td><td>Prev Event</td><td>Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block</td></tr>
<tr><td>11b</td><td>Reserved</td><td></td></tr>
</table></td></tr>
<tr><td></td><td>18:3</td><td>Compare Value
<table>
<tr><td>Format:</td><td>U16</td></tr>
</table>
The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance</td></tr>
</table>

CEC6-0 - Customizable Event Creation 6-0

		counter or fed into other CEC blocks.
	2:0	**Compare Function** Format: U3 This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

Customizable Event Creation 6-1

CEC6-1 - Customizable Event Creation 6-1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	027A4h

This register configures the input conditioning portion of CEC (custom event creation) block 6, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:16	**Considerations** This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.

Value	Name	Description
0b	Live	Input bit is not delayed by 1 clock before event calculation
1b	Delayed	Input bit is delayed by 1 clock before event calculation

DWord	Bit	Description
	15:0	**Mask** This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used.

Value	Name	Description
0b	Unmasked	Input bit is considered in event calculation
1b	Masked	Input bit is ignored in event calculation

Customizable Event Creation 7-0

CEC7-0 - Customizable Event Creation 7-0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	027A8h

This register is used to define custom counter event 7, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Format: U11 The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. **Value** / **Name** / **Description** / **Programming Notes** 0b / Pass-through / Input bit is passed through to comparator as is / 1b / Negated / Input bit is negated before passing to comparator / [] If the input bit is negated using any bit in this field, then the corresponding Considerations bit in the CEC7-1 register must also be set.
	20:19	**Source Select** Format: U2 Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). **Value** / **Name** / **Description** 01b / Prev Event / Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block 11b / Reserved /
	18:3	**Compare Value** Format: U16 The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance

counter or fed into other CEC blocks.

2:0 **Compare Function**

Format:	U3

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

Customizable Event Creation 7-1

CEC7-1 - Customizable Event Creation 7-1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	027ACh

This register configures the input conditioning portion of CEC (custom event creation) block 3, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:16	**Considerations** This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.

Value	Name	Description
0b	Live	Input bit is not delayed by 1 clock before event calculation
1b	Delayed	Input bit is delayed by 1 clock before event calculation

DWord	Bit	Description
0	15:0	**Mask** This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used.

Value	Name	Description
0b	Unmasked	Input bit is considered in event calculation
1b	Masked	Input bit is ignored in event calculation

DATAM

DATAM	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	60030h-60033h
Name:	Transcoder A Data M Value 1
ShortName:	TRANS_DATAM1_A
Power:	PG2
Reset:	soft
Address:	61030h-61033h
Name:	Transcoder B Data M Value 1
ShortName:	TRANS_DATAM1_B
Power:	PG2
Reset:	soft
Address:	62030h-62033h
Name:	Transcoder C Data M Value 1
ShortName:	TRANS_DATAM1_C
Power:	PG2
Reset:	soft
Address:	6F030h-6F033h
Name:	Transcoder EDP Data M Value 1
ShortName:	TRANS_DATAM1_EDP
Power:	PG1
Reset:	soft

This register is double buffered to update on the next MSA after LINKN is written.

DWord	Bit	Description	
0	31	**Reserved**	
		Format:	MBZ

DATAM		
	30:25	**TU or VCpayload Size** In DisplayPort SST mode this field is the size of the transfer unit, minus one. Typically it is programmed with a value of 63 for TU size of 64. In DisplayPort MST mode this field is the Virtual Channel payload size, minus one. **Restriction** In DisplayPort MST mode the Virtual Channel payload size must not be programmed greater than 62 (resulting payload size of 63). In DisplayPort MST mode the Virtual Channel payload size must not be changed while the Virtual Channel is enabled, even after a transcoder has been disabled.
	24	**Reserved** Format: MBZ
	23:0	**Data M value** This field is the data M value for internal use.

DATAN

DATAN	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	60034h-60037h
Name:	Transcoder A Data N Value 1
ShortName:	TRANS_DATAN1_A
Power:	PG2
Reset:	soft
Address:	61034h-61037h
Name:	Transcoder B Data N Value 1
ShortName:	TRANS_DATAN1_B
Power:	PG2
Reset:	soft
Address:	62034h-62037h
Name:	Transcoder C Data N Value 1
ShortName:	TRANS_DATAN1_C
Power:	PG2
Reset:	soft
Address:	6F034h-6F037h
Name:	Transcoder EDP Data N Value 1
ShortName:	TRANS_DATAN1_EDP
Power:	PG1
Reset:	soft

This register is double buffered to update on the next MSA after LINKN is written.

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:0	**Data N value** This field is the data N value for internal use.

DBUF_CTL

DBUF_CTL		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Access:	R/W	
Size (in bits):	32	
Address:	45008h-4500Bh	
Name:	DBUF Slice 1 Control	
ShortName:	DBUF_CTL_S1	
Power:	PG0	
Reset:	soft	
Address:	44FE8h-44FEBh	
Name:	DBUF Slice 2 Control	
ShortName:	DBUF_CTL_S2	
Power:	PG0	
Reset:	soft	

DWord	Bit	Description
0	31	**DBUF Power Request** Access: R/W This field requests DBUF power to enable or disable. 0b: Disable 1b: Enable **Programming Notes** DBUF power must be enabled prior to using internal display engine features. Enable power by programming the power request to 1, then wait for the power state to indicate it is enabled.
	30	**DBUF Power State** Access: RO This field indicates the status of DBUF power. 0b: Disabled 1b: Enabled
	29:28	**Reserved** Format: MBZ

DBUF_CTL		
	27	**Reserved**
	26	**Reserved** Format: MBZ
	25:24	**Reserved**
	23:19	**Reserved**
	18:0	**Reserved** Format: MBZ

DBUF_ECC_STAT

DBUF_ECC_STAT	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/WC
Size (in bits):	32
Address:	45010h-45013h
Name:	DBUF Slice 1 ECC Status
ShortName:	DBUF_ECC_STAT_S1
Power:	PG0
Reset:	soft
Address:	44FF0h-44FF3h
Name:	DBUF Slice 2 ECC Status
ShortName:	DBUF_ECC_STAT_S2
Power:	PG0
Reset:	soft

Each of these fields is a sticky bit that gives the ECC error status for a particular memory bank. A '1' in a bit indicates that ECC detected an error. A write of '1' to a bit will clear the bit. Single errors are corrected by ECC. Double errors are not correctable.

DWord	Bit	Description
0	31	**Double Error Bank 15**
	30	**Double Error Bank 14**
	29	**Double Error Bank 13**
	28	**Double Error Bank 12**
	27	**Double Error Bank 11**
	26	**Double Error Bank 10**
	25	**Double Error Bank 9**
	24	**Double Error Bank 8**
	23	**Double Error Bank 7**
	22	**Double Error Bank 6**
	21	**Double Error Bank 5**
	20	**Double Error Bank 4**
	19	**Double Error Bank 3**

DBUF_ECC_STAT		
	18	**Double Error Bank 2**
	17	**Double Error Bank 1**
	16	**Double Error Bank 0**
	15	**Single Error Bank 15**
	14	**Single Error Bank 14**
	13	**Single Error Bank 13**
	12	**Single Error Bank 12**
	11	**Single Error Bank 11**
	10	**Single Error Bank 10**
	9	**Single Error Bank 9**
	8	**Single Error Bank 8**
	7	**Single Error Bank 7**
	6	**Single Error Bank 6**
	5	**Single Error Bank 5**
	4	**Single Error Bank 4**
	3	**Single Error Bank 3**
	2	**Single Error Bank 2**
	1	**Single Error Bank 1**
	0	**Single Error Bank 0**

DC_STATE_EN

DC_STATE_EN

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	45504h-45507h
Name:	Display C State Enable
ShortName:	DC_STATE_EN
Power:	PG0
Reset:	soft

DWord	Bit	Description
0	31	**MODE SET in Progress** This bit indicates that Mode set is in progress and DCPR will not generate any CSR_Start to DMC when set. Software needs to program this bit when mode set is started and software should reset it when mode set is done. Value / Name: 0b: CSR_start generation not gated **[Default]** 1b: CSR_start generation is gated
	30:10	**Reserved**
	9	**In CSR Flow** Value / Name: 0b: Not In CSR 1b: In CSR Restriction: This field is used for hardware communication. Software must not change this field.
	8	**Block Outbound Traffic** Access is read/write, but hardware can also clear the value based on the PM Request. Value / Name: 0b: Do Not Block

DC_STATE_EN

		1b: Block
		Restriction: This field is used for hardware communication. Software must not change this field.
	7:5	**Reserved**
	4	**Mask Poke** This field masks the poke signal that would otherwise be generated by a write to the DC_STATE_SEL register. 0b: Unmask 1b: Mask **Restriction**: This field is used for hardware communication. Software must not change this field.
	3	**DC9 Allow** This field indicates software allows Display C9. When allowed, the PCU can save the display PCI Config context and power down display 0b: Do not allow 1b: Allow
	2	**Reserved**
	1:0	**Dynamic DC State Enable** This field enables hardware to dynamically enter and exit Display C states. 00b: Disable 01b: Enable up to DC5 10b: Enable up to DC6 **Restriction**: The Display CSR code must be loaded before this field is enabled.

DDI_AUX_CTL

DDI_AUX_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	64010h-64013h
Name:	DDI A AUX Channel Control
ShortName:	DDI_AUX_CTL_A
Power:	PG1
Reset:	soft
Address:	64110h-64113h
Name:	DDI B AUX Channel Control
ShortName:	DDI_AUX_CTL_B
Power:	PG2
Reset:	soft
Address:	64210h-64213h
Name:	DDI C AUX Channel Control
ShortName:	DDI_AUX_CTL_C
Power:	PG2
Reset:	soft
Address:	64310h-64313h
Name:	DDI D AUX Channel Control
ShortName:	DDI_AUX_CTL_D
Power:	PG2
Reset:	soft
Address:	64410h-64413h
Name:	DDI E AUX Channel Control
ShortName:	DDI_AUX_CTL_E

DDI_AUX_CTL

Power:	PG2
Reset:	soft

Address:	64510h-64513h
Name:	DDI F AUX Channel Control
ShortName:	DDI_AUX_CTL_F
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31	**Send Busy** Access: R/W Set Writing this bit with 1b initiates the transaction, when read this bit will be a 1b until the transmission completes. The transaction is completed when the response is received or when a timeout occurs. This is a sticky bit. Write a 1b to this bit to set it and initiate the transaction. Hardware will clear it when the transaction completes. **Programming Notes** Aux IO power must be enabled in PWR_WELL_CTL prior to starting an Aux transaction. **Restriction** Do not change any fields while Send Busy is asserted. Do not write a 1b again until transaction completes.
	30	**Done** Access: R/WC A sticky bit that indicates the transaction has completed. Write a 1 to this bit to clear the event Value: 0b – Name: Not done Value: 1b – Name: Done
	29	**Interrupt on Done** Access: R/W Enable an interrupt when the transaction completes or times out. Value: 0b – Name: Disable Value: 1b – Name: Enable
	28	**Time out error** Access: R/WC A sticky bit that indicates the transaction has timed out. Write a 1 to this bit to clear the event. Value – Name

DDI_AUX_CTL

	0b	Not error
	1b	Error

27:26 Time out timer value

Access:	R/W

Used to determine how long to wait for receiver response before timing out.

Value	Name
01b	600us **[Default]**
10b	800us
11b	4000us

25 Receive error

Access:	R/WC

A sticky bit that indicates that the data received was corrupted, not in multiples of a full byte, or more than 20 bytes. Write a 1 to this bit to clear the event.

Value	Name
0b	Not Error
1b	Error

24:20 Message Size

Access:	Write/Read Status

The value written to this field indicates the total number bytes to transmit (including the header). The value read from this field indicates the number of bytes received, including the header, in the last transaction. Sync/Stop are not part of the message or the message size. Reads of this field will give the response message size. The read value will not be valid while Send/Busy bit 31 is asserted.

Restriction
Message sizes of 0 or >20 are not allowed. Reads and writes are valid only when the done bit is set and timeout or receive error has not occurred.

19:16 Reserved

15 Reserved

14 Reserved

13 Reserved

12 Reserved

11 IO Select

DDI_AUX_CTL

		Access: R/W This field selects which IO will be used for the Aux transaction. It must not be switched while a transaction is in progress. **Value** / **Name** / **Description** 1b / TBT / Use Thunderbolt IO 0b / Legacy / Use legacy IO. Either typeC or regular DDI, depending on project and SKU
	10	**Reserved**
	9:5	**Fast Wake Sync Pulse Count** Default Value: 1 0001b 18 pulses Access: R/W This field determines the total number of SYNC pulses sent during the SYNC phase of a fast wake transaction. The value programmed is the number of pulses minus 1. When this is field is set to "n" the aux controller will send "n+1" SYNC pulses before transmitting the STOP pattern.
	4:0	**Sync Pulse Count** Default Value: 1 1111b 32 pulses Access: R/W This field determines the total number of SYNC pulses sent during the SYNC phase of a standard transaction. The value programmed is the number of pulses minus 1. When this is field is set to "n" the aux controller will send "n+1" SYNC pulses before transmitting the STOP pattern. **Restriction** This field must be programmed to at least 25 decimal to send the minimum amount of pulses required for a standard transaction.

DDI_AUX_DATA

DDI_AUX_DATA	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Write/Read Status
Size (in bits):	32
Address:	64014h-64027h
Name:	DDI A AUX Channel Data
ShortName:	DDI_AUX_DATA_A_*
Power:	PG1
Reset:	soft
Address:	64114h-64127h
Name:	DDI B AUX Channel Data
ShortName:	DDI_AUX_DATA_B_*
Power:	PG2
Reset:	soft
Address:	64214h-64227h
Name:	DDI C AUX Channel Data
ShortName:	DDI_AUX_DATA_C_*
Power:	PG2
Reset:	soft
Address:	64314h-64327h
Name:	DDI D AUX Channel Data
ShortName:	DDI_AUX_DATA_D_*
Power:	PG2
Reset:	soft
Address:	64414h-64427h
Name:	DDI E AUX Channel Data
ShortName:	DDI_AUX_DATA_E_*

DDI_AUX_DATA

Power:	PG2
Reset:	soft
Address:	64514h-64527h
Name:	DDI F AUX Channel Data
ShortName:	DDI_AUX_DATA_F_*
Power:	PG2
Reset:	soft

There are 5 DWords of this register format per instance.

DWord	Bit	Description
0	31:0	**AUX CH DATA** This field contains a DWord of the AUX message. Writes to this register give the data to transmit during the transaction. The MSbyte is transmitted first. Reads to this register will give the response data after transaction complete. The read value will not be valid while the Aux Channel Control Register Send/Busy bit is asserted

DDI_BUF_CTL

DDI_BUF_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	64000h-64003h
Name:	DDI A Buffer Control
ShortName:	DDI_BUF_CTL_A
Power:	PG1
Reset:	soft
Address:	64100h-64103h
Name:	DDI B Buffer Control
ShortName:	DDI_BUF_CTL_B
Power:	PG1
Reset:	soft
Address:	64200h-64203h
Name:	DDI C Buffer Control
ShortName:	DDI_BUF_CTL_C
Power:	PG1
Reset:	soft
Address:	64300h-64303h
Name:	DDI D Buffer Control
ShortName:	DDI_BUF_CTL_D
Power:	PG1
Reset:	soft
Address:	64400h-64403h
Name:	DDI E Buffer Control
ShortName:	DDI_BUF_CTL_E

DDI_BUF_CTL

Power: PG1
Reset: soft

Address: 64500h-64503h
Name: DDI F Buffer Control
ShortName: DDI_BUF_CTL_F

Power: PG1
Reset: soft

Do not read or write the register when the associated power well is disabled.

DWord	Bit	Description
0	31	**DDI Buffer Enable** This bit enables the DDI buffer. Value: 0b = Disable; 1b = Enable
	30	**Reserved** Format: MBZ
	29	**Override Training Enable** This field enables the override on the training enable signal that tells the DDI I/O to pick up any DDI voltage swing and pre-emphasis changes. Value: 1b = Enable Override; 0b = Disable Override
	28	**Phy Param Adjust** Enables adjustment of Phy parameters such as voltage swing and pre emphasis outside Inik training process. This field is conditioned on "override training enable" (DDI_BUF_CTL[29]). Value: 1b = Enable; 0b = Disable
	27:24	**Reserved** Format: MBZ
	23:17	**Reserved** Format: MBZ

DDI_BUF_CTL

16 Port Reversal

This field enables lane reversal within the port. Lane reversal swaps the data on the lanes as they are output from the port.

Value	Name
0b	Not reversed
1b	Reversed

Programming Notes
Type-C/TBT dynamic connections: The DDIs going to thunderbolt or USB-C DP alternate mode should not be reversed here. The reversal is taken care of in the FIA. Static/fixed connections (DP/HDMI) through FIA: In the case of static connections such as "No pin assignment (Non Type-C DP)", DDIs will use this lane reversal bit. All other connections: DDIs will use this lane reversal bit.

Restriction
This field must not be changed while the DDI is enabled.

15:8 USB Type-C DP Lane Staggering Delay

Specifies the number of symbol clocks delay used to stagger assertion/deassertion of the port lane enables. The target time recommended by circuit team is 100ns or greater. The delay should be programmed based on link clock frequency. This staggering delay is ONLY required when the port is used in USB Type C mode. Otherwise the default delay is zero which means no staggering. Example: 270MHz link clock = 1/270MHz = 3.7ns. (100ns/3.7ns)=27.02 symbols. Round up to 28.

7 DDI Idle Status

Access:	RO

This bit indicates when the DDI buffer is idle.

Value	Name
0b	Buffer Not Idle
1b	Buffer Idle

6:5 Reserved

Format:	MBZ

4 Reserved

Format:	MBZ

3:1 DP Port Width Selection

Description
This bit selects the number of lanes to be enabled on the DDI link for DisplayPort.

Value	Name	Description
000b	x1	x1 Mode
001b	x2	x2 Mode
011b	x4	x4 Mode
Others	Reserved	Reserved

Restriction
When in DisplayPort mode the value selected here must match the value selected in TRANS_DDI_FUNC_CTL attached to this DDI.
This field must not be changed while the DDI is enabled.

0 **Init Display Detected**

Access:	RO

Strap indicating whether a display was detected on this port during initialization. It signifies the level of the port detect pin at boot. This bit is only informative. It does not prevent this port from being enabled in hardware. This field only indicates the DDIA detection. Detection for other ports is read from SFUSE_STRAP.

Value	Name	Description
0b	Not Detected	Digital display not detected during initialization
1b	Detected	Digital display detected during initialization

DDI_CLK_SEL

DDI_CLK_SEL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	46108h-4610Bh
Name:	DDI C Clock Select
ShortName:	DDI_CLK_SEL_C
Power:	PG0
Reset:	soft
Address:	4610Ch-4610Fh
Name:	DDI D Clock Select
ShortName:	DDI_CLK_SEL_D
Power:	PG0
Reset:	soft
Address:	46110h-46113h
Name:	DDI E Clock Select
ShortName:	DDI_CLK_SEL_E
Power:	PG0
Reset:	soft
Address:	46114h-46117h
Name:	DDI F Clock Select
ShortName:	DDI_CLK_SEL_F
Power:	PG0
Reset:	soft
Address:	46118h-4611Bh
Name:	DDI G Clock Select
ShortName:	DDI_CLK_SEL_G

DDI_CLK_SEL

Power:	PG0
Reset:	soft

Address:	4611Ch-4611Fh
Name:	DDI H Clock Select
ShortName:	DDI_CLK_SEL_H
Power:	PG0
Reset:	soft

DWord	Bit	Description
0	31:28	**Clock Select** Select which clock to use for this DDI.

Value	Name	Description
0000b	None	Nothing selected. Clock is disabled for this DDI.
1000b	MG	MG PLL output
1100b	TBT 162	Thunderbolt 162 MHz
1101b	TBT 270	Thunderbolt 270 MHz
1110b	TBT 540	Thunderbolt 540 MHz
1111b	TBT 810	Thunderbolt 810 MHz

Restriction
This must not be changed while the DDI is enabled or any transcoder directed to the DDI is enabled.

DWord	Bit	Description
	27:0	**Reserved**

Format:	MBZ

DE_PIPE_INTERRUPT

DE_PIPE_INTERRUPT	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	44400h-4440Fh
Name:	Display Engine Pipe A Interrupts
ShortName:	DE_PIPE_INTERRUPT_A
Power:	PG1
Reset:	soft
Address:	44410h-4441Fh
Name:	Display Engine Pipe B Interrupts
ShortName:	DE_PIPE_INTERRUPT_B
Power:	PG2
Reset:	soft
Address:	44420h-4442Fh
Name:	Display Engine Pipe C Interrupts
ShortName:	DE_PIPE_INTERRUPT_C
Power:	PG2
Reset:	soft

Description

This table indicates which events are mapped to each bit of the Display Engine Pipe Interrupt registers. The IER enabled Display Engine Pipe Interrupt IIR (sticky) bits are ORed together to generate the DE_Pipe Interrupts Pending bit in the Master Interrupt Control register. There is one full set of Display Engine Pipe interrupts per display pipes A/B/C. The STEREO3D_EVENT_MASK selects between left eye and right eye reporting of vertical blank, vertical sync, and scanline events in stereo 3D modes.

0x44400 = ISR A, 0x44410 = ISR B, 0x44420 = ISR C
0x44404 = IMR A, 0x44414 = IMR B, 0x44424 = IMR C
0x44408 = IIR A, 0x44418 = IIR B, 0x44428 = IIR C
0x4440C = IER A, 0x4441C = IER B, 0x4442C = IER C

DWord	Bit	Description
0	31	**Underrun** **Description**

DE_PIPE_INTERRUPT

		The ISR is an active high pulse when there is an underrun on the transcoder attached to this pipe.
	30	**Unused_Int_30** These interrupts are currently unused.
	29	**Reserved**
	28	**Reserved**
	27:23	**Unused_Int_27_23** These interrupts are currently unused.
	22	**Plane7_GTT_Fault_Status** The ISR is an active high pulse when a GTT fault is detected for plane 7 on this pipe.
	21	**Plane6_GTT_Fault_Status** The ISR is an active high pulse when a GTT fault is detected for plane 6 on this pipe.
	20	**Plane5_GTT_Fault_Status** The ISR is an active high pulse when a GTT fault is detected for plane 5 on this pipe.
	19	**Reserved** Format: MBZ
	18	**Plane7_Flip_Done** The ISR is an active high pulse when the flip is done for plane 7 on this pipe.
	17	**Plane6_Flip_Done** The ISR is an active high pulse when the flip is done for plane 6 on this pipe.
	16	**Plane5_Flip_Done** The ISR is an active high pulse when the flip is done for plane 5 on this pipe.

DE_PIPE_INTERRUPT

	15:13	**Unused_Int_15_13** These interrupts are currently unused.
	12	**DPST_Histogram_event** The ISR is an active high pulse on the DPST Histogram event on this pipe.
	11	**Cursor_GTT_Fault_Status** The ISR is an active high pulse when a GTT fault is detected for the cursor on this pipe.
	10	**Plane4_GTT_Fault_Status** **Description** The ISR is an active high pulse when a GTT fault is detected for plane 4 on this pipe.
	9	**Plane3_GTT_Fault_Status** **Description** The ISR is an active high pulse when a GTT fault is detected for plane 3 on this pipe.
	8	**Plane2_GTT_Fault_Status** The ISR is an active high pulse when a GTT fault is detected for plane 2 on this pipe.
	7	**Plane1_GTT_Fault_Status** The ISR is an active high pulse when a GTT fault is detected for plane 1 on this pipe.
	6	**Plane4_Flip_Done** **Description** The ISR is an active high pulse when the flip is done for plane 4 on this pipe.
	5	**Plane3_Flip_Done** **Description** The ISR is an active high pulse when the flip is done for plane 3 on this pipe.

DE_PIPE_INTERRUPT		
	4	**Plane2_Flip_Done** The ISR is an active high pulse when the flip is done for plane 2 on this pipe.
	3	**Plane1_Flip_Done** The ISR is an active high pulse when the flip is done for plane 1 on this pipe.
	2	**Scan_Line_Event** The ISR is an active high pulse on the scan line event of the transcoder attached to this pipe.
	1	**Vsync** The ISR is an active high level for the duration of the vertical sync of the transcoder attached to this pipe.
	0	**Vblank** The ISR is an active high level for the duration of the vertical blank of the transcoder attached to this pipe.

DE_PLL_ADCFG_1

DE_PLL_ADCFG_1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6D804h-6D807h
Name:	DE PLL Control
ShortName:	DE_PLL_ADCFG_1
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31	**SKIP TDCCALIB** Value: 0b — Name: Value: 1b — Name: **[Default]**
	30	**PLLEN VAL** Value: 0b — Name: Value: 1b — Name: **[Default]**
	29	**PLLEN OVRD** Value: 0b — Name: Value: 1b — Name:
	28:23	**PEMOD AMP**
	22	**PE MINMAXRST** Value: 0b — Name: Value: 1b — Name:
	21	**PE MINMAXEN** Value: 0b — Name: Value: 1b — Name:
	20:19	**LOCKWDET WIN**

DE_PLL_ADCFG_1

	18:12	**LOCKTIMERCNT TH** Default Value: 28h
	11	**Reserved** Format: MBZ
	10:9	**KPSCALE**
	8:7	**KPKISCALE CNT** Default Value: 3h
	6:5	**KISCALE**
	4:1	**INT COEFF** Default Value: Ch
	0	**FINE SWEEPEN** Value / Name 0b 1b

DE_POWER1

DE_POWER1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	42400h-42403h
Name:	Display Engine Power 1
ShortName:	DE_POWER1
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31	**Power Well 2 State** This field indicates the status of display power well 2. Value: 0b = Off; 1b = On
	30	**Display Pipes Enabled** This field indicates if any display pipes are enabled. Value: 0b = Disabled (All display pipes disabled); 1b = Enabled (One or more display pipes enabled)
	29	**Reserved** Format: MBZ
	28	**Power Well 1 State** This field indicates the status of display power well 1. Value: 0b = Off; 1b = On
	27:26	**SRD Status** Description

DE_POWER1

		This field indicates the live status of the SRD link on eDP DDI-A. **Value** / **Name** / **Description** 00b / Full Off / Link is fully off. DDI lanes are disabled and most memory reads are disabled. 01b / Full On / Link is fully on. Normal operation. 10b / Standby / Link is in standby. Most memory reads are disabled. 11b / Reserved / Reserved
	25	**KVM Session Status** This field indicates the status of KVM session. **Value** / **Name** / **Description** 0b / Disabled / KVM session disabled 1b / Enabled / KVM session enabled
	24:14	**Reserved** Format: MBZ
	13:10	**Enabled Pipe Scalers** Indicates total usage of the Scaler EBBs.
	9:8	**Enabled DEPLLs** The total number of Display PLLs enabled.
	7:4	**Transmit Lanes Enabled** The total number of DDI lanes enabled.
	3	**Enabled CDPLLs** Indicates if CD PLL is enabled.
	2:0	**Enabled MGPLLs** The total number of Display MG PLLs enabled.

DE_POWER2

DE_POWER2		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Access:	RO	
Size (in bits):	32	
Address:	42404h-42407h	
Name:	Display Engine Power 2	
ShortName:	DE_POWER2	
Power:	PG0	
Reset:	global	
DWord	**Bit**	**Description**
0	31:0	**DE bandwidth counter** This counter increments on every cache line put arriving at the DE. The bandwidth is estimated by taking the difference between two reads at a known interval. Access is actually a read/write variant. Writes to this register will load the write data into the counter.

DE_RR_DEST

DE_RR_DEST

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	44058h-4405Bh
Name:	Render Response Destination
ShortName:	DE_RR_DEST
Power:	PG0
Reset:	soft

This register selects the destination of certain render responses that may go to CS, BCS, or both. In order for a response to be sent to a particular destination, the event most occur, the event must be unmasked, and that destination must be selected.

DWord	Bit	Description
0	31:6	**Reserved** Format: MBZ
	5:4	**Pipe C Vertical Blank Destination** This field selects the destination for the render response sent on pipe C start of vertical blank. 00b: CS 01b: BCS 10b,11b: Both CS and BCS
	3:2	**Pipe B Vertical Blank Destination** This field selects the destination for the render response sent on pipe B start of vertical blank. 00b: CS 01b: BCS 10b,11b: Both CS and BCS
	1:0	**Pipe A Vertical Blank Destination** This field selects the destination for the render response sent on pipe A start of vertical blank.

DE_RR_DEST			
		Value	Name
		00b	CS
		01b	BCS
		10b,11b	Both CS and BCS

DE_RRMR_DW1

DE_RRMR_DW1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	44048h-4404Bh
Name:	Render Response Mask DW 1
ShortName:	DE_RRMR_DW1
Power:	PG0
Reset:	soft

This register contains the Dword 1 of the CS/BCS render response bit mask. For more details refer to DE_RRMR.

DWord	Bit	Description
0	31	**Mask 31** Value: 0b – Not Masked Value: 1b – Masked **[Default]**
	30	**Mask 30** Value: 0b – Not Masked Value: 1b – Masked **[Default]**
	29	**Mask 29** Value: 0b – Not Masked Value: 1b – Masked **[Default]**
	28	**Mask 28** Value: 0b – Not Masked Value: 1b – Masked **[Default]**
	27	**Mask 27** Value: 0b – Not Masked Value: 1b – Masked **[Default]**
	26	**Mask 26**

DE_RRMR_DW1

		Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	25	**Mask 25** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	24	**Mask 24** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	23	**Mask 23** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	22	**Mask 22** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	21	**Mask 21** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	20	**Mask 20** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	19	**Mask 19** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	18	**Mask 18** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**

DE_RRMR_DW1

17	**Mask 17** **Value** / **Name** 0b – Not Masked 1b – Masked **[Default]**
16	**Mask 16** **Value** / **Name** 0b – Not Masked 1b – Masked **[Default]**
15	**Mask 15** **Value** / **Name** 0b – Not Masked 1b – Masked **[Default]**
14	**Mask 14** **Value** / **Name** 0b – Not Masked 1b – Masked **[Default]**
13	**Mask 13** **Value** / **Name** 0b – Not Masked 1b – Masked **[Default]**
12	**Mask 12** **Value** / **Name** 0b – Not Masked 1b – Masked **[Default]**
11	**Mask 11** **Value** / **Name** 0b – Not Masked 1b – Masked **[Default]**
10	**Mask 10** **Value** / **Name** 0b – Not Masked 1b – Masked **[Default]**
9	**Mask 9** **Value** / **Name** 0b – Not Masked

DE_RRMR_DW1

	1b	Masked **[Default]**
8	**Mask 8**	
	Value	**Name**
	0b	Not Masked
	1b	Masked **[Default]**
7	**Mask 7**	
	Value	**Name**
	0b	Not Masked
	1b	Masked **[Default]**
6	**Mask 6**	
	Value	**Name**
	0b	Not Masked
	1b	Masked **[Default]**
5	**Mask 5**	
	Value	**Name**
	0b	Not Masked
	1b	Masked **[Default]**
4	**Mask 4**	
	Value	**Name**
	0b	Not Masked
	1b	Masked **[Default]**
3	**Mask 3**	
	Value	**Name**
	0b	Not Masked
	1b	Masked **[Default]**
2	**Mask 2**	
	Value	**Name**
	0b	Not Masked
	1b	Masked **[Default]**
1	**Mask 1**	
	Value	**Name**
	0b	Not Masked
	1b	Masked **[Default]**
0	**Mask 0**	
	Value	**Name**

DE_RRMR_DW1			
		0b	Not Masked
		1b	Masked **[Default]**

DE_RRMR_DW2

DE_RRMR_DW2

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	4404Ch-4404Fh
Name:	Render Response Mask DW 2
ShortName:	DE_RRMR_DW2
Power:	PG0
Reset:	soft

This register contains the DWord 2 of the CS/BCS render response bit mask. For more details refer to DE_RRMR.

DWord	Bit	Description
0	31	**Mask 31** Value: 0b – Not Masked Value: 1b – Masked **[Default]**
	30	**Mask 30** Value: 0b – Not Masked Value: 1b – Masked **[Default]**
	29	**Mask 29** Value: 0b – Not Masked Value: 1b – Masked **[Default]**
	28	**Mask 28** Value: 0b – Not Masked Value: 1b – Masked **[Default]**
	27	**Mask 27** Value: 0b – Not Masked Value: 1b – Masked **[Default]**
	26	**Mask 26**

DE_RRMR_DW2

Value	Name
0b	Not Masked
1b	Masked **[Default]**

25 **Mask 25**

Value	Name
0b	Not Masked
1b	Masked **[Default]**

24 **Mask 24**

Value	Name
0b	Not Masked
1b	Masked **[Default]**

23 **Mask 23**

Value	Name
0b	Not Masked
1b	Masked **[Default]**

22 **Mask 22**

Value	Name
0b	Not Masked
1b	Masked **[Default]**

21 **Mask 21**

Value	Name
0b	Not Masked
1b	Masked **[Default]**

20 **Mask 20**

Value	Name
0b	Not Masked
1b	Masked **[Default]**

19 **Mask 19**

Value	Name
0b	Not Masked
1b	Masked **[Default]**

18 **Mask 18**

Value	Name
0b	Not Masked
1b	Masked **[Default]**

DE_RRMR_DW2

	17	**Mask 17** **Value** / **Name** 0b – Not Masked 1b – Masked **[Default]**
	16	**Mask 16** **Value** / **Name** 0b – Not Masked 1b – Masked **[Default]**
	15	**Mask 15** **Value** / **Name** 0b – Not Masked 1b – Masked **[Default]**
	14	**Mask 14** **Value** / **Name** 0b – Not Masked 1b – Masked **[Default]**
	13	**Mask 13** **Value** / **Name** 0b – Not Masked 1b – Masked **[Default]**
	12	**Mask 12** **Value** / **Name** 0b – Not Masked 1b – Masked **[Default]**
	11	**Mask 11** **Value** / **Name** 0b – Not Masked 1b – Masked **[Default]**
	10	**Mask 10** **Value** / **Name** 0b – Not Masked 1b – Masked **[Default]**
	9	**Mask 9** **Value** / **Name** 0b – Not Masked

DE_RRMR_DW2

	1b	Masked **[Default]**
8	**Mask 8**	
	Value	**Name**
	0b	Not Masked
	1b	Masked **[Default]**
7	**Mask 7**	
	Value	**Name**
	0b	Not Masked
	1b	Masked **[Default]**
6	**Mask 6**	
	Value	**Name**
	0b	Not Masked
	1b	Masked **[Default]**
5	**Mask 5**	
	Value	**Name**
	0b	Not Masked
	1b	Masked **[Default]**
4	**Mask 4**	
	Value	**Name**
	0b	Not Masked
	1b	Masked **[Default]**
3	**Mask 3**	
	Value	**Name**
	0b	Not Masked
	1b	Masked **[Default]**
2	**Mask 2**	
	Value	**Name**
	0b	Not Masked
	1b	Masked **[Default]**
1	**Mask 1**	
	Value	**Name**
	0b	Not Masked
	1b	Masked **[Default]**
0	**Mask 0**	
	Value	**Name**

DE_RRMR_DW2			
		0b	Not Masked
		1b	Masked **[Default]**

DE_RRMR

DE_RRMR	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	44050h-44053h
Name:	Render Response Mask
ShortName:	DE_RRMR
Power:	PG0
Reset:	soft

Description

This register contains a bit mask which selects which events cause and are reported in the render response message. See the render response message definition table to find the source event for each bit. The render response message is sent from the display engine to the render command streamer (CS) or blitter command streamer (BCS). The message is used to inform CS and BCS of certain display events. This register is used to control which render response message bits are masked or unmasked. Unmasked bits will cause a render response message to be sent and will be reported in that message. Masked bits will not be reported and will not cause a render response message to be sent. Vertical blank events occur periodically while the associated display pipe timing generator is running and will be reported in a render response to CS or BCS (depending on DE_RR_DEST destination selection) if un-masked here. Scanline events occur after they have been initiated through MMIO writes or LRI to the Display Load Scan Lines register. A flip event will be reported in a render response to CS if un-masked here and the Display Load Scanline source is CS. A flip event will be reported in a render response to BCS if un-masked here and the Display Load Scanline source is BCS. Flip done events occur after they have been initiated through MI_DISPLAY_FLIP or MMIO write to plane surface address registers. A flip event will be reported in a render response to CS if un-masked here and the flip source is CS. A flip event will be reported in a render response to BCS if un-masked here and the flip source is BCS.

This register defines the DWord 0 of the render response bit mask. DWord 1 and DWord 2 are defined in DE_RRMR_DW1 and DE_RRMR_DW2 registers.

Programming Notes

Programming this register can be done through MMIO or a command streamer LOAD_REGISTER_IMMEDIATE (LRI) command. When using LRI care must be taken to follow all the programming rules for LRI targeting the display engine. Unmasked events will wake GT as they occur, so for improved power savings it is recommended to only unmask events that are required.

Restriction

Events must be unmasked prior to waiting for them with a MI_WAIT_FOR_EVENT ring command, or in the case of flips or scanlines, prior to starting the flip or loading the scanline.

DWord	Bit	Description
0	31	**Mask 31** | | | |---|---| | | | | Value | Name | |---|---| | 0b | Not Masked | | 1b | Masked **[Default]** |
	30	**Mask 30** | | | |---|---| | | | | Value | Name | |---|---| | 0b | Not Masked | | 1b | Masked **[Default]** |
	29	**Mask 29** | Value | Name | |---|---| | 0b | Not Masked | | 1b | Masked **[Default]** |
	28	**Mask 28** | | | |---|---| | | | | Value | Name | |---|---| | 0b | Not Masked | | 1b | Masked **[Default]** |
	27	**Mask 27** | | | |---|---| | | | | Value | Name | |---|---| | 0b | Not Masked | | 1b | Masked **[Default]** |
	26	**Mask 26** | | | |---|---| | | | | Value | Name | |---|---| | 0b | Not Masked | | 1b | Masked **[Default]** |
	25	**Mask 25** | | | |---|---| | | |

DE_RRMR

Value	Name
0b	Not Masked
1b	Masked **[Default]**

24 **Mask 24**

Value	Name
0b	Not Masked
1b	Masked **[Default]**

23 **Mask 23**

Value	Name
0b	Not Masked
1b	Masked **[Default]**

22 **Mask 22**

Value	Name
0b	Not Masked
1b	Masked **[Default]**

21 **Mask 21**

Value	Name
0b	Not Masked
1b	Masked **[Default]**

20 **Mask 20**

Value	Name
0b	Not Masked
1b	Masked **[Default]**

19 **Mask 19**

Value	Name
0b	Not Masked
1b	Masked **[Default]**

18 **Mask 18**

Value	Name
0b	Not Masked

DE_RRMR

		1b: Masked **[Default]**
	17	**Mask 17** 0b: Not Masked 1b: Masked **[Default]**
	16	**Mask 16** 0b: Not Masked 1b: Masked **[Default]**
	15	**Mask 15** 0b: Not Masked 1b: Masked **[Default]**
	14	**Mask 14** 0b: Not Masked 1b: Masked **[Default]**
	13	**Mask 13** 0b: Not Masked 1b: Masked **[Default]**
	12	**Mask 12** 0b: Not Masked 1b: Masked **[Default]**
	11	**Mask 11** 0b: Not Masked 1b: Masked **[Default]**
	10	**Mask 10** 0b: Not Masked 1b: Masked **[Default]**

DE_RRMR

	9	**Mask 9** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	8	**Mask 8** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	7	**Mask 7** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	6	**Mask 6** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	5	**Mask 5** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	4	**Mask 4** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	3	**Mask 3** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	2	**Mask 2** Value: 0b — Name: Not Masked Value: 1b — Name: Masked **[Default]**
	1	**Mask 1** Value — Name

<table>
<tr><th colspan="3">DE_RRMR</th></tr>
<tr><td rowspan="2"></td><td></td><td><table>
<tr><td>0b</td><td>Not Masked</td></tr>
<tr><td>1b</td><td>Masked [Default]</td></tr>
</table></td></tr>
<tr><td>0</td><td>Mask 0<table>
<tr><th>Value</th><th>Name</th></tr>
<tr><td>0b</td><td>Not Masked</td></tr>
<tr><td>1b</td><td>Masked [Default]</td></tr>
</table></td></tr>
</table>

Decouple Register 0 DW0

DECOUPREG0DW0 - Decouple Register 0 DW0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00F00h-00F03h	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg0DW0Data** Access: R/W Decouple Register 0 DW0 Data.

Decouple Register 0 DW1

DECOUPREG0DW1 - Decouple Register 0 DW1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00F04h-00F07h	
DWord	**Bit**	**Description**
0	31	**GO** Access: R/W Lock Decouple Register Go/Status Bit: Software sets this bit along with attributes (full DW write) to initiate a DCR request. Hardware clears this bit to 0 when the command is complete. This bit serves as a lock for the register pair preventing software from updating the status/values once set.
	30:28	**OP** Access: R/W Lock Decouple Register Opcode: 3'b000 = Read, 3'b001 = Write; All others undefined (Request ignored and go/status cleared).
	27:24	**BE_B** Access: R/W Lock Decouple Register Active Low Byte Enables. Byte enables affect data merging into MGSR shadow storage however GT only supports full dword accesses.
	23:0	**Addr** Access: R/W Lock Decouple Register Address.

Decouple Register 1 DW0

DECOUPREG1DW0 - Decouple Register 1 DW0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00F08h-00F0Bh	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg1DW0Data** Access: R/W Decouple Register 1 DW0 Data.

Decouple Register 1 DW1

DECOUPREG1DW1 - Decouple Register 1 DW1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00F0Ch-00F0Fh	
DWord	**Bit**	**Description**
0	31	**GO** Access: R/W Lock Decouple Register Go/Status Bit: Software sets this bit along with attributes (full DW write) to initiate a DCR request. Hardware clears this bit to 0 when the command is complete. This bit serves as a lock for the register pair preventing software from updating the status/values once set.
	30:28	**OP** Access: R/W Lock Decouple Register Opcode: 3'b000 = Read, 3'b001 = Write; All others undefined (Request ignored and go/status cleared).
	27:24	**BE_B** Access: R/W Lock Decouple Register Active Low Byte Enables. Byte enables affect data merging into MGSR shadow storage however GT only supports full dword accesses.
	23:0	**Addr** Access: R/W Lock Decouple Register Address.

Decouple Register 2 DW0

DECOUPREG2DW0 - Decouple Register 2 DW0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00F10h-00F13h	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg2DW0Data** Access: R/W Decouple Register 2 DW0 Data.

Decouple Register 2 DW1

DECOUPREG2DW1 - Decouple Register 2 DW1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00F14h-00F17h	
DWord	**Bit**	**Description**
0	31	**GO** Access: R/W Lock Decouple Register Go/Status Bit: Software sets this bit along with attributes (full DW write) to initiate a DCR request. Hardware clears this bit to 0 when the command is complete. This bit serves as a lock for the register pair preventing software from updating the status/values once set.
	30:28	**OP** Access: R/W Lock Decouple Register Opcode: 3'b000 = Read, 3'b001 = Write; All others undefined (Request ignored and go/status cleared).
	27:24	**BE_B** Access: R/W Lock Decouple Register Active Low Byte Enables. Byte enables affect data merging into MGSR shadow storage however GT only supports full dword accesses.
	23:0	**Addr** Access: R/W Lock Decouple Register Address.

Decouple Register 3 DW0

DECOUPREG3DW0 - Decouple Register 3 DW0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00F18h-00F1Bh	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg3DW0Data** Access: R/W Decouple Register 3 DW0 Data.

Decouple Register 3 DW1

DECOUPREG3DW1 - Decouple Register 3 DW1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00F1Ch-00F1Fh	
DWord	**Bit**	**Description**
0	31	**GO** Access: R/W Lock Decouple Register Go/Status Bit: Software sets this bit along with attributes (full DW write) to initiate a DCR request. Hardware clears this bit to 0 when the command is complete. This bit serves as a lock for the register pair preventing software from updating the status/values once set.
	30:28	**OP** Access: R/W Lock Decouple Register Opcode: 3'b000 = Read, 3'b001 = Write; All others undefined (Request ignored and go/status cleared).
	27:24	**BE_B** Access: R/W Lock Decouple Register Active Low Byte Enables. Byte enables affect data merging into MGSR shadow storage however GT only supports full dword accesses.
	23:0	**Addr** Access: R/W Lock Decouple Register Address.

Decouple Register 4 DW0

DECOUPREG4DW0 - Decouple Register 4 DW0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00F20h-00F23h	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg4DW0Data** Access: R/W Decouple Register 4 DW0 Data. Due to Gen10 architectural bug 1942120, DCR requests on the NP path will be blocked during CPD

Decouple Register 4 DW1

DECOUPREG4DW1 - Decouple Register 4 DW1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00F24h-00F27h	
DWord	**Bit**	**Description**
0	31	**GO** Access: R/W Lock Decouple Register Go/Status Bit: Software sets this bit along with attributes (full DW write) to initiate a DCR request. Hardware clears this bit to 0 when the command is complete. This bit serves as a lock for the register pair preventing software from updating the status/values once set.
	30:28	**OP** Access: R/W Lock Decouple Register Opcode: 3'b000 = Read, 3'b001 = Write; All others undefined (Request ignored and go/status cleared).
	27:24	**BE_B** Access: R/W Lock Decouple Register Active Low Byte Enables. Byte enables affect data merging into MGSR shadow storage however GT only supports full dword accesses.
	23:0	**Addr** Access: R/W Lock Decouple Register Address.

Decouple Register 5 DW0

DECOUPREG5DW0 - Decouple Register 5 DW0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00F28h-00F2Bh	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg5DW0Data** Access: R/W Decouple Register 5 DW0 Data.

Decouple Register 5 DW1

DECOUPREG5DW1 - Decouple Register 5 DW1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00F2Ch-00F2Fh	
DWord	**Bit**	**Description**
0	31	**GO** Access: R/W Lock Decouple Register Go/Status Bit: Software sets this bit along with attributes (full DW write) to initiate a DCR request. Hardware clears this bit to 0 when the command is complete. This bit serves as a lock for the register pair preventing software from updating the status/values once set.
	30:28	**OP** Access: R/W Lock Decouple Register Opcode: 3'b000 = Read, 3'b001 = Write; All others undefined (Request ignored and go/status cleared).
	27:24	**BE_B** Access: R/W Lock Decouple Register Active Low Byte Enables. Byte enables affect data merging into MGSR shadow storage however GT only supports full dword accesses.
	23:0	**Addr** Access: R/W Lock Decouple Register Address.

Decouple Register 6 DW0

DECOUPREG6DW0 - Decouple Register 6 DW0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00F30h-00F33h	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg6DW0Data** Access: R/W Decouple Register 6 DW0 Data.

Decouple Register 6 DW1

DECOUPREG6DW1 - Decouple Register 6 DW1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00F34h-00F37h

DWord	Bit	Description
0	31	**GO** Access: R/W Lock Decouple Register Go/Status Bit: Software sets this bit along with attributes (full DW write) to initiate a DCR request. Hardware clears this bit to 0 when the command is complete. This bit serves as a lock for the register pair preventing software from updating the status/values once set.
	30:28	**OP** Access: R/W Lock Decouple Register Opcode: 3'b000 = Read, 3'b001 = Write; All others undefined (Request ignored and go/status cleared).
	27:24	**BE_B** Access: R/W Lock Decouple Register Active Low Byte Enables. Byte enables affect data merging into MGSR shadow storage however GT only supports full dword accesses.
	23:0	**Addr** Access: R/W Lock Decouple Register Address.

Decouple Register 7 DW0

DECOUPREG7DW0 - Decouple Register 7 DW0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00F38h-00F3Bh	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg7DW0Data** Access: R/W Decouple Register 7 DW0 Data.

Decouple Register 7 DW1

DECOUPREG7DW1 - Decouple Register 7 DW1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00F3Ch-00F3Fh	
DWord	**Bit**	**Description**
0	31	**GO** Access: R/W Lock Decouple Register Go/Status Bit: Software sets this bit along with attributes (full DW write) to initiate a DCR request. Hardware clears this bit to 0 when the command is complete. This bit serves as a lock for the register pair preventing software from updating the status/values once set.
	30:28	**OP** Access: R/W Lock Decouple Register Opcode: 3'b000 = Read, 3'b001 = Write; All others undefined (Request ignored and go/status cleared).
	27:24	**BE_B** Access: R/W Lock Decouple Register Active Low Byte Enables. Byte enables affect data merging into MGSR shadow storage however GT only supports full dword accesses.
	23:0	**Addr** Access: R/W Lock Decouple Register Address.

Decouple Register 8 DW0

DECOUPREG8DW0 - Decouple Register 8 DW0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00F40h-00F43h	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg8DW0Data** Access: R/W Decouple Register 8 DW0 Data.

Decouple Register 8 DW1

DECOUPREG8DW1 - Decouple Register 8 DW1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00F44h-00F47h	
DWord	**Bit**	**Description**
0	31	**GO** Access: R/W Lock Decouple Register Go/Status Bit: Software sets this bit along with attributes (full DW write) to initiate a DCR request. Hardware clears this bit to 0 when the command is complete. This bit serves as a lock for the register pair preventing software from updating the status/values once set.
	30:28	**OP** Access: R/W Lock Decouple Register Opcode: 3'b000 = Read, 3'b001 = Write; All others undefined (Request ignored and go/status cleared).
	27:24	**BE_B** Access: R/W Lock Decouple Register Active Low Byte Enables. Byte enables affect data merging into MGSR shadow storage however GT only supports full dword accesses.
	23:0	**Addr** Access: R/W Lock Decouple Register Address.

Decouple Register 9 DW0

DECOUPREG9DW0 - Decouple Register 9 DW0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00F48h-00F4Bh	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg9DW0Data** Access: R/W Decouple Register 9 DW0 Data.

Decouple Register 9 DW1

DECOUPREG9DW1 - Decouple Register 9 DW1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00F4Ch-00F4Fh	
DWord	**Bit**	**Description**
0	31	**GO** Access: R/W Lock Decouple Register Go/Status Bit: Software sets this bit along with attributes (full DW write) to initiate a DCR request. Hardware clears this bit to 0 when the command is complete. This bit serves as a lock for the register pair preventing software from updating the status/values once set.
	30:28	**OP** Access: R/W Lock Decouple Register Opcode: 3'b000 = Read, 3'b001 = Write; All others undefined (Request ignored and go/status cleared).
	27:24	**BE_B** Access: R/W Lock Decouple Register Active Low Byte Enables. Byte enables affect data merging into MGSR shadow storage however GT only supports full dword accesses.
	23:0	**Addr** Access: R/W Lock Decouple Register Address.

Decouple Register 10 DW0

DECOUPREG10DW0 - Decouple Register 10 DW0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00F50h-00F53h	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg10DW0Data** Access: R/W Decouple Register 10 DW0 Data.

Decouple Register 10 DW1

DECOUPREG10DW1 - Decouple Register 10 DW1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00F54h-00F57h	
DWord	**Bit**	**Description**
0	31	**GO** Access: R/W Lock Decouple Register Go/Status Bit: Software sets this bit along with attributes (full DW write) to initiate a DCR request. Hardware clears this bit to 0 when the command is complete. This bit serves as a lock for the register pair preventing software from updating the status/values once set.
	30:28	**OP** Access: R/W Lock Decouple Register Opcode: 3'b000 = Read, 3'b001 = Write; All others undefined (Request ignored and go/status cleared).
	27:24	**BE_B** Access: R/W Lock Decouple Register Active Low Byte Enables. Byte enables affect data merging into MGSR shadow storage however GT only supports full dword accesses.
	23:0	**Addr** Access: R/W Lock Decouple Register Address.

Decouple Register 11 DW0

DECOUPREG11DW0 - Decouple Register 11 DW0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00F58h-00F5Bh	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg11DW0Data** Access: R/W Decouple Register 11 DW0 Data.

Decouple Register 11 DW1

DECOUPREG11DW1 - Decouple Register 11 DW1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00F5Ch-00F5Fh	
DWord	**Bit**	**Description**
0	31	**GO** Access: R/W Lock Decouple Register Go/Status Bit: Software sets this bit along with attributes (full DW write) to initiate a DCR request. Hardware clears this bit to 0 when the command is complete. This bit serves as a lock for the register pair preventing software from updating the status/values once set.
	30:28	**OP** Access: R/W Lock Decouple Register Opcode: 3'b000 = Read, 3'b001 = Write; All others undefined (Request ignored and go/status cleared).
	27:24	**BE_B** Access: R/W Lock Decouple Register Active Low Byte Enables. Byte enables affect data merging into MGSR shadow storage however GT only supports full dword accesses.
	23:0	**Addr** Access: R/W Lock Decouple Register Address.

Decouple Register 12 DW0

DECOUPREG12DW0 - Decouple Register 12 DW0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00F60h-00F63h	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg12DW0Data** Access: R/W Decouple Register 12 DW0 Data.

Decouple Register 12 DW1

DECOUPREG12DW1 - Decouple Register 12 DW1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00F64h-00F67h	
DWord	**Bit**	**Description**
0	31	**GO** Access: R/W Lock Decouple Register Go/Status Bit: Software sets this bit along with attributes (full DW write) to initiate a DCR request. Hardware clears this bit to 0 when the command is complete. This bit serves as a lock for the register pair preventing software from updating the status/values once set.
	30:28	**OP** Access: R/W Lock Decouple Register Opcode: 3'b000 = Read, 3'b001 = Write; All others undefined (Request ignored and go/status cleared).
	27:24	**BE_B** Access: R/W Lock Decouple Register Active Low Byte Enables. Byte enables affect data merging into MGSR shadow storage however GT only supports full dword accesses.
	23:0	**Addr** Access: R/W Lock Decouple Register Address.

Decouple Register 13 DW0

DECOUPREG13DW0 - Decouple Register 13 DW0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00F68h-00F6Bh	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg13DW0Data** Access: R/W Decouple Register 13 DW0 Data.

Decouple Register 13 DW1

DECOUPREG13DW1 - Decouple Register 13 DW1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00F6Ch-00F6Fh	
DWord	**Bit**	**Description**
0	31	**GO** Access: R/W Lock Decouple Register Go/Status Bit: Software sets this bit along with attributes (full DW write) to initiate a DCR request. Hardware clears this bit to 0 when the command is complete. This bit serves as a lock for the register pair preventing software from updating the status/values once set.
	30:28	**OP** Access: R/W Lock Decouple Register Opcode: 3'b000 = Read, 3'b001 = Write; All others undefined (Request ignored and go/status cleared).
	27:24	**BE_B** Access: R/W Lock Decouple Register Active Low Byte Enables. Byte enables affect data merging into MGSR shadow storage however GT only supports full dword accesses.
	23:0	**Addr** Access: R/W Lock Decouple Register Address.

Decouple Register 14 DW0

DECOUPREG14DW0 - Decouple Register 14 DW0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00F70h-00F73h	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg14DW0Data** Access: R/W Decouple Register 14 DW0 Data.

Decouple Register 14 DW1

DECOUPREG14DW1 - Decouple Register 14 DW1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00F74h-00F77h	
DWord	**Bit**	**Description**
0	31	**GO** Access: R/W Lock Decouple Register Go/Status Bit: Software sets this bit along with attributes (full DW write) to initiate a DCR request. Hardware clears this bit to 0 when the command is complete. This bit serves as a lock for the register pair preventing software from updating the status/values once set.
	30:28	**OP** Access: R/W Lock Decouple Register Opcode: 3'b000 = Read, 3'b001 = Write; All others undefined (Request ignored and go/status cleared).
	27:24	**BE_B** Access: R/W Lock Decouple Register Active Low Byte Enables. Byte enables affect data merging into MGSR shadow storage however GT only supports full dword accesses.
	23:0	**Addr** Access: R/W Lock Decouple Register Address.

Decouple Register 15 DW0

DECOUPREG15DW0 - Decouple Register 15 DW0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00F78h-00F7Bh	
DWord	**Bit**	**Description**
0	31:0	**DecoupReg15DW0Data** Access: R/W Decouple Register 15 DW0 Data.

Decouple Register 15 DW1

DECOUPREG15DW1 - Decouple Register 15 DW1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00F7Ch-00F7Fh	
DWord	**Bit**	**Description**
0	31	**GO** Access: R/W Lock Decouple Register Go/Status Bit: Software sets this bit along with attributes (full DW write) to initiate a DCR request. Hardware clears this bit to 0 when the command is complete. This bit serves as a lock for the register pair preventing software from updating the status/values once set.
	30:28	**OP** Access: R/W Lock Decouple Register Opcode: 3'b000 = Read, 3'b001 = Write; All others undefined (Request ignored and go/status cleared).
	27:24	**BE_B** Access: R/W Lock Decouple Register Active Low Byte Enables. Byte enables affect data merging into MGSR shadow storage however GT only supports full dword accesses.
	23:0	**Addr** Access: R/W Lock Decouple Register Address.

DE HPD Interrupt Definition

DE HPD Interrupt Definition	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	44470h-4447Fh
Name:	Display Engine HPD Interrupts
ShortName:	DE_HPD_INTERRUPT
Power:	PG0
Reset:	soft

This table indicates which events are mapped to each bit of the Display Engine HPD Interrupt registers.
0x44470 = ISR
0x44474 = IMR
0x44478 = IIR
0x4447C = IER

DWord	Bit	Description
0	31	**Unused 31**
	30	**Unused 30**
	29	**Unused 29**
	28	**Unused 28**
	27	**Unused 27**
	26	**Unused 26**
	25	**Unused 25**
	24	**Unused 24**
	23	**TC8 Hotplug** The ISR gives the live state of the HPD for typeC DP alternate mode. The IIR is set if a short or long pulse is detected when HPD input is enabled.
	22	**TC7 Hotplug** The ISR gives the live state of the HPD for typeC DP alternate mode. The IIR is set if a short or long pulse is detected when HPD input is enabled.
	21	**TC6 Hotplug** The ISR gives the live state of the HPD for typeC DP alternate mode. The IIR is set if a short or long pulse is detected when HPD input is enabled.
	20	**TC5 Hotplug** The ISR gives the live state of the HPD for typeC DP alternate mode. The IIR is set if a short or long pulse is detected when HPD input is enabled.
	19	**TC4 Hotplug**

DE HPD Interrupt Definition		
		The ISR gives the live state of the HPD for typeC DP alternate mode. The IIR is set if a short or long pulse is detected when HPD input is enabled.
	18	**TC3 Hotplug** The ISR gives the live state of the HPD for typeC DP alternate mode. The IIR is set if a short or long pulse is detected when HPD input is enabled.
	17	**TC2 Hotplug** The ISR gives the live state of the HPD for typeC DP alternate mode. The IIR is set if a short or long pulse is detected when HPD input is enabled.
	16	**TC1 Hotplug** The ISR gives the live state of the HPD for typeC DP alternate mode. The IIR is set if a short or long pulse is detected when HPD input is enabled.
	15	**Unused 15**
	14	**Unused 14**
	13	**Unused 13**
	12	**Unused 12**
	11	**Unused 11**
	10	**Unused 10**
	9	**Unused 9**
	8	**Unused 8**
	7	**TBT8 Hotplug** The ISR gives the live state of the HPD for thunderbolt. The IIR is set if a short or long pulse is detected when HPD input is enabled.
	6	**TBT7 Hotplug** The ISR gives the live state of the HPD for thunderbolt. The IIR is set if a short or long pulse is detected when HPD input is enabled.
	5	**TBT6 Hotplug** The ISR gives the live state of the HPD for thunderbolt. The IIR is set if a short or long pulse is detected when HPD input is enabled.
	4	**TBT5 Hotplug** The ISR gives the live state of the HPD for thunderbolt. The IIR is set if a short or long pulse is detected when HPD input is enabled.
	3	**TBT4 Hotplug** The ISR gives the live state of the HPD for thunderbolt. The IIR is set if a short or long pulse is detected when HPD input is enabled.
	2	**TBT3 Hotplug** The ISR gives the live state of the HPD for thunderbolt. The IIR is set if a short or long pulse is detected when HPD input is enabled.
	1	**TBT2 Hotplug** The ISR gives the live state of the HPD for thunderbolt. The IIR is set if a short or long pulse is detected when HPD input is enabled.

DE HPD Interrupt Definition		
	0	**TBT1 Hotplug** The ISR gives the live state of the HPD for thunderbolt. The IIR is set if a short or long pulse is detected when HPD input is enabled.

DE Misc Interrupt Definition

DE Misc Interrupt Definition

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	44460h-4446Fh
Name:	Display Engine Miscellaneous Interrupts
ShortName:	DE_MISC_INTERRUPT
Power:	PG0
Reset:	soft

This table indicates which events are mapped to each bit of the Display Engine Miscellaneous Interrupt registers.
0x44460 = ISR
0x44464 = IMR
0x44468 = IIR
0x4446C = IER

DWord	Bit	Description
0	31	**Poison** The ISR is an active high pulse on receiving the poison response to a memory transaction.
	30	**ECC_Double_Error** The ISR is an active high level while any of the ECC Double Error status bits are set.
	29:27	**Reserved** Format: MBZ
	26	**Reserved** Format: MBZ
	25	**Reserved**
	24	**Reserved**
	23	**WD0_Interrupts_Combined** The ISR is an active high level while any of the WD0_IIR bits are set.
	22:20	**Reserved** Format: MBZ

DE Misc Interrupt Definition

	19	**SRD_Interrupts_Combined** The ISR is an active high level while any of the SRD_IIR bits are set.
	18	**WD1_Interrupts_Combined** The ISR is an active high level while any of the WD1_IIR bits are set.
	17:16	**Reserved** Format: MBZ
	15	**GTC_Interrupts_Combined** The ISR is an active high level while any of the GTC_IIR bits are set.
	14:9	**Reserved** Format: MBZ
	8	**Reserved** Format: MBZ
	7	**Reserved**
	6	**Reserved**
	5	**Reserved**
	4	**Reserved**
	3:1	**Reserved** Format: MBZ
	0	**Reserved** Format: MBZ

DE Port Interrupt Definition

DE Port Interrupt Definition	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	44440h-4444Fh
Name:	Display Engine Port Interrupts
ShortName:	DE_PORT_INTERRUPT
Power:	PG0
Reset:	soft

This table indicates which events are mapped to each bit of the Display Engine Port Interrupt registers.
0x44440 = ISR
0x44444 = IMR
0x44448 = IIR
0x4444C = IER

DWord	Bit	Description
0	31	**DSI1** The ISR is an active high level indicating an interrupt is set in DSI_INTER_IDENT_REG_1.
	30	**DSI0** The ISR is an active high level indicating an interrupt is set in DSI_INTER_IDENT_REG_0.
	29	**AUX Channel E** The ISR is an active high pulse on the AUX DDI E done event. This event will not occur for SRD AUX done.
	28	**AUX Channel F** The ISR is an active high pulse on the AUX DDI F done event. This event will not occur for SRD AUX done.
	27	**AUX Channel D**

DE Port Interrupt Definition		
		The ISR is an active high pulse on the AUX DDI D done event. This event will not occur for SRD AUX done.
	26	**AUX Channel C** The ISR is an active high pulse on the AUX DDI C done event. This event will not occur for SRD AUX done.
	25	**AUX Channel B** The ISR is an active high pulse on the AUX DDI B done event. This event will not occur for SRD AUX done.
	24	**DSI1 TE** The ISR is an active high level indicating a TE interrupt is set in DSI_INTER_IDENT_REG_1.
	23	**DSI0 TE** The ISR is an active high level indicating a TE interrupt is set in DSI_INTER_IDENT_REG_0.
	22:12	**Reserved**
	11:10	**Reserved**
	9:8	**Reserved**
	7:6	**Reserved**
	5:3	**Reserved**
	2	**Reserved**
	1	**GMbus** The ISR is an active high pulse when any of the unmasked events in GMBUS4 Interrupt Mask register occur. This field is only used on projects that have GMBUS integrated into the north display. Projects that have GMBUS in the south display have the GMBUS interrupt in the south display interrupts.

DE Port Interrupt Definition		
	0	**AUX_Channel_A** The ISR is an active high pulse on the AUX DDI A done event. This event will not occur for SRD AUX done.

Device 0 Capabilities A

CAPID0_A_0_0_0_PCI - Device 0 Capabilities A

Register Space:	PCI: 0/0/0
Source:	BSpec
Size (in bits):	32
Address:	000E4h

DWord	Bit	Description
0	31	**Display HD Audio Disable** Default Value: 0b Access: R/W Unused - Bit field not relevant for the current project
	30	**PEG12 Disable** Default Value: 0b Access: R/W Unused - Bit field not relevant for the current project
	29	**PEG11 Disable** Default Value: 0b Access: R/W Unused - Bit field not relevant for the current project
	28	**PEG10 Disable** Default Value: 0b Access: R/W Unused - Bit field not relevant for the current project
	27	**PCI Express Link Width Upconfig Disable** Default Value: 0b Access: R/W Unused - Bit field not relevant for the current project

CAPID0_A_0_0_0_PCI - Device 0 Capabilities A

26	**DMI Width** Default Value: 0b Access: R/W Unused - Bit field not relevant for the current project
25	**ECC Disable** Default Value: 0b Access: R/W Unused - Bit field not relevant for the current project
24	**Force DRAM ECC Enabled** Default Value: 0b Access: R/W Unused - Bit field not relevant for the current project
23	**VTd Disable** Default Value: 0b Access: R/W 0: Enable VTd 1: Disable VTd
22	**DMI Gen 2 Disable** Default Value: 0b Access: R/W Unused - Bit field not relevant for the current project
21	**PEG Gen 2 Disable** Default Value: 0b Access: R/W Unused - Bit field not relevant for the current project
20:19	**DDR Size**

CAPID0_A_0_0_0_PCI - Device 0 Capabilities A

	Default Value:	00b
	Access:	R/W

Unused - Bit field not relevant for the current project

18 **Bclk overclocking disable**

Default Value:	0b
Access:	R/W

Unused - Bit field not relevant for the current project

17 **Disable 1N Mode**

Default Value:	0b
Access:	R/W

Unused - Bit field not relevant for the current project

16 **Full ULT Fuse Read Disable**

Default Value:	0b
Access:	R/W

Unused - Bit field not relevant for the current project

15 **Camarillo Device Disable**

Default Value:	0b
Access:	R/W

0: DPTF (Camarillo) associated memory spaces are accessible.
1: DPTF (Camarillo) associated memory and IO spaces are disabled. DEVEN_0_0_0_PCI field for DPTF can not be set.

14 **2 DIMMS per Channel Disable**

Default Value:	0b
Access:	R/W

Unused - Bit field not relevant for the current project

13 **X2APIC Enabled**

CAPID0_A_0_0_0_PCI - Device 0 Capabilities A

	Default Value:	0b
	Access:	R/W

Unused - Bit field not relevant for the current project

12 **Performance Dual Channel Disable**

Default Value:	0b
Access:	R/W

Unused - Bit field not relevant for the current project

11 **Internal Graphics Disable**

Default Value:	0b
Access:	R/W

0b: There is a graphics engine within this CPU. Internal Graphics Device (Device 2) is enabled and all of its memory and I/O spaces are accessible. Configuration cycles to Device 2 will be completed within the CPU. All non-SMM memory and IO accesses to VGA will be handled based on Memory and IO enables of Device 2 and IO registers within Device 2 and VGA Enable of the PCI to PCI bridge control (If PCI Express GFX attach is supported). A selected amount of Graphics Memory space is pre-allocated from the main memory based on Graphics Mode Select (GMS in the GGC Register). Graphics Memory is pre-allocated above TSEG Memory. 1b: There is no graphics engine within this CPU. Internal Graphics Device (Device 2) and all of its memory and I/O functions are disabled. Configuration cycle targeted to Device 2 will be passed on. All non-SMM memory and IO accesses to VGA will be handled based on VGA Enable of the PCI to PCI bridge control. Device 2 is disabled and hidden.

10 **Reserved**

9:8 **Capability Device ID**

Default Value:	00b
Access:	R/W

7:4 **Compatibility Rev ID**

Default Value:	0000b
Access:	R/W

Unused - Bit field not relevant for the current project

CAPID0_A_0_0_0_PCI - Device 0 Capabilities A

	3	**DDR Overclocking** Default Value: 0b Access: R/W Unused - Bit field not relevant for the current project
	2	**IA Overclocking Enabled by DSKU** Default Value: 0b Access: R/W Unused - Bit field not relevant for the current project
	1	**DDR Write VRef Enable** Default Value: 0b Access: R/W Unused - Bit field not relevant for the current project
	0	**DDR3L Enable** Default Value: 0b Access: R/W Unused - Bit field not relevant for the current project

Device 0 Capabilities B

CAPID0_B_0_0_0_PCI - Device 0 Capabilities B

Register Space:	PCI: 0/0/0
Source:	BSpec
Size (in bits):	32
Address:	000E8h

DWord	Bit	Description
0	31	**Reserved_31** Default Value: 0b Access: R/W Unused - Bit field not relevant for the current project
	30	**IA Overclocking DSKU Control Disable** Default Value: 0b Access: R/W Unused - Bit field not relevant for the current project
	29	**IA Overclocking Enable** Default Value: 0b Access: R/W Unused - Bit field not relevant for the current project
	28	**SMT Capability** Default Value: 0b Access: R/W Unused - Bit field not relevant for the current project
	27:25	**Cache Size Capability** Default Value: 000b Access: R/W Unused - Bit field not relevant for the current project

CAPID0_B_0_0_0_PCI - Device 0 Capabilities B

24	**SVMDIS** Access: R/W 0b: SVM mode enabled **[Default]** 1b: SVM mode disabled
23:21	**DDR3 Maximum Frequency Capability with 100 Memory** Access: R/W Unused - Bit field not relevant for the current project
20	**Gen3 Disable Fuse for PCIe PEG Controllers** Default Value: 0b Access: R/W Unused - Bit field not relevant for the current project
19	**Package Type** Default Value: 0b Access: R/W Unused - Bit field not relevant for the current project
18	**Additive Graphics Enabled** Default Value: 0b Access: R/W Unused - Bit field not relevant for the current project
17	**Additive Graphics Capable** Default Value: 0b Access: R/W Unused - Bit field not relevant for the current project
16	**Primary PEG Port x16 Disable**

CAPID0_B_0_0_0_PCI - Device 0 Capabilities B

		Default Value: 0b Access: R/W Unused - Bit field not relevant for the current project
	15:12	**Reserved_15_12** Default Value: 0000b Access: R/W Unused - Bit field not relevant for the current project
	11	**Reserved**
	10:8	**Reserved_10_8** Default Value: 000b Access: R/W Unused - Bit field not relevant for the current project
	7	**Reserved**
	6:4	**DDR3 Maximum Frequency Capability** Default Value: 000b Access: R/W Unused - Bit field not relevant for the current project
	3	**Reserved_3** Default Value: 0b Access: R/W Unused - Bit field not relevant for the current project
	2	**DDR4 DSKU Enable** Default Value: 0b Access: R/W

<table>
<tr><th colspan="3">CAPID0_B_0_0_0_PCI - Device 0 Capabilities B</th></tr>
<tr><td></td><td></td><td>Unused - Bit field not relevant for the current project</td></tr>
<tr><td></td><td>1</td><td>Dual PEG Force x1 when VGA Enabled<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td></td><td></td></tr><tr><td>Access:</td><td>R/W</td></tr></table>Unused - Bit field not relevant for the current project</td></tr>
<tr><td></td><td>0</td><td>Single PEG Force x1 when VGA Enabled<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td></td><td></td></tr><tr><td>Access:</td><td>R/W</td></tr></table>Unused - Bit field not relevant for the current project</td></tr>
</table>

DFSDONE

DFSDONE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	51080h-51083h
Name:	Display Fuse Done
ShortName:	DFSDONE
Power:	PG0
Reset:	global

This register is not reset by FLR.

DWord	Bit	Description
0	31:1	**Reserved** Format: MBZ
	0	**Download Done** This field indicates when fuse download is complete. 0b: Note Done 1b: Done

DFSM

DFSM

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	51000h-51003h
Name:	Display Fuse
ShortName:	DFSM
Power:	PG0
Reset:	global

This register contains fuse and strap settings for display. This register is not reset by FLR.

DWord	Bit	Description
0	31	**Reserved**
	30	**Display PipeA Disable** This bit indicates whether the display pipe A (first pipe) capability is disabled. Value: 0b – Name: Enable – Description: Pipe A Capability Enabled Value: 1b – Name: Disable – Description: Pipe A Capability Disabled
	29	**Reserved**
	28	**Display PipeC Disable** This bit indicates whether the display pipe C (third pipe) capability is disabled. Value: 0b – Name: Enable – Description: Pipe C Capability Enabled Value: 1b – Name: Disable – Description: Pipe C Capability Disabled
	27	**Display PM Disable** This bit indicates whether the display power management FBC and DPST capabilities are disabled. Value: 0b – Name: Enable – Description: PM Capability Enabled Value: 1b – Name: Disable – Description: PM Capability Disabled
	26	**Display eDP Disable** Description: This bit indicates whether the display embedded DisplayPort eDP DDIA capability is disabled.

Value	Name	Description
0b	Enable	eDP Capability Enabled
1b	Disable	eDP Capability Disabled

25 **Reserved**

24 **Reserved**

23 **Reserved**

22 **Display PipeD Disable**

This bit indicates whether the display pipe D (fourth pipe) capability is disabled.

Value	Name
0b	Enable
1b	Disable

21 **Display PipeB Disable**

This bit indicates whether the display pipe B (second pipe) capability is disabled.

Value	Name
0b	Pipe B Capability Enabled
1b	Pipe B Capability Disabled

20 **Display WD Disable**

This bit indicates whether the display WD capability is disabled.

Value	Name	Description
0b	Enable	WD Capability Enabled
1b	Disable	WD Capability Disabled

19 **Reserved**

18 **Reserved**

17 **Spare 17**

16 **Isolated Decode Disable**

This field indicates whether the Isolated Decode feature is disabled.

Value	Name

	0b	Isolated Decode Capability Enabled
	1b	Isolated Decode Capability Disabled

15:8 **Audio Codec ID**

This field indicates the lower 8 bits of the audio codec device ID. See the root node F00 verb for the device IDs on each project.

Value	Name	Description
0Bh	Audio Codec ID 280Bh **[Default]**	Default value is N/A. Fuse download will override with correct value for this project.

7 **Display DSC Disable**

This field indicates whether the DSC (port Display Stream Compression) feature is disabled.

Value	Name
0b	DSC Capability Enabled
1b	DSC Capability Disabled

6 **Display RSB Enable**

This bit indicates whether the remote screen blanking feature is enabled in the display engine.

Value	Name	Description
0b	Disable	RSB Capability Disabled
1b	Enable	RSB Capability Enabled

5 **Reserved**

4 **Reserved**

3 **Reserved**

2 **Reserved**

1 **Reserved**

0 **Display Audio Codec Disable**

This bit indicates whether the display audio codec capability is disabled.

Value	Name	Description
0b	Enable	Audio Codec Capability Enabled
1b	Disable	Audio Codec Capability Disabled

Discard Enables for Z streams

Z_DISCARD_EN - Discard Enables for Z streams

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	07040h
ShortName:	Z_DISCARD_EN

Under Posh Based Tiled Rendering (aka PTBR), at the end of tile, certain streams can be discarded from the on-chip caches i.e. without evicting to memory. SW programs LOAD_REG_MEMORY command in the RCS command buffer to program this register. HW uses this value live from the register
This register defines the discard bits for Z streams.
Setting the discard enable bit for a stream, allows HW to drop writing back dirty cachelines from on-chip caches to memory.

Programming Notes

This register value must not change during the render pass (aka tile pass).

DWord	Bit	Description
0	31:2	**Reserved** Default Value: 000000000000000b Access: R/W
	1	**STC Discard Enable** When this bit is set, Stencil (STC) stream can be discarded at the end of tile in the PTBR mode. 0 – Disable **[Default]** 1 – Enable
	0	**Z Discard Enable** Access: R/W When this bit is set, all Z streams i.e. HiZ and Z can be discarded at the end of tile in the PTBR mode. 0 – Disable **[Default]** 1 – Enable

DISPLAY_INT_CTL

DISPLAY_INT_CTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W, RO
Size (in bits):	32
Address:	44200h-44203h
Name:	Display Interrupt Control
ShortName:	DISPLAY_INT_CTL
Power:	PG0
Reset:	soft

This register has the master enable for display interrupts and gives an overview of what interrupts are pending.
An interrupt pending bit will read 1b while one or more interrupts of that category are set (IIR) and enabled (IER).
All Pending Interrupts are ORed together to generate the combined interrupt.
The combined interrupt is ANDed with the Display Interrupt enable to create the display enabled interrupt.
The display enabled interrupt goes to graphics interrupt processing.
The master interrupt enable must be set before any of these interrupts will propagate to graphics interrupt processing.

DWord	Bit	Description
0	31	**Display Interrupt Enable** Access: R/W This is the master control for display interrupts. This must be enabled for any of these interrupts to propagate to graphics interrupt processing. Value: 0b — Name: Disable Value: 1b — Name: Enable
	30:25	**Reserved**
	24	**Audio Codec Interrupts Pending** Access: RO This field indicates if interrupts of this category are pending.
	23	**DE PCH Interrupts Pending** Access: RO This field indicates if interrupts of this category are pending. The PCH Display interrupt is configured through the SDE interrupt registers.
	22	**DE Misc Interrupts Pending**

DISPLAY_INT_CTL		
		Access: RO This field indicates if interrupts of this category are pending.
	21	**DE HPD Interrupts Pending** Access: RO This field indicates if interrupts of this category are pending.
	20	**DE Port Interrupts Pending** Access: RO This field indicates if interrupts of this category are pending.
	19	**DE Pipe D Interrupts Pending** Access: RO This field indicates if interrupts of this category are pending.
	18	**DE Pipe C Interrupts Pending** Access: RO This field indicates if interrupts of this category are pending.
	17	**DE Pipe B Interrupts Pending** Access: RO This field indicates if interrupts of this category are pending.
	16	**DE Pipe A Interrupts Pending** Access: RO This field indicates if interrupts of this category are pending.
	15:0	**Reserved**

Display CSR Program

Display CSR Program	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	196608
Address:	80000h-85FFFh
Name:	Display CSR Program
Power:	PG0
Reset:	global

This address range is used to store the display context save and restore program.

DWord	Bit	Description
0..6143	196607:0	**Program**

DISPLAY FUNCTION ID

DISPLAY_FUNCID - DISPLAY FUNCTION ID

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	10108Ch

This register is used to identify which Virtual function, if any, is allowed to access or configure Display-related HW.

DWord	Bit	Description
0	31:8	**Reserved** Default Value: 000000h Access: RO Reserved
	7:0	**DISPLAY FUNCTION** Default Value: 00000000b Access: R/W 0 : Display HW is accessible by the Physical function only. 1-N : Display HW is accessible by the specified Virtual Function, in addition to the Physical function.

Display Message Forward Status Register

DISPLAY_MESSAGE_FORWARD_STATUS - Display Message Forward Status Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	022E8h-022EBh
Name:	Display Message Forward Status Register
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_RCSUNIT
Address:	182E8h-182EBh
Name:	Display Message Forward Status Register
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_POCSUNIT
Address:	222E8h-222EBh
Name:	Display Message Forward Status Register
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_BCSUNIT
Address:	1C02E8h-1C02EBh
Name:	Display Message Forward Status Register
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_VCSUNIT0
Address:	1C42E8h-1C42EBh
Name:	Display Message Forward Status Register
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_VCSUNIT1
Address:	1C82E8h-1C82EBh
Name:	Display Message Forward Status Register
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_VECSUNIT0
Address:	1D02E8h-1D02EBh
Name:	Display Message Forward Status Register
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_VCSUNIT2

DISPLAY_MESSAGE_FORWARD_STATUS - Display Message Forward Status Register

Address:	1D42E8h-1D42EBh
Name:	Display Message Forward Status Register
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_VCSUNIT3
Address:	1D82E8h-1D82EBh
Name:	Display Message Forward Status Register
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_VECSUNIT1
Address:	1E02E8h-1E02EBh
Name:	Display Message Forward Status Register
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_VCSUNIT4
Address:	1E42E8h-1E42EBh
Name:	Display Message Forward Status Register
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_VCSUNIT5
Address:	1E82E8h-1E82EBh
Name:	Display Message Forward Status Register
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_VECSUNIT2
Address:	1F02E8h-1F02EBh
Name:	Display Message Forward Status Register
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_VCSUNIT6
Address:	1F42E8h-1F42EBh
Name:	Display Message Forward Status Register
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_VCSUNIT7
Address:	1F82E8h-1F82EBh
Name:	Display Message Forward Status Register
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_VECSUNIT3

This register stores the internal HW status flags related to display message forward logic. This register should

DISPLAY_MESSAGE_FORWARD_STATUS - Display Message Forward Status Register

not be accessed by SW. This register is part of power context image. Note: Even though this register exists in VideoCS and VideoEnhancementCS, individual bit driven functionality is not supported.

Programming Notes	Source
This register functionality is not supported and must not be programmed for Position command streamer.	PositionCS

DWord	Bit	Description
0	31:30	**Reserved** Source: RenderCS, BlitterCS Format: MBZ
	29:28	**Reserved**
	27:26	**Reserved**
	25:24	**Reserved**
	23:22	**Reserved**
	21:20	**Reserved**
	19:18	**Reserved**
	17:16	**Reserved**
	15:14	**Reserved**
	13:12	**Reserved**
	11:10	**Reserved**
	9:8	**Reserved**
	7:6	**Reserved**
	5:4	**Reserved**
	3:2	**Reserved**
	1:0	**Reserved**

Display Message Forward Status Register 2

DISPLAY_MESSAGE_FORWARD_STATUS_2 - Display Message Forward Status Register 2	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02188h-0218Bh
Name:	DISPLAY_MESSAGE_FORWARD_STATUS_2
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_2_RCSUNIT
Address:	18188h-1818Bh
Name:	DISPLAY_MESSAGE_FORWARD_STATUS_2
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_2_POCSUNIT
Address:	22188h-2218Bh
Name:	DISPLAY_MESSAGE_FORWARD_STATUS_2
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_2_BCSUNIT
Address:	1C0188h-1C018Bh
Name:	DISPLAY_MESSAGE_FORWARD_STATUS_2
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_2_VCSUNIT0
Address:	1C4188h-1C418Bh
Name:	DISPLAY_MESSAGE_FORWARD_STATUS_2
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_2_VCSUNIT1
Address:	1C8188h-1C818Bh
Name:	DISPLAY_MESSAGE_FORWARD_STATUS_2
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_2_VECSUNIT0
Address:	1D0188h-1D018Bh
Name:	DISPLAY_MESSAGE_FORWARD_STATUS_2
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_2_VCSUNIT2

DISPLAY_MESSAGE_FORWARD_STATUS_2 - Display Message Forward Status Register 2

Address:	1D4188h-1D418Bh
Name:	DISPLAY_MESSAGE_FORWARD_STATUS_2
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_2_VCSUNIT3
Address:	1D8188h-1D818Bh
Name:	DISPLAY_MESSAGE_FORWARD_STATUS_2
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_2_VECSUNIT1
Address:	1E0188h-1E018Bh
Name:	DISPLAY_MESSAGE_FORWARD_STATUS_2
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_2_VCSUNIT4
Address:	1E4188h-1E418Bh
Name:	DISPLAY_MESSAGE_FORWARD_STATUS_2
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_2_VCSUNIT5
Address:	1E8188h-1E818Bh
Name:	DISPLAY_MESSAGE_FORWARD_STATUS_2
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_2_VECSUNIT2
Address:	1F0188h-1F018Bh
Name:	DISPLAY_MESSAGE_FORWARD_STATUS_2
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_2_VCSUNIT6
Address:	1F4188h-1F418Bh
Name:	DISPLAY_MESSAGE_FORWARD_STATUS_2
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_2_VCSUNIT7
Address:	1F8188h-1F818Bh
Name:	DISPLAY_MESSAGE_FORWARD_STATUS_2
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_2_VECSUNIT3

This register stores the internal HW status flags related to display message forward logic. This register should

DISPLAY_MESSAGE_FORWARD_STATUS_2 - Display Message Forward Status Register 2

not be accessed by SW. This register is part of power context image. Note: Even though this register exists in VideoCS and VideoEnhancementCS, individual bit driven functionality is not supported.

DWord	Bit	Description
0	31:30	**Reserved**
	29:28	**Reserved**
	27:26	**Reserved**
	25:24	**Reserved**
	23:22	**Reserved**
	21:20	**Reserved**
	19:18	**Reserved**
	17:16	**Reserved**
	15:14	**Reserved**
	13:12	**Reserved**
	11:10	**Reserved**
	9:8	**Reserved**
	7:6	**Reserved**
	5:4	**Reserved**
	3:2	**Reserved**
	1:0	**Reserved**

Display Message Forward Status Register 3

DISPLAY_MESSAGE_FORWARD_STATUS_3 - Display Message Forward Status Register 3	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0218Ch-0218Fh
Name:	DISPLAY_MESSAGE_FORWARD_STATUS_3
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_3_RCSUNIT
Address:	1818Ch-1818Fh
Name:	DISPLAY_MESSAGE_FORWARD_STATUS_3
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_3_POCSUNIT
Address:	2218Ch-2218Fh
Name:	DISPLAY_MESSAGE_FORWARD_STATUS_3
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_3_BCSUNIT
Address:	1C018Ch-1C018Fh
Name:	DISPLAY_MESSAGE_FORWARD_STATUS_3
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_3_VCSUNIT0
Address:	1C418Ch-1C418Fh
Name:	DISPLAY_MESSAGE_FORWARD_STATUS_3
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_3_VCSUNIT1
Address:	1C818Ch-1C818Fh
Name:	DISPLAY_MESSAGE_FORWARD_STATUS_3
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_3_VECSUNIT0
Address:	1D018Ch-1D018Fh
Name:	DISPLAY_MESSAGE_FORWARD_STATUS_3
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_3_VCSUNIT2

DISPLAY_MESSAGE_FORWARD_STATUS_3 - Display Message Forward Status Register 3

Address:	1D418Ch-1D418Fh
Name:	DISPLAY_MESSAGE_FORWARD_STATUS_3
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_3_VCSUNIT3
Address:	1D818Ch-1D818Fh
Name:	DISPLAY_MESSAGE_FORWARD_STATUS_3
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_3_VECSUNIT1
Address:	1E018Ch-1E018Fh
Name:	DISPLAY_MESSAGE_FORWARD_STATUS_3
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_3_VCSUNIT4
Address:	1E418Ch-1E418Fh
Name:	DISPLAY_MESSAGE_FORWARD_STATUS_3
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_3_VCSUNIT5
Address:	1E818Ch-1E818Fh
Name:	DISPLAY_MESSAGE_FORWARD_STATUS_3
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_3_VECSUNIT2
Address:	1F018Ch-1F018Fh
Name:	DISPLAY_MESSAGE_FORWARD_STATUS_3
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_3_VCSUNIT6
Address:	1F418Ch-1F418Fh
Name:	DISPLAY_MESSAGE_FORWARD_STATUS_3
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_3_VCSUNIT7
Address:	1F818Ch-1F818Fh
Name:	DISPLAY_MESSAGE_FORWARD_STATUS_3
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_3_VECSUNIT3

This register stores the internal HW status flags related to display message forward logic. This register should

DISPLAY_MESSAGE_FORWARD_STATUS_3 - Display Message Forward Status Register 3

not be accessed by SW. This register is part of power context image. Note: Even though this register exists in VideoCS and VideoEnhancementCS, individual bit driven functionality is not supported.

DWord	Bit	Description
0	31:10	**Reserved** Format: PBC
	9:8	**Reserved**
	7:6	**Reserved**
	5:4	**Reserved**
	3:2	**Reserved**
	1:0	**Reserved**

DOUBLE_BUFFER_CTL

DOUBLE_BUFFER_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	44500h-44503h
Name:	Double Buffer Control
ShortName:	DOUBLE_BUFFER_CTL
Power:	PG0
Reset:	soft

This register together with the Allow Double Buffer Disable fields in the plane control registers allows for the double buffer update of registers in multiple resources to be synchronized together for an atomic update.

Programming Notes

Sequence for synchronizing the double buffer updates of multiple resources:
1. Set the Allow Double Buffer Update Disable field for each resource to be synchronized together and write the appropriate register to arm and trigger the update. Set the Global Double Buffer Update Disable field. The order in which these fields are set does not matter.
2. Program the registers that need to be synchronized together.
3. Clear the Global Double Buffer Update Disable field. Any pending updates will take place at the next periodic udate event.
4. If a resource no longer needs to be synchronized, clear the Allow Double Buffer Update Disable field for that resource and write the appropriate register to arm and trigger the update. If the resource will continue to be synchronized, the field can remain set and does not need to be set again when returning to step 1 of this sequence.

DWord	Bit	Description
0	31:1	**Reserved** Format: MBZ
	0	**Global Double Buffer Update Disable** This field controls whether the double buffer update is disabled for the resources which have allowed it to be disabled. This only disables the double buffer update for periodic events, like the start of vertical blank. It does not change the behavior for constant events, like pipe not enabled. This applies to MMIO register updates as well as command streamer initiated flips. When the double buffer update is disabled, the values written into the double buffered registers will not take effect at the periodic update event. After the double buffer update is no longer disabled, any pending updates will take place at the next periodic update event. Asynchronous flips initiated by MMIO or command streamers are not effected by disabling double

buffering.
Synchronous flips (regular and stereo 3D) initiated by MMIO or command streamers will not complete or give the flip done indication while double buffering is disabled for a plane. They will complete and give the flip done at the next start of vertical blank (selectable right or left eye vertical blank when using stereo 3D) after the double buffering is re-enabled.

Value	Name
0b	Not Disabled
1b	Disabled

DP_TP_CTL

DP_TP_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	64040h-64043h
Name:	DDI A DisplayPort Transport Control
ShortName:	DP_TP_CTL_A
Power:	PG1
Reset:	soft
Address:	64140h-64143h
Name:	DDI B DisplayPort Transport Control
ShortName:	DP_TP_CTL_B
Power:	PG2
Reset:	soft
Address:	64240h-64243h
Name:	DDI C DisplayPort Transport Control
ShortName:	DP_TP_CTL_C
Power:	PG2
Reset:	soft
Address:	64340h-64343h
Name:	DDI D DisplayPort Transport Control
ShortName:	DP_TP_CTL_D
Power:	PG2
Reset:	soft
Address:	64440h-64443h
Name:	DDI E DisplayPort Transport Control
ShortName:	DP_TP_CTL_E
Power:	PG2

DP_TP_CTL

Reset: soft

Address: 64540h-64543h
Name: DDI F DisplayPort Transport Control
ShortName: DP_TP_CTL_F

Power: PG2
Reset: soft

DWord	Bit	Description
0	31	**Transport Enable** This bit enables the DisplayPort transport function. Value: 0b = Disable; 1b = Enable
	30	**FEC Enable** Description: Forward Error Correction (FEC) coding for Display Ports (DP). The data M and data N must account for the FEC overhead when FEC is enabled. FEC can only be enabled after DP_TP_CTL isenabled. FEC can only be disabled after DP_TP_CTL is disabled. FEC is not supported on DDIA. FEC is not supported for DP - x1 and DP MST cases. Value: 0b = disable; 1b = enable
	29:28	**Reserved**
	27	**Transport Mode Select** Description: This bit selects between DisplayPort SST and MST modes of operation. This bit is ignored by DDI A (EDP) since it does not support multistreaming. Value: 0b = SST mode (DisplayPort SST mode); 1b = MST mode (DisplayPort MST mode)

DP_TP_CTL

Restriction
The DisplayPort mode (SST or MST) selected here must match the mode selected in the Transcoder DDI Function Control registers for the transcoders attached to this transport. This field must not be changed while the DDI function is enabled.

26 **Reserved**

Format:	MBZ

25 **Force ACT**

Description
This bit forces DisplayPort MST ACT to be sent one time at the next link frame boundary. After ACT is sent, as indicated in the ACT sent status bit, this bit can be cleared and set again to send ACT again.
This bit is ignored by DDI A (EDP) since it does not support multistreaming.

Value	Name	Description
0b	Do not force	Do not force ACT to be sent
1b	Force	Force ACT to be sent one time

24:21 **Reserved**

Format:	MBZ

20:19 **Training Pattern 4 Select**

Value	Name	Description
00b	Training Pattern 4a **[Default]**	**CP2520 Pattern 3**:SR-BS-BS-SR-248 00hs (after data symbol scrambling and ANSI8B/10B coding)
01b	Training Pattern 4b	**CP2520 Pattern 2**:SR-BF-BF-SR-248 00hs (after data symbol scrambling and ANSI8B/10B coding)
10b	Training Pattern 4c	**CP2520 Pattern 1**:SR-CP-CP-SR-248 of 00hs (after data symbol scrambling and ANSI8B/10B coding)
11b	Reserved	

18 **Enhanced Framing Enable**

Description
This bit selects enhanced framing for DisplayPort SST.
Hardware internally enables enhanced framing for DisplayPort MST.

Value	Name
0b	Disabled
1b	Enabled

DP_TP_CTL

		Restriction In DisplayPort MST mode this bit must be set to Disabled. This field must not be changed while the DDI function is enabled.
	17:16	**Reserved** Format: MBZ
	15	**Reserved** Format: MBZ
	14:11	**Reserved** Format: MBZ
	10:8	**DP Link Training Enable** These bits are used for DisplayPort link initialization as defined in the DisplayPort specification. During training patterns, hardware will internally manage enabling and disabling of scrambling. Scrambling disable bit will be ignored at that time. DP_TP_STATUS has an indication that the required number of idle patterns has been sent.

Value	Name	Description
000b	Pattern 1	Training Pattern 1 enabled
001b	Pattern 2	Training Pattern 2 enabled
010b	Idle	Idle Pattern enabled
011b	Normal	Link not in training: Send normal pixels
100b	Pattern 3	Training Pattern 3 enabled
101b	Pattern 4	Training Pattern 4 enabled
Others	Reserved	Reserved

Restriction
When enabling or re-enabling the port, it must be turned on with pattern 1 enabled.

	7	**Reserved**
	6	**Alternate SR Enable** This bit enables the DisplayPort Alternate Scrambler Reset, intended for use only with embedded DisplayPort receivers.

Value	Name
0b	Disable
1b	Enable

Restriction
This field must not be changed while the DDI function is enabled.

	5:0	**Reserved**

DP_TP_CTL			
		Format:	MBZ

DP_TP_STATUS

DP_TP_STATUS	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	64144h-64147h
Name:	DDI B DisplayPort Transport Status
ShortName:	DP_TP_STATUS_B
Power:	PG2
Reset:	soft
Address:	64244h-64247h
Name:	DDI C DisplayPort Transport Status
ShortName:	DP_TP_STATUS_C
Power:	PG2
Reset:	soft
Address:	64344h-64347h
Name:	DDI D DisplayPort Transport Status
ShortName:	DP_TP_STATUS_D
Power:	PG2
Reset:	soft
Address:	64444h-64447h
Name:	DDI E DisplayPort Transport Status
ShortName:	DP_TP_STATUS_E
Power:	PG2
Reset:	soft
Address:	64544h-64547h
Name:	DDI F DisplayPort Transport Status
ShortName:	DP_TP_STATUS_F

DP_TP_STATUS

Power: PG2

Reset: soft

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28	**FEC enable live status** Access: RO This bit provides live status of FEC enable/disable in hardware.
	27	**Idle Link Frame Status** Access: R/WC This bit indicates if a link frame boundary has been sent in idle pattern. This is a sticky bit, cleared by writing 1b to it. 0b: Idle link frame not sent 1b: Idle link frame sent
	26	**Active Link Frame Status** Access: R/WC This bit indicates if a link frame boundary has been sent in active (at least one VC enabled). This is a sticky bit, cleared by writing 1b to it. 0b: Active link frame not sent 1b: Active link frame sent
	25	**Min Idles Sent** Access: RO This bit indicates that the minimum required number of idle patterns has been sent when DP_TP_CTL is set to send idle patterns. This bit will clear itself when DP_TP_CTL is not longer set to send idle patterns. 0b: Min idles not sent 1b: Min idles sent
	24	**ACT Sent Status** Access: R/WC This bit indicates if DisplayPort MST ACT has been sent. This is a sticky bit, cleared by writing 1b to it. Value / Name

DP_TP_STATUS

	0b	ACT not sent
	1b	ACT sent

23 Mode Status

Access:	RO

This bit indicates what mode the transport is currently in.

Value	Name	Description
0b	SST	Single-stream mode
1b	MST	Multi-stream mode

22:19 Reserved

Format:	MBZ

18 Reserved

Format:	MBZ

17:16 Streams Enabled

Access:	RO

This field indicates the number of streams (transcoders) enabled on this port during multistream operation. This field should be ignored in single stream mode.

Value	Name	Description
00b	Zero	Zero streams enabled
01b	One	One stream enabled
10b	Two	Two streams enabled
11b	Three	Three streams enabled

15:13 Reserved

Format:	MBZ

12 Reserved

Format:	MBZ

11:10 Reserved

Format:	MBZ

9:8 Payload Mapping VC2

Access:	RO

This field indicates which transcoder is mapped to Virtual Channel 2 during multistream operation. This field should be ignored if the number of streams enabled is less than three. This

DP_TP_STATUS

field should be ignored in single stream mode.

Value	Name	Description
00b	A	Transcoder A mapped to this VC
01b	B	Transcoder B mapped to this VC
10b	C	Transcoder C mapped to this VC

7:6 **Reserved**

Format:	MBZ

5:4 **Payload Mapping VC1**

Access:	RO

This field indicates which transcoder is mapped to Virtual Channel 1 during multistream operation. This field should be ignored if the number of streams enabled is less than two. This field should be ignored in single stream mode.

Value	Name	Description
00b	A	Transcoder A mapped to this VC
01b	B	Transcoder B mapped to this VC
10b	C	Transcoder C mapped to this VC

3:2 **Reserved**

Format:	MBZ

1:0 **Payload Mapping VC0**

Access:	RO

This field indicates which transcoder is mapped to Virtual Channel 0 during multistream operation. This field should be ignored if the number of streams enabled is less than one. This field should be ignored in single stream mode.

Value	Name	Description
00b	A	Transcoder A mapped to this VC
01b	B	Transcoder B mapped to this VC
10b	C	Transcoder C mapped to this VC

DPCLKA_CFGCR0

DPCLKA_CFGCR0	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	164280h-164283h
Name:	DPCLKA_CFGCR0
ShortName:	DPCLKA_CFGCR0
Power:	PG0
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31	**Reserved**
	30	**Reserved**
	29	**Reserved**
	28	**Reserved** Format: MBZ
	27	**Reserved**
	26	**Reserved**
	25	**Reserved**
	24	**DDIC Clock Off** This field gates off the clock going to the display engine. 0b: On

DPCLKA_CFGCR0

	1b	Off **[Default]**

23 TC6 Clock Off

This field gates off the clock going to the display engine.

Value	Name
0b	On
1b	Off **[Default]**

22 TC5 Clock Off

This field gates off the clock going to the display engine.

Value	Name
0b	On
1b	Off **[Default]**

21 TC4 Clock Off

This field gates off the clock going to the display engine.

Value	Name
0b	On
1b	Off **[Default]**

20 Reserved

19 Reserved

18 Reserved

17 Reserved

16 Reserved

15 Reserved

14 TC3 Clock Off

This field gates off the clock going to the display engine.

Value	Name
0b	On

DPCLKA_CFGCR0

	1b	Off **[Default]**

13 TC2 Clock Off

This field gates off the clock going to the display engine.

Value	Name
0b	On
1b	Off **[Default]**

12 TC1 Clock Off

This field gates off the clock going to the display engine.

Value	Name
0b	On
1b	Off **[Default]**

11 DDIB Clock Off

This field gates off the DDIB clock going to the display engine. DSI1 clock gating is independent and controlled by the MIPI DSI mode programming.

Value	Name
0b	On
1b	Off **[Default]**

10 DDIA Clock Off

This field gates off the DDIA clock going to the display engine. DSI0 clock gating is independent and controlled by the MIPI DSI mode programming.

Value	Name
0b	On
1b	Off **[Default]**

9:8 Reserved

7:6 Reserved

5:4 DDIC Clock Select

This field selects which DPLL will drive the port clock for DDIC.

Value	Name
00b	DPLL0

	01b	DPLL1
	10b	DPLL4

3:2 **DDIB Clock Select**

This field selects which DPLL will drive the port clock for DDIB and DSI1.

Value	Name
00b	DPLL0
01b	DPLL1
10b	DPLL4

1:0 **DDIA Clock Select**

This field selects which DPLL will drive the port clock for DDIA and DSI0.

Value	Name
00b	DPLL0
01b	DPLL1
10b	DPLL4

DPFC_CONTROL_SA

DPFC_CTL_SA - DPFC_CONTROL_SA

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	100100h

This register contains control bits related to Display Frame Buffer Compression Host Invalidation in System Agent.

DWord	Bit	Description
0	31:30	**Reserved** Default Value: 00b Access: R/W Reserved
	29	**CPUFNCEN** Default Value: 0b Access: R/W 0: Display Buffer is not in a CPU fence. No modifications are allowed from CPU to the Display Buffer. 1: Display Buffer exists in a CPU fence.
	28:5	**Reserved** Default Value: 000000h Access: R/W Reserved
	4:0	**CPUFNCNUM** Default Value: 00h Access: R/W This field specifies the CPU visible FENCE number corresponding to the placement of the uncompressed frame buffer.

DPFC_CPU_FENCE_OFFSET

DPFC_CFO - DPFC_CPU_FENCE_OFFSET

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	100104h

This register contains control bits related to Display Frame Buffer Compression Host Invalidation in System Agent.

DWord	Bit	Description
0	31:22	**Reserved** Default Value: 000h Access: R/W Reserved
	21:0	**YFNCDISP** Default Value: 000000h Access: R/W Y offset from the CPU fence to the Display Buffer base

DPHY_CLK_TIMING_PARAM

DPHY_CLK_TIMING_PARAM

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32

Address:	162180h-162183h
Name:	DPHY 0 Clock Lane Timing Parameter
ShortName:	DPHY_CLK_TIMING_PARAM_0
Power:	PG0
Reset:	global

Address:	6C180h-6C183h
Name:	DPHY 1 Clock Lane Timing Parameter
ShortName:	DPHY_CLK_TIMING_PARAM_1
Power:	PG0
Reset:	global

This register specifies the D-PHY timing parameters for the Clock Lane, if SW is overriding the HW defaults. This register is located within the combo-PHY and is used to apply the overrides to the Clock Lane. The DSI Controller within the Display Core has an identical register (DSI_CLK_TIMING_PARAM) that is used to calculate the transition latencies of the Clock Lane. Both registers should be programmed by Software if an override is to be applied to the Clock Lane.
All fields are defined in number of Escape clocks.

Restriction

Overall restriction is that the timing parameters must be non-zero if SW is overriding the HW timing parameters.
The programming of this register must be equal to or less than the programming of it's sister register that lives within the Display Core (DSI_CLK_TIMING_PARAM).

DWord	Bit	Description
0	31	**CLK_PREPARE Override** Access: R/W This field controls the override of the CLK-PREPARE timing parameter. Value 0b: HW maintains **[Default]** Value 1b: SW overrides
	30:28	**CLK_PREPARE** Access: R/W

DPHY_CLK_TIMING_PARAM

This parameter defines the time that the Host drives the Clock Lane with the LP-00 Lane state (the Bridge state) immediately before the HS-0 Line state.
This field represents a hexadecimal value with a precision of 1.2 – i.e. the most significant bit is the integer and the least significant 2 bits are fraction bits. So, the field can represent a range of 0.25 to 1.75 (12.5ns to 87.5ns assuming an Escape clock with a 20MHz frequency)
HW maintains this timing parameter at 1 Escape clock (minimum 50ns)

Value	Name
001b	0.25 Escape clocks
010b	0.50 Escape clocks
011b	0.75 Escape clocks
100b	1.00 Escape clocks
101b	1.25 Escape clocks
110b	1.50 Escape clocks
111b	1.75 Escape clocks
Others	Reserved

Programming Notes
Caution: The MIPI D-PHY specification has a maximum of 95ns for this parameter.

27 **CLK_ZERO Override**

Access:	R/W

This field controls the override of the CLK-ZERO timing parameter

Value	Name
0	HW Maintains
1	SW overrides

26:24 **Reserved**

Format:	MBZ

23:20 **CLK_ZERO**

Access:	R/W

This parameter defines the time that the Host drives the HS-0 Lane state on the Clock Lane.
HW maintains this parameter at 5 Escape clocks (minimum 250ns)

19 **CLK_PRE Override**

Access:	R/W

This field controls the override of the CLK-PRE timing parameter.

Value	Name
0	HW Maintains
1	SW overrides

18 **Reserved**

DPHY_CLK_TIMING_PARAM

	Format:	MBZ

17:16 CLK_PRE

Access:	R/W

This parameter defines the time that the HS clock shall be driven by the Host prior to any Data Lane beginning its transition from the LP state to the HS state.
HW maintains this parameter at 8 UI (1 Byte clock). This field will override the parameter with a value measured in Escape clocks which will be much greater than 8 UI.

15 CLK_POST Override

Access:	R/W

This field controls the override of the CLK-POST timing parameter

Value	Name
0	HW Maintains
1	SW overrides

14:11 Reserved

Format:	MBZ

10:8 CLK_POST

Access:	R/W

This parameter defines the time the Host continues to transmit the HS clock after the last Data Lane has transitioned to the LP state.
HW maintains this parameter at 1.25 Escape clocks plus 7 Byte clocks (minimum 62.5ns + 56 UI)

7 CLK_TRAIL Override

Access:	R/W

This field controls the override of the CLK-TRAIL timing parameter

Value	Name
0	HW Maintains
1	SW overrides

6:3 Reserved

Format:	MBZ

2:0 CLK_TRAIL

Access:	R/W

This parameter defines the time that the Host drives the HS-0 Lane state on the Clock Lane after the CLK-POST time has been achieved.
HW maintains this parameter at 1.25 Escape clocks (minimum 62.5ns)

DPHY_DATA_TIMING_PARAM

DPHY_DATA_TIMING_PARAM

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32

Address:	162184h-162187h
Name:	DPHY 0 Data Lane Timing Parameter
ShortName:	DPHY_DATA_TIMING_PARAM_0
Power:	PG0
Reset:	global

Address:	6C184h-6C187h
Name:	DPHY 1 Data Lane Timing Parameter
ShortName:	DPHY_DATA_TIMING_PARAM_1
Power:	PG0
Reset:	global

This register specifies the D-PHY timing parameters for the Data Lane, if SW is overriding the HW defaults.
This register is located within the combo-PHY and is used to apply the overrides to the Data Lanes. The DSI Controller within the Display Core has an identical register (DSI_DATA_TIMING_PARAM) that is used to calculate the transition latencies of the Data Lanes. Both registers should be programmed by Software if an override is to be applied to the Clock Lane.
All fields are defined in number of Escape clocks.

Restriction

Overall restriction is that the timing parameters must be non-zero if SW is overriding the HW timing parameters.
The programming of this register must be equal to or less than the programming of it's sister register that lives within the Display Core (DSI_DATA_TIMING_PARAM).

DWord	Bit	Description
0	31	**HS_PREPARE Override** Access: R/W This field controls the override of the HS-PREPARE timing parameter. Value 0: HW maintains Value 1: SW overrides
	30:27	**Reserved** Format: MBZ

DPHY_DATA_TIMING_PARAM

26:24 **HS_PREPARE**

Access:	R/W

This parameter defines the time that the Host drives a Data Lane with the LP-00 Lane state (the Bridge state) immediately before driving the HS-0 Line state.
This field represents a hexadecimal value with a precision of 1.2 – i.e. the most significant bit is the integer and the least significant 2 bits are fraction bits. So, the field can represent a range of 0.25 to 1.75 (12.5ns to 87.5ns assuming an Escape clock with a 20MHz frequency)
HW maintains this parameter at 1 Escape clock (minimum 50ns)

Value	Name
001b	0.25 Escape clocks
010b	0.50 Escape clocks
011b	0.75 Escape clocks
100b	1.0 Escape clocks
101b	1.25 Escape clocks
110b	1.50 Escape clocks
111b	1.75 Escape clocks
Others	Reserved

Programming Notes
Caution: The MIPI D-PHY specification has a maximum of 85ns + 6UI for this parameter.

23 **HS_ZERO Override**

Access:	R/W

This field controls the override of the HS-ZERO timing parameter

Value	Name
0	HW maintains
1	SW overrides

22:20 **Reserved**

Format:	MBZ

19:16 **HS_ZERO**

Access:	R/W

This parameter defines the time that the Host drives the HS-0 Lane state on a Data Lane.
HW maintains this parameter at 2 Escape clocks plus 1 Byte clock (minimum 100ns + 8UI)

15 **HS_TRAIL Override**

Access:	R/W

This field controls the override of the HS-TRAIL timing parameter

Value	Name
0	HW maintains

DPHY_DATA_TIMING_PARAM

	1	SW overrides

14:11 Reserved

Format:	MBZ

10:8 HS_TRAIL

Access:	R/W

This parameter defines the time that the Host drives the flipped differential state of the last payload data bit of a HS transmission on a Data Lane.
HW maintains this parameter at 1.5 Escape clocks (minimum 75ns)

7 HS_EXIT Override

Access:	R/W

This field controls the override of the HS-EXIT timing parameter

Value	Name
0	HW maintains
1	SW overrides

6:3 Reserved

Format:	MBZ

2:0 HS_EXIT

Access:	R/W

This parameter defines the time that the Host drives the LP-11 Lane state (i.e. the Stop state) following a HS burst.
HW maintains this parameter at 2 Escape clocks (minimum 100ns)

DPHY_ESC_CLK_DIV

DPHY_ESC_CLK_DIV	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	162190h-162193h
Name:	DPHY 0 Escape Clock Divider
ShortName:	DPHY_ESC_CLK_DIV_0
Power:	PG0
Reset:	global
Address:	6C190h-6C193h
Name:	DPHY 1 Escape Clock Divider
ShortName:	DPHY_ESC_CLK_DIV_1
Power:	PG0
Reset:	global

This register defines the clock divider variable M needed to generate an Escape clock from the 8X clock.
This register is located within the combo-PHY. There is an identical register (DSI_ESC_CLK_DIV) located within the Display Core. Both of these registers should be programmed by Software.

Restriction :
The programming of this register must be identical to the programming of its sister register that lives within the Display Core (DSI_ESC_CLK_DIV).
If operating in Dual Link mode, then both Combo-PHY registers (DPHY_ESC_CLK_DIV_0 and DPHY_ESC_CLK_DIV_1) have to be programmed to the same value as the sister register that lives within the Display Core's master port (DSI_ESC_CLK_DIV_0)

DWord	Bit	Description
0	31:21	**Reserved**
	20:16	**Byte Clocks per Escape Clock** Access: RO This field reports the number of Byte clocks present within a given Escape clock. The DSI transcoder calculates this variable based off of the Escape clock divider M. N = Ceiling(M/8) The DSI complex (transcoder and D-PHY) use this information to emulate an Escape clock using the Byte clock.
	15:9	**Reserved**
	8:0	**Escape Clock Divider M** Access: R/W

DPHY_ESC_CLK_DIV		
		This field specifies the divider variable (M) needed to derive the Escape clock from the Link clock (i.e. the 8X frequency) Escape frequency = 8X frequency / M The DSI transcoder does not use a physical Escape clock, so there is no physical divider, but the transcoder needs to know the value of M to emulate the Escape clock in Byte clocks. **Restriction** The Escape clock frequency must be as close to, but not greater than 20MHz. Therefore, the programming of M should be: M = Ceiling(8X Frequency (in MHz) / 20 MHz)

DPHY_TA_TIMING_PARAM

DPHY_TA_TIMING_PARAM

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32

Address:	162188h-16218Bh
Name:	DPHY 0 Turnaround Timing Parameter
ShortName:	DPHY_TA_TIMING_PARAM_0
Power:	PG0
Reset:	global

Address:	6C188h-6C18Bh
Name:	DPHY 1 Turnaround Timing Parameter
ShortName:	DPHY_TA_TIMING_PARAM_1
Power:	PG0
Reset:	global

This register specifies the D-PHY timing parameters used for the Bus Turn-Around flow, if SW is overriding the HW defaults.
All fields are defined in number of Escape clocks.

Restriction

Overall restriction is that the timing parameters must be non-zero if SW is overriding the HW timing parameters.
If operating in Dual Link mode, then SW should program both Combo-PHY registers (DPHY_TA_TIMING_PARAM_0 and DPHY_TA_TIMING_PARAM_1), if necessary.

DWord	Bit	Description
0	31	**TA_SURE Override** Access: R/W This field controls the override of the TA-SURE timing parameter Value 0: HW maintains Value 1: SW overrides
	30:21	**Reserved** Format: MBZ
	20:16	**TA_SURE** Access: R/W

DPHY_TA_TIMING_PARAM

This parameter defines the time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.
This field represents a hexadecimal value with a precision of 3.2 – i.e. the most significant 3 bits are the integer and the least significant 2 bits are fraction bits. So, the field can represent a range of 0.25 to 7.75 (12.5ns to 387.5ns assuming an Escape clock with a 20MHz frequency)
HW maintains this parameter at 1 Escape clock (minimum 50ns).

Programming Notes

1. Caution: The MIPI D-PHY specification has a maximum of 2 Escape clocks for this parameter
2. If operating at or below an 800MHz Link frequency, this parameter should be overridden and programmed to a value of 0

15 TA_GO Override

Access:	R/W

This field controls the override of the TA-GO timing parameter

Value	Name
0	HW maintains
1	SW overrides

14:12 Reserved

Format:	MBZ

11:8 TA_GO

Access:	R/W

This parameter defines the time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Turnaround.
HW maintains this parameter at 4 Escape clocks (minimum 200ns)

Programming Notes

Caution: The MIPI D-PHY specification has a fixed requirement of 4 Escape clocks for this parameter

7 TA_GET Override

Access:	R/W

This field controls the override of the TA-GET timing parameter

Value	Name
0	HW maintains
1	SW overrides

6:4 Reserved

Format:	MBZ

3:0 TA_GET

Access:	R/W

This parameter defines the time that the new transmitter drives the Bridge state (LP-00) after

DPHY_TA_TIMING_PARAM		
		accepting control during a Link Turnaround. HW maintains this parameter at 5 Escape clocks (minumum 250ns) **Programming Notes** Caution: The MIPI D-PHY specification has a fixed requirement of 5 Escape clocks for this parameter

DPHY_TRIG_EXT

DPHY_TRIG_EXT	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	16218Ch-16218Fh
Name:	DPHY 0 Trigger Extension
ShortName:	DPHY_TRIG_EXT_0
Power:	PG0
Reset:	global
Address:	6C18Ch-6C18Fh
Name:	DPHY 1 Trigger Extension
ShortName:	DPHY_TRIG_EXT_1
Power:	PG0
Reset:	global

This register specifies the amount of time to extend a Trigger message to the Peripheral.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**Trigger Extension** Access: R/W This field specifies the number of Escape clocks to extend a trigger message by. This effectively extends the duration that the trigger is asserted at the Peripheral's Protocol Layer. This field is only used if a Trigger Message is initiated from the DSI_LP_MSG register.

DPLC_CTL

DPLC_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled
Address:	49400h-49403h
Name:	Pipe A LDPST Control
ShortName:	DPLC_CTL_A
Power:	PG1
Reset:	soft

Description

Restriction : LDPST is supported for horizontal and vertical pipe sizes up to 4096 pixels.

Restriction

The following programming sequence should be followed.

1. Enable LDPST with the Orientation and the Tile Size bits programmed correctly.
2. Program IE coefficients
3. Enable pipe.

Orientation and Tile Size must not be changed when the LDPST function is enabled.

DWord	Bit	Description
0	31	**Function Enable** This field enables the LDPST function. Histogram is enabled directly by this field. Value: 0b – Disable; 1b – Enable
	30	**Reserved**
	29	**Load IE** Access: R/W Set Hardware clears this field after the load is complete. Value: 0b – Ready/Done

DPLC_CTL

	1b	Loading

28 Orientation

This field sets the orientation. In case of preload when there is a change in Orientation for next frame, this bit needs to be set before the IE correction points are written.

Value	Name	Description
0b	Landscape	16x9 tile arrangement
1b	Portrait	9x16 tile arrangement

27 Frame Histogram Done

Access:	RO

This bit is set by H/W when done creating histograms for all valid tiles (based on hsize and vsize). S/W should start reading from histogram buffers only when this bit is set at Vblank. This bit is cleared by H/W only.

Value	Name	Description
0b	Not Done	Histogram creation not done
1b	Done	Histogram creation done

26 Histogram Buffer ID

Access:	RO

This bit is set or cleared by H/W to indicate which double buffered BANK H/W is working on for creating histogram for current frame. This bit toggles one clk after Vblank if Hist_buffer_delay bit is not set.

Value	Name	Description
0b	Bank0	Creating Histogram in Bank0
1b	Bank1	Creating Histogram in Bank1

25 IE Buffer ID

Access:	RO

This bit is set or cleared by H/W to indicate which double buffered BANK H/W is using for reading correction factors for current frame. This bit will toggle at Vblank when load IE bit is set.

Value	Name	Description
0b	Bank0	Reading correction factors from Bank 0
1b	Bank1	Reading correction factors from Bank 0

24 Reserved

Format:	MBZ

23 Reserved

Format:	MBZ

DPLC_CTL

	22:20	**Reserved** Format: MBZ
	19	**Reserved** Format: MBZ
	18:14	**Reserved** Format: MBZ
	13:12	**Enhancement mode** These bits are the control bits to select between Look up table mode and Multiplier mode. **Value** / **Name** / **Description** 00b / Direct **[Default]** / Direct look up Mode 01b / Multiplicative / Multiplicative Mode 10b / Reserved / Reserved 11b / Reserved / Reserved
	11	**Reserved**
	10	**Reserved**
	9	**Reserved**
	8	**Reserved**
	7	**Reserved**
	6	**Reserved**
	5	**Reserved**
	4	**Reserved**
	3	**Reserved**
	2	**Reserved**
	1	**Hist Buffer Delay** Access: R/W This field controls when the histogram readback buffer is loaded in H/W. S/W can set this bit while reading the histogram bin registers to ensure that the H/W does not overwrite the histogram registers with the data for the new frame. This bit must be cleared by the S/W as soon as the histogram bin read is complete.
	0	**Reserved**

DPLC_HIST_DATA

DPLC_HIST_DATA	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	49408h-4940Bh
Name:	Pipe A LDPST Histogram Data
ShortName:	DPLC_HIST_DATA_A
Power:	PG1
Reset:	soft

This register contains the histogram values for the array of LDPST Histogram table entries.
The data format is arranged as 32 dwords for each tile, containing 32 bins. The index register controls which bin and dword is accessed.

DWord	Bit	Description
0	31:17	**Reserved** Format: MBZ
	16:0	**Bin** Histogram Data for Bin

DPLC_HIST_INDEX

DPLC_HIST_INDEX

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	49404h-49407h
Name:	Pipe A LDPST Histogram Index
ShortName:	DPLC_HIST_INDEX_A
Power:	PG1
Reset:	soft

Description

The LDPST Histogram table tile entries are accessed through index and data registers.
Each tile is composed of 32 histogram bins in 32 data Dwords.
The index fields address the individual tiles and Dwords.
Hardware will automatically walk the indexes through each Dword and raster scan through the X and Y, starting from the upper left corner of the display. The automatic walk is based on the programmed pipe source size.
Software can manually program the index to access specific tiles and Dwords.

There are 144 tiles arranged in a 16x9 (horizontal x vertical) or 9x16 array, depending on the DPLC_CTL Orientation setting.

DWord	Bit	Description
0	31:21	**Reserved** Format: MBZ
	20	**Reserved** Format: MBZ
	19:16	**Y Index** Access: Write/Read Status This index points to the current vertical tile row in the array. This index auto increments by one after each horizontal tile row is completed. It will automatically rollover when the final (16th or 9th) vertical tile row is completed. Value: [0,15]
	15:13	**Reserved** Format: MBZ

DPLC_HIST_INDEX

	12	**Reserved** Format: MBZ
	11:8	**X Index** Access: Write/Read Status This index points to current horizontal tile in the array. This index auto increments by one after the final (32nd) Dword is accessed. It will automatically rollover when the final (16th or 9th) horizontal tile is completed. [0,15]
	7:5	**Reserved** Format: MBZ
	4:0	**DW Index** Access: Write/Read Status This index points to the next Dword within the tile. This index auto increments by one after each read to the data register is completed. It will automatically rollover when the final (32nd) Dword is accessed. [0,31]

DPLL_CFGCR0

DPLL_CFGCR0	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	164000h-164003h
Name:	DPLL0_CFGCR0
ShortName:	DPLL0_CFGCR0
Power:	PG0
Reset:	global
Address:	164080h-164083h
Name:	DPLL1_CFGCR0
ShortName:	DPLL1_CFGCR0
Power:	PG0
Reset:	global
Address:	164100h-164103h
Name:	TBTPLL_CFGCR0
ShortName:	TBTPLL_CFGCR0
Power:	PG0
Reset:	global
Address:	164200h-164203h
Name:	DPLL4_CFGCR0
ShortName:	DPLL4_CFGCR0
Power:	PG0
Reset:	global

This register is used to configure the DPLL mode, frequency, and SSC.
This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31:26	**Reserved**

DPLL_CFGCR0

	Format:	MBZ

25 SSC Enable

SSC enable

Value	Name
0b	Disable
1b	Enable

24:10 DCO Fraction

Default Value:	0x4000

(DCO Frequency/Reference Frequency - INT(DCO Frequency/Reference Frequency)) * 2^15

9:0 DCO Integer

Default Value:	0x151

INT (DCO Frequency/Reference Frequency)

DPLL_CFGCR1

DPLL_CFGCR1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	164004h-164007h
Name:	DPLL0_CFGCR1
ShortName:	DPLL0_CFGCR1
Power:	PG0
Reset:	global
Address:	164084h-164087h
Name:	DPLL1_CFGCR1
ShortName:	DPLL1_CFGCR1
Power:	PG0
Reset:	global
Address:	164104h-164107h
Name:	TBTPLL_CFGCR1
ShortName:	TBTPLL_CFGCR1
Power:	PG0
Reset:	global
Address:	164204h-164207h
Name:	DPLL4_CFGCR1
ShortName:	DPLL4_CFGCR1
Power:	PG0
Reset:	global

Description
This register, together with DPLL_CFGCR0, is used to configure the DPLL frequency.
This register is not reset by the device 2 FLR.

Programming Notes
The post divider is P*Q*K

<table>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td>0</td><td>31:18</td><td>Reserved
<table><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td></td><td>17:10</td><td>Qdiv Ratio
This field specifies the Q divider ratio. This field is only used when Qdiv Mode is set to Enable to get a divider value other than 1.</td></tr>
<tr><td></td><td>9</td><td>Qdiv Mode
This field enables the Q divider when the ratio is not 1.<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0b</td><td>Disable</td><td>Q divider = 1</td></tr><tr><td>1b</td><td>Enable</td><td>Q divider = Qdiv Ratio</td></tr></table><table><tr><th>Restriction</th></tr><tr><td>If K is not 2, Q MUST be 1 to ensure 50% duty cycle.</td></tr></table></td></tr>
<tr><td></td><td>8:6</td><td>Kdiv
This field specifies the K divider ratio.<table><tr><th>Value</th><th>Name</th></tr><tr><td>001b</td><td>1 [Default]</td></tr><tr><td>010b</td><td>2</td></tr><tr><td>100b</td><td>3</td></tr></table></td></tr>
<tr><td></td><td>5:2</td><td>Pdiv
This field specifies the P divider ratio.<table><tr><th>Value</th><th>Name</th></tr><tr><td>0001b</td><td>2</td></tr><tr><td>0010b</td><td>3 [Default]</td></tr><tr><td>0100b</td><td>5</td></tr><tr><td>1000b</td><td>7</td></tr></table></td></tr>
<tr><td></td><td>1:0</td><td>Central Frequency
<table><tr><td></td><td></td></tr></table>This field specifies the center frequency.
Display software must leave this field at the default value. It no longer needs to be configured as part of PLL programming.<table><tr><th>Value</th><th>Name</th></tr><tr><td>00b</td><td>9600 MHz</td></tr><tr><td>01b</td><td>9000 MHz</td></tr><tr><td>10b</td><td>Reserved</td></tr><tr><td>11b</td><td>8400 MHz [Default]</td></tr></table></td></tr>
</table>

DPLL_ENABLE

DPLL_ENABLE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	46010h-46013h
Name:	DPLL 0 Enable
ShortName:	DPLL0_ENABLE
Power:	Always on
Reset:	soft
Address:	46014h-46017h
Name:	DPLL 1 Enable
ShortName:	DPLL1_ENABLE
Power:	Always on
Reset:	soft
Address:	46020h-46023h
Name:	Thunderbolt PLL Enable
ShortName:	TBT_PLL_ENABLE
Power:	Always on
Reset:	soft
Address:	46030h-46033h
Name:	MG PLL 1 Enable
ShortName:	MGPLL1_ENABLE
Power:	Always on
Reset:	soft
Address:	46034h-46037h
Name:	MG PLL 2 Enable
ShortName:	MGPLL2_ENABLE
Power:	Always on
Reset:	soft

DPLL_ENABLE	
Address:	46038h-4603Bh
Name:	MG PLL 3 Enable
ShortName:	MGPLL3_ENABLE
Power:	Always on
Reset:	soft
Address:	4603Ch-4603Fh
Name:	MG PLL 4 Enable
ShortName:	MGPLL4_ENABLE
Power:	Always on
Reset:	soft
Address:	46040h-46043h
Name:	MG PLL 5 Enable
ShortName:	MGPLL5_ENABLE
Power:	Always on
Reset:	soft
Address:	46044h-46047h
Name:	MG PLL 6 Enable
ShortName:	MGPLL6_ENABLE
Power:	Always on
Reset:	soft
Address:	46048h-4604Bh
Name:	MG PLL 7 Enable
ShortName:	MGPLL7_ENABLE
Power:	Always on
Reset:	soft
Address:	4604Ch-4604Fh
Name:	MG PLL 8 Enable
ShortName:	MGPLL8_ENABLE
Power:	Always on
Reset:	soft

DPLL_ENABLE

These registers are used to enable the PLLs for driving the ports.

DWord	Bit	Description
0	31	**PLL Enable** This field enables or disables the PLL. Value: 0b = Disable; 1b = Enable
	30	**PLL Lock** Access: RO This fields indicates the status of the PLL Lock. Value: 0b = Not locked or not enabled; 1b = Locked
	29	**Reserved** Format: MBZ
	28	**Reserved**
	27	**Power Enable** This field enables or disables the PLL power. Value: 0b = Disable; 1b = Enable
	26	**Power State** Access: RO This fields indicates the status of the PLL power. Value: 0b = Disabled; 1b = Enabled
	25:12	**Reserved** Format: MBZ
	11	**Reserved** Format: MBZ
	10:0	**Reserved** Format: MBZ

DPST_BIN

DPST_BIN	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank
Address:	490C4h-490C7h
Name:	Pipe DPST Bin Data
ShortName:	DPST_BIN_A
Power:	PG1
Reset:	soft
Address:	491C4h-491C7h
Name:	Pipe DPST Bin Data
ShortName:	DPST_BIN_B
Power:	PG2
Reset:	soft
Address:	492C4h-492C7h
Name:	Pipe DPST Bin Data
ShortName:	DPST_BIN_C
Power:	PG2
Reset:	soft

Access to this address are steered to the correct register by programming the Bin Register Function Select and the Bin Register Index. Updates take place at the start of vertical blank.

DWord	Bit	Description
0	31	**Busy Bit** If (DPST_CTL:Bin Register Function Select = Threshold Count) {This is a read only bit. If set, the engine is busy and the rest of the register is undefined. If clear, the register contains valid data.} Else (Image Enhancement) {This bit is reserved.}
	30:24	**Reserved**
	23:0	**Data** If (DPST_CTL : Bin Register Function Select = Threshold Count) {Bits 23:0 are read only bits. They indicate the total number of pixels in this bin. The bin value is updated when guardband interrupt delay is met, and is not valid until after a histogram event has occurred. The bin value will stop incrementing once the maximum has been reached.} Else (Image Enhancement) {Bits

DPST_BIN		
		23:10 are reserved and should be written as zeroes. Bits 9:0 are R/W double-buffered and program the correction value for this bin. Writes to this register are double buffered on the next vblank. The value written here is the 10bit corrected channel value for the lowest point of the bin.}

DPST_CTL

DPST_CTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	490C0h-490C3h
Name:	Pipe DPST Control
ShortName:	DPST_CTL_A
Power:	PG1
Reset:	soft
Address:	491C0h-491C3h
Name:	Pipe DPST Control
ShortName:	DPST_CTL_B
Power:	PG2
Reset:	soft
Address:	492C0h-492C3h
Name:	Pipe DPST Control
ShortName:	DPST_CTL_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
	31:25	**Reserved**
	24	**Histogram Mode Select** Value / Name / Description 0b / YUV / YUV Luma Mode 1b / HSV / HSV Intensity Mode
	23:15	**Reserved**
	14:13	**Enhancement mode** Value / Name / Description 00b / Direct / Direct look up mode 01b / Additive / Additive mode 10b / Multiplicative / Multiplicative mode 11b / Reserved / Reserved

<table>
<tr><th colspan="3">DPST_CTL</th></tr>
<tr><td></td><td>12</td><td>Reserved</td></tr>
<tr><td></td><td>11</td><td>Bin Register Function Select
This field indicates what data is being written to or read from the bin data register.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th></tr>
<tr><td>0b</td><td>TC</td><td>Threshold Count. A read from the bin data register returns that bin's threshold value from the most recent vblank load event (guardband threshold trip). Valid range for the Bin Index is 0 to 31.</td></tr>
<tr><td>1b</td><td></td><td>Reserved</td></tr>
</table></td></tr>
<tr><td></td><td>10:7</td><td>Reserved</td></tr>
<tr><td></td><td>6:0</td><td>Bin Register Index
This field indicates the bin number whose data can be accessed through the bin data register. This value is automatically incremented by a read or a write to the bin data register if the busy bit is not set.</td></tr>
</table>

DPST_GUARD

DPST_GUARD

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank
Address:	490C8h-490CBh
Name:	Pipe DPST Threshold Guardband
ShortName:	DPST_GUARD_A
Power:	PG1
Reset:	soft
Address:	491C8h-491CBh
Name:	Pipe DPST Threshold Guardband
ShortName:	DPST_GUARD_B
Power:	PG2
Reset:	soft
Address:	492C8h-492CBh
Name:	Pipe DPST Threshold Guardband
ShortName:	DPST_GUARD_C
Power:	PG2
Reset:	soft

Updates take place at the start of vertical blank.

DWord	Bit	Description
0	31	**Histogram Interrupt enable** Value / Name / Description 0b / Disable / Disabled 1b / Enable / This generates a histogram interrupt once a Histogram event occurs.
	30	**Histogram Event status** Access: R/WC When a Histogram event has occurred, this will get set by the hardware. For any more Histogram events to occur, clear this bit by writing a '1'. Value / Name / Description 0b / Not Occurred / Histogram event has not occurred

DPST_GUARD				
		1b	Occured	Histogram event has occurred
	29:22	**Guardband Interrupt Delay** An interrupt is always generated after this many consecutive frames of the guardband threshold being surpassed. This value is double buffered on start of vblank. **Restriction** A value of 0 is invalid.		
	21:0	**Threshold Guardband** This value is used to determine the guardband for the threshold interrupt generation. This single value is used for all the segments. This value is double buffered on start of vblank. This value is shifted left 2 bits (multiplied by 4) for use with the 24 bit bin values.		

Driver Render Force Wake Ack

DRIVER_RENDER_FWAKE_ACK - Driver Render Force Wake Ack

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00D84h

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].
To set bit0, for example, the data would be 0x0001_0001.
To clear bit0, for example, the data would be 0x0001_0000.
Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO
	15:0	**GPM Driver ForceWake Ack** Access: R/W 1'b0 : GT Render Can be powered down (default) 1'b1 : GT Render cannot be powered down

Driver VDBox0 Force Wake Ack

DRIVER_VDBOX0_FWAKE_ACK - Driver VDBox0 Force Wake Ack	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00D50h
Name:	Driver VDBox0 Force Wake Ack
ShortName:	DRIVER_VDBOX0_FWAKE_ACK

This register is used for GPM to handshake the driver's VDBox0 forcewake request

DWord	Bit	Description
0	31:16	**Reserved** Access: RO
	15:0	**GPM Driver Vdbox0 ForceWake Ack** Access: R/W 1'b0 : GT Media Slice 0 can be powered down (default) 1'b1 : GT Media Slice 0 cannot be powered down

Driver VDBox1 Force Wake Ack

DRIVER_VDBOX1_FWAKE_ACK - Driver VDBox1 Force Wake Ack	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00D54h
Name:	Driver VDBox1 Force Wake Ack
ShortName:	DRIVER_VDBOX1_FWAKE_ACK

This register is used for GPM to handshake the driver's VDBox1 forcewake request

DWord	Bit	Description
0	31:16	**Reserved** Access: RO
	15:0	**GPM Driver Vdbox1 ForceWake Ack** Access: R/W 1'b0 : GT Media Slice 0 can be powered down (default) 1'b1 : GT Media Slice 0 cannot be powered down

Driver VDBox2 Force Wake Ack

DRIVER_VDBOX2_FWAKE_ACK - Driver VDBox2 Force Wake Ack

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00D58h
Name:	Driver VDBox2 Force Wake Ack
ShortName:	DRIVER_VDBOX2_FWAKE_ACK

This register is used for GPM to handshake the driver's VDBox2 forcewake request

DWord	Bit	Description
0	31:16	**Reserved** Access: RO
	15:0	**GPM Driver Vdbox2 ForceWake Ack** Access: R/W 1'b0 : GT Media Slice 1 can be powered down (default) 1'b1 : GT Media Slice 1 cannot be powered down

Driver VDBox3 Force Wake Ack

DRIVER_VDBOX3_FWAKE_ACK - Driver VDBox3 Force Wake Ack	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00D5Ch
Name:	Driver VDBox3 Force Wake Ack
ShortName:	DRIVER_VDBOX3_FWAKE_ACK

This register is used for GPM to handshake the driver's VDBox3 forcewake request

DWord	Bit	Description
0	31:16	**Reserved** Access: RO
	15:0	**GPM Driver Vdbox3 ForceWake Ack** Access: R/W 1'b0 : GT Media Slice 1 can be powered down (default) 1'b1 : GT Media Slice 1 cannot be powered down

Driver VDBox4 Force Wake Ack

DRIVER_VDBOX4_FWAKE_ACK - Driver VDBox4 Force Wake Ack	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00D60h
Name:	Driver VDBox4 Force Wake Ack
ShortName:	DRIVER_VDBOX4_FWAKE_ACK

This register is used for GPM to handshake the driver's VDBox4 forcewake request

DWord	Bit	Description
0	31:16	**Reserved** Access: RO
	15:0	**GPM Driver Vdbox4 ForceWake Ack** Access: R/W 1'b0 : GT Media Slice 2 can be powered down (default) 1'b1 : GT Media Slice 2 cannot be powered down

Driver VDBox5 Force Wake Ack

DRIVER_VDBOX5_FWAKE_ACK - Driver VDBox5 Force Wake Ack	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00D64h
Name:	Driver VDBox5 Force Wake Ack
ShortName:	DRIVER_VDBOX5_FWAKE_ACK

This register is used for GPM to handshake the driver's VDBox5 forcewake request

DWord	Bit	Description
0	31:16	**Reserved** Access: RO
	15:0	**GPM Driver Vdbox5 ForceWake Ack** Access: R/W 1'b0 : GT Media Slice 2 can be powered down (default) 1'b1 : GT Media Slice 2 cannot be powered down

Driver VDBox6 Force Wake Ack

DRIVER_VDBOX6_FWAKE_ACK - Driver VDBox6 Force Wake Ack

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00D68h
Name:	Driver VDBox6 Force Wake Ack
ShortName:	DRIVER_VDBOX6_FWAKE_ACK

This register is used for GPM to handshake the driver's VDBox6 forcewake request

DWord	Bit	Description
0	31:16	**Reserved** Access: RO
	15:0	**GPM Driver Vdbox6 ForceWake Ack** Access: R/W 1'b0 : GT Media Slice 3 can be powered down (default) 1'b1 : GT Media Slice 3 cannot be powered down

Driver VDBox7 Force Wake Ack

DRIVER_VDBOX7_FWAKE_ACK - Driver VDBox7 Force Wake Ack	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00D6Ch
Name:	Driver VDBox7 Force Wake Ack
ShortName:	DRIVER_VDBOX7_FWAKE_ACK

This register is used for GPM to handshake the driver's VDBox7 forcewake request

DWord	Bit	Description
0	31:16	**Reserved** Access: RO
	15:0	**GPM Driver Vdbox7 ForceWake Ack** Access: R/W 1'b0 : GT Media Slice 3 can be powered down (default) 1'b1 : GT Media Slice 3 cannot be powered down

Driver VEBox0 Force Wake Ack

DRIVER_VEBOX0_FWAKE_ACK - Driver VEBox0 Force Wake Ack	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00D70h
Name:	Driver VEBox0 Force Wake Ack
ShortName:	DRIVER_VEBOX0_FWAKE_ACK

This register is used for GPM to handshake the driver's VEBox0 forcewake request

DWord	Bit	Description
0	31:16	**Reserved** Access: RO
	15:0	**GPM Driver Vebox0 ForceWake Ack** Access: R/W 1'b0 : GT Media Slice 0 can be powered down (default) 1'b1 : GT Media Slice 0 cannot be powered down

Driver VEBox1 Force Wake Ack

DRIVER_VEBOX1_FWAKE_ACK - Driver VEBox1 Force Wake Ack	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00D74h
Name:	Driver VEBox1 Force Wake Ack
ShortName:	DRIVER_VEBOX1_FWAKE_ACK

This register is used for GPM to handshake the driver's VEBox1 forcewake request

DWord	Bit	Description
0	31:16	**Reserved** Access: RO
	15:0	**GPM Driver Vebox1 ForceWake Ack** Access: R/W 1'b0 : GT Media Slice 1 can be powered down (default) 1'b1 : GT Media Slice 1 cannot be powered down

Driver Vebox2 Force Wake Ack

DRIVER_VEBOX2_FWAKE_ACK - Driver Vebox2 Force Wake Ack

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00D78h
Name:	Driver Vebox2 Force Wake Ack
ShortName:	DRIVER_VEBOX2_FWAKE_ACK

This register stores the ACK, from GPMunit, once the driver forcewake has been serviced
Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].
To set bit0, for example, the data would be 0x0001_0001.
To clear bit0, for example, the data would be 0x0001_0000.
Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO
	15:0	**GPM Driver Vebox2 ForceWake Ack** Access: R/W 1'b0 : GT Media Can be powered down (default) 1'b1 : GT Media cannot be powered down

Driver Vebox3 Force Wake Ack

DRIVER_VEBOX3_FWAKE_ACK - Driver Vebox3 Force Wake Ack

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00D7Ch
Name:	Driver Vebox3 Force Wake Ack
ShortName:	DRIVER_VEBOX3_FWAKE_ACK

This rgeister stores the Force wake ACK, from GPM, for driver forcewake to VEBOX3
Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].
To set bit0, for example, the data would be 0x0001_0001.
To clear bit0, for example, the data would be 0x0001_0000.
Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO
	15:0	**GPM Driver Vebox3 ForceWake Ack** Access: R/W 1'b0 : GT Media Can be powered down (default) 1'b1 : GT Media cannot be powered down

DSC_CRC_CTL

DSC_CRC_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6B284h-6B287h
Name:	DSC_CRC_CTL_A
ShortName:	DSC_CRC_CTL_A
Power:	PG1
Reset:	soft
Address:	6BA84h-6BA87h
Name:	DSC_CRC_CTL_C
ShortName:	DSC_CRC_CTL_C
Power:	PG1
Reset:	soft
Address:	7822Ch-7822Fh
Name:	DSC0_CRC_CTL_PB
ShortName:	DSC0_CRC_CTL_PB
Power:	PG3
Reset:	soft
Address:	7832Ch-7832Fh
Name:	DSC1_CRC_CTL_PB
ShortName:	DSC1_CRC_CTL_PB
Power:	PG3
Reset:	soft
Address:	7842Ch-7842Fh
Name:	DSC0_CRC_CTL_PC
ShortName:	DSC0_CRC_CTL_PC

DSC_CRC_CTL

Power:	PG4
Reset:	soft
Address:	7852Ch-7852Fh
Name:	DSC1_CRC_CTL_PC
ShortName:	DSC1_CRC_CTL_PC
Power:	PG4
Reset:	soft

DWord	Bit	Description
0	31	**Enable CRC** Access: R/W Enables the CRC calculations.The CRC will give a done indication and a new result at the end of each frame. 0b – Disable 1b – Enable
	30	**CRC Done** Access: R/WC This bit is set on the rising edge of the CRC done indication.This is a sticky bit, cleared by writing 1b to it. 0b – Not Done 1b – Done
	29	**CRC Change** Access: R/WC This bit is set if the CRC result value changes from the previous value. This is a sticky bit, cleared by writing 1b to it. 0b – No Change 1b – Change
	28:0	**Reserved** Format: MBZ

DSC_CRC_RES

DSC_CRC_RES	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	6B288h-6B28Bh
Name:	DSC_CRC_RES_A
ShortName:	DSC_CRC_RES_A
Power:	PG1
Reset:	soft
Address:	6BA88h-6BA8Bh
Name:	DSC_CRC_RES_C
ShortName:	DSC_CRC_RES_C
Power:	PG1
Reset:	soft
Address:	78230h-78233h
Name:	DSC0_CRC_RES_PB
ShortName:	DSC0_CRC_RES_PB
Power:	PG3
Reset:	soft
Address:	78330h-78333h
Name:	DSC1_CRC_RES_PB
ShortName:	DSC1_CRC_RES_PB
Power:	PG3
Reset:	soft
Address:	78430h-78433h
Name:	DSC0_CRC_RES_PC
ShortName:	DSC0_CRC_RES_PC

DSC_CRC_RES

Power:	PG4
Reset:	soft
Address:	78530h-78533h
Name:	DSC1_CRC_RES_PC
ShortName:	DSC1_CRC_RES_PC
Power:	PG4
Reset:	soft

DWord	Bit	Description
0	31:0	**CRC Result Value** This field contains the CRC result at the end of a CRC frame. The CRC done bit indicates when the result is valid.

DSC_PICTURE_PARAMETER_SET_0

DSC_PICTURE_PARAMETER_SET_0	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6B200h-6B203h
Name:	DSCA_PICTURE_PARAMETER_SET_0
ShortName:	DSCA_PICTURE_PARAMETER_SET_0
Power:	PG1
Reset:	soft
Address:	6BA00h-6BA03h
Name:	DSCC_PICTURE_PARAMETER_SET_0
ShortName:	DSCC_PICTURE_PARAMETER_SET_0
Power:	PG1
Reset:	soft
Address:	78270h-78273h
Name:	DSC0_PICTURE_PARAMETER_SET_0_PB
ShortName:	DSC0_PICTURE_PARAMETER_SET_0_PB
Power:	PG3
Reset:	soft
Address:	78370h-78373h
Name:	DSC1_PICTURE_PARAMETER_SET_0_PB
ShortName:	DSC1_PICTURE_PARAMETER_SET_0_PB
Power:	PG3
Reset:	soft
Address:	78470h-78473h
Name:	DSC0_PICTURE_PARAMETER_SET_0_PC
ShortName:	DSC0_PICTURE_PARAMETER_SET_0_PC

DSC_PICTURE_PARAMETER_SET_0

Power:	PG4
Reset:	soft
Address:	78570h-78573h
Name:	DSC1_PICTURE_PARAMETER_SET_0_PC
ShortName:	DSC1_PICTURE_PARAMETER_SET_0_PC
Power:	PG4
Reset:	soft

DWord	Bit	Description
0	31	**Reserved** | | |
	30:21	**Reserved** Format: MBZ
	20	**Reserved** | | |
	19	**vbr_enable** Access: R/W Restriction : DSC variable bit rate modeis not supported. 0b – disable **[Default]** – "0" padding bits are stuffed at the end of a slice to ensure that the total number of bits within the slice is equal to the slice bit budget. 1b – Enable – Bit stuffing is bypassed
	18	**enable_422** Access: R/W 0b – 444 **[Default]** – Input uses 4:4:4 sampling 1b – 422 – Input uses 4:2:2 sampling
	17	**convert_rgb** Access: R/W Indicates whether DSC color space conversion is active. 0b – YCbCr – Color space is YCbCr 1b – convert_rgb – Encoder converts RGB to YCoCg-R, and decoder converts YCoCg-R to RGB.
	16	**block_pred_enable**

DSC_PICTURE_PARAMETER_SET_0

		Access: R/W

Value	Name	Description
0b	disable	BP is not used to code any groups within the picture
1b	enable	Decoder must select between BP and MMAP

15:12 linebuf_depth

Access: R/W

Contains the line buffer bit depth used to generate the bitstream. If a component's bit depth (after color space conversion) is greater than this value, the line storage rounds the reconstructed values to this number of bits.
0x8 = 8 bits
0x9 = 9 bits
0xA = 10 bits
0xB = 11 bits
0xC = 12 bits
0xD = 13 bits
All other encodings are RESERVED

11:8 bits_per_component

Access: R/W

Indicates the number of bits per component for the original pixels of the encoded picture.
0x8 = 8bpc
0xA = 10bpc
0xC = 12bpc
All other encodings are RESERVED

7:4 dsc_version_minor

Access: R/W

Description
Contains the major version of DSC.

3:0 dsc_version_major

Access: R/W

Contains the major version of DSC.
0x1 = Encoder implements DSC

DSC_PICTURE_PARAMETER_SET_1

DSC_PICTURE_PARAMETER_SET_1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6B204h-6B207h
Name:	DSCA_PICTURE_PARAMETER_SET_1
ShortName:	DSCA_PICTURE_PARAMETER_SET_1
Power:	PG1
Reset:	soft
Address:	6BA04h-6BA07h
Name:	DSCC_PICTURE_PARAMETER_SET_1
ShortName:	DSCC_PICTURE_PARAMETER_SET_1
Power:	PG1
Reset:	soft
Address:	78274h-78277h
Name:	DSC0_PICTURE_PARAMETER_SET_1_PB
ShortName:	DSC0_PICTURE_PARAMETER_SET_1_PB
Power:	PG3
Reset:	soft
Address:	78374h-78377h
Name:	DSC1_PICTURE_PARAMETER_SET_1_PB
ShortName:	DSC1_PICTURE_PARAMETER_SET_1_PB
Power:	PG3
Reset:	soft
Address:	78474h-78477h
Name:	DSC0_PICTURE_PARAMETER_SET_1_PC
ShortName:	DSC0_PICTURE_PARAMETER_SET_1_PC

DSC_PICTURE_PARAMETER_SET_1

Power:	PG4
Reset:	soft
Address:	78574h-78577h
Name:	DSC1_PICTURE_PARAMETER_SET_1_PC
ShortName:	DSC1_PICTURE_PARAMETER_SET_1_PC
Power:	PG4
Reset:	soft

DWord	Bit	Description
0	31:20	**RESERVED** Format: MBZ
	19:10	**RESERVED** Format: MBZ
	9:0	**bits_per_pixel** Access: R/W Specifies the target bits/pixel (bpp) rate that is used by the encoder, in steps of 1/16 of a bit per pixel (four fractional bits). Only values greater than or equal to 6.0 are allowed. If vbr_enable is cleared to 0, this value must be less than or equal to the sustained rate that would apply if MPP is always selected with QP = 0, which is a function of bits_per_component, convert_rgb, and rc_range_parameters[0]. If native_422 or native_420 is set to 1, this value shall be programmed to double the target bits per pixel rate.

DSC_PICTURE_PARAMETER_SET_2

DSC_PICTURE_PARAMETER_SET_2	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6B208h-6B20Bh
Name:	DSCA_PICTURE_PARAMETER_SET_2
ShortName:	DSCA_PICTURE_PARAMETER_SET_2
Power:	PG1
Reset:	soft
Address:	6BA08h-6BA0Bh
Name:	DSCC_PICTURE_PARAMETER_SET_2
ShortName:	DSCC_PICTURE_PARAMETER_SET_2
Power:	PG1
Reset:	soft
Address:	78278h-7827Bh
Name:	DSC0_PICTURE_PARAMETER_SET_2_PB
ShortName:	DSC0_PICTURE_PARAMETER_SET_2_PB
Power:	PG3
Reset:	soft
Address:	78378h-7837Bh
Name:	DSC1_PICTURE_PARAMETER_SET_2_PB
ShortName:	DSC1_PICTURE_PARAMETER_SET_2_PB
Power:	PG3
Reset:	soft
Address:	78478h-7847Bh
Name:	DSC0_PICTURE_PARAMETER_SET_2_PC
ShortName:	DSC0_PICTURE_PARAMETER_SET_2_PC

DSC_PICTURE_PARAMETER_SET_2

Power:	PG4
Reset:	soft
Address:	78578h-7857Bh
Name:	DSC1_PICTURE_PARAMETER_SET_2_PC
ShortName:	DSC1_PICTURE_PARAMETER_SET_2_PC
Power:	PG4
Reset:	soft

DWord	Bit	Description
0	31:16	**pic_width** Access: Double Buffered On a single pipe if we are using 1 VDSC instance, picture_width of that VDSC instance = input frame picture_width. On a single pipe if we are using 2 VDSC instances, picture_width of each instance =input frame picture_width divided by 2. In the casea full frame is processed by2*N VDSC instancesfromN pipes, picture_width of each instance = input framepicture_width divivded by 2*N.
	15:0	**pic_height** Access: Double Buffered This field is always programmed to input frame picture height.

DSC_PICTURE_PARAMETER_SET_3

DSC_PICTURE_PARAMETER_SET_3	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6B20Ch-6B20Fh
Name:	DSCA_PICTURE_PARAMETER_SET_3
ShortName:	DSCA_PICTURE_PARAMETER_SET_3
Power:	PG1
Reset:	soft
Address:	6BA0Ch-6BA0Fh
Name:	DSCC_PICTURE_PARAMETER_SET_3
ShortName:	DSCC_PICTURE_PARAMETER_SET_3
Power:	PG1
Reset:	soft
Address:	7827Ch-7827Fh
Name:	DSC0_PICTURE_PARAMETER_SET_3_PB
ShortName:	DSC0_PICTURE_PARAMETER_SET_3_PB
Power:	PG3
Reset:	soft
Address:	7837Ch-7837Fh
Name:	DSC1_PICTURE_PARAMETER_SET_3_PB
ShortName:	DSC1_PICTURE_PARAMETER_SET_3_PB
Power:	PG3
Reset:	soft
Address:	7847Ch-7847Fh
Name:	DSC0_PICTURE_PARAMETER_SET_3_PC
ShortName:	DSC0_PICTURE_PARAMETER_SET_3_PC

DSC_PICTURE_PARAMETER_SET_3

Power:	PG4
Reset:	soft

Address:	7857Ch-7857Fh
Name:	DSC1_PICTURE_PARAMETER_SET_3_PC
ShortName:	DSC1_PICTURE_PARAMETER_SET_3_PC
Power:	PG4
Reset:	soft

DWord	Bit	Description
0	31:16	**slice_width** Access: R/W This defines the width of the slice in number of pixels.
	15:0	**slice_height** Access: R/W This defines the height of the slice in number of pixels.

DSC_PICTURE_PARAMETER_SET_4

DSC_PICTURE_PARAMETER_SET_4	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6B210h-6B213h
Name:	DSCA_PICTURE_PARAMETER_SET_4
ShortName:	DSCA_PICTURE_PARAMETER_SET_4
Power:	PG1
Reset:	soft
Address:	6BA10h-6BA13h
Name:	DSCC_PICTURE_PARAMETER_SET_4
ShortName:	DSCC_PICTURE_PARAMETER_SET_4
Power:	PG1
Reset:	soft
Address:	78280h-78283h
Name:	DSC0_PICTURE_PARAMETER_SET_4_PB
ShortName:	DSC0_PICTURE_PARAMETER_SET_4_PB
Power:	PG1
Reset:	soft
Address:	78380h-78383h
Name:	DSC1_PICTURE_PARAMETER_SET_4_PB
ShortName:	DSC1_PICTURE_PARAMETER_SET_4_PB
Power:	PG1
Reset:	soft
Address:	78480h-78483h
Name:	DSC0_PICTURE_PARAMETER_SET_4_PC
ShortName:	DSC0_PICTURE_PARAMETER_SET_4_PC

DSC_PICTURE_PARAMETER_SET_4

Power:	PG1
Reset:	soft
Address:	78580h-78583h
Name:	DSC1_PICTURE_PARAMETER_SET_4_PC
ShortName:	DSC1_PICTURE_PARAMETER_SET_4_PC
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:16	**initial_dec_delay** Access: R/W
	15:10	**RESERVED** Format: MBZ
	9:0	**initial_xmit_delay** Access: R/W

DSC_PICTURE_PARAMETER_SET_5

DSC_PICTURE_PARAMETER_SET_5	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6B214h-6B217h
Name:	DSCA_PICTURE_PARAMETER_SET_5
ShortName:	DSCA_PICTURE_PARAMETER_SET_5
Power:	PG1
Reset:	soft
Address:	6BA14h-6BA17h
Name:	DSCC_PICTURE_PARAMETER_SET_5
ShortName:	DSCC_PICTURE_PARAMETER_SET_5
Power:	PG1
Reset:	soft
Address:	78284h-78287h
Name:	DSC0_PICTURE_PARAMETER_SET_5_PB
ShortName:	DSC0_PICTURE_PARAMETER_SET_5_PB
Power:	PG3
Reset:	soft
Address:	78384h-78387h
Name:	DSC1_PICTURE_PARAMETER_SET_5_PB
ShortName:	DSC1_PICTURE_PARAMETER_SET_5_PB
Power:	PG3
Reset:	soft
Address:	78484h-78487h
Name:	DSC0_PICTURE_PARAMETER_SET_5_PC
ShortName:	DSC0_PICTURE_PARAMETER_SET_5_PC

DSC_PICTURE_PARAMETER_SET_5

Power:	PG4
Reset:	soft
Address:	78584h-78587h
Name:	DSC1_PICTURE_PARAMETER_SET_5_PC
ShortName:	DSC1_PICTURE_PARAMETER_SET_5_PC
Power:	PG4
Reset:	soft

DWord	Bit	Description
0	31:28	**RESERVED** Format: MBZ
	27:16	**scale_decrement_interval** Access: R/W
	15:0	**scale_increment_interval** Access: R/W

DSC_PICTURE_PARAMETER_SET_6

DSC_PICTURE_PARAMETER_SET_6	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6B218h-6B21Bh
Name:	DSCA_PICTURE_PARAMETER_SET_6
ShortName:	DSCA_PICTURE_PARAMETER_SET_6
Power:	PG1
Reset:	soft
Address:	6BA18h-6BA1Bh
Name:	DSCC_PICTURE_PARAMETER_SET_6
ShortName:	DSCC_PICTURE_PARAMETER_SET_6
Power:	PG1
Reset:	soft
Address:	78288h-7828Bh
Name:	DSC0_PICTURE_PARAMETER_SET_6_PB
ShortName:	DSC0_PICTURE_PARAMETER_SET_6_PB
Power:	PG3
Reset:	soft
Address:	78388h-7838Bh
Name:	DSC1_PICTURE_PARAMETER_SET_6_PB
ShortName:	DSC1_PICTURE_PARAMETER_SET_6_PB
Power:	PG3
Reset:	soft
Address:	78488h-7848Bh
Name:	DSC0_PICTURE_PARAMETER_SET_6_PC
ShortName:	DSC0_PICTURE_PARAMETER_SET_6_PC

DSC_PICTURE_PARAMETER_SET_6

Power:	PG4
Reset:	soft
Address:	78588h-7858Bh
Name:	DSC1_PICTURE_PARAMETER_SET_6_PC
ShortName:	DSC1_PICTURE_PARAMETER_SET_6_PC
Power:	PG4
Reset:	soft

DWord	Bit	Description
0	31:29	**RESERVED** Format: MBZ
	28:24	**flatness_max_qp** Access: R/W
	23:21	**RESERVED** Format: MBZ
	20:16	**flatness_min_qp** Access: R/W
	15:13	**RESERVED** Format: MBZ
	12:8	**first_line_bpg_offset** Access: R/W
	7:6	**RESERVED** Format: MBZ
	5:0	**initial_scale_value** Access: R/W Specifies the initial rcXformScale factor value used at the beginning of a slice. This is an unsigned field with three fractional bits.

DSC_PICTURE_PARAMETER_SET_7

DSC_PICTURE_PARAMETER_SET_7	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6B21Ch-6B21Fh
Name:	DSCA_PICTURE_PARAMETER_SET_7
ShortName:	DSCA_PICTURE_PARAMETER_SET_7
Power:	PG1
Reset:	soft
Address:	6BA1Ch-6BA1Fh
Name:	DSCC_PICTURE_PARAMETER_SET_7
ShortName:	DSCC_PICTURE_PARAMETER_SET_7
Power:	PG1
Reset:	soft
Address:	7828Ch-7828Fh
Name:	DSC0_PICTURE_PARAMETER_SET_7_PB
ShortName:	DSC0_PICTURE_PARAMETER_SET_7_PB
Power:	PG3
Reset:	soft
Address:	7838Ch-7838Fh
Name:	DSC1_PICTURE_PARAMETER_SET_7_PB
ShortName:	DSC1_PICTURE_PARAMETER_SET_7_PB
Power:	PG3
Reset:	soft
Address:	7848Ch-7848Fh
Name:	DSC0_PICTURE_PARAMETER_SET_7_PC
ShortName:	DSC0_PICTURE_PARAMETER_SET_7_PC

DSC_PICTURE_PARAMETER_SET_7

Power:	PG4
Reset:	soft
Address:	7858Ch-7858Fh
Name:	DSC1_PICTURE_PARAMETER_SET_7_PC
ShortName:	DSC1_PICTURE_PARAMETER_SET_7_PC
Power:	PG4
Reset:	soft

DWord	Bit	Description
0	31:16	**nfl_bpg_offset** Access: R/W Specifies the number of bits (including fractional bits) that are deallocated for each group, for groups after the first line of a slice. This is an unsigned value with 11 fractional bits.
	15:0	**slice_bpg_offset** Access: R/W Specifies the number of bits (including fractional bits) that are deallocated for each group to enforce the slice constraint (i.e., the final buffer model fullness cannot exceed the initial transmission delay times bits per group), while allowing a programmable initial_offset. This is an unsigned value with 11 fractional bits.

DSC_PICTURE_PARAMETER_SET_8

DSC_PICTURE_PARAMETER_SET_8	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6B220h-6B223h
Name:	DSCA_PICTURE_PARAMETER_SET_8
ShortName:	DSCA_PICTURE_PARAMETER_SET_8
Power:	PG1
Reset:	soft
Address:	6BA20h-6BA23h
Name:	DSCC_PICTURE_PARAMETER_SET_8
ShortName:	DSCC_PICTURE_PARAMETER_SET_8
Power:	PG1
Reset:	soft
Address:	78290h-78293h
Name:	DSC0_PICTURE_PARAMETER_SET_8_PB
ShortName:	DSC0_PICTURE_PARAMETER_SET_8_PB
Power:	PG3
Reset:	soft
Address:	78390h-78393h
Name:	DSC1_PICTURE_PARAMETER_SET_8_PB
ShortName:	DSC1_PICTURE_PARAMETER_SET_8_PB
Power:	PG3
Reset:	soft
Address:	78490h-78493h
Name:	DSC0_PICTURE_PARAMETER_SET_8_PC
ShortName:	DSC0_PICTURE_PARAMETER_SET_8_PC

DSC_PICTURE_PARAMETER_SET_8

Power:	PG4
Reset:	soft
Address:	78590h-78593h
Name:	DSC1_PICTURE_PARAMETER_SET_8_PC
ShortName:	DSC1_PICTURE_PARAMETER_SET_8_PC
Power:	PG4
Reset:	soft

DWord	Bit	Description
0	31:16	**initial_offset** Access: R/W
	15:0	**final_offset** Access: R/W

DSC_PICTURE_PARAMETER_SET_9

DSC_PICTURE_PARAMETER_SET_9	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6B224h-6B227h
Name:	DSCA_PICTURE_PARAMETER_SET_9
ShortName:	DSCA_PICTURE_PARAMETER_SET_9
Power:	PG1
Reset:	soft
Address:	6BA24h-6BA27h
Name:	DSCC_PICTURE_PARAMETER_SET_9
ShortName:	DSCC_PICTURE_PARAMETER_SET_9
Power:	PG1
Reset:	soft
Address:	78294h-78297h
Name:	DSC0_PICTURE_PARAMETER_SET_9_PB
ShortName:	DSC0_PICTURE_PARAMETER_SET_9_PB
Power:	PG3
Reset:	soft
Address:	78394h-78397h
Name:	DSC1_PICTURE_PARAMETER_SET_9_PB
ShortName:	DSC1_PICTURE_PARAMETER_SET_9_PB
Power:	PG3
Reset:	soft
Address:	78494h-78497h
Name:	DSC0_PICTURE_PARAMETER_SET_9_PC
ShortName:	DSC0_PICTURE_PARAMETER_SET_9_PC

DSC_PICTURE_PARAMETER_SET_9

Power:	PG4
Reset:	soft
Address:	78594h-78597h
Name:	DSC1_PICTURE_PARAMETER_SET_9_PC
ShortName:	DSC1_PICTURE_PARAMETER_SET_9_PC
Power:	PG4
Reset:	soft

DWord	Bit	Description
0	31:20	**RESERVED** Format: MBZ
	19:16	**rc_edge_factor** Access: R/W
	15:0	**rc_model_Size** Access: R/W

DSC_PICTURE_PARAMETER_SET_10

DSC_PICTURE_PARAMETER_SET_10	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6B228h-6B22Bh
Name:	DSCA_PICTURE_PARAMETER_SET_10
ShortName:	DSCA_PICTURE_PARAMETER_SET_10
Power:	PG1
Reset:	soft
Address:	6BA28h-6BA2Bh
Name:	DSCC_PICTURE_PARAMETER_SET_10
ShortName:	DSCC_PICTURE_PARAMETER_SET_10
Power:	PG1
Reset:	soft
Address:	78298h-7829Bh
Name:	DSC0_PICTURE_PARAMETER_SET_10_PB
ShortName:	DSC0_PICTURE_PARAMETER_SET_10_PB
Power:	PG1
Reset:	soft
Address:	78398h-7839Bh
Name:	DSC1_PICTURE_PARAMETER_SET_10_PB
ShortName:	DSC1_PICTURE_PARAMETER_SET_10_PB
Power:	PG1
Reset:	soft
Address:	78498h-7849Bh
Name:	DSC0_PICTURE_PARAMETER_SET_10_PC
ShortName:	DSC0_PICTURE_PARAMETER_SET_10_PC

DSC_PICTURE_PARAMETER_SET_10

Power:	PG1
Reset:	soft
Address:	78598h-7859Bh
Name:	DSC1_PICTURE_PARAMETER_SET_10_PC
ShortName:	DSC1_PICTURE_PARAMETER_SET_10_PC
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:24	**RESERVED** Format: MBZ
	23:20	**rc_tgt_offset_lo** Access: R/W
	19:16	**rc_tgt_offset_hi** Access: R/W
	15:13	**RESERVED** Format: MBZ
	12:8	**rc_quant_incr_limit1** Access: R/W
	7:5	**RESERVED** Format: MBZ
	4:0	**rc_quant_incr_limit0** Access: R/W

DSC_PICTURE_PARAMETER_SET_11

DSC_PICTURE_PARAMETER_SET_11	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6B22Ch-6B22Fh
Name:	DSCA_PICTURE_PARAMETER_SET_11
ShortName:	DSCA_PICTURE_PARAMETER_SET_11
Power:	PG1
Reset:	soft
Address:	6BA2Ch-6BA2Fh
Name:	DSCC_PICTURE_PARAMETER_SET_11
ShortName:	DSCC_PICTURE_PARAMETER_SET_11
Power:	PG1
Reset:	soft
Address:	7829Ch-7829Fh
Name:	DSC0_PICTURE_PARAMETER_SET_11_PB
ShortName:	DSC0_PICTURE_PARAMETER_SET_11_PB
Power:	PG3
Reset:	soft
Address:	7839Ch-7839Fh
Name:	DSC1_PICTURE_PARAMETER_SET_11_PB
ShortName:	DSC1_PICTURE_PARAMETER_SET_11_PB
Power:	PG3
Reset:	soft
Address:	7849Ch-7849Fh
Name:	DSC0_PICTURE_PARAMETER_SET_11_PC
ShortName:	DSC0_PICTURE_PARAMETER_SET_11_PC

DSC_PICTURE_PARAMETER_SET_11

Power:	PG4
Reset:	soft
Address:	7859Ch-7859Fh
Name:	DSC1_PICTURE_PARAMETER_SET_11_PC
ShortName:	DSC1_PICTURE_PARAMETER_SET_11_PC
Power:	PG4
Reset:	soft

DWord	Bit	Description
0	31:0	**RESERVED** Format: MBZ

DSC_PICTURE_PARAMETER_SET_12

DSC_PICTURE_PARAMETER_SET_12	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6B260h-6B263h
Name:	DSCA_PICTURE_PARAMETER_SET_12
ShortName:	DSCA_PICTURE_PARAMETER_SET_12
Power:	PG1
Reset:	soft
Address:	6BA60h-6BA63h
Name:	DSCC_PICTURE_PARAMETER_SET_12
ShortName:	DSCC_PICTURE_PARAMETER_SET_12
Power:	PG1
Reset:	soft
Address:	782A0h-782A3h
Name:	DSC0_PICTURE_PARAMETER_SET_12_PB
ShortName:	DSC0_PICTURE_PARAMETER_SET_12_PB
Power:	PG3
Reset:	soft
Address:	783A0h-783A3h
Name:	DSC1_PICTURE_PARAMETER_SET_12_PB
ShortName:	DSC1_PICTURE_PARAMETER_SET_12_PB
Power:	PG3
Reset:	soft
Address:	784A0h-784A3h
Name:	DSC0_PICTURE_PARAMETER_SET_12_PC
ShortName:	DSC0_PICTURE_PARAMETER_SET_12_PC

DSC_PICTURE_PARAMETER_SET_12

Power:	PG4
Reset:	soft
Address:	785A0h-785A3h
Name:	DSC1_PICTURE_PARAMETER_SET_12_PC
ShortName:	DSC1_PICTURE_PARAMETER_SET_12_PC
Power:	PG4
Reset:	soft

DWord	Bit	Description
0	31:0	**RESERVED** Format: MBZ

DSC_PICTURE_PARAMETER_SET_13

DSC_PICTURE_PARAMETER_SET_13	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6B264h-6B267h
Name:	DSCA_PICTURE_PARAMETER_SET_13
ShortName:	DSCA_PICTURE_PARAMETER_SET_13
Power:	PG1
Reset:	soft
Address:	6BA64h-6BA67h
Name:	DSCC_PICTURE_PARAMETER_SET_13
ShortName:	DSCC_PICTURE_PARAMETER_SET_13
Power:	PG1
Reset:	soft
Address:	782A4h-782A7h
Name:	DSC0_PICTURE_PARAMETER_SET_13_PB
ShortName:	DSC0_PICTURE_PARAMETER_SET_13_PB
Power:	PG3
Reset:	soft
Address:	783A4h-783A7h
Name:	DSC1_PICTURE_PARAMETER_SET_13_PB
ShortName:	DSC1_PICTURE_PARAMETER_SET_13_PB
Power:	PG3
Reset:	soft
Address:	784A4h-784A7h
Name:	DSC0_PICTURE_PARAMETER_SET_13_PC
ShortName:	DSC0_PICTURE_PARAMETER_SET_13_PC

DSC_PICTURE_PARAMETER_SET_13

Power:	PG4
Reset:	soft
Address:	785A4h-785A7h
Name:	DSC1_PICTURE_PARAMETER_SET_13_PC
ShortName:	DSC1_PICTURE_PARAMETER_SET_13_PC
Power:	PG4
Reset:	soft

DWord	Bit	Description
0	31:0	**RESERVED** Format: MBZ

DSC_PICTURE_PARAMETER_SET_14

DSC_PICTURE_PARAMETER_SET_14	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6B268h-6B26Bh
Name:	DSCA_PICTURE_PARAMETER_SET_14
ShortName:	DSCA_PICTURE_PARAMETER_SET_14
Power:	PG1
Reset:	soft
Address:	6BA68h-6BA6Bh
Name:	DSCC_PICTURE_PARAMETER_SET_14
ShortName:	DSCC_PICTURE_PARAMETER_SET_14
Power:	PG1
Reset:	soft
Address:	782A8h-782ABh
Name:	DSC0_PICTURE_PARAMETER_SET_14_PB
ShortName:	DSC0_PICTURE_PARAMETER_SET_14_PB
Power:	PG3
Reset:	soft
Address:	783A8h-783ABh
Name:	DSC1_PICTURE_PARAMETER_SET_14_PB
ShortName:	DSC1_PICTURE_PARAMETER_SET_14_PB
Power:	PG3
Reset:	soft
Address:	784A8h-784ABh
Name:	DSC0_PICTURE_PARAMETER_SET_14_PC
ShortName:	DSC0_PICTURE_PARAMETER_SET_14_PC

DSC_PICTURE_PARAMETER_SET_14

Power:	PG4
Reset:	soft
Address:	785A8h-785ABh
Name:	DSC1_PICTURE_PARAMETER_SET_14_PC
ShortName:	DSC1_PICTURE_PARAMETER_SET_14_PC
Power:	PG4
Reset:	soft

DWord	Bit	Description
0	31:0	**RESERVED** Format: MBZ

DSC_PICTURE_PARAMETER_SET_15

DSC_PICTURE_PARAMETER_SET_15	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6B26Ch-6B26Fh
Name:	DSCA_PICTURE_PARAMETER_SET_15
ShortName:	DSCA_PICTURE_PARAMETER_SET_15
Power:	PG1
Reset:	soft
Address:	6BA6Ch-6BA6Fh
Name:	DSCC_PICTURE_PARAMETER_SET_15
ShortName:	DSCC_PICTURE_PARAMETER_SET_15
Power:	PG1
Reset:	soft
Address:	782ACh-782AFh
Name:	DSC0_PICTURE_PARAMETER_SET_15_PB
ShortName:	DSC0_PICTURE_PARAMETER_SET_15_PB
Power:	PG3
Reset:	soft
Address:	783ACh-783AFh
Name:	DSC1_PICTURE_PARAMETER_SET_15_PB
ShortName:	DSC1_PICTURE_PARAMETER_SET_15_PB
Power:	PG3
Reset:	soft
Address:	784ACh-784AFh
Name:	DSC0_PICTURE_PARAMETER_SET_15_PC
ShortName:	DSC0_PICTURE_PARAMETER_SET_15_PC

DSC_PICTURE_PARAMETER_SET_15

Power:	PG4
Reset:	soft
Address:	785ACh-785AFh
Name:	DSC1_PICTURE_PARAMETER_SET_15_PC
ShortName:	DSC1_PICTURE_PARAMETER_SET_15_PC
Power:	PG4
Reset:	soft

DWord	Bit	Description
0	31:0	**RESERVED** Format: MBZ

DSC_PICTURE_PARAMETER_SET_16

DSC_PICTURE_PARAMETER_SET_16	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6B270h-6B273h
Name:	DSCA_PICTURE_PARAMETER_SET_16
ShortName:	DSCA_PICTURE_PARAMETER_SET_16
Power:	PG1
Reset:	soft
Address:	6BA70h-6BA73h
Name:	DSCC_PICTURE_PARAMETER_SET_16
ShortName:	DSCC_PICTURE_PARAMETER_SET_16
Power:	PG1
Reset:	soft
Address:	782B0h-782B3h
Name:	DSC0_PICTURE_PARAMETER_SET_16_PB
ShortName:	DSC0_PICTURE_PARAMETER_SET_16_PB
Power:	PG3
Reset:	soft
Address:	783B0h-783B3h
Name:	DSC1_PICTURE_PARAMETER_SET_16_PB
ShortName:	DSC1_PICTURE_PARAMETER_SET_16_PB
Power:	PG3
Reset:	soft
Address:	784B0h-784B3h
Name:	DSC0_PICTURE_PARAMETER_SET_16_PC
ShortName:	DSC0_PICTURE_PARAMETER_SET_16_PC

DSC_PICTURE_PARAMETER_SET_16

Power:	PG4
Reset:	soft
Address:	785B0h-785B3h
Name:	DSC1_PICTURE_PARAMETER_SET_16_PC
ShortName:	DSC1_PICTURE_PARAMETER_SET_16_PC
Power:	PG4
Reset:	soft

DWord	Bit	Description
0	31:20	**slice_row_per_frame** Access: Double Buffered This is the field driver will program to indicate slice_row_per_frame for full frame. There is another field in DSC_PICTURE_PARAMETER_SET_1 to indicate slice_row_per_framebased onPSR2 SU region size. This field indicates number of slices stacked in the vertical direction. Example: Input to DSS unit: 3840x2160 to be compressed as 4 slices Input to each VDSC instance: 1920x2160 slice_per_line: 1 slice_row_per_frame: 2
	19	**RESERVED** Format: MBZ
	18:16	**slice_per_line** Access: R/W Refer to the description under slice_row_per_frame.
	15:0	**slice_chunk_size** Access: R/W

DSC_RC_BUF_THRESH_0

DSC_RC_BUF_THRESH_0	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	64
Address:	6B230h-6B237h
Name:	DSCA_RC_BUF_THRESH_0
ShortName:	DSCA_RC_BUF_THRESH_0
Power:	PG1
Reset:	soft
Address:	6BA30h-6BA37h
Name:	DSCC_RC_BUF_THRESH_0
ShortName:	DSCC_RC_BUF_THRESH_0
Power:	PG1
Reset:	soft
Address:	78254h-7825Bh
Name:	DSC0_RC_BUF_THRESH_0_PB
ShortName:	DSC0_RC_BUF_THRESH_0_PB
Power:	PG3
Reset:	soft
Address:	78354h-7835Bh
Name:	DSC1_RC_BUF_THRESH_0_PB
ShortName:	DSC1_RC_BUF_THRESH_0_PB
Power:	PG3
Reset:	soft
Address:	78454h-7845Bh
Name:	DSC0_RC_BUF_THRESH_0_PC
ShortName:	DSC0_RC_BUF_THRESH_0_PC

DSC_RC_BUF_THRESH_0

Power:	PG4
Reset:	soft
Address:	78554h-7855Bh
Name:	DSC1_RC_BUF_THRESH_0_PC
ShortName:	DSC1_RC_BUF_THRESH_0_PC
Power:	PG4
Reset:	soft

DWord	Bit	Description
0	31:24	**rc_buf_thresh_3** Access: R/W
	23:16	**rc_buf_thresh_2** Access: R/W
	15:8	**rc_buf_thresh_1** Access: R/W
	7:0	**rc_buf_thresh_0** Access: R/W
1	31:24	**rc_buf_thresh_7** Access: R/W
	23:16	**rc_buf_thresh_6** Access: R/W
	15:8	**rc_buf_thresh_5** Access: R/W
	7:0	**rc_buf_thresh_4** Access: R/W

DSC_RC_BUF_THRESH_1

DSC_RC_BUF_THRESH_1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	64
Address:	6B238h-6B23Fh
Name:	DSCA_RC_BUF_THRESH_1
ShortName:	DSCA_RC_BUF_THRESH_1
Power:	PG1
Reset:	soft
Address:	6BA38h-6BA3Fh
Name:	DSCC_RC_BUF_THRESH_1
ShortName:	DSCC_RC_BUF_THRESH_1
Power:	PG1
Reset:	soft
Address:	7825Ch-78263h
Name:	DSC0_RC_BUF_THRESH_1_PB
ShortName:	DSC0_RC_BUF_THRESH_1_PB
Power:	PG3
Reset:	soft
Address:	7835Ch-78363h
Name:	DSC1_RC_BUF_THRESH_1_PB
ShortName:	DSC1_RC_BUF_THRESH_1_PB
Power:	PG3
Reset:	soft
Address:	7845Ch-78463h
Name:	DSC0_RC_BUF_THRESH_1_PC
ShortName:	DSC0_RC_BUF_THRESH_1_PC

DSC_RC_BUF_THRESH_1

Power:	PG4
Reset:	soft
Address:	7855Ch-78563h
Name:	DSC1_RC_BUF_THRESH_1_PC
ShortName:	DSC1_RC_BUF_THRESH_1_PC
Power:	PG4
Reset:	soft

DWord	Bit	Description
0	31:24	**rc_buf_thresh_11** Access: R/W
	23:16	**rc_buf_thresh_10** Access: R/W
	15:8	**rc_buf_thresh_9** Access: R/W
	7:0	**rc_buf_thresh_8** Access: R/W
1	31:16	**RESERVED** Format: MBZ
	15:8	**rc_buf_thresh_13** Access: R/W
	7:0	**rc_buf_thresh_12** Access: R/W

DSC_RC_RANGE_PARAMETERS_0

DSC_RC_RANGE_PARAMETERS_0	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	64
Address:	6B240h-6B247h
Name:	DSCA_RC_RANGE_PARAMETERS_0
ShortName:	DSCA_RC_RANGE_PARAMETERS_0
Power:	PG1
Reset:	soft
Address:	6BA40h-6BA47h
Name:	DSCC_RC_RANGE_PARAMETERS_0
ShortName:	DSCC_RC_RANGE_PARAMETERS_0
Power:	PG1
Reset:	soft
Address:	78208h-7820Fh
Name:	DSC0_RC_RANGE_PARAMETERS_0_PB
ShortName:	DSC0_RC_RANGE_PARAMETERS_0_PB
Power:	PG3
Reset:	soft
Address:	78308h-7830Fh
Name:	DSC1_RC_RANGE_PARAMETERS_0_PB
ShortName:	DSC1_RC_RANGE_PARAMETERS_0_PB
Power:	PG3
Reset:	soft
Address:	78408h-7840Fh
Name:	DSC0_RC_RANGE_PARAMETERS_0_PC
ShortName:	DSC0_RC_RANGE_PARAMETERS_0_PC

DSC_RC_RANGE_PARAMETERS_0

Power:	PG4
Reset:	soft
Address:	78508h-7850Fh
Name:	DSC1_RC_RANGE_PARAMETERS_0_PC
ShortName:	DSC1_RC_RANGE_PARAMETERS_0_PC
Power:	PG4
Reset:	soft

DWord	Bit	Description
0	31:26	**rc_bpg_offset_1** Access: R/W
	25:21	**rc_max_qp_1**
	20:16	**rc_min_qp_1**
	15:10	**rc_bpg_offset_0** Access: R/W
	9:5	**rc_max_qp_0**
	4:0	**rc_min_qp_0**
1	31:26	**rc_bpg_offset_3** Access: R/W
	25:21	**rc_max_qp_3**
	20:16	**rc_min_qp_3**
	15:10	**rc_bpg_offset_2** Access: R/W
	9:5	**rc_max_qp_2**
	4:0	**rc_min_qp_2**

DSC_RC_RANGE_PARAMETERS_1

DSC_RC_RANGE_PARAMETERS_1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	64
Address:	6B248h-6B24Fh
Name:	DSCA_RC_RANGE_PARAMETERS_1
ShortName:	DSCA_RC_RANGE_PARAMETERS_1
Power:	PG1
Reset:	soft
Address:	6BA48h-6BA4Fh
Name:	DSCC_RC_RANGE_PARAMETERS_1
ShortName:	DSCC_RC_RANGE_PARAMETERS_1
Power:	PG1
Reset:	soft
Address:	78210h-78217h
Name:	DSC0_RC_RANGE_PARAMETERS_1_PB
ShortName:	DSC0_RC_RANGE_PARAMETERS_1_PB
Power:	PG3
Reset:	soft
Address:	78310h-78317h
Name:	DSC1_RC_RANGE_PARAMETERS_1_PB
ShortName:	DSC1_RC_RANGE_PARAMETERS_1_PB
Power:	PG3
Reset:	soft
Address:	78410h-78417h
Name:	DSC0_RC_RANGE_PARAMETERS_1_PC
ShortName:	DSC0_RC_RANGE_PARAMETERS_1_PC

DSC_RC_RANGE_PARAMETERS_1

Power:	PG4
Reset:	soft
Address:	78510h-78517h
Name:	DSC1_RC_RANGE_PARAMETERS_1_PC
ShortName:	DSC1_RC_RANGE_PARAMETERS_1_PC
Power:	PG4
Reset:	soft

DWord	Bit	Description
0	31:26	**rc_bpg_offset_5** Access: R/W
	25:21	**rc_max_qp_5**
	20:16	**rc_min_qp_5**
	15:10	**rc_bpg_offset_4** Access: R/W
	9:5	**rc_max_qp_4**
	4:0	**rc_min_qp_4**
1	31:26	**rc_bpg_offset_7** Access: R/W
	25:21	**rc_max_qp_7**
	20:16	**rc_min_qp_7**
	15:10	**rc_bpg_offset_6** Access: R/W
	9:5	**rc_max_qp_6**
	4:0	**rc_min_qp_6**

DSC_RC_RANGE_PARAMETERS_2

DSC_RC_RANGE_PARAMETERS_2	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	64
Address:	6B250h-6B257h
Name:	DSCA_RC_RANGE_PARAMETERS_2
ShortName:	DSCA_RC_RANGE_PARAMETERS_2
Power:	PG1
Reset:	soft
Address:	6BA50h-6BA57h
Name:	DSCC_RC_RANGE_PARAMETERS_2
ShortName:	DSCC_RC_RANGE_PARAMETERS_2
Power:	PG1
Reset:	soft
Address:	78218h-7821Fh
Name:	DSC0_RC_RANGE_PARAMETERS_2_PB
ShortName:	DSC0_RC_RANGE_PARAMETERS_2_PB
Power:	PG3
Reset:	soft
Address:	78318h-7831Fh
Name:	DSC1_RC_RANGE_PARAMETERS_2_PB
ShortName:	DSC1_RC_RANGE_PARAMETERS_2_PB
Power:	PG3
Reset:	soft
Address:	78418h-7841Fh
Name:	DSC0_RC_RANGE_PARAMETERS_2_PC
ShortName:	DSC0_RC_RANGE_PARAMETERS_2_PC

DSC_RC_RANGE_PARAMETERS_2

Power:	PG4
Reset:	soft
Address:	78518h-7851Fh
Name:	DSC1_RC_RANGE_PARAMETERS_2_PC
ShortName:	DSC1_RC_RANGE_PARAMETERS_2_PC
Power:	PG4
Reset:	soft

DWord	Bit	Description
0	31:26	**rc_bpg_offset_9** Access: R/W
	25:21	**rc_max_qp_9**
	20:16	**rc_min_qp_9**
	15:10	**rc_bpg_offset_8** Access: R/W
	9:5	**rc_max_qp_8**
	4:0	**rc_min_qp_8**
1	31:26	**rc_bpg_offset_11** Access: R/W
	25:21	**rc_max_qp_11**
	20:16	**rc_min_qp_11**
	15:10	**rc_bpg_offset_10** Access: R/W
	9:5	**rc_max_qp_10**
	4:0	**rc_min_qp_10**

DSC_RC_RANGE_PARAMETERS_3

DSC_RC_RANGE_PARAMETERS_3	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	64
Address:	6B258h-6B25Fh
Name:	DSCA_RC_RANGE_PARAMETERS_3
ShortName:	DSCA_RC_RANGE_PARAMETERS_3
Power:	PG1
Reset:	soft
Address:	6BA58h-6BA5Fh
Name:	DSCC_RC_RANGE_PARAMETERS_3
ShortName:	DSCC_RC_RANGE_PARAMETERS_3
Power:	PG1
Reset:	soft
Address:	78220h-78227h
Name:	DSC0_RC_RANGE_PARAMETERS_3_PB
ShortName:	DSC0_RC_RANGE_PARAMETERS_3_PB
Power:	PG3
Reset:	soft
Address:	78320h-78327h
Name:	DSC1_RC_RANGE_PARAMETERS_3_PB
ShortName:	DSC1_RC_RANGE_PARAMETERS_3_PB
Power:	PG3
Reset:	soft
Address:	78420h-78427h
Name:	DSC0_RC_RANGE_PARAMETERS_3_PC
ShortName:	DSC0_RC_RANGE_PARAMETERS_3_PC

DSC_RC_RANGE_PARAMETERS_3

Power:	PG4
Reset:	soft
Address:	78520h-78527h
Name:	DSC1_RC_RANGE_PARAMETERS_3_PC
ShortName:	DSC1_RC_RANGE_PARAMETERS_3_PC
Power:	PG4
Reset:	soft

DWord	Bit	Description
0	31:26	**rc_bpg_offset_13** Access: R/W
	25:21	**rc_max_qp_13**
	20:16	**rc_min_qp_13**
	15:10	**rc_bpg_offset_12** Access: R/W
	9:5	**rc_max_qp_12**
	4:0	**rc_min_qp_12**
1	31:26	**Reserved**
	25:21	**Reserved**
	20:16	**Reserved**
	15:10	**rc_bpg_offset_14** Access: R/W
	9:5	**rc_max_qp_14**
	4:0	**rc_min_qp_14**

DSI_CALIB_TO

DSI_CALIB_TO

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	6B050h-6B053h
Name:	DSI 0 Calibration Timeout
ShortName:	DSI_CALIB_TO_0
Power:	PG1
Reset:	soft
Address:	6B850h-6B853h
Name:	DSI 1 Calibration Timeout
ShortName:	DSI_CALIB_TO_1
Power:	PG1
Reset:	soft

This register specifies the amount of time that the Host will drive the Link with the HS calibration sequence. The values are specified in Byte clocks and the values specified should be zero based (i.e. value of 1 = 2 Byte clocks, value of 2 = 3 Byte clocks, etc)

Restriction : The timeout values should be greater than zero if the respective calibration type is enabled.

DWord	Bit	Description
0	31:20	**Periodic Calibration Timeout** Default Value: 07Fh Access: R/W This field represents the amount of time that the Host will give to transmitting the HS calibration sequence for Periodic Calibrations. The transcoder will ignore this field if Periodic Calibration is not enabled within the TRANS_DSI_FUNC_CONF register. The default value will be set to 128 Byte clocks Restriction : When periodic calibration is enabled in Video Mode, the Horizontal size between synchronous packets must be great enough to support the HS calibration burst without the loss of synchronous packets. Software will need to ensure that the following equation is met to prevent synchronization packet loss: Periodic Calib Duration < (H. Size * Bits per Pixel) / (Link Width * 8) – 16*N Notes: 1. The "H. Size" term is dependent on the mode of operation (i.e. Sync Pulse or Sync Event).

		In Sync Pulse, H. Size = H. Sync Start + (H. Total – H. Sync End). In Sync Event, H. Size = H. Total. 2. HS bursts and calibrations cannot be concatenated together on Data Lanes which means the Data Lanes have to enter the LP state on either end of the calibration. The "16*N" term within the equation is used to account for the HS to HS latency of transitioning the Data Lanes on either end of the calibration.The variable N is the number of Byte clocks within an Escape clock (N = ceiling(((8X Frequency (in MHz) / 20 MHz) / 8))
	19:16	**Reserved**
	15:0	**Initial Calibration Timeout** Default Value: 0FFFh Access: R/W This field represents the amount of time the Host will give to transmitting the HS calibration sequence for the Initial Calibration, if enabled. The transcoder will ignore this field if Calibration is not enabled within the TRANS_DSI_FUNC_CONF register. The default value will be set to 4096 Byte clocks

DSI_CLK_TIMING_PARAM

DSI_CLK_TIMING_PARAM

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6B080h-6B083h
Name:	DSI 0 Clock Lane Timing Parameter
ShortName:	DSI_CLK_TIMING_PARAM_0
Power:	PG1
Reset:	soft
Address:	6B880h-6B883h
Name:	DSI 1 Clock Lane Timing Parameter
ShortName:	DSI_CLK_TIMING_PARAM_1
Power:	PG1
Reset:	soft

This register specifies the D-PHY timing parameters for the Clock Lane, if SW is overriding the HW defaults.
This register is located within the Core Display and is used by the DSI Controller to calculate Link transition latencies of the Clock Lane. There is an identical register (DPHY_CLK_TIMING_PARAM) located within the combo-PHY that actually applies the overrides to the D-PHY Clock Lane. Both registers should be programmed by Software if an override needs to be applied to the Clock Lane within the D-PHY.
Since this register is being used to calculate the Link transition latencies of the Clock Lane, but does not actually affect the transition times within the D-PHY, this register can be used to add guardbands to the DSI Controller's transition latency calculations.
The lower 12 bits of the offset address for this register should correspond to the lower offset address of its sister D-PHY register within the combo-PHY.
All fields are defined in number of Escape clocks.

Restriction
Overall restriction is that the timing parameters must be non-zero if SW is overriding the HW timing parameters. The programming of this register must be equal to or greater than the programming of it's sister register that lives within the combo-PHY (DPHY_CLK_TIMING_PARAM).

DWord	Bit	Description
0	31	**CLK_PREPARE Override** Access: R/W This field controls the override of the CLK-PREPARE timing parameter. Value: 0b — Name: HW maintains **[Default]**

DSI_CLK_TIMING_PARAM

	1b	SW overrides

30:28 CLK_PREPARE

Access:	R/W

This parameter defines the time that the Host drives the Clock Lane with the LP-00 Lane state (the Bridge state) immediately before the HS-0 Line state.
This field represents a hexadecimal value with a precision of 1.2 – i.e. the most significant bit is the integer and the least significant 2 bits are fraction bits. So, the field can represent a range of 0.25 to 1.75 (12.5ns to 87.5ns assuming an Escape clock with a 20MHz frequency)
HW maintains this timing parameter at 1 Escape clock (minimum 50ns)

Value	Name
001b	0.25 Escape clocks
010b	0.50 Escape clocks
011b	0.75 Escape clocks
100b	1.00 Escape clocks
101b	1.25 Escape clocks
110b	1.50 Escape clocks
111b	1.75 Escape clocks
Others	Reserved

Programming Notes
Caution: The MIPI D-PHY specification has a maximum of 95ns for this parameter.

27 CLK_ZERO Override

Access:	R/W

This field controls the override of the CLK-ZERO timing parameter

Value	Name
0	HW Maintains
1	SW overrides

26:24 Reserved

Format:	MBZ

23:20 CLK_ZERO

Access:	R/W

This parameter defines the time that the Host drives the HS-0 Lane state on the Clock Lane.
HW maintains this parameter at 5 Escape clocks (minimum 250ns)

19 CLK_PRE Override

Access:	R/W

This field controls the override of the CLK-PRE timing parameter.

Value	Name

DSI_CLK_TIMING_PARAM

	0	HW Maintains
	1	SW overrides

18 Reserved

Format:	MBZ

17:16 CLK_PRE

Access:	R/W

This parameter defines the time that the HS clock shall be driven by the Host prior to any Data Lane beginning its transition from the LP state to the HS state.
HW maintains this parameter at 8 UI (1 Byte clock). This field will override the parameter with a value measured in Escape clocks which will be much greater than 8 UI.

15 CLK_POST Override

Access:	R/W

This field controls the override of the CLK-POST timing parameter

Value	Name
0	HW Maintains
1	SW overrides

14:11 Reserved

Format:	MBZ

10:8 CLK_POST

Access:	R/W

This parameter defines the time the Host continues to transmit the HS clock after the last Data Lane has transitioned to the LP state.
HW maintains this parameter at 1.25 Escape clocks plus 7 Byte clocks (minimum 62.5ns + 56 UI)

7 CLK_TRAIL Override

Access:	R/W

This field controls the override of the CLK-TRAIL timing parameter

Value	Name
0	HW Maintains
1	SW overrides

6:3 Reserved

Format:	MBZ

2:0 CLK_TRAIL

Access:	R/W

This parameter defines the time that the Host drives the HS-0 Lane state on the Clock Lane after the CLK-POST time has been achieved.
HW maintains this parameter at 1.25 Escape clocks (minimum 62.5ns)

DSI_CMD_FRMCTL

DSI_CMD_FRMCTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6B034h-6B037h
Name:	DSI Transcoder 0 Command Mode Frame Control
ShortName:	DSI_CMD_FRMCTL_0
Power:	PG1
Reset:	soft
Address:	6B834h-6B837h
Name:	DSI Transcoder 1 Command Mode Frame Control
ShortName:	DSI_CMD_FRMCTL_1
Power:	PG1
Reset:	soft

This register is used to control initiating frame updates to the Peripheral in Command Mode
The fields within this register are only observed by the DSI transcoder when it is in the Command Mode of operation

DWord	Bit	Description
0	31	**Frame Update Request** Access: R/W Set This bit controls when the transcoder will start the next frame when it is in Command Mode. The transcoder will act on this bit only when it is in the Command Mode and the Transcoder is enabled (TRANS_CONF). Software can write to this bit, but Hardware will be responsible for clearing it. **Value** / **Name** 0b: No frame request present 1b: Frame request present
	30	**Reserved**
	29	**Periodic Frame Update Enable** Access: R/W When the Intel graphics driver is not present (e.g. the driver is uninstalled, the OS basic driver is present, or pre-boot time) there will be no frame update requests to the DSI transcoder through the Frame Update Request of this register. Therefore, this field will enable a mechanism that will

initiate periodic frame update requests when TE events are received from the Panel.
When enabling this feature, the expectation will be that SW has configured the Panel to send TE events to the Host (i.e. set_tear_on, etc.). HW will do the following when this bit is set:

1. It will override the TE Source bit of the TRANS_DSI_FUNC_CONF register to the GPIO setting. The DSI transcoder HW does not have a mechanism to automatically send Bus Turn-Around's to the Panel to receive in-band TE events
2. It will override the Mode of Operation of the TRANS_DSI_FUNC_CONF register to a non-gating Command Mode of operation

Value	Name
0b	Periodic Frame Update disabled
1b	Periodic Frame Update Enabled

Programming Notes

Note that when theTakeover MIPI DBI bit is set within the MSG_MEDE_KVMR_SPR_CTL register then HW will do the following if the DSI transcoder is operating in a Command Mode (i.e. DBI):

1. It will enable the Periodic Frame Update mode of operation
2. It will override the TE Source bit of the TRANS_DSI_FUNC_CONF register to the GPIO setting
3. It will override the Mode of Operation of the TRANS_DSI_FUNC_CONF register to a non-gating Command Mode of operation

If the DSI transcoder is not operating in a DBI mode, then the transcoder will ignore the Takeover MIPI DBI bit.

28 **Null Packet Enable**

Access:	R/W

This bit controls whether Null Packets will be transmitted between Pixel Packets in Command Mode operation.
If a Pixel Packet ends and the next Pixel Packet is within the transcoders pipeline but not visible to the HS arbiter, then the transcoder will begin transmitting Null Packet bursts to keep the Link in the HS state.
If the current Pixel Packet ends and the next Pixel Packet is not within the transcoders pipeline, then the transcoder will allow the Link to enter the LP state.
This field is ignored when the transcoder is operating in Video Mode.

Value	Name
0b	Null packet injection disabled
1b	Null packet injection enabled

27:1 **Reserved**

0 **Frame in Progress**

Access:	RO

DSI_CMD_FRMCTL		
		This bit reflects whether the DSI transcoder is currently processing/sending a frame to the Peripheral.

DSI_CMD_RXCTL

DSI_CMD_RXCTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6B0D4h-6B0D7h
Name:	DSI Transcoder 0 Command Receive Control
ShortName:	DSI_CMD_RXCTL_0
Power:	PG1
Reset:	soft
Address:	6B8D4h-6B8D7h
Name:	DSI Transcoder 1 Command Receive Control
ShortName:	DSI_CMD_RXCTL_1
Power:	PG1
Reset:	soft

This register controls how received DSI packets from the Peripheral are handled.

DWord	Bit	Description
0	31:17	**Reserved** Format: MBZ
	16	**Read Unloads DW** Access: R/W This bit controls whether the DSI_RXDATA register read unloads the DW from the transcoder's receive queue. If DSI_RXDATA reads do not unload the transcoder's receive queue, then the transcoder will continue to return the DW of data at the head of the queue. Otherwise, every read to the DSI_RXDATA will return a new DW of data. Value / Name: 0b – DSI_RXDATA reads do not unload DW 1b – DSI_RXDATA reads unload DW
	15	**Received Unassigned Trigger** Access: R/WC The unassigned trigger (10100000 [lsb on the left to the msb on the right]) has been received. Value / Name: 0b – Trigger message not received

DSI_CMD_RXCTL

	1b	Trigger message received

14 Received Acknowledge Trigger

Access:	R/WC

The Acknowledge trigger message (00100001 [lsb to msb]) has been received.

Value	Name
0b	Trigger message not received
1b	Trigger message received

13 Received Tear Effect Trigger

Access:	R/WC

The Tear Effect (TE) trigger message (01011101 [lsb to msb]) has been received.

Value	Name
0b	Trigger message not received
1b	Trigger message received

12 Received Reset Trigger

Access:	R/WC

The Reset trigger message (01100010 [lsb to msb]) has been received.
The Peripheral is not expected to send this trigger message to the Host, but even if it does, the hardware does not take any action on this message

Value	Name
0b	Trigger message not received
1b	Trigger message received

11 Received Payload was Lost

Access:	R/WC

This bit indicates if the DSI transcoder had to drop one or more of the payload bytes from a response packet being recieved from the Peripheral.
Software should check that the "Maximum Return Packet Size" programming is set correctly within the Peripheral

Value	Name
0b	No payload bytes dropped
1b	Payload bytes dropped

10 Received CRC was Lost

Access:	R/WC

When set, the DSI transcoder had to drop one or more of the CRC bytes from a response packet being received from the Peripheral.
If the "Received Payload was Lost" bit is set, then this bit will most likely also be set.
It is not imperative that the CRC is captured within the queue, so this is not an error but only a heads up that it may not be present.
If Software wishes the CRC to always be present within the Payload Receive queue, then it should adjust the "Maximum Return Packet Size" programming within the Peripheral to account for the

DSI_CMD_RXCTL

		CRC Value: 0b — Name: No CRC bytes dropped Value: 1b — Name: CRC bytes dropped
	9:8	**Reserved**
	7:0	**Number Rx Payload DW** Access: RO This field represents the number of DW's currently within the transcoder's Payload Receive queue. Note that the queue will be flushed at the beginning of a Bus Turn-Around (BTA) HW currently maintains an 8 DW queue.

DSI_CMD_RXHDR

DSI_CMD_RXHDR	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	6B0E0h-6B0E3h
Name:	DSI 0 Command Receive Header
ShortName:	DSI_CMD_RXHDR_0
Power:	PG1
Reset:	soft
Address:	6B8E0h-6B8E3h
Name:	DSI 1 Command Receive Header
ShortName:	DSI_CMD_RXHDR_1
Power:	PG1
Reset:	soft

This register reads the READ Response packet header received from the Periphery. This register is RO.

DWord	Bit	Description
0	31:0	**Received Header** Access: RO This field contains the READ Response packet haader received from the Periphery. Software can read this as many times as it wishes (i.e. the "Read Unloads DW" bit of the DSI_CMD_RXCTL has no effect on this data).

DSI_CMD_RXPYLD

DSI_CMD_RXPYLD	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	6B0E4h-6B0E7h
Name:	DSI 0 Command Receive Payload
ShortName:	DSI_CMD_RXPYLD_0
Power:	PG1
Reset:	soft
Address:	6B8E4h-6B8E7h
Name:	DSI 1 Command Receive Payload
ShortName:	DSI_CMD_RXPYLD_1
Power:	PG1
Reset:	soft

This register reads from the Receive Payload queue within the transcoder which contains the payload data of READ Response packets received from the Periphery. A read to this register will pull a DW of data from a receive queue within the DSI transcoder unless the DSI_CMD_RXCTL is programmed to prevent this. This register is RO.

DWord	Bit	Description
0	31:0	**Received Payload** Access: RO This field contains the READ Response payload data and CRC received from the Periphery. This data is taken from the head of the DSI transcoder's receive queue. If the "Read Unloads DW" bit of the DSI_CMD_RXCTL is set, then multiple reads to this register will return the same data (i.e. the data at the head of the receive queue). If there is a read to this register when the transcoders receive queue is empty (i.e. the "Number Rx DW" within DSI_CMD_RXDATA is zero), then the data returned will be all zeros. Note that the contents of the Receive Payload queue within the transcoder is flushed for every entry into a Bus Turn-Around state.

DSI_CMD_TXCTL

DSI_CMD_TXCTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6B0D0h-6B0D3h
Name:	DSI Transcoder 0 Command Transmit Control
ShortName:	DSI_CMD_TXCTL_0
Power:	PG1
Reset:	soft
Address:	6B8D0h-6B8D3h
Name:	DSI Transcoder 1 Command Transmit Control
ShortName:	DSI_CMD_TXCTL_1
Power:	PG1
Reset:	soft

This register controls how DSI command packets are built and transmitted over the DSI Link.

DWord	Bit	Description
0	31:25	**Reserved** Format: MBZ
	24	**Keep Link in HS** Access: R/W This field will keep the Link in the HS state between SW initiated command packets to the Periphery. The transitions between the LP and HS states can result in significant latencies and can have a negative impact on SW performance. If between HS commands there is no other HS traffic to transmit, then the DSI transcoder will begin transmitting Null packets until the next HS packet arrives. **Restriction** Restrictions: 1. HW will only act on this bit when the DSI transcoder is in the Command Mode of operation. 2. SW must clear this bit if it is going to initiate a LP transaction (e.g. a LPDT, BTA, Trigger, etc). 3. SW should clear this bit when it is finished sending its burst of commands to the Periphery.

DSI_CMD_TXCTL		
	23:13	**Reserved** Format: MBZ
	12:8	**Free Header Credits** Access: RO This field represents the number of Header resources that are currently available to SW. SW will need a Header Credit to write to either the Command Tx Header (DSI_CMD_TXHDR) or the LP Message (DSI_LP_MSG) registers. A write to either of these registers will consume a Header Credit. The transcoder will release a Header Credit after it has pulled the command from its internal command header queue. HW currently maintains 16 Header Credits.
	7:0	**Free Payload Credits** Access: RO This field represents the number of Payload resources that are currently available to SW. SW will need a Payload Credit to write to the Command Tx Payload register (DSI_CMD_TXPYLD). A write to the Tx Payload register will consume 1 Payload Credit (i.e. 1 Payload Credit is equal to 1 to 4 bytes of payload). The transcoder will release a Payload Credit after it has pulled a DW of data from its internal command payload queue. HW currently maintains 64 Payload Credits (i.e. HW can accept payloads of up to 256 bytes).

DSI_CMD_TXHDR

DSI_CMD_TXHDR

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6B100h-6B103h
Name:	DSI Transcoder 0 Transmit Packet Header
ShortName:	DSI_CMD_TXHDR_0
Power:	PG1
Reset:	soft
Address:	6B900h-6B903h
Name:	DSI Transcoder 1 Transmit Packet Header
ShortName:	DSI_CMD_TXHDR_1
Power:	PG1
Reset:	soft

This register is used to write a packet header to the DSI transcoder.

DWord	Bit	Description
0	31	**Payload** Access: R/W When set, the DSI packet carries a payload of data. Value / Name: 0b – Short packet format (no payload) 1b – Long packet format (payload) **Restriction** Restrictions: 1. SW must ensure that the Data Type encoding matches the packet format specified by this attribute. 2. SW must ensure that the payload data is written into the Command Payload queue before writing to this register, if this bit is set.
	30	**LPDT** Access: R/W Low Power Data Transfer. This field will direct the DSI transcoder on what mode (HS or LP) to transmit the packet in.

DSI_CMD_TXHDR

Value	Name
0b	Cmd transmitted in HS state
1b	Cmd transmitted in LP Escape mode

Restriction
SW must expect synchronization events to be missed, if it sets this attribute when the DSI controller is in the Video Mode of operation and the Timing Generator is enabled. SW is highly discouraged from setting this bit when in Video Mode.

29 **Vertical Blank Fence**

Access:	R/W

This field will direct the DSI transcoder to wait until the start of the next V. Blank (in Video Mode) or the end of the frame (in Command Mode) before it executes the Command.
This can be used for Frame Synchronized Commands that have to be fenced after the transmission of an Execute Queue.

Value	Name
0b	Cmd will not be fenced
1b	Cmd will be fenced

28:24 **Reserved**

Format:	MBZ

23:8 **Word Count - Parameters**

Access:	R/W

This field specifies either the DSI Word Count (i.e. the length of the payload in bytes), or the two bytes of Parameters.
The interpretation of this field by the DSI transcoder will be based off of the Payload attribute above.
When the Payload bit is '0', then these bytes represent Parameters
When the Payload bit is '1', then these bytes represent the Word Count of the Payload
The interpretation of this field by the Periphery will be based off of the Data Type field below

Restriction
When the command carries a payload, SW must ensure that the value within this field matches the amount of payload data loaded into the Command Payload queue associated with this packet For Short packets, it will be the responsibility of SW to adhere to the DSI protocols if the packet carries only one, or no parameter

7:6 **Virtual Channel**

Access:	R/W

This field specifies the virtual channel to transmit the command over the DSI Link.

5:0 **Data Type**

DSI_CMD_TXHDR			
		Access:	R/W
		This field specifies the DSI command Data Type.	

DSI_CMD_TXPYLD

DSI_CMD_TXPYLD	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6B104h-6B107h
Name:	DSI Transcoder 0 Transmit Packet Payload
ShortName:	DSI_CMD_TXPYLD_0
Power:	PG1
Reset:	soft
Address:	6B904h-6B907h
Name:	DSI Transcoder 1 Transmit Packet Payload
ShortName:	DSI_CMD_TXPYLD_1
Power:	PG1
Reset:	soft

This register is used to write a DW of packet payload to the DSI transcoder.

DWord	Bit	Description
0	31:0	**Payload Data** Access: R/W This register is a proxy into the payload of the command packet to be injected onto the DSI Link. Writes to this register will load the DW of data into a Command Payload queue that will be unloaded by HW after the packet has been validated via a write to the DSI_CMD_TXHDR register. When reading from this register, only the payload data from the last write will be available. **Restriction** Software must have an available Payload credit to write to this register. SW must write the payload in ascending order (i.e. DW 0 is written first, the final DW is written last). SW must load the entire payload within the Command Payload queue before writing to the Command Header register (DSI_CMD_TXHDR). The write to the Command Header register validates the payload written to this queue. SW must ensure that the WC of the Packet Header matches the amount of data written to the Command Payload queue.

DSI_DATA_TIMING_PARAM

DSI_DATA_TIMING_PARAM

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32

Address:	6B084h-6B087h
Name:	DSI 0 Data Lane Timing Parameter
ShortName:	DSI_DATA_TIMING_PARAM_0
Power:	PG1
Reset:	soft

Address:	6B884h-6B887h
Name:	DSI 1 Data Lane Timing Parameter
ShortName:	DSI_DATA_TIMING_PARAM_1
Power:	PG1
Reset:	soft

This register specifies the D-PHY timing parameters for the Data Lane, if SW is overriding the HW defaults.
This register is located within the Core Display and is used by the DSI Controller to calculate Link transition latencies of the Data Lanes. There is an identical register (DPHY_DATA_TIMING_PARAM) located within the combo-PHY that actually applies the overrides to the D-PHY Data Lanes. Both registers should be programmed by Software if an override needs to be applied to the Data Lanes within the D-PHY.
Since this register is being used to calculate the Link transition latencies of the Data Lanes, but does not actually affect the transition times within the D-PHY, this register can be used to add guardbands to the DSI Controller's transition latency calculations.
The lower 12 bits of the offset address for this register should correspond to the lower offset address of its sister D-PHY register within the combo-PHY.
All fields are defined in number of Escape clocks.

Restriction
Overall restriction is that the timing parameters must be non-zero if SW is overriding the HW timing parameters. The programming of this register must be equal to or greater than the programming of it's sister register that lives within the combo-PHY (DPHY_DATA_TIMING_PARAM).

DWord	Bit	Description
0	31	**HS_PREPARE Override** Access: R/W This field controls the override of the HS-PREPARE timing parameter. Value / Name

0	HW maintains	
1	SW overrides	

30:27 **Reserved**

Format:	MBZ

26:24 **HS_PREPARE**

Access:	R/W

This parameter defines the time that the Host drives a Data Lane with the LP-00 Lane state (the Bridge state) immediately before driving the HS-0 Line state.
This field represents a hexadecimal value with a precision of 1.2 – i.e. the most significant bit is the integer and the least significant 2 bits are fraction bits. So, the field can represent a range of 0.25 to 1.75 (12.5ns to 87.5ns assuming an Escape clock with a 20MHz frequency)
HW maintains this parameter at 1 Escape clock (minimum 50ns)

Value	Name
001b	0.25 Escape clocks
010b	0.50 Escape clocks
011b	0.75 Escape clocks
100b	1.0 Escape clocks
101b	1.25 Escape clocks
110b	1.50 Escape clocks
111b	1.75 Escape clocks
Others	Reserved

Programming Notes
Caution: The MIPI D-PHY specification has a maximum of 85ns + 6UI for this parameter.

23 **HS_ZERO Override**

Access:	R/W

This field controls the override of the HS-ZERO timing parameter

Value	Name
0	HW maintains
1	SW overrides

22:20 **Reserved**

Format:	MBZ

19:16 **HS_ZERO**

Access:	R/W

This parameter defines the time that the Host drives the HS-0 Lane state on a Data Lane.
HW maintains this parameter at 2 Escape clocks plus 1 Byte clock (minimum 100ns + 8UI)

15 **HS_TRAIL Override**

DSI_DATA_TIMING_PARAM

		Access: R/W
		This field controls the override of the HS-TRAIL timing parameter

Value	Name
0	HW maintains
1	SW overrides

14:11	**Reserved**
	Format: MBZ
10:8	**HS_TRAIL**
	Access: R/W
	This parameter defines the time that the Host drives the flipped differential state of the last payload data bit of a HS transmission on a Data Lane. HW maintains this parameter at 1.5 Escape clocks (minimum 75ns)
7	**HS_EXIT Override**
	Access: R/W
	This field controls the override of the HS-EXIT timing parameter

Value	Name
0	HW maintains
1	SW overrides

6:3	**Reserved**
	Format: MBZ
2:0	**HS_EXIT**
	Access: R/W
	This parameter defines the time that the Host drives the LP-11 Lane state (i.e. the Stop state) following a HS burst. HW maintains this parameter at 2 Escape clocks (minimum 100ns)

DSI_ESC_CLK_DIV

DSI_ESC_CLK_DIV

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	6B090h-6B093h
Name:	DSI 0 Escape Clock Divider
ShortName:	DSI_ESC_CLK_DIV_0
Power:	PG1
Reset:	soft
Address:	6B890h-6B893h
Name:	DSI 1 Escape Clock Divider
ShortName:	DSI_ESC_CLK_DIV_1
Power:	PG1
Reset:	soft

This register defines the clock divider variable M needed to generate an Escape clock from the 8X clock
This register is located within the Core Display. There is an identical register (DPHY_ESC_CLK_DIV) located within the combo-PHY. Both of these registers should be programmed by Software.
The lower 12 bits of the offset address for this register should correspond to the lower offset address of its sister D-PHY register within the combo-PHY.

Restriction : The programming of this register must be identical to the programming of its sister register that lives within the combo-PHY (DPHY_ESC_CLK_DIV)

DWord	Bit	Description
0	31:21	**Reserved**
	20:16	**Byte Clocks per Escape Clock** Access: RO This field reports the number of Byte clocks present within a givenEscape clock. The DSI transcoder calculates this variable based off of the Escape clock divider M. N = Ceiling(M/8) The DSI complex (transcoder and D-PHY) use this information to emulate an Escape clock using the Byte clock. Note that the value reported here is zero-based (i.e. Ceiling(M/8) - 1)
	15:9	**Reserved**
	8:0	**Escape Clock Divider M** Access: R/W This field specifies the divider variable (M) needed to derive the Escape clock from the Link clock

DSI_ESC_CLK_DIV		
		(i.e. the 8X frequency) Escape frequency = 8X frequency / M The DSI transcoder does not use a physical Escape clock, so there is no physical divider, but the transcoder needs to know the value of M to emulate the Escape clock in Byte clocks. **Restriction** The Escape clock frequency must be as close to, but not greater than 20MHz. Therefore, the programming of M should be: M = Ceiling(8X Frequency (in MHz) / 20 MHz)

DSI_HTX_TO

DSI_HTX_TO	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6B044h-6B047h
Name:	DSI 0 HS Transmit Timeout
ShortName:	DSI_HTX_TO_0
Power:	PG1
Reset:	soft
Address:	6B844h-6B847h
Name:	DSI 1 HS Transmit Timeout
ShortName:	DSI_HTX_TO_1
Power:	PG1
Reset:	soft

This register specifies the HS Tx timeout.

DWord	Bit	Description
0	31:16	**HS TX Timeout** Default Value: FFFFh Access: R/W This field represents the upper 16 bits of the HS Transmit Timeout (i.e. the timeout has a granularity of 64K). The time is specified in Byte clocks. This field will default to the maximum possible value. **Programming Notes** This timer is zero-based (i.e. a value of 0 will have a timeout of 64K) If the DSI transcoder is in the Video Mode and is not able to place the Link in the LP state during the H. Blank regions of the V. Active region, then SW must program this to be greater that the amount of time it takes to transmit the full frame (V. Total * H. Total). The value should be set to a value greater than the Peripheral's HS RX Timeout.
	15:1	**Reserved** Format: MBZ
	0	**HTX_TO** Access: R/WC The HS TX Timer has timed out. HW will set this bit, SW will clear it with a write of 1b.

DSI_INTER_IDENT_REG

DSI_INTER_IDENT_REG	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/WC
Size (in bits):	32
Address:	6B074h-6B077h
Name:	DSI Transcoder 0 Interrupt Identity Register
ShortName:	DSI_INTER_IDENT_REG_0
Power:	PG1
Reset:	soft
Address:	6B874h-6B877h
Name:	DSI Transcoder 1 Interrupt Identity Register
ShortName:	DSI_INTER_IDENT_REG_1
Power:	PG1
Reset:	soft

The DSI Interrupt Identity Register (IIR) logs non-masked DSI interrupts received from the Periphery and Host. The DSI_INTER_MSK_REG (IMR) controls which interrupts will be logged within the IIR.

DWord	Bit	Description
0	31	**TE Event** Access: R/WC A Tear Effect (TE) event was received
	30	**Rx Data / BTA Terminated** Access: R/WC READ response data has been received, or the BTA has been terminated
	29	**Tx Data** Access: R/WC A transmit credit has been freed
	28	**ULPS Entry Done** Access: R/WC A Ultra Low Power State Entry flow has completed
	27	**Non-TE Trigger Received**

DSI_INTER_IDENT_REG

		Access: R/WC A non-TE trigger has been received from the Periphery. The DSI_CMD_RXCTL will indicate the trigger received.
	26	**Host Checksum Error** Access: R/WC Host reported a checksum error
	25	**Host Multi ECC Error** Access: R/WC Host reported a multi-bit ECC error
	24	**Host Single ECC Error** Access: R/WC Host reported a single-bit ECC
	23	**Host Contention Detected** Access: R/WC Host reported a LP contention
	22	**Host False Control Error** Access: R/WC Host reported a False Control error
	21	**Host Timeout Error** Access: R/WC Host reported a Timeout error
	20	**Host Low Power Transmit Sync Error** Access: R/WC Host reported a LP Transmission byte alignment problem
	19	**Host Escape Mode Entry Command Error** Access: R/WC Host reported an Escape Mode entry command error
	18:17	**Spare 18_17** Access: R/WC Spare R/WC bits for future use

DSI_INTER_IDENT_REG

	16	**Frame Update Done** Access: R/WC A frame update is done. This interrupt is only valid when the transcoder is in Command Mode
	15	**Protocol Violation** Access: R/WC Peripheral reported a protocol violation
	14	**Spare 14** Access: R/WC Spare R/WC bit for future use
	13	**Invalid Tx Length** Access: R/WC Peripheral reported an invalid transmission length
	12	**Invalid VC** Access: R/WC Peripheral reported an invalid DSI VC ID
	11	**Invalid Data Type** Access: R/WC Peripheral reported a non-recognizable DSI Data Type
	10	**Peripheral Checksum Error** Access: R/WC Peripheral reported a checksum error
	9	**Peripheral Multi ECC Error** Access: R/WC Peripheral reported a multi-bit ECC error
	8	**Peripheral Single ECC Error** Access: R/WC Peripheral reported a single-bit ECC error
	7	**Peripheral Contention Detected** Access: R/WC Peripheral reported a LP contention

DSI_INTER_IDENT_REG

	6	**Peripheral False Control Error** Access: R/WC Peripheral reported a False Control error
	5	**Peripheral Timeout Error** Access: R/WC Peripheral reported a timeout error
	4	**Peripheral Low Power Transmit Sync Error** Access: R/WC Peripheral reported a LP Transmission byte alignment problem
	3	**Peripheral Escape Mode Entry Command Error** Access: R/WC Peripheral reported an Escape Mode entry command error
	2	**EoT Sync Error** Access: R/WC Peripheral reported an End of Transmission byte alignment problem
	1	**SoT Sync Error** Access: R/WC Peripheral reported a Start of Transmission leader sequence corruption error
	0	**SoT Error** Access: R/WC Peripheral reported a Start of Transmission Error

DSI_INTER_MSK_REG

DSI_INTER_MSK_REG

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6B070h-6B073h
Name:	DSI Transcoder 0 Interrupt Mask Register
ShortName:	DSI_INTER_MSK_REG_0
Power:	PG1
Reset:	soft
Address:	6B870h-6B873h
Name:	DSI Transcoder 1 Interrupt Mask Register
ShortName:	DSI_INTER_MSK_REG_1
Power:	PG1
Reset:	soft

The DSI Interrupt Mask Register (IMR) provides a filter to the events that can cause interrupts (i.e. the register will determine which events will be logged within the DSI Interrupt Identity Register (IIR))

DWord	Bit	Description
0	31	**TE Event** Access: R/W Tear Effect (TE) interrupt mask 0: Event Unmasked 1: Event Masked **[Default]**
	30	**Rx Data/BTA Terminated** Access: R/W READ response data received, or the BTA has been terminated interrupt mask 0: Event Unmasked 1: Event Masked **[Default]**
	29	**Tx Data** Access: R/W Freed transmit credit interrupt mask Value / Name

0	Event Unmasked
1	Event Masked **[Default]**

28 **ULPS Entry Done**

Access:	R/W

Ultra Low Power State Entry flow interrupt mask

Value	Name
0	Event Unmasked
1	Event Masked **[Default]**

27 **Non-TE Trigger Received**

Access:	R/W

Non-TE trigger received interrupt mask

Value	Name
0	Event Unmasked
1	Event Masked **[Default]**

26 **Host Checksum Error**

Access:	R/W

Host reported a checksum error interrupt mask

Value	Name
0	Event Unmasked
1	Event Masked **[Default]**

Programming Notes
Masking this event effectively disables the CRC checking for received payloads

25 **Host Multi ECC Error**

Access:	R/W

Host reported a multi-bit ECC error interrupt mask

Value	Name
0	Event Unmasked
1	Event Masked **[Default]**

Programming Notes
Masking this event along with the Host Single ECC Error mask bit will disable ECC checking for recieved packet headers

24 **Host Single ECC Error**

Access:	R/W

Host reported a single-bit ECC error interrupt mask

Value	Name

DSI_INTER_MSK_REG

		0 Event Unmasked 1 Event Masked **[Default]** **Programming Notes** Masking this event along with the Host Multi ECC Error mask bit will disable ECC checking for received packet headers
	23	**Host Contention Detected** Access: R/W Host reported a LP contention interrupt mask **Value** / **Name** 0 Event Unmasked 1 Event Masked **[Default]**
	22	**Host False Control Error** Access: R/W Host reported a False Control error interrupt mask **Value** / **Name** 0 Event Unmasked 1 Event Masked **[Default]**
	21	**Host Timeout Error** Access: R/W Host reported a Timeout error interrupt mask **Value** / **Name** 0 Event Unmasked 1 Event Masked **[Default]**
	20	**Host Low Power Transmit Sync Error** Access: R/W Host reported a LP Transmission byte alignment problem interrupt mask **Value** / **Name** 0 Event Unmasked 1 Event Masked **[Default]**
	19	**Host Escape Mode Entry Command Error** Access: R/W Host reported an Escape Mode entry command error interrupt mask **Value** / **Name** 0 Event Unmasked 1 Event Masked **[Default]**
	18:17	**Spare 18_17**

DSI_INTER_MSK_REG

	Default Value:	11b
	Access:	R/W

Spare R/W bits for future use

16 Frame Update Done

Frame update finished mask

Value	Name
0b	Event Unmasked
1b	Event Masked **[Default]**

15 Protocol Violation

Access:	R/W

Peripheral reported a protocol violation interrupt mask

Value	Name
0	Event Unmasked
1	Event Masked **[Default]**

14 Spare 14

Default Value:	1b
Access:	R/W

Spare R/W bit for future use

13 Invalid Tx Length

Access:	R/W

Peripheral reported an invalid transmission length interrupt mask

Value	Name
0	Event Unmasked
1	Event Masked **[Default]**

12 Invalid VC

Access:	R/W

Peripheral reported an invalid DSI VC ID interrupt mask

Value	Name
0	Event Unmasked
1	Event Masked **[Default]**

11 Invalid Data Type

Access:	R/W

Peripheral reported a non-recognizable DSI Data Type interrupt mask

Value	Name
0	Event Unmasked

DSI_INTER_MSK_REG

1	Event Masked **[Default]**

10 — Peripheral Checksum Error

Access:	R/W

Peripheral reported a checksum error interrupt mask

Value	Name
0	Event Unmasked
1	Event Masked **[Default]**

9 — Peripheral Multi ECC Error

Access:	R/W

Peripheral reported a multi-bit ECC error interrupt mask

Value	Name
0	Event Unmasked
1	Event Masked **[Default]**

8 — Peripheral Single ECC Error

Access:	R/W

Peripheral reported a single-bit ECC error interrupt mask

Value	Name
0	Event Unmasked
1	Event Masked **[Default]**

7 — Peripheral Contention Detected

Access:	R/W

Peripheral reported a LP contention interrupt mask

Value	Name
0	Event Unmasked
1	Event Masked **[Default]**

6 — Peripheral False Control Error

Access:	R/W

Peripheral reported a False Control error interrupt mask

Value	Name
0	Event Unmasked
1	Event Masked **[Default]**

5 — Peripheral Timeout Error

Access:	R/W

Peripheral reported a timeout error interrupt mask

Value	Name
0	Event Unmasked

DSI_INTER_MSK_REG

	1	Event Masked **[Default]**

4 — Peripheral Low Power Transmit Sync Error

Access:	R/W

Peripheral reported a LP Transmission byte alignment problem interrupt mask

Value	Name
0	Event Unmasked
1	Event Masked **[Default]**

3 — Peripheral Escape Mode Entry Command Error

Access:	R/W

Peripheral reported an Escape Mode entry command error interrupt mask

Value	Name
0	Event Unmasked
1	Event Masked **[Default]**

2 — EoT Sync Error

Access:	R/W

Peripheral reported an End of Transmission byte alignment problem interrupt mask

Value	Name
0	Event Unmasked
1	Event Masked **[Default]**

1 — SoT Sync Error

Access:	R/W

Peripheral reported a Start of Transmission leader sequence corruption error interrupt mask

Value	Name
0	Event Unmasked
1	Event Masked **[Default]**

0 — SoT Error

Access:	R/W

Peripheral reported a Start of Transmission Error interrupt mask

Value	Name
0	Event Unmasked
1	Event Masked **[Default]**

DSI_IO_MODECTL

DSI_IO_MODECTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	6B094h-6B097h
Name:	DSI Transcoder 0 IO Mode Control
ShortName:	DSI_IO_MODECTL_0
Power:	PG1
Reset:	soft
Address:	6B894h-6B897h
Name:	DSI Transcoder 1 IO Mode Control
ShortName:	DSI_IO_MODECTL_1
Power:	PG1
Reset:	soft

This register is used to control the mode of operation within the Combo-PHY which is shared between the MIPI DSI transcoder and the eDP/DP DDI.
Each DSI transcoder is attached to the following Combo-PHY:
DSI0: Combo-PHY A
DSI1: Combo-PHY B
Note that the Combo-PHY's are also referred to as DDI A / DDI B

Restriction : If the Combo-PHY is going to be used by the DSI transcoder, then this register must be programmed **before** the power request is sent to the Combo-PHY

DWord	Bit	Description
0	31:1	**Reserved**
	0	**Combo PHY Mode** Access: R/W For products using a Combo-PHY for the DSI port, this bit selects the mode of operation within the Combo-PHY to which the DSI transcoder is attached. For products using a dedicated DSI PHY, this bit controls the clock request to the PHY. 0b – DDI Mode / No Clock Request 1b – MIPI DSI Mode / Clock Request

DSI_LP_MSG

DSI_LP_MSG

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W Set
Size (in bits):	32
Address:	6B0D8h-6B0DBh
Name:	DSI 0 Low Power Message
ShortName:	DSI_LP_MSG_0
Power:	PG1
Reset:	soft
Address:	6B8D8h-6B8DBh
Name:	DSI 1 Low Power Message
ShortName:	DSI_LP_MSG_1
Power:	PG1
Reset:	soft

This register contains the LP messages that can be sent to the Periphery.

Restriction
Software must have a Header credit to write to this register.

DWord	Bit	Description
0	31:19	**Reserved** Format: MBZ
	18	**Link Direction** Access: RO This field advertises the current state of the Link direction 0b: Link is in the Forward direction 1b: Link is in the Reverse direction
	17	**LP Tx in Progress** Access: RO This status bit indicates whether the DSI transcoder is currently servicing a LP transaction. 0b: Transcoder is not transmitting in the LP Esc mode 1b: Transcoder is transmitting in the LP Esc mode

DSI_LP_MSG

16 — In ULPS

Access:	RO

This status bit indicates whether the DSI Link is in the Ultra Low Power State (ULPS), or not.
This bit should acurately reflect the ultra low power state of the Link even when the DSI transcoder function is disabled.

Value	Name
0b	The DSI Link is not in ULPS
1b	The DSI Link is in ULPS

15:11 — Reserved

Format:	MBZ

10:9 — Trigger Type

Access:	R/W

This field specifies the type of Trigger Message to send the Peripheral. It is only sampled when a Trigger Message is being sent to the Peripheral.

Value	Name	Description
00b	Reset Trigger	Entry Command [lsb:msb]: 01100010
01b	Unknown 3	Entry Command [lsb:msb]: 01011101
10b	Unknown 4	Entry Command [lsb:msb]: 00100001
11b	Unknown 5	Entry Command [lsb:msb]: 10100000

Programming Notes
Note that the “Unassigned” triggers are not specifically assigned to a given action/function within the DSI spec. Therefore, these can be used as general purpose trigger messages that the Periphery defines

8 — ULPS Type

Access:	R/W

This bit specifies the LP state that the Lanes (both Data and Clock) will be left in after entering ULPS

Value	Name	Description
0b	LP-00	Lanes will be left in the LP-00 state
1b	LP-11	Lanes will be left in the LP-11 state

7:3 — Reserved

Format:	MBZ

2 — Trigger Message

Access:	R/W Set

This bit will direct the DSI Transcoder to issue a Trigger Message to the Peripheral. The type of trigger is specified with the Trigger Type field within this register.
Trigger signaling is a mechanism to send a flag to the Protocol Layer of the Periphery using the

DSI_LP_MSG

		Escape Mode of transmission. **Programming Notes** The trigger flag, as seen by the Peripheral, can be extended using the "Trigger Extension" in the DPHY_TRIG_EXT. The DSI Transcoder will clear this bit when it is finished with the transmission of the message (including the Trigger Extension)
	1	**Bus Turnaround** Access: R/W Set This bit will direct the DSI Transcoder to issue a BTA request to the Periphery. **Programming Notes** When in Video Mode, the DSI transcoder will dispatch a BTA request (by itself) within the next Vertical blank line that it sees. SW must program the Turnaround Timeout (DSI_TA_TO) and the LP Rx (Host) Timeout (DSI_LRX_H_TO) properly to avoid having synchronization events being missed. In other words, the total amount of time it takes to send a BTA and receive a response from the Panel needs to be less than the Vertical blank line time.
	0	**ULPS Entry** Access: R/W Set Ultra Low Power State Entry. When set, the DSI Transcoder will transmit the ULPS Entry Command on all Data Lanes and it will bring the Clock Lane to the ULPS state. The state of the Lanes at the end of the ULPS flow is dictated by the ULPS Type within this register. When HW has finished the UPLS sequence it will clear this bit. **Restriction** Before setting this bit Software must disable the DSI's Timing Generator

DSI_LRX_H_TO

DSI_LRX_H_TO	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6B048h-6B04Bh
Name:	DSI 0 LP Rx (Host) Timeout
ShortName:	DSI_LRX_H_TO_0
Power:	PG1
Reset:	soft
Address:	6B848h-6B84Bh
Name:	DSI 1 LP Rx (Host) Timeout
ShortName:	DSI_LRX_H_TO_1
Power:	PG1
Reset:	soft

This register specifies the LP Rx (Host) timeout.

DWord	Bit	Description
0	31:17	**Reserved** Format: MBZ
	16	**LRX_H_TO** Default Value: 0b Access: R/WC The LP RX Timer has timed out. HW will set this bit, SW must clear it with a write of 1b.
	15:0	**LP RX_H Timeout** Access: R/W This field represents the maximum amount of time the DSI transcoder will give to the Peripheral to transmit its response back to the Host. If the timer times out, then the DSI transcoder will set the LRX_H_TO bit in this register and the "Host Timeout Error" bit within the DSI_INTER_IDENT_REG register, if this interrupt event is unmasked (DSI_INTER_MSK_REG). The time is specified in Escape clocks. **Programming Notes** The LP RX Timer will be disabled if this value is zero

DSI_PWAIT_TO

DSI_PWAIT_TO	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6B040h-6B043h
Name:	DSI 0 Peripheral Wait Timeout
ShortName:	DSI_PWAIT_TO_0
Power:	PG1
Reset:	soft
Address:	6B840h-6B843h
Name:	DSI 1 Peripheral Wait Timeout
ShortName:	DSI_PWAIT_TO_1
Power:	PG1
Reset:	soft

This register represents a Peripheral wait time used in conjunction with either a BTA or a Trigger LP message.
The times specified within this register are in terms of Escape clocks.
The timers are zero-based (i.e. a value of 0 equals 1 Escape clock)

DWord	Bit	Description
0	31:16	**Peripheral Reset Timeout** Access: R/W This field represents the time to wait after a Reset Trigger has been transmitted to the Peripheral (PR_TO). The timer will start after the Trigger message has been sent and the DSI transcoder will block all other traffic until the timer reaches the timeout value.
	15:0	**Peripheral Response Timeout** Access: R/W This field represents the time to wait before asking the Peripheral for a response (PRESP_TO). The timer will start when the DSI transcoder receives the BTA request from SW and the Link enters the Stop state. When the timer reaches the timeout value, the DSI transcoder will begin the BTA request to the Peripheral.

DSI_T_INIT_MASTER

DSI_T_INIT_MASTER	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6B088h-6B08Bh
Name:	DSI 0 Initialization Master Time
ShortName:	DSI_T_INIT_MASTER_0
Power:	PG1
Reset:	soft
Address:	6B888h-6B88Bh
Name:	DSI 1 Initialization Master Time
ShortName:	DSI_T_INIT_MASTER_1
Power:	PG1
Reset:	soft

This register specifies the amount of time (in Escape clocks) to drive the Link in the initialization (i.e. LP-11) state.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**Master Initialization Time** Default Value: 07D0h Access: R/W This field specifies the INIT_MASTER timing parameter used by the Host to drive the Link initialization. This field is specified in Escape clocks where the Escape clock operates at a maximum frequency of 20MHz. **Programming Notes** The default value of this register will produce an initialization duration of 100us which is the minimum requirement for the INIT timing parameter. The Periphery may require a longer initialization period (INIT + INTERNAL_DELAY), so the value programmed should be greater than the Periphery's initialization requirements.

DSI_T_WAKEUP

DSI_T_WAKEUP

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6B08Ch-6B08Fh
Name:	DSI 0 Wakeup Timing Parameter
ShortName:	DSI_T_WAKEUP_0
Power:	PG1
Reset:	soft
Address:	6B88Ch-6B88Fh
Name:	DSI 1 Wakeup Timing Parameter
ShortName:	DSI_T_WAKEUP_1
Power:	PG1
Reset:	soft

This is the timing parameter T-WAKEUP used to drive the Mark-1 state on the Link when exiting ULPS.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**Wakeup Time** Default Value: 4E20h Access: R/W This field represents the T_{WAKEUP} timing parameter used when ULPS is being exited. The time is specified in number of Escape clocks. The default of this field will be set to 1ms (MIPI DSI specification minimum). **Restriction** A value of zero is invalid

DSI_TA_TIMING_PARAM

DSI_TA_TIMING_PARAM

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32

Address:	6B098h-6B09Bh
Name:	Core DPHY 0 Turnaround Timing Parameter
ShortName:	DSI_TA_TIMING_PARAM_0
Power:	PG1
Reset:	soft

Address:	6B898h-6B89Bh
Name:	Core DPHY 1 Turnaround Timing Parameter
ShortName:	DSI_TA_TIMING_PARAM_1
Power:	PG1
Reset:	soft

This register specifies the D-PHY timing parameters used for the Bus Turn-Around flow, if SW is overriding the HW defaults.
All fields are defined in number of Escape clocks.
This register controls the D-PHY located within the Display Core.

Restriction : Overall restriction is that the timing parameters must be non-zero if SW is overriding the HW timing parameters.

DWord	Bit	Description
0	31	**TA_SURE Override** This field controls the override of the TA-SURE timing parameter Value: 0b — Name: HW maintains Value: 1b — Name: SW overrides
	30:21	**Reserved**
	20:16	**TA_SURE** This parameter defines the time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround. This field represents a hexadecimal value with a precision of 3.2 – i.e. the most significant 3 bits are the integer and the least significant 2 bits are fraction bits. So, the field can represent a range of 0.25 to 7.75 (12.5ns to 387.5ns assuming an Escape clock with a 20MHz frequency) HW maintains this parameter at 1 Escape clock (minimum 50ns).

DSI_TA_TIMING_PARAM

		Programming Notes 1. Caution: The MIPI D-PHY specification has a maximum of 2 Escape clocks for this parameter 2. If operating at or below an 800MHz Link frequency, this parameter should be overridden and programmed to a value of 0
	15	**TA_GO Override** This field controls the override of the TA-GO timing parameter **Value** / **Name** 0b – HW maintains 1b – SW overrides
	14:12	**Reserved**
	11:8	**TA_GO** This parameter defines the time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Turnaround. HW maintains this parameter at 4 Escape clocks (minimum 200ns) **Programming Notes** Caution: The MIPI D-PHY specification has a fixed requirement of 4 Escape clocks for this parameter
	7	**TA_GET Override** This field controls the override of the TA-GET timing parameter **Value** / **Name** 0b – HW maintains 1b – SW overrides
	6:4	**Reserved**
	3:0	**TA_GET** This parameter defines the time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround. HW maintains this parameter at 5 Escape clocks (minumum 250ns) **Programming Notes** Caution: The MIPI D-PHY specification has a fixed requirement of 5 Escape clocks for this parameter

DSI_TA_TO

DSI_TA_TO	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6B04Ch-6B04Fh
Name:	DSI 0 Turnaround Timeout
ShortName:	DSI_TA_TO_0
Power:	PG1
Reset:	soft
Address:	6B84Ch-6B84Fh
Name:	DSI 1 Turnaround Timeout
ShortName:	DSI_TA_TO_1
Power:	PG1
Reset:	soft

This register specifies the Turnaround timeout.

DWord	Bit	Description
0	31:17	**Reserved** Format: MBZ
	16	**TA_TO** Access: R/WC The Turnaround Timer has timed out. HW will set this bit, SW must clear it with a write of 1b.
	15:0	**Turnaround Timeout** Access: R/W This field represents the maximum amount of time the Host will give to the Peripheral to acknowledge the Bus Turnaround request. If the timer times out, then the DSI transcoder will set the TA_TO bit in this register and the "Host Timeout Error" bit within the DSI_INTER_IDENT_REG register, if this interrupt event is unmasked (DSI_INTER_MSK_REG). The time is specified in Escape clocks. **Programming Notes** The TA TO Timer will be disabled if this value is zero

DSI_TRIG_EXT

DSI_TRIG_EXT	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6B09Ch-6B09Fh
Name:	Core DPHY 0 Trigger Extension
ShortName:	DSI_TRIG_EXT_0
Power:	PG1
Reset:	soft
Address:	6B89Ch-6B89Fh
Name:	Core DPHY 1 Trigger Extension
ShortName:	DSI_TRIG_EXT_1
Power:	PG1
Reset:	soft

This register specifies the amount of time to extend a Trigger message to the Peripheral.
This register controls the D-PHY located within the Display Core.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**Trigger Extension** This field specifies the number of Escape clocks to extend a trigger message by. This effectively extends the duration that the trigger is asserted at the Peripheral's Protocol Layer. This field is only used if a Trigger Message is initiated from the DSI_LP_MSG register.

DS Invocation Counter

DS_INVOCATION_COUNT - DS Invocation Counter	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02308h
Name:	DS Invocation Counter
ShortName:	DS_INVOCATION_COUNT

This register stores the number of domain points shaded by the DS threads. Domain points which hit in the DS cache will not cause this register to increment. Note that the spawning of a DS thread which shades two domain points will cause this counter to increment by two.This register is part of the context save and restore.

DWord	Bit	Description
0..1	63:32	**DS Invocation Count UDW** Number of domain points shaded by the DS threads. Updated only when DS Function Enable and Statistics Enable are set in 3DSTATE_DS
	31:0	**DS Invocation Count LDW** Number of domain points shaded by the DS threads. Updated only when DS Function Enable and Statistics Enable are set in 3DSTATE_DS

DSSM

DSSM

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	51004h-51007h
Name:	Display Strap State
ShortName:	DSSM
Power:	PG0
Reset:	global

This register contains fuse and strap settings for display. This register is not reset by FLR.

DWord	Bit	Description
0	31:29	**Reference Frequency** Access: RO This field indicates the reference clock frequency. Software should use this value when programming the display clocks. 000b: 24 MHz 001b: 19.2 MHz 010b: 38.4 MHz
	28	**Spare 28**
	27	**Spare 27**
	26	**Spare 26**
	25	**Spare 25**
	24	**Spare 24**
	23	**Spare 23**
	22	**Spare 22**
	21	**Spare 21**
	20	**Spare 20**
	19	**Spare 19**
	18	**Spare 18**
	17	**Spare 17**
	16	**Spare 16**

DSSM

15	**Spare 15**
14	**Spare 14**
13	**Spare 13**
12	**Spare 12**
11	**Spare 11**
10	**Spare 10**
9	**Spare 9**
8	**Spare 8**
7	**Spare 7**
6	**Spare 6**
5	**Spare 5**
4	**Spare 4**
3	**WD Video Fault Continue** This field specifies whether WD video should continue data writes after a fault or stop the writes.
2	**Reserved**
1	**Part Is SOC** This field specifies whether this part is a SoC or not.
0	**DisplayPort A Present** This bit specifies whether the port was present during initalization. This strap state can also be read in the DDI_BUF_CTL_A 0x64000 register bit 0.

Value	Name
0b	Stop Writes
1b	Continue Writes

Value	Name
0b	Not SoC
1b	SoC

Value	Name	Description
0b	Not Present	Port not present
1b	Present	Port present

DSSM		
		Workaround
		The strap is not connected on the A steppings.

EMRR Mask LSB

EMRRMASK_LSB - EMRR Mask LSB		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	09208h	
EMRR Mask Value		
DWord	**Bit**	**Description**
0	31:12	**EMRR MASK LSB BITS** Access: RO EMRR MASK VALUE.
	11	**EMRR ENABLE** Access: RO EMRR Enable.
	10	**EMRR LOCK** Access: RO EMRR LOCK bit.
	9:0	**Spares** Access: RO

EMRR Mask MSB

EMRRMASK_MSB - EMRR Mask MSB		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	0920Ch	
EMRR Mask Value		
DWord	**Bit**	**Description**
0	31:0	**EMRR MASK MSB BITS** Access: RO EMRR MASK VALUE.

Error Identity Register

EIR - Error Identity Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	020B0h-020B3h
Name:	Error Identity Register
ShortName:	EIR_RCSUNIT
Address:	180B0h-180B3h
Name:	Error Identity Register
ShortName:	EIR_POCSUNIT
Address:	220B0h-220B3h
Name:	Error Identity Register
ShortName:	EIR_BCSUNIT
Address:	1C00B0h-1C00B3h
Name:	Error Identity Register
ShortName:	EIR_VCSUNIT0
Address:	1C40B0h-1C40B3h
Name:	Error Identity Register
ShortName:	EIR_VCSUNIT1
Address:	1C80B0h-1C80B3h
Name:	Error Identity Register
ShortName:	EIR_VECSUNIT0
Address:	1D00B0h-1D00B3h
Name:	Error Identity Register
ShortName:	EIR_VCSUNIT2
Address:	1D40B0h-1D40B3h
Name:	Error Identity Register
ShortName:	EIR_VCSUNIT3
Address:	1D80B0h-1D80B3h
Name:	Error Identity Register
ShortName:	EIR_VECSUNIT1

EIR - Error Identity Register

Address:	1E00B0h-1E00B3h
Name:	Error Identity Register
ShortName:	EIR_VCSUNIT4

Address:	1E40B0h-1E40B3h
Name:	Error Identity Register
ShortName:	EIR_VCSUNIT5

Address:	1E80B0h-1E80B3h
Name:	Error Identity Register
ShortName:	EIR_VECSUNIT2

Address:	1F00B0h-1F00B3h
Name:	Error Identity Register
ShortName:	EIR_VCSUNIT6

Address:	1F40B0h-1F40B3h
Name:	Error Identity Register
ShortName:	EIR_VCSUNIT7

Address:	1F80B0h-1F80B3h
Name:	Error Identity Register
ShortName:	EIR_VECSUNIT3

The EIR register contains the persistent values of Hardware-Detected Error Condition bits. Any bit set in this register will cause the Master Error bit in the ISR to be set. The EIR register is also used by software to clear detected errors (by writing a 1 to the appropriate bit(s)), except for the unrecoverable bits described.)

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask
	15:0	**Error Identity Bits** This register contains the persistent values of ESR error status bits that are unmasked via the EMR register. (See Table Table 3-3. Hardware-Detected Error Bits). The logical OR of all (defined) bits in this register is reported in the Master Error bit of the Interrupt Status Register. In order to clear an error condition, software must first clear the error by writing a 1 to the appropriate bit(s) in this field. If required, software should then proceed to clear the Master Error bit of the IIR. Reserved bits are RO. Refer the table titled "Hardware-Detected Error Bits" for independent bit defintions. Value: 1h — Name: Error occurred

EIR - Error Identity Register

		Programming Notes
		Writing a 1 to a set bit will cause that error condition to be cleared. However, neither the Page Table Error bit (Bit 4) nor the Instruction Error bit (Bit 0) can be cleared except by reset (i.e., it is a fatal error).

Error Mask Register

EMR - Error Mask Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	020B4h-020B7h
Name:	Error Mask Register
ShortName:	EMR_RCSUNIT
Address:	180B4h-180B7h
Name:	Error Mask Register
ShortName:	EMR_POCSUNIT
Address:	220B4h-220B7h
Name:	Error Mask Register
ShortName:	EMR_BCSUNIT
Address:	1C00B4h-1C00B7h
Name:	Error Mask Register
ShortName:	EMR_VCSUNIT0
Address:	1C40B4h-1C40B7h
Name:	Error Mask Register
ShortName:	EMR_VCSUNIT1
Address:	1C80B4h-1C80B7h
Name:	Error Mask Register
ShortName:	EMR_VECSUNIT0
Address:	1D00B4h-1D00B7h
Name:	Error Mask Register
ShortName:	EMR_VCSUNIT2
Address:	1D40B4h-1D40B7h
Name:	Error Mask Register
ShortName:	EMR_VCSUNIT3
Address:	1D80B4h-1D80B7h
Name:	Error Mask Register
ShortName:	EMR_VECSUNIT1

EMR - Error Mask Register

Address:	1E00B4h-1E00B7h
Name:	Error Mask Register
ShortName:	EMR_VCSUNIT4

Address:	1E40B4h-1E40B7h
Name:	Error Mask Register
ShortName:	EMR_VCSUNIT5

Address:	1E80B4h-1E80B7h
Name:	Error Mask Register
ShortName:	EMR_VECSUNIT2

Address:	1F00B4h-1F00B7h
Name:	Error Mask Register
ShortName:	EMR_VCSUNIT6

Address:	1F40B4h-1F40B7h
Name:	Error Mask Register
ShortName:	EMR_VCSUNIT7

Address:	1F80B4h-1F80B7h
Name:	Error Mask Register
ShortName:	EMR_VECSUNIT3

The EMR register is used by software to control which Error Status Register bits are masked or unmasked. Unmasked bits will be reported in the EIR, thus setting the Master Error ISR bit and possibly triggering a CPU interrupt, and will persist in the EIR until cleared by software. Masked bits will not be reported in the EIR and therefore cannot generate Master Error conditions or CPU interrupts. Reserved bits are RO.

DWord	Bit	Description
0	31:8	**Reserved** Default Value: FFFFFFh Format: PBC **Programming Notes** These bits are not implemented in HW and must be set to '1'
	7:0	**Error Mask Bits** This register contains a bit mask that selects which error condition bits (from the ESR) are reported in the EIR. Refer the table titled "Hardware-Detected Error Bits" for independent bit defintions. Value: FFh — Name: **[Default]** — Description:

EMR - Error Mask Register				
		0h	Not Masked	Will be reported in the EIR
		1h	Masked	Will not be reported in the EIR

Error Status Register

ESR - Error Status Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	020B8h-020BBh
Name:	Error Status Register
ShortName:	ESR_RCSUNIT
Address:	180B8h-180BBh
Name:	Error Status Register
ShortName:	ESR_POCSUNIT
Address:	220B8h-220BBh
Name:	Error Status Register
ShortName:	ESR_BCSUNIT
Address:	1C00B8h-1C00BBh
Name:	Error Status Register
ShortName:	ESR_VCSUNIT0
Address:	1C40B8h-1C40BBh
Name:	Error Status Register
ShortName:	ESR_VCSUNIT1
Address:	1C80B8h-1C80BBh
Name:	Error Status Register
ShortName:	ESR_VECSUNIT0
Address:	1D00B8h-1D00BBh
Name:	Error Status Register
ShortName:	ESR_VCSUNIT2
Address:	1D40B8h-1D40BBh
Name:	Error Status Register
ShortName:	ESR_VCSUNIT3
Address:	1D80B8h-1D80BBh
Name:	Error Status Register
ShortName:	ESR_VECSUNIT1

ESR - Error Status Register

Address:	1E00B8h-1E00BBh
Name:	Error Status Register
ShortName:	ESR_VCSUNIT4

Address:	1E40B8h-1E40BBh
Name:	Error Status Register
ShortName:	ESR_VCSUNIT5

Address:	1E80B8h-1E80BBh
Name:	Error Status Register
ShortName:	ESR_VECSUNIT2

Address:	1F00B8h-1F00BBh
Name:	Error Status Register
ShortName:	ESR_VCSUNIT6

Address:	1F40B8h-1F40BBh
Name:	Error Status Register
ShortName:	ESR_VCSUNIT7

Address:	1F80B8h-1F80BBh
Name:	Error Status Register
ShortName:	ESR_VECSUNIT3

The ESR register contains the current values of all Hardware-Detected Error condition bits (these are all by definition persistent). The EMR register selects which of these error conditions are reported in the persistent EIR (i.e., set bits must be cleared by software) and thereby causing a Master Error interrupt condition to be reported in the ISR.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**Error Status Bits** This register contains the non-persistent values of all hardware-detected error condition bits. Refer the table titled "Hardware-Detected Error Bits" for independent bit defintions. Value: 1h — Name: Error Condition Detected

EU_GRF_CLEAR

EU_GRF_CLEAR - EU_GRF_CLEAR	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0E550h
Name:	EU_GRF_CLEAR
ShortName:	EU_GRF_CLEAR

This is a basic register template

DWord	Bit	Description	
0	31:0	**GRF_CLEAR**	
		Default Value:	0000000000000000b
		Access:	RO

EU Mask Programming

TD_PM_MODE_EUCOUNT - EU Mask Programming

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	WO
Size (in bits):	32
Address:	0E4F8h
Name:	EU Mask Programming
ShortName:	TD_PM_MODE_EUCOUNT

DWord	Bit	Description
0	31:8	**Reserved** Format: MBZ
	7	**EU 7 Enable** Format: Enable Value 0: Enabled **[Default]** Value 1: Disabled
	6	**EU 6 Enable** Format: Enable Value 0: Enabled **[Default]** Value 1: Disabled
	5	**EU 5 Enable** Format: Enable Value 0: Enabled **[Default]** Value 1: Disabled
	4	**EU 4 Enable** Format: Enable

TD_PM_MODE_EUCOUNT - EU Mask Programming

		Value: 0 — Enabled **[Default]** Value: 1 — Disabled
	3	**EU 3 Enable** Format: Enable Value: 0 — Enabled **[Default]** Value: 1 — Disabled
	2	**EU 2 Enable** Format: Enable Value: 0 — Enabled **[Default]** Value: 1 — Disabled
	1	**EU 1 Enable** Format: Enable Value: 0 — Enabled **[Default]** Value: 1 — Disabled
	0	**EU 0 Enable** Format: Enable Value: 0 — Enabled **[Default]** Value: 1 — Disabled

EUP1 BONUS2 Reg

EUP1SPCBONUS2 - EUP1 BONUS2 Reg		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	24698h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:8	**Reserved** Access: RO Reserved
	7	**BONUS2 BIT 7** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS2 BIT 6** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS2 BIT 5** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS2 BIT 4** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	3	**BONUS2 BIT 3** Access: R/W

EUP1SPCBONUS2 - EUP1 BONUS2 Reg		
		SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS2 BIT 2** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS2 BIT 1** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS2 BIT 0** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

EUP1 BONUS11 Reg

EUP1SPCBONUS1 - EUP1 BONUS11 Reg		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	24694h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:8	**Reserved** Access: RO Reserved
	7	**BONUS1 BIT 7** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS1 BIT 6** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS1 BIT 5** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS1 BIT 4** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	3	**BONUS1 BIT 3** Access: R/W

EUP1SPCBONUS1 - EUP1 BONUS11 Reg

		SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS1 BIT 2** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS1 BIT 1** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS1 BIT 0** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

EUP2 BONUS1 Reg

EUP2SPCBONUS1 - EUP2 BONUS1 Reg		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	24714h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:8	**Reserved** Access: RO Reserved
	7	**BONUS1 BIT 7** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS1 BIT 6** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS1 BIT 5** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS1 BIT 4** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	3	**BONUS1 BIT 3** Access: R/W

EUP2SPCBONUS1 - EUP2 BONUS1 Reg		
		SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS1 BIT 2** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS1 BIT 1** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS1 BIT 0** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

EUP2 BONUS2 Reg

EUP2SPCBONUS2 - EUP2 BONUS2 Reg		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	24718h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:8	**Reserved** Access: RO Reserved
	7	**BONUS2 BIT 7** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS2 BIT 6** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS2 BIT 5** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS2 BIT 4** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	3	**BONUS2 BIT 3** Access: R/W

EUP2SPCBONUS2 - EUP2 BONUS2 Reg

		SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS2 BIT 2** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS2 BIT 1** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS2 BIT 0** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

EUP 2 Power Down FSM control register with lock

EUP2SPCPOWERDNFSMCTL - EUP 2 Power Down FSM control register with lock		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	24710h	
DWord	**Bit**	**Description**
0	31	**power down control Lock** Access: R/W Lock 0 = Bits of EU PAIR 0 POWERDNFSMCTL register are R/W 1 = All bits of EU PAIR 0 POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:13	**Reserved** Access: RO Reserved
	12	**Leave firewall disabled** Access: R/W Lock When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e dont firewall the gated domain, but complete logical flow
	11	**Leave reset de-asserted** Access: R/W Lock When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e dont assert reset, but complete logical flow
	10	**Leave CLKs ON** Access: R/W Lock

EUP2SPCPOWERDNFSMCTL - EUP 2 Power Down FSM control register with lock

		When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e dont clock gate, but complete logical flow
	9	**Leave FET On** Access: R/W Lock When This bit is set SPC will not turn off the PFET eventhough it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e dont power off pfet, but complete logical flow
	8:6	**Power Down state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Gate Clocks
	5:3	**Power Down state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default :Firewall ON
	2:0	**Power Down state 1** Default Value: 000b Access: R/W Lock This will be the 1st state before power is turned OFF in the well Encodings: 000 = Assert Reset

EUP2SPCPOWERDNFSMCTL - EUP 2 Power Down FSM control register with lock		
		001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Assert Reset

EUP 2 Power on FSM control register with lock

EUP2SPCPOWERUPFSMCTL - EUP 2 Power on FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	2470Ch

DWord	Bit	Description
0	31	**power up control Lock** Access: R/W Lock 0 = Bits of EU PAIR 0 POWERUPFSMCTL register are R/W 1 = All bits of EU PAIR 0 POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:9	**Reserved** Access: RO Reserved
	8:6	**Power UP state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - De-assert resets 3'b000: 10ns (or 1 bclk)
	5:3	**Power UP state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF

		010 = De-assert resets 1xx = Rsvd for future Default - Firewall OFF
	2:0	**Power UP state 1** Default Value: 000b Access: R/W Lock This will be the 1st state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Clock Ungate

EUP3 BONUS1 Reg

EUP3SPCBONUS1 - EUP3 BONUS1 Reg		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	24794h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:8	**Reserved** Access: RO Reserved
	7	**BONUS1 BIT 7** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS1 BIT 6** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS1 BIT 5** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS1 BIT 4** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	3	**BONUS1 BIT 3** Access: R/W

EUP3SPCBONUS1 - EUP3 BONUS1 Reg

		SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS1 BIT 2** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS1 BIT 1** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS1 BIT 0** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

EUP3 BONUS2 Reg

EUP3SPCBONUS2 - EUP3 BONUS2 Reg		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	24798h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:8	**Reserved** Access: RO Reserved
	7	**BONUS2 BIT 7** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS2 BIT 6** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS2 BIT 5** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS2 BIT 4** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	3	**BONUS2 BIT 3** Access: R/W

EUP3SPCBONUS2 - EUP3 BONUS2 Reg

		SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS2 BIT 2** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS2 BIT 1** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS2 BIT 0** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

EU PAIR 1 PFET control register with lock

EUP1SPCPFETCTL - EU PAIR 1 PFET control register with lock		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	24688h	
DWord	**Bit**	**Description**
0	31	**PFET Control Lock** Access: R/W Lock 0 = Bits of EU PAIR 1 PGFETCTL register are R/W 1 = All bits of EU PAIR 1 PGFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:24	**Reserved** Access: RO Reserved
	23	**Power Well Status** Access: RO 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	22	**Powergood timer error** Access: RO 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	21:19	**Delay from enabling secondary PFETs to power good.** Default Value: 100b Access: R/W Lock Delay from enabling secondary PFETs to power good

EUP1SPCPFETCTL - EU PAIR 1 PFET control register with lock

3'b000: 40ns
3'b001: 80ns
3'b010: 160ns
3'b011: 240ns
3'b100: 320ns
3'b101: 480ns
3'b110: 640ns
3'b111: 1280ns

18:16 **Strobe pulse period**

Access:	R/W Lock

Time period b/w two adjacent strobes to the primary FETs
3'b000: 10ns (or 1 bclk)
3'b001: 20ns (or 2 bclk)
3'b010: 30ns (or 3 bclk)
3'b111: 80ns (or 8 bclk)

Value	Name
001b	**[Default]**

15:0 **PFET Ladder Step Sequence**

Default Value:	1111111111111111b
Access:	R/W Lock

PFET Ladder STEP sequence
The PFET ladder has 16 steps, each represented by its corresponding bit in pfetlddrstepseq[15:0]. If the bit location is set, it means we must step on that ladder stage before we go to the next stage.
The SPC controller will step through all the steps with asserted bits periodically with period equal to strbpulsprd[2:0]
Programming Rule: pfetldrstepseq[15] and pfetldrstepseq[0] must be '1; A '0 setting for these bits is illegal.
15'FFFFh: Ladder step (ladder_sel) goes 0, 1, 2, ?.15.
15'FFF1h: Ladder step goes 0, 4, 5, 6,?15; Steps 1, 2, 3 are skipped.
15'D555h: Ladder step goes 0, 2, 4, 6, 8, 10, 12, 14, 15; Steps 1, 3, 5, 7, 9, 11, 13 are skipped.
15'80001h: Ladder step goes 0, 15; Steps 1, 2, 3, 4, ?14 are skipped.

EU PAIR 1 Power Context Save request

EUP1PGCTXREQ - EU PAIR 1 Power Context Save request		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	24684h	
DWord	**Bit**	**Description**
0	31:16	**Message Mask** Access: RO Message Mask bots for lower 16 bits
	15:10	**Reserved** Access: RO Reserved
	9	**Power context save request** Access: R/W Set Power Context Save Request 1'b0 : Power context save is not being requested 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

EU PAIR 1 Power Down FSM control register with lock

EUP1SPCPOWERDNFSMCTL - EU PAIR 1 Power Down FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	24690h

DWord	Bit	Description
0	31	**power down control Lock** Access: R/W Lock 0 = Bits of EU PAIR 0 POWERDNFSMCTL register are R/W 1 = All bits of EU PAIR 0 POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:13	**Reserved** Access: RO Reserved
	12	**Leave firewall disabled** Access: R/W Lock When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e dont firewall the gated domain, but complete logical flow
	11	**Leave reset de-asserted** Access: R/W Lock When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e dont assert reset, but complete logical flow
	10	**Leave CLKs ON** Access: R/W Lock

EUP1SPCPOWERDNFSMCTL - EU PAIR 1 Power Down FSM control register with lock

		When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e dont clock gate, but complete logical flow
	9	**Leave FET On** Access: R/W Lock When This bit is set SPC will not turn off the PFET eventhough it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e dont power off pfet, but complete logical flow
	8:6	**Power Down state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Gate Clocks
	5:3	**Power Down state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default :Firewall ON
	2:0	**Power Down state 1** Default Value: 000b Access: R/W Lock This will be the 1st state before power is turned OFF in the well Encodings: 000 = Assert Reset

EUP1SPCPOWERDNFSMCTL - EU PAIR 1 Power Down FSM control register with lock		
		001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Assert Reset

EU PAIR 1 Power Gate Control Request

EUP1PGCTLREQ - EU PAIR 1 Power Gate Control Request		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	24680h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:16	**Message Mask** Access: RO Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:2	**Reserved** Access: RO Reserved
	1	**CLK RST FWE Request** Access: R/W EU PAIR 0 CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**Power Gate Request** Access: R/W EU PAIR 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

EU PAIR 1 Power on FSM control register with lock

EUP1SPCPOWERUPFSMCTL - EU PAIR 1 Power on FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	2468Ch

DWord	Bit	Description
0	31	**power up control Lock** Access: R/W Lock 0 = Bits of EU PAIR 0 POWERUPFSMCTL register are R/W 1 = All bits of EU PAIR 0 POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:9	**Reserved** Access: RO Reserved
	8:6	**Power UP state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - De-assert resets 3'b000: 10ns (or 1 bclk)
	5:3	**Power UP state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF

		010 = De-assert resets 1xx = Rsvd for future Default - Firewall OFF
	2:0	**Power UP state 1** Default Value: 000b Access: R/W Lock This will be the 1st state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Clock Ungate

EU PAIR 2 PGFET control register with lock

EUP2SPCPFETCTL - EU PAIR 2 PGFET control register with lock		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	24708h	
DWord	**Bit**	**Description**
0	31	**PFET Control Lock** Access: R/W Lock 0 = Bits of EU PAIR 0 PGFETCTL register are R/W 1 = All bits of EU PAIR 0 PGFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:24	**Reserved** Access: RO Reserved
	23	**Power Well Status** Access: RO 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	22	**Powergood timer error** Access: RO 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	21:19	**Delay from enabling secondary PFETs to power good.** Default Value: 100b Access: R/W Lock Delay from enabling secondary PFETs to power good

EUP2SPCPFETCTL - EU PAIR 2 PGFET control register with lock

		3'b000: 40ns 3'b001: 80ns 3'b010: 160ns 3'b011: 240ns 3'b100: 320ns 3'b101: 480ns 3'b110: 640ns 3'b111: 1280ns
	18:16	**Stroble pulse period** Access: R/W Lock Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk) **Value** / **Name** 001b / **[Default]**
	15:0	**PFET Ladder Step Sequence** Default Value: 1111111111111111b Access: R/W Lock PFET Ladder STEP sequence The PFET ladder has 16 steps, each represented by its corresponding bit in pfetlddrstepseq[15:0]. If the bit location is set, it means we must step on that ladder stage before we go to the next stage. The SPC controller will step through all the steps with asserted bits periodically with period equal to strbpulsprd[2:0] Programming Rule: pfetldrstepseq[15] and pfetldrstepseq[0] must be '1; A '0 setting for these bits is illegal. 15'FFFFh: Ladder step (ladder_sel) goes 0, 1, 2, ?.15. 15'FFF1h: Ladder step goes 0, 4, 5, 6,?15; Steps 1, 2, 3 are skipped. 15'D555h: Ladder step goes 0, 2, 4, 6, 8, 10, 12, 14, 15; Steps 1, 3, 5, 7, 9, 11, 13 are skipped. 15'80001h: Ladder step goes 0, 15; Steps 1, 2, 3, 4, ?14 are skipped.

EU PAIR 2 Power Context Save request

EUP2PGCTXREQ - EU PAIR 2 Power Context Save request		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	24704h	
DWord	**Bit**	**Description**
0	31:16	**Message Mask** Access: RO Message Mask bots for lower 16 bits
	15:10	**Reserved** Access: RO Reserved
	9	**Power context save request** Access: R/W Set Power Context Save Request 1'b0 : Power context save is not being requested 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

EU PAIR 2 Power Gate Control Request

EUP2PGCTLREQ - EU PAIR 2 Power Gate Control Request		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	24700h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:16	**Message Mask** Access: RO Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:2	**Reserved** Access: RO Reserved
	1	**CLK RST FWE Request** Access: R/W EU PAIR 0 CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**Power Gate Request** Access: R/W EU PAIR 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

EU PAIR 3 PGFET control register with lock

EUP3SPCPFETCTL - EU PAIR 3 PGFET control register with lock		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	24788h	
DWord	**Bit**	**Description**
0	31	**PFET Control Lock** Access: R/W Lock 0 = Bits of EU PAIR 0 PGFETCTL register are R/W 1 = All bits of EU PAIR 0 PGFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:24	**Reserved** Access: RO Reserved
	23	**Power Well Status** Access: RO 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	22	**Powergood timer error** Access: RO 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	21:19	**Delay from enabling secondary PFETs to power good.** Default Value: 100b Access: R/W Lock Delay from enabling secondary PFETs to power good

EUP3SPCPFETCTL - EU PAIR 3 PGFET control register with lock

		3'b000: 40ns 3'b001: 80ns 3'b010: 160ns 3'b011: 240ns 3'b100: 320ns 3'b101: 480ns 3'b110: 640ns 3'b111: 1280ns
	18:16	**Time period last primay pfet strobe to secondary pfet strobe** Access: R/W Lock Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk) **Value** / **Name** 001b / **[Default]**
	15:0	**PFET Ladder Step Sequence** Default Value: 1111111111111111b Access: R/W Lock PFET Ladder STEP sequence The PFET ladder has 16 steps, each represented by its corresponding bit in pfetlddrstepseq[15:0]. If the bit location is set, it means we must step on that ladder stage before we go to the next stage. The SPC controller will step through all the steps with asserted bits periodically with period equal to strbpulsprd[2:0] Programming Rule: pfetldrstepseq[15] and pfetldrstepseq[0] must be '1; A '0 setting for these bits is illegal. 15'FFFFh: Ladder step (ladder_sel) goes 0, 1, 2, ?.15. 15'FFF1h: Ladder step goes 0, 4, 5, 6,?15; Steps 1, 2, 3 are skipped. 15'D555h: Ladder step goes 0, 2, 4, 6, 8, 10, 12, 14, 15; Steps 1, 3, 5, 7, 9, 11, 13 are skipped. 15'80001h: Ladder step goes 0, 15; Steps 1, 2, 3, 4, ?14 are skipped.

EU PAIR 3 Power Context Save request

EUP3PGCTXREQ - EU PAIR 3 Power Context Save request		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	24784h	

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO Message Mask bots for lower 16 bits
	15:10	**Reserved** Access: RO Reserved
	9	**Power context save request** Access: R/W Set Power Context Save Request 1'b0 : Power context save is not being requested 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

EU PAIR 3 Power Down FSM control register with lock

EUP3SPCPOWERDNFSMCTL - EU PAIR 3 Power Down FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	24790h

DWord	Bit	Description
0	31	**power down control Lock** Access: R/W Lock 0 = Bits of EU PAIR 0 POWERDNFSMCTL register are R/W 1 = All bits of EU PAIR 0 POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:13	**Reserved** Access: RO Reserved
	12	**Leave firewall disabled** Access: R/W Lock When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e dont firewall the gated domain, but complete logical flow
	11	**Leave reset de-asserted** Access: R/W Lock When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e dont assert reset, but complete logical flow
	10	**Leave CLKs ON** Access: R/W Lock

EUP3SPCPOWERDNFSMCTL - EU PAIR 3 Power Down FSM control register with lock

		When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e dont clock gate, but complete logical flow
	9	**Leave FET On** Access: R/W Lock When This bit is set SPC will not turn off the PFET eventhough it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e dont power off pfet, but complete logical flow
	8:6	**Power Down state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Gate Clocks
	5:3	**Power Down state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default :Firewall ON
	2:0	**Power Down state 1** Default Value: 000b Access: R/W Lock This will be the 1st state before power is turned OFF in the well Encodings: 000 = Assert Reset

EUP3SPCPOWERDNFSMCTL - EU PAIR 3 Power Down FSM control register with lock		
		001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Assert Reset

EU PAIR 3 Power Gate Control Request

EUP3PGCTLREQ - EU PAIR 3 Power Gate Control Request		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	24780h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:16	**Message Mask** Access: RO Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:2	**Reserved** Access: RO Reserved
	1	**CLK RST FWE Request** Access: R/W EU PAIR 0 CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**Power Gate Request** Access: R/W EU PAIR 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

EU PAIR 3 Power on FSM control register with lock

EUP3SPCPOWERUPFSMCTL - EU PAIR 3 Power on FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	2478Ch

DWord	Bit	Description
0	31	**power up control Lock** Access: R/W Lock 0 = Bits of EU PAIR 0 POWERUPFSMCTL register are R/W 1 = All bits of EU PAIR 0 POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:9	**Reserved** Access: RO Reserved
	8:6	**Power UP state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - De-assert resets 3'b000: 10ns (or 1 bclk)
	5:3	**Power UP state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets

		1xx = Rsvd for future Default - Firewall OFF
	2:0	**Power UP state 1** Default Value: 000b Access: R/W Lock This will be the 1st state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Clock Ungate

Exec-List Context Offset

CXT_EL_OFFSET - Exec-List Context Offset	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	021ACh-021AFh
Name:	Exec-List Context Offset
ShortName:	CXT_EL_OFFSET_RCSUNIT
Address:	181ACh-181AFh
Name:	Exec-List Context Offset
ShortName:	CXT_EL_OFFSET_POCSUNIT
Address:	221ACh-221AFh
Name:	Exec-List Context Offset
ShortName:	CXT_EL_OFFSET_BCSUNIT
Address:	1C01ACh-1C01AFh
Name:	Exec-List Context Offset
ShortName:	CXT_EL_OFFSET_VCSUNIT0
Address:	1C41ACh-1C41AFh
Name:	Exec-List Context Offset
ShortName:	CXT_EL_OFFSET_VCSUNIT1
Address:	1C81ACh-1C81AFh
Name:	Exec-List Context Offset
ShortName:	CXT_EL_OFFSET_VECSUNIT0
Address:	1D01ACh-1D01AFh
Name:	Exec-List Context Offset
ShortName:	CXT_EL_OFFSET_VCSUNIT2
Address:	1D41ACh-1D41AFh
Name:	Exec-List Context Offset
ShortName:	CXT_EL_OFFSET_VCSUNIT3
Address:	1D81ACh-1D81AFh
Name:	Exec-List Context Offset
ShortName:	CXT_EL_OFFSET_VECSUNIT1
Address:	1E01ACh-1E01AFh

CXT_EL_OFFSET - Exec-List Context Offset

Name:	Exec-List Context Offset
ShortName:	CXT_EL_OFFSET_VCSUNIT4
Address:	1E41ACh-1E41AFh
Name:	Exec-List Context Offset
ShortName:	CXT_EL_OFFSET_VCSUNIT5
Address:	1E81ACh-1E81AFh
Name:	Exec-List Context Offset
ShortName:	CXT_EL_OFFSET_VECSUNIT2
Address:	1F01ACh-1F01AFh
Name:	Exec-List Context Offset
ShortName:	CXT_EL_OFFSET_VCSUNIT6
Address:	1F41ACh-1F41AFh
Name:	Exec-List Context Offset
ShortName:	CXT_EL_OFFSET_VCSUNIT7
Address:	1F81ACh-1F81AFh
Name:	Exec-List Context Offset
ShortName:	CXT_EL_OFFSET_VECSUNIT3

This register provides the layout format of LRCA in Exec-List mode of scheduling. Each field represents its location in 4KB offset from LRCA base address. Register gets initialized to default value coming out of reset. SW must not program this register.

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:20	**CSFE Engine Context Size** Value: 6h — Name: **[Default]**
	19:16	**Ring Context Offset** Default Value: 1h
	15:13	**Ring Context Size** Value: 5h — Name: **[Default]**
	12:4	**Reserved** Format: MBZ
	3:0	**PerProcess HW Status Page Offset** Default Value: 0h

Execlist Control Register

EXECLIST_CONTROL - Execlist Control Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	WO
Size (in bits):	32
Address:	02550h-02553h
Name:	EXECLIST CONTROL
ShortName:	EXECLIST_CONTROL_RCSUNIT
Address:	18550h-18553h
Name:	EXECLIST CONTROL
ShortName:	EXECLIST_CONTROL_POCSUNIT
Address:	22550h-22553h
Name:	EXECLIST CONTROL
ShortName:	EXECLIST_CONTROL_BCSUNIT
Address:	1C0550h-1C0553h
Name:	EXECLIST CONTROL
ShortName:	EXECLIST_CONTROL_VCSUNIT0
Address:	1C4550h-1C4553h
Name:	EXECLIST CONTROL
ShortName:	EXECLIST_CONTROL_VCSUNIT1
Address:	1C8550h-1C8553h
Name:	EXECLIST CONTROL
ShortName:	EXECLIST_CONTROL_VECSUNIT0
Address:	1D0550h-1D0553h
Name:	EXECLIST CONTROL
ShortName:	EXECLIST_CONTROL_VCSUNIT2

EXECLIST_CONTROL - Execlist Control Register

Address:	1D4550h-1D4553h
Name:	EXECLIST CONTROL
ShortName:	EXECLIST_CONTROL_VCSUNIT3

Address:	1D8550h-1D8553h
Name:	EXECLIST CONTROL
ShortName:	EXECLIST_CONTROL_VECSUNIT1

Address:	1E0550h-1E0553h
Name:	EXECLIST CONTROL
ShortName:	EXECLIST_CONTROL_VCSUNIT4

Address:	1E4550h-1E4553h
Name:	EXECLIST CONTROL
ShortName:	EXECLIST_CONTROL_VCSUNIT5

Address:	1E8550h-1E8553h
Name:	EXECLIST CONTROL
ShortName:	EXECLIST_CONTROL_VECSUNIT2

Address:	1F0550h-1F0553h
Name:	EXECLIST CONTROL
ShortName:	EXECLIST_CONTROL_VCSUNIT6

Address:	1F4550h-1F4553h
Name:	EXECLIST CONTROL
ShortName:	EXECLIST_CONTROL_VCSUNIT7

Address:	1F8550h-1F8553h
Name:	EXECLIST CONTROL
ShortName:	EXECLIST_CONTROL_VECSUNIT3

DWord	Bit	Description
0	31:3	**Reserved**
	2	**Use HW Element Pointer** HW element pointer gets saved on a context getting preempted due to Preempt to Idle (indicates

EXECLIST_CONTROL - Execlist Control Register		
		the element number of the preempted context in the EQ). On a load following Preempt to Idle SW can set "Use Element Pointer" to indicate HW to resume from the element on which preemption has occurred due to Preempt to Idle, not setting “Use Element Pointer” will result in HW executing from Element-0. o UseHWElementPointer = 1 : HW saves its position in the N deep execution Q across any C6 events. When HW sees Load + UseHWElementPointer, HW will restart execution at the element pointed to by the Element Pointer. • This usage is only expected post a PreemptToIdle message, and is independent of C6 entry-exit in between PreemptToIdle and Load. • Load+UseHWElementPointer on the first load (out of reset) will cause execution to begin at the first valid element in the Q • Load+UseHWElementPointer without a preceding PreemptToIdle (i.e. when trying to Preempt a currently running Q) will cause undefined behaviour. o UseHWElementPointer = 0 : HW begins execution at the first valid element in the Q.
	1	**Preempt to Idle** When SW writes a 1 to this bit, HW will immediately copy the contents of the Execution queue into the Submission queue. HW will preempt the executing context on appropriate preemption boundary, saves state and invalidates all the pending elements of the execution queue to be executed. HW saves the element pointer of the EQ on which it got preempted (indicates the element number of the preempted context in the EQ), element pointer is power context save/restored by HW. This forces HW to go idle triggering idle sequence for power management. A Preempt-to-idle message must be followed by a Load message to resume operation. This Load message may occur before or after a power gating/C6 sequence
	0	**Load** Writing to the Load bit triggers HW to sample Submission Queue (SQ) to Execution Queue (EQ) and start executing from Element-0 of Execution Queue. Doing a Load during an ongoing execution of an context will result in preemption and the new submission queue gets sampled to Execution Queue, however HW will not start executing from the newly updated Execution Queue until the preempted context is completely saved. Multiple loads occurring during the preemption of an executing context will result in EQ getting updated multiple times with the SQ and engine will only execute the most up to date EQ available upon completion of the preemption.

Execlist Status

EXECLIST_STATUS - Execlist Status	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	64
Address:	02234h-0223Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_RCSUNIT
Address:	18234h-1823Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_POCSUNIT
Address:	22234h-2223Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_BCSUNIT
Address:	1C0234h-1C023Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_VCSUNIT0
Address:	1C4234h-1C423Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_VCSUNIT1
Address:	1C8234h-1C823Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_VECSUNIT0
Address:	1D0234h-1D023Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_VCSUNIT2
Address:	1D4234h-1D423Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_VCSUNIT3
Address:	1D8234h-1D823Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_VECSUNIT1

EXECLIST_STATUS - Execlist Status

Address:	1E0234h-1E023Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_VCSUNIT4

Address:	1E4234h-1E423Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_VCSUNIT5

Address:	1E8234h-1E823Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_VECSUNIT2

Address:	1F0234h-1F023Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_VCSUNIT6

Address:	1F4234h-1F423Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_VCSUNIT7

Address:	1F8234h-1F823Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_VECSUNIT3

This register contains the pointers and full indicator for the Execlist Queue and the context ID of the currently running context. DefaultValue = UUUU UUU1h (4:0 default to 00001b, others UNDEFINED).

Programming Notes	Source
This register functionality is not supported and must not be programmed for Position command streamer.	PositionCS

DWord	Bit	Description
0	63:32	**Current Context ID** Format: U32 Contains the context ID of the currently running context.
	31	**Reserved** Format: MBZ
	30	**Pending Load** Format: U1 When set indicates the Load of SQ to EQ is complete. Hardware is in the process of making the first valid element of the EQ to be active (executing).

EXECLIST_STATUS - Execlist Status

29:28	**Reserved** Format: MBZ
27	**Arbitration Enable** Format: U1 This field reflects the Arbitration Flag set by the MI_ARB_ON_OFF command in Command Streamer.
26:12	**Last Context Switch Reason** Access: R/W Format: U15 **Description** This field contains the switch reason for the last context to switch away, as captured in the Context Status Dword, bits 8:0. **Programming Notes** This field should not written by SW.
11:8	**Active Context Offset** When Active Context field is set, this field indicates the active context offset within the execution queue.
7	**Active Context** When set indicates there is an active context being executed in hardware.
6:5	**Reserved** Format: MBZ
4	**Valid Execution Queue Duplicate** Indicates there is an active context or a pending context or a pending load in progress.
3	**Valid Execution Queue**

EXECLIST_STATUS - Execlist Status

		Indicates there is an active context or a pending context or a pending load in progress.
	2	**Preempt to Idle Pending** Preempt to Idle Pending: HW has received Preempt to Idle load request from the scheduler and hardware is in the process of switching out the active context if any to force HW go IDLE.
	1	**Two Pending Load's** Indicates there are two pending loads in HW, (n-1)th load's first valid element is being pursued by HW to be made active and the Nth load's first valid element will be considered once (N-1)th is active. This situation will arise when Nth load happens while (N-1)th load is pending in hardware. Any further Load (N+1) occurring while this bit is set will result in overwriting the Nth SQ load, that is Nth SQ load contents will never be seen by hardware.
	0	**Execution Queue Invalid** Default Value: 1h There are no contexts available in Execution Queue to be executed. There are no pending loads (including Preempt To Idle) to be processed by the hardware. Scheduler can look for this bit to be set before doing a load of SQ to avoid preemption of any active contexts in hardware.

Execlist Submission Queue Contents

EXECLIST_SQ_CONTENTS - Execlist Submission Queue Contents	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	512
Trusted Type:	1
Address:	02510h-0254Fh
Name:	EXECLIST SQ CONTENTS
ShortName:	EXECLIST_SQ_CONTENTS_RCSUNIT
Address:	18510h-1854Fh
Name:	EXECLIST SQ CONTENTS
ShortName:	EXECLIST_SQ_CONTENTS_POCSUNIT
Address:	22510h-2254Fh
Name:	EXECLIST SQ CONTENTS
ShortName:	EXECLIST_SQ_CONTENTS_BCSUNIT
Address:	1C0510h-1C054Fh
Name:	EXECLIST SQ CONTENTS
ShortName:	EXECLIST_SQ_CONTENTS_VCSUNIT0
Address:	1C4510h-1C454Fh
Name:	EXECLIST SQ CONTENTS
ShortName:	EXECLIST_SQ_CONTENTS_VCSUNIT1
Address:	1C8510h-1C854Fh
Name:	EXECLIST SQ CONTENTS
ShortName:	EXECLIST_SQ_CONTENTS_VECSUNIT0
Address:	1D0510h-1D054Fh
Name:	EXECLIST SQ CONTENTS
ShortName:	EXECLIST_SQ_CONTENTS_VCSUNIT2

EXECLIST_SQ_CONTENTS - Execlist Submission Queue Contents

Address:	1D4510h-1D454Fh
Name:	EXECLIST SQ CONTENTS
ShortName:	EXECLIST_SQ_CONTENTS_VCSUNIT3

Address:	1D8510h-1D854Fh
Name:	EXECLIST SQ CONTENTS
ShortName:	EXECLIST_SQ_CONTENTS_VECSUNIT1

Address:	1E0510h-1E054Fh
Name:	EXECLIST SQ CONTENTS
ShortName:	EXECLIST_SQ_CONTENTS_VCSUNIT4

Address:	1E4510h-1E454Fh
Name:	EXECLIST SQ CONTENTS
ShortName:	EXECLIST_SQ_CONTENTS_VCSUNIT5

Address:	1E8510h-1E854Fh
Name:	EXECLIST SQ CONTENTS
ShortName:	EXECLIST_SQ_CONTENTS_VECSUNIT2

Address:	1F0510h-1F054Fh
Name:	EXECLIST SQ CONTENTS
ShortName:	EXECLIST_SQ_CONTENTS_VCSUNIT6

Address:	1F4510h-1F454Fh
Name:	EXECLIST SQ CONTENTS
ShortName:	EXECLIST_SQ_CONTENTS_VCSUNIT7

Address:	1F8510h-1F854Fh
Name:	EXECLIST SQ CONTENTS
ShortName:	EXECLIST_SQ_CONTENTS_VECSUNIT3

Contents of submission queue from Element-0 to Element-7.

All "Element* Low Dword" have the format of the Bits[31:0] of the "Context Descriptor" definition.

EXECLIST_SQ_CONTENTS - Execlist Submission Queue Contents

All "Element* HighDword" have the format of the Bits[63:32] of the "Context Descriptor" definition.

DWord	Bit	Description
0	31:0	**Element 0 Low DWord** Format: U32
1	31:0	**Element 0 High DWord** Format: U32
2	31:0	**Element 1 Low DWord** Format: U32
3	31:0	**Element 1 High DWord** Format: U32
4	31:0	**Element 2 Low DWord** Format: U32
5	31:0	**Element 2 High DWord** Format: U32
6	31:0	**Element 3 Low DWord** Format: U32
7	31:0	**Element 3 High DWord** Format: U32
8	31:0	**Element 4 Low DWord** Format: U32
9	31:0	**Element 4 High DWord** Format: U32
10	31:0	**Element 5 Low DWord** Format: U32
11	31:0	**Element 5 High DWord** Format: U32
12	31:0	**Element 6 Low DWord** Format: U32
13	31:0	**Element 6 High DWord** Format: U32
14	31:0	**Element 7 Low DWord** Format: U32
15	31:0	**Element 7 High DWord** Format: U32

Execlist Submit Port Register

EXECLIST_SUBMITPORT - Execlist Submit Port Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	WO
Size (in bits):	32
Address:	02230h-02233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_RCSUNIT
Address:	18230h-18233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_POCSUNIT
Address:	22230h-22233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_BCSUNIT
Address:	1C0230h-1C0233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_VCSUNIT0
Address:	1C4230h-1C4233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_VCSUNIT1
Address:	1C8230h-1C8233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_VECSUNIT0
Address:	1D0230h-1D0233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_VCSUNIT2
Address:	1D4230h-1D4233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_VCSUNIT3
Address:	1D8230h-1D8233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_VECSUNIT1

EXECLIST_SUBMITPORT - Execlist Submit Port Register

Address:	1E0230h-1E0233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_VCSUNIT4

Address:	1E4230h-1E4233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_VCSUNIT5

Address:	1E8230h-1E8233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_VECSUNIT2

Address:	1F0230h-1F0233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_VCSUNIT6

Address:	1F4230h-1F4233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_VCSUNIT7

Address:	1F8230h-1F8233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_VECSUNIT3

ELSP provides a mechanism to load the elements of the Submission Queue in a cyclic order starting from Element-0 to Element-7. Consecutive writes to ELSP results in progressively updating lower dword followed by upper dword of successive elements starting from Element-0 to Element7. On reaching upper dword of Element-7 it wraps back to lower dword of Element-0.
Example: The first dword write to ELSP results in updating the lower dword of Element-0 and the following write updates the upper dword of Element-0 and the following write updates the lower dword of Element-1 and so on, on updating upper dword of Element-7 it wraps back to lower dword of Element-0.

DWord	Bit	Description
0	31:0	**Context Descriptor DW** Format: Context Descriptor See "Context Descriptor Format" for format. The element that this DW is submitted as and whether it is the high DW or the low DW is determined by order. This register must be written to 16 times in order to write to all the eight elments of an Submission Queue. .

Execute Condition Code Register

EXCC - Execute Condition Code Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	02028h-0202Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_RCSUNIT
Address:	18028h-1802Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_POCSUNIT
Address:	22028h-2202Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_BCSUNIT
Address:	1C0028h-1C002Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_VCSUNIT0
Address:	1C4028h-1C402Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_VCSUNIT1
Address:	1C8028h-1C802Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_VECSUNIT0
Address:	1D0028h-1D002Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_VCSUNIT2
Address:	1D4028h-1D402Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_VCSUNIT3
Address:	1D8028h-1D802Bh
Name:	Execute Condition Code Register

EXCC - Execute Condition Code Register

ShortName:	EXCC_VECSUNIT1
Address:	1E0028h-1E002Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_VCSUNIT4
Address:	1E4028h-1E402Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_VCSUNIT5
Address:	1E8028h-1E802Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_VECSUNIT2
Address:	1F0028h-1F002Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_VCSUNIT6
Address:	1F4028h-1F402Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_VCSUNIT7
Address:	1F8028h-1F802Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_VECSUNIT3

This register contains user defined and hardware generated conditions that are used by MI_WAIT_FOR_EVENT commands. An MI_WAIT_FOR_EVENT instruction excludes the executing ring from arbitration if the selected event evaluates to a 1, while instruction is discarded if the condition evaluates to a 0. Once excluded a ring is enabled into arbitration when the selected condition evaluates to a 0. This register also contains control for the invalidation of indirect state pointers on context restore.

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask These bits serves as a write enable for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.
	15	**Context Wait for V-blank on Pipe-D** This field when set indicates the corresponding context has executed MI_WAIT_FOR_EVENT with "Display Pipe C Vertical Blank Wait Enable" set. This is an internal HW flag and should not be accessed by SW.

EXCC - Execute Condition Code Register

	14	**Context Wait for V-blank on Pipe-C** Source: RenderCS, BlitterCS This field when set indicates the corresponding context has executed MI_WAIT_FOR_EVENT with "Display Pipe C Vertical Blank Wait Enable" set. This is an internal HW flag and should not be accessed by SW.
	13	**Context Wait for V-blank on Pipe-B** Source: RenderCS, BlitterCS This field when set indicates the corresponding context has executed MI_WAIT_FOR_EVENT with "Display Pipe B Vertical Blank Wait Enable" set. This is an internal HW flag and should not be accessed by SW.
	12	**Context Wait for V-blank on Pipe-A** Source: RenderCS, BlitterCS This field when set indicates the corresponding context has executed MI_WAIT_FOR_EVENT with "Display Pipe A Vertical Blank Wait Enable" set. This is an internal HW flag and should not be accessed by SW.
	11:5	**Reserved** Format: MBZ
	4:0	**User Defined Condition Codes** Source: RenderCS The software may signal a Stream Semaphore by setting the Mask bit and Signal Bit together to match the bit field specified in a WAIT_FOR_EVENT (Semaphore).

FAULT_TLB_RD_DATA0 Register

FAULT_TLB_RD_DATA0 - FAULT_TLB_RD_DATA0 Register		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	04B10h	
DWord	**Bit**	**Description**
0	31:0	**FAULT_TLB_READ_DATA0 Register** Default Value: 00000000h Access: RO Fault cycle Virtual address [43:12]

FAULT_TLB_RD_DATA1 Register

FAULT_TLB_RD_DATA1 - FAULT_TLB_RD_DATA1 Register		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	04B14h	

DWord	Bit	Description
0	31:9	**Reserved** Default Value: 000000h Access: RO
	8:7	**TLB Entry Page Size** Default Value: 00b Access: RO 2'b00 - 4k, 2'b01 - 64k, 2'b10 - 2M, 2'b11 - 1G
	6	**TLB Entry Present** Default Value: 0h Access: RO 1'b1 - Present, 1'b0 - Not Present
	5	**TLB Entry Valid** Default Value: 0h Access: RO 1'b1 - Valid, 1'b0 - Not Valid
	4	**Cycle GTT Sel** Default Value: 0h Access: RO Cycle GTT SEL (1-GGTT Cycle, 0-PPGTT Cycle)
	3:0	**Address** Default Value: 0000b Access: RO Bit[3:0] Fault cycle Virtual address [47:44]

Fault Mode Control

FLTMODECTL - Fault Mode Control		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	0CEACh	
DWord	**Bit**	**Description**
0	31:1	**Reserved** Default Value: 00000000000000000000000000000000b Access: RO
	0	**Fault Halt Enable Bit** Default Value: 0b Access: R/W When set, it would enable the Fault and Halt behavior for streamable clients. Page walker will no longer use Fault and Stream mode for any client, instead it will downgrade the fault treatment to fault and halt. This behavior is applicable to HDC/Sampler/I$ given they are the only page fault streamable interfaces. This bit is only applicable under advanced context when PFM is selected for Fault and Stream.

Fault Mode Control

FAULT_MODE_CONTROL - Fault Mode Control		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	0404Ch	
DWord	**Bit**	**Description**
0	31:1	**Reserved** Format: MBZ
	0	**Fault and Halt Enable** Format: Enable When set, it would enable the Fault and Halt behavior for streamable clients. Page walker will no longer use Fault and Stream mode for any client, instead it will downgrade the fault treatment to Fault and Halt. This behavior is applicable to HDC/Sampler/I$ given they are the only page fault streamable interfaces. *This bit is only applicable under advanced context when PFM is selected for Fault and Stream.*

FBC_CFB_BASE

FBC_CFB_BASE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	43200h-43203h
Name:	FBC Compressed Buffer Address
ShortName:	FBC_CFB_BASE
Power:	PG1
Reset:	soft

Restriction
The contents of this register must not be changed while compression is enabled.

DWord	Bit	Description
0	31:28	**Reserved** Format: MBZ
	27:12	**CFB Offset Address** This register specifies bits 27:12 of the offset of the Compressed Frame Buffer from the base of stolen memory. A programmed value of 0x0001 in this field corresponds to an offset of 0x1000 (4K) bytes. **Restriction** The buffer must be 4K byte aligned. The offset must be greater than 4K bytes, avoiding the first 4KB of stolen memory.
	11:0	**Reserved** Format: MBZ

FBC_CTL

FBC_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	43208h-4320Bh
Name:	FBC Control
ShortName:	FBC_CTL
Power:	PG1
Reset:	soft

Description
FBC is tied to Plane 1 A.

Programming Notes
Frame Buffer Compression is supported with surfaces of up to 8192 pixels x 4096 lines and plane sizes up to 5120 pixels x 4096 lines.
The FBC compressed vertical limit is 2560 lines, after which the remaining lines will be displayed correctly, but will not be compressed.

Restriction
PLANE_SURF must be 512KB aligned when FBC is enabled with asynchronous flips on linear memory surfaces.
The contents of this register must not be changed, except the enable bit, while compression is enabled. Frame Buffer Compression is only supported with 16bpp and 32bpp 8:8:8 RGB plane source pixel formats. It is not supported with any other format. The 16bpp format requires the compression ratio to be set to 2:1 or 4:1.
Frame Buffer Compression is only supported while the plane it is tied to has a source size of at least 200 pixels x 32 lines.
Frame Buffer Compression is not supported with interlaced fetch. With plane 90/270 rotation, all frame buffer modifications will result in full frame invalidation and recompression. FBC should not be enabled with RGB 16bpp plane formats when plane 90/270 rotation is enabled.

DWord	Bit	Description
0	31	**Enable FBC** This bit is used to globally enable FBC function at the next Vertical Blank start. FBC should not be enabled when the pipe is disabled.

Value	Name

	0b	Disable
	1b	Enable

30:29 Reserved

Format:	MBZ

28 CPU Fence Enable

Description
This field is ignored. Host aperture tracking is enabled only through DPFC_CONTROL_SA.

Value	Name	Description
0b	No CPU Disp Buf	Display Buffer is not in a CPU fence. No modifications are allowed from CPU to the Display Buffer.
1b	CPU Disp Buf	Display Buffer exists in a CPU fence.

27:25 Reserved

Format:	MBZ

24:19 Reserved

Format:	MBZ

18 Reserved

17 Reserved

16 Reserved

15 Reserved

14:11 Reserved

Format:	MBZ

10 Reserved

9:8 Reserved

7:6 Compression Limit

This register sets a minimum limit on compression. This determines the maximum size of the compressed frame buffer. Display lines that do not meet the compression limit will not be compressed, so the best compression will be achieved with a 1:1 ratio.

Compression Ratio 1, Pixel Format 16 bpp - Not Supported
Compression Ratio 1, Pixel Format 32 bpp - Supported (CFB=FB)
Compression Ratio 1/2, Pixel Format 16 bpp - Supported (CFB=FB)

Compression Ratio 1/2, Pixel Format 32 bpp - Supported (CFB=1/2 FB)
Compression Ratio 1/4, Pixel Format 16 bpp - Supported (CFB=1/2 FB)
Compression Ratio 1/4, Pixel Format 32 bpp - Supported (CFB=1/4 FB)

FB = Frame Buffer Size
CFB = Compressed Frame Buffer Size

Value	Name	Description
00b	1:1	Compressed buffer is the same size as the uncompressed buffer.
01b	2:1	Compressed buffer is one half the size of the uncompressed buffer.
10b	4:1	Compressed buffer is one quarter the size of the uncompressed buffer.
11b	Reserved	Reserved

5:4 **Write Back Watermark**

The compressed data write back engine waits for this number of entries to be ready before writing the data out to memory.

Value	Name	Description
00b	4	4 entries
01b	8	8 entries
10b	16	16 entries
11b	32	32 entries

3:0 **CPU Fence Number**

Value	Name
0000b	Fence 0

Restriction
This field must be programmed to 0000b.

FBC_RT_BASE_ADDR_REGISTER

FBC_RT_BASE_ADDR_REGISTER - FBC_RT_BASE_ADDR_REGISTER

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	32
Address:	07020h

This Register is saved and restored as part of Context.

DWord	Bit	Description
0	31:12	**FBC RT Base Address** Access: R/W Format: GraphicsAddress[31:12] 4KB aligned Base Address as mapped in the PPGTT or in the GGTT for the render target. This base address must be the one that is either front buffer or the back-buffer (a flip target). It must be programmed before any draw call binding that render target base address.
	11:2	**Reserved** Access: R/W Format: PBC
	1	**FBC Front Buffer Target** Access: R/W **Value 0h** **[Default]**: FBC is targeting the Back Buffer for compression. This buffer can be cached in the MLC/LLC, so a GFDT flush is required before FBC can begin compression. **Value 1h**: FBC is targeting the Font Buffer for compression. This buffer cannot be cached in the MLC/LLC. FBC compression can begin after any RC flush.
	0	**PPGTT Render Target Base Address Valid for FBC** Access: R/W **Value 0h**: Base address in this register [31:12] is not valid and therefore FBC will not get

			[Default]	any modifications from rendering.
		1h		Base address in this register [31:12] is valid and HW needs to compare the current render target base address with this base address to provide modifications to FBC.

FBC_RT_BASE_ADDR_REGISTER_UPPER

FBC_RT_BASE_ADDR_REGISTER_UPPER - FBC_RT_BASE_ADDR_REGISTER_UPPER

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	32
Address:	07024h

This Register is saved and restored as part of Context.

Programming Notes

"Render Tracking with Nuke" is the only FBC functional mode supported by render engine. SW must always program the FBC_RT_BASE_ADDR_REGISTER_* register in Render Engine to a reserved value (0xFFFF_FFFF) such that the programmed value doesn't match the render target surface address programmed. This would disable render engine from generating modify messages to FBC unit in display. Refer "Frame Buffer Compression" section for more details related to FBC functionality and programming.

DWord	Bit	Description
0	31:16	**Reserved** Access: R/W Format: PBC
	15:0	**FBC RT Base Address Upper DWORD** Access: R/W Format: GraphicsAddress[47:32] Must be set to modify corresponding data bit. Reads to this field returns zero. Upper 4KB aligned Base Address as mapped in the PPGTT or in the GGTT for the render target. This base address must be the one that is either front buffer or the back-buffer (a flip target). It can be only programmed once per context. **Programming Notes** It must be programmed before any draw call binding that render target base address.

FBC LLC Config Read Control Register

FBC_LLC_READ_CTRL - FBC LLC Config Read Control Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	09044h

FBC LLC Config Read Control Register

DWord	Bit	Description
0	31	**FBC LLC Config Read Control Register Lock** Access: R/W Lock 0 = Bits of FBC_CTRL Register are R/W. 1 = All bits of FBC_CTRL Register are RO (including this lock bit). Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 does not clear the lock). These bits are not reset on FLR.
	30	**FBC LLC Config Start Value** Default Value: 1b Access: R/W Lock PCU_CR_LLC_CONFIG Read Cycle Interval in microseconds. 1'b0 - Treat LLC as partially open on reset (boot or C6 exit) (Default). 1'b1 - Treat LLC as fully open on reset (boot or C6 exit). This must not be set unless coordinated with Uncore.
	29:16	**Reserved** Access: RO Reserved.
	15:0	**FBC LLC Config Read Interval** Default Value: 00FFh Access: R/W Lock PCU_CR_LLC_CONFIG Read Cycle Interval in microseconds. 0x0000: Do not read PCU_CR_LLC_CONFIG (use Start Value only). 0x0001-0xFFFF : Read PCU_CR_LLC_CONFIG at the specified interval, until LLC_FULLY_OPEN=1. Default: 0xFF (approx 170us).

FENCE_LSB

FENCE_LSB	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	100020h
Name:	FENCE4_LSB
ShortName:	FENCE4_LSB
Address:	100028h
Name:	FENCE5_LSB
ShortName:	FENCE5_LSB
Address:	100030h
Name:	FENCE6_LSB
ShortName:	FENCE6_LSB
Address:	100038h
Name:	FENCE7_LSB
ShortName:	FENCE7_LSB
Address:	100040h
Name:	FENCE8_LSB
ShortName:	FENCE8_LSB
Address:	100048h
Name:	FENCE9_LSB
ShortName:	FENCE9_LSB
Address:	100050h
Name:	FENCE10_LSB
ShortName:	FENCE10_LSB
Address:	100058h
Name:	FENCE11_LSB
ShortName:	FENCE11_LSB
Address:	100060h
Name:	FENCE12_LSB
ShortName:	FENCE12_LSB
Address:	100068h

FENCE_LSB	
Name:	FENCE13_LSB
ShortName:	FENCE13_LSB
Address:	100070h
Name:	FENCE14_LSB
ShortName:	FENCE14_LSB
Address:	100078h
Name:	FENCE15_LSB
ShortName:	FENCE15_LSB
Address:	100080h
Name:	FENCE16_LSB
ShortName:	FENCE16_LSB
Address:	100088h
Name:	FENCE17_LSB
ShortName:	FENCE17_LSB
Address:	100090h
Name:	FENCE18_LSB
ShortName:	FENCE18_LSB
Address:	100098h
Name:	FENCE19_LSB
ShortName:	FENCE19_LSB
Address:	1000A0h
Name:	FENCE20_LSB
ShortName:	FENCE20_LSB
Address:	1000A8h
Name:	FENCE21_LSB
ShortName:	FENCE21_LSB
Address:	1000B0h
Name:	FENCE22_LSB
ShortName:	FENCE22_LSB
Address:	1000B8h
Name:	FENCE23_LSB
ShortName:	FENCE23_LSB
Address:	1000C0h
Name:	FENCE24_LSB
ShortName:	FENCE24_LSB

FENCE_LSB

Address:	1000C8h
Name:	FENCE25_LSB
ShortName:	FENCE25_LSB

Address:	1000D0h
Name:	FENCE26_LSB
ShortName:	FENCE26_LSB

Address:	1000D8h
Name:	FENCE27_LSB
ShortName:	FENCE27_LSB

Address:	1000E0h
Name:	FENCE28_LSB
ShortName:	FENCE28_LSB

Address:	1000E8h
Name:	FENCE29_LSB
ShortName:	FENCE29_LSB

Address:	1000F0h
Name:	FENCE30_LSB
ShortName:	FENCE30_LSB

Address:	1000F8h
Name:	FENCE31_LSB
ShortName:	FENCE31_LSB

Fence Registers LSBs

DWord	Bit	Description
0	31:12	**FENCELO** Default Value: 000000h Access: R/W Bits 31:12 of the ending Graphics Address of the fence region. Fence regions must be aligned to a 4KB page. This address represents the last 4KB page of the fence region (Lower Bound is included in the fence region). Graphics Address is the offset within GMADR space.
	11:2	**RESERVED** Default Value: 000h Access: RO Reserved

FENCE_LSB

	1	**TILE** Default Value: 0b Access: R/W This field specifies the spatial ordering of QW within tiles. 0b - Consecutive SWords (32B) sequenced in the X direction 1b - Consecutive OWords (16B) sequenced in the Y direction
	0	**FENCEVAL** Default Value: 0b Access: R/W This field specifies whether or not this fence register defines a fence region. 0b - FENCE INVALID 1b - FENCE VALID

FENCE_MSB

FENCE_MSB	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	100024h
Name:	FENCE4_MSB
ShortName:	FENCE4_MSB
Address:	10002Ch
Name:	FENCE5_MSB
ShortName:	FENCE5_MSB
Address:	100034h
Name:	FENCE6_MSB
ShortName:	FENCE6_MSB
Address:	10003Ch
Name:	FENCE7_MSB
ShortName:	FENCE7_MSB
Address:	100044h
Name:	FENCE8_MSB
ShortName:	FENCE8_MSB
Address:	10004Ch
Name:	FENCE9_MSB
ShortName:	FENCE9_MSB
Address:	100054h
Name:	FENCE10_MSB
ShortName:	FENCE10_MSB
Address:	10005Ch
Name:	FENCE11_MSB
ShortName:	FENCE11_MSB
Address:	100064h
Name:	FENCE12_MSB
ShortName:	FENCE12_MSB
Address:	10006Ch

FENCE_MSB	
Name:	FENCE13_MSB
ShortName:	FENCE13_MSB
Address:	100074h
Name:	FENCE14_MSB
ShortName:	FENCE14_MSB
Address:	10007Ch
Name:	FENCE15_MSB
ShortName:	FENCE15_MSB
Address:	100084h
Name:	FENCE16_MSB
ShortName:	FENCE16_MSB
Address:	10008Ch
Name:	FENCE17_MSB
ShortName:	FENCE17_MSB
Address:	100094h
Name:	FENCE18_MSB
ShortName:	FENCE18_MSB
Address:	10009Ch
Name:	FENCE19_MSB
ShortName:	FENCE19_MSB
Address:	1000A4h
Name:	FENCE20_MSB
ShortName:	FENCE20_MSB
Address:	1000ACh
Name:	FENCE21_MSB
ShortName:	FENCE21_MSB
Address:	1000B4h
Name:	FENCE22_MSB
ShortName:	FENCE22_MSB
Address:	1000BCh
Name:	FENCE23_MSB
ShortName:	FENCE23_MSB
Address:	1000C4h
Name:	FENCE24_MSB
ShortName:	FENCE24_MSB

FENCE_MSB

Address:	1000CCh
Name:	FENCE25_MSB
ShortName:	FENCE25_MSB

Address:	1000D4h
Name:	FENCE26_MSB
ShortName:	FENCE26_MSB

Address:	1000DCh
Name:	FENCE27_MSB
ShortName:	FENCE27_MSB

Address:	1000E4h
Name:	FENCE28_MSB
ShortName:	FENCE28_MSB

Address:	1000ECh
Name:	FENCE29_MSB
ShortName:	FENCE29_MSB

Address:	1000F4h
Name:	FENCE30_MSB
ShortName:	FENCE30_MSB

Address:	1000FCh
Name:	FENCE31_MSB
ShortName:	FENCE31_MSB

Fence Registers MSBs

DWord	Bit	Description
0	31:12	**FENCEUP** Default Value: 00000000h Access: R/W Bits 31:12 of the ending Graphics Address of the fence region. Fence regions must be aligned to a 4KB page. This address represents the last 4KB page of the fence region (Upper Bound is included in the fence region). Graphics Address is the offset within GMADR space.
	11	**Reserved** Default Value: 0b Access: RO Reserved

FENCE_MSB

	10:0	**Pitch** Default Value: 000h Access: R/W This field specifies the width (pitch) of the fence region in multiple of tile widths. For Tile X this field must be programmed to a multiple of 512B (003 is the minimum value) and for Tile Y this field must be programmed to a multiple of 128B (000 is the minimum value). 000h = 128B 001h = 256B 002h = 384B 003h = 512B 004h = 640B 005h = 768B 006h = 896B 007h = 1024B ... 3FFh = 128KB 4FFh = 160KB 5FFh = 192KB 6FFh = 224KB 7FFh = 256KB

Fence Control Register

MFCR - Fence Control Register

Register Space: MMIO: 0/2/0

Source: BSpec

Size (in bits): 32

Address: 09070h

Fence Control Register

DWord	Bit	Description
0	31	**Fuse Override Lock** Access: R/W Lock SW Fuse Override Lock Bit
	30:28	**ECORSVD** Access: R/W ECO purposes Reserved
	27:26	**GT VBOX DISABLE FUSE OVERRIDE** Access: R/W Lock S/W GT Vbox Disable Fuse Override Bits
	25:22	**GT SUBSLICE DISABLE FUSE OVERRIDE** Access: R/W Lock SW GT SubSlice Disable Fuse Override Bits
	21:16	**GT SLICE ENABLE FUSE OVERRIDE** Default Value: 111111b Access: R/W Lock SW GT Slice Enable Fuse Override Bits
	15:5	**RSVD** Access: RO
	4	**Reserved**
	3	**Reserved**
	2	**Write/Read Port Block** Access: R/W 0 - Dont Block the R/W port when Query is started.

MFCR - Fence Control Register

		1 - Block the R/W port until the Memory Fence is completed. This is applicable for only Memory Fence.
	1	**LLC Query Enable** Access: R/W 0 - Query for 16 Ways. 1 - Query for 32 Ways. No Flexing.
	0	**Fence Controller GFDT Mode** Access: R/W Fence Controller GFDT Mode. 0 - Single bit GFDT mode. 1 - Two bit GFDT mode.

FF Performance

FF_PERF - FF Performance

Register Space:	MMIO: 0/2/0
Source:	RenderCS, PositionCS
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	06B1Ch
Name:	Render CS FF Performance
ShortName:	RCS_FF_PERF
Address:	17B1Ch
Name:	Position CS POSH Pipeline FF Performance
ShortName:	PCS_FF_PERF

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask[15:0] Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15:11	**Reserved** Access: R/W Format: PBC
	10:8	**Throttle counter value** Access: R/W Counter value defining how many clocks the interface needs to be slowed down. Value: 0h — Name: **[Default]** — Description: Masked by default.
	7:3	**Reserved** Access: R/W

FF_PERF - FF Performance

	Format:	PBC

2 Enable throttling for SF-WM interface

Access:	R/W

Value	Name	Description
0h	Disable	No throttling
1h	Enable	Enable throttling in all SF-WM interfaces

Programming Notes
This field must not be programmed for SVGR unit.

1 Enable throttling for SF-SBE interface

Access:	R/W

Value	Name	Description
0h	Disable	No throttling
1h	Enable	Enable throttling in all SF-SBE interfaces

Programming Notes
This field must not be programmed for SVGR unit.

0 Enable throttling for CL-SF interface

Access:	R/W

Value	Name	Description
0h	Disable	No throttling
1h	Enable	Enable throttling in all CL-SF interfaces

Restriction
This bit must not be set. SW may choose to use SF-SBE throttle interface(bit 1) to achieve the same effect.

FIX BONUS1 Reg

FIXSPCBONUS1 - FIX BONUS1 Reg		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	24314h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:8	**Reserved** Access: RO Reserved
	7	**BONUS1 BIT 7** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS1 BIT 6** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS1 BIT 5** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS1 BIT 4** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	3	**BONUS1 BIT 3** Access: R/W

FIXSPCBONUS1 - FIX BONUS1 Reg

		SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS1 BIT 2** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS1 BIT 1** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS1 BIT 0** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

FIX BONUS2 Reg

FIXSPCBONUS2 - FIX BONUS2 Reg		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	24318h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:8	**Reserved** Access: RO Reserved
	7	**BONUS2 BIT 7** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS2 BIT 6** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS2 BIT 5** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS2 BIT 4** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	3	**BONUS2 BIT 3** Access: R/W

FIXSPCBONUS2 - FIX BONUS2 Reg

		SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS2 BIT 2** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS2 BIT 1** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS2 BIT 0** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

FIX PGFET control register with lock

FIXSPCPFETCTL - FIX PGFET control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	24308h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock 0 = Bits of Slice 0 PGFETCTL register are R/W 1 = All bits of Slice 0 PGFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:24	**Reserved** Access: RO Reserved
	23	**Power Well Status** Access: RO 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	22	**Powergood timer error** Access: RO 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	21:19	**Delay from enabling secondary PFETs to power good.** Access: R/W Lock Delay from enabling secondary PFETs to power good 3'b000: 40ns

FIXSPCPFETCTL - FIX PGFET control register with lock

3'b001: 80ns
3'b010: 160ns
3'b011: 240ns
3'b100: 320ns
3'b101: 480ns
3'b110: 640ns
3'b111: 1280ns

Value	Name
101b	**[Default]**

18:16 **Strobe pulse period**

Default Value:	010b
Access:	R/W Lock

Time period b/w two adjacent strobes to the primary FETs
3'b000: 10ns (or 1 bclk)
3'b001: 20ns (or 2 bclk)
3'b010: 30ns (or 3 bclk)
3'b111: 80ns (or 8 bclk)

15:0 **PFET Ladder Step Sequence**

Default Value:	1111111111111111b
Access:	R/W Lock

PFET Ladder STEP sequence
The PFET ladder has 16 steps, each represented by its corresponding bit in pfetlddrstepseq[15:0]. If the bit location is set, it means we must step on that ladder stage before we go to the next stage.
The SPC controller will step through all the steps with asserted bits periodically with period equal to strbpulsprd[2:0]
Programming Rule: pfetldrstepseq[15] and pfetldrstepseq[0] must be '1; A '0 setting for these bits is illegal.
15'FFFFh: Ladder step (ladder_sel) goes 0, 1, 2, ?.15.
15'FFF1h: Ladder step goes 0, 4, 5, 6,?15; Steps 1, 2, 3 are skipped.
15'D555h: Ladder step goes 0, 2, 4, 6, 8, 10, 12, 14, 15; Steps 1, 3, 5, 7, 9, 11, 13 are skipped.
15'80001h: Ladder step goes 0, 15; Steps 1, 2, 3, 4, ?14 are skipped.

Fix Power Context Save request

FIXPGCTXREQ - Fix Power Context Save request		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	24304h	
DWord	**Bit**	**Description**
0	31:16	**Message Mask** Access: RO Message Mask bots for lower 16 bits
	15:10	**Reserved** Access: RO Reserved
	9	**Power context save request** Access: R/W Set Power Context Save Request 1'b0 : Power context save is not being requested 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

FIX Power Down FSM control register with lock

FIXSPCPOWERDNFSMCTL - FIX Power Down FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	24310h

DWord	Bit	Description
0	31	**power down control Lock** Access: R/W Lock 0 = Bits of Slice 0 POWERDNFSMCTL register are R/W 1 = All bits of Slice 0 POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:13	**Reserved** Access: RO Reserved
	12	**Leave firewall disabled** Access: R/W Lock When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e dont firewall the gated domain, but complete logical flow
	11	**Leave reset de-asserted** Access: R/W Lock When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e dont assert reset, but complete logical flow
	10	**Leave CLKs ON** Access: R/W Lock

FIXSPCPOWERDNFSMCTL - FIX Power Down FSM control register with lock

		When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e dont clock gate, but complete logical flow
	9	**Leave FET On** Access: R/W Lock When This bit is set SPC will not turn off the PFET eventhough it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e dont power off pfet, but complete logical flow
	8:6	**Power Down state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Gate Clocks
	5:3	**Power Down state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default :Firewall ON
	2:0	**Power Down state 1** Default Value: 000b Access: R/W Lock This will be the 1st state before power is turned OFF in the well Encodings: 000 = Assert Reset

FIXSPCPOWERDNFSMCTL - FIX Power Down FSM control register with lock		
		001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Assert Reset

Fix Power Gate Control Request

FIXPGCTLREQ - Fix Power Gate Control Request		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	24300h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:16	**Message Mask** Access: RO Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:2	**Reserved** Access: RO Reserved
	1	**CLK RST FWE Request** Access: R/W SLICE 0 CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**Power Gate Request** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

FIX Power on FSM control register with lock

FIXSPCPOWERUPFSMCTL - FIX Power on FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	2430Ch

DWord	Bit	Description
0	31	**power up control Lock** Access: R/W Lock 0 = Bits of Slice 0 POWERUPFSMCTL register are R/W 1 = All bits of Slice 0 POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:9	**Reserved** Access: RO Reserved
	8:6	**Power UP state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - De-assert resets 3'b000: 10ns (or 1 bclk)
	5:3	**Power UP state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF

		010 = De-assert resets 1xx = Rsvd for future Default - Firewall OFF
	2:0	**Power UP state 1** Default Value: 000b Access: R/W Lock This will be the 1st state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Clock Ungate

Flexible EU Event Control 0

EU_PERF_CNT_CTL0 - Flexible EU Event Control 0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0E458h

This register configures flexible EU event 0/1. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.

DWord	Bit	Description
0	31:24	**Reserved** Default Value: 0xf Default
	23:20	**Fine Event Filter Select EU event 1** This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 1. Note that the fine event filter is logically applied after the coarse event filter. Value: 0xf — Name: Default **[Default]** Value: [0x0-0xA] — Name:
	19:16	**Coarse Event Filter Select EU event 1** This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 1. Note that the coarse event filter is logically applied before the fine event filter. Value: 0xf — Name: Default **[Default]** Value: [0x0-0x8] — Name:
	15:12	**Increment Event for EU event 1** This field controls which increment event provides the basis for flexible EU event 1. Value: 0xf — Name: Default **[Default]** Value: [0x0-0x8] — Name:

EU_PERF_CNT_CTL0 - Flexible EU Event Control 0

	11:8	**Fine Event Filter Select EU event 0** This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 0. Note that the fine event filter is logically applied after the coarse event filter. **Value** / **Name** 0xf — Default **[Default]** [0x0-0xA]
	7:4	**Coarse Event Filter Select EU event 0** This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 0. Note that the coarse event filter is logically applied before the fine event filter. **Value** / **Name** 0xf — Default **[Default]** [0x0-0x8]
	3:0	**Increment Event for EU event 0** This field controls which increment event provides the basis for flexible EU event 0. **Value** / **Name** 0xf — Default **[Default]** [0x0-0x8]

Flexible EU Event Control 1

EU_PERF_CNT_CTL1 - Flexible EU Event Control 1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0E558h

This register configures flexible EU event 2/3. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.

DWord	Bit	Description
0	31:24	**Reserved** Default Value: 0xf Default
	23:20	**Fine Event Filter Select EU event 3** This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 3. Note that the fine event filter is logically applied after the coarse event filter. Value: 0xf — Name: Default **[Default]** Value: [0x0-0xA] — Name:
	19:16	**Coarse Event Filter Select EU event 3** This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 3. Note that the coarse event filter is logically applied before the fine event filter. Value: 0xf — Name: Default **[Default]** Value: [0x0-0x8] — Name:
	15:12	**Increment Event for EU event 3** This field controls which increment event provides the basis for flexible EU event 3. Value: 0xf — Name: Default **[Default]** Value: [0x0-0x8] — Name:

EU_PERF_CNT_CTL1 - Flexible EU Event Control 1

	11:8	**Fine Event Filter Select EU event 2** This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 2. Note that the fine event filter is logically applied after the coarse event filter. **Value** / **Name** 0xf — Default **[Default]** [0x0-0xA]
	7:4	**Coarse Event Filter Select EU event 2** This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 2. Note that the coarse event filter is logically applied before the fine event filter. **Value** / **Name** 0xf — Default **[Default]** [0x0-0x8]
	3:0	**Increment Event for EU event 2** This field controls which increment event provides the basis for flexible EU event 2. **Value** / **Name** 0xf — Default **[Default]** [0x0-0x8]

Flexible EU Event Control 2

EU_PERF_CNT_CTL2 - Flexible EU Event Control 2

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0E658h

This register configures flexible EU event 4/5. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.

DWord	Bit	Description
0	31:24	**Reserved** Default Value: 0xf Default
	23:20	**Fine Event Filter Select EU event 1** This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 5. Note that the fine event filter is logically applied after the coarse event filter. Value: 0xf — Name: Default **[Default]** Value: [0x0-0xA] — Name:
	19:16	**Coarse Event Filter Select EU event 1** This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 5. Note that the coarse event filter is logically applied before the fine event filter. Value: 0xf — Name: Default **[Default]** Value: [0x0-0x8] — Name:
	15:12	**Increment Event for EU event 1** This field controls which increment event provides the basis for flexible EU event 5. Value: 0xf — Name: Default **[Default]** Value: [0x0-0x8] — Name:

EU_PERF_CNT_CTL2 - Flexible EU Event Control 2

	11:8	**Fine Event Filter Select EU event 0** This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 4. Note that the fine event filter is logically applied after the coarse event filter. **Value** / **Name** 0xf — Default **[Default]** [0x0-0xA]
	7:4	**Coarse Event Filter Select EU event 0** This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 4. Note that the coarse event filter is logically applied before the fine event filter. **Value** / **Name** 0xf — Default **[Default]** [0x0-0x8]
	3:0	**Increment Event for EU event 0** This field controls which increment event provides the basis for flexible EU event 4. **Value** / **Name** 0xf — Default **[Default]** [0x0-0x8]

Flexible EU Event Control 3

EU_PERF_CNT_CTL3 - Flexible EU Event Control 3

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0E758h

This register configures flexible EU event 6/7. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.

DWord	Bit	Description
0	31:24	**Reserved** Default Value: 0xf Default
	23:20	**Fine Event Filter Select EU event 1** This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 7. Note that the fine event filter is logically applied after the coarse event filter. Value: 0xf — Name: Default **[Default]** Value: [0x0-0xA]
	19:16	**Coarse Event Filter Select EU event 1** This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 7. Note that the coarse event filter is logically applied before the fine event filter. Value: 0xf — Name: Default **[Default]** Value: [0x0-0x8]
	15:12	**Increment Event for EU event 1** This field controls which increment event provides the basis for flexible EU event 7. Value: 0xf — Name: Default **[Default]** Value: [0x0-0x8]

EU_PERF_CNT_CTL3 - Flexible EU Event Control 3

	11:8	**Fine Event Filter Select EU event 0** This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 6. Note that the fine event filter is logically applied after the coarse event filter. **Value** / **Name** 0xf — Default **[Default]** [0x0-0xA]
	7:4	**Coarse Event Filter Select EU event 0** This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 6. Note that the coarse event filter is logically applied before the fine event filter. **Value** / **Name** 0xf — Default **[Default]** [0x0-0x8]
	3:0	**Increment Event for EU event 0** This field controls which increment event provides the basis for flexible EU event 6. **Value** / **Name** 0xf — Default **[Default]** [0x0-0x8]

Flexible EU Event Control 4

EU_PERF_CNT_CTL4 - Flexible EU Event Control 4

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0E45Ch

This register configures flexible EU event 8/9. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.

DWord	Bit	Description
0	31:24	**Reserved** Default Value: 0xf Default
	23:20	**Fine Event Filter Select EU event 1** This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 9. Note that the fine event filter is logically applied after the coarse event filter. Value: 0xf — Name: Default **[Default]** Value: [0x0-0xA] — Name:
	19:16	**Coarse Event Filter Select EU event 1** This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 9. Note that the coarse event filter is logically applied before the fine event filter. Value: 0xf — Name: Default **[Default]** Value: [0x0-0x8] — Name:
	15:12	**Increment Event for EU event 1** This field controls which increment event provides the basis for flexible EU event 9. Value: 0xf — Name: Default **[Default]** Value: [0x0-0x8] — Name:

EU_PERF_CNT_CTL4 - Flexible EU Event Control 4

	11:8	**Fine Event Filter Select EU event 0** This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 8. Note that the fine event filter is logically applied after the coarse event filter. **Value** / **Name** 0xf — Default **[Default]** [0x0-0xA]
	7:4	**Coarse Event Filter Select EU event 0** This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 8. Note that the coarse event filter is logically applied before the fine event filter. **Value** / **Name** 0xf — Default **[Default]** [0x0-0x8]
	3:0	**Increment Event for EU event 0** This field controls which increment event provides the basis for flexible EU event 8. **Value** / **Name** 0xf — Default **[Default]** [0x0-0x8]

Flexible EU Event Control 5

EU_PERF_CNT_CTL5 - Flexible EU Event Control 5

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0E55Ch

This register configures flexible EU event 10/11. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.

DWord	Bit	Description
0	31:24	**Reserved** Default Value: 0xf Default
	23:20	**Fine Event Filter Select EU event 1** This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 11. Note that the fine event filter is logically applied after the coarse event filter. Value: 0xf — Name: Default **[Default]** Value: [0x0-0xA]
	19:16	**Coarse Event Filter Select EU event 1** This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 11. Note that the coarse event filter is logically applied before the fine event filter. Value: 0xf — Name: Default **[Default]** Value: [0x0-0x8]
	15:12	**Increment Event for EU event 1** This field controls which increment event provides the basis for flexible EU event 11. Value: 0xf — Name: Default **[Default]** Value: [0x0-0x8]

EU_PERF_CNT_CTL5 - Flexible EU Event Control 5

	11:8	**Fine Event Filter Select EU event 0** This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 10. Note that the fine event filter is logically applied after the coarse event filter. **Value** / **Name** 0xf — Default **[Default]** [0x0-0xA]
	7:4	**Coarse Event Filter Select EU event 0** This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 10. Note that the coarse event filter is logically applied before the fine event filter. **Value** / **Name** 0xf — Default **[Default]** [0x0-0x8]
	3:0	**Increment Event for EU event 0** This field controls which increment event provides the basis for flexible EU event 10. **Value** / **Name** 0xf — Default **[Default]** [0x0-0x8]

Flexible EU Event Control 6

EU_PERF_CNT_CTL6 - Flexible EU Event Control 6

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0E65Ch

This register configures flexible EU event 12/13. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.

DWord	Bit	Description
0	31:24	**Reserved** Default Value: 0xf Default
	23:20	**Fine Event Filter Select EU event 1** This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 13. Note that the fine event filter is logically applied after the coarse event filter. Value: 0xf — Name: Default **[Default]** Value: [0x0-0xA]
	19:16	**Coarse Event Filter Select EU event 1** This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 13. Note that the coarse event filter is logically applied before the fine event filter. Value: 0xf — Name: Default **[Default]** Value: [0x0-0x8]
	15:12	**Increment Event for EU event 1** This field controls which increment event provides the basis for flexible EU event 13. Value: 0xf — Name: Default **[Default]** Value: [0x0-0x8]

EU_PERF_CNT_CTL6 - Flexible EU Event Control 6

	11:8	**Fine Event Filter Select EU event 0** This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 12. Note that the fine event filter is logically applied after the coarse event filter. **Value** / **Name** 0xf — Default **[Default]** [0x0-0xA]
	7:4	**Coarse Event Filter Select EU event 0** This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 12. Note that the coarse event filter is logically applied before the fine event filter. **Value** / **Name** 0xf — Default **[Default]** [0x0-0x8]
	3:0	**Increment Event for EU event 0** This field controls which increment event provides the basis for flexible EU event 12. **Value** / **Name** 0xf — Default **[Default]** [0x0-0x8]

FORCE_TO_NONPRIV

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	024D0h-024D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_RCSUNIT
Address:	024D4h-024D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_RCSUNIT
Address:	024D8h-024DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_RCSUNIT
Address:	024DCh-024DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_RCSUNIT
Address:	024E0h-024E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_RCSUNIT
Address:	024E4h-024E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_RCSUNIT
Address:	024E8h-024EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_RCSUNIT
Address:	024ECh-024EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_RCSUNIT
Address:	024F0h-024F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_RCSUNIT

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Address:	024F4h-024F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_RCSUNIT
Address:	024F8h-024FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_RCSUNIT
Address:	024FCh-024FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_RCSUNIT
Address:	184D0h-184D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_POCSUNIT
Address:	184D4h-184D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_POCSUNIT
Address:	184D8h-184DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_POCSUNIT
Address:	184DCh-184DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_POCSUNIT
Address:	184E0h-184E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_POCSUNIT
Address:	184E4h-184E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_POCSUNIT
Address:	184E8h-184EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_POCSUNIT
Address:	184ECh-184EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_POCSUNIT
Address:	184F0h-184F3h
Name:	FORCE_TO_NONPRIV

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
ShortName:	FORCE_TO_NONPRIV_8_POCSUNIT
Address:	184F4h-184F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_POCSUNIT
Address:	184F8h-184FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_POCSUNIT
Address:	184FCh-184FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_POCSUNIT
Address:	224D0h-224D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_BCSUNIT
Address:	224D4h-224D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_BCSUNIT
Address:	224D8h-224DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_BCSUNIT
Address:	224DCh-224DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_BCSUNIT
Address:	224E0h-224E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_BCSUNIT
Address:	224E4h-224E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_BCSUNIT
Address:	224E8h-224EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_BCSUNIT
Address:	224ECh-224EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_BCSUNIT

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Address:	224F0h-224F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_BCSUNIT
Address:	224F4h-224F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_BCSUNIT
Address:	224F8h-224FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_BCSUNIT
Address:	224FCh-224FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_BCSUNIT
Address:	1C04D0h-1C04D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_VCSUNIT0
Address:	1C04D4h-1C04D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VCSUNIT0
Address:	1C04D8h-1C04DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_VCSUNIT0
Address:	1C04DCh-1C04DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_VCSUNIT0
Address:	1C04E0h-1C04E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_VCSUNIT0
Address:	1C04E4h-1C04E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_VCSUNIT0
Address:	1C04E8h-1C04EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_VCSUNIT0
Address:	1C04ECh-1C04EFh
Name:	FORCE_TO_NONPRIV

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
ShortName:	FORCE_TO_NONPRIV_7_VCSUNIT0
Address:	1C04F0h-1C04F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_VCSUNIT0
Address:	1C04F4h-1C04F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VCSUNIT0
Address:	1C04F8h-1C04FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_VCSUNIT0
Address:	1C04FCh-1C04FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VCSUNIT0
Address:	1C44D0h-1C44D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_VCSUNIT1
Address:	1C44D4h-1C44D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VCSUNIT1
Address:	1C44D8h-1C44DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_VCSUNIT1
Address:	1C44DCh-1C44DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_VCSUNIT1
Address:	1C44E0h-1C44E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_VCSUNIT1
Address:	1C44E4h-1C44E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_VCSUNIT1
Address:	1C44E8h-1C44EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_VCSUNIT1

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Address:	1C44ECh-1C44EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_VCSUNIT1
Address:	1C44F0h-1C44F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_VCSUNIT1
Address:	1C44F4h-1C44F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VCSUNIT1
Address:	1C44F8h-1C44FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_VCSUNIT1
Address:	1C44FCh-1C44FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VCSUNIT1
Address:	1C84D0h-1C84D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_VECSUNIT0
Address:	1C84D4h-1C84D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VECSUNIT0
Address:	1C84D8h-1C84DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_VECSUNIT0
Address:	1C84DCh-1C84DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_VECSUNIT0
Address:	1C84E0h-1C84E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_VECSUNIT0
Address:	1C84E4h-1C84E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_VECSUNIT0
Address:	1C84E8h-1C84EBh
Name:	FORCE_TO_NONPRIV

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
ShortName:	FORCE_TO_NONPRIV_6_VECSUNIT0
Address:	1C84ECh-1C84EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_VECSUNIT0
Address:	1C84F0h-1C84F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_VECSUNIT0
Address:	1C84F4h-1C84F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VECSUNIT0
Address:	1C84F8h-1C84FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_VECSUNIT0
Address:	1C84FCh-1C84FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VECSUNIT0
Address:	1D04D0h-1D04D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_VCSUNIT2
Address:	1D04D4h-1D04D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VCSUNIT2
Address:	1D04D8h-1D04DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_VCSUNIT2
Address:	1D04DCh-1D04DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_VCSUNIT2
Address:	1D04E0h-1D04E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_VCSUNIT2
Address:	1D04E4h-1D04E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_VCSUNIT2

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Address:	1D04E8h-1D04EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_VCSUNIT2
Address:	1D04ECh-1D04EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_VCSUNIT2
Address:	1D04F0h-1D04F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_VCSUNIT2
Address:	1D04F4h-1D04F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VCSUNIT2
Address:	1D04F8h-1D04FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_VCSUNIT2
Address:	1D04FCh-1D04FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VCSUNIT2
Address:	1D44D0h-1D44D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_VCSUNIT3
Address:	1D44D4h-1D44D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VCSUNIT3
Address:	1D44D8h-1D44DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_VCSUNIT3
Address:	1D44DCh-1D44DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_VCSUNIT3
Address:	1D44E0h-1D44E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_VCSUNIT3
Address:	1D44E4h-1D44E7h
Name:	FORCE_TO_NONPRIV

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
ShortName:	FORCE_TO_NONPRIV_5_VCSUNIT3
Address:	1D44E8h-1D44EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_VCSUNIT3
Address:	1D44ECh-1D44EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_VCSUNIT3
Address:	1D44F0h-1D44F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_VCSUNIT3
Address:	1D44F4h-1D44F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VCSUNIT3
Address:	1D44F8h-1D44FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_VCSUNIT3
Address:	1D44FCh-1D44FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VCSUNIT3
Address:	1D84D0h-1D84D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_VECSUNIT1
Address:	1D84D4h-1D84D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VECSUNIT1
Address:	1D84D8h-1D84DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_VECSUNIT1
Address:	1D84DCh-1D84DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_VECSUNIT1
Address:	1D84E0h-1D84E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_VECSUNIT1

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Address:	1D84E4h-1D84E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_VECSUNIT1
Address:	1D84E8h-1D84EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_VECSUNIT1
Address:	1D84ECh-1D84EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_VECSUNIT1
Address:	1D84F0h-1D84F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_VECSUNIT1
Address:	1D84F4h-1D84F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VECSUNIT1
Address:	1D84F8h-1D84FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_VECSUNIT1
Address:	1D84FCh-1D84FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VECSUNIT1
Address:	1E04D0h-1E04D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_VCSUNIT4
Address:	1E04D4h-1E04D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VCSUNIT4
Address:	1E04D8h-1E04DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_VCSUNIT4
Address:	1E04DCh-1E04DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_VCSUNIT4
Address:	1E04E0h-1E04E3h
Name:	FORCE_TO_NONPRIV

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
ShortName:	FORCE_TO_NONPRIV_4_VCSUNIT4
Address:	1E04E4h-1E04E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_VCSUNIT4
Address:	1E04E8h-1E04EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_VCSUNIT4
Address:	1E04ECh-1E04EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_VCSUNIT4
Address:	1E04F0h-1E04F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_VCSUNIT4
Address:	1E04F4h-1E04F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VCSUNIT4
Address:	1E04F8h-1E04FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_VCSUNIT4
Address:	1E04FCh-1E04FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VCSUNIT4
Address:	1E44D0h-1E44D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_VCSUNIT5
Address:	1E44D4h-1E44D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VCSUNIT5
Address:	1E44D8h-1E44DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_VCSUNIT5
Address:	1E44DCh-1E44DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_VCSUNIT5

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Address:	1E44E0h-1E44E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_VCSUNIT5
Address:	1E44E4h-1E44E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_VCSUNIT5
Address:	1E44E8h-1E44EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_VCSUNIT5
Address:	1E44ECh-1E44EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_VCSUNIT5
Address:	1E44F0h-1E44F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_VCSUNIT5
Address:	1E44F4h-1E44F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VCSUNIT5
Address:	1E44F8h-1E44FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_VCSUNIT5
Address:	1E44FCh-1E44FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VCSUNIT5
Address:	1E84D0h-1E84D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_VECSUNIT2
Address:	1E84D4h-1E84D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VECSUNIT2
Address:	1E84D8h-1E84DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_VECSUNIT2
Address:	1E84DCh-1E84DFh
Name:	FORCE_TO_NONPRIV

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
ShortName:	FORCE_TO_NONPRIV_3_VECSUNIT2
Address:	1E84E0h-1E84E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_VECSUNIT2
Address:	1E84E4h-1E84E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_VECSUNIT2
Address:	1E84E8h-1E84EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_VECSUNIT2
Address:	1E84ECh-1E84EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_VECSUNIT2
Address:	1E84F0h-1E84F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_VECSUNIT2
Address:	1E84F4h-1E84F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VECSUNIT2
Address:	1E84F8h-1E84FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_VECSUNIT2
Address:	1E84FCh-1E84FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VECSUNIT2
Address:	1F04D0h-1F04D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_VCSUNIT6
Address:	1F04D4h-1F04D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VCSUNIT6
Address:	1F04D8h-1F04DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_VCSUNIT6

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Address:	1F04DCh-1F04DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_VCSUNIT6
Address:	1F04E0h-1F04E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_VCSUNIT6
Address:	1F04E4h-1F04E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_VCSUNIT6
Address:	1F04E8h-1F04EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_VCSUNIT6
Address:	1F04ECh-1F04EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_VCSUNIT6
Address:	1F04F0h-1F04F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_VCSUNIT6
Address:	1F04F4h-1F04F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VCSUNIT6
Address:	1F04F8h-1F04FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_VCSUNIT6
Address:	1F04FCh-1F04FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VCSUNIT6
Address:	1F44D0h-1F44D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_VCSUNIT7
Address:	1F44D4h-1F44D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VCSUNIT7
Address:	1F44D8h-1F44DBh
Name:	FORCE_TO_NONPRIV

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
ShortName:	FORCE_TO_NONPRIV_2_VCSUNIT7
Address:	1F44DCh-1F44DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_VCSUNIT7
Address:	1F44E0h-1F44E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_VCSUNIT7
Address:	1F44E4h-1F44E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_VCSUNIT7
Address:	1F44E8h-1F44EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_VCSUNIT7
Address:	1F44ECh-1F44EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_VCSUNIT7
Address:	1F44F0h-1F44F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_VCSUNIT7
Address:	1F44F4h-1F44F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VCSUNIT7
Address:	1F44F8h-1F44FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_VCSUNIT7
Address:	1F44FCh-1F44FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VCSUNIT7
Address:	1F84D0h-1F84D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_VECSUNIT3
Address:	1F84D4h-1F84D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VECSUNIT3

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Address:	1F84D8h-1F84DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_VECSUNIT3
Address:	1F84DCh-1F84DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_VECSUNIT3
Address:	1F84E0h-1F84E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_VECSUNIT3
Address:	1F84E4h-1F84E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_VECSUNIT3
Address:	1F84E8h-1F84EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_VECSUNIT3
Address:	1F84ECh-1F84EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_VECSUNIT3
Address:	1F84F0h-1F84F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_VECSUNIT3
Address:	1F84F4h-1F84F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VECSUNIT3
Address:	1F84F8h-1F84FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_VECSUNIT3
Address:	1F84FCh-1F84FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VECSUNIT3
These registers are privilege registers and are not allowed to be written from non-privilege batch buffer. These are global registers and power context save/restored.	
Workaround	
These register must be programmed as non-privileged to give PPGTT batch buffer access: 3DPRIM_XP0(0x2690), 3DPRIM_XP1(0x2694) and 3DPRIM_XP2(0x2698).	

DWord	Bit	Description
0	31	**Reserved** Format: MBZ
	30	**Reserved**
	29:28	**Reserved**
	27	**Reserved** Format: MBZ
	26	**Reserved** Format: MBZ
	25:2	**Non Privilege Register Address** Format: MmioAddress[25:2] This field contains the MMIO offset of a register. MMIO offset programmed in this field will be treated as a non-privilege register by render command streamer while processing register writes from a non-privilege batch buffer. This register provides programmability is to extend the non-privilege register table mentioned in MI_BATCH_BUFFER_START command in render command streamer. Value: 3800h — Name: **[Default]**
	1:0	**Reserved** Format: MBZ

FUSE_STATUS

FUSE_STATUS

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	42000h-42003h
Name:	Fuse Status
ShortName:	FUSE_STATUS
Power:	PG0
Reset:	global

This register is on the ungated clock and the chip reset, not the FLR.

DWord	Bit	Description
0	31	**Fuse Download Status** Access: RO This field indicates the status of fuse and strap download to the Display Engine. After fuse and strap download, fuses will be distributed within the Display Engine. 0b – Not Done 1b – Done
	30:28	**Reserved**
	27	**Fuse PG0 Distribution Status** Access: RO This field indicates the status of fuse distribution to power well #0. 0b – Not Done 1b – Done
	26	**Fuse PG1 Distribution Status** Access: RO This field indicates the status of fuse distribution to power well #1. 0b – Not Done 1b – Done
	25	**Fuse PG2 Distribution Status**

FUSE_STATUS

		Access: RO
		This field indicates the status of fuse distribution to power well #2.

Value	Name
0b	Not Done
1b	Done

	24	**Fuse PG3 Distribution Status**
		Access: RO
		This field indicates the status of fuse distribution to power well #3.

Value	Name
0b	Not Done
1b	Done

	23	**Fuse PG4 Distribution Status**
		Access: RO
		This field indicates the status of fuse distribution to power well #4.

Value	Name
0b	Not Done
1b	Done

	22:0	**Reserved**

GAM BDF Register

GAM_BDF - GAM BDF Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	04200h

This register holds the bus,device and function number

DWord	Bit	Description
0	31:24	**Bus Number** Default Value: 00h Access: R/W This field specifies the PCI bus number of the graphics device.
	23:19	**Device Number** Default Value: 00010b Access: R/W This field specifies the PCI device number of the graphics device
	18:16	**Function Number** Default Value: 000b Access: RO This field specifies the PCI function number of the graphics device. The function number has a meaning only when the graphics device is not virtualized.
	15:0	**Reserved** Default Value: 0000h Access: R/W Reserved for future use.

GAMMA_MODE

GAMMA_MODE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank
Address:	4A480h-4A483h
Name:	Pipe Gamma Mode
ShortName:	GAMMA_MODE_A
Power:	PG1
Reset:	soft
Address:	4AC80h-4AC83h
Name:	Pipe Gamma Mode
ShortName:	GAMMA_MODE_B
Power:	PG2
Reset:	soft
Address:	4B480h-4B483h
Name:	Pipe Gamma Mode
ShortName:	GAMMA_MODE_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31	**Pre CSC Gamma Enable** This bit enables the pipe pre color space conversion gamma. Restriction : This bit must not be set when any of the individual plane 'Pipe CSC Enable' bit is set in PLANE_COLOR_CTL register. Value: 1b — Name: Enable Value: 0b — Name: Disable
	30	**Post CSC Gamma Enable**

GAMMA_MODE

This bit enables the pipe post color space conversion gamma.

Restriction : This bit must not be set when any of the individual plane 'Pipe Gamma Enable' bit is set in PLANE_COLOR_CTL register.

Value	Name
1b	Enable
0b	Disable

29:16 **Reserved**

Format:	MBZ

15 **Reserved**

14:2 **Reserved**

Format:	MBZ

1:0 **Gamma Mode**

Description
This field selects which mode the pipe palette/gamma correction logic works in. Other gamma units, such as in the planes, are unaffected by these bits.
This field applies to post csc gamma. Pre csc gamma mode is fixed and not configurable.

Value	Name	Description
00b	8 bit	8-bit Legacy Palette Mode
01b	10 bit	10-bit Precision Palette Mode
10b	12 bit	12-bit Interpolated Gamma Mode
11b	12 bit Multi Segment	12-bit Multi-segmented Gamma Mode

Gated Clock Counter for DFR Testability

SAMPLER_DFR_GATED_COUNT - Gated Clock Counter for DFR Testability

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	0E14Ch

For testability of DFR feature

DWord	Bit	Description
0	31:0	**Counter Bits** Format: U32 Count of edge-skipped sampler clocks.

General Purpose Register

CS_GPR - General Purpose Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	1024
Address:	02600h-0267Fh
Name:	General Purpose Register
ShortName:	CS_GPR_RCSUNIT
Address:	18600h-1867Fh
Name:	General Purpose Register
ShortName:	CS_GPR_POCSUNIT
Address:	22600h-2267Fh
Name:	General Purpose Register
ShortName:	CS_GPR_BCSUNIT
Address:	1C0600h-1C067Fh
Name:	General Purpose Register
ShortName:	CS_GPR_VCSUNIT0
Address:	1C4600h-1C467Fh
Name:	General Purpose Register
ShortName:	CS_GPR_VCSUNIT1
Address:	1C8600h-1C867Fh
Name:	General Purpose Register
ShortName:	CS_GPR_VECSUNIT0
Address:	1D0600h-1D067Fh
Name:	General Purpose Register
ShortName:	CS_GPR_VCSUNIT2
Address:	1D4600h-1D467Fh
Name:	General Purpose Register
ShortName:	CS_GPR_VCSUNIT3
Address:	1D8600h-1D867Fh
Name:	General Purpose Register
ShortName:	CS_GPR_VECSUNIT1

CS_GPR - General Purpose Register

Address:	1E0600h-1E067Fh
Name:	General Purpose Register
ShortName:	CS_GPR_VCSUNIT4

Address:	1E4600h-1E467Fh
Name:	General Purpose Register
ShortName:	CS_GPR_VCSUNIT5

Address:	1E8600h-1E867Fh
Name:	General Purpose Register
ShortName:	CS_GPR_VECSUNIT2

Address:	1F0600h-1F067Fh
Name:	General Purpose Register
ShortName:	CS_GPR_VCSUNIT6

Address:	1F4600h-1F467Fh
Name:	General Purpose Register
ShortName:	CS_GPR_VCSUNIT7

Address:	1F8600h-1F867Fh
Name:	General Purpose Register
ShortName:	CS_GPR_VECSUNIT3

Description	Source
This is a General Purpose Register bank of sixteen 64bit registers, which will be used as temporary storage by MI_MATH command to do ALU operations.	

GPR Index	MMIO Offset	Source
R_0	0x2600	RenderCS
R_1	0x2608	
R_2	0x2610	
R_3	0x2618	
R_4	0x2620	
R_5	0x2628	
R_6	0x2630	
R_7	0x2638	
R_8	0x2640	
R_9	0x2648	
R_10	0x2650	
R_11	0x2658	
R_12	0x2660	

CS_GPR - General Purpose Register

R_13	0x2668
R_14	0x2670
R_15	0x2678

DWord	Bit	Description
0..1	63:32	**CS_GPR_DATA1** Source: CommandStreamer
	31:0	**CS_GPR_DATA0** Source: CommandStreamer
2..3	63:32	**CS_GPR_DATA3** Source: CommandStreamer
	31:0	**CS_GPR_DATA2** Source: CommandStreamer
4..5	63:32	**CS_GPR_DATA5** Source: CommandStreamer
	31:0	**CS_GPR_DATA4** Source: CommandStreamer
6..7	63:32	**CS_GPR_DATA7** Source: CommandStreamer
	31:0	**CS_GPR_DATA6** Source: CommandStreamer
8..9	63:32	**CS_GPR_DATA9** Source: CommandStreamer
	31:0	**CS_GPR_DATA8** Source: CommandStreamer
10..11	63:32	**CS_GPR_DATA11** Source: CommandStreamer
	31:0	**CS_GPR_DATA10** Source: CommandStreamer
12..13	63:32	**CS_GPR_DATA13** Source: CommandStreamer
	31:0	**CS_GPR_DATA12** Source: CommandStreamer
14..15	63:32	**CS_GPR_DATA15** Source: CommandStreamer

CS_GPR - General Purpose Register		
	31:0	**CS_GPR_DATA14** Source: CommandStreamer
16..17	63:32	**CS_GPR_DATA17** Source: CommandStreamer
	31:0	**CS_GPR_DATA16** Source: CommandStreamer
18..19	63:32	**CS_GPR_DATA19** Source: CommandStreamer
	31:0	**CS_GPR_DATA18** Source: CommandStreamer
20..21	63:32	**CS_GPR_DATA21** Source: CommandStreamer
	31:0	**CS_GPR_DATA20** Source: CommandStreamer
22..23	63:32	**CS_GPR_DATA23** Source: CommandStreamer
	31:0	**CS_GPR_DATA22** Source: CommandStreamer
24..25	63:32	**CS_GPR_DATA25** Source: CommandStreamer
	31:0	**CS_GPR_DATA24** Source: CommandStreamer
26..27	63:32	**CS_GPR_DATA27** Source: CommandStreamer
	31:0	**CS_GPR_DATA26** Source: CommandStreamer
28..29	63:32	**CS_GPR_DATA29** Source: CommandStreamer
	31:0	**CS_GPR_DATA28** Source: CommandStreamer
30..31	63:32	**CS_GPR_DATA31** Source: CommandStreamer
	31:0	**CS_GPR_DATA30** Source: CommandStreamer

GFX_FLSH_CNT

GFX_FLSH_CNT - GFX_FLSH_CNT		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	101008h	
Used to flush Gunit TLB		
DWord	**Bit**	**Description**
0	31:1	**RESERVED** Default Value: 00000000h Access: RO Reserved
	0	**GfxFlshCntl** Default Value: 0b Access: WO Access type of this register is WO. A write to this bit flushes the Gfx TLB in GUNIT. The data associated with the write is discarded and a read return all 0s.

GFX Fault Counter

GFX_FAULT_CNTR - GFX Fault Counter		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	04904h	

DWord	Bit	Description
0	31:0	**GFX Flt Counter** Default Value: 00000000h Access: RO This counter only applies to advance context when fault and stream mode is selected.

GFX Fixed Counter

GFX_FIXED_CNTR - GFX Fixed Counter		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	04908h	

DWord	Bit	Description
0	31:0	**GFX Fixed Count** Default Value: 00000000h Access: RO This counter only applies to advance context when fault and stream mode is selected.

Global System Interrupt Routine

EU_GLOBAL_SIP - Global System Interrupt Routine

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0E42Ch

DWord	Bit	Description
0	31:3	**Global SIP** Format: GraphicsAddress[31:3] Specifies the base address for System Interrupt Routine that over-rides the SIP set by the state (STATE_SIP).
	2:1	**Reserved** Format: PBC
	0	**Global SIP Enable** The bit specifies if the System Routine starts from the Global SIP provided by the DW OR the SIP provided by the state (STATE_SIP)

Value	Name
0	SIP used is from STATE_EIP
1	SIP used is from MMIO register

GO Messaging Register for KCRunit

MSG_GO_KCR - GO Messaging Register for KCRunit

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	080BCh
Name:	GO Messaging Register for KCRunit
ShortName:	MSG_GO_KCR

Register that handshakes with KCR for GO messaging for different reasons including Media/Render power down, Media/Render soft resets and GT C6 enter/exit
GA* Response to Allow Graphics Cycles to Read/Write from Memory.
1'b0: No gfx cycles allowed to memory (default).
1'b1: Allow gfx cycles to memory.
GPM currently only ever sends the same GO request for all agents; either all is go=0, or all is go=1.
Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].
To set bit0, for example, the data would be 0x0001_0001.
To clear bit0, for example, the data would be 0x0001_0000.
Note that mask bit is the data bit offset + 16.
Message registers are protected from non-GT writes via the Message Channel.
GA* Response to Allow Graphics Cycles to Read/Write from Memory.
1'b0: No gfx cycles allowed to memory (default).
1'b1: Allow gfx cycles to memory.
GPM currently only ever sends the same GO request for all agents; either all is go=0, or all is go=1.

DWord	Bit	Description
0	31:14	**Reserved** Access: RO
	13	**Preparation for C6 enter/BCS reset enter/exit** Access: R/W u Go Acknowledgement 1'b0: Go=0 Ack (default). 1'b1: Go=1 Ack.
	12	**Response to Render soft reset or C6 entry/exit** Access: R/W Go Acknowledgement for Render related flows 1'b0: Go=0 Ack (default).

MSG_GO_KCR - GO Messaging Register for KCRunit

		1'b1: Go=1 Ack.
	11	**Response to VEBOX3 soft reset or Media Slice 3 entry/exit** Access: R/W Go Acknowledgement for VEBOX3 related flows 1'b0: Go=0 Ack (default). 1'b1: Go=1 Ack.
	10	**Response to VEBOX2 soft reset or Media Slice 2 entry/exit** Access: R/W Go Acknowledgement for VEBOX2 related flows 1'b0: Go=0 Ack (default). 1'b1: Go=1 Ack.
	9	**Response to VEBOX1 soft reset or Media Slice 1 entry/exit** Access: R/W Go Acknowledgement for VEBOX1 related flows 1'b0: Go=0 Ack (default). 1'b1: Go=1 Ack.
	8	**Response to VEBOX0 soft reset or Media Slice 0 entry/exit** Access: R/W Go Acknowledgement for VEBOX0 related flows 1'b0: Go=0 Ack (default). 1'b1: Go=1 Ack.
	7	**Response to VDBOX7 soft reset or Media Slice 3 entry/exit** Access: R/W Go Acknowledgement for VDBOX7 related flows 1'b0: Go=0 Ack (default). 1'b1: Go=1 Ack.
	6	**Response to VDBOX6 soft reset or Media Slice 3 entry/exit** Access: R/W Go Acknowledgement for VDBOX6 related flows 1'b0: Go=0 Ack (default). 1'b1: Go=1 Ack.
	5	**Response to VDBOX5 soft reset or Media Slice 2 entry/exit** Access: R/W Go Acknowledgement for VDBOX5 related flows

MSG_GO_KCR - GO Messaging Register for KCRunit

		1'b0: Go=0 Ack (default). 1'b1: Go=1 Ack.
	4	**Response to VDBOX4 soft reset or Media Slice 2 entry/exit** Access: R/W Go Acknowledgement for VDBOX4 related flows 1'b0: Go=0 Ack (default). 1'b1: Go=1 Ack.
	3	**Response to VDBOX3 soft reset or Media Slice 1 entry/exit** Access: R/W Go Acknowledgement for VDBOX3 related flows 1'b0: Go=0 Ack (default). 1'b1: Go=1 Ack.
	2	**Response to VDBOX2 soft reset or Media Slice 1 entry/exit** Access: R/W Go Acknowledgement for VDBOX2 related flows 1'b0: Go=0 Ack (default). 1'b1: Go=1 Ack.
	1	**Response to VDBOX1 soft reset or Media Slice 0 entry/exit** Access: R/W Go Acknowledgement for VDBOX1 related flows 1'b0: Go=0 Ack (default). 1'b1: Go=1 Ack.
	0	**Response to VDBOX0 soft reset or Media Slice 0 entry/exit** Access: R/W Go Acknowledgement for VDBOX0 related flows 1'b0: Go=0 Ack (default). 1'b1: Go=1 Ack.

GPGPU Context Restore Request To TDL

GPGPU_CTX_RESTORE - GPGPU Context Restore Request To TDL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	WO
Size (in bits):	32
Address:	0E4ACh
Name:	GPGPU Context Restore Request To TDL Slice 0 SubSlice 0
ShortName:	GPGPU_CTX_RESTORE_S0_SS0
Address:	0E5ACh
Name:	GPGPU Context Restore Request To TDL Slice 0 SubSlice 1
ShortName:	GPGPU_CTX_RESTORE_S0_SS1
Address:	0E6ACh
Name:	GPGPU Context Restore Request To TDL Slice 0 SubSlice 2
ShortName:	GPGPU_CTX_RESTORE_S0_SS2
Address:	0E414h
Name:	GPGPU Context Restore Request To TDL Slice 1 SubSlice 0
ShortName:	GPGPU_CTX_RESTORE_S1_SS0
Address:	0E514h
Name:	GPGPU Context Restore Request To TDL Slice 1 SubSlice 1
ShortName:	GPGPU_CTX_RESTORE_S1_SS1
Address:	0E614h
Name:	GPGPU Context Restore Request To TDL Slice 1 SubSlice 2
ShortName:	GPGPU_CTX_RESTORE_S1_SS2
Address:	0E4CCh
Name:	GPGPU Context Restore Request To TDL Slice 2 SubSlice 0
ShortName:	GPGPU_CTX_RESTORE_S2_SS0

GPGPU_CTX_RESTORE - GPGPU Context Restore Request To TDL	
Address:	0E5CCh
Name:	GPGPU Context Restore Request To TDL Slice 2 SubSlice 1
ShortName:	GPGPU_CTX_RESTORE_S2_SS1
Address:	0E6CCh
Name:	GPGPU Context Restore Request To TDL Slice 2 SubSlice 2
ShortName:	GPGPU_CTX_RESTORE_S2_SS2
Address:	0E4DCh
Name:	GPGPU Context Restore Request To TDL Slice 3 SubSlice 0
ShortName:	GPGPU_CTX_RESTORE_S3_SS0
Address:	0E5DCh
Name:	GPGPU Context Restore Request To TDL Slice 3 SubSlice 1
ShortName:	GPGPU_CTX_RESTORE_S3_SS1
Address:	0E6DCh
Name:	GPGPU Context Restore Request To TDL Slice 3 SubSlice 2
ShortName:	GPGPU_CTX_RESTORE_S3_SS2
Address:	0E4ECh
Name:	GPGPU Context Restore Request To TDL Slice 4 SubSlice 0
ShortName:	GPGPU_CTX_RESTORE_S4_SS0
Address:	0E5ECh
Name:	GPGPU Context Restore Request To TDL Slice 4 SubSlice 1
ShortName:	GPGPU_CTX_RESTORE_S4_SS1
Address:	0E6ECh
Name:	GPGPU Context Restore Request To TDL Slice 4 SubSlice 2
ShortName:	GPGPU_CTX_RESTORE_S4_SS2
Address:	0E4FCh
Name:	GPGPU Context Restore Request To TDL Slice 5 SubSlice 0
ShortName:	GPGPU_CTX_RESTORE_S5_SS0

GPGPU_CTX_RESTORE - GPGPU Context Restore Request To TDL

Address:	0E5FCh
Name:	GPGPU Context Restore Request To TDL Slice 5 SubSlice 1
ShortName:	GPGPU_CTX_RESTORE_S5_SS1

Address:	0E6FCh
Name:	GPGPU Context Restore Request To TDL Slice 5 SubSlice 2
ShortName:	GPGPU_CTX_RESTORE_S5_SS2

DWord	Bit	Description
0	31:0	**Reserved** Format: MBZ

GPGPU Context Save Request To TDL

GPGPU_CTX_SAVE - GPGPU Context Save Request To TDL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	WO
Size (in bits):	32
Address:	0E4D8h

DWord	Bit	Description
0	31:0	**Reserved** Format: MBZ

GPGPU Dispatch Dimension X

GPGPU_DISPATCHDIMX - GPGPU Dispatch Dimension X	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02500h

DWord	Bit	Description
0	31:0	**Dispatch Dimension X** Format: U32 The number of thread groups to be dispatched in the X dimension (max x + 1). Value: 0, FFFFFFFFh; Name:

GPGPU Dispatch Dimension Y

GPGPU_DISPATCHDIMY - GPGPU Dispatch Dimension Y

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02504h

DWord	Bit	Description
0	31:0	**Dispatch Dimension Y** Format: U32 The number of thread groups to be dispatched in the Y dimension (max y + 1 Value: 0, FFFFFFFFh Name:

GPGPU Dispatch Dimension Z

GPGPU_DISPATCHDIMZ - GPGPU Dispatch Dimension Z

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02508h

DWord	Bit	Description
0	31:0	**Dispatch Dimension Z** Format: U32 The number of thread groups to be dispatched in the Zdimension (max Z + 1) Value: 0, FFFFFFFFh Name:

GP Thread Time

GP_THREAD_TIME - GP Thread Time	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	053C4h

Reading this register returns the cumulative GP context execution time. This register uses the same clock frequency as CTX_TIMESTAMP, but differs from CTX_TIMESTAMP because it excludes the execution time during preemption save or restore. This register gets context save/restored on a context switch.
The granularity of this toggle is at the rate of the bit 3 in the "Reported Timestamp Count" register(0x2358). The toggle will be 8 times slower that "Reported Timestamp Count". The granularity of the time stamp base unit for "Reported Timestamp Count" is defined in the “Timestamp Bases” subsection in Power Management chapter.

DWord	Bit	Description
0	31:0	**Timestamp Value** Access: RO Number of clock ticks that the context has run.

GPU_Ticks_Counter

GPU_TICKS - GPU_Ticks_Counter	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02910h

Reading this register returns the live value of the GPU ticks counter that is sampled and included in the performance counter report header. It increments every GFX clock and hence the number of increments per second changes with GFX frequency.

DWord	Bit	Description
0	31:0	**Considerations** Format: U32 This 32-bit field returns bits 31:0 of the GPU tick counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Graphics Master Interrupt

GFX_MSTR_INTR - Graphics Master Interrupt

Register Space: MMIO: 0/2/0

Source: BSpec

Size (in bits): 32

Address: 190010h

Top level register that indicates interrupt from hardware.
Bits in this register are set interrupts are pending in the underlying PCU, display or GT interrupts

DWord	Bit	Description
0	31	**Master Interrupt** Access: R/W This is the master control for graphics interrupts. This must be enabled for any of these interrupts to propagate to PCI device interrupt . Value: 0b — Name: **[Default]** — BSpec
	30	**PCU** Access: RO Variant Value: 0b — Name: **[Default]** — BSpec
	29	**GU_MISC** Access: RO Variant Value: 0b — Name: **[Default]** — BSpec
	28:17	**Reserved** Reserved
	16	**Display** Access: RO Variant Value: 0b — Name: **[Default]** — BSpec
	15:2	**Reserved** Reserved

GFX_MSTR_INTR - Graphics Master Interrupt

	1	**GT DW1** Access: RO Variant **Value** / **Name** 0b **[Default]** BSpec
	0	**GT DW0** Access: RO Variant **Value** / **Name** 0b **[Default]** BSpec

Graphics Memory Range Address

GMADR_0_2_0_PCI - Graphics Memory Range Address

Register Space:	PCI: 0/2/0
Source:	BSpec
Size (in bits):	64
Address:	00018h

GMADR is the PCI aperture used by S/W to access tiled GFX surfaces in a linear fashion.

DWord	Bit	Description
0	63:32	**Memory Base Address** Default Value: 00000000h Access: R/W Set by the OS, these bits correspond to address signals [63:32].
	31	**4096 MB Address Mask** Default Value: 0b Access: R/W Lock This bit is either part of the Memory Base Address (R/W) or part of Address Mask (RO) depending on the value of MSAC.APSZ. RO and forced to 0 when MSAC.APSZ >= 4096MB. (i.e. MSAC.APSZ[4]=1)
	30	**2048 MB Address Mask** Default Value: 0b Access: R/W Lock This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ. RO and forced to 0 when MSAC.APSZ >= 2048MB. (i.e. MSAC.APSZ[3]=1)
	29	**1024 MB Address Mask** Default Value: 0b Access: R/W Lock This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ. RO and forced to 0 when MSAC.APSZ >= 1024MB. (i.e. MSAC.APSZ[2]=1)
	28	**512MB Address Mask** Default Value: 0b

GMADR_0_2_0_PCI - Graphics Memory Range Address

		Access: R/W Lock This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ. RO and forced to 0 when MSAC.APSZ >= 512MB. (i.e. MSAC.APSZ[1]=1)
	27	**256 MB Address Mask** Default Value: 0b Access: R/W Lock This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ. RO and forced to 0 when MSAC.APSZ >= 256MB. (i.e. MSAC.APSZ[0]=1)
	26:4	**Address Mask** Default Value: 00000000000000000000000b Access: RO Hardwired to 0s to indicate at least 128MB address range.
	3	**Prefetchable Memory** Default Value: 1b Access: RO Hardwired to 1 to enable prefetching.
	2:1	**Memory Type** Default Value: 10b Access: RO Hardwired to 2h to indicate 64 bit base address.
	0	**Memory/IO Space** Default Value: 0b Access: RO Hardwired to 0 to indicate memory space.

Graphics MOCS LECC 00 TC 00 Register

GFX_MOCS_LECC_00_TC_00 - Graphics MOCS LECC 00 TC 00 Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0C800h
Name:	Graphics MOCS 0
ShortName:	GFX_MOCS_0
Address:	0C840h
Name:	Graphics MOCS 16
ShortName:	GFX_MOCS_16
Address:	0C880h
Name:	Graphics MOCS 32
ShortName:	GFX_MOCS_32
Address:	0C8C0h
Name:	Graphics MOCS 48
ShortName:	GFX_MOCS_48

GFX MOCS register

DWord	Bit	Description
0	31:19	**Reserved** Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service**

GFX_MOCS_LECC_00_TC_00 - Graphics MOCS LECC 00 TC 00 Register

	Default Value:	00b
	Access:	R/W

Class of Service sent to LLC to determine subset of ways the memory object will be stored in.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3
Max QoS:* Class 0
Relative QoS:* 0 > 1 > 2 ≥ 3**
* Max/Relative statements above based on default/non-firmware-overridden GT QoS masks.
** CLOS2 = CLOS3 equivalence only on 4-way LLC SKUs.

14 **Snoop Control Field**

Default Value:	0b
Access:	R/W

Description
Not used in ICL.

13:11 **Page Faulting Mode**

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8 **Skip Caching control**

Default Value:	000b
Access:	R/W

Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface.
If "0" - than corresponding address bit value is do not care
Bit[8]=1: address bit[9] needs to be "0" to cache in target
Bit[9]=1: address bit[10] needs to be "0" to cache in target
Bit[10]=1: address bit[11] needs to be "0" to cache in target

7 **Enable Reverse Skip Caching**

Default Value:	0b
Access:	R/W

GFX_MOCS_LECC_00_TC_00 - Graphics MOCS LECC 00 TC 00 Register

		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W

GFX_MOCS_LECC_00_TC_00 - Graphics MOCS LECC 00 TC 00 Register		
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based contr ols have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

Graphics MOCS LECC 00 TC 01 Register

GFX_MOCS_LECC_00_TC_01 - Graphics MOCS LECC 00 TC 01 Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0C804h
Name:	Graphics MOCS 1
ShortName:	GFX_MOCS_1
Address:	0C844h
Name:	Graphics MOCS 17
ShortName:	GFX_MOCS_17
Address:	0C884h
Name:	Graphics MOCS 33
ShortName:	GFX_MOCS_33
Address:	0C8C4h
Name:	Graphics MOCS 49
ShortName:	GFX_MOCS_49

GFX MOCS register

DWord	Bit	Description
0	31:19	**Reserved** Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service**

GFX_MOCS_LECC_00_TC_01 - Graphics MOCS LECC 00 TC 01 Register

	Default Value:	00b
	Access:	R/W

Class of Service sent to LLC to determine subset of ways the memory object will be stored in.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3
Max QoS:* Class 0
Relative QoS:* 0 > 1 > 2 ≥ 3**
* Max/Relative statements above based on default/non-firmware-overridden GT QoS masks.
** CLOS2 = CLOS3 equivalence only on 4-way LLC SKUs.

14 **Snoop Control Field**

Default Value:	0b
Access:	R/W

Description
Not used in ICL.

13:11 **Page Faulting Mode**

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8 **Skip Caching control**

Default Value:	000b
Access:	R/W

Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface.
If "0" - than corresponding address bit value is do not care
Bit[8]=1: address bit[9] needs to be "0" to cache in target
Bit[9]=1: address bit[10] needs to be "0" to cache in target
Bit[10]=1: address bit[11] needs to be "0" to cache in target

7 **Enable Reverse Skip Caching**

Default Value:	0b
Access:	R/W

GFX_MOCS_LECC_00_TC_01 - Graphics MOCS LECC 00 TC 01 Register

		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W

GFX_MOCS_LECC_00_TC_01 - Graphics MOCS LECC 00 TC 01 Register		
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based contr ols have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

Graphics MOCS LECC 00 TC 10 Register

GFX_MOCS_LECC_00_TC_10 - Graphics MOCS LECC 00 TC 10 Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0C808h
Name:	Graphics MOCS 2
ShortName:	GFX_MOCS_2
Address:	0C848h
Name:	Graphics MOCS 18
ShortName:	GFX_MOCS_18
Address:	0C888h
Name:	Graphics MOCS 34
ShortName:	GFX_MOCS_34
Address:	0C8C8h
Name:	Graphics MOCS 50
ShortName:	GFX_MOCS_50

GFX MOCS register

DWord	Bit	Description
0	31:19	**Reserved** Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service**

GFX_MOCS_LECC_00_TC_10 - Graphics MOCS LECC 00 TC 10 Register

	Default Value:	00b
	Access:	R/W

Class of Service sent to LLC to determine subset of ways the memory object will be stored in.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3
Max QoS:* Class 0
Relative QoS:* 0 > 1 > 2 ≥ 3**
* Max/Relative statements above based on default/non-firmware-overridden GT QoS masks.
** CLOS2 = CLOS3 equivalence only on 4-way LLC SKUs.

14 **Snoop Control Field**

Default Value:	0b
Access:	R/W

Description
Not used in ICL.

13:11 **Page Faulting Mode**

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8 **Skip Caching control**

Default Value:	000b
Access:	R/W

Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface.
If "0" - than corresponding address bit value is do not care
Bit[8]=1: address bit[9] needs to be "0" to cache in target
Bit[9]=1: address bit[10] needs to be "0" to cache in target
Bit[10]=1: address bit[11] needs to be "0" to cache in target

7 **Enable Reverse Skip Caching**

Default Value:	0b
Access:	R/W

GFX_MOCS_LECC_00_TC_10 - Graphics MOCS LECC 00 TC 10 Register

		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W

GFX_MOCS_LECC_00_TC_10 - Graphics MOCS LECC 00 TC 10 Register		
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based contr ols have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

Graphics MOCS LECC 01 TC 00 Register

GFX_MOCS_LECC_01_TC_00 - Graphics MOCS LECC 01 TC 00 Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0C80Ch
Name:	Graphics MOCS 3
ShortName:	GFX_MOCS_3
Address:	0C84Ch
Name:	Graphics MOCS 19
ShortName:	GFX_MOCS_19
Address:	0C88Ch
Name:	Graphics MOCS 35
ShortName:	GFX_MOCS_35
Address:	0C8CCh
Name:	Graphics MOCS 51
ShortName:	GFX_MOCS_51

GFX MOCS register

DWord	Bit	Description
0	31:19	**Reserved** Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service**

GFX_MOCS_LECC_01_TC_00 - Graphics MOCS LECC 01 TC 00 Register

	Default Value:	00b
	Access:	R/W

Class of Service sent to LLC to determine subset of ways the memory object will be stored in.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3
Max QoS:* Class 0
Relative QoS:* 0 > 1 > 2 ≥ 3**
* Max/Relative statements above based on default/non-firmware-overridden GT QoS masks.
** CLOS2 = CLOS3 equivalence only on 4-way LLC SKUs.

14 **Snoop Control Field**

Default Value:	0b
Access:	R/W

Description
Not used in ICL.

13:11 **Page Faulting Mode**

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8 **Skip Caching control**

Default Value:	000b
Access:	R/W

Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface.
If "0" - than corresponding address bit value is do not care
Bit[8]=1: address bit[9] needs to be "0" to cache in target
Bit[9]=1: address bit[10] needs to be "0" to cache in target
Bit[10]=1: address bit[11] needs to be "0" to cache in target

7 **Enable Reverse Skip Caching**

Default Value:	0b
Access:	R/W

GFX_MOCS_LECC_01_TC_00 - Graphics MOCS LECC 01 TC 00 Register

		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W

GFX_MOCS_LECC_01_TC_00 - Graphics MOCS LECC 01 TC 00 Register		
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based contr ols have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

Graphics MOCS LECC 10 TC 00 Register

GFX_MOCS_LECC_10_TC_00 - Graphics MOCS LECC 10 TC 00 Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0C810h
Name:	Graphics MOCS 4
ShortName:	GFX_MOCS_4
Address:	0C828h
Name:	Graphics MOCS 10
ShortName:	GFX_MOCS_10
Address:	0C850h
Name:	Graphics MOCS 20
ShortName:	GFX_MOCS_20
Address:	0C868h
Name:	Graphics MOCS 26
ShortName:	GFX_MOCS_26
Address:	0C890h
Name:	Graphics MOCS 36
ShortName:	GFX_MOCS_36
Address:	0C8A8h
Name:	Graphics MOCS 42
ShortName:	GFX_MOCS_42
Address:	0C8D0h
Name:	Graphics MOCS 52
ShortName:	GFX_MOCS_52
Address:	0C8E8h
Name:	Graphics MOCS 58
ShortName:	GFX_MOCS_58
GFX MOCS register	

DWord	Bit	Description
0	31:19	**Reserved**

GFX_MOCS_LECC_10_TC_00 - Graphics MOCS LECC 10 TC 00 Register

	Default Value:	0000000000000b
	Access:	RO

18:17 Self Snoop Enable

Default Value:	00b
Access:	R/W

00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic
01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface
11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface

16:15 Class of Service

Default Value:	00b
Access:	R/W

Class of Service sent to LLC to determine subset of ways the memory object will be stored in.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3
Max QoS:* Class 0
Relative QoS:* 0 > 1 > 2 ≥ 3**
* Max/Relative statements above based on default/non-firmware-overridden GT QoS masks.
** CLOS2 = CLOS3 equivalence only on 4-way LLC SKUs.

14 Snoop Control Field

Default Value:	0b
Access:	R/W

Description
Not used in ICL.

13:11 Page Faulting Mode

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)

GFX_MOCS_LECC_10_TC_00 - Graphics MOCS LECC 10 TC 00 Register

		001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is do not care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0"

GFX_MOCS_LECC_10_TC_00 - Graphics MOCS LECC 10 TC 00 Register

		00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based contr ols have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

Graphics MOCS LECC 10 TC 01 Register

GFX_MOCS_LECC_10_TC_01 - Graphics MOCS LECC 10 TC 01 Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0C814h
Name:	Graphics MOCS 5
ShortName:	GFX_MOCS_5
Address:	0C82Ch
Name:	Graphics MOCS 11
ShortName:	GFX_MOCS_11
Address:	0C854h
Name:	Graphics MOCS 21
ShortName:	GFX_MOCS_21
Address:	0C86Ch
Name:	Graphics MOCS 27
ShortName:	GFX_MOCS_27
Address:	0C894h
Name:	Graphics MOCS 37
ShortName:	GFX_MOCS_37
Address:	0C8ACh
Name:	Graphics MOCS 43
ShortName:	GFX_MOCS_43
Address:	0C8D4h
Name:	Graphics MOCS 53
ShortName:	GFX_MOCS_53
Address:	0C8ECh
Name:	Graphics MOCS 59
ShortName:	GFX_MOCS_59

GFX MOCS register

DWord	Bit	Description
0	31:19	**Reserved**

GFX_MOCS_LECC_10_TC_01 - Graphics MOCS LECC 10 TC 01 Register

	Default Value:	0000000000000b
	Access:	RO

18:17 **Self Snoop Enable**

Default Value:	00b
Access:	R/W

00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic
01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface
11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface

16:15 **Class of Service**

Default Value:	00b
Access:	R/W

Class of Service sent to LLC to determine subset of ways the memory object will be stored in.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3
Max QoS:* Class 0
Relative QoS:* 0 > 1 > 2 ≥ 3**
* Max/Relative statements above based on default/non-firmware-overridden GT QoS masks.
** CLOS2 = CLOS3 equivalence only on 4-way LLC SKUs.

14 **Snoop Control Field**

Default Value:	0b
Access:	R/W

Description
Not used in ICL.

13:11 **Page Faulting Mode**

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)

GFX_MOCS_LECC_10_TC_01 - Graphics MOCS LECC 10 TC 01 Register

		001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is do not care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0"

GFX_MOCS_LECC_10_TC_01 - Graphics MOCS LECC 10 TC 01 Register

		00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based contr ols have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

Graphics MOCS LECC 10 TC 10 Register

GFX_MOCS_LECC_10_TC_10 - Graphics MOCS LECC 10 TC 10 Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0C818h
Name:	Graphics MOCS 6
ShortName:	GFX_MOCS_6
Address:	0C830h
Name:	Graphics MOCS 12
ShortName:	GFX_MOCS_12
Address:	0C858h
Name:	Graphics MOCS 22
ShortName:	GFX_MOCS_22
Address:	0C870h
Name:	Graphics MOCS 28
ShortName:	GFX_MOCS_28
Address:	0C898h
Name:	Graphics MOCS 38
ShortName:	GFX_MOCS_38
Address:	0C8B0h
Name:	Graphics MOCS 44
ShortName:	GFX_MOCS_44
Address:	0C8D8h
Name:	Graphics MOCS 54
ShortName:	GFX_MOCS_54
Address:	0C8F0h
Name:	Graphics MOCS 60
ShortName:	GFX_MOCS_60
GFX MOCS register	

DWord	Bit	Description
0	31:19	**Reserved**

GFX_MOCS_LECC_10_TC_10 - Graphics MOCS LECC 10 TC 10 Register

	Default Value:	0000000000000b
	Access:	RO

18:17 Self Snoop Enable

Default Value:	00b
Access:	R/W

00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic
01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface
11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface

16:15 Class of Service

Default Value:	00b
Access:	R/W

Class of Service sent to LLC to determine subset of ways the memory object will be stored in.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3
Max QoS:* Class 0
Relative QoS:* 0 > 1 > 2 ≥ 3**
* Max/Relative statements above based on default/non-firmware-overridden GT QoS masks.
** CLOS2 = CLOS3 equivalence only on 4-way LLC SKUs.

14 Snoop Control Field

Default Value:	0b
Access:	R/W

Description
Not used in ICL.

13:11 Page Faulting Mode

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)

GFX_MOCS_LECC_10_TC_10 - Graphics MOCS LECC 10 TC 10 Register

		001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is do not care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0"

GFX_MOCS_LECC_10_TC_10 - Graphics MOCS LECC 10 TC 10 Register

		00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based contr ols have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

Graphics MOCS LECC 11 TC 00 Register

GFX_MOCS_LECC_11_TC_00 - Graphics MOCS LECC 11 TC 00 Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0C81Ch
Name:	Graphics MOCS 7
ShortName:	GFX_MOCS_7
Address:	0C834h
Name:	Graphics MOCS 13
ShortName:	GFX_MOCS_13
Address:	0C85Ch
Name:	Graphics MOCS 23
ShortName:	GFX_MOCS_23
Address:	0C874h
Name:	Graphics MOCS 29
ShortName:	GFX_MOCS_29
Address:	0C89Ch
Name:	Graphics MOCS 39
ShortName:	GFX_MOCS_39
Address:	0C8B4h
Name:	Graphics MOCS 45
ShortName:	GFX_MOCS_45
Address:	0C8DCh
Name:	Graphics MOCS 55
ShortName:	GFX_MOCS_55
Address:	0C8F4h
Name:	Graphics MOCS 61
ShortName:	GFX_MOCS_61

GFX MOCS register

DWord	Bit	Description
0	31:19	**Reserved**

GFX_MOCS_LECC_11_TC_00 - Graphics MOCS LECC 11 TC 00 Register

	Default Value:	0000000000000b
	Access:	RO

18:17 Self Snoop Enable

Default Value:	00b
Access:	R/W

00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic
01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface
11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface

16:15 Class of Service

Default Value:	00b
Access:	R/W

Class of Service sent to LLC to determine subset of ways the memory object will be stored in.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3
Max QoS:* Class 0
Relative QoS:* 0 > 1 > 2 ≥ 3**
* Max/Relative statements above based on default/non-firmware-overridden GT QoS masks.
** CLOS2 = CLOS3 equivalence only on 4-way LLC SKUs.

14 Snoop Control Field

Default Value:	0b
Access:	R/W

Description
Not used in ICL.

13:11 Page Faulting Mode

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)

GFX_MOCS_LECC_11_TC_00 - Graphics MOCS LECC 11 TC 00 Register

		001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is do not care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0"

		00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based contr ols have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

Graphics MOCS LECC 11 TC 01 Register

GFX_MOCS_LECC_11_TC_01 - Graphics MOCS LECC 11 TC 01 Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0C820h
Name:	Graphics MOCS 8
ShortName:	GFX_MOCS_8
Address:	0C838h
Name:	Graphics MOCS 14
ShortName:	GFX_MOCS_14
Address:	0C860h
Name:	Graphics MOCS 24
ShortName:	GFX_MOCS_24
Address:	0C878h
Name:	Graphics MOCS 30
ShortName:	GFX_MOCS_30
Address:	0C8A0h
Name:	Graphics MOCS 40
ShortName:	GFX_MOCS_40
Address:	0C8B8h
Name:	Graphics MOCS 46
ShortName:	GFX_MOCS_46
Address:	0C8E0h
Name:	Graphics MOCS 56
ShortName:	GFX_MOCS_56
Address:	0C8F8h
Name:	Graphics MOCS 62
ShortName:	GFX_MOCS_62

GFX MOCS register

DWord	Bit	Description
0	31:19	**Reserved**

GFX_MOCS_LECC_11_TC_01 - Graphics MOCS LECC 11 TC 01 Register

	Default Value:	0000000000000b
	Access:	RO

18:17 Self Snoop Enable

Default Value:	00b
Access:	R/W

00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic
01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface
11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface

16:15 Class of Service

Default Value:	00b
Access:	R/W

Class of Service sent to LLC to determine subset of ways the memory object will be stored in.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3
Max QoS:* Class 0
Relative QoS:* 0 > 1 > 2 ≥ 3**
* Max/Relative statements above based on default/non-firmware-overridden GT QoS masks.
** CLOS2 = CLOS3 equivalence only on 4-way LLC SKUs.

14 Snoop Control Field

Default Value:	0b
Access:	R/W

Description
Not used in ICL.

13:11 Page Faulting Mode

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)

GFX_MOCS_LECC_11_TC_01 - Graphics MOCS LECC 11 TC 01 Register

		001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is do not care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0"

		00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based contr ols have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

Graphics MOCS LECC 11 TC 10 Register

GFX_MOCS_LECC_11_TC_10 - Graphics MOCS LECC 11 TC 10 Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0C824h
Name:	Graphics MOCS 9
ShortName:	GFX_MOCS_9
Address:	0C83Ch
Name:	Graphics MOCS 15
ShortName:	GFX_MOCS_15
Address:	0C864h
Name:	Graphics MOCS 25
ShortName:	GFX_MOCS_25
Address:	0C87Ch
Name:	Graphics MOCS 31
ShortName:	GFX_MOCS_31
Address:	0C8A4h
Name:	Graphics MOCS 41
ShortName:	GFX_MOCS_41
Address:	0C8BCh
Name:	Graphics MOCS 47
ShortName:	GFX_MOCS_47
Address:	0C8E4h
Name:	Graphics MOCS 57
ShortName:	GFX_MOCS_57
Address:	0C8FCh
Name:	Graphics MOCS 63
ShortName:	GFX_MOCS_63

GFX MOCS register

DWord	Bit	Description
0	31:19	**Reserved**

GFX_MOCS_LECC_11_TC_10 - Graphics MOCS LECC 11 TC 10 Register

	Default Value:	0000000000000b
	Access:	RO

18:17 Self Snoop Enable

Default Value:	00b
Access:	R/W

00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic
01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface
11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface

16:15 Class of Service

Default Value:	00b
Access:	R/W

Class of Service sent to LLC to determine subset of ways the memory object will be stored in.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3
Max QoS:* Class 0
Relative QoS:* 0 > 1 > 2 ≥ 3**
* Max/Relative statements above based on default/non-firmware-overridden GT QoS masks.
** CLOS2 = CLOS3 equivalence only on 4-way LLC SKUs.

14 Snoop Control Field

Default Value:	0b
Access:	R/W

Description
Not used in ICL.

13:11 Page Faulting Mode

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)

GFX_MOCS_LECC_11_TC_10 - Graphics MOCS LECC 11 TC 10 Register

		001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is do not care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0"

GFX_MOCS_LECC_11_TC_10 - Graphics MOCS LECC 11 TC 10 Register

		00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based contr ols have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

Graphics Mode Register

GFX_MODE - Graphics Mode Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	0229Ch-0229Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_RCSUNIT
Address:	1829Ch-1829Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_POCSUNIT
Address:	2229Ch-2229Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_BCSUNIT
Address:	1C029Ch-1C029Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_VCSUNIT0
Address:	1C429Ch-1C429Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_VCSUNIT1
Address:	1C829Ch-1C829Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_VECSUNIT0
Address:	1D029Ch-1D029Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_VCSUNIT2
Address:	1D429Ch-1D429Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_VCSUNIT3
Address:	1D829Ch-1D829Fh
Name:	Graphics Mode Register

GFX_MODE - Graphics Mode Register

ShortName:	GFX_MODE_VECSUNIT1
Address:	1E029Ch-1E029Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_VCSUNIT4
Address:	1E429Ch-1E429Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_VCSUNIT5
Address:	1E829Ch-1E829Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_VECSUNIT2
Address:	1F029Ch-1F029Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_VCSUNIT6
Address:	1F429Ch-1F429Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_VCSUNIT7
Address:	1F829Ch-1F829Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_VECSUNIT3

This register contains a control bit for the new execlist and 2-level PPGTT functions.

Programming Notes	Source
"Privilege Check Disable" is the only programmable bits in GFX_MODE register for PositionCS, functionality for the rest of the bits is not supported by Position command streamer.	PositionCS

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15	**Reserved** Format: PBC
	14	**Reserved** Format: PBC

GFX_MODE - Graphics Mode Register

13 **Reserved**

Source:	VideoCS, VideoEnhancementCS, PositionCS
Exists If:	//VideoCS, VideoEnhancementCS, PositionCS
Format:	PBC

13 **Reserved**

Source:	RenderCS
Exists If:	//RenderCS
Format:	PBC

12 **Reserved**

Format:	PBC

11 **Virtual Function MMIO Read Access Control**

This bit controls the disabling and enabling of MMIO read access of an virtual function context running on an engine.

Value	Name	Description
0	**[Default]**	A VF context running on an engine can do MMIO read access to other engines. Ex: VF context running on RenderCS can do MMIO read access to VideoCS.
1		A VF context running on an engine can't do MMIO read access to other engines. Ex: VF context running on RenderCS can't do MMIO read access to VideoCS.

10 **Reserved**

Format:	PBC

9 **Per-Process GTT Enable**

Per-Process GTT Enable

Value	Name	Description
0h	PPGTT Disable **[Default]**	When clear, the Global GTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.
1h	PPGTT Enable	When set, the PPGTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.

Programming Notes
This bit is used for enabling PPGTT access in Ring Buffer mode of scheduling. Privilege field in

context descriptor states the same in Execlist Mode of scheduling. This field should be set before programming PDP0/1/2/3 registers in order to set the PPGTT translation of memory access.
Programming this bit doesn't enable or disable the PPGTT translation of memory access immediately; the change comes in to affect only when the Page Directory registers are programmed. Programming this bit must be followed by programming Page Directory Registers in order to enable or disable the PPGTT translation of memory access.

8 **Reserved**

8 **Reserved**

Source:	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS
Format:	PBC

7 **64Bit Virtual Addressing Enable**

64Bit Virtual Addressing Enable

Value	Name	Description
0h	64Bit Virtual Addressing Disable **[Default]**	When clear indicates GFX operating in 32bit Virtual Addressing for PPGTT based memory access.
1h	64Bit Virtual Addressing Enable	When Set indicates GFX operating in 64bit (48bit Canonical) Virtual Addressing for PPGTT based memory access.

Programming Notes

This bit is only valid when PPGTT is enabled in ring buffer mode of scheduling. Context Descriptor has a similar bit to control 64bit virtual addressing in execlist mode of scheduling. Whether this field is set or clear virtual addresses translated through GGTT are always 32Bit. This field should be programmed before enabling PPGTT access. When this field is not set or for GGTT virtual addresses, Graphics Address [47:32] field of any commands or register exercised by SW should be programmed to 0x0.

6:5 **Reserved**

4 **Reserved**

3 **Disable Legacy Mode**

Description

This bit must be set to disable Legacy behavior to support features added for the current project.

When set the size of the CSB status FIFO is 12 deep.

Value	Name	Description
0h	Enable Legacy **[Default]**	Any features using this bit will be compatible with legacy drivers.
1h	Disable Legacy	HW will not be compatible with legacy drivers.

GFX_MODE - Graphics Mode Register

		Programming Notes A graphics reset is required prior to changing the value of this bit.
	2	**Reserved** Format: PBC
	1	**Reserved** Format: PBC
	0	**Privilege Check Disable** This field when set, disables Privilege Violation checks on non-privileged batch buffers. When set Privileged commands are allowed to be executed from non-privileged batch buffers.

Graphics Virtual Master Interrupt

GFX_VIRT_MSTR_INTR - Graphics Virtual Master Interrupt

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	191010h
Name:	VF1_GFX_MSTR_INTR
Address:	192010h
Name:	VF2_GFX_MSTR_INTR
Address:	193010h
Name:	VF3_GFX_MSTR_INTR
Address:	194010h
Name:	VF4_GFX_MSTR_INTR
Address:	195010h
Name:	VF5_GFX_MSTR_INTR
Address:	196010h
Name:	VF6_GFX_MSTR_INTR
Address:	197010h
Name:	VF7_GFX_MSTR_INTR

Top level register that indicates interrupt from hardware.
Bits in this register are set interrupts are pending in the underlying PCU, display or GT interrupts

DWord	Bit	Description
0	31	**Master Interrupt** Access: R/W
	30	**PCU** Access: RO
	29:17	**Reserved**
	16	**Display** Access: RO
	15:2	**Reserved**
	1	**GT DW1** Access: R/W

GFX_VIRT_MSTR_INTR - Graphics Virtual Master Interrupt		
	0	**GT DW0** Access: R/W

GS Invocation Counter

GS_INVOCATION_COUNT - GS Invocation Counter	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02328h
Name:	GS Invocation Counter
ShortName:	GS_INVOCATION_COUNT

This register stores the number of objects that are part of geometry shader threads. This register is part of the context save and restore.

DWord	Bit	Description
0	63:32	**GS Invocation Count UDW** Number of objects that are dispatched as a geometry shader threads invoked by the GS stage. Updated only when **Statistics Enable** is set in GS_STATE (see the Geometry Shader Chapter in the 3D Volume.)
	31:0	**GS Invocation Count LDW** Number of objects that are dispatched as a geometry shader threads invoked by the GS stage. Updated only when **Statistics Enable** is set in GS_STATE (see the Geometry Shader Chapter in the 3D Volume.)

GS Primitives Counter

GS_PRIMITIVES_COUNT - GS Primitives Counter

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02330h
Name:	GS Primitives Counter
ShortName:	GS_PRIMITIVES_COUNT

This register reflects the total number of primitives that have been output by the Geometry Shader stage. This register is part of the context save and restore.

DWord	Bit	Description
0	63:32	**GS Primitives Count UDW** Total number of primitives output by the geometry stage. Updated only when Statistics Enable is set in GS_STATE (see the Geometry Shader Chapter in the 3D Volume.)
	31:0	**GS Primitives Count LDW** Total number of primitives output by the geometry stage. Updated only when Statistics Enable is set in GS_STATE (see the Geometry Shader Chapter in the 3D Volume.)

GT4 Mode Control Register

GT4MODECTL - GT4 Mode Control Register		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	09038h	
GT4 Mode Control Register		
DWord	**Bit**	**Description**
0	31:18	**RSVD** Access: R/W
	17:10	**Reserved**
	9:2	**Reserved**
	1:0	**GT4 Mode Control** Access: R/W GT4 Usage mode: 00b: Non-GT4. 01b: GT4 is used in Alternate Frame rendering Mode (AFR). 10b: Basic Split Frame rendering Mode (SFR). 11b: Complex Split Frame rendering Mode (SFR w/ CBR).

GTC_CTL

GTC_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	67000h-67003h
Name:	Global Time Code Control
ShortName:	GTC_CTL
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31	**GTC Function Enable** This bit enables the GTC counter. Value / Name: 0b – Disable 1b – Enable Restriction: Enable this bit before enabling GTC controller operation on a port with a GTC capable device.
	30:29	**Reserved** Format: MBZ
	28:13	**Reserved**
	12:1	**Reserved** Format: MBZ
	0	**Reserved**

GTC_DDA_M

GTC_DDA_M		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Access:	R/W	
Size (in bits):	32	
Address:	67010h-67013h	
Name:	Global Time Code DDA M	
ShortName:	GTC_DDA_M	
Power:	PG1	
Reset:	soft	
DWord	**Bit**	**Description**
0	31:24	**Reserved**
	23:0	**GTC DDA M** This field is used to program the M value of the GTC DDA. The ratio of M to N programmed depends on the GTC reference clock. The DDA programmed values are related by the following formula: 1/(accumulator increment) = Reference Clock * DDA_M / DDA_N

GTC_DDA_N

GTC_DDA_N		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Access:	R/W	
Size (in bits):	32	
Address:	67014h-67017h	
Name:	Global Time Code DDA N	
ShortName:	GTC_DDA_N	
Power:	PG1	
Reset:	soft	

DWord	Bit	Description
0	31:24	**GTC Accum Inc** Format: U7.1 This field is the GTC accumulator increment value in nanoseconds each time the DDA trips. It is programmed in 7.1 fixed point binary format where the LSB represents 0.5ns increment.
	23:0	**GTC DDA N** This field is used to program the N value of the GTC DDA. The ratio of M to N programmed depends on the GTC reference clock and should not result in any accumulation error in any 10ms interval period. The DDA programmed values are related by the following formula: 1/(accumulator increment) = Reference Clock * DDA_M / DDA_N

GTC_IIR

GTC_IIR	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/WC
Size (in bits):	32
Address:	67058h-6705Bh
Name:	Global Time Code Interrupt Identity
ShortName:	GTC_IIR
Power:	PG1
Reset:	soft

See the GTC interrupt bit definition to find the source event for each interrupt bit.

DWord	Bit	Description
0	31:0	**Interrupt Identity Bits** This field holds the persistent values of the GTC interrupt bits which are unmasked by the GTC_IMR. Bits set in this register will propagate to the GTC interrupt in the Display Engine Miscellaneous Interrupts. Bits set in this register will remain set (persist) until the interrupt condition is cleared by writing a '1' to the appropriate bits.

Value	Name
0b	Condition Not Detected
1b	Condition Detected

GTC_IMR

GTC_IMR	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	67054h-67057h
Name:	Global Time Code Interrupt Mask
ShortName:	GTC_IMR
Power:	PG1
Reset:	soft

See the GTC interrupt bit definition to find the source event for each interrupt bit.

DWord	Bit	Description
0	31:0	**Interrupt Mask Bits** This field contains a bit mask which selects which GTC events are reported int the GTC IIR.

Value	Name
0b	Not Masked
1b	Masked
FFFFFFFFh	All interrupts masked **[Default]**

GTC_LIVE

GTC_LIVE		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Access:	RO	
Size (in bits):	32	
Address:	67020h-67023h	
Name:	Global Time Code Live	
ShortName:	GTC_LIVE	
Power:	PG1	
Reset:	soft	

DWord	Bit	Description
0	31:0	**GTC Live Value** This field contains the live current value of the GTC. It is inactive when the GTC controller function is disabled. This register also samples and holds the live GTC value following a Audio Time Capture (ATC) event until software reads this register. A subsequent read of this register will reflect the live value.

GTC_PORT_CTL

GTC_PORT_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	64070h-64073h
Name:	DDI A GTC Port Control
ShortName:	GTC_PORT_CTL_A
Power:	PG1
Reset:	soft
Address:	64170h-64173h
Name:	DDI B GTC Port Control
ShortName:	GTC_PORT_CTL_B
Power:	PG2
Reset:	soft
Address:	64270h-64273h
Name:	DDI C GTC Port Control
ShortName:	GTC_PORT_CTL_C
Power:	PG2
Reset:	soft
Address:	64370h-64373h
Name:	DDI D GTC Port Control
ShortName:	GTC_PORT_CTL_D
Power:	PG2
Reset:	soft
Address:	64470h-64473h
Name:	DDI E GTC Port Control
ShortName:	GTC_PORT_CTL_E

GTC_PORT_CTL

Power: PG2
Reset: soft

Address: 64570h-64573h
Name: DDI F GTC Port Control
ShortName: GTC_PORT_CTL_F

Power: PG2
Reset: soft

DWord	Bit	Description
0	31	**Port Global Time Code Enable** This bit enables the GTC controller to start lock acquisition phase with remote GTC sink connected to this port. This bit has no effect if the GTC controller is disabled. **Value** / **Name** 0b – Disable 1b – Enable **Restriction** The Maintenance Phase Enable bit must be initially written as '0' when this bit is set.
	30:25	**Reserved**
	24	**Maintenance Phase Enable** This bit is used by software to transition from lock acquisition to lock maintenance phase. The GTC controller generates an interrupt at the end of the lock phase as determined by lock acquisition duration field. Software shall read the sink device GTC lock done bit. If set, software shall set this bit to '1' after first writing the GTC skew value to the RX GTC skew DPCD offset with GTC skew enable bit set to '1'. **Value** / **Name** / **Description** 0b – Lock – Lock acquisition phase. The controller writes or reads GTC every 1ms. 1b – Maintain – Lock maintenance phase. The controller writes or reads GTC every 10ms.
	23:1	**Reserved**
	0	**Port RX Lock Done** This bit indicates the remote GTC sink has achieved lock. This bit shall be written by software after reading remote GTC sink DPCD register. This bit shall be cleared by software when GTC controller is reset from lock maintenance mode to lock acquisition mode or when the controller is disabled. **Value** / **Name** 0b – Not Locked 1b – Locked

GTC_PORT_MISC

GTC_PORT_MISC	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	64094h-64097h
Name:	DDI A GTC Port Miscellaneous
ShortName:	GTC_PORT_MISC_A
Power:	PG1
Reset:	soft
Address:	64194h-64197h
Name:	DDI B GTC Port Miscellaneous
ShortName:	GTC_PORT_MISC_B
Power:	PG2
Reset:	soft
Address:	64294h-64297h
Name:	DDI C GTC Port Miscellaneous
ShortName:	GTC_PORT_MISC_C
Power:	PG2
Reset:	soft
Address:	64394h-64397h
Name:	DDI D GTC Port Miscellaneous
ShortName:	GTC_PORT_MISC_D
Power:	PG2
Reset:	soft
Address:	64494h-64497h
Name:	DDI E GTC Port Miscellaneous
ShortName:	GTC_PORT_MISC_E

GTC_PORT_MISC

Power:	PG2
Reset:	soft
Address:	64594h-64597h
Name:	DDI F GTC Port Miscellaneous
ShortName:	GTC_PORT_MISC_F
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31:22	**Reserved** Format: MBZ
	21:12	**GTC Update Message Delay** Default Value: 00110100b 52 nanoseconds This field programs the absolute delay in nanoseconds between the GTC at the aux sync point event and the corresponding GTC value at the capture point. It represents the delay between the GTC values at the aux sync point and capture point introduced due to synchronization and glitch suppression.
	11:8	**Min Lock Duration** Default Value: 1010b 10ms This field determines the minimum duration in milliseconds of lock acquisition and maintenance phase after which software is notified through interrupt. The GTC interrupt enable and mask register must be enabled beforehand. Software may also poll the interrupt identity bit in IIR.
	7:0	**Reserved** Format: MBZ

GTC_PORT_TX_CURR

GTC_PORT_TX_CURR	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	64078h-6407Bh
Name:	DDI A GTC Port TX Current
ShortName:	GTC_PORT_TX_CURR_A
Power:	PG1
Reset:	soft
Address:	64178h-6417Bh
Name:	DDI B GTC Port TX Current
ShortName:	GTC_PORT_TX_CURR_B
Power:	PG2
Reset:	soft
Address:	64278h-6427Bh
Name:	DDI C GTC Port TX Current
ShortName:	GTC_PORT_TX_CURR_C
Power:	PG2
Reset:	soft
Address:	64378h-6437Bh
Name:	DDI D GTC Port TX Current
ShortName:	GTC_PORT_TX_CURR_D
Power:	PG2
Reset:	soft
Address:	64478h-6447Bh
Name:	DDI E GTC Port TX Current
ShortName:	GTC_PORT_TX_CURR_E

GTC_PORT_TX_CURR

Power:	PG2
Reset:	soft
Address:	64578h-6457Bh
Name:	DDI F GTC Port TX Current
ShortName:	GTC_PORT_TX_CURR_F
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31:0	**Global Time Code Port TX Current** This field contains the local GTC value sampled at the Aux sync point of the response message from the remote GTC sink following software read of the remote sink GTC DPCD register.

GTC_PORT_TX_PREV

GTC_PORT_TX_PREV	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	64080h-64083h
Name:	DDI A GTC Port TX Previous
ShortName:	GTC_PORT_TX_PREV_A
Power:	PG1
Reset:	soft
Address:	64180h-64183h
Name:	DDI B GTC Port TX Previous
ShortName:	GTC_PORT_TX_PREV_B
Power:	PG2
Reset:	soft
Address:	64280h-64283h
Name:	DDI C GTC Port TX Previous
ShortName:	GTC_PORT_TX_PREV_C
Power:	PG2
Reset:	soft
Address:	64380h-64383h
Name:	DDI D GTC Port TX Previous
ShortName:	GTC_PORT_TX_PREV_D
Power:	PG2
Reset:	soft
Address:	64480h-64483h
Name:	DDI E GTC Port TX Previous
ShortName:	GTC_PORT_TX_PREV_E

GTC_PORT_TX_PREV

Power:	PG2
Reset:	soft
Address:	64580h-64583h
Name:	DDI F GTC Port TX Previous
ShortName:	GTC_PORT_TX_PREV_F
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31:0	**Global Time Code Port TX Previous** This field contains the previous local GTC value sampled at Aux sync point. It is transferred from the GTC_PORT_TX_CURR register when the current value is updated.

GTDRIVER_MAILBOX_DATA1

GTDRIVER_MAILBOX_DATA1 - GTDRIVER_MAILBOX_DATA1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	13812Ch

Data register for the GFX-DRIVER-to-PCODE mailbox. This mailbox is implemented as a means for tuning parameters for specific GFX workloads. This register is used in conjunction with GTDRIVER_MAILBOX_INTERFACE. THIS REGISTER IS DUPLICATED IN THE PCU I/O SPACE, XML CHANGES MUST BE MADE IN BOTH PLACES.

DWord	Bit	Description
0	31:0	**Considerations**

GTDRIVER_MAILBOX_INTERFACE

GTDRIVER_MAILBOX_INTERFACE - GTDRIVER_MAILBOX_INTERFACE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	138124h

Control and Status register for the GFX-DRIVER-to-PCODE mailbox. This mailbox is implemented as a means for tuning parameters for specific GFX workloads. This register is used in conjunction with GTDRIVER_MAILBOX_DATA. THIS REGISTER IS DUPLICATED IN THE PCU.

DWord	Bit	Description
0	31:0	**Considerations**

GTDRIVER_P2G_EVENTS

GTDRIVER_P2G_EVENTS - GTDRIVER_P2G_EVENTS			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Access:	R/W		
Size (in bits):	32		
Address:	138160h		
This extended capability allows PCODE to send an interrupt notification upon completion of a mailbox command. It is enabled via the GFX Driver Mailbox. PCODE will set the appropriate bit in this register to 1b, and will then write to 0.2.0.GTTMMADR.PIM[PCU_MBOXE]. The GFX Driver will clear the appropriate bit in this register by writing a 1 to the bit. THIS REGISTER IS DUPLICATED IN THE PCU I/O SPACE, XML CHANGES MUST BE MADE IN BOTH PLACES.			
DWord	**Bit**	**Description**	
0	31:0	**Considerations**	

GT Engine Interrupt Enable

GT_ENG_INTR_ENABLE - GT Engine Interrupt Enable

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	190030h
ShortName:	RENDER_COPY_INTR_ENABLE
Address:	190034h
ShortName:	VIDEODECODE_VIDEOENHANCE_INTR_ENABLE
Address:	190044h
ShortName:	GUNIT_CSME_INTR_ENABLE

SW/FW programs this register to control interrupt events that are to be ignored (dropped).
Register content is saved/restored during RC6.
Bits in the registers described above are in the order: Engine1_Engine0_INTR_ENABLE.

Register Address	Engine 1	Engine 0	Structure defining bits
190030	Render	Copy	Render: Render Engine Interrupt Vector Copy: Blitter Interrupt Vector
190034	Vide Decode	Video Enhace	Video Decode: VideoDecoder Interrupt Vector Video Enhance: VideEnhancement Interupt Vector
190044	GUnit	CSME	GUnit: G-Unit Interrupt Vector CSME: Manageability Engine Interrupt Vector
190048	CCS	Reserved	CCS: Compute CS Reserved

DWord	Bit	Description
0	31:16	**Engine1 Interrupt Enable** Default Value: 0000h Access: R/W
	15:0	**Engine0 Interrupt Enable** Default Value: 0000h Access: R/W

GT Engine Interrupt Mask

GT_ENG_INTR_MASK - GT Engine Interrupt Mask			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Size (in bits):	32		
Address:	190090h		
ShortName:	RCS0_RSVD_INTR_MASK		
Address:	1900A0h		
ShortName:	BCS_RSVD_INTR_MASK		
Address:	1900A8h		
ShortName:	VCS0_VCS1_INTR_MASK		
Address:	1900ACh		
ShortName:	VCS2_VCS3_INTR_MASK		
Address:	1900B0h		
ShortName:	VCS4_VCS5_INTR_MASK		
Address:	1900B4h		
ShortName:	VCS6_VCS7_INTR_MASK		
Address:	1900D0h		
ShortName:	VECS0_VECS1_INTR_MASK		
Address:	1900D4h		
ShortName:	VECS2_VECS3_INTR_MASK		
Address:	1900F4h		
ShortName:	GUNIT_CSME_INTR_MASK		
DWord	**Bit**	**Description**	
0	31:16	**Engine1 Interrupt Mask**	
		Default Value:	0000h
		Access:	R/W
	15:0	**Engine0 Interrupt Mask**	
		Default Value:	0000h
		Access:	R/W

GTICP BONUS1 Reg

GTICPBONUS1 - GTICP BONUS1 Reg		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	24014h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:16	**Message Mask** Access: RO Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:8	**Reserved** Access: RO Reserved
	7	**BONUS BIT 7** Access: R/W SLICE 0 BONUS BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS BIT 6** Access: R/W SLICE 0 BONUS BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS BIT 5** Access: R/W SLICE 0 BONUS BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS BIT 4** Access: R/W

GTICPBONUS1 - GTICP BONUS1 Reg

		SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	3	**BONUS BIT 3** Access: R/W SLICE 0 BONUS BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS BIT 2** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS BIT 1** Access: R/W SLICE 0 BONUS BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS BIT 0** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

GTICP BONUS2 Reg

GTICPBONUS2 - GTICP BONUS2 Reg

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	24018h

Clock Gating Messages Register

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:8	**Reserved** Access: RO Reserved
	7	**BONUS BIT 7** Access: R/W SLICE 0 BONUS BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS BIT 6** Access: R/W SLICE 0 BONUS BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS BIT 5** Access: R/W SLICE 0 BONUS BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS BIT 4** Access: R/W

GTICPBONUS2 - GTICP BONUS2 Reg

		SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	3	**BONUS BIT 3** Access: R/W SLICE 0 BONUS BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS BIT 2** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS BIT 1** Access: R/W SLICE 0 BONUS BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS BIT 0** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

GT Interrupt DW0

GT_INTR_DW0 - GT Interrupt DW0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	190018h	
Engine bits in this register are set if any of the unmasked bits in the underlying engine 16b interrupt vector is non-zero		
DWord	**Bit**	**Description**
0	31	**CSME** Access: R/W
	30:29	**Reserved** Access: R/W
	28	**GUNIT** Access: R/W
	27:26	**Reserved** Access: R/W
	25	**Reserved** Access: R/W
	24	**Reserved** Access: R/W
	23	**Reserved**
	22:21	**Reserved** Access: R/W
	20	**WDPERF** Access: R/W
	19	**KCR** Access: R/W
	18:17	**RSVD** Access: R/W
	16	**GTPM** Access: R/W
	15	**BCS**

GT_INTR_DW0 - GT Interrupt DW0		
		Access: R/W
	14:1	**Reserved**
	0	**RCS0** Access: R/W

GT Interrupt DW1

GT_INTR_DW1 - GT Interrupt DW1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	19001Ch	
Interrupt bits indicating one of theunderlying engine interrupts is non-zero		
DWord	**Bit**	**Description**
0	31	**VECS0** Access: R/W
	30	**VECS1** Access: R/W
	29	**VECS2** Access: R/W
	28	**VECS3** Access: R/W
	27:8	**Reserved** Access: R/W
	7	**VCS7** Access: R/W
	6	**VCS6** Access: R/W
	5	**VCS5** Access: R/W
	4	**VCS4** Access: R/W
	3	**VCS3** Access: R/W
	2	**VCS2** Access: R/W
	1	**VCS1** Access: R/W
	0	**VCS0** Access: R/W

GT Interrupt Identity

GT_INTR_IDENTITY - GT Interrupt Identity

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	190060h
ShortName:	INTR_IDENTITY_REG0
Address:	190064h
Name:	INTR_IDENTITY_REG1

HW displays the interrupt bits for engine chosen using Selector.
Only unmasked interrupts are displayed. Masked interrupts continue to accumulate behind the mask.
After processing, SW shall write 1's to clear. (Bit 31 must be cleared by SW)
Write to Clear indicates to HW that processing is complete (for displayed interrupts).

DWord	Bit	Description
0	31	**Data Valid** Access: R/W
	30:26	**Reserved**
	25:20	**Engine Instance ID** Engine Instance ID format is defined in structure "Engine ID Definition"
	19	**Reserved**
	18:16	**Engine Class ID** Engine class is defined in structure "Engine ID Definition"
	15:0	**Engine Interrupt** Access: R/W Format is specific to the engine that is sending the interrupt. Format is defined in structure "EngineInterrupt Vector" (where engine is Blitter/G-Unit/GTPM/Render Engine/Video Decoder/VideoEnhancement).

GT Interrupt IIR Selector

GT_INTR_IIR_SELECTOR - GT Interrupt IIR Selector		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	190070h	
ShortName:	IIR_REG0_SELECTOR	
Address:	190074h	
ShortName:	IIR_REG1_SELECTOR	
This is a basic register template		

DWord	Bit	Description
0	31:0	**Engine ID** Access: R/W SW/FW shall program the appropriate Engine ID to view the interrupts from an engine Register: Bit Definition IIR_REG0_SELECTOR: Format: GT Interrupt DW0 IIR_REG1_SELECTOR: Format: GT Interrupt DW1

GTI PGFET control register with lock

GTIPFETCTL - GTI PGFET control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	24008h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock 0 = Bits of MEDIA1 PGFETCTL register are R/W 1 = All bits of MEDIA1 PGFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:26	**Reserved** Access: RO Reserved
	25	**Leave firewall disabled** Access: R/W Lock When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e dont firewall the gated domain, but complete logical flow
	24	**Leave FET On** Access: R/W Lock When This bit is set SPC will not turn off the PFET eventhough it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e dont power off pfet, but complete logical flow
	23	**Power Well Status** Access: RO 0 = Well is powered Down

GTIPFETCTL - GTI PGFET control register with lock

		1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	22	**Powergood timer error** Access: RO 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	21:19	**Delay from enabling secondary PFETs to power good.** Default Value: 110b Access: R/W Lock Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns 3'b010: 160ns 3'b011: 240ns 3'b100: 320ns 3'b101: 480ns 3'b110: 640ns 3'b111: 1280ns
	18:16	**Strobe pulse period** Access: R/W Lock Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk) **Value** / **Name** 110b / **[Default]**
	15:0	**PFET Ladder Step Sequence** Access: R/W Lock PFET Ladder STEP sequence The PFET ladder has 16 steps, each represented by its corresponding bit in pfetlddrstepseq[15:0]. If the bit location is set, it means we must step on that ladder stage before we go to the next stage. The SPC controller will step through all the steps with asserted bits periodically with period equal to strbpulsprd[2:0]

GTIPFETCTL - GTI PGFET control register with lock

Programming Rule: pfetldrstepseq[15] and pfetldrstepseq[0] must be ‘1; A ‘0 setting for these bits is illegal.
15'FFFFh: Ladder step (ladder_sel) goes 0, 1, 2, ?.15.
15'FFF1h: Ladder step goes 0, 4, 5, 6,?15; Steps 1, 2, 3 are skipped.
15'D555h: Ladder step goes 0, 2, 4, 6, 8, 10, 12, 14, 15; Steps 1, 3, 5, 7, 9, 11, 13 are skipped.
15'80001h: Ladder step goes 0, 15; Steps 1, 2, 3, 4, ?14 are skipped.

Value	Name
1111111111111111b	**[Default]**

GTI Power Gate Control Request

GTIPGCTLREQ - GTI Power Gate Control Request		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	24000h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:16	**Message Mask** Access: RO Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:1	**Reserved** Access: RO Reserved
	0	**Power Gate Request** Access: R/W Media1 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

GT Mode Register

GT_MODE - GT Mode Register

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	07008h
Name:	GT Mode Register
ShortName:	GT_MODE

This Register is used to control the 6EU and 12EU configuration for GT. Writing 0x01FF01FF to this register enables the 6EU mode.

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask[15:0] Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15	**EU Local Thread Checking Enable** Access: R/W This field configures the EU local thread checking. If enable the stateless access will be checked against the local thread's scratch space size and start address. 0h – Disable **[Default]** – EU local thread checking is disabled. 1h – Enable – EU local thread checking is enabled.
	14:13	**SFR mode** Access: R/W Format: U2 This field must be zero when not in GT4(SFR) configuration i.e GTB_rendermode fuse set to SFR.
	12:11	**Reserved** Access: R/W

GT_MODE - GT Mode Register

	Format:	PBC

10 HW Binding Table Alignment

Access:	R/W
Format:	Disable

Description
This bit changes the format of the binding table pointer.
When this bit is set, the format of the binding table is SW binding table format whether Binding Table Pool is enabled or disabled.

Value	Name	Description
0h	Legacy **[Default]**	Binding table pointer 15:5 Maps to 15:5 for INTERFACE_DESCRIPTOR DATA. Binding table pointer 15:5 Maps to 15:5 for 3DSTATE_BINDING_TABLE_POINTER_* if Binding Table Pool is disabled. Binding table pointer 15:5 Maps to 16:6 for 3DSTATE_BINDING_TABLE_POINTER_* if Binding Table Pool is enabled.
1h	Enable 512KB Binding Table size	Binding table pointer maps to 18:8 for both 3DSTATE_BINDING_TABLE_POINTER_* and INTERFACE_DESCRIPTOR DATA.

9 Reserved

Access:	R/W
Format:	PBC

8 Reserved

Access:	R/W
Format:	PBC

7 Reserved

Format:	MBZ

6 Reserved

Access:	R/W
Format:	PBC

5:4 Slice2 IZ Hashing: 7 EU subslice encoding

GT_MODE - GT Mode Register

Access:		R/W

These bits control 3-way sub-slice hashing by conveying which sub-slice has 7 EUs.

Value	Name	Description
0h	**[Default]**	All subslices have equal number of EUs.
1h		Subslice 2 has 7 EUs.
2h		Subslice 1 has 7 EU.
3h		Subslice 0 has 7 EUs.

Programming Notes
SW must program these bits based on EU Disable Fuses in Slice 2.

3:2 **Slice1 IZ Hashing: 7 EU subslice encoding**

Access:		R/W

These bits control 3-way sub-slice hashing by conveying which sub-slice has 7 EUs.

Value	Name	Description
0h	**[Default]**	All subslices have equal number of EUs.
1h		Subslice 2 has 7 EUs.
2h		Subslice 1 has 7 EUs.
3h		Subslice 0 has 7 EUs.

Programming Notes
SW must program these bits based on EU Disable Fuses in Slice 1.

1:0 **Slice 0 IZ Hashing: 7 EU subslice encoding**

Access:		R/W

These bits control 3-way sub-slice hashing by conveying which sub-slice has 7 EUs.

Value	Name	Description
0h	**[Default]**	All subslices have equal number of EUs.
1h		Subslice 2 has 7 EUs.
2h		Subslice 1 has 7 EUs.
3h		Subslice 0 has 7 EUs.

Programming Notes
SW must program these bits based on EU Disable Fuses in Slice 0.

GTT Cache Enable

GTT_CACHE_EN - GTT Cache Enable

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	04024h

Enable GTT Cache for respective client(s), A0: Must program/observed this to all 0 due to Big Pages Bug 1898112.
GTT Cache should be enabled only when running legacy contexts. GTT cache is not snooped, and no A/D bit updates are done on the cached PTEs. thus, cached PTEs cannot be used when running advanced contexts.

DWord	Bit	Description
0	31	**GTT Cache Enable for Blitter Engine** Default Value: 0b Access: R/W 1'b1: BLIT Engine (overrides individual enables of the units)
	30	**GTT Cache Enable for VEBX Engine** Default Value: 0b Access: R/W 1'b1: VEBX Engine (overrides individual enables of the units)
	29	**GTT Cache Enable for MFX Engine** Default Value: 0b Access: R/W 1'b1: MFX Engine (overrides individual enables of the units)
	28	**GTT Cache Enable for GFX Engine** Default Value: 0b Access: R/W 1'b1: GFX Engine (overrides individual enables of the units)
	27:15	**Reserved** Default Value: 0000h Access: RO 27-15: Reserved
	14	**GTT Cache Enable for VMC**

GTT_CACHE_EN - GTT Cache Enable

		Default Value: 0b Access: R/W 1'b1: Enable GTT cache for VMCunit
	13	**GTT Cache Enable for VLF** Default Value: 0b Access: R/W 1'b1: Enable GTT cache for VLFunit
	12	**GTT Cache Enable for BLB** Default Value: 0b Access: R/W 1'b1: Enable GTT cache for BLBunit
	11	**GTT Cache Enable for VFW** Default Value: 0b Access: R/W 1'b1: Enable GTT cache for VFWunit
	10	**GTT Cache Enable for VEO** Default Value: 0b Access: R/W 1'b1: Enable GTT cache for VEOunit
	9	**GTT Cache Enable for HIZ** Default Value: 0b Access: R/W 1'b1: Enable GTT cache for HIZunit
	8	**GTT Cache Enable for RCZ** Default Value: 0b Access: R/W 1'b1: Enable GTT Cache for RCZunit
	7	**GTT Cache Enable for RCC** Default Value: 0b Access: R/W 1'b1: enable GTT cache for RCCunit

GTT_CACHE_EN - GTT Cache Enable

	6	**GTT Cache Enable for ISC** Default Value: 0b Access: R/W 1'b1: Enable GTT cache for ISCunit
	5	**GTT Cache Enable for DC** Default Value: 0b Access: R/W 1'b1: enable GTT cache for DCunit
	4	**GTT Cache Enable for MT** Default Value: 0b Access: R/W 1'b1: Enable GTT cache for MTunit
	3	**GTT Cache Enable for SOL** Default Value: 0b Access: R/W 1'b1: Enable GTT cache for SOLunit
	2	**GTT Cache Enable for VF** Default Value: 0b Access: R/W 1'b1: Enable GTT cache for VFunit
	1	**GTT Cache Enable for RS** Default Value: 0b Access: R/W 1'b1: enable GTT cache for RSunit
	0	**GTT Cache Enable for CS** Default Value: 0b Access: R/W 1'b1: enable GTT cache for CSunit

GT Virtual Function Engine Interrupt Enable

GT_ENG_INTR_ENABLE - GT Virtual Function Engine Interrupt Enable	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	191030h
ShortName:	VF1_RENDER_COPY_INTR_ENABLE
Address:	192030h
ShortName:	VF2_RENDER_COPY_INTR_ENABLE
Address:	193030h
ShortName:	VF3_RENDER_COPY_INTR_ENABLE
Address:	194030h
ShortName:	VF4_RENDER_COPY_INTR_ENABLE
Address:	195030h
ShortName:	VF5_RENDER_COPY_INTR_ENABLE
Address:	196030h
ShortName:	VF6_RENDER_COPY_INTR_ENABLE
Address:	197030h
ShortName:	VF7_RENDER_COPY_INTR_ENABLE
Address:	191034h
ShortName:	VF1_VIDEODECODE_VIDEOENHANCE_INTR_ENABLE
Address:	192034h
ShortName:	VF2_VIDEODECODE_VIDEOENHANCE_INTR_ENABLE
Address:	193034h
ShortName:	VF3_VIDEODECODE_VIDEOENHANCE_INTR_ENABLE
Address:	194034h
ShortName:	VF4_VIDEODECODE_VIDEOENHANCE_INTR_ENABLE
Address:	195034h
ShortName:	VF5_VIDEODECODE_VIDEOENHANCE_INTR_ENABLE
Address:	196034h
ShortName:	VF6_VIDEODECODE_VIDEOENHANCE_INTR_ENABLE

GT_ENG_INTR_ENABLE - GT Virtual Function Engine Interrupt Enable

Address: 197034h

ShortName: VF7_VIDEODECODE_VIDEOENHANCE_INTR_ENABLE

DWord	Bit	Description
0	31:16	**Engine1 Interrupt Enable** Access: R/W
	15:0	**Engine0 Interrupt Enable** Access: R/W

GT Virtual Function Engine Interrupt Mask

GT Virtual Function Engine Interrupt Mask	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	191090h
ShortName:	VF1_RCS0_RSVD_INTR_MASK
Address:	192090h
ShortName:	VF2_RCS0_RSVD_INTR_MASK
Address:	193090h
ShortName:	VF3_RCS0_RSVD_INTR_MASK
Address:	194090h
ShortName:	VF4_RCS0_RSVD_INTR_MASK
Address:	195090h
ShortName:	VF5_RCS0_RSVD_INTR_MASK
Address:	196090h
ShortName:	VF6_RCS0_RSVD_INTR_MASK
Address:	197090h
ShortName:	VF7_RCS0_RSVD_INTR_MASK
Address:	1910A0h
ShortName:	VF1_BCS_RSVD_INTR_MASK
Address:	1920A0h
ShortName:	VF2_BCS_RSVD_INTR_MASK
Address:	1930A0h
ShortName:	VF3_BCS_RSVD_INTR_MASK
Address:	1940A0h
ShortName:	VF4_BCS_RSVD_INTR_MASK
Address:	1950A0h
ShortName:	VF5_BCS_RSVD_INTR_MASK
Address:	1960A0h
ShortName:	VF6_BCS_RSVD_INTR_MASK
Address:	1970A0h

GT Virtual Function Engine Interrupt Mask	
ShortName:	VF7_BCS_RSVD_INTR_MASK
Address:	1910A8h
ShortName:	VF1_VCS0_VCS1_INTR_MASK
Address:	1920A8h
ShortName:	VF2_VCS0_VCS1_INTR_MASK
Address:	1930A8h
ShortName:	VF3_VCS0_VCS1_INTR_MASK
Address:	1940A8h
ShortName:	VF4_VCS0_VCS1_INTR_MASK
Address:	1950A8h
ShortName:	VF5_VCS0_VCS1_INTR_MASK
Address:	1960A8h
ShortName:	VF6_VCS0_VCS1_INTR_MASK
Address:	1970A8h
ShortName:	VF7_VCS0_VCS1_INTR_MASK
Address:	1910ACh
ShortName:	VF1_VCS2_VCS3_INTR_MASK
Address:	1920ACh
ShortName:	VF2_VCS2_VCS3_INTR_MASK
Address:	1930ACh
ShortName:	VF3_VCS2_VCS3_INTR_MASK
Address:	1940ACh
ShortName:	VF4_VCS2_VCS3_INTR_MASK
Address:	1950ACh
ShortName:	VF5_VCS2_VCS3_INTR_MASK
Address:	1960ACh
ShortName:	VF6_VCS2_VCS3_INTR_MASK
Address:	1970ACh
ShortName:	VF7_VCS2_VCS3_INTR_MASK
Address:	1910B0h
ShortName:	VF1_VCS4_VCS5_INTR_MASK
Address:	1920B0h
ShortName:	VF2_VCS4_VCS5_INTR_MASK

GT Virtual Function Engine Interrupt Mask	
Address:	1930B0h
ShortName:	VF3_VCS4_VCS5_INTR_MASK
Address:	1940B0h
ShortName:	VF4_VCS4_VCS5_INTR_MASK
Address:	1950B0h
ShortName:	VF5_VCS4_VCS5_INTR_MASK
Address:	1960B0h
ShortName:	VF6_VCS4_VCS5_INTR_MASK
Address:	1970B0h
ShortName:	VF7_VCS4_VCS5_INTR_MASK
Address:	1910B4h
ShortName:	VF1_VCS6_VCS7_INTR_MASK
Address:	1920B4h
ShortName:	VF2_VCS6_VCS7_INTR_MASK
Address:	1930B4h
ShortName:	VF3_VCS6_VCS7_INTR_MASK
Address:	1940B4h
ShortName:	VF4_VCS6_VCS7_INTR_MASK
Address:	1950B4h
ShortName:	VF5_VCS6_VCS7_INTR_MASK
Address:	1960B4h
ShortName:	VF6_VCS6_VCS7_INTR_MASK
Address:	1970B4h
ShortName:	VF7_VCS6_VCS7_INTR_MASK
Address:	1910D0h
ShortName:	VF1_VECS0_VECS1_INTR_MASK
Address:	1920D0h
ShortName:	VF2_VECS0_VECS1_INTR_MASK
Address:	1930D0h
ShortName:	VF3_VECS0_VECS1_INTR_MASK
Address:	1940D0h
ShortName:	VF4_VECS0_VECS1_INTR_MASK
Address:	1950D0h

GT Virtual Function Engine Interrupt Mask

ShortName:	VF5_VECS0_VECS1_INTR_MASK
Address:	1960D0h
ShortName:	VF6_VECS0_VECS1_INTR_MASK
Address:	1970D0h
ShortName:	VF7_VECS0_VECS1_INTR_MASK
Address:	1910D4h
ShortName:	VF1_VECS2_VECS3_INTR_MASK
Address:	1920D4h
ShortName:	VF2_VECS2_VECS3_INTR_MASK
Address:	1930D4h
ShortName:	VF3_VECS2_VECS3_INTR_MASK
Address:	1940D4h
ShortName:	VF4_VECS2_VECS3_INTR_MASK
Address:	1950D4h
ShortName:	VF5_VECS2_VECS3_INTR_MASK
Address:	1960D4h
ShortName:	VF6_VECS2_VECS3_INTR_MASK
Address:	1970D4h
ShortName:	VF7_VECS2_VECS3_INTR_MASK

Register content is saved/restored during RC6.
Bits in the registers described above are in the order: Engine1_Engine0_INTR_MASK.
For e.g: Engine1 houses bits for: RCS0, BCS, VCS0,...
Engine0 houses bits for: RSVD, RSVD, VCS1,...

Register Address	Engine 1	Engine 0	Structure defining bits
190090	RCS0	Reserved	Format: Render Engine Interrupt Vector
1900A0	BCS	Reserved	Format: Blitter Interrupt Vector
1900A8 1900AC 1900B0 1900B4	VCS0 VCS2 VCS4 VCS6	VCS1 VCS3 VCS5 VCS7	Format: VideoDecoder Interrupt Vector
1900D0 1900D4	VECS0 VECS2	VECS1 VECS3	Format: VideEnhancement Interrupt Vector
1900F4	GUnit	CSME	GUnit: G-Unit Interrupt Vector CSME: Manageability Engine Interrupt Vector

DWord	Bit	Description
0	31:16	**Engine1 Interrupt Mask**

GT Virtual Function Engine Interrupt Mask			
		Access:	R/W
	15:0	**Engine0 Interrupt Mask**	
		Access:	R/W

GT Virtual Function IIR Selector

GT_VF_INTR_IIR_SELECTOR - GT Virtual Function IIR Selector	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	191070h
ShortName:	VF1_IIR_REG0_SELECTOR
Address:	191074h
ShortName:	VF1_IIR_REG1_SELECTOR
Address:	192070h
ShortName:	VF2_IIR_REG0_SELECTOR
Address:	192074h
ShortName:	VF2_IIR_REG1_SELECTOR
Address:	193070h
ShortName:	VF3_IIR_REG0_SELECTOR
Address:	193074h
ShortName:	VF3_IIR_REG1_SELECTOR
Address:	194070h
ShortName:	VF4_IIR_REG0_SELECTOR
Address:	194074h
ShortName:	VF4_IIR_REG1_SELECTOR
Address:	195070h
ShortName:	VF5_IIR_REG0_SELECTOR
Address:	195074h
ShortName:	VF5_IIR_REG1_SELECTOR
Address:	196070h
ShortName:	VF6_IIR_REG0_SELECTOR
Address:	196074h
ShortName:	VF6_IIR_REG1_SELECTOR
Address:	197070h
ShortName:	VF7_IIR_REG0_SELECTOR
Address:	197074h

GT_VF_INTR_IIR_SELECTOR - GT Virtual Function IIR Selector

ShortName: VF7_IIR_REG1_SELECTOR

This is a basic register template

DWord	Bit	Description
0	31:0	**Engine ID** Access: R/W SW/FW shall program the appropriate Engine ID to view the interrupts from an engine Register: IIR_REG0_SELECTOR — Bit Definiition: Format: GT Interrupt DW0 Register: IIR_REG1_SELECTOR — Bit Definiition: Format: GT Interrupt DW1

GT Virtual Function Interrupt DW0

GT_VF_INTR_DW0 - GT Virtual Function Interrupt DW0	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	191018h
Name:	VF1_INTR_DW0
Address:	192018h
Name:	VF2_INTR_DW0
Address:	193018h
Name:	VF3_INTR_DW0
Address:	194018h
Name:	VF4_INTR_DW0
Address:	195018h
Name:	VF5_INTR_DW0
Address:	196018h
Name:	VF6_INTR_DW0
Address:	197018h
Name:	VF7_INTR_DW0

Bits set in this register indicate if an engine has an interrupt that requires servicing.

DWord	Bit	Description
0	31	**CSME** Access: R/W
	30:29	**Reserved** Access: R/W
	28	**GUNIT**

GT_VF_INTR_DW0 - GT Virtual Function Interrupt DW0		
		Access: R/W
	27:26	**Reserved** Access: R/W
	25	**Reserved** Access: R/W
	24	**Reserved** Access: R/W
	23	**Reserved**
	22:21	**Reserved** Access: R/W
	20	**WDPERF** Access: R/W
	19	**KCR** Access: R/W
	18:17	**RSVD** Access: R/W
	16	**GTPM** Access: R/W
	15	**BCS** Access: R/W
	14:1	**Reserved**
	0	**RCS0** Access: R/W

GT Virtual Function Interrupt DW1

GT_VF_INTR_DW1 - GT Virtual Function Interrupt DW1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	19101Ch
ShortName:	VF1_INTR_DW1
Address:	19201Ch
ShortName:	VF2_INTR_DW1
Address:	19301Ch
ShortName:	VF3_INTR_DW1
Address:	19401Ch
ShortName:	VF4_INTR_DW1
Address:	19501Ch
ShortName:	VF5_INTR_DW1
Address:	19601Ch
ShortName:	VF6_INTR_DW1
Address:	19701Ch
ShortName:	VF7_INTR_DW1

Interrupt bits indicating one of theunderlying engine interrupts is non-zero

DWord	Bit	Description
0	31	**VECS0** Access: R/W
	30	**VECS1** Access: R/W
	29	**VECS2** Access: R/W
	28	**VECS3** Access: R/W
	27:8	**Reserved** Access: R/W
	7	**VCS7** Access: R/W

GT_VF_INTR_DW1 - GT Virtual Function Interrupt DW1		
	6	**VCS6** Access: R/W
	5	**VCS5** Access: R/W
	4	**VCS4** Access: R/W
	3	**VCS3** Access: R/W
	2	**VCS2** Access: R/W
	1	**VCS1** Access: R/W
	0	**VCS0** Access: R/W

GT Virtual Function Interrupt Identity

GT_VF_INTR_IDENTITY - GT Virtual Function Interrupt Identity	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	191060h
ShortName:	VF1_INTR_IDENTITY_REG0
Address:	191064h
ShortName:	VF1_INTR_IDENTITY_REG1
Address:	192060h
ShortName:	VF2_INTR_IDENTITY_REG0
Address:	192064h
ShortName:	VF2_INTR_IDENTITY_REG1
Address:	193060h
ShortName:	VF3_INTR_IDENTITY_REG0
Address:	193064h
ShortName:	VF3_INTR_IDENTITY_REG1
Address:	194060h
ShortName:	VF4_INTR_IDENTITY_REG0
Address:	194064h
ShortName:	VF4_INTR_IDENTITY_REG1
Address:	195060h
ShortName:	VF5_INTR_IDENTITY_REG0
Address:	195064h

GT_VF_INTR_IDENTITY - GT Virtual Function Interrupt Identity

ShortName:	VF5_INTR_IDENTITY_REG1

Address:	196060h
ShortName:	VF6_INTR_IDENTITY_REG0

Address:	196064h
ShortName:	VF6_INTR_IDENTITY_REG1

Address:	197060h
ShortName:	VF7_INTR_IDENTITY_REG0

Address:	197064h
ShortName:	VF7_INTR_IDENTITY_REG1

HW displays the interrupt bits for engine chosen using Selector.
Only unmasked interrupts are displayed. Masked interrupts continue to accumulate behind the mask.
After processing, SW shall write 1's to clear. (Bit 31 must be cleared by SW)
Write to Clear indicates to HW that processing is complete (for displayed interrupts).

DWord	Bit	Description
0	31	**Data Valid** Access: R/W
	30:26	**Reserved**
	25:20	**Engine Instance ID**
	19	**Reserved**
	18:16	**Engine Class ID**
	15:0	**Engine Interrupt** Access: R/W

Gunit Internal Interrupt Port

G-UNIT_INTERNAL_INTR_PORT - Gunit Internal Interrupt Port

Register Space: MMIO: 0/2/0

Source: BSpec

Size (in bits): 32

Address: 190000h

ShortName: GT_TO_GUNIT_INTR_PORT

Gunit internal interrupt port that is used by engines to communicate interrupts

DWord	Bit	Description
0	31:30	**Reserved** Default Value: 00b Access: RO Reserved
	29:27	**Virtual Function Number** Default Value: 000b Access: R/W VF Number
	26	**Reserved** Default Value: 0b Access: RO Reserved
	25:20	**Engine Instance ID** Default Value: 000000b Access: R/W Engine Instance ID format is defined in structure "Engine ID Definition
	19	**Reserved** Default Value: 0b Access: RO Reserved
	18:16	**Engine Class ID** Default Value: 000b

G-UNIT_INTERNAL_INTR_PORT - Gunit Internal Interrupt Port

		Access: R/W Engine class ID format is defined in structure "Engine ID Definition
	15:0	**Engine Interrupt** Default Value: 0000h Access: R/W Format is specific to the engine that is sending the interrupt. Format is defined in structure EngineInterrupt Vector (where engine isBlitter/G-Unit/GTPM/Render Engine/Video Decoder/VideoEnhancement).

Hardware Status Mask Register

HWSTAM - Hardware Status Mask Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	02098h-0209Bh
Name:	Hardware Status Mask Register
ShortName:	HWSTAM_RCSUNIT
Address:	18098h-1809Bh
Name:	Hardware Status Mask Register
ShortName:	HWSTAM_POCSUNIT
Address:	22098h-2209Bh
Name:	Hardware Status Mask Register
ShortName:	HWSTAM_BCSUNIT
Address:	1C0098h-1C009Bh
Name:	Hardware Status Mask Register
ShortName:	HWSTAM_VCSUNIT0
Address:	1C4098h-1C409Bh
Name:	Hardware Status Mask Register
ShortName:	HWSTAM_VCSUNIT1
Address:	1C8098h-1C809Bh
Name:	Hardware Status Mask Register
ShortName:	HWSTAM_VECSUNIT0
Address:	1D0098h-1D009Bh
Name:	Hardware Status Mask Register
ShortName:	HWSTAM_VCSUNIT2
Address:	1D4098h-1D409Bh
Name:	Hardware Status Mask Register
ShortName:	HWSTAM_VCSUNIT3
Address:	1D8098h-1D809Bh
Name:	Hardware Status Mask Register

HWSTAM - Hardware Status Mask Register

ShortName:	HWSTAM_VECSUNIT1

Address:	1E0098h-1E009Bh
Name:	Hardware Status Mask Register
ShortName:	HWSTAM_VCSUNIT4

Address:	1E4098h-1E409Bh
Name:	Hardware Status Mask Register
ShortName:	HWSTAM_VCSUNIT5

Address:	1E8098h-1E809Bh
Name:	Hardware Status Mask Register
ShortName:	HWSTAM_VECSUNIT2

Address:	1F0098h-1F009Bh
Name:	Hardware Status Mask Register
ShortName:	HWSTAM_VCSUNIT6

Address:	1F4098h-1F409Bh
Name:	Hardware Status Mask Register
ShortName:	HWSTAM_VCSUNIT7

Address:	1F8098h-1F809Bh
Name:	Hardware Status Mask Register
ShortName:	HWSTAM_VECSUNIT3

The HWSTAM register has the same format as the Interrupt Control Registers. The bits in this register are mask bits that prevent the corresponding bits in the Interrupt Status Register from generating a Hardware Status Write (PCI write cycle). Any unmasked interrupt bit (HWSTAM bit set to 0) will allow the Interrupt Status Register to be written to the ISR location (within the memory page specified by the Hardware Status Page Address Register) when that Interrupt Status Register bit changes state.

Programming Notes

- To write the interrupt to the HWSP, the corresponding IMR bit must also be clear (enabled).
- At most 1 bit can be unmasked at any given time.

DWord	Bit	Description
0	31:0	**Hardware Status Mask** Refer to the Interrupt Control Register section for bit definitions. Reserved bits are RO.

Value	Name
00000000h	**[Default]**

Hardware Status Page Address Register

HWS_PGA - Hardware Status Page Address Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	02080h-02083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_RCSUNIT
Address:	18080h-18083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_POCSUNIT
Address:	22080h-22083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_BCSUNIT
Address:	1C0080h-1C0083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_VCSUNIT0
Address:	1C4080h-1C4083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_VCSUNIT1
Address:	1C8080h-1C8083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_VECSUNIT0
Address:	1D0080h-1D0083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_VCSUNIT2
Address:	1D4080h-1D4083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_VCSUNIT3
Address:	1D8080h-1D8083h
Name:	Hardware Status Page Address Register

HWS_PGA - Hardware Status Page Address Register

ShortName:	HWS_PGA_VECSUNIT1
Address:	1E0080h-1E0083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_VCSUNIT4
Address:	1E4080h-1E4083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_VCSUNIT5
Address:	1E8080h-1E8083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_VECSUNIT2
Address:	1F0080h-1F0083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_VCSUNIT6
Address:	1F4080h-1F4083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_VCSUNIT7
Address:	1F8080h-1F8083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_VECSUNIT3

This register is used to program the 4 KB-aligned System Memory address of the Hardware Status Page used to report hardware status into (typically cacheable) System Memory.

DWord	Bit	Description
0	31:12	**Address** Format: GraphicsAddress[31:12]Hardware Status Page Layout This field is used by SW to specify Bits 31:12 of the 4 KB-aligned System Memory address of the 4 KB page known as the Hardware Status Page. The Global GTT is used to map this page from the graphics virtual address to physical address. **Programming Notes** If the Per-Process Virtual Address Space and Exec List Enable bit is set, HW requires that the status page is programmed to allow for the context switch status to be reported.
	11:0	**Reserved** Format: MBZ

HCP Bitstream Output Minimal Size Padding Count Report Register

HCP_MINSIZE_PADDING_COUNT - HCP Bitstream Output Minimal Size Padding Count Report Register

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1E9B4h

This register stores the count in bytes of **minimal size padding insertion. It is primarily provided for statistical data gathering.** This register is part of the context save and restore.

DWord	Bit	Description
0	31:0	**HCP MinSize Padding Count** Format: U32 Total number of bytes in the bitstream output contributing to minimal size padding operation. This count is updated each time when the padding count is incremented.

HCP CABAC Status

HCP_CABAC_STATUS - HCP CABAC Status	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Size (in bits):	32
Trusted Type:	1
Address:	1C2804h
Description:	For VDBox0
Address:	1C6804h
Description:	For VDBox1
Address:	1D2804h
Description:	For VDBox2
Address:	1D6804h
Description:	For VDBox3
Address:	1E2804h
Description:	For VDBox4
Address:	1E6804h
Description:	For VDBox5
Address:	1F2804h
Description:	For VDBox6
Address:	1F6804h
Description:	For VDBox7

HCP CABAC status or VP9 Decode status

DWord	Bit	Description	
0	31:18	**Reserved**	
		Format:	MBZ

HCP_CABAC_STATUS - HCP CABAC Status

	17:12	**Reserved** Exists If: // HEVC decode = 1 Format: MBZ
	17:0	**VP9 SuperBlock Concealment Counter** Exists If: // VP9 decode = 1 Format: U18 Indicate the number of Superblock (SB) concealed by VP9 decoder (not decoded from bitstream due to error)
	11	**Temporal Direction Motion Vector Out-of-Bound Error** Default Value: 0 Access: RO Exists If: // HEVC decode = 1 Format: U1 This flag indicates motion vectors calculated from the Temporal Direct Motion vector is larger than the allowed range for HEVC decode.
	10:7	**Reserved** Exists If: // HEVC decode = 1 Format: MBZ
	6	**Motion Vector Delta SE** Default Value: 0 Access: RO Exists If: // HEVC decode = 1 Format: U1 This flag indicates out-of-bound motion vector delta SEs coded in the bit-stream for HEVC decode.
	5	**Delta QP SE** Default Value: 0 Access: RO Exists If: // HEVC decode = 1 Format: U1 This flag indicates leading-one overflow during CABAC decode of cu_qp_delta_abs for HEVC decode.
	4	**Residual Error**

HCP_CABAC_STATUS - HCP CABAC Status

		Default Value: 0 Access: RO Exists If: // HEVC decode = 1 Format: U1 This flag indicates out-of-bound absolute coefficient level SEs coded in the bit-streamfor HEVC decode.
	3	**Slice and Error** Default Value: 0 Access: RO Exists If: // HEVC decode = 1 Format: U1 This flag indicates a pre-mature end to the slice or an inconsistent end of slice on the last Ctb of a slice for HEVC decode.
	2:1	**Reserved** Exists If: // HEVC decode = 1 Format: MBZ
	0	**HEVC Ctb Concealment Flag** Default Value: 0 Access: RO Exists If: // HEVC decode = 1 Format: U1 Each pulse from this flag indicates one Ctb is concealed by the HEVC decode.

HCP Decode Status

HCP_DEC_STATUS - HCP Decode Status	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1C2800h
Description:	For VDBox0
Address:	1C6800h
Description:	For VDBox1
Address:	1D2800h
Description:	For VDBox2
Address:	1D6800h
Description:	For VDBox3
Address:	1E2800h
Description:	For VDBox4
Address:	1E6800h
Description:	For VDBox5
Address:	1F2800h
Description:	For VDBox6
Address:	1F6800h
Description:	For VDBox7
HCP Decode status.	

DWord	Bit	Description
0	31:18	**Number of Ctbs Concealed**

HCP_DEC_STATUS - HCP Decode Status

		Default Value: 0 Format: U14 This 14-bit field indicates the number of Ctbs concealed during the decoding of the current frame. This field is cleared with the HCP_PIPE_MODE_SELECT command.
	17	**Frame Dec Active** Default Value: 0 Format: U1 This flag indicates that the decoder hardware is actively decoding a picture.
	16	**Indirect Bitstream ObjectAccess Upper Bound Error** Default Value: 0 Format: U1 This flag indicates that the upper bound bit-stream address was reached.
	15:0	**Bit-stream Error Flags** Default Value: 0 Format: U16 This 16-bit field indicates the number of bit stream errors detected for each bit field indicated in the CABAC Status register.

HCP Image Status Control

HCP_IMAGE_STATUS_CONTROL - HCP Image Status Control

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	1E9BCh

DWord	Bit	Description
0	31:24	**Cumulative Frame Delta QP/QIndex** Format: S7 Used for Frame Level Multi-pass Rate Control. HEVC: cu_qp = input (first pass) cu_qp + Cumulative Frame Delta Qp. Pak does clamping to max value based on bitdepth. Bit31 is the sign bit. VP9: cu_qindex = input (first pass) cu_qindex + Cumulative Frame Delta Qindex. Pak does clamping to -127..127 after adding. Bit31 is the sign bit. VDENC: In VDenc mode this value is added even in first pass (always)so the recommendation is to set this value to zero in first pass
	23	**Reserved** Format: MBZ
	22:16	**Cumulative Frame Delta LF** Access: RO Format: S6 Used for Frame Level Multi-pass Rate Control. LF_level = input (first pass) LF_level + Cumulative Frame Delta LF level. Pak does clamping to -63..63 after adding.
	15:12	**Reserved** Format: MBZ
	11:8	**Total Num-Pass** Format: U4
	7:3	**Reserved** Format: MBZ
	2	**Frame Bit Count Violate - under run** Access: RO Format: U1

		This can trigger Frame Level Multi-pass Rate Control. Set to 1 if frame bit count is less than or equal to FrameBitRateMin
	1	**Frame Bit Count Violate - over run** Access: RO Format: U1 This can trigger Frame Level Multi-pass Rate Control. Set to 1 if frame bit count is less than or equal to FrameBitRateMax
	0	**LCU Bit Count Violate- overrun**

HCP Image Status Mask

HCP_IMAGE_STATUS_MASK - HCP Image Status Mask	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1E9B8h

This register stores the image status(flags).

DWord	Bit	Description
0	31:3	**Reserved** Format: MBZ
	2	**FrameBitRateMinReportMask** Same as **FrameSzUnderStatusEn** in HCP_PIC_STATE.
	1	**FrameBitRateMaxReportMask** Same as **FrameSzOverStatusEn** in HCP_PIC_STATE.
	0	**FrameLcuMaxReportMask**

HCP Last Position

HCP_LAST_POSITION - HCP Last Position	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Size (in bits):	32
Trusted Type:	1
Address:	1C2808h
Description:	For VDBox0
Address:	1C6808h
Description:	For VDBox1
Address:	1D2808h
Description:	For VDBox2
Address:	1D6808h
Description:	For VDBox3
Address:	1E2808h
Description:	For VDBox4
Address:	1E6808h
Description:	For VDBox5
Address:	1F2808h
Description:	For VDBox6
Address:	1F6808h
Description:	For VDBox7

Last row and column position of the decoder.

- The HCP Last Position register reports the position of the last Ctb to be decoded by the HCP hardware.
- It can be reset to 0H with the HCP_PIPE_MODE_SELECT command.

DWord	Bit	Description
0	31:25	**Reserved** Format: MBZ
	24:16	**Last Row Position in Ctbs** Default Value: 0 Access: RO Format: U9
	15:9	**Reserved** Format: MBZ
	8:0	**Last Column Position in Ctbs** Default Value: 0 Access: RO Format: U9

HCP Picture Checksum cIdx0

HCP_PICTURE_CHECKSUM_CIDX0 - HCP Picture Checksum cIdx0	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1C281Ch
Description:	For VDBox0
Address:	1C681Ch
Description:	For VDBox1
Address:	1D281Ch
Description:	For VDBox2
Address:	1D681Ch
Description:	For VDBox3
Address:	1E281Ch
Description:	For VDBox4
Address:	1E681Ch
Description:	For VDBox5
Address:	1F281Ch
Description:	For VDBox6
Address:	1F681Ch
Description:	For VDBox7

- The HCP Picture Checksum cIdx0 register reports the 32-bit unsigned picture checksum for cIdx=0 calculated by the HCP hardware and whose algorithm is defined in Annex D of the HEVC standard specification.

HCP_PICTURE_CHECKSUM_CIDX0 - HCP Picture Checksum cIdx0

- This calculated value is updated at the end of the frame.

DWord	Bit	Description
0	31:0	**Picture checksum cIdx0** Default Value: 0 Format: U32

HCP Picture Checksum cIdx1

HCP_PICTURE_CHECKSUM_CIDX1 - HCP Picture Checksum cIdx1	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1C2820h
Description:	For VDBox0
Address:	1C6820h
Description:	For VDBox1
Address:	1D2820h
Description:	For VDBox2
Address:	1D6820h
Description:	For VDBox3
Address:	1E2820h
Description:	For VDBox4
Address:	1E6820h
Description:	For VDBox5
Address:	1F2820h
Description:	For VDBox6
Address:	1F6820h
Description:	For VDBox7

- The HCP Picture Checksum cIdx1 register reports the 32-bit unsigned picture checksum for cIdx=1 calculated by the HCP hardware and whose algorithm is defined in Annex D of the HEVC standard specification.

HCP_PICTURE_CHECKSUM_CIDX1 - HCP Picture Checksum cIdx1

- This calculated value is updated at the end of the frame.

DWord	Bit	Description
0	31:0	**Picture checksum cIdx1** Default Value: 0 Format: U32

HCP Picture Checksum cIdx2

HCP_PICTURE_CHECKSUM_CIDX2 - HCP Picture Checksum cIdx2	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1C2824h
Description:	For VDBox0
Address:	1C6824h
Description:	For VDBox1
Address:	1D2824h
Description:	For VDBox2
Address:	1D6824h
Description:	For VDBox3
Address:	1E2824h
Description:	For VDBox4
Address:	1E6824h
Description:	For VDBox5
Address:	1F2824h
Description:	For VDBox6
Address:	1F6824h
Description:	For VDBox7

- The HCP Picture Checksum cIdx2 register reports the 32-bit unsigned picture checksum for cIdx=2 calculated by the HCP hardware and whose algorithm is defined in Annex D of the HEVC standard specification.

HCP_PICTURE_CHECKSUM_CIDX2 - HCP Picture Checksum cIdx2

- This calculated value is updated at the end of the frame.

DWord	Bit	Description
0	31:0	**Picture checksum cIdx2** Default Value: 0 Format: U32

HCP PMU Status

HCP_PMU_STATUS - HCP PMU Status	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Size (in bits):	32
Trusted Type:	1
Address:	1C280Ch
Description:	For VDBox0
Address:	1C680Ch
Description:	For VDBox1
Address:	1D280Ch
Description:	For VDBox2
Address:	1D680Ch
Description:	For VDBox3
Address:	1E280Ch
Description:	For VDBox4
Address:	1E680Ch
Description:	For VDBox5
Address:	1F280Ch
Description:	For VDBox6
Address:	1F680Ch
Description:	For VDBox7

PMU counter overflow status.

- The HCP PMU Status register reports the overflow status of the HCP PMU Luma Cache Miss Counter, the HCP PMU Chroma cache Miss Counter and the HCP Frame Decode Active Counter.

HCP_PMU_STATUS - HCP PMU Status

- It can be reset to 0H with the HCP_PIPE_MODE_SELECT command.

DWord	Bit	Description
0	31:3	**Reserved** Format: MBZ
	2	**Event Counter Overflow - Frame Decode Active** Access: RO Format: U1 Value 1: Counter overflow Value 0: Non-Active **[Default]**
	1	**Event Counter Overflow - Chroma Cache Miss** Access: RO Format: U1 Value 1: Counter overflow Value 0: Non-Active **[Default]**
	0	**Event Counter Overflow - Luma Cache Miss** Access: RO Format: U1 Value 1: Counter overflow Value 0: Non-Active **[Default]**

HCP Qp Status Count

HCP_QP_STATUS_COUNT - HCP Qp Status Count

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	64
Trusted Type:	1
Address:	1E9C0h

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:0	**Cumulative QP** Format: U24 Cumulative QP for all LCU of a Frame (Can be used for computing average QP).
1	31:15	**Reserved** Format: MBZ
	14:8	**Frame Max CU QP** Format: U7 Valid Range: 0-51 for 8bit, 0-63 for 10bit and 0-75 for 12bit
	7	**Reserved** Format: MBZ
	6:0	**Frame Min CU QP** Format: U7 Valid Range: 0-51 for 8bit and 0-63 for 10bit range 0-75 for 12bit

HCP Reported Bitstream Output CABAC Bin Count Register

HCP_CABAC_BIN_COUNT_FRAME - HCP Reported Bitstream Output CABAC Bin Count Register

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1E9ACh

This register stores the count of number of bins per frame.

DWord	Bit	Description
0	31:0	**HCP Cabac Bin Count** Default Value: 0 Format: U32 Total number of BINs in the bitstream output per frame from the encoder. This count is updated for every time the bin counter is incremented and its reset at image start.

HCP Unit Done

HCP_UNIT_DONE - HCP Unit Done

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1E9D8h

DWord	Bit	Description
0	31:26	**Reserved** Format: MBZ
	25	**Reserved**
	24	**HFC unit Done** Format: U1
	23	**HSF unit Done** Format: U1
	22	**VHLF unit Done** Format: U1
	21	**HHLF unit Done** Format: U1
	20	**HED unit Done** Format: U1
	19	**HVD unit Done** Format: U1
	18	**HPP unit Done**

HCP_UNIT_DONE - HCP Unit Done

		Format: U1
	17	**HMC unit Done** Format: U1
	16	**HIT unit Done** Format: U1
	15	**HPR unit Done** Format: U1
	14	**HFE unit Done** Format: U1
	13	**HBE unit Done** Format: U1
	12	**HMXF unit Done** Format: U1
	11	**HMXB unit Done** Format: U1
	10:9	**Reserved**
	8	**VNC unit done** Format: U1
	7	**VNE unit done** Format: U1
	6	**HSAO Unit Done** Format: U1
	5	**HLC unit done** Format: U1

HCP_UNIT_DONE - HCP Unit Done		
	4	**HLE unit done** Format: U1
	3	**HFQ unit done** Format: U1
	2	**HFT unit done** Format: U1
	1	**HRS unit done** Format: U1
	0	**HPO unit done** Format: U1

HDC Mode Control Register

HDC_MODE - HDC Mode Control Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	WO
Size (in bits):	32
Address:	0E5F4h
Name:	HDC Mode Control Register
ShortName:	HDC_MODE

Mode controls for Shared Function Data Port accesses.

Programming Notes

The register is write-only from LRI command. However, it is readable for context save.

DWord	Bit	Description
0	31:16	**Mask Bits** Default Value: 0000h Format: Mask Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15:12	**Reserved** Format: MBZ
	11	**HDC L1 Cache** Format: Disable When set, disables the HDC private L1 cache. When clear, enables the HDC private L1 cache to keep copies of data read from the L2 cache. The HDC L1 cache does not keep copies of SLM data, URB data, nor data written to the L2 cache. Value: 0h — Name: Enable **[Default]** — Description: Enable use of L1 cache by HDC Value: 1h — Name: Disable — Description: Disable use of L1 cache by HDC **Programming Notes** The HDC L1 cache is a read-only cache and is NOT coherent with L2 cache. Software must manage the coherency by invalidating this L1 cache when L2 data has been written through another HDC to an address being used by this HDC.
	10	**TRTTE**

HDC_MODE - HDC Mode Control Register

	Default Value:	0h
	Format:	Enable

If this control is set, then every data port virtual address is checked against TRVADV to determine if the access will be translated through the Tiled Resources Translation Table (TRTT).

Accesses made during the SIP routine for Context Save/Restore always bypass the TRTT, regardless of the setting of this control.

Programming Notes

To enable Tiled Resources, the context must program both this MMIO to enable TRTT and the corresponding L3 TRTT MMIO registers.

9:6 **TRVADV**

Default Value:	0h
Format:	U4

If TRTTE in this register is enabled and if the Virtual Address [47:44] matches this value, then the virtual address is looked up in the Tiled Resources Translation Table (TRTT).

5 **Force Fault and Stream on Non-Coherent**

Format:	Enable

When set, handle all page faults on non-coherent Data Cache Data Port accesses as Fault-and-Stream (when Fault-and-Stream page fault mode is selected in the context). When this control is not set, page faults on non-coherent, non-TRTT accesses are handled as Fault-and-Halt.

Regardless of the setting of this control, all SIP accesses during Context Save/Restore are forced to be non-coherent, and page faults are handled as Fault-and-Halt.

Value	Name
0h	Force Disabled **[Default]**
1h	Force Enabled

Programming Notes

The disabled setting is the legacy behavior. When page faults occur, GPU performance and preemption latencies will be better with this set.

4 **Force Non-Coherent**

Force all Data Cache Data Port access to be Non-Coherent (virtual addresses) and non-faultable regardless of the surface state or binding table index.

HDC_MODE - HDC Mode Control Register

Value	Name	Description
0h	Force Disabled **[Default]**	Access Coherence Computed Normally
1h	Force Enabled	Accesses are all Non-Coherent and Non-Faultable

Programming Notes
Only change this mode after a pipeflush and cache flush (all threads and their all accesses completed).
Do not use **Force Non-Coherent** with Tiled Resources that return NULL pages. Tile Resources are only supported in with coherent cache mode.

Restriction
The **Force Non-Coherent** setting must follow the setting of the page fault mode: clear when Fault-and-Stream, and optionally set when Fault-and-Halt. But when in Fault-and-Halt mode, only non-coherent accesses are allowed. Coherent accesses require Fault-and-Stream mode be enabled to handle a rare condition with TLB invalidation during page fault handling. Do not set **Force Non-Coherent** when the Gen system is in Fault-and-Stream page fault mode, the results are undefined.

3 **Reserved**

Format:	MBZ

2:0 **Reserved**

Format:	MBZ

HDPORT_STATE

HDPORT_STATE

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	45050h-45053h
Name:	HDPORT State
ShortName:	HDPORT_STATE
Power:	PG0
Reset:	soft

This register is used to indicate when display resources have been pre-empted by hardware for the HDPORT feature. The usage is set during boot, before BIOS or software is active.
The list of DPLLs and DDIs in this register many not accurately reflect the total number of DPLLs and DDIs supported by display engine. HDPORT will not use any DPLL or DDI not listed here. It will not use any DPLL or DDI that is listed here, but not supported by the particular product or SKU.

Programming Notes

HDPORT is a client of the typeC ports and is handled by the typeC flows so display software does not need to consider the HDPORT state.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15	**DPLL2 Used** This field indicates whether DPLL 2 is being used by HDPORT. 0b – Not used 1b – Used
	14	**DPLL3 Used** This field indicates whether DPLL 3 is being used by HDPORT. 0b – Not used 1b – Used
	13	**DPLL1 Used** This field indicates whether DPLL 1 is being used by HDPORT. 0b – Not used

HDPORT_STATE

	1b	Used

12	**DPLL0 Used** This field indicates whether DPLL 0 is being used by HDPORT.

Value	Name
0b	Not used
1b	Used

11	**Spare 11**
10	**Spare 10**
9	**Spare 9**
8	**DDI3 Type** This field indicates whether DDI 3 (DDI D) is being used in HDMI or DP mode by HDPORT.

Value	Name
0b	DP
1b	HDMI

7	**DDI3 Used** This field indicates whether DDI 3 (DDI D) is being used by HDPORT.

Value	Name
0b	Not used
1b	Used

6	**DDI2 Type** This field indicates whether DDI 2 (DDI C) is being used in HDMI or DP mode by HDPORT.

Value	Name
0b	DP
1b	HDMI

5	**DDI2 Used** This field indicates whether DDI 2 (DDI C) is being used by HDPORT.

Value	Name
0b	Not used
1b	Used

4	**DDI1 Type** This field indicates whether DDI 1 (DDI B) is being used by the HDPORT in HDMI or DP mode.

Value	Name
0b	DP
1b	HDMI

HDPORT_STATE

	3	**DDI1 Used** This field indicates whether DDI 1 (DDI B) is being used by HDPORT. **Value** / **Name** 0b – Not used 1b – Used
	2	**DDI0 Type** This field indicates whether DDI 0 (DDI A and DDI E) is being used in HDMI or DP mode by HDPORT. **Value** / **Name** 0b – DP 1b – HDMI
	1	**DDI0 Used** This field indicates whether DDI 0 (DDI A and DDI E) is being used by HDPORT. **Value** / **Name** 0b – Not used 1b – Used
	0	**HDPORT Enabled** This field indicates whether HDPORT is enabled. **Value** / **Name** 0b – Disabled 1b – Enabled

HEVC Local APIC Retry Vector

HEVC_LAPIC_RETRY_VECT - HEVC Local APIC Retry Vector

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Address:	0D594h

Holds the 4 last retry interrupt vectors. The retry vector register holds the last 4 values acknowledged as an interrupt retry. Retries are errors in hardware and are not expected. No interrupt is actually retried, and the interrupt stimulus will be lost if a retry occurs. The system will hang eventually. A 2-bit counter (starting at reset value of 0) is used to point to the slot/byte location from which to load the next retry vector (into the 4 available slots) in sequence. This means if a 5th retry vector shows up, it will be loaded into slot 0 again (as the counter wraps around), over-writing the retry vector which existed there in slot_0.

DWord	Bit	Description
0	31:24	**Vector Slot 3** Format: U8
	23:16	**Vector Slot 2** Format: U8
	15:8	**Vector Slot 1** Format: U8
	7:0	**Vector Slot 0** Format: U8

HOTPLUG_CTL

HOTPLUG_CTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32

Address:	44030h-44033h
Name:	Thunderbolt Hot Plug Control
ShortName:	TBT_HOTPLUG_CTL
Power:	PG0
Reset:	soft

Address:	44038h-4403Bh
Name:	Type-C Hot Plug Control
ShortName:	TC_HOTPLUG_CTL
Power:	PG0
Reset:	soft

DWord	Bit	Description
0	31	**Port8 HPD Enable** Value: 0b = Disable; 1b = Enable
	30	**Reserved**
	29:28	**Port8 HPD Status** Access: R/WC Value: 00b = Hot plug event not detected; 01b = Short pulse detected; 10b = Long pulse detected; 11b = Short and long pulses detected
	27	**Port7 HPD Enable** Value: 0b = Disable; 1b = Enable

HOTPLUG_CTL

	26	**Reserved**
	25:24	**Port7 HPD Status** Access: R/WC **Value** / **Name** 00b: Hot plug event not detected 01b: Short pulse detected 10b: Long pulse detected 11b: Short and long pulses detected
	23	**Port6 HPD Enable** **Value** / **Name** 0b: Disable 1b: Enable
	22	**Reserved**
	21:20	**Port6 HPD Status** Access: R/WC **Value** / **Name** 00b: Hot plug event not detected 01b: Short pulse detected 10b: Long pulse detected 11b: Short and long pulses detected
	19	**Port5 HPD Enable** **Value** / **Name** 0b: Disable 1b: Enable
	18	**Reserved**
	17:16	**Port5 HPD Status** Access: R/WC **Value** / **Name** 00b: Hot plug event not detected 01b: Short pulse detected 10b: Long pulse detected 11b: Short and long pulses detected
	15	**Port4 HPD Enable**

HOTPLUG_CTL

		Value / **Name** 0b – Disable 1b – Enable
	14	**Reserved**
	13:12	**Port4 HPD Status** Access: R/WC 00b – Hot plug event not detected 01b – Short pulse detected 10b – Long pulse detected 11b – Short and long pulses detected
	11	**Port3 HPD Enable** 0b – Disable 1b – Enable
	10	**Reserved**
	9:8	**Port3 HPD Status** Access: R/WC 00b – Hot plug event not detected 01b – Short pulse detected 10b – Long pulse detected 11b – Short and long pulses detected
	7	**Port2 HPD Enable** 0b – Disable 1b – Enable
	6	**Reserved**
	5:4	**Port2 HPD Status** Access: R/WC 00b – Hot plug event not detected 01b – Short pulse detected

HOTPLUG_CTL

		10b: Long pulse detected 11b: Short and long pulses detected
	3	**Port1 HPD Enable** 0b: Disable 1b: Enable
	2	**Reserved**
	1:0	**Port1 HPD Status** Access: R/WC 00b: Hot plug event not detected 01b: Short pulse detected 10b: Long pulse detected 11b: Short and long pulses detected

HS Invocation Counter

HS_INVOCATION_COUNT - HS Invocation Counter

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02300h
Name:	HS Invocation Counter
ShortName:	HS_INVOCATION_COUNT

This register stores the number of patch objects processed by the HS unit. E.g., A PATCHLIST_2 topology with 6 vertices would cause this counter to increment by 3 (there are 3 2-vertex patch objects in that topology).This register is part of the context save and restore.

DWord	Bit	Description
0	63:32	**HS Invocation Count UDW** Number of patch objects processed by the HS stage. Updated only when HS Enable and HS Statistics Enable are set in 3DSTATE_HS
	31:0	**HS Invocation Count LDW** Number of patch objects processed by the HS stage. Updated only when HS Enable and HS Statistics Enable are set in 3DSTATE_HS

IA Vertices Count

IA_VERTICES_COUNT - IA Vertices Count	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02310h-02317h
Name:	IA Vertices Count
ShortName:	IA_VERTICES_COUNT_RCSUNIT_BE_GEOMETRY
Address:	18310h-18317h
Name:	IA Vertices Count
ShortName:	IA_VERTICES_COUNT_POCSUNIT_BE_GEOMETRY
Address:	02310h-02317h
Name:	IA Vertices Count
ShortName:	IA_VERTICES_COUNT_RCSUNIT_BE
Address:	18310h-18317h
Name:	IA Vertices Count
ShortName:	IA_VERTICES_COUNT_POCSUNIT_BE
This register stores the count of vertices processed by VF. This register is part of the context save and restore.	

DWord	Bit	Description
0	63:32	**IA Vertices Count Report UDW** Total number of vertices fetched by the VF stage. This count is updated for every input vertex as long as Statistics Enable is set in VF_STATE (see the Vertex Fetch Chapter in the 3D Volume.)
	31:0	**IA Vertices Count Report LDW** Total number of vertices fetched by the VF stage. This count is updated for every input vertex as long as Statistics Enable is set in VF_STATE (see the Vertex Fetch Chapter in the 3D Volume.)

IDI Cacheable Register

IDICA - IDI Cacheable Register		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	09014h	
Cacheable		
DWord	**Bit**	**Description**
0	31:30	**LLCWBCA** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.
	29:28	**LLCPRFOCA** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.
	27:26	**LLCPCCA** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.
	25:24	**LLCPDCA** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.
	23:22	**CLFCA** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.
	21:20	**POCA** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.
	19:18	**ITMCA** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.
	17:16	**WCILFCA** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.

IDICA - IDI Cacheable Register

15:14	**WILCA** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b. CANNOT BE FLEXED.
13:12	**WCILCA** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b. CANNOT BE FLEXED.
11:10	**WBMCA** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.
9:8	**RFOCA** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.
7:6	**PORINCA** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.
5:4	**PRDCA** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.
3:2	**DRDCA** Access: R/W 00b: Whatever the logic decides (so force feature is disabled) - Default. 01b: Always drive 0. 10b: Always drive 1. 11b: Reserved.
1:0	**CRDCA** Access: R/W 00b: Whatever the logic decides (so force feature is disabled) - Default. 01b: Always drive 0. 10b: Always drive 1. 11b: Reserved.

IDI Control register

IDICR - IDI Control register		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	09008h	

DWord	Bit	Description
0	31	**IDICR Lock bit** Access: R/W Lock
	30:24	**Spares** Access: R/W ECO purposes and Reserved.
	23:22	**Reserved**
	21:16	**IDI HASH MASK** Access: R/W IDI HASH MASK: When a corresponding bit is set, the address line going into HASH for CBO ID calculation is forced to logic0. 21=> Address Bit[11] 20=> Address Bit[10] 19=> Address Bit[9] 18=> Address Bit[8] 17=> Address Bit[7] 16=> Address Bit[6] Note: It is required for GFX Driver to set [19:16] to 1 when eDRAM configuration is enabled.
	15	**GFX Data regulation** Access: R/W Lock This bit is not used by MBGF unit for any functionality, hence made it as spare for ECO purposes.
	14:10	**Reserved**
	9	**MEM Push write enable** Access: R/W Enables MemPushWrite usage on IDI for non-cacheable access that target eDRAM, but not LLC,

IDICR - IDI Control register

		and are not Write Through. This opcode results in a single write response, instead of two, which improves IDI BW when there is concurrent read and write traffic. 0 = no MemPushWr 1 = allow MemPushWr
	8	**I2M Write Enable** Access: R/W Lock
	7	**Snoop Request control** Default Value: 1b Access: R/W 1: Snoop is allowed only when there are no Pending response. 0: Means after every 24 u2c response we allow one snoop request to bypass.
	6:4	**LRUHint** Access: R/W 000b: No LRUHint command sent to uncore. It is reserved. 001b: If LRUHint is asserted from SQ with a read or write command, IDI dispatcher chooses to send an LlcPrefData. 101b: If LRUHint is asserted from SQ with a read or write command, IDI dispatcher chooses to send an LLCPrefCode command on the C2U request channel. 010b: If LRUHint is asserted from SQ with a read/write command, IDI dispatcher chooses to send an LlcPrefRFO command on the C2U request channel. 011b: If LRUHint is asserted from SQ with a read, IDI dispatcher chooses to send LlcPrefData command on the C2U request channel. If LRUHint is asserted from SQ with a write, IDI dispatcher chooses to send LlcPrefRFO command on the C2U request channel. 111b: If LRUHint is asserted from SQ with a read, IDI dispatcher chooses to send LLCPrefCode command on the C2U request channel. If LRUHint is asserted from SQ with a write, IDI dispatcher chooses to send LlcPrefRFO command on the C2U request channel.
	3	**RSVD** Access: RO
	2	**Resport 1 disable** Access: R/W 0: Default value - Both the Response ports on the BGF side are enabled. 1: Rsp Port1 Disable - Response Port1 is disable on the BGF Side.
	1:0	**SQ Grant Counter** Default Value: 01b Access: R/W SQ grant counter - 2-bit grant counter for SQ requests

IDICR - IDI Control register		
		00b: 1 grant. 01b: 2 grants. 10b: 4 grants. 11b: 8 grants.

IDI Look up Register

IDILK2 - IDI Look up Register		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	08514h	
IDI Look up Register		

DWord	Bit	Description
0	31:30	**Spares** Access: R/W Lock
	29	**RSVD** Access: RO
	28	**Colloc bit for Slice 5** Access: R/W Lock Co-located indicates that the Collocated Cbo should receive this request.
	27	**Direction bit for Slice 5** Access: R/W Lock In Half ring uncore topologies this indicates if the 1: Going Up. 0: Going Down.
	26	**Polarity bit for Slice 5** Access: R/W Lock Polarity based on the current core Slice ID and the Destination Cbo ID - should this request be sent to the rings in Even or Odd cycles (this is basically the Distance between the source and destination). 1 - Even. 0 - Odd.
	25	**For Me for Slice 5** Access: R/W Lock The next slice the Target of this request (MyNeigbourId == DestCboId).
	24	**Spares2** Access: R/W Lock Reserved for Slice 4.

IDILK2 - IDI Look up Register

23	**Colloc bit for Slice 4** Access: R/W Lock Co-located indicates that the Collocated Cbo should receive this request.
22	**Direction bit for Slice 4** Access: R/W Lock In Half ring uncore topologies this indicates if the 1: Going Up. 0: Going Down.
21	**Polarity Bit for Slice 4** Access: R/W Lock Polarity based on the current core Slice ID and the Destination Cbo ID - should this request be sent to the rings in Even or Odd cycles (this is basically the Distance between the source and destination). 1 - Even. 0 - Odd.
20	**For Me bit for Slice 4** Access: R/W Lock The next slice the Target of this request (MyNeigbourId == DestCboId).
19	**Spare for Slice 3** Access: R/W Lock Reserved for Slice 3.
18	**Colloc bit for Slice 3** Access: R/W Lock Co-located indicates that the Collocated Cbo should receive this request.
17	**Direction bit for S3** Access: R/W Lock In Half ring uncore topologies this indicates if the 1: Going Up. 0: Going Down.
16	**Polarity Bit for Slice 3** Access: R/W Lock Polarity based on the current core Slice ID and the Destination Cbo ID - should this request be sent to the rings in Even or Odd cycles (this is basically the Distance between the source and

IDILK2 - IDI Look up Register

		destination). 1 - Even. 0 - Odd.
	15	**For Me Bit for Slice 3** Access: R/W Lock The next slice the Target of this request (MyNeigbourId == DestCboId).
	14	**Spare for Slice 2** Access: R/W Lock Reserved for Slice 2.
	13	**Colloc bit for Slice 2** Access: R/W Lock Co-located indicates that the Collocated Cbo should receive this request.
	12	**Direction Bit for Slice 2** Access: R/W Lock In Half ring uncore topologies this indicates if the 1: Going Up. 0: Going Down.
	11	**Polarity Bit for Slice 2** Access: R/W Lock Polarity based on the current core Slice ID and the Destination Cbo ID - should this request be sent to the rings in Even or Odd cycles (this is basically the Distance between the source and destination). 1 - Even. 0 - Odd.
	10	**For me Bit for Slice 2** Access: R/W Lock The next slice the Target of this request (MyNeigbourId == DestCboId).
	9	**Spare for Slice 1** Access: R/W Lock Reserved for Slice 1.
	8	**Colloc Bit for Slice 1** Access: R/W Lock Co-located indicates that the Collocated Cbo should receive this request.

IDILK2 - IDI Look up Register

	7	**Direction Bit for Slice 1** Access: R/W Lock In Half ring uncore topologies this indicates if the 1: Going Up. 0: Going Down.
	6	**Polarity Bit for Slice 1** Access: R/W Lock Polarity based on the current core Slice ID and the Destination Cbo ID - should this request be sent to the rings in Even or Odd cycles (this is basically the Distance between the source and destination). 1 - Even. 0 - Odd.
	5	**For Me Bit for Slice 1** Access: R/W Lock The next slice the Target of this request (MyNeigbourId == DestCboId).
	4	**Spare for Slice 0** Access: R/W Lock Reserved for Slice 0.
	3	**Colloc Bit for Slice 0** Access: R/W Lock Co-located indicates that the Collocated Cbo should receive this request.
	2	**Direction Bit in Slice0** Access: R/W Lock Direction bit for Slice0: In Half ring uncore topologies this indicates if the request needs to be driven on the Up going (1) or the down (0) going ring direction. For Full ring it indicates Clock-wise (1) or counter clock-wise directions. 1: Going Up. 0: Going Down.
	1	**Polarity Bit for Slice 0** Access: R/W Lock Polarity based on the current core Slice ID and the Destination Cbo ID - should this request be sent to the rings in Even or Odd cycles (this is basically the Distance between the source and destination).

		1 - Even. 0 - Odd.
	0	**For Me bit for Slice0** Access: R/W Lock The next slice the Target of this request (MyNeigbourId == DestCboId).

IDILook up Table register

IDILK1 - IDILook up Table register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	08510h

IDI Look Up register I

DWord	Bit	Description
0	31:21	**Spares** Access: R/W Lock
	20:16	**GT Logical ID** Access: R/W Lock Logical ID for GT.
	15:14	**Spares1** Access: R/W Lock Reserved for SA slice.
	13	**Colloc bit for SA Slice** Access: R/W Lock Co-located indicates that the Collocated Cbo should receive this request.
	12	**Direction Bit for SA** Access: R/W Lock In Half ring uncore topologies this indicates if the request needs to be driven on the Up going (1) or the down (0) going ring direction. For Full ring it indicates Clock-wise (1) or counter clock-wise directions. 1: Going Up. 0: Going Down.
	11	**Polarity bit for SA Slice** Access: R/W Lock Polarity based on the current core Slice ID and the Destination Cbo ID - should this request be sent to the rings in Even or Odd cycles (this is basically the Distance between the source and destination). 1 - Even. 0 - Odd.

IDILK1 - IDILook up Table register

	10	**For Me bit for SA** Access: R/W Lock The next slice the Target of this request (MyNeigbourId == DestCboId).
	9:5	**Number of LLC SA Slices** Access: R/W Lock Number of Slice information in the system. This register contains the number of LLC cache slices on the RING. Default: 0000b.
	4:0	**Colocated Slice ID for GT** Access: R/W Lock This register contains the ID of the slice that is servicing GT's co-located cycles. The default is for slice0 to service GT.

IDI MESSAGES

IDIMSG - IDI MESSAGES

Register Space: MMIO: 0/2/0

Source: BSpec

Size (in bits): 32

Address: 08500h

IDI Message Register

DWord	Bit	Description
0	31:16	**Mask Bits** Access: RO Reserved.
	15:13	**RSVD** Access: RO
	12	**MCHECK COMPLETE** Access: R/W iMPH writes to this bit to initiate MCHECK COMPLETE Routine (PPPE flow).
	11	**Spare** Access: R/W Spare Messaging Bit with self-clear.
	10	**MBC Busy ACK** Access: R/W 1 - Busy ACK from GPMunit(Non-Idle). 0 - Non Busy ACK from Gpmunit (Idle). This bit is valid only if 26th Bit is set.
	9	**Reserved**
	8	**Reserved**
	7	**RSVD** Access: RO
	6	**Request to Block IDI** Access: R/W Block and Unblock IDI Request - usually done during CPD Entry and Exits. This is valid only if 22nd bit is set. Block IDI - CPD Entry = 1.

		Unblock IDI CPD Exit = 0.
	5	**RSVD**
	4	**Mbcunit Arbitration request/Release ACK** Access: R/W Arbitration request is sent during the MAE update. The ack is received from GPMunit. This is valid only if 20th bit is set. Arb req ack = 1. Arb release ack = 0.
	3	**IDI Shutdown request** Access: R/W IDI Shutdown Request from GPM to MBCunit. This is valid only if the 19th bit is set.
	2	**IDI Wakeup Message** Access: R/W IDI wakeup message from PM to MBCunit. This is valid only if 18th bit is set.
	1	**Credit Active De-assertreq ACK** Access: R/W Credit Active De-assertreq ACK - GPMunit sends to the MBCunit. This is valid only if the 17th bit of this register is set.
	0	**Boot Context Fetch Request** Access: R/W Do Boot Context Fetch Message - from GPM This is valid only if the 16th bit of this register is set.

IDI Self Snoop Register

IDISLFSNP - IDI Self Snoop Register

Register Space: MMIO: 0/2/0

Source: BSpec

Size (in bits): 32

Address: 09018h

Cacheable

DWord	Bit	Description
0	31:30	**LLCWBSNP** Access: R/W Lock
	29:28	**LLCPRFOSNP** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b. CANNOT BE FLEXED.
	27:26	**LLCPCSNP** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b. CANNOT BE FLEXED.
	25:24	**LLCPDSNP** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b. CANNOT BE FLEXED.
	23:22	**CLFCA** Access: R/W Lock
	21:20	**POCA** Access: R/W Lock
	19:18	**ITMSNP** Access: R/W Lock
	17:16	**WCILFSNP** Access: R/W Lock

IDISLFSNP - IDI Self Snoop Register

	15:14	**WILSNP** Access: R/W Lock
	13:12	**WCILSNP** Access: R/W Lock
	11:10	**WBMSNP** Access: R/W Lock
	9:8	**RFOSNP** Access: R/W Lock
	7:6	**PORINSNP** Access: R/W Lock
	5:4	**PRDSNP** Access: R/W NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b. CANNOT BE FLEXED.
	3:2	**DRDSNP** Access: R/W Lock
	1:0	**CRDSP** Access: R/W 00b: Whatever the logic decides (so force feature is disabled) - Default. 01b: Always drive 0. 10b: Always drive 1. 11b: Reserved.

IDLE Messaging Register for Media5 Engine

MSG_IDLE_VCS5 - IDLE Messaging Register for Media5 Engine

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	080CCh
Name:	IDLE Messaging Register for Media5 Engine
ShortName:	MSG_IDLE_VCS5

Register that is used for VDBOX5 communication with GPM

DWord	Bit	Description
0	31:14	**Reserved** Access: RO
	13	**Media Force Wake Request for Media Slice 3** Access: R/W Media Slice 3 Force Wake Request 1'b0: Media Slice 3 can be powered down (default). 1'b1: Media Slice 3 cannot be powered down.
	12	**Media Force Wake Request for Media Slice 2** Access: R/W Media Slice 2 Force Wake Request 1'b0: Media Slice 2 can be powered down (default). 1'b1: Media Slice 2 cannot be powered down.
	11	**Media Force Wake Request for Media Slice 1** Access: R/W Media Slice 1 Force Wake Request 1'b0: Media Slice 1 can be powered down (default). 1'b1: Media Slice 1 cannot be powered down.
	10	**Render Force Wake Request** Access: R/W Render Force Wake Request 1'b0: Render can be powered down (default). 1'b1: Render cannot be powered down.

MSG_IDLE_VCS5 - IDLE Messaging Register for Media5 Engine

	9	**Media Force Wake Request for Media Slice 0** Access: R/W Media Slice 0 Force Wake Request 1'b0: Media Slice 0 can be powered down (default). 1'b1: Media Slice 0 cannot be powered down.
	8:5	**Reserved** Access: RO
	4	**Preparation for Reset Acknowledgement** Access: R/W Go Acknowledgement. 1'b0: Go=0 Ack (default). 1'b1: Go=1 Ack. Requirement is that when Go=0 request is sent, the agent has to indicate busy before sending the Go=0 acknowledgement. It can only go idle again once Go=1 is received.
	3:0	**Idle Messaging** Access: R/W Idle Messaging. Bit[3]. Secondary Pipe Clock Gating. 1'b0: Secondary pipe clock must be on (default). 1'b1: Secondary pipe clock may be gated. Only used by Render CS for the Fixed Function DOP. Bit[2]. Primary Pipe Clock Gating. 1'b0: Primary pipe clock must be on (default). 1'b1: Primary pipe clock may be gated. Bit[1]. C6 Allowed. 1'b0: Do not allow GT to enter C6 (default). 1'b1: GT may enter C6. Bit[0]. Idle Indication. 1'b0: Pipe is busy (default). 1'b1: Pipe is idle. ** See the Valid Combinations for Idle Messaging Table.

Idle Switch Delay

IDLEDLY - Idle Switch Delay	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0223Ch-0223Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_RCSUNIT
Address:	1823Ch-1823Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_POCSUNIT
Address:	2223Ch-2223Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_BCSUNIT
Address:	1C023Ch-1C023Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_VCSUNIT0
Address:	1C423Ch-1C423Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_VCSUNIT1
Address:	1C823Ch-1C823Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_VECSUNIT0
Address:	1D023Ch-1D023Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_VCSUNIT2
Address:	1D423Ch-1D423Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_VCSUNIT3
Address:	1D823Ch-1D823Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_VECSUNIT1

IDLEDLY - Idle Switch Delay

Address:	1E023Ch-1E023Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_VCSUNIT4

Address:	1E423Ch-1E423Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_VCSUNIT5

Address:	1E823Ch-1E823Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_VECSUNIT2

Address:	1F023Ch-1F023Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_VCSUNIT6

Address:	1F423Ch-1F423Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_VCSUNIT7

Address:	1F823Ch-1F823Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_VECSUNIT3

The IDLEDLY register contains an Idle Delay field which specifies eight times the time stamp base units allowed for command streamer to wait before a context is switched out leading to IDLE state in Execlist mode, i.e following this context switch there is no active element available in HW to execute. Refer “Time Stamp Bases” subsection in Power Management chapter for time stamp base unit granularity. Example: An IDLE Delay count of “2” with Time stamp base unit value of 80ns would mean an idle delay wait of 1280ns (2*8*80). A default value of 0, means that by default, there is no restriction to wait on a context switch leading to IDLE. This register has no significance when Execlists are not enabled.

DWord	Bit	Description
0	31:21	**Reserved** Format: MBZ
	20:0	**IDLE Delay** Format: U21 Eight times the time stamp base units allowed. Refer “Time Stamp Bases” subsection in Power Management chapter for time stamp base unit granularity. Example: An IDLE Delay count of “2” with Time stamp base unit value of 80ns would mean an idle delay wait of 1280ns (2*8*80).

Indirect Context Offset Pointer

INDIRECT_CTX_OFFSET - Indirect Context Offset Pointer	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	021C8h-021CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_RCSUNIT
Address:	181C8h-181CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_POCSUNIT
Address:	221C8h-221CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_BCSUNIT
Address:	1C01C8h-1C01CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_VCSUNIT0
Address:	1C41C8h-1C41CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_VCSUNIT1
Address:	1C81C8h-1C81CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_VECSUNIT0
Address:	1D01C8h-1D01CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_VCSUNIT2
Address:	1D41C8h-1D41CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_VCSUNIT3
Address:	1D81C8h-1D81CBh
Name:	Indirect Context Offset Pointer

INDIRECT_CTX_OFFSET - Indirect Context Offset Pointer

ShortName:	INDIRECT_CTX_OFFSET_VECSUNIT1
Address:	1E01C8h-1E01CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_VCSUNIT4
Address:	1E41C8h-1E41CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_VCSUNIT5
Address:	1E81C8h-1E81CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_VECSUNIT2
Address:	1F01C8h-1F01CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_VCSUNIT6
Address:	1F41C8h-1F41CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_VCSUNIT7
Address:	1F81C8h-1F81CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_VECSUNIT3

This register is used to program the offset where commands RCS_INDIRECT_CTX points to will be executed as part of engine context restore.

Programming Notes	Source
BlitterCS/VideoCS/VideoCS2/VideoEnhancementCS/PositionCS: This register functionality is not supported and must not be programmed for these command streamers.	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS, PositionCS
Offset of Indirect CS context must be always programmed to a command boundary and cacheline boundary inside the context image.	
Indirect context pointer itself is restored during context restore and hence Indirect Context Offset must not be programmed with value less than 0x5.	

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:6	**Offset of Indirect CS Context** Format: U10 This is the cache line offset for the Indirect CS context. This defaults to execute between CS and SVG context. It is not valid to program this to a value that is greater or equal to the starting

INDIRECT_CTX_OFFSET - Indirect Context Offset Pointer

		offset for RS context. If context must be programmed at the end of engine context then program then use BB_PER_CTX_PTR. **Value** / **Name** 1Ah / **[Default]**
	5:0	**Reserved** Format: MBZ

Indirect Context Pointer

INDIRECT_CTX - Indirect Context Pointer	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	021C4h-021C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_RCSUNIT
Address:	181C4h-181C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_POCSUNIT
Address:	221C4h-221C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_BCSUNIT
Address:	1C01C4h-1C01C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_VCSUNIT0
Address:	1C41C4h-1C41C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_VCSUNIT1
Address:	1C81C4h-1C81C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_VECSUNIT0
Address:	1D01C4h-1D01C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_VCSUNIT2
Address:	1D41C4h-1D41C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_VCSUNIT3
Address:	1D81C4h-1D81C7h
Name:	Indirect Context Pointer

INDIRECT_CTX - Indirect Context Pointer

ShortName:	INDIRECT_CTX_VECSUNIT1
Address:	1E01C4h-1E01C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_VCSUNIT4
Address:	1E41C4h-1E41C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_VCSUNIT5
Address:	1E81C4h-1E81C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_VECSUNIT2
Address:	1F01C4h-1F01C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_VCSUNIT6
Address:	1F41C4h-1F41C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_VCSUNIT7
Address:	1F81C4h-1F81C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_VECSUNIT3

This register is used to program the indirect address to be executed between CS and SVG engine context if enabled. This will only get executed due to regular context save/restore and not during power restore. This register is part of the execution list context and will be executed per context. Only supported if execution list is enabled. There is no preempting workloads within this context.

Programming Notes	Source
BlitterCS/VideoCS/VideoCS2/VideoEnhancementCS/PositionCS: This register functionality is not supported and must not be programmed for these command streamers.	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS, PositionCS
The following commands are not supported within Render CS indirect context:	RenderCS

Command Name
MI_WAIT_FOR_EVENT
MI_SEMAPHORE_SIGNAL
MI_ARB_CHECK
MI_RS_CONTROL
MI_REPORT_HEAD
MI_URB_ATOMIC_ALLOC

MI_SUSPEND_FLUSH	
MI_TOPOLOGY_FILTER	
MI_RS_CONTEXT	
MI_SET_CONTEXT	
MI_URB_CLEAR	
MI_SEMAPHORE_WAIT in Memory Poll Mode is not supported. MI_SEMAPHORE_WAIT in register poll mode is supported.	
MI_BATCH_BUFFER_START	
MI_CONDITIONAL_BATCH_BUFFER_END	
MEDIA_OBJECT_WALKER	
GPGPU_WALKER	
3DPRIMITIVE	
3DSTATE_BINDING_TABLE_POINTERS_VS	
3DSTATE_BINDING_TABLE_POINTERS_HS	
3DSTATE_BINDING_TABLE_POINTERS_DS	
3DSTATE_BINDING_TABLE_POINTERS_GS	
3DSTATE_BINDING_TABLE_POINTERS_PS	
3DSTATE_GATHER_CONSTANT_VS	
3DSTATE_GATHER_CONSTANT_GS	
3DSTATE_GATHER_CONSTANT_HS	
3DSTATE_GATHER_CONSTANT_DS	
3DSTATE_GATHER_CONSTANT_PS	
3DSTATE_DX9_CONSTANTF_VS	
3DSTATE_DX9_CONSTANTF_HS	
3DSTATE_DX9_CONSTANTF_DS	
3DSTATE_DX9_CONSTANTF_GS	
3DSTATE_DX9_CONSTANTF_PS	
3DSTATE_DX9_CONSTANTI_VS	
3DSTATE_DX9_CONSTANTI_HS	
3DSTATE_DX9_CONSTANTI_DS	
3DSTATE_DX9_CONSTANTI_GS	
3DSTATE_DX9_CONSTANTI_PS	
3DSTATE_DX9_CONSTANTB_VS	
3DSTATE_DX9_CONSTANTB_HS	
3DSTATE_DX9_CONSTANTB_DS	

INDIRECT_CTX - Indirect Context Pointer

3DSTATE_DX9_CONSTANTB_GS
3DSTATE_DX9_CONSTANTB_PS
3DSTATE_DX9_LOCAL_VALID_VS
3DSTATE_DX9_LOCAL_VALID_DS
3DSTATE_DX9_LOCAL_VALID_HS
3DSTATE_DX9_LOCAL_VALID_GS
3DSTATE_DX9_LOCAL_VALID_PS
3DSTATE_DX9_GENERATE_ACTIVE_VS
3DSTATE_DX9_GENERATE_ACTIVE_HS
3DSTATE_DX9_GENERATE_ACTIVE_DS
3DSTATE_DX9_GENERATE_ACTIVE_GS
3DSTATE_DX9_GENERATE_ACTIVE_PS
3DSTATE_BINDING_TABLE_EDIT_VS
3DSTATE_BINDING_TABLE_EDIT_GS
3DSTATE_BINDING_TABLE_EDIT_HS
3DSTATE_BINDING_TABLE_EDIT_DS
3DSTATE_BINDING_TABLE_EDIT_PS
3DSTATE_CONSTANT_VS
3DSTATE_CONSTANT_GS
3DSTATE_CONSTANT_PS
3DSTATE_CONSTANT_HS
3DSTATE_CONSTANT_DS
MI_BATCH_BUFFER_END

DWord	Bit	Description
0	31:6	**Indirect CS Context Address** Format: GraphicsAddress[31:6] Pointer to the Context in memory to be executed as a batch.
	5:0	**Size of Indirect CS Context** Format: U6 This is the size of the Indirect Context for CS. This size supports up to 63 cache lines worth of commands where a cache line is 64B. If programmed to zero then the indirect fetch of the CS context is disabled. Value: [0,63] Name:

Instruction Parser Mode Register

INSTPM - Instruction Parser Mode Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	020C0h-020C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_RCSUNIT
Address:	180C0h-180C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_POCSUNIT
Address:	220C0h-220C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_BCSUNIT
Address:	1C00C0h-1C00C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_VCSUNIT0
Address:	1C40C0h-1C40C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_VCSUNIT1
Address:	1C80C0h-1C80C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_VECSUNIT0
Address:	1D00C0h-1D00C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_VCSUNIT2
Address:	1D40C0h-1D40C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_VCSUNIT3
Address:	1D80C0h-1D80C3h
Name:	Instruction Parser Mode Register

INSTPM - Instruction Parser Mode Register

ShortName:	INSTPM_VECSUNIT1
Address:	1E00C0h-1E00C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_VCSUNIT4
Address:	1E40C0h-1E40C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_VCSUNIT5
Address:	1E80C0h-1E80C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_VECSUNIT2
Address:	1F00C0h-1F00C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_VCSUNIT6
Address:	1F40C0h-1F40C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_VCSUNIT7
Address:	1F80C0h-1F80C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_VECSUNIT3

The INSTPM register is used to control the operation of the Instruction Parser. Certain classes of instructions can be disabled (ignored) - often useful for detecting performance bottlenecks. Also, Synchronizing Flush operations can be initiated - useful for ensuring the completion (vs. only parsing) of rendering instructions.

Programming Notes

- If an instruction type is disabled, the parser will read those instructions but not process them.
- Error checking will be performed even if the instruction is ignored.
- All Reserved bits are implemented.
- This Register is saved and restored as part of Context.

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask Masks: These bits serve as write enables for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.

INSTPM - Instruction Parser Mode Register

15 **Register Poll Mode Semaphore Wait Event IDLE message Disable**

This bit controls the DOP CG behavior of CS while waiting for pending semaphore wait for event to be satisfied in register poll mode of operation.

Value	Name	Description
0	**[Default]**	When Rest, CS trigger DOP CG on an unsuccessful semaphore wait in register poll mode of operation.
1		When Set, CS doesn't trigger DOP CG on an unsuccessful semaphore wait in register poll mode of operation.

14 **Reserved**

Source:	VideoCS, VideoCS2, VideoEnhancementCS
Format:	MBZ

14 **Ignore "Posh Start" and "Posh Enable" fields in Batch Start command**

Source:	RenderCS, PositionCS

This bit controls the execution of ring buffers and batch buffer by PositionCS and RenderCS.

Value	Name	Description
0	**[Default]**	PositonCS and RenderCS consider the "Posh Start" and "Posh Enable" fields programmed in the MI_BATCH_BUFFER_START command and execute accordingly. PositionCS parses (doesn't execute) the commands programmed in the ring buffer.
1		PositonCS and RenderCS ignores the "Posh Start" and "Posh Enable" fields programmed in the MI_BATCH_BUFFER_START command. PositionCS executes all the commands programmed in the ring buffer and the batch buffers.

13 **Enable Semaphore Register Poll Mask**

This bit enables masking of the register data red prior to semaphore comparison on a register poll mode.

Value	Name	Description
1		In register poll mode of operation "Semaphore Address Upper Dword" will be used as mask and applied to the data red form the register prior to comparison. Mask Bit Set to '0' indicate the corresponding bit red from the register is considered as it is unmodified for comparison. Mask Bit Set to '1' indicate the corresponding bit red from the register is forced to '0' for comparison.
0	**[Default]**	Regular comparison withno mask applied.

INSTPM - Instruction Parser Mode Register

	12	**Reserved** Format: MBZ
	11	**CLFLUSH Toggle** Source: RenderCS, PositionCS Access: RO Format: U1 This bit changes polarity each time the MI_CLFLUSH command completes. This bit is Read Only.
	11	**Reserved** Source: BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS Format: MBZ
	10	**Reserved** Format: MBZ
	9:0	**Reserved** Format: MBZ

I/O Base Address

IOBAR_0_2_0_PCI - I/O Base Address

Register Space:	PCI: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00020h

This register provides the Base offset of the I/O registers within Device #2. Bits 15:6 are programmable allowing the I/O Base to be located anywhere in 16bit I/O Address Space. Bits 2:1 are fixed and return zero; bit 0 is hardwired to a one indicating that 8 bytes of I/O space are decoded. Access to the 8Bs of IO space is allowed in PM state D0 when IO Enable (PCICMD bit 0) set. Access is disallowed in PM states D1-D3 or if IO Enable is clear or if Device #2 is turned off or if Internal graphics is disabled through the fuse or fuse override mechanisms. Note that access to this IO BAR is independent of VGA functionality within Device #2. If accesses to this IO bar is allowed then all 8, 16 or 32 bit IO cycles from IA cores that falls within the 8B are claimed.

DWord	Bit	Description
0	31:16	**Reserved** Default Value: 0000000b Access: RO Reserved
	15:6	**IO Base Address** Default Value: 0000000000b Access: R/W Set by the OS, these bits correspond to address signals [15:6].
	5:3	**Reserved** Default Value: 0000000b Access: RO Reserved
	2:1	**Memory Type** Default Value: 00b Access: RO Hardwired to 0s to indicate 32-bit address.
	0	**Memory/IO Space** Default Value: 1b Access: RO

IOBAR_0_2_0_PCI - I/O Base Address		
		Hardwired to "1" to indicate IO space.

IOMMU_DEFEATURE_MISCDIS3

IOMMU_DEFEATURE_MISCDIS3 - IOMMU_DEFEATURE_MISCDIS3

Register Space: MMIO: 0/2/0

Source: BSpec

Size (in bits): 32

Address: 101064h

Register to disable certain functionality of IOMMU

DWord	Bit	Description
0	31:2	**MISC2SPARE** Default Value: 00000000000000000000000000000000b Access: R/W Spare bits
	1	**MAJOR_VERSION** Default Value: 0b Access: R/W Disables the IOMMU's major version indication
	0	**MINOR_VERSION** Default Value: 0b Access: R/W Disables the IOMMU's minor version indication

KVMR_SPR_COLOR_CTL

KVMR_SPR_COLOR_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	45030h-45033h
Name:	Kvmr Sprite Color Control
ShortName:	KVMR_SPR_COLOR_CTL
Power:	PG0
Reset:	soft

DWord	Bit	Description
0	31	**Enable Color Processing** This field enables the sRGB de-gamma, color space conversion to BT2020 and tone mapping with the programmed tone mapping factor. Value: 1b — Name: Enable Value: 0b — Name: Disable
	30:10	**Reserved** Format: MBZ
	9:0	**Tone Mapping Factor** This field specifies the tone mapping factor. Each color component gets corrected with this programmed 10 bit fractional value.

L3 Control Register

L3CNTLREG - L3 Control Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	07034h
Name:	L3 Control Register
ShortName:	L3CNTLREG

Programming Notes

The L3 allocation programming should assign all ways of the cache with no left over ways. Refer to L3 section for the recommended settings.

Any L3 configuration change that reduces the data cache allocation when strong IA coherency is used requires the full flush of L3 prior to the programming update.
An explicit or implicit flush of L3 (DC Flush) through the command streamer doesn't result in flushing/invalidating the IA Coherent lines from L3. However this can be achieved by setting the "**Pipe line flush Coherent lines**" control bit in the "L3SQCREG4" register.

DWord	Bit	Description
0	31:25	**All L3 Client Pool** Access: R/W Number of ways allocated for the all client pool. This is a combined pool for all clients. [0h,60h] — **Please refer to L3 Section with Allocation and Programming for recommended settings.** 60h — **[Default]** — Increments of 2KB Per bank if Bitfield "Use full ways" (bit 10 of this register) is clear. Else increments of 4KB per bank. (L3 size needs to be calculated based on bank count per SKU). Please refer to L3 Section with Allocation and Programming for recommended settings. **Programming Notes** When this field is non-zero, **DC Way Assignment** and **Read Only Client Pool** should be 0KB.
	24:18	**DC Way Assignment** Access: R/W Number of ways allocated for DC. Note this allocation is only for DC data types.

L3CNTLREG - L3 Control Register

Value	Name	Description
[0h,60h]		**Please refer to L3 Section with Allocation and Programming for recommended settings.**
00h	**[Default]**	Increments of 2KB Per bank if Bitfield "Use full ways" (bit 10 of this register) is clear. Else increments of 4KB per bank. (L3 size needs to be calculated based on bank count per SKU)

Programming Notes
Note: This field must be 0KB if All L3 Client Pool is non-zero. **Please refer to L3 HAS for valid programming values**

17:11 **Read Only Client Pool**

Access:	R/W

Number of ways allocated for Read Only L3 clients. This is a combined pool for all Read Only clients.

Value	Name	Description
[0h,60h]		**Please refer to L3 HAS for valid programming values.**
00h	**[Default]**	Increments of 2KB Per bank if Bitfield "Use full ways" (bit 10 of this register) is clear. Else increments of 4KB per bank. (L3 size needs to be calculated based on bank count per SKU)

Programming Notes
Note: This field must be 0KB if All L3 Client Pool is non-zero. **Please refer to L3 HAS for valid programming values**

10 **Use full ways**

Access:	R/W

This bit controls the granularity of programming for all the allocation fields in this register. If this bit is cleared, then the programming is in the legacy mode where the granularity of programming is 2KB per bank. When this bit is set, the granularity of programming increases to 4KB per bank. For non-legacy allocation sizes that require more than 254K per bank for a given segment, this bit must be set.

Value	Name	Description
0	**[Default]**	The number of ways programmed in the client pool fields of this register will be used after dividing the number programmed by 2. Odd values not allowed. This setting is not allowed when enabling the PTBR feature that caches the color and Z clients in the L3 cache.
1		The number of ways programmed in the client pool fields of this register will be used as is. Odd values allowed.

9 **Error Detection Behavior Control**

L3CNTLREG - L3 Control Register

	Access:	R/W
	Format:	Enable

The L3 error detection can be enabled to hang the GPU on a non-recoverable error due to SER type events. Such option will be used when corresponding context has data consistency requirements. Once error detection is enabled, s/w has to initialize URB or SLM to all 0's (based on usage model) prior to execution of the workload. Initialization is required to clean up the error detection logic and syndrome tracking.

Value	Name	Description
0h	**[Default]**	RTL enforces a hang on parity errors or double bit error
1h		RTL does not hang on parity errors or double bit error

8 **GPGPU L3 Credit Mode Enable**

	Access:	R/W
	Format:	Enable

This bit is required to be enabled under GPGPU workloads to provide the MAX latency coverage from L3 cache. It will override the registers 0xB100[18:14] and 0xB100[23:19], to 0 and the maximum value respectively.

7:1 **URB Allocation**

	Access:	R/W

Number of ways allocated for URB usage

Value	Name	Description
[0h,7Fh]		**Please refer to L3 HAS for valid programming values. At least one way needs to be programmed in L3 space.**
20h	**[Default]**	Increments of 2KB per bank if Bitfield "Use full ways" (bit 10 of this register) is clear. Else increments of 4KB per bank. (L3 size needs to be calculated based on bank count per SKU)

Programming Notes
Please refer to L3 HAS for valid programming values. At least one way needs to be programmed in L3 space.

0 **Reserved**

	Format:	PBC

L3 Control Register1

L3CNTLREG1 - L3 Control Register1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0B10Ch

DWord	Bit	Description
0	31:28	**Data Fifo Depth Control** Default Value: 1000b Access: R/W Data Fifo Depth Control (TS mode). Value cannot be zero for normal operation. lbcf_csr_lc_datafifo_depth[3:0].
	27:24	**Data Clock off time** Access: R/W **Description** Data Clock off time (DATACLKOFF): Data Clock off time – LTCD_DATAunit is gated after the programmed number of clocks are observed after the pipeline has become idle. lbcf_csr_lc_dataclkoff_time[3:0]. Min value to be 4'h0100. It should be between 4'h4 : 4'hf. **Value** / **Name**: 0001b / **[Default]**
	23:20	**TAG CLK OFF TIME** Access: R/W **Description** TAG CLK OFF TIME (TAGCLKOFF): TAG Clock Off time. This is the time, which Clock gating Logic checks before it turns off the clock. lbcf_csr_lc_tagclkoff_time[3:0].

L3CNTLREG1 - L3 Control Register1

		Values can be between 4'h1 - 4'hf. **Value**: 0001b — **Name**: **[Default]**
	19	**L3 Aging Disable Bit** Default Value: 0b Access: R/W L3 Aging Disable Bit (L3AGDIS): Aging Disable. lbcf_csr_lc_agingdis.
	18:15	**Fill aging** Default Value: 1111b Access: R/W Fill aging (L3AGF): Aging Counter for Fill. lbcf_csr_lc_fill_aging_cnt[3:0]. If bit B10C.19 is 0 then this register value has to be nonzero.
	14:11	**Aging Counter for Read 1 Port** Default Value: 1111b Access: R/W Aging Counter for Read 1 Port (L3AGR1): Aging Counter for Read 1 Port. lbcf_csr_lc_r1_aging_cnt[3:0]. If bit B10C.19 is 0 then this register value has to be nonzero.
	10:7	**L3 Aging Counter for R0** Default Value: 1111b Access: R/W L3 Aging Counter for R0 (L3AGR0): Aging Counter for R0 Port. lbcf_csr_lc_r0_aging_cnt[3:0]. If bit B10C.19 is 0 then this register value has to be nonzero.
	6:4	**L3 Aging Counter for SNOOP**

		Default Value: 111b Access: R/W L3 Aging Counter for SNOOP: Aging Counter for Snoop Port. lbcf_csr_lc_snp_aging_cnt[3:0].
	3:0	**Fill aging for port1** Default Value: 1111b Access: R/W Fill aging (L3AGF): Aging Counter for Fill port 1. lbcf_csr_lc_fill1_aging_cnt[3:0]. If bit B10C.19 is 0 then this register value has to be nonzero.

L3 SQC registers 1

L3SQCREG1 - L3 SQC registers 1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0B100h

Programming Notes

Workaround Credits between LNI/LSQC are not updated in case of Render DOP gating condition)- DOP Render clock ungating needs to happen before L3SQCREG1 is programmed and it should happen through the driver.

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Reserved.
	23:17	**L3SQ General Priority Credit Initialization** Access: R/W Number of general priority credits that SQ presents to L3 Arbiter blocks. This inherently also determines the depth of the SQ; reduce the number of credits and SQ uses fewer slots. The number of general priority credits is always greater than that of high priority credits. Total number of general and high priority credits should be less than or equal to 64. This implies that the sum of the programmed general priority and high priority values should be less than or equal to 32 The number of general priority credits is equal to double the value written in this register. Example: [00001b = 2 credits; 00100b = 8 credits] Valid values for general priority credits can range from: [1 to 32]. Other values are reserved Signal name: lbcf_csr_lsqc_gen_credit_init **Value** / **Name**: 0010100b / **[Default]** **Programming Notes**: The number of general priority credits is always greater than that of high priority credits. Total number of general and high priority credits should be less than or equal to 64. This implies that the sum of the programmed general priority and high priority values should be less than or equal to 32 lbcf_csr_lsqc_gen_credit_init + lbcf_csr_lsqc_hp_credit_init less than or equal to 32
	16:11	**L3SQ High Priority Credit Initialization**

L3SQCREG1 - L3 SQC registers 1

	Access:	R/W

Number of high priority credits that SQ presents to L3 Arbiter blocks. This inherently also determines the depth of the SQ; reduce the number of credits and SQ uses fewer slots.
The number of high priority credits is always lesser than that of general priority credits. Total number of general and high priority credits should be less than or equal to 64. This implies that the sum of the programmed general priority and high priority values should be less than or equal to 32
The number of high priority credits is equal to double the value written in this register. Example: [00001b = 2 credits; 00100b = 8 credits]
Valid values for high priority credits can range from: [0 to 15]. Other values are reserved
Signal name: lbcf_csr_lsqc_gen_credit_init

Value	Name
000100b	**[Default]**

Programming Notes
The number of high priority credits is always lesser than that of general priority credits. Total number of general and high priority credits should be less than or equal to 64. This implies that the sum of the programmed general priority and high priority values should be less than or equal to 32 lbcf_csr_lsqc_gen_credit_init + lbcf_csr_lsqc_hp_credit_init less than or equal to 32

10 **Reserved**

Access:	RO

Reserved.

9 **L3SQ Read Once Enable for Sampler Client**

Access:	R/W

L3SQ Read Once Enable for Sampler Client (SQROE):
Enables Read Once indications to L3 Cache from SQ. Once enabled, any reads from Sampler client (MT) are sent as Read Once.
0 = (default) Reads from Sampler clients issue Read to L3 Cache.
1 = Reads from Sampler clients issue Read Once to L3 Cache.
lbcf_csr_sampler_readonce_en.

8:6 **Reserved**

Access:	RO

Reserved.

5:3 **L3SQ Outstanding L3 Fills**

Access:	R/W

		L3SQ Outstanding L3 Fills (SQOUTSL3F): Identifies the number of L3 Fills that can be outstanding before SQ throttles the fill requests to L3 Cache. This is not an exact limit, but instead it is used as a threshold to throttling. Once the fill count is greater than or equal to the threshold, then no fills are issued until the fill responses are received to bring the outstanding count back below the threshold. 000b = (default) No limit. 001b = 1 fill. 010b = 2 fills. 011b = 4 fills. 100b = 8 fills. 101b = 16 fills. 11Xb = Reserved. Ibcf_csr_lsqc_outs_fill[2:0].
	2:0	**L3SQ Outstanding L3 Lookups** Access: R/W L3SQ Outstanding L3 Lookups (SQOUTSL3L): Identifies the number of L3 lookups that can be outstanding before SQ throttles the lookup requests to L3 Cache. This is not an exact limit, but instead it is used as a threshold to throttling. once the lookup count is greater than or equal to the threshold, then no lookups are issued until the lookup responses are received to bring the outstanding count back below the threshold. 000b = (default) No limit. 001b = 1 lookup. 010b = 2 lookups. 011b = 4 lookups. 100b = 8 lookups. 101b = 16 lookups. 11Xb = Reserved. Ibcf_csr_lsqc_outs_lookup[2:0].

LINKM

LINKM	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	60040h-60043h
Name:	Transcoder A Link M Value 1
ShortName:	TRANS_LINKM1_A
Power:	PG2
Reset:	soft
Address:	61040h-61043h
Name:	Transcoder B Link M Value 1
ShortName:	TRANS_LINKM1_B
Power:	PG2
Reset:	soft
Address:	62040h-62043h
Name:	Transcoder C Link M Value 1
ShortName:	TRANS_LINKM1_C
Power:	PG2
Reset:	soft
Address:	6F040h-6F043h
Name:	Transcoder EDP Link M Value 1
ShortName:	TRANS_LINKM1_EDP
Power:	PG1
Reset:	soft

This register is double buffered to update on the next MSA after LINKN is written.

DWord	Bit	Description	
0	31:24	**Reserved**	
		Format:	MBZ

LINKM		
	23:0	**Link M value** This field is the link M value for external transmission in the Main Stream Attributes.

LINKN

LINKN	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	60044h-60047h
Name:	Transcoder A Link N Value 1
ShortName:	TRANS_LINKN1_A
Power:	PG2
Reset:	soft
Address:	61044h-61047h
Name:	Transcoder B Link N Value 1
ShortName:	TRANS_LINKN1_B
Power:	PG2
Reset:	soft
Address:	62044h-62047h
Name:	Transcoder C Link N Value 1
ShortName:	TRANS_LINKN1_C
Power:	PG2
Reset:	soft
Address:	6F044h-6F047h
Name:	Transcoder EDP Link N Value 1
ShortName:	TRANS_LINKN1_EDP
Power:	PG1
Reset:	soft

This register is double buffered to update on the next MSA after written. **Writes to this register arm M/N registers for this transcoder.**

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:0	**Link N value** This field is the link N value for external transmission in the Main Stream Attributes and VB-ID.

Load Indirect Base Vertex

3DPRIM_BASE_VERTEX - Load Indirect Base Vertex	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	32
Address:	02440h-02443h
Name:	Load Indirect Base Vertex
ShortName:	3DPRIM_BASE_VERTEX_RCSUNIT_BE_GEOMETRY
Address:	18440h-18443h
Name:	Load Indirect Base Vertex
ShortName:	3DPRIM_BASE_VERTEX_POCSUNIT_BE_GEOMETRY
Address:	02440h-02443h
Name:	Load Indirect Base Vertex
ShortName:	3DPRIM_BASE_VERTEX_RCSUNIT_BE
Address:	18440h-18443h
Name:	Load Indirect Base Vertex
ShortName:	3DPRIM_BASE_VERTEX_POCSUNIT_BE

DWord	Bit	Description
0	31:0	**Base Vertex** Format: S31 This register is used to store the Base Vertex of the 3D_PRIMITIVE command when Load Indirect Enable is set.

Load Indirect Extended Parameter 0

3DPRIM_XP0 - Load Indirect Extended Parameter 0	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	32
Address:	02690h-02693h
Name:	Load Indirect Extended Parameter 0
ShortName:	3DPRIM_XP0_RCSUNIT_BE_GEOMETRY
Address:	18690h-18693h
Name:	Load Indirect Extended Parameter 0
ShortName:	3DPRIM_XP0_POCSUNIT_BE_GEOMETRY
Address:	02690h-02693h
Name:	Load Indirect Extended Parameter 0
ShortName:	3DPRIM_XP0_RCSUNIT_BE
Address:	18690h-18693h
Name:	Load Indirect Extended Parameter 0
ShortName:	3DPRIM_XP0_POCSUNIT_BE

DWord	Bit	Description
0	31:0	**Extended Parameter 0** Format: U32 This register is used to store the Extended Parameter 0 of the 3D_PRIMITIVE command when Load Indirect Enable is set.

Load Indirect Extended Parameter 1

3DPRIM_XP1 - Load Indirect Extended Parameter 1	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	32
Address:	02694h-02697h
Name:	Load Indirect Extended Parameter 1
ShortName:	3DPRIM_XP1_RCSUNIT_BE_GEOMETRY
Address:	18694h-18697h
Name:	Load Indirect Extended Parameter 1
ShortName:	3DPRIM_XP1_POCSUNIT_BE_GEOMETRY
Address:	02694h-02697h
Name:	Load Indirect Extended Parameter 1
ShortName:	3DPRIM_XP1_RCSUNIT_BE
Address:	18694h-18697h
Name:	Load Indirect Extended Parameter 1
ShortName:	3DPRIM_XP1_POCSUNIT_BE

DWord	Bit	Description
0	31:0	**Extended Parameter 1** Format: U32 This register is used to store the Extended Parameter 1 of the 3D_PRIMITIVE command when Load Indirect Enable is set.

Load Indirect Extended Parameter 2

3DPRIM_XP2 - Load Indirect Extended Parameter 2	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	32
Address:	02698h-0269Bh
Name:	Load Indirect Extended Parameter 2
ShortName:	3DPRIM_XP2_RCSUNIT_BE_GEOMETRY
Address:	18698h-1869Bh
Name:	Load Indirect Extended Parameter 2
ShortName:	3DPRIM_XP2_POCSUNIT_BE_GEOMETRY
Address:	02698h-0269Bh
Name:	Load Indirect Extended Parameter 2
ShortName:	3DPRIM_XP2_RCSUNIT_BE
Address:	18698h-1869Bh
Name:	Load Indirect Extended Parameter 2
ShortName:	3DPRIM_XP2_POCSUNIT_BE

DWord	Bit	Description
0	31:0	**Extended Parameter 2** Format: U32 This register is used to store the Extended Parameter 2 of the 3D_PRIMITIVE command when Load Indirect Enable is set.

Load Indirect Instance Count

3DPRIM_INSTANCE_COUNT - Load Indirect Instance Count	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	32
Address:	02438h-0243Bh
Name:	Load Indirect Instance Count
ShortName:	3DPRIM_INSTANCE_COUNT_RCSUNIT_BE_GEOMETRY
Address:	18438h-1843Bh
Name:	Load Indirect Instance Count
ShortName:	3DPRIM_INSTANCE_COUNT_POCSUNIT_BE_GEOMETRY
Address:	02438h-0243Bh
Name:	Load Indirect Instance Count
ShortName:	3DPRIM_INSTANCE_COUNT_RCSUNIT_BE
Address:	18438h-1843Bh
Name:	Load Indirect Instance Count
ShortName:	3DPRIM_INSTANCE_COUNT_POCSUNIT_BE

DWord	Bit	Description
0	31:0	**Instance Count** This register is used to store the Instance Count of the 3D_PRIMITIVE command when Load Indirect Enable is set.

Load Indirect Start Instance

3DPRIM_START_INSTANCE - Load Indirect Start Instance	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	32
Address:	0243Ch-0243Fh
Name:	Load Indirect Start Instance
ShortName:	3DPRIM_START_INSTANCE_RCSUNIT_BE_GEOMETRY
Address:	1843Ch-1843Fh
Name:	Load Indirect Start Instance
ShortName:	3DPRIM_START_INSTANCE_POCSUNIT_BE_GEOMETRY
Address:	0243Ch-0243Fh
Name:	Load Indirect Start Instance
ShortName:	3DPRIM_START_INSTANCE_RCSUNIT_BE
Address:	1843Ch-1843Fh
Name:	Load Indirect Start Instance
ShortName:	3DPRIM_START_INSTANCE_POCSUNIT_BE

DWord	Bit	Description
0	31:0	**Start Vertex** Format: U32 This register is used to store the Start Instance of the 3D_PRIMITIVE command when Load Indirect Enable is set.

Load Indirect Start Vertex

3DPRIM_START_VERTEX - Load Indirect Start Vertex	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	32
Address:	02430h-02433h
Name:	Load Indirect Start Vertex
ShortName:	3DPRIM_START_VERTEX_RCSUNIT_BE_GEOMETRY
Address:	18430h-18433h
Name:	Load Indirect Start Vertex
ShortName:	3DPRIM_START_VERTEX_POCSUNIT_BE_GEOMETRY
Address:	02430h-02433h
Name:	Load Indirect Start Vertex
ShortName:	3DPRIM_START_VERTEX_RCSUNIT_BE
Address:	18430h-18433h
Name:	Load Indirect Start Vertex
ShortName:	3DPRIM_START_VERTEX_POCSUNIT_BE

DWord	Bit	Description
0	31:0	**Start Vertex** Format: U32 This register is used to store the Start Vertex of the 3D_PRIMITIVE command when Load Indirect Enable is set.

Load Indirect Vertex Count

3DPRIM_VERTEX_COUNT - Load Indirect Vertex Count

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	32
Address:	02434h-02437h
Name:	Load Indirect Vertex Count
ShortName:	3DPRIM_VERTEX_COUNT_RCSUNIT_BE_GEOMETRY
Address:	18434h-18437h
Name:	Load Indirect Vertex Count
ShortName:	3DPRIM_VERTEX_COUNT_POCSUNIT_BE_GEOMETRY
Address:	02434h-02437h
Name:	Load Indirect Vertex Count
ShortName:	3DPRIM_VERTEX_COUNT_RCSUNIT_BE
Address:	18434h-18437h
Name:	Load Indirect Vertex Count
ShortName:	3DPRIM_VERTEX_COUNT_POCSUNIT_BE

DWord	Bit	Description
0	31:0	**Vertex Count** Format: U32 This register is used to store the Vertex Count of the 3D_PRIMITIVE command when Load Indirect Enable is set.

LUT_3D_CTL

LUT_3D_CTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled
Address:	490A4h-490A7h
Name:	Pipe A 3D LUT Control
ShortName:	LUT_3D_CTL_A
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31	**LUT 3D Enable** This field enables the 3D LUT. Value / Name: 0b – Disable 1b – Enable **Programming Notes** 3D LUT can be enabled/disabled at any time irrespective of when the pipe is enabled/disabled. Program the Bit 10 of register 420b0h to 1b to ensure that the 3D LUT functionality gets enabled right on the first frame when the pipe turns on.
	30	**New LUT Ready** Access: R/W Set This bit must be set to '1' after all the 3D LUT entries are programmed. This bit will get cleared by hardware after the LUT buffer is loaded in to the internal working RAM. Value / Name / Description: 0b – New LUT not ready – New LUT is not yet ready/hardware finished loading the LUT buffer in to internal working RAM. 1b – New LUT Ready – New LUT is ready. **Restriction** Once set, only hardware is allowed to clear this bit. Software cannot clear this bit.

LUT_3D_CTL

	29	**Allow Double Buffer Update Disable** Access: R/W This field controls whether double buffer updates are allowed to be disabled for the 3D LUT registers that are double buffered. The DOUBLE_BUFFER_CTL register can be configured to globally disable double buffer updates for those resources that allow them to be disabled. **Value** / **Name** 0b: Not Allowed 1b: Allowed **[Default]**
	28:0	**Reserved** Format: MBZ

LUT_3D_DATA

LUT_3D_DATA	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	490ACh-490AFh
Name:	Pipe A 3D LUT Data
ShortName:	LUT_3D_DATA_A
Power:	PG1
Reset:	soft

These are the 3D LUT entries. The 3D LUT Index Value indicates the 3D LUT location to be accessed through this register.
Even though this specific register is not double buffered, the 3D LUT table that this register accesses is (i.e. this register updates the table's back buffer). The double buffering point for the table (after DB'ing is armed) is the start of V. Blank or the Pipe is disabled

Restriction
This register must be written only as a full 32 bit dword. Byte or word writes are not supported.

DWord	Bit	Description
0	31:30	**Reserved**
	29:0	**LUT 3D Entry** 3D LUT entry value programmed as R10G10B10.

LUT_3D_INDEX

LUT_3D_INDEX

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	490A8h-490ABh
Name:	Pipe A 3D LUT Index
ShortName:	LUT_3D_INDEX_A
Power:	PG1
Reset:	soft

This index controls access to the pre-double buffered array of 3D LUT entries.
Even though this specific register is not double buffered, the 3D LUT table that this register accesses is (i.e. this register updates the table's back buffer). The double buffering point for the table (after DB'ing is armed) is the start of V. Blank or the Pipe is disabled

DWord	Bit	Description
0	31:14	**Reserved** Format: MBZ
	13	**Index Auto Increment** This field enables the index value to auto increment on each read or write to the data register.. Value: 0b — Name: No Increment Value: 1b — Name: Auto Increment
	12:0	**Index Value** This field indicates the data location to be accessed through the data register. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set. When automatically incrementing, the current automatically calculated index value can be read here, and the index will roll over to 0 after reaching the end of the allowed range. Value: [0,4912] — Name: