Intel® Iris® Plus Graphics and UHD Graphics Open Source

Programmer's Reference Manual

For the 2019 10th Generation Intel Core™ Processors based on the "Ice Lake" Platform

Volume 2c: Command Reference: Registers
Part 2 – Registers M through Z

January 2020, Revision 1.0

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MBC Control Register

MBCTL - MBC Control Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0907Ch

MBC Control Register

DWord	Bit	Description
0	31:18	**ECORSVD** Access: R/W ECO purposes Reserved
	17	**U2C Global PMON Enable Override** Default Value: 1b Access: R/W U2C Performance Monitor Global Enable Override 0 - U2C Global PMON needs to be enabled for performance monitors to be enabled (default) 1 - Overrride U2C Global PMON Enable is ignored in baled performance monitor counters
	16	**VCR Fuse Writes as Posted** Access: R/W Non-posted fuse fetching is NOT supported. Only posted is allowed (the default). 0 - MBCunit sends VCR Fuse Writes as Non-posted. 1 - MBCunit sends VCR Fuse Writes as posted.
	15:8	**RSVD** Access: RO
	7	**Disable Wait for SQemtpy in MAE** Access: R/W 0 - Wait for SQempty for MAE update Flow. 1 - MBC MAE update FSM does not wait for the SQempty to complete the FSM.
	6	**Reserved**
	5	**RSVD** Access: RO
	4	**MBC Driver Boot Enable**

MBCTL - MBC Control Register

		Access: R/W Config bit for driver managed boot kick off. 1 - Enable Boot Fetch without any PM interaction. 0 - Default (no action). This Bit is cleared by the Hardware once the Boot fetch is complete. **This bit is unsupported and must not be set**
	3	**Context Fetch Needed** Access: R/W Context Fetch Needed for Power Exits. 0 - Context Fetch Not Needed. 1 - Context Fetch Needed for Power Exits (CPD Entry).
	2	**BME Update Enable** Access: R/W BME update Enable: 0 - Default BME Update is not Enabled. MBC ignores all the BME updates from SA. 1- BME update is Enabled.
	1	**MAE Update Enable** Access: R/W MAE update Enable: 0 - Default MAE Update is not Enabled. MBC ignores all the MAE updates from SA. 1 - MAE update is Enabled. MBC responds to the MAE updates.
	0	**RSVD** Access: RO

MBUS_ABOX_CTL

MBUS_ABOX_CTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	45038h-4503Bh
Name:	MBus ABox Control
ShortName:	MBUS_ABOX_CTL
Power:	Always on
Reset:	soft

DWord	Bit	Description
0	31	**Status** Access: RO This field indicates if the box is enabled. 0b: Disabled 1b: Enabled
	30:28	**Reserved** Format: MBZ
	27:24	**Ring Stop Address** Access: RO This field indicates the address of the box in the ring.
	23:22	**Reserved** Format: MBZ
	21:20	**BW Credits** Default Value: 1h BW credits are used by the VGA host controller to write data to Display Buffer.
	19:16	**B Credits** Default Value: 1h

MBUS_ABOX_CTL

		B Credits are used by the Arbiter to request data from the Display Buffer for FBC/WiDi write back to memory.
	15:13	**Reserved** Format: MBZ
	12:8	**BT Credits Pool2** Default Value: 10h BT credits are used by the Arbiter to request trackers from the Display Buffer.
	7:5	**Reserved** Format: MBZ
	4:0	**BT Credits Pool1** Default Value: 10h BT credits are used by the Arbiter to request trackers from the Display Buffer.

MBUS_BBOX_CTL

MBUS_BBOX_CTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32

Address:	45040h-45043h
Name:	MBus BBox 1 Control
ShortName:	MBUS_BBOX_CTL_S1
Power:	PG0
Reset:	soft

Address:	45044h-45047h
Name:	MBus BBox 2 Control
ShortName:	MBUS_BBOX_CTL_S2
Power:	PG0
Reset:	soft

DWord	Bit	Description
0	31	**Status** Access: RO This field indicates if the box is enabled. 0b: Disabled 1b: Enabled
	30:28	**Reserved** Format: MBZ
	27:24	**Ring Stop Address** Access: RO This field indicates the address of the box in the ring.
	23:0	**Reserved** Format: MBZ

MBUS_DBOX_CTL

MBUS_DBOX_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank OR pipe disabled
Address:	7003Ch-7003Fh
Name:	Pipe MBus DBox Control
ShortName:	PIPE_MBUS_DBOX_CTL_A
Power:	PG1
Reset:	soft
Address:	7103Ch-7103Fh
Name:	Pipe MBus DBox Control
ShortName:	PIPE_MBUS_DBOX_CTL_B
Power:	PG2
Reset:	soft
Address:	7203Ch-7203Fh
Name:	Pipe MBus DBox Control
ShortName:	PIPE_MBUS_DBOX_CTL_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31	**Status** Access: RO This field indicates if the box is enabled. Value / Name: 0b – Disabled 1b – Enabled
	30:28	**Reserved**

MBUS_DBOX_CTL

	Format:	MBZ
27:24	**Ring Stop Address**	
	Access:	RO
	This field indicates the address of the box in the ring.	
23:16	**Reserved**	
	Format:	MBZ
15:14	**BW Credits**	
	Default Value:	1h
	BW credits are used by the display pipe to write color clear/WiDi/FBC/data in to display buffer.	
13	**Reserved**	
	Format:	MBZ
12:8	**B Credits**	
	Default Value:	06h
	B credits are used by the display pipe to request data from display buffer.	
7:4	**Reserved**	
	Format:	MBZ
3:0	**A Credits**	
	Default Value:	2h
	A credits are used by the display pipe to make data/TLB/VTd/MCS requests to Arbiter.	

MBUS_UBOX_CTL

MBUS_UBOX_CTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	4503Ch-4503Fh
Name:	MBus UBox Control
ShortName:	MBUS_UBOX_CTL
Power:	PG0
Reset:	soft

DWord	Bit	Description
0	31	**Status** Access: RO This field indicates if the box is enabled. 0b: Disabled 1b: Enabled
	30:28	**Reserved** Format: MBZ
	27:24	**Ring Stop Address** Access: RO This field indicates the address of the box in the ring.
	23:7	**Reserved** Format: MBZ
	6:4	**KVM Sprite A Credits** Default Value: 1 A Credits used by KVM to make data requests to Arbiter.
	3	**Reserved** Format: MBZ

MBUS_UBOX_CTL		
	2:0	**VGA B Credits** Default Value: 4 B credits used by VGA to request data from Display Buffer.

MCR Packet Control

MCRPKT_CTRL - MCR Packet Control

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00FDCh-00FDFh

DWord	Bit	Description
0	31	**MULTICAST** Default Value: 1b Access: R/W Value determines the multicast value driven to MCR. 0 - not multicast 1 - multicast The usage model is that the value is returned to the default (1), after completion of the unicast request.
	30:27	**SLICEID** Default Value: 0000b Access: R/W Value determines the slice ID driven to MCR.
	26:24	**SUBSLICEID** Default Value: 000b Access: R/W Value determines the subslice ID (or l3_bank) driven to MCR.
	23:0	**Reserved** Access: RO

MDRB Context Base 1

MDRB_CTXBASE1 - MDRB Context Base 1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00DC8h

RC6 Save Location

DWord	Bit	Description
0	31:6	**MDRB Memory Base Low** Access: R/W Lock This field is used to set the base of memory where the RC6 power context will be saved This value MUST be above the base and below the top of stolen memory This register is locked (becomes read-only) when RC6MEMLOCK is 1
	5:1	**Reserved** Access: RO
	0	**Ctx Base is Enabled** Access: R/W Lock 1'b0 : The MDRB base has not been enabled, so don't do the MDRB context save (This is default value and BIOS has to program it to enable context save) 1'b1 : The MDRB base has been enabled, so go ahead with the context save

MDRB Context Base 2

MDRB_CTXBASE2 - MDRB Context Base 2		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00DCCh	
RC6 Base Location		
DWord	**Bit**	**Description**
0	31:0	**MDRB Memory Base High** Access: R/W Lock This field is used to set the base of memory where the RC6 power context will be saved This value MUST be above the base and below the top of stolen memory This register is locked (becomes read-only) when RC6MEMLOCK is 1

Media 0 MOCS LECC 00 TC 00 Register

MFX0_MOCS_LECC_00_TC_00 - Media 0 MOCS LECC 00 TC 00 Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0C900h
Name:	Media 0 MOCS 0
ShortName:	MFX0_MOCS_0
Address:	0C940h
Name:	Media 0 MOCS 16
ShortName:	MFX0_MOCS_16
Address:	0C980h
Name:	Media 0 MOCS 32
ShortName:	MFX0_MOCS_32
Address:	0C9C0h
Name:	Media 0 MOCS 48
ShortName:	MFX0_MOCS_48

MFX0 MOCS register

DWord	Bit	Description
0	31:19	**Reserved** Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service**

MFX0_MOCS_LECC_00_TC_00 - Media 0 MOCS LECC 00 TC 00 Register

		Default Value: 00b Access: R/W This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec. 00: Value from Private PAT Registers(40E0/40E4/40E8/40EC) 01: Class 1 10: Class 2 11: Class 3
	14	**Reserved**
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is do not care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W

		Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page

MFX0_MOCS_LECC_00_TC_00 - Media 0 MOCS LECC 00 TC 00 Register		
		table controls and cannot be managed via MOCS index

Media 0 MOCS LECC 00 TC 01 Register

MFX0_MOCS_LECC_00_TC_01 - Media 0 MOCS LECC 00 TC 01 Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0C904h
Name:	Media 0 MOCS 1
ShortName:	MFX0_MOCS_1
Address:	0C944h
Name:	Media 0 MOCS 17
ShortName:	MFX0_MOCS_17
Address:	0C984h
Name:	Media 0 MOCS 33
ShortName:	MFX0_MOCS_33
Address:	0C9C4h
Name:	Media 0 MOCS 49
ShortName:	MFX0_MOCS_49

MFX0 MOCS register

DWord	Bit	Description
0	31:19	**Reserved** Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service**

MFX0_MOCS_LECC_00_TC_01 - Media 0 MOCS LECC 00 TC 01 Register

		Default Value: 00b Access: R/W This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec. 00: Value from Private PAT Registers(40E0/40E4/40E8/40EC) 01: Class 1 10: Class 2 11: Class 3
	14	**Reserved**
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is do not care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W

		Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page

MFX0_MOCS_LECC_00_TC_01 - Media 0 MOCS LECC 00 TC 01 Register		
		table controls and cannot be managed via MOCS index

Media0 MOCS LECC 00 TC 10 Register

MFX0_MOCS_LECC_00_TC_10 - Media0 MOCS LECC 00 TC 10 Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0C908h
Name:	Media0 MOCS 2
ShortName:	MFX0_MOCS_2
Address:	0C948h
Name:	Media0 MOCS 18
ShortName:	MFX0_MOCS_18
Address:	0C988h
Name:	Media0 MOCS 34
ShortName:	MFX0_MOCS_34
Address:	0C9C8h
Name:	Media0 MOCS 50
ShortName:	MFX0_MOCS_50

MFX0 MOCS register

DWord	Bit	Description
0	31:19	**Reserved** Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service**

MFX0_MOCS_LECC_00_TC_10 - Media0 MOCS LECC 00 TC 10 Register

		Default Value: 00b Access: R/W This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec. 00: Value from Private PAT Registers(40E0/40E4/40E8/40EC) 01: Class 1 10: Class 2 11: Class 3
	14	**Reserved**
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is do not care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W

MFX0_MOCS_LECC_00_TC_10 - Media0 MOCS LECC 00 TC 10 Register

		Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page

MFX0_MOCS_LECC_00_TC_10 - Media0 MOCS LECC 00 TC 10 Register		
		table controls and cannot be managed via MOCS index

Media0 MOCS LECC 01 TC 00 Register

MFX0_MOCS_LECC_01_TC_00 - Media0 MOCS LECC 01 TC 00 Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0C90Ch
Name:	Media0 MOCS 3
ShortName:	MFX0_MOCS_3
Address:	0C94Ch
Name:	Media0 MOCS 19
ShortName:	MFX0_MOCS_19
Address:	0C98Ch
Name:	Media0 MOCS 35
ShortName:	MFX0_MOCS_35
Address:	0C9CCh
Name:	Media0 MOCS 51
ShortName:	MFX0_MOCS_51

MFX0 MOCS register

DWord	Bit	Description
0	31:19	**Reserved** Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service**

MFX0_MOCS_LECC_01_TC_00 - Media0 MOCS LECC 01 TC 00 Register

		Default Value: 00b Access: R/W This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec. 00: Value from Private PAT Registers(40E0/40E4/40E8/40EC) 01: Class 1 10: Class 2 11: Class 3
	14	**Reserved**
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is do not care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W

		Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page

MFX0_MOCS_LECC_01_TC_00 - Media0 MOCS LECC 01 TC 00 Register		
		table controls and cannot be managed via MOCS index

Media0 MOCS LECC 10 TC 00 Register

MFX0_MOCS_LECC_10_TC_00 - Media0 MOCS LECC 10 TC 00 Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0C910h
Name:	Media 0 MOCS 4
ShortName:	MFX0_MOCS_4
Address:	0C928h
Name:	Media 0 MOCS 10
ShortName:	MFX0_MOCS_10
Address:	0C950h
Name:	Media 0 MOCS 20
ShortName:	MFX0_MOCS_20
Address:	0C968h
Name:	Media 0 MOCS 26
ShortName:	MFX0_MOCS_26
Address:	0C990h
Name:	Media 0 MOCS 36
ShortName:	MFX0_MOCS_36
Address:	0C9A8h
Name:	Media 0 MOCS 42
ShortName:	MFX0_MOCS_42
Address:	0C9D0h
Name:	Media 0 MOCS 52
ShortName:	MFX0_MOCS_52
Address:	0C9E8h
Name:	Media 0 MOCS 58
ShortName:	MFX0_MOCS_58
MFX0 MOCS register	

DWord	Bit	Description
0	31:19	**Reserved**

MFX0_MOCS_LECC_10_TC_00 - Media0 MOCS LECC 10 TC 00 Register

		Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service** Default Value: 00b Access: R/W This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec. 00: Value from Private PAT Registers(40E0/40E4/40E8/40EC) 01: Class 1 10: Class 2 11: Class 3
	14	**Reserved**
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is do not care

MFX0_MOCS_LECC_10_TC_00 - Media0 MOCS LECC 10 TC 00 Register

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC)

MFX0_MOCS_LECC_10_TC_00 - Media0 MOCS LECC 10 TC 00 Register

		01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

Media0 MOCS LECC 10 TC 01 Register

MFX0_MOCS_LECC_10_TC_01 - Media0 MOCS LECC 10 TC 01 Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0C914h
Name:	Media 0 MOCS 5
ShortName:	MFX0_MOCS_5
Address:	0C92Ch
Name:	Media 0 MOCS 11
ShortName:	MFX0_MOCS_11
Address:	0C954h
Name:	Media 0 MOCS 21
ShortName:	MFX0_MOCS_21
Address:	0C96Ch
Name:	Media 0 MOCS 27
ShortName:	MFX0_MOCS_27
Address:	0C994h
Name:	Media 0 MOCS 37
ShortName:	MFX0_MOCS_37
Address:	0C9ACh
Name:	Media 0 MOCS 43
ShortName:	MFX0_MOCS_43
Address:	0C9D4h
Name:	Media 0 MOCS 53
ShortName:	MFX0_MOCS_53
Address:	0C9ECh
Name:	Media 0 MOCS 59
ShortName:	MFX0_MOCS_59

MFX0 MOCS register

DWord	Bit	Description
0	31:19	**Reserved**

MFX0_MOCS_LECC_10_TC_01 - Media0 MOCS LECC 10 TC 01 Register

	Default Value:	0000000000000b
	Access:	RO

18:17 Self Snoop Enable

Default Value:	00b
Access:	R/W

00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic
01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface
11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface

16:15 Class of Service

Default Value:	00b
Access:	R/W

This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3

14 Reserved

13:11 Page Faulting Mode

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8 Skip Caching control

Default Value:	000b
Access:	R/W

Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface.
If "0" - than corresponding address bit value is do not care

MFX0_MOCS_LECC_10_TC_01 - Media0 MOCS LECC 10 TC 01 Register

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC)

MFX0_MOCS_LECC_10_TC_01 - Media0 MOCS LECC 10 TC 01 Register

		01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

Media 0 MOCS LECC 10 TC 10 Register

MFX0_MOCS_LECC_10_TC_10 - Media 0 MOCS LECC 10 TC 10 Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0C918h
Name:	Media 0 MOCS 6
ShortName:	MFX0_MOCS_6
Address:	0C930h
Name:	Media 0 MOCS 12
ShortName:	MFX0_MOCS_12
Address:	0C958h
Name:	Media 0 MOCS 22
ShortName:	MFX0_MOCS_22
Address:	0C970h
Name:	Media 0 MOCS 28
ShortName:	MFX0_MOCS_28
Address:	0C998h
Name:	Media 0 MOCS 38
ShortName:	MFX0_MOCS_38
Address:	0C9B0h
Name:	Media 0 MOCS 44
ShortName:	MFX0_MOCS_44
Address:	0C9D8h
Name:	Media 0 MOCS 54
ShortName:	MFX0_MOCS_54
Address:	0C9F0h
Name:	Media 0 MOCS 60
ShortName:	MFX0_MOCS_60

MFX0 MOCS register

DWord	Bit	Description
0	31:19	**Reserved**

MFX0_MOCS_LECC_10_TC_10 - Media 0 MOCS LECC 10 TC 10 Register

	Default Value:	0000000000000b
	Access:	RO

18:17 Self Snoop Enable

Default Value:	00b
Access:	R/W

00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic
01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface
11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface

16:15 Class of Service

Default Value:	00b
Access:	R/W

This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3

14 Reserved

13:11 Page Faulting Mode

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8 Skip Caching control

Default Value:	000b
Access:	R/W

Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface.
If "0" - than corresponding address bit value is do not care

MFX0_MOCS_LECC_10_TC_10 - Media 0 MOCS LECC 10 TC 10 Register

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC)

<table>
<tr><th colspan="3">MFX0_MOCS_LECC_10_TC_10 - Media 0 MOCS LECC 10 TC 10 Register</th></tr>
<tr><td></td><td></td><td>01: LLC Only
10: LLC/eLLC Allowed
11: LLC/eLLC Allowed</td></tr>
<tr><td></td><td>1:0</td><td>LLC/eDRAM cacheability control<table><tr><td>Default Value:</td><td>10b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>Memory type information used in LLC/eDRAM.
00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)
01: Uncacheable (UC) - non-cacheable
10: Writethrough (WT)
11: Writeback (WB)
Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used
Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index</td></tr>
</table>

Media 0 MOCS LECC 11 TC 00 Register

MFX0_MOCS_LECC_11_TC_00 - Media 0 MOCS LECC 11 TC 00 Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0C91Ch
Name:	Media 0 MOCS 7
ShortName:	MFX0_MOCS_7
Address:	0C934h
Name:	Media 0 MOCS 13
ShortName:	MFX0_MOCS_13
Address:	0C95Ch
Name:	Media 0 MOCS 23
ShortName:	MFX0_MOCS_23
Address:	0C974h
Name:	Media 0 MOCS 29
ShortName:	MFX0_MOCS_29
Address:	0C99Ch
Name:	Media 0 MOCS 39
ShortName:	MFX0_MOCS_39
Address:	0C9B4h
Name:	Media 0 MOCS 45
ShortName:	MFX0_MOCS_45
Address:	0C9DCh
Name:	Media 0 MOCS 55
ShortName:	MFX0_MOCS_55
Address:	0C9F4h
Name:	Media 0 MOCS 61
ShortName:	MFX0_MOCS_61

MFX0 MOCS register

DWord	Bit	Description
0	31:19	**Reserved**

MFX0_MOCS_LECC_11_TC_00 - Media 0 MOCS LECC 11 TC 00 Register

	Default Value:	0000000000000b
	Access:	RO

18:17 Self Snoop Enable

Default Value:	00b
Access:	R/W

00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic
01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface
11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface

16:15 Class of Service

Default Value:	00b
Access:	R/W

This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3

14 Reserved

13:11 Page Faulting Mode

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8 Skip Caching control

Default Value:	000b
Access:	R/W

Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface.
If "0" - than corresponding address bit value is do not care

MFX0_MOCS_LECC_11_TC_00 - Media 0 MOCS LECC 11 TC 00 Register

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC)

<table>
<tr><th colspan="3">MFX0_MOCS_LECC_11_TC_00 - Media 0 MOCS LECC 11 TC 00 Register</th></tr>
<tr><td></td><td></td><td>01: LLC Only
10: LLC/eLLC Allowed
11: LLC/eLLC Allowed</td></tr>
<tr><td></td><td>1:0</td><td>LLC/eDRAM cacheability control<table><tr><td>Default Value:</td><td>11b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>Memory type information used in LLC/eDRAM.
00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)
01: Uncacheable (UC) - non-cacheable
10: Writethrough (WT)
11: Writeback (WB)
Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used
Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index</td></tr>
</table>

Media 0 MOCS LECC 11 TC 01 Register

MFX0_MOCS_LECC_11_TC_01 - Media 0 MOCS LECC 11 TC 01 Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0C920h
Name:	Media 0 MOCS 8
ShortName:	MFX0_MOCS_8
Address:	0C938h
Name:	Media 0 MOCS 14
ShortName:	MFX0_MOCS_14
Address:	0C960h
Name:	Media 0 MOCS 24
ShortName:	MFX0_MOCS_24
Address:	0C978h
Name:	Media 0 MOCS 30
ShortName:	MFX0_MOCS_30
Address:	0C9A0h
Name:	Media 0 MOCS 40
ShortName:	MFX0_MOCS_40
Address:	0C9B8h
Name:	Media 0 MOCS 46
ShortName:	MFX0_MOCS_46
Address:	0C9E0h
Name:	Media 0 MOCS 56
ShortName:	MFX0_MOCS_56
Address:	0C9F8h
Name:	Media 0 MOCS 62
ShortName:	MFX0_MOCS_62

MFX0 MOCS register

DWord	Bit	Description
0	31:19	**Reserved**

MFX0_MOCS_LECC_11_TC_01 - Media 0 MOCS LECC 11 TC 01 Register

	Default Value:	0000000000000b
	Access:	RO

18:17 Self Snoop Enable

Default Value:	00b
Access:	R/W

00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic
01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface
11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface

16:15 Class of Service

Default Value:	00b
Access:	R/W

This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3

14 Reserved

13:11 Page Faulting Mode

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8 Skip Caching control

Default Value:	000b
Access:	R/W

Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface.
If "0" - than corresponding address bit value is do not care

MFX0_MOCS_LECC_11_TC_01 - Media 0 MOCS LECC 11 TC 01 Register

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC)

<table>
<tr><th colspan="3">MFX0_MOCS_LECC_11_TC_01 - Media 0 MOCS LECC 11 TC 01 Register</th></tr>
<tr><td></td><td></td><td>01: LLC Only
10: LLC/eLLC Allowed
11: LLC/eLLC Allowed</td></tr>
<tr><td></td><td>1:0</td><td>LLC/eDRAM cacheability control<table><tr><td>Default Value:</td><td>11b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>Memory type information used in LLC/eDRAM.
00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)
01: Uncacheable (UC) - non-cacheable
10: Writethrough (WT)
11: Writeback (WB)
Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used
Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index</td></tr>
</table>

Media 0 MOCS LECC 11 TC 10 Register

MFX0_MOCS_LECC_11_TC_10 - Media 0 MOCS LECC 11 TC 10 Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0C924h
Name:	Media 0 MOCS 9
ShortName:	MFX0_MOCS_9
Address:	0C93Ch
Name:	Media 0 MOCS 15
ShortName:	MFX0_MOCS_15
Address:	0C964h
Name:	Media 0 MOCS 25
ShortName:	MFX0_MOCS_25
Address:	0C97Ch
Name:	Media 0 MOCS 31
ShortName:	MFX0_MOCS_31
Address:	0C9A4h
Name:	Media 0 MOCS 41
ShortName:	MFX0_MOCS_41
Address:	0C9BCh
Name:	Media 0 MOCS 47
ShortName:	MFX0_MOCS_47
Address:	0C9E4h
Name:	Media 0 MOCS 57
ShortName:	MFX0_MOCS_57
Address:	0C9FCh
Name:	Media 0 MOCS 63
ShortName:	MFX0_MOCS_63

MFX0 MOCS register

DWord	Bit	Description
0	31:19	**Reserved**

MFX0_MOCS_LECC_11_TC_10 - Media 0 MOCS LECC 11 TC 10 Register

	Default Value:	0000000000000b
	Access:	RO

18:17 Self Snoop Enable

Default Value:	00b
Access:	R/W

00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic
01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface
11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface

16:15 Class of Service

Default Value:	00b
Access:	R/W

This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3

14 Reserved

13:11 Page Faulting Mode

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8 Skip Caching control

Default Value:	000b
Access:	R/W

Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface.
If "0" - than corresponding address bit value is do not care

MFX0_MOCS_LECC_11_TC_10 - Media 0 MOCS LECC 11 TC 10 Register

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC)

<table>
<tr><th colspan="3">MFX0_MOCS_LECC_11_TC_10 - Media 0 MOCS LECC 11 TC 10 Register</th></tr>
<tr><td></td><td></td><td>01: LLC Only
10: LLC/eLLC Allowed
11: LLC/eLLC Allowed</td></tr>
<tr><td></td><td>1:0</td><td>LLC/eDRAM cacheability control
<table><tr><td>Default Value:</td><td>11b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>Memory type information used in LLC/eDRAM.
00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)
01: Uncacheable (UC) - non-cacheable
10: Writethrough (WT)
11: Writeback (WB)
Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used
Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index</td></tr>
</table>

Media 1 MOCS LECC 00 TC 00 Register

MFX1_MOCS_LECC_00_TC_00 - Media 1 MOCS LECC 00 TC 00 Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CA00h
Name:	Media 1 MOCS 0
ShortName:	MFX1_MOCS_0
Address:	0CA40h
Name:	Media 1 MOCS 16
ShortName:	MFX1_MOCS_16
Address:	0CA80h
Name:	Media 1 MOCS 32
ShortName:	MFX1_MOCS_32
Address:	0CAC0h
Name:	Media 1 MOCS 48
ShortName:	MFX1_MOCS_48

MFX1 MOCS register

DWord	Bit	Description
0	31:19	**Reserved** Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service**

MFX1_MOCS_LECC_00_TC_00 - Media 1 MOCS LECC 00 TC 00 Register

		Default Value: 00b Access: R/W This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec. 00: Value from Private PAT Registers(40E0/40E4/40E8/40EC) 01: Class 1 10: Class 2 11: Class 3
	14	**Reserved**
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is do not care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W

MFX1_MOCS_LECC_00_TC_00 - Media 1 MOCS LECC 00 TC 00 Register

		Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

Media 1 MOCS LECC 00 TC 01 Register

MFX1_MOCS_LECC_00_TC_01 - Media 1 MOCS LECC 00 TC 01 Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CA04h
Name:	Media 1 MOCS 1
ShortName:	MFX1_MOCS_1
Address:	0CA44h
Name:	Media 1 MOCS 17
ShortName:	MFX1_MOCS_17
Address:	0CA84h
Name:	Media 1 MOCS 33
ShortName:	MFX1_MOCS_33
Address:	0CAC4h
Name:	Media 1 MOCS 49
ShortName:	MFX1_MOCS_49

MFX1 MOCS register

DWord	Bit	Description
0	31:19	**Reserved** Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service**

MFX1_MOCS_LECC_00_TC_01 - Media 1 MOCS LECC 00 TC 01 Register

		Default Value: 00b Access: R/W This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec. 00: Value from Private PAT Registers(40E0/40E4/40E8/40EC) 01: Class 1 10: Class 2 11: Class 3
	14	**Reserved**
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is do not care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W

MFX1_MOCS_LECC_00_TC_01 - Media 1 MOCS LECC 00 TC 01 Register

		Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

Media1 MOCS LECC 00 TC 10 Register

MFX1_MOCS_LECC_00_TC_10 - Media1 MOCS LECC 00 TC 10 Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CA08h
Name:	Media1 MOCS 2
ShortName:	MFX1_MOCS_2
Address:	0CA48h
Name:	Media1 MOCS 18
ShortName:	MFX1_MOCS_18
Address:	0CA88h
Name:	Media1 MOCS 34
ShortName:	MFX1_MOCS_34
Address:	0CAC8h
Name:	Media1 MOCS 50
ShortName:	MFX1_MOCS_50

MFX1 MOCS register

DWord	Bit	Description
0	31:19	**Reserved** Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service**

MFX1_MOCS_LECC_00_TC_10 - Media1 MOCS LECC 00 TC 10 Register

		Default Value: 00b Access: R/W This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec. 00: Value from Private PAT Registers(40E0/40E4/40E8/40EC) 01: Class 1 10: Class 2 11: Class 3
	14	**Reserved**
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is do not care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS

		Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

Media1 MOCS LECC 01 TC 00 Register

MFX1_MOCS_LECC_01_TC_00 - Media1 MOCS LECC 01 TC 00 Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CA0Ch
Name:	Media1 MOCS 3
ShortName:	MFX1_MOCS_3
Address:	0CA4Ch
Name:	Media1 MOCS 19
ShortName:	MFX1_MOCS_19
Address:	0CA8Ch
Name:	Media1 MOCS 35
ShortName:	MFX1_MOCS_35
Address:	0CACCh
Name:	Media1 MOCS 51
ShortName:	MFX1_MOCS_51

MFX1 MOCS register

DWord	Bit	Description
0	31:19	**Reserved** Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service**

MFX1_MOCS_LECC_01_TC_00 - Media1 MOCS LECC 01 TC 00 Register

		Default Value: 00b Access: R/W This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec. 00: Value from Private PAT Registers(40E0/40E4/40E8/40EC) 01: Class 1 10: Class 2 11: Class 3
	14	**Reserved**
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is do not care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W

MFX1_MOCS_LECC_01_TC_00 - Media1 MOCS LECC 01 TC 00 Register

		Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

Media1 MOCS LECC 10 TC 00 Register

MFX1_MOCS_LECC_10_TC_00 - Media1 MOCS LECC 10 TC 00 Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CA10h
Name:	Media 1 MOCS 4
ShortName:	MFX1_MOCS_4
Address:	0CA28h
Name:	Media 1 MOCS 10
ShortName:	MFX1_MOCS_10
Address:	0CA50h
Name:	Media 1 MOCS 20
ShortName:	MFX1_MOCS_20
Address:	0CA68h
Name:	Media 1 MOCS 26
ShortName:	MFX1_MOCS_26
Address:	0CA90h
Name:	Media 1 MOCS 36
ShortName:	MFX1_MOCS_36
Address:	0CAA8h
Name:	Media 1 MOCS 42
ShortName:	MFX1_MOCS_42
Address:	0CAD0h
Name:	Media 1 MOCS 52
ShortName:	MFX1_MOCS_52
Address:	0CAE8h
Name:	Media 1 MOCS 58
ShortName:	MFX1_MOCS_58

MFX1 MOCS register

DWord	Bit	Description
0	31:19	**Reserved**

MFX1_MOCS_LECC_10_TC_00 - Media1 MOCS LECC 10 TC 00 Register

	Default Value:	0000000000000b
	Access:	RO

18:17 Self Snoop Enable

Default Value:	00b
Access:	R/W

00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic
01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface
11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface

16:15 Class of Service

Default Value:	00b
Access:	R/W

This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3

14 Reserved

13:11 Page Faulting Mode

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8 Skip Caching control

Default Value:	000b
Access:	R/W

Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface.
If "0" - than corresponding address bit value is do not care

MFX1_MOCS_LECC_10_TC_00 - Media1 MOCS LECC 10 TC 00 Register

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC)

<table>
<tr><th colspan="3">MFX1_MOCS_LECC_10_TC_00 - Media1 MOCS LECC 10 TC 00 Register</th></tr>
<tr><td></td><td></td><td>01: LLC Only
10: LLC/eLLC Allowed
11: LLC/eLLC Allowed</td></tr>
<tr><td></td><td>1:0</td><td>LLC/eDRAM cacheability control<table><tr><td>Default Value:</td><td>10b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>Memory type information used in LLC/eDRAM.
00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)
01: Uncacheable (UC) - non-cacheable
10: Writethrough (WT)
11: Writeback (WB)
Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used
Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index</td></tr>
</table>

Media1 MOCS LECC 10 TC 01 Register

MFX1_MOCS_LECC_10_TC_01 - Media1 MOCS LECC 10 TC 01 Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CA14h
Name:	Media 1 MOCS 5
ShortName:	MFX1_MOCS_5
Address:	0CA2Ch
Name:	Media 1 MOCS 11
ShortName:	MFX1_MOCS_11
Address:	0CA54h
Name:	Media 1 MOCS 21
ShortName:	MFX1_MOCS_21
Address:	0CA6Ch
Name:	Media 1 MOCS 27
ShortName:	MFX1_MOCS_27
Address:	0CA94h
Name:	Media 1 MOCS 37
ShortName:	MFX1_MOCS_37
Address:	0CAACh
Name:	Media 1 MOCS 43
ShortName:	MFX1_MOCS_43
Address:	0CAD4h
Name:	Media 1 MOCS 53
ShortName:	MFX1_MOCS_53
Address:	0CAECh
Name:	Media 1 MOCS 59
ShortName:	MFX1_MOCS_59

MFX1 MOCS register

DWord	Bit	Description
0	31:19	**Reserved**

MFX1_MOCS_LECC_10_TC_01 - Media1 MOCS LECC 10 TC 01 Register

	Default Value:	0000000000000b
	Access:	RO

18:17 Self Snoop Enable

Default Value:	00b
Access:	R/W

00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic
01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface
11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface

16:15 Class of Service

Default Value:	00b
Access:	R/W

This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3

14 Reserved

13:11 Page Faulting Mode

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8 Skip Caching control

Default Value:	000b
Access:	R/W

Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface.
If "0" - than corresponding address bit value is do not care

MFX1_MOCS_LECC_10_TC_01 - Media1 MOCS LECC 10 TC 01 Register

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC)

<table>
<tr><th colspan="3">MFX1_MOCS_LECC_10_TC_01 - Media1 MOCS LECC 10 TC 01 Register</th></tr>
<tr><td></td><td></td><td>01: LLC Only
10: LLC/eLLC Allowed
11: LLC/eLLC Allowed</td></tr>
<tr><td></td><td>1:0</td><td>LLC/eDRAM cacheability control
<table><tr><td>Default Value:</td><td>10b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>Memory type information used in LLC/eDRAM.
00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)
01: Uncacheable (UC) - non-cacheable
10: Writethrough (WT)
11: Writeback (WB)
Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used
Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index</td></tr>
</table>

Media 1 MOCS LECC 10 TC 10 Register

MFX1_MOCS_LECC_10_TC_10 - Media 1 MOCS LECC 10 TC 10 Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CA18h
Name:	Media 1 MOCS 6
ShortName:	MFX1_MOCS_6
Address:	0CA30h
Name:	Media 1 MOCS 12
ShortName:	MFX1_MOCS_12
Address:	0CA58h
Name:	Media 1 MOCS 22
ShortName:	MFX1_MOCS_22
Address:	0CA70h
Name:	Media 1 MOCS 28
ShortName:	MFX1_MOCS_28
Address:	0CA98h
Name:	Media 1 MOCS 38
ShortName:	MFX1_MOCS_38
Address:	0CAB0h
Name:	Media 1 MOCS 44
ShortName:	MFX1_MOCS_44
Address:	0CAD8h
Name:	Media 1 MOCS 54
ShortName:	MFX1_MOCS_54
Address:	0CAF0h
Name:	Media 1 MOCS 60
ShortName:	MFX1_MOCS_60

MFX1 MOCS register

DWord	Bit	Description
0	31:19	**Reserved**

MFX1_MOCS_LECC_10_TC_10 - Media 1 MOCS LECC 10 TC 10 Register

	Default Value:	0000000000000b
	Access:	RO

18:17 Self Snoop Enable

Default Value:	00b
Access:	R/W

00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic
01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface
11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface

16:15 Class of Service

Default Value:	00b
Access:	R/W

This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3

14 Reserved

13:11 Page Faulting Mode

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8 Skip Caching control

Default Value:	000b
Access:	R/W

Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface.
If "0" - than corresponding address bit value is do not care

MFX1_MOCS_LECC_10_TC_10 - Media 1 MOCS LECC 10 TC 10 Register

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC)

MFX1_MOCS_LECC_10_TC_10 - Media 1 MOCS LECC 10 TC 10 Register

		01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

Media 1 MOCS LECC 11 TC 00 Register

MFX1_MOCS_LECC_11_TC_00 - Media 1 MOCS LECC 11 TC 00 Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CA1Ch
Name:	Media 1 MOCS 7
ShortName:	MFX1_MOCS_7
Address:	0CA34h
Name:	Media 1 MOCS 13
ShortName:	MFX1_MOCS_13
Address:	0CA5Ch
Name:	Media 1 MOCS 23
ShortName:	MFX1_MOCS_23
Address:	0CA74h
Name:	Media 1 MOCS 29
ShortName:	MFX1_MOCS_29
Address:	0CA9Ch
Name:	Media 1 MOCS 39
ShortName:	MFX1_MOCS_39
Address:	0CAB4h
Name:	Media 1 MOCS 45
ShortName:	MFX1_MOCS_45
Address:	0CADCh
Name:	Media 1 MOCS 55
ShortName:	MFX1_MOCS_55
Address:	0CAF4h
Name:	Media 1 MOCS 61
ShortName:	MFX1_MOCS_61

MFX1 MOCS register

DWord	Bit	Description
0	31:19	**Reserved**

MFX1_MOCS_LECC_11_TC_00 - Media 1 MOCS LECC 11 TC 00 Register

	Default Value:	0000000000000b
	Access:	RO

18:17 Self Snoop Enable

Default Value:	00b
Access:	R/W

00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic
01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface
11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface

16:15 Class of Service

Default Value:	00b
Access:	R/W

This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3

14 Reserved

13:11 Page Faulting Mode

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8 Skip Caching control

Default Value:	000b
Access:	R/W

Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface.
If "0" - than corresponding address bit value is do not care

MFX1_MOCS_LECC_11_TC_00 - Media 1 MOCS LECC 11 TC 00 Register

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC)

<table>
<tr><th colspan="3">MFX1_MOCS_LECC_11_TC_00 - Media 1 MOCS LECC 11 TC 00 Register</th></tr>
<tr><td></td><td></td><td>01: LLC Only
10: LLC/eLLC Allowed
11: LLC/eLLC Allowed</td></tr>
<tr><td></td><td>1:0</td><td>LLC/eDRAM cacheability control<table><tr><td>Default Value:</td><td>11b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>Memory type information used in LLC/eDRAM.
00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)
01: Uncacheable (UC) - non-cacheable
10: Writethrough (WT)
11: Writeback (WB)
Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used
Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index</td></tr>
</table>

Media 1 MOCS LECC 11 TC 01 Register

MFX1_MOCS_LECC_11_TC_01 - Media 1 MOCS LECC 11 TC 01 Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CA20h
Name:	Media 1 MOCS 8
ShortName:	MFX1_MOCS_8
Address:	0CA38h
Name:	Media 1 MOCS 14
ShortName:	MFX1_MOCS_14
Address:	0CA60h
Name:	Media 1 MOCS 24
ShortName:	MFX1_MOCS_24
Address:	0CA78h
Name:	Media 1 MOCS 30
ShortName:	MFX1_MOCS_30
Address:	0CAA0h
Name:	Media 1 MOCS 40
ShortName:	MFX1_MOCS_40
Address:	0CAB8h
Name:	Media 1 MOCS 46
ShortName:	MFX1_MOCS_46
Address:	0CAE0h
Name:	Media 1 MOCS 56
ShortName:	MFX1_MOCS_56
Address:	0CAF8h
Name:	Media 1 MOCS 62
ShortName:	MFX1_MOCS_62
MFX1 MOCS register	

DWord	Bit	Description
0	31:19	**Reserved**

MFX1_MOCS_LECC_11_TC_01 - Media 1 MOCS LECC 11 TC 01 Register

	Default Value:	0000000000000b
	Access:	RO

18:17 Self Snoop Enable

Default Value:	00b
Access:	R/W

00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic
01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface
11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface

16:15 Class of Service

Default Value:	00b
Access:	R/W

This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3

14 Reserved

13:11 Page Faulting Mode

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8 Skip Caching control

Default Value:	000b
Access:	R/W

Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface.
If "0" - than corresponding address bit value is do not care

MFX1_MOCS_LECC_11_TC_01 - Media 1 MOCS LECC 11 TC 01 Register

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC)

<table>
<tr><th colspan="3">MFX1_MOCS_LECC_11_TC_01 - Media 1 MOCS LECC 11 TC 01 Register</th></tr>
<tr><td></td><td></td><td>01: LLC Only
10: LLC/eLLC Allowed
11: LLC/eLLC Allowed</td></tr>
<tr><td></td><td>1:0</td><td>LLC/eDRAM cacheability control<table><tr><td>Default Value:</td><td>11b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>Memory type information used in LLC/eDRAM.
00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)
01: Uncacheable (UC) - non-cacheable
10: Writethrough (WT)
11: Writeback (WB)
Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used
Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index</td></tr>
</table>

Media 1 MOCS LECC 11 TC 10 Register

MFX1_MOCS_LECC_11_TC_10 - Media 1 MOCS LECC 11 TC 10 Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CA24h
Name:	Media 1 MOCS 9
ShortName:	MFX1_MOCS_9
Address:	0CA3Ch
Name:	Media 1 MOCS 15
ShortName:	MFX1_MOCS_15
Address:	0CA64h
Name:	Media 1 MOCS 25
ShortName:	MFX1_MOCS_25
Address:	0CA7Ch
Name:	Media 1 MOCS 31
ShortName:	MFX1_MOCS_31
Address:	0CAA4h
Name:	Media 1 MOCS 41
ShortName:	MFX1_MOCS_41
Address:	0CABCh
Name:	Media 1 MOCS 47
ShortName:	MFX1_MOCS_47
Address:	0CAE4h
Name:	Media 1 MOCS 57
ShortName:	MFX1_MOCS_57
Address:	0CAFCh
Name:	Media 1 MOCS 63
ShortName:	MFX1_MOCS_63

MFX1 MOCS register

DWord	Bit	Description
0	31:19	**Reserved**

MFX1_MOCS_LECC_11_TC_10 - Media 1 MOCS LECC 11 TC 10 Register

		Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service** Default Value: 00b Access: R/W This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec. 00: Value from Private PAT Registers(40E0/40E4/40E8/40EC) 01: Class 1 10: Class 2 11: Class 3
	14	**Reserved**
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is do not care

MFX1_MOCS_LECC_11_TC_10 - Media 1 MOCS LECC 11 TC 10 Register

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC)

<table>
<tr><th colspan="3">MFX1_MOCS_LECC_11_TC_10 - Media 1 MOCS LECC 11 TC 10 Register</th></tr>
<tr><td></td><td></td><td>01: LLC Only
10: LLC/eLLC Allowed
11: LLC/eLLC Allowed</td></tr>
<tr><td></td><td>1:0</td><td>LLC/eDRAM cacheability control<table><tr><td>Default Value:</td><td>11b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>Memory type information used in LLC/eDRAM.
00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)
01: Uncacheable (UC) - non-cacheable
10: Writethrough (WT)
11: Writeback (WB)
Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used
Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index</td></tr>
</table>

Media2 MOCS Register

MFX2_MOCS - Media2 MOCS Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	10000h
Name:	MFX2 MOCS 0
ShortName:	MFX2_MOCS_0
Address:	10004h
Name:	MFX2 MOCS 1
ShortName:	MFX2_MOCS_1
Address:	10008h
Name:	MFX2 MOCS 2
ShortName:	MFX2_MOCS_2
Address:	1000Ch
Name:	MFX2 MOCS 3
ShortName:	MFX2_MOCS_3
Address:	10010h
Name:	MFX2 MOCS 4
ShortName:	MFX2_MOCS_4
Address:	10014h
Name:	MFX2 MOCS 5
ShortName:	MFX2_MOCS_5
Address:	10018h
Name:	MFX2 MOCS 6
ShortName:	MFX2_MOCS_6
Address:	1001Ch
Name:	MFX2 MOCS 7
ShortName:	MFX2_MOCS_7
Address:	10020h
Name:	MFX2 MOCS 8
ShortName:	MFX2_MOCS_8
Address:	10024h

MFX2_MOCS - Media2 MOCS Register	
Name:	MFX2 MOCS 9
ShortName:	MFX2_MOCS_9
Address:	10028h
Name:	MFX2 MOCS 10
ShortName:	MFX2_MOCS_10
Address:	1002Ch
Name:	MFX2 MOCS 11
ShortName:	MFX2_MOCS_11
Address:	10030h
Name:	MFX2 MOCS 12
ShortName:	MFX2_MOCS_12
Address:	10034h
Name:	MFX2 MOCS 13
ShortName:	MFX2_MOCS_13
Address:	10038h
Name:	MFX2 MOCS 14
ShortName:	MFX2_MOCS_14
Address:	1003Ch
Name:	MFX2 MOCS 15
ShortName:	MFX2_MOCS_15
Address:	10040h
Name:	MFX2 MOCS 16
ShortName:	MFX2_MOCS_16
Address:	10044h
Name:	MFX2 MOCS 17
ShortName:	MFX2_MOCS_17
Address:	10048h
Name:	MFX2 MOCS 18
ShortName:	MFX2_MOCS_18
Address:	1004Ch
Name:	MFX2 MOCS 19
ShortName:	MFX2_MOCS_19
Address:	10050h
Name:	MFX2 MOCS 20
ShortName:	MFX2_MOCS_20

MFX2_MOCS - Media2 MOCS Register	
Address:	10054h
Name:	MFX2 MOCS 21
ShortName:	MFX2_MOCS_21
Address:	10058h
Name:	MFX2 MOCS 22
ShortName:	MFX2_MOCS_22
Address:	1005Ch
Name:	MFX2 MOCS 23
ShortName:	MFX2_MOCS_23
Address:	10060h
Name:	MFX2 MOCS 24
ShortName:	MFX2_MOCS_24
Address:	10064h
Name:	MFX2 MOCS 25
ShortName:	MFX2_MOCS_25
Address:	10068h
Name:	MFX2 MOCS 26
ShortName:	MFX2_MOCS_26
Address:	1006Ch
Name:	MFX2 MOCS 27
ShortName:	MFX2_MOCS_27
Address:	10070h
Name:	MFX2 MOCS 28
ShortName:	MFX2_MOCS_28
Address:	10074h
Name:	MFX2 MOCS 29
ShortName:	MFX2_MOCS_29
Address:	10078h
Name:	MFX2 MOCS 30
ShortName:	MFX2_MOCS_30
Address:	1007Ch
Name:	MFX2 MOCS 31
ShortName:	MFX2_MOCS_31
Address:	10080h
Name:	MFX2 MOCS 32

MFX2_MOCS - Media2 MOCS Register	
ShortName:	MFX2_MOCS_32
Address:	10084h
Name:	MFX2 MOCS 33
ShortName:	MFX2_MOCS_33
Address:	10088h
Name:	MFX2 MOCS 34
ShortName:	MFX2_MOCS_34
Address:	1008Ch
Name:	MFX2 MOCS 35
ShortName:	MFX2_MOCS_35
Address:	10090h
Name:	MFX2 MOCS 36
ShortName:	MFX2_MOCS_36
Address:	10094h
Name:	MFX2 MOCS 37
ShortName:	MFX2_MOCS_37
Address:	10098h
Name:	MFX2 MOCS 38
ShortName:	MFX2_MOCS_38
Address:	1009Ch
Name:	MFX2 MOCS 39
ShortName:	MFX2_MOCS_39
Address:	100A0h
Name:	MFX2 MOCS 40
ShortName:	MFX2_MOCS_40
Address:	100A4h
Name:	MFX2 MOCS 41
ShortName:	MFX2_MOCS_41
Address:	100A8h
Name:	MFX2 MOCS 42
ShortName:	MFX2_MOCS_42
Address:	100ACh
Name:	MFX2 MOCS 43
ShortName:	MFX2_MOCS_43

MFX2_MOCS - Media2 MOCS Register	
Address:	100B0h
Name:	MFX2 MOCS 44
ShortName:	MFX2_MOCS_44
Address:	100B4h
Name:	MFX2 MOCS 45
ShortName:	MFX2_MOCS_45
Address:	100B8h
Name:	MFX2 MOCS 46
ShortName:	MFX2_MOCS_46
Address:	100BCh
Name:	MFX2 MOCS 47
ShortName:	MFX2_MOCS_47
Address:	100C0h
Name:	MFX2 MOCS 48
ShortName:	MFX2_MOCS_48
Address:	100C4h
Name:	MFX2 MOCS 49
ShortName:	MFX2_MOCS_49
Address:	100C8h
Name:	MFX2 MOCS 50
ShortName:	MFX2_MOCS_50
Address:	100CCh
Name:	MFX2 MOCS 51
ShortName:	MFX2_MOCS_51
Address:	100D0h
Name:	MFX2 MOCS 52
ShortName:	MFX2_MOCS_52
Address:	100D4h
Name:	MFX2 MOCS 53
ShortName:	MFX2_MOCS_53
Address:	100D8h
Name:	MFX2 MOCS 54
ShortName:	MFX2_MOCS_54
Address:	100DCh
Name:	MFX2 MOCS 55

MFX2_MOCS - Media2 MOCS Register

ShortName:	MFX2_MOCS_55

Address:	100E0h
Name:	MFX2 MOCS 56
ShortName:	MFX2_MOCS_56

Address:	100E4h
Name:	MFX2 MOCS 57
ShortName:	MFX2_MOCS_57

Address:	100E8h
Name:	MFX2 MOCS 58
ShortName:	MFX2_MOCS_58

Address:	100ECh
Name:	MFX2 MOCS 59
ShortName:	MFX2_MOCS_59

Address:	100F0h
Name:	MFX2 MOCS 60
ShortName:	MFX2_MOCS_60

Address:	100F4h
Name:	MFX2 MOCS 61
ShortName:	MFX2_MOCS_61

Address:	100F8h
Name:	MFX2 MOCS 62
ShortName:	MFX2_MOCS_62

Address:	100FCh
Name:	MFX2 MOCS 63
ShortName:	MFX2_MOCS_63

MFX2 MOCS register.

DWord	Bit	Description
0	31:19	**Reserved** Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit

		logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service** Default Value: 00b Access: R/W This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec. 00: Value from Private PAT Registers(40E0/40E4/40E8/40EC) 01: Class 1 10: Class 2 11: Class 3
	14	**Reserved**
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is do not care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior)

		1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

Media3 MOCS Register

MFX3_MOCS - Media3 MOCS Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	10100h
Name:	MFX3 MOCS 0
ShortName:	MFX3_MOCS_0
Address:	10104h
Name:	MFX3 MOCS 1
ShortName:	MFX3_MOCS_1
Address:	10108h
Name:	MFX3 MOCS 2
ShortName:	MFX3_MOCS_2
Address:	1010Ch
Name:	MFX3 MOCS 3
ShortName:	MFX3_MOCS_3
Address:	10110h
Name:	MFX3 MOCS 4
ShortName:	MFX3_MOCS_4
Address:	10114h
Name:	MFX3 MOCS 5
ShortName:	MFX3_MOCS_5
Address:	10118h
Name:	MFX3 MOCS 6
ShortName:	MFX3_MOCS_6
Address:	1011Ch
Name:	MFX3 MOCS 7
ShortName:	MFX3_MOCS_7
Address:	10120h
Name:	MFX3 MOCS 8
ShortName:	MFX3_MOCS_8
Address:	10124h

MFX3_MOCS - Media3 MOCS Register	
Name:	MFX3 MOCS 9
ShortName:	MFX3_MOCS_9
Address:	10128h
Name:	MFX3 MOCS 10
ShortName:	MFX3_MOCS_10
Address:	1012Ch
Name:	MFX3 MOCS 11
ShortName:	MFX3_MOCS_11
Address:	10130h
Name:	MFX3 MOCS 12
ShortName:	MFX3_MOCS_12
Address:	10134h
Name:	MFX3 MOCS 13
ShortName:	MFX3_MOCS_13
Address:	10138h
Name:	MFX3 MOCS 14
ShortName:	MFX3_MOCS_14
Address:	1013Ch
Name:	MFX3 MOCS 15
ShortName:	MFX3_MOCS_15
Address:	10140h
Name:	MFX3 MOCS 16
ShortName:	MFX3_MOCS_16
Address:	10144h
Name:	MFX3 MOCS 17
ShortName:	MFX3_MOCS_17
Address:	10148h
Name:	MFX3 MOCS 18
ShortName:	MFX3_MOCS_18
Address:	1014Ch
Name:	MFX3 MOCS 19
ShortName:	MFX3_MOCS_19
Address:	10150h
Name:	MFX3 MOCS 20
ShortName:	MFX3_MOCS_20

MFX3_MOCS - Media3 MOCS Register	
Address:	10154h
Name:	MFX3 MOCS 21
ShortName:	MFX3_MOCS_21
Address:	10158h
Name:	MFX3 MOCS 22
ShortName:	MFX3_MOCS_22
Address:	1015Ch
Name:	MFX3 MOCS 23
ShortName:	MFX3_MOCS_23
Address:	10160h
Name:	MFX3 MOCS 24
ShortName:	MFX3_MOCS_24
Address:	10164h
Name:	MFX3 MOCS 25
ShortName:	MFX3_MOCS_25
Address:	10168h
Name:	MFX3 MOCS 26
ShortName:	MFX3_MOCS_26
Address:	1016Ch
Name:	MFX3 MOCS 27
ShortName:	MFX3_MOCS_27
Address:	10170h
Name:	MFX3 MOCS 28
ShortName:	MFX3_MOCS_28
Address:	10174h
Name:	MFX3 MOCS 29
ShortName:	MFX3_MOCS_29
Address:	10178h
Name:	MFX3 MOCS 30
ShortName:	MFX3_MOCS_30
Address:	1017Ch
Name:	MFX3 MOCS 31
ShortName:	MFX3_MOCS_31
Address:	10180h
Name:	MFX3 MOCS 32

MFX3_MOCS - Media3 MOCS Register	
ShortName:	MFX3_MOCS_32
Address:	10184h
Name:	MFX3 MOCS 33
ShortName:	MFX3_MOCS_33
Address:	10188h
Name:	MFX3 MOCS 34
ShortName:	MFX3_MOCS_34
Address:	1018Ch
Name:	MFX3 MOCS 35
ShortName:	MFX3_MOCS_35
Address:	10190h
Name:	MFX3 MOCS 36
ShortName:	MFX3_MOCS_36
Address:	10194h
Name:	MFX3 MOCS 37
ShortName:	MFX3_MOCS_37
Address:	10198h
Name:	MFX3 MOCS 38
ShortName:	MFX3_MOCS_38
Address:	1019Ch
Name:	MFX3 MOCS 39
ShortName:	MFX3_MOCS_39
Address:	101A0h
Name:	MFX3 MOCS 40
ShortName:	MFX3_MOCS_40
Address:	101A4h
Name:	MFX3 MOCS 41
ShortName:	MFX3_MOCS_41
Address:	101A8h
Name:	MFX3 MOCS 42
ShortName:	MFX3_MOCS_42
Address:	101ACh
Name:	MFX3 MOCS 43
ShortName:	MFX3_MOCS_43

MFX3_MOCS - Media3 MOCS Register	
Address:	101B0h
Name:	MFX3 MOCS 44
ShortName:	MFX3_MOCS_44
Address:	101B4h
Name:	MFX3 MOCS 45
ShortName:	MFX3_MOCS_45
Address:	101B8h
Name:	MFX3 MOCS 46
ShortName:	MFX3_MOCS_46
Address:	101BCh
Name:	MFX3 MOCS 47
ShortName:	MFX3_MOCS_47
Address:	101C0h
Name:	MFX3 MOCS 48
ShortName:	MFX3_MOCS_48
Address:	101C4h
Name:	MFX3 MOCS 49
ShortName:	MFX3_MOCS_49
Address:	101C8h
Name:	MFX3 MOCS 50
ShortName:	MFX3_MOCS_50
Address:	101CCh
Name:	MFX3 MOCS 51
ShortName:	MFX3_MOCS_51
Address:	101D0h
Name:	MFX3 MOCS 52
ShortName:	MFX3_MOCS_52
Address:	101D4h
Name:	MFX3 MOCS 53
ShortName:	MFX3_MOCS_53
Address:	101D8h
Name:	MFX3 MOCS 54
ShortName:	MFX3_MOCS_54
Address:	101DCh
Name:	MFX3 MOCS 55

MFX3_MOCS - Media3 MOCS Register

ShortName:	MFX3_MOCS_55

Address:	101E0h
Name:	MFX3 MOCS 56
ShortName:	MFX3_MOCS_56

Address:	101E4h
Name:	MFX3 MOCS 57
ShortName:	MFX3_MOCS_57

Address:	101E8h
Name:	MFX3 MOCS 58
ShortName:	MFX3_MOCS_58

Address:	101ECh
Name:	MFX3 MOCS 59
ShortName:	MFX3_MOCS_59

Address:	101F0h
Name:	MFX3 MOCS 60
ShortName:	MFX3_MOCS_60

Address:	101F4h
Name:	MFX3 MOCS 61
ShortName:	MFX3_MOCS_61

Address:	101F8h
Name:	MFX3 MOCS 62
ShortName:	MFX3_MOCS_62

Address:	101FCh
Name:	MFX3 MOCS 63
ShortName:	MFX3_MOCS_63

MFX3 MOCS register.

DWord	Bit	Description
0	31:19	**Reserved** Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit

MFX3_MOCS - Media3 MOCS Register

		logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service** Default Value: 00b Access: R/W This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec. 00: Value from Private PAT Registers(40E0/40E4/40E8/40EC) 01: Class 1 10: Class 2 11: Class 3
	14	**Reserved**
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is do not care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior)

MFX3_MOCS - Media3 MOCS Register

		1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

Media4 MOCS Register

MFX4_MOCS - Media4 MOCS Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	10200h
Name:	MFX4 MOCS 0
ShortName:	MFX4_MOCS_0
Address:	10204h
Name:	MFX4 MOCS 1
ShortName:	MFX4_MOCS_1
Address:	10208h
Name:	MFX4 MOCS 2
ShortName:	MFX4_MOCS_2
Address:	1020Ch
Name:	MFX4 MOCS 3
ShortName:	MFX4_MOCS_3
Address:	10210h
Name:	MFX4 MOCS 4
ShortName:	MFX4_MOCS_4
Address:	10214h
Name:	MFX4 MOCS 5
ShortName:	MFX4_MOCS_5
Address:	10218h
Name:	MFX4 MOCS 6
ShortName:	MFX4_MOCS_6
Address:	1021Ch
Name:	MFX4 MOCS 7
ShortName:	MFX4_MOCS_7
Address:	10220h
Name:	MFX4 MOCS 8
ShortName:	MFX4_MOCS_8
Address:	10224h

MFX4_MOCS - Media4 MOCS Register	
Name:	MFX4 MOCS 9
ShortName:	MFX4_MOCS_9
Address:	10228h
Name:	MFX4 MOCS 10
ShortName:	MFX4_MOCS_10
Address:	1022Ch
Name:	MFX4 MOCS 11
ShortName:	MFX4_MOCS_11
Address:	10230h
Name:	MFX4 MOCS 12
ShortName:	MFX4_MOCS_12
Address:	10234h
Name:	MFX4 MOCS 13
ShortName:	MFX4_MOCS_13
Address:	10238h
Name:	MFX4 MOCS 14
ShortName:	MFX4_MOCS_14
Address:	1023Ch
Name:	MFX4 MOCS 15
ShortName:	MFX4_MOCS_15
Address:	10240h
Name:	MFX4 MOCS 16
ShortName:	MFX4_MOCS_16
Address:	10244h
Name:	MFX4 MOCS 17
ShortName:	MFX4_MOCS_17
Address:	10248h
Name:	MFX4 MOCS 18
ShortName:	MFX4_MOCS_18
Address:	1024Ch
Name:	MFX4 MOCS 19
ShortName:	MFX4_MOCS_19
Address:	10250h
Name:	MFX4 MOCS 20
ShortName:	MFX4_MOCS_20

MFX4_MOCS - Media4 MOCS Register	
Address:	10254h
Name:	MFX4 MOCS 21
ShortName:	MFX4_MOCS_21
Address:	10258h
Name:	MFX4 MOCS 22
ShortName:	MFX4_MOCS_22
Address:	1025Ch
Name:	MFX4 MOCS 23
ShortName:	MFX4_MOCS_23
Address:	10260h
Name:	MFX4 MOCS 24
ShortName:	MFX4_MOCS_24
Address:	10264h
Name:	MFX4 MOCS 25
ShortName:	MFX4_MOCS_25
Address:	10268h
Name:	MFX4 MOCS 26
ShortName:	MFX4_MOCS_26
Address:	1026Ch
Name:	MFX4 MOCS 27
ShortName:	MFX4_MOCS_27
Address:	10270h
Name:	MFX4 MOCS 28
ShortName:	MFX4_MOCS_28
Address:	10274h
Name:	MFX4 MOCS 29
ShortName:	MFX4_MOCS_29
Address:	10278h
Name:	MFX4 MOCS 30
ShortName:	MFX4_MOCS_30
Address:	1027Ch
Name:	MFX4 MOCS 31
ShortName:	MFX4_MOCS_31
Address:	10280h
Name:	MFX4 MOCS 32

MFX4_MOCS - Media4 MOCS Register	
ShortName:	MFX4_MOCS_32
Address:	10284h
Name:	MFX4 MOCS 33
ShortName:	MFX4_MOCS_33
Address:	10288h
Name:	MFX4 MOCS 34
ShortName:	MFX4_MOCS_34
Address:	1028Ch
Name:	MFX4 MOCS 35
ShortName:	MFX4_MOCS_35
Address:	10290h
Name:	MFX4 MOCS 36
ShortName:	MFX4_MOCS_36
Address:	10294h
Name:	MFX4 MOCS 37
ShortName:	MFX4_MOCS_37
Address:	10298h
Name:	MFX4 MOCS 38
ShortName:	MFX4_MOCS_38
Address:	1029Ch
Name:	MFX4 MOCS 39
ShortName:	MFX4_MOCS_39
Address:	102A0h
Name:	MFX4 MOCS 40
ShortName:	MFX4_MOCS_40
Address:	102A4h
Name:	MFX4 MOCS 41
ShortName:	MFX4_MOCS_41
Address:	102A8h
Name:	MFX4 MOCS 42
ShortName:	MFX4_MOCS_42
Address:	102ACh
Name:	MFX4 MOCS 43
ShortName:	MFX4_MOCS_43

MFX4_MOCS - Media4 MOCS Register	
Address:	102B0h
Name:	MFX4 MOCS 44
ShortName:	MFX4_MOCS_44
Address:	102B4h
Name:	MFX4 MOCS 45
ShortName:	MFX4_MOCS_45
Address:	102B8h
Name:	MFX4 MOCS 46
ShortName:	MFX4_MOCS_46
Address:	102BCh
Name:	MFX4 MOCS 47
ShortName:	MFX4_MOCS_47
Address:	102C0h
Name:	MFX4 MOCS 48
ShortName:	MFX4_MOCS_48
Address:	102C4h
Name:	MFX4 MOCS 49
ShortName:	MFX4_MOCS_49
Address:	102C8h
Name:	MFX4 MOCS 50
ShortName:	MFX4_MOCS_50
Address:	102CCh
Name:	MFX4 MOCS 51
ShortName:	MFX4_MOCS_51
Address:	102D0h
Name:	MFX4 MOCS 52
ShortName:	MFX4_MOCS_52
Address:	102D4h
Name:	MFX4 MOCS 53
ShortName:	MFX4_MOCS_53
Address:	102D8h
Name:	MFX4 MOCS 54
ShortName:	MFX4_MOCS_54
Address:	102DCh
Name:	MFX4 MOCS 55

MFX4_MOCS - Media4 MOCS Register

ShortName:	MFX4_MOCS_55
Address:	102E0h
Name:	MFX4 MOCS 56
ShortName:	MFX4_MOCS_56
Address:	102E4h
Name:	MFX4 MOCS 57
ShortName:	MFX4_MOCS_57
Address:	102E8h
Name:	MFX4 MOCS 58
ShortName:	MFX4_MOCS_58
Address:	102ECh
Name:	MFX4 MOCS 59
ShortName:	MFX4_MOCS_59
Address:	102F0h
Name:	MFX4 MOCS 60
ShortName:	MFX4_MOCS_60
Address:	102F4h
Name:	MFX4 MOCS 61
ShortName:	MFX4_MOCS_61
Address:	102F8h
Name:	MFX4 MOCS 62
ShortName:	MFX4_MOCS_62
Address:	102FCh
Name:	MFX4 MOCS 63
ShortName:	MFX4_MOCS_63

MFX4 MOCS register.

DWord	Bit	Description
0	31:19	**Reserved** Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit

		logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service** Default Value: 00b Access: R/W This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec. 00: Value from Private PAT Registers(40E0/40E4/40E8/40EC) 01: Class 1 10: Class 2 11: Class 3
	14	**Reserved**
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is do not care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior)

		1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

Media5 MOCS Register

MFX5_MOCS - Media5 MOCS Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	10300h
Name:	MFX5 MOCS 0
ShortName:	MFX5_MOCS_0
Address:	10304h
Name:	MFX5 MOCS 1
ShortName:	MFX5_MOCS_1
Address:	10308h
Name:	MFX5 MOCS 2
ShortName:	MFX5_MOCS_2
Address:	1030Ch
Name:	MFX5 MOCS 3
ShortName:	MFX5_MOCS_3
Address:	10310h
Name:	MFX5 MOCS 4
ShortName:	MFX5_MOCS_4
Address:	10314h
Name:	MFX5 MOCS 5
ShortName:	MFX5_MOCS_5
Address:	10318h
Name:	MFX5 MOCS 6
ShortName:	MFX5_MOCS_6
Address:	1031Ch
Name:	MFX5 MOCS 7
ShortName:	MFX5_MOCS_7
Address:	10320h
Name:	MFX5 MOCS 8
ShortName:	MFX5_MOCS_8
Address:	10324h

MFX5_MOCS - Media5 MOCS Register	
Name:	MFX5 MOCS 9
ShortName:	MFX5_MOCS_9
Address:	10328h
Name:	MFX5 MOCS 10
ShortName:	MFX5_MOCS_10
Address:	1032Ch
Name:	MFX5 MOCS 11
ShortName:	MFX5_MOCS_11
Address:	10330h
Name:	MFX5 MOCS 12
ShortName:	MFX5_MOCS_12
Address:	10334h
Name:	MFX5 MOCS 13
ShortName:	MFX5_MOCS_13
Address:	10338h
Name:	MFX5 MOCS 14
ShortName:	MFX5_MOCS_14
Address:	1033Ch
Name:	MFX5 MOCS 15
ShortName:	MFX5_MOCS_15
Address:	10340h
Name:	MFX5 MOCS 16
ShortName:	MFX5_MOCS_16
Address:	10344h
Name:	MFX5 MOCS 17
ShortName:	MFX5_MOCS_17
Address:	10348h
Name:	MFX5 MOCS 18
ShortName:	MFX5_MOCS_18
Address:	1034Ch
Name:	MFX5 MOCS 19
ShortName:	MFX5_MOCS_19
Address:	10350h
Name:	MFX5 MOCS 20
ShortName:	MFX5_MOCS_20

MFX5_MOCS - Media5 MOCS Register	
Address:	10354h
Name:	MFX5 MOCS 21
ShortName:	MFX5_MOCS_21
Address:	10358h
Name:	MFX5 MOCS 22
ShortName:	MFX5_MOCS_22
Address:	1035Ch
Name:	MFX5 MOCS 23
ShortName:	MFX5_MOCS_23
Address:	10360h
Name:	MFX5 MOCS 24
ShortName:	MFX5_MOCS_24
Address:	10364h
Name:	MFX5 MOCS 25
ShortName:	MFX5_MOCS_25
Address:	10368h
Name:	MFX5 MOCS 26
ShortName:	MFX5_MOCS_26
Address:	1036Ch
Name:	MFX5 MOCS 27
ShortName:	MFX5_MOCS_27
Address:	10370h
Name:	MFX5 MOCS 28
ShortName:	MFX5_MOCS_28
Address:	10374h
Name:	MFX5 MOCS 29
ShortName:	MFX5_MOCS_29
Address:	10378h
Name:	MFX5 MOCS 30
ShortName:	MFX5_MOCS_30
Address:	1037Ch
Name:	MFX5 MOCS 31
ShortName:	MFX5_MOCS_31
Address:	10380h
Name:	MFX5 MOCS 32

MFX5_MOCS - Media5 MOCS Register	
ShortName:	MFX5_MOCS_32
Address:	10384h
Name:	MFX5 MOCS 33
ShortName:	MFX5_MOCS_33
Address:	10388h
Name:	MFX5 MOCS 34
ShortName:	MFX5_MOCS_34
Address:	1038Ch
Name:	MFX5 MOCS 35
ShortName:	MFX5_MOCS_35
Address:	10390h
Name:	MFX5 MOCS 36
ShortName:	MFX5_MOCS_36
Address:	10394h
Name:	MFX5 MOCS 37
ShortName:	MFX5_MOCS_37
Address:	10398h
Name:	MFX5 MOCS 38
ShortName:	MFX5_MOCS_38
Address:	1039Ch
Name:	MFX5 MOCS 39
ShortName:	MFX5_MOCS_39
Address:	103A0h
Name:	MFX5 MOCS 40
ShortName:	MFX5_MOCS_40
Address:	103A4h
Name:	MFX5 MOCS 41
ShortName:	MFX5_MOCS_41
Address:	103A8h
Name:	MFX5 MOCS 42
ShortName:	MFX5_MOCS_42
Address:	103ACh
Name:	MFX5 MOCS 43
ShortName:	MFX5_MOCS_43

MFX5_MOCS - Media5 MOCS Register	
Address:	103B0h
Name:	MFX5 MOCS 44
ShortName:	MFX5_MOCS_44
Address:	103B4h
Name:	MFX5 MOCS 45
ShortName:	MFX5_MOCS_45
Address:	103B8h
Name:	MFX5 MOCS 46
ShortName:	MFX5_MOCS_46
Address:	103BCh
Name:	MFX5 MOCS 47
ShortName:	MFX5_MOCS_47
Address:	103C0h
Name:	MFX5 MOCS 48
ShortName:	MFX5_MOCS_48
Address:	103C4h
Name:	MFX5 MOCS 49
ShortName:	MFX5_MOCS_49
Address:	103C8h
Name:	MFX5 MOCS 50
ShortName:	MFX5_MOCS_50
Address:	103CCh
Name:	MFX5 MOCS 51
ShortName:	MFX5_MOCS_51
Address:	103D0h
Name:	MFX5 MOCS 52
ShortName:	MFX5_MOCS_52
Address:	103D4h
Name:	MFX5 MOCS 53
ShortName:	MFX5_MOCS_53
Address:	103D8h
Name:	MFX5 MOCS 54
ShortName:	MFX5_MOCS_54
Address:	103DCh
Name:	MFX5 MOCS 55

MFX5_MOCS - Media5 MOCS Register

ShortName:	MFX5_MOCS_55

Address:	103E0h
Name:	MFX5 MOCS 56
ShortName:	MFX5_MOCS_56

Address:	103E4h
Name:	MFX5 MOCS 57
ShortName:	MFX5_MOCS_57

Address:	103E8h
Name:	MFX5 MOCS 58
ShortName:	MFX5_MOCS_58

Address:	103ECh
Name:	MFX5 MOCS 59
ShortName:	MFX5_MOCS_59

Address:	103F0h
Name:	MFX5 MOCS 60
ShortName:	MFX5_MOCS_60

Address:	103F4h
Name:	MFX5 MOCS 61
ShortName:	MFX5_MOCS_61

Address:	103F8h
Name:	MFX5 MOCS 62
ShortName:	MFX5_MOCS_62

Address:	103FCh
Name:	MFX5 MOCS 63
ShortName:	MFX5_MOCS_63

MFX5 MOCS register.

DWord	Bit	Description
0	31:19	**Reserved** Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit

		logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service** Default Value: 00b Access: R/W This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec. 00: Value from Private PAT Registers(40E0/40E4/40E8/40EC) 01: Class 1 10: Class 2 11: Class 3
	14	**Reserved**
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is do not care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior)

		1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

Media6 MOCS Register

MFX6_MOCS - Media6 MOCS Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	10400h
Name:	MFX6 MOCS 0
ShortName:	MFX6_MOCS_0
Address:	10404h
Name:	MFX6 MOCS 1
ShortName:	MFX6_MOCS_1
Address:	10408h
Name:	MFX6 MOCS 2
ShortName:	MFX6_MOCS_2
Address:	1040Ch
Name:	MFX6 MOCS 3
ShortName:	MFX6_MOCS_3
Address:	10410h
Name:	MFX6 MOCS 4
ShortName:	MFX6_MOCS_4
Address:	10414h
Name:	MFX6 MOCS 5
ShortName:	MFX6_MOCS_5
Address:	10418h
Name:	MFX6 MOCS 6
ShortName:	MFX6_MOCS_6
Address:	1041Ch
Name:	MFX6 MOCS 7
ShortName:	MFX6_MOCS_7
Address:	10420h
Name:	MFX6 MOCS 8
ShortName:	MFX6_MOCS_8
Address:	10424h

MFX6_MOCS - Media6 MOCS Register	
Name:	MFX6 MOCS 9
ShortName:	MFX6_MOCS_9
Address:	10428h
Name:	MFX6 MOCS 10
ShortName:	MFX6_MOCS_10
Address:	1042Ch
Name:	MFX6 MOCS 11
ShortName:	MFX6_MOCS_11
Address:	10430h
Name:	MFX6 MOCS 12
ShortName:	MFX6_MOCS_12
Address:	10434h
Name:	MFX6 MOCS 13
ShortName:	MFX6_MOCS_13
Address:	10438h
Name:	MFX6 MOCS 14
ShortName:	MFX6_MOCS_14
Address:	1043Ch
Name:	MFX6 MOCS 15
ShortName:	MFX6_MOCS_15
Address:	10440h
Name:	MFX6 MOCS 16
ShortName:	MFX6_MOCS_16
Address:	10444h
Name:	MFX6 MOCS 17
ShortName:	MFX6_MOCS_17
Address:	10448h
Name:	MFX6 MOCS 18
ShortName:	MFX6_MOCS_18
Address:	1044Ch
Name:	MFX6 MOCS 19
ShortName:	MFX6_MOCS_19
Address:	10450h
Name:	MFX6 MOCS 20
ShortName:	MFX6_MOCS_20

MFX6_MOCS - Media6 MOCS Register	
Address:	10454h
Name:	MFX6 MOCS 21
ShortName:	MFX6_MOCS_21
Address:	10458h
Name:	MFX6 MOCS 22
ShortName:	MFX6_MOCS_22
Address:	1045Ch
Name:	MFX6 MOCS 23
ShortName:	MFX6_MOCS_23
Address:	10460h
Name:	MFX6 MOCS 24
ShortName:	MFX6_MOCS_24
Address:	10464h
Name:	MFX6 MOCS 25
ShortName:	MFX6_MOCS_25
Address:	10468h
Name:	MFX6 MOCS 26
ShortName:	MFX6_MOCS_26
Address:	1046Ch
Name:	MFX6 MOCS 27
ShortName:	MFX6_MOCS_27
Address:	10470h
Name:	MFX6 MOCS 28
ShortName:	MFX6_MOCS_28
Address:	10474h
Name:	MFX6 MOCS 29
ShortName:	MFX6_MOCS_29
Address:	10478h
Name:	MFX6 MOCS 30
ShortName:	MFX6_MOCS_30
Address:	1047Ch
Name:	MFX6 MOCS 31
ShortName:	MFX6_MOCS_31
Address:	10480h
Name:	MFX6 MOCS 32

MFX6_MOCS - Media6 MOCS Register	
ShortName:	MFX6_MOCS_32
Address:	10484h
Name:	MFX6 MOCS 33
ShortName:	MFX6_MOCS_33
Address:	10488h
Name:	MFX6 MOCS 34
ShortName:	MFX6_MOCS_34
Address:	1048Ch
Name:	MFX6 MOCS 35
ShortName:	MFX6_MOCS_35
Address:	10490h
Name:	MFX6 MOCS 36
ShortName:	MFX6_MOCS_36
Address:	10494h
Name:	MFX6 MOCS 37
ShortName:	MFX6_MOCS_37
Address:	10498h
Name:	MFX6 MOCS 38
ShortName:	MFX6_MOCS_38
Address:	1049Ch
Name:	MFX6 MOCS 39
ShortName:	MFX6_MOCS_39
Address:	104A0h
Name:	MFX6 MOCS 40
ShortName:	MFX6_MOCS_40
Address:	104A4h
Name:	MFX6 MOCS 41
ShortName:	MFX6_MOCS_41
Address:	104A8h
Name:	MFX6 MOCS 42
ShortName:	MFX6_MOCS_42
Address:	104ACh
Name:	MFX6 MOCS 43
ShortName:	MFX6_MOCS_43

MFX6_MOCS - Media6 MOCS Register	
Address:	104B0h
Name:	MFX6 MOCS 44
ShortName:	MFX6_MOCS_44
Address:	104B4h
Name:	MFX6 MOCS 45
ShortName:	MFX6_MOCS_45
Address:	104B8h
Name:	MFX6 MOCS 46
ShortName:	MFX6_MOCS_46
Address:	104BCh
Name:	MFX6 MOCS 47
ShortName:	MFX6_MOCS_47
Address:	104C0h
Name:	MFX6 MOCS 48
ShortName:	MFX6_MOCS_48
Address:	104C4h
Name:	MFX6 MOCS 49
ShortName:	MFX6_MOCS_49
Address:	104C8h
Name:	MFX6 MOCS 50
ShortName:	MFX6_MOCS_50
Address:	104CCh
Name:	MFX6 MOCS 51
ShortName:	MFX6_MOCS_51
Address:	104D0h
Name:	MFX6 MOCS 52
ShortName:	MFX6_MOCS_52
Address:	104D4h
Name:	MFX6 MOCS 53
ShortName:	MFX6_MOCS_53
Address:	104D8h
Name:	MFX6 MOCS 54
ShortName:	MFX6_MOCS_54
Address:	104DCh
Name:	MFX6 MOCS 55

MFX6_MOCS - Media6 MOCS Register

ShortName:	MFX6_MOCS_55

Address:	104E0h
Name:	MFX6 MOCS 56
ShortName:	MFX6_MOCS_56

Address:	104E4h
Name:	MFX6 MOCS 57
ShortName:	MFX6_MOCS_57

Address:	104E8h
Name:	MFX6 MOCS 58
ShortName:	MFX6_MOCS_58

Address:	104ECh
Name:	MFX6 MOCS 59
ShortName:	MFX6_MOCS_59

Address:	104F0h
Name:	MFX6 MOCS 60
ShortName:	MFX6_MOCS_60

Address:	104F4h
Name:	MFX6 MOCS 61
ShortName:	MFX6_MOCS_61

Address:	104F8h
Name:	MFX6 MOCS 62
ShortName:	MFX6_MOCS_62

Address:	104FCh
Name:	MFX6 MOCS 63
ShortName:	MFX6_MOCS_63

MFX6 MOCS register.

DWord	Bit	Description
0	31:19	**Reserved** Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit

		logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service** Default Value: 00b Access: R/W This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec. 00: Value from Private PAT Registers(40E0/40E4/40E8/40EC) 01: Class 1 10: Class 2 11: Class 3
	14	**Reserved**
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is do not care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior)

		1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

Media7 MOCS Register

MFX7_MOCS - Media7 MOCS Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	10500h
Name:	MFX7 MOCS 0
ShortName:	MFX7_MOCS_0
Address:	10504h
Name:	MFX7 MOCS 1
ShortName:	MFX7_MOCS_1
Address:	10508h
Name:	MFX7 MOCS 2
ShortName:	MFX7_MOCS_2
Address:	1050Ch
Name:	MFX7 MOCS 3
ShortName:	MFX7_MOCS_3
Address:	10510h
Name:	MFX7 MOCS 4
ShortName:	MFX7_MOCS_4
Address:	10514h
Name:	MFX7 MOCS 5
ShortName:	MFX7_MOCS_5
Address:	10518h
Name:	MFX7 MOCS 6
ShortName:	MFX7_MOCS_6
Address:	1051Ch
Name:	MFX7 MOCS 7
ShortName:	MFX7_MOCS_7
Address:	10520h
Name:	MFX7 MOCS 8
ShortName:	MFX7_MOCS_8
Address:	10524h

MFX7_MOCS - Media7 MOCS Register	
Name:	MFX7 MOCS 9
ShortName:	MFX7_MOCS_9
Address:	10528h
Name:	MFX7 MOCS 10
ShortName:	MFX7_MOCS_10
Address:	1052Ch
Name:	MFX7 MOCS 11
ShortName:	MFX7_MOCS_11
Address:	10530h
Name:	MFX7 MOCS 12
ShortName:	MFX7_MOCS_12
Address:	10534h
Name:	MFX7 MOCS 13
ShortName:	MFX7_MOCS_13
Address:	10538h
Name:	MFX7 MOCS 14
ShortName:	MFX7_MOCS_14
Address:	1053Ch
Name:	MFX7 MOCS 15
ShortName:	MFX7_MOCS_15
Address:	10540h
Name:	MFX7 MOCS 16
ShortName:	MFX7_MOCS_16
Address:	10544h
Name:	MFX7 MOCS 17
ShortName:	MFX7_MOCS_17
Address:	10548h
Name:	MFX7 MOCS 18
ShortName:	MFX7_MOCS_18
Address:	1054Ch
Name:	MFX7 MOCS 19
ShortName:	MFX7_MOCS_19
Address:	10550h
Name:	MFX7 MOCS 20
ShortName:	MFX7_MOCS_20

MFX7_MOCS - Media7 MOCS Register	
Address:	10554h
Name:	MFX7 MOCS 21
ShortName:	MFX7_MOCS_21
Address:	10558h
Name:	MFX7 MOCS 22
ShortName:	MFX7_MOCS_22
Address:	1055Ch
Name:	MFX7 MOCS 23
ShortName:	MFX7_MOCS_23
Address:	10560h
Name:	MFX7 MOCS 24
ShortName:	MFX7_MOCS_24
Address:	10564h
Name:	MFX7 MOCS 25
ShortName:	MFX7_MOCS_25
Address:	10568h
Name:	MFX7 MOCS 26
ShortName:	MFX7_MOCS_26
Address:	1056Ch
Name:	MFX7 MOCS 27
ShortName:	MFX7_MOCS_27
Address:	10570h
Name:	MFX7 MOCS 28
ShortName:	MFX7_MOCS_28
Address:	10574h
Name:	MFX7 MOCS 29
ShortName:	MFX7_MOCS_29
Address:	10578h
Name:	MFX7 MOCS 30
ShortName:	MFX7_MOCS_30
Address:	1057Ch
Name:	MFX7 MOCS 31
ShortName:	MFX7_MOCS_31
Address:	10580h
Name:	MFX7 MOCS 32

MFX7_MOCS - Media7 MOCS Register	
ShortName:	MFX7_MOCS_32
Address:	10584h
Name:	MFX7 MOCS 33
ShortName:	MFX7_MOCS_33
Address:	10588h
Name:	MFX7 MOCS 34
ShortName:	MFX7_MOCS_34
Address:	1058Ch
Name:	MFX7 MOCS 35
ShortName:	MFX7_MOCS_35
Address:	10590h
Name:	MFX7 MOCS 36
ShortName:	MFX7_MOCS_36
Address:	10594h
Name:	MFX7 MOCS 37
ShortName:	MFX7_MOCS_37
Address:	10598h
Name:	MFX7 MOCS 38
ShortName:	MFX7_MOCS_38
Address:	1059Ch
Name:	MFX7 MOCS 39
ShortName:	MFX7_MOCS_39
Address:	105A0h
Name:	MFX7 MOCS 40
ShortName:	MFX7_MOCS_40
Address:	105A4h
Name:	MFX7 MOCS 41
ShortName:	MFX7_MOCS_41
Address:	105A8h
Name:	MFX7 MOCS 42
ShortName:	MFX7_MOCS_42
Address:	105ACh
Name:	MFX7 MOCS 43
ShortName:	MFX7_MOCS_43

MFX7_MOCS - Media7 MOCS Register	
Address:	105B0h
Name:	MFX7 MOCS 44
ShortName:	MFX7_MOCS_44
Address:	105B4h
Name:	MFX7 MOCS 45
ShortName:	MFX7_MOCS_45
Address:	105B8h
Name:	MFX7 MOCS 46
ShortName:	MFX7_MOCS_46
Address:	105BCh
Name:	MFX7 MOCS 47
ShortName:	MFX7_MOCS_47
Address:	105C0h
Name:	MFX7 MOCS 48
ShortName:	MFX7_MOCS_48
Address:	105C4h
Name:	MFX7 MOCS 49
ShortName:	MFX7_MOCS_49
Address:	105C8h
Name:	MFX7 MOCS 50
ShortName:	MFX7_MOCS_50
Address:	105CCh
Name:	MFX7 MOCS 51
ShortName:	MFX7_MOCS_51
Address:	105D0h
Name:	MFX7 MOCS 52
ShortName:	MFX7_MOCS_52
Address:	105D4h
Name:	MFX7 MOCS 53
ShortName:	MFX7_MOCS_53
Address:	105D8h
Name:	MFX7 MOCS 54
ShortName:	MFX7_MOCS_54
Address:	105DCh
Name:	MFX7 MOCS 55

MFX7_MOCS - Media7 MOCS Register

ShortName:	MFX7_MOCS_55

Address:	105E0h
Name:	MFX7 MOCS 56
ShortName:	MFX7_MOCS_56

Address:	105E4h
Name:	MFX7 MOCS 57
ShortName:	MFX7_MOCS_57

Address:	105E8h
Name:	MFX7 MOCS 58
ShortName:	MFX7_MOCS_58

Address:	105ECh
Name:	MFX7 MOCS 59
ShortName:	MFX7_MOCS_59

Address:	105F0h
Name:	MFX7 MOCS 60
ShortName:	MFX7_MOCS_60

Address:	105F4h
Name:	MFX7 MOCS 61
ShortName:	MFX7_MOCS_61

Address:	105F8h
Name:	MFX7 MOCS 62
ShortName:	MFX7_MOCS_62

Address:	105FCh
Name:	MFX7 MOCS 63
ShortName:	MFX7_MOCS_63

MFX7 MOCS register.

DWord	Bit	Description
0	31:19	**Reserved** Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit

		logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service** Default Value: 00b Access: R/W This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec. 00: Value from Private PAT Registers(40E0/40E4/40E8/40EC) 01: Class 1 10: Class 2 11: Class 3
	14	**Reserved**
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is do not care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior)

		1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

MEDIA Clock Gating Messages

MEDCGMSG - MEDIA Clock Gating Messages

Register Space: MMIO: 0/2/0

Source: BSpec

Size (in bits): 32

Address: 08118h

MEDIA Clock Gating Messages Register

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO **Programming Notes** **Message Mask** To write to bits 15:0, the corresponding message mask bits must be written. For example, to set bit 14, bit 30 needs to be 1 : 40004000.
	15:12	**SFC Clock Gating Control Message** Access: R/W 0 – SFC Clock Un-gate Request: Setting the SFC Clock Gating Control Message to zero (0) un-gates the cmclk clock in the 1st Media block. Bit12 : SFC (csfcclk) clock gate control for vesfcbox0 Bit13 : SFC (csfcclk) clock gate control for vesfcbox1 Bit14 : SFC (csfcclk) clock gate control for vesfcbox2 Bit15 : SFC (csfcclk) clock gate control for vesfcbox3 1 – SFC Clock Gate Request: Setting the SFC Clock Gating Control Message to one (1) gates the cmclk clock in the 1st Media block.
	11:8	**VEbox Clock Gating Control message** Access: R/W 0 – VEbox Clock Un-gate Request: Setting the VEbox Clock Gating Control Message to zero (0) un-gates the cvclk clock. Bit8 : vebox(cvclk) clock gate control for vesfcbox0 Bit9 : vebox(cvclk) clock gate control for vesfcbox1

MEDCGMSG - MEDIA Clock Gating Messages

				Bit10 : vebox(cvclk) clock gate control for vesfcbox2 Bit11 : vebox(cvclk) clock gate control for vesfcbox3
		1	VEbox Clock Gate Request	Setting the VEbox Clock Gating Control Message to one (1) gates the cvclk clock.

7:0 **Media Clock Gating Control Message**

Access:	R/W

Value	Name	Description
0	Media Clock Un-gate Request	Setting the Media Clock Gating Control Message to zero (0) un-gates the cmclk clock. Bit0 : media(cmclk) clock gate control for vdbox0 Bit1 : media(cmclk) clock gate control for vdbox1 Bit2 : media(cmclk) clock gate control for vdbox2 Bit3 : media(cmclk) clock gate control for vdbox3 Bit4 : media(cmclk) clock gate control for vdbox4 Bit5 : media(cmclk) clock gate control for vdbox5 Bit6 : media(cmclk) clock gate control for vdbox6 Bit7 : media(cmclk) clock gate control for vdbox7
1	Media Clock Gate Request	Setting the Media Clock Gating Control Message to one (1) gates the cmclk clock.

Media Control Surface Cache Invalidate

MCSCI - Media Control Surface Cache Invalidate

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	04AACh

Description

This register can be used by SW to invalidate the RCP/WCP caches for a particular engine, asynchronous to batch execution.
When using this register based invalidation, SW must ensure the pipeline for the engine for which the invalidation is being issued is flushed, and the engine is idle.

DWord	Bit	Description
0	31:16	**Bit Masks** Default Value: 0000h Access: R/W Mask Bits act as Write Enables for the bits[15:0] of this register
	15	**Disable H/W based RCP$/WCP$ cache invalidate** Default Value: 0b Access: R/W Disable H/W based end of context detection Bit[15] Disable H/W based RCP$/WCP$ cache invalidation 1'b1 : Disable the h/w based end of context detection to clear the contents of RCP$ and WCP$ 1'b0 : Does not disable the h/w based end of context detection
	14	**Reserved_14** Default Value: 0b Access: R/W
	13	**Reserved_13** Default Value: 0b Access: R/W
	12	**Reserved_12** Default Value: 0b Access: R/W

MCSCI - Media Control Surface Cache Invalidate

	11	**Reserved_11** Default Value: 0b Access: R/W
	10	**Reserved_10** Default Value: 0b Access: R/W
	9	**Reserved_9** Default Value: 0b Access: R/W
	8	**Reserved_8** Default Value: 0b Access: R/W
	7	**Reserved_7** Default Value: 0b Access: R/W
	6	**Reserved_6** Default Value: 0b Access: R/W
	5	**Reserved_5** Default Value: 0b Access: R/W
	4	**Invalidate WIDI WCP$/RCP$ entries** Default Value: 0b Access: R/W Hardware Clear Invalidate WIDI WCP$/RCP$ entries Bit[4] Clear WIDI engine enqueued entries from WCP$/RCP$ 1'b0 : Enqueued entries from WCP$/RCP$ are not cleared; 1'b1 : Enqueued entries from WCP$/RCP$ are cleared This event is instantaneous This bit is write-to-clear
	3	**Invalidate Media#1 WCP$/RCP$ entries** Default Value: 0b Access: R/W Hardware Clear Invalidate Media#1 WCP$/RCP$ entries Bit[3] Clear Media#1 engine enqueued entries from WCP$/RCP$

		1'b0 : Enqueued entries from WCP$/RCP$ are not cleared; 1'b1 : Enqueued entries from WCP$/RCP$ are cleared This event is instantaneous This bit is write-to-clear
	2	**Invalidate Media#0 WCP$/RCP$ entries** Default Value: 0b Access: R/W Hardware Clear Invalidate Media#0 WCP$/RCP$ entries Bit[2] Clear Media#0 engine enqueued entries from WCP$/RCP$ 1'b0 : Enqueued entries from WCP$/RCP$ are not cleared; 1'b1 : Enqueued entries from WCP$/RCP$ are cleared This event is instantaneous This bit is write-to-clear
	1	**Invalidate VEBOX WCP$/RCP$ entries** Default Value: 0b Access: R/W Hardware Clear Invalidate VEBOX WCP$/RCP$ entries Bit[1] Clear VEBOX engine enqueued entries from WCP$/RCP$ 1'b0 : Enqueued entries from WCP$/RCP$ are not cleared; 1'b1 : Enqueued entries from WCP$/RCP$ are cleared This event is instantaneous This bit is write-to-clear
	0	**Invalidate Render(When used for Media) WCP$/RCP$ entries** Default Value: 0b Access: R/W Hardware Clear Invalidate Render WCP$/RCP$ entries Bit[0] Clear Render engine enqueued entries from WCP$/RCP$ 1'b0 : Enqueued entries from WCP$/RCP$ are not cleared; 1'b1 : Enqueued entries from WCP$/RCP$ are cleared This event is instantaneous This bit is write-to-clear

Media Die Recovery

MED_DIE_RECOVERY - Media Die Recovery

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	12298h
Name:	VCS Media Die Recovery
ShortName:	VCS_MED_DIE_RECOVERY

This register is stored in the VCS but is used in the HWM unit. This register programs the die recovery override and engine ID's.

DWord	Bit	Description
0	31:12	**Reserved** Access: RO
	11:9	**Forced Next Engine ID** Access: R/W This field is the next engine ID.
	8	**Force Next Engine ID** Access: R/W The bit forces the next engine ID.
	7:4	**Reserved** Access: RO
	3:1	**Forced Previous Engine ID** Access: R/W This field is the previous engine ID.
	0	**Force Previous Engine ID** Access: R/W The bit forces the previous engine ID.

Media FIFO Messaging Register for Shadow Register Unit

MSG_FIFO_MGSR_MEDIA - Media FIFO Messaging Register for Shadow Register Unit

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	080E4h
Name:	Media FIFO Messaging Register for Shadow Register Unit
ShortName:	MSG_FIFO_MGSR_MEDIA

Register that has the ACK information, back from MGSR as to whether a specific VD/VE Box has been blocked/unblocked
0 -- Box has been blocked
1 -- Box has been unblocked
Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].
To set bit0, for example, the data would be 0x0001_0001.
To clear bit0, for example, the data would be 0x0001_0000.
Note that mask bit is the data bit offset + 16.
Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description
0	31:12	**Reserved** Access: RO
	11	**Acknowledge that Media FIFO has been Blocked for VEBOX3** Access: R/W Acknowledge that MEDIA FIFO has been Blocked for VEBOX3 1'b0 : Media FIFO Block Ack for VEBOX3(default) 1'b1 : Media FIFO Unblock Ack VEBOX3 Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.
	10	**Acknowledge that Media FIFO has been Blocked for VEBOX2** Access: R/W Acknowledge that MEDIA FIFO has been Blocked for VEBOX2 1'b0 : Media FIFO Block Ack for VEBOX2(default) 1'b1 : Media FIFO Unblock Ack VEBOX2 Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.

MSG_FIFO_MGSR_MEDIA - Media FIFO Messaging Register for Shadow Register Unit

	9	**Acknowledge that Media FIFO has been Blocked for VEBOX1** Access: R/W Acknowledge that MEDIA FIFO has been Blocked for VEBOX1 1'b0 : Media FIFO Block Ack for VEBOX1(default) 1'b1 : Media FIFO Unblock Ack VEBOX1 Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.
	8	**Acknowledge that Media FIFO has been Blocked for VEBOX0** Access: R/W Acknowledge that MEDIA FIFO has been Blocked for VEBOX0 1'b0 : Media FIFO Block Ack for VEBOX0(default) 1'b1 : Media FIFO Unblock Ack VEBOX0 Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.
	7	**Acknowledge that Media FIFO has been Blocked for VDBOX7** Access: R/W Acknowledge that MEDIA FIFO has been Blocked for VDBOX7 1'b0 : Media FIFO Block Ack for VDBOX7(default) 1'b1 : Media FIFO Unblock Ack VDBOX7 Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.
	6	**Acknowledge that Media FIFO has been Blocked for VDBOX6** Access: R/W Acknowledge that MEDIA FIFO has been Blocked for VDBOX6 1'b0 : Media FIFO Block Ack for VDBOX6(default) 1'b1 : Media FIFO Unblock Ack VDBOX6 Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.
	5	**Acknowledge that Media FIFO has been Blocked for VDBOX5** Access: R/W Acknowledge that MEDIA FIFO has been Blocked for VDBOX5 1'b0 : Media FIFO Block Ack for VDBOX5(default) 1'b1 : Media FIFO Unblock Ack VDBOX5 Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.

MSG_FIFO_MGSR_MEDIA - Media FIFO Messaging Register for Shadow Register Unit

	4	**Acknowledge that Media FIFO has been Blocked for VDBOX4** Access: R/W Acknowledge that MEDIA FIFO has been Blocked for VDBOX4 1'b0 : Media FIFO Block Ack for VDBOX4(default) 1'b1 : Media FIFO Unblock Ack VDBOX4 Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.
	3	**Acknowledge that Media FIFO has been Blocked for VDBOX3** Access: R/W Acknowledge that MEDIA FIFO has been Blocked for VDBOX3 1'b0 : Media FIFO Block Ack for VDBOX3(default) 1'b1 : Media FIFO Unblock Ack VDBOX3 Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.
	2	**Acknowledge that Media FIFO has been Blocked for VDBOX2** Access: R/W Acknowledge that MEDIA FIFO has been Blocked for VDBOX2 1'b0 : Media FIFO Block Ack for VDBOX2(default) 1'b1 : Media FIFO Unblock Ack VDBOX2 Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.
	1	**Acknowledge that Media FIFO has been Blocked for VDBOX1** Access: R/W Acknowledge that MEDIA FIFO has been Blocked for VDBOX1 1'b0 : Media FIFO Block Ack for VDBOX1(default) 1'b1 : Media FIFO Unblock Ack VDBOX1 Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.
	0	**Acknowledge that Media FIFO has been Blocked for VDBOX0** Access: R/W Acknowledge that MEDIA FIFO has been Blocked for VDBOX0 1'b0 : Media FIFO Block Ack for VDBOX0(default) 1'b1 : Media FIFO Unblock Ack VDBOX0 Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.

Media unit Level Clock Gating override during rstflow 94B0

MEDMISCCP94B0 - Media unit Level Clock Gating override during rstflow 94B0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	094B0h

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31:1	**Reserved** Access: R/W Reserved
	0	**misccp Clock Gating Disable during rstflow** Access: R/W misccp Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) w/a for A-step would be to make BIOS to write value 1 to this bit for power-on.

Messaging Register for GPMunit

MSG_GPM - Messaging Register for GPMunit

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00C00h

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].
To set bit0, for example, the data would be 0x0001_0001.
To clear bit0, for example, the data would be 0x0001_0000.
Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO
	15	**GPM Messages Bit 15** Access: R/W Placeholder for GPM Messages. RPMunit could self-clear these bits upon sampling.
	14	**GPM Messages Bit 14** Access: R/W Placeholder for GPM Messages. RPMunit could self-clear these bits upon sampling.
	13	**GPM Messages Bit 13** Access: R/W Placeholder for GPM Messages. RPMunit could self-clear these bits upon sampling.
	12	**GPM Messages Bit 12** Access: R/W Placeholder for GPM Messages. RPMunit could self-clear these bits upon sampling.
	11	**GPM Messages Bit 11** Access: R/W Placeholder for GPM Messages.

MSG_GPM - Messaging Register for GPMunit

		RPMunit could self-clear these bits upon sampling.
	10	**GPM Messages Bit 10** Access: R/W Placeholder for GPM Messages. RPMunit could self-clear these bits upon sampling.
	9	**GPM Messages Bit 9** Access: R/W Placeholder for GPM Messages. RPMunit could self-clear these bits upon sampling.
	8	**GPM Messages Bit 8** Access: R/W Placeholder for GPM Messages. RPMunit could self-clear these bits upon sampling.
	7	**Media PowerGate License Request** Access: R/W GPMunit Media PG License Level Request 1'b1 : Media PG ON License Request 1'b0 : Media PG OFF License Request
	6:5	**ICCP Low Level Request** Access: R/W GPMunit IccP License Level Request 2'b00 : Low IccP License Request (default) 2'b01 : High IccP License Request
	4	**Request to send CPD Exit Ack Message on EventBus (U2C)** Access: R/W Request from GPMunit for RPMunit to send CPD_EXIT_ACK message on the Eventbus. RPMunit self-clears this bit upon sampling.
	3	**Request to send CPD Enter Ack Message on EventBus (U2C)** Access: R/W Request from GPMunit for RPMunit to send CPD_ENTER_ACK message on the Eventbus. RPMunit self-clears this bit upon sampling.
	2	**Request to send Credit Active Deassert Message on EventBus (U2C)** Access: R/W

MSG_GPM - Messaging Register for GPMunit		
		Request from GPMunit for RPMunit to send CREDIT_ACTIVE_DEASSERT message on the Eventbus. RPMunit self-clears this bit upon sampling.
	1	**Request to send Credit Active Assert Message on EventBus (U2C)** Access: R/W Request from GPMunit for RPMunit to send CREDIT_ACTIVE_ASSERT message on the Eventbus. RPMunit self-clears this bit upon sampling.
	0	**Request to send IDI Shutdown Ack Message on EventBus (U2C)** Access: R/W Request from GPMunit for RPMunit to send IDI_SHUTDOWN_ACK message on the Eventbus. RPMunit self-clears this bit upon sampling.

Messaging Register for MDRBunit

MSG_MDRB - Messaging Register for MDRBunit

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00C08h

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].
To set bit0, for example, the data would be 0x0001_0001.
To clear bit0, for example, the data would be 0x0001_0000.
Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO
	15:6	**MDRB Messages** Access: R/W Placeholder for MDRB Messages. MDRBunit could self-clear these bits upon sampling.
	5	**RFO's are pending after Context Restore is Complete** Access: R/W There are RFO's pending even after Context Restore process is complete for MDRB RFO's are pending = 1'b1 There are no RFO's pending = 1'b0
	4	**Context Restore is Complete** Access: R/W The Context Restore process is complete for MDRB Context Restore is Done = 1'b1 Context Restore is not yet complete = 1'b0
	3	**RFO's are pending after Context Save is Complete** Access: R/W There are RFO's pending even after Context Save process is complete for MDRB RFO's are pending = 1'b1 There are no RFO's pending = 1'b0

MSG_MDRB - Messaging Register for MDRBunit

	2	**Context Save is Complete** Access: R/W The Context Save process is complete for MDRB Context Save is Done = 1'b1 Context Save is not yet complete = 1'b0
	1	**RFO Enable/Disable Ack for RPM (internal) RFO Request** Access: R/W RFO Enable/Disable Ack for Internal RFO Request. Enable Ack = 1'b1 Disable Ack = 1'b0
	0	**RFO Enable/Disable Ack for U2C (Evtentbus) RFO Request** Default Value: 0b Access: R/W RFO Enable/Disable Ack for U2C RFO Request. Enable Ack = 1'b1 Disable Ack = 1'b0

Messaging Register for MGSRunit

MSG_MGSR - Messaging Register for MGSRunit

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00C04h

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].
To set bit0, for example, the data would be 0x0001_0001.
To clear bit0, for example, the data would be 0x0001_0000.
Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO
	15:0	**MGSR Messages** Access: R/W Placeholder for MGSR Messages. MGSRunit could self-clear these bits upon sampling.

Messaging Register for SPCunit

MSG_SPC - Messaging Register for SPCunit

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00C10h

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].
To set bit0, for example, the data would be 0x0001_0001.
To clear bit0, for example, the data would be 0x0001_0000.
Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description
0	31:1	**Reserved** Access: RO
	0	**SPC GTI PGCTL ACK** Access: R/W SPC PowerGate Control Ack Message 1'b0 : PowerDown Ack (default). 1'b1 : PowerUp Ack (default).

MFC_AVC_CABAC_INSERTION_COUNT

AVC_CABAC_INSERTION_COUNT - MFC_AVC_CABAC_INSERTION_COUNT	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	128ACh

This register stores the count in bytes of **CABAC ZERO_WORD insertion. It is primarily provided for statistical data gathering.**

DWord	Bit	Description
0	31:0	**MFC AVC Cabac Insertion Count** Total number of bytes in the bitstream output before for the CABAC zero word insertion. This count is updated each time when the insertion count is incremented.

MFC_AVC Bitstream Decoding Front-End Parsing Logic Error Counter

MFC_VIN_AVD_ERROR_CNTR - MFC_AVC Bitstream Decoding Front-End Parsing Logic Error Counter

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	12804h

DWord	Bit	Description
0 avd_error_flagsR[31:0]	31:0	**Reserved** Format: MBZ

MFC Image Status Control

MFC_IMAGE_STATUS_CONTROL - MFC Image Status Control

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	128B8h

This register stores the suggested data for next frame in multi-pass.

DWord	Bit	Description
0	31:24	**Cumulative slice delta QP**
	23:16	**QP Value** suggested slice QP delta value for frame level Rate control. This value can be +ve or -ve
	15	**QP-Polarity Change** Cumulative slice delta QP polarity change.
	14:13	**Num-Pass Polarity Change** Number of passes after cumulative slice delta QP polarity changes.
	12	**VDENC Slice Overflow Error Occurred** Format: U1 True when slice size exceeds slice max size on final pass when VDENC is using attempting to use slice overflow prevention.
	11:8	**Total Num-Pass**
	7:4	**Reserved** Format: MBZ
	3	**Missing Huffman Code** Jpeg HW encoder reports if Huffman table entry is missing.
	2	**Panic** Panic triggered to avoid too big packed file.
	1	**Frame Bit Count** Frame Bit count over-run/under-run flag
	0	**Max Conformance Flag** Max Macroblock conformance flag or Frame Bit count over-run/under-run

MFC Image Status Mask

MFC_IMAGE_STATUS_MASK - MFC Image Status Mask		
Register Space:	MMIO: 0/2/0	
Source:	VideoCS	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	128B4h	
This register stores the image status(flags).		
DWord	**Bit**	**Description**
0	31:0	**Control Mask** Control Mask for dynamic frame repeat.

MFC QP Status Count

MFC_QUP_CT - MFC QP Status Count

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	128BCh

This register stores the suggested QP COUNTS in multi-pass.

DWord	Bit	Description
0	31:24	**Cumulative QP Adjust** Format: U8 Cumulative QP adjustment after multiple passes. If there is no need to multi-pass, this value would be zero. (This is in sign magnitude form).
	23:0	**Cumulative QP** Format: U24 Cumulative QP for all MB of a Frame (Can be used for computing average QP).

MFD Error Status

MFD_ERROR_STATUS - MFD Error Status	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1C0800h
Description:	For VDBox0
Address:	1C4800h
Description:	For VDBox1
Address:	1D0800h
Description:	For VDBox2
Address:	1D4800h
Description:	For VDBox3
Address:	1E0800h
Description:	For VDBox4
Address:	1E4800h
Description:	For VDBox5
Address:	1F0800h
Description:	For VDBox6
Address:	1F4800h
Description:	For VDBox7
This register stores the error status flags and count reports by the bit-stream decoder. This register is not part of hardware context save and restore. Driver should read the content prior to starting a new batch/frame.	

DWord	Bit	Description

MFD_ERROR_STATUS - MFD Error Status		
0	31:20	**Reserved** Format: MBZ This field is currently reserved
	19:16	**AVC Short Format Error Flags** Exists If: // AVC Short Format == Ture Bit-stream error detected by VLD short format bit-stream decoder**.** These flags are reset at the beginning of a frame and updated until starting of another frame. [19] – Slice Type SE Error Flag – Invalid Slice Type SE [18] – MMCO SE Error Flag – Invalid memory management control operation SE. MMCO Loop does not end (mmco control != 0) even after all MMCO SEs are decoded OR MMCO SEs are still being decoded and MMCO SE loop end (mmco control == 0) is hit [17] – Reordering IDC Error Flag – Syntax Element modification_of_pic_nums_idc >= 6 OR modification_of_pic_nums_idc != 3 (end of reordering loop) but reordering count has already hit maximum value [16] – Premature bitstream end is hit before finishing slice header decode
	15:0	**Bit-stream Error flags** Exists If: // AVC CAVLC, AVC CABAC, VC1 and MPEG2 == True Bitstream error detected by the VLD bit-stream decoder. These flags are reset at the beginning of a frame and updated until starting of another frame. AVC CAVLC: Please refer to AVC CAVLC table for each bit field AVC CABAC: Please refer to AVC CABAC table for each bit field VC1: Please refer to VC1 table for each bit field MPEG2: Please refer to MPEG2 table for each bit field

MFD Picture Parameter

MFD_PICTURE_PARAM - MFD Picture Parameter	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	1C0820h
Description:	For VDbox0
Address:	1C4820h
Description:	For VDbox1
Address:	1D0820h
Description:	For VDbox2
Address:	1D4820h
Description:	For VDbox3
Address:	1E0820h
Description:	For VDbox4
Address:	1E4820h
Description:	For VDbox5
Address:	1F0820h
Description:	For VDbox6
Address:	1F4820h
Description:	For VDbox7

DWord	Bit	Description
0	31:0	**Reserved** Format: MBZ

MFX_Memory_Latency_Count1

MFX_LAT_CT1 - MFX_Memory_Latency_Count1	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1C0870h
Description:	For VDBox0
Address:	1C4870h
Description:	For VDBox1
Address:	1D0870h
Description:	For VDBox2
Address:	1D4870h
Description:	For VDBox3
Address:	1E0870h
Description:	For VDBox4
Address:	1E4870h
Description:	For VDBox5
Address:	1F0870h
Description:	For VDBox6
Address:	1F4870h
Description:	For VDBox7

This register stores the max and min memory latency counts reported on reference read requests. This register is not part of hardware context save and restore.

DWord	Bit	Description

MFX_LAT_CT1 - MFX_Memory_Latency_Count1		
0	31:24	**Max Request Count** This field indicates the maximum number of requests allowed by the memory sub-system channel.
	23:16	**Current Request Count** This field indicates the number of requests currently outstanding in the memory sub-system. This field should report with a value of zero at the end of frame; otherwise the motion compensation engine is most likely hung waiting for read data to be returned from sub-system.
	15:8	**MFX Reference picture read request - Max Latency Count in 8xMedia clock cycles** This field reports the maximum memory latency count on all reference reads requested by the motion compensation engine.
	7:0	**MFX Reference picture read request - Min Latency Count in 8xMedia clock cycles** This field reports the minimum memory latency count on all reference reads requested by the motion compensation engine.

MFX0 Fault Counter

MFX0_FAULT_CNTR - MFX0 Fault Counter		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	045A8h	
DWord	**Bit**	**Description**
0	31:0	**MFX0 Fault Counter** Default Value: 00000000h Access: RO This counter only applies to advance context when fault and stream mode is selected.

MFX0 Fixed Counter

MFX0_FIXED_CNTR - MFX0 Fixed Counter		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	045ACh	
DWord	**Bit**	**Description**
0	31:0	**MFX0 Fixed Counter** Default Value: 00000000h Access: RO This counter only applies to advance context when fault and stream mode is selected.

MFX1 Fault Counter

MFX1_FAULT_CNTR - MFX1 Fault Counter		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	045B0h	
DWord	**Bit**	**Description**
0	31:0	**MFX1 Fault Counter** Default Value: 00000000h Access: RO This counter only applies to advance context when fault and stream mode is selected.

MFX1 Fixed Counter

MFX1_FIXED_CNTR - MFX1 Fixed Counter		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	045B4h	
DWord	**Bit**	**Description**
0	31:0	**MFX1 Fixed Counter** Default Value: 00000000h Access: RO This counter only applies to advance context when fault and stream mode is selected.

MFX Frame BitStream SE/BIN Count

MFX_SE-BIN_CT - MFX Frame BitStream SE/BIN Count	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1C086Ch
Description:	For VDBox0
Address:	1C486Ch
Description:	For VDBox1
Address:	1D086Ch
Description:	For VDBox2
Address:	1D486Ch
Description:	For VDBox3
Address:	1E086Ch
Description:	For VDBox4
Address:	1E486Ch
Description:	For VDBox5
Address:	1F086Ch
Description:	For VDBox6
Address:	1F486Ch
Description:	For VDBox7

This register stores the number of BINs (AVC CABAC) and SEs (CAVLD, VLD) decoded in a frame. This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:0	**MFX Frame Bit-stream SE/BIN Count** Total number of BINs/SEs decoded in current frame. This number is used with frame performance count to derive Bin/clk or SE/clk.

MFX Frame Macroblock Count

MFX_MB_COUNT - MFX Frame Macroblock Count	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1C0868h
Description:	For VDBox0
Address:	1C4868h
Description:	For VDBox1
Address:	1D0868h
Description:	For VDBox2
Address:	1D4868h
Description:	For VDBox3
Address:	1E0868h
Description:	For VDBox4
Address:	1E4868h
Description:	For VDBox5
Address:	1F0868h
Description:	For VDBox6
Address:	1F4868h
Description:	For VDBox7
This register stores the number of Macro-blocks decoded/encoded in current frame. This register is not part of hardware context save and restore.	

DWord	Bit	Description

MFX_MB_COUNT - MFX Frame Macroblock Count

0	31:20	**MBZ** Exists If: // JPEG == True Format: MBZ This field is currently reserved
	31:16	**Intra MB Count** Exists If: // AVC CAVLC, AVC CABAC, VC1 and MPEG2 == True Format: U16
	19:0	**JPEG Block Count** Exists If: // JPEG == True Format: U20 This 20-bit field indicates the number of 8x8 blocks within the JPEG frame. This field is clear at the start of decoding a new frame.
	15:0	**Number of MB Concealment** Exists If: // AVC CAVLC, AVC CABAC, VC1 and MPEG2 == True This 16-bit field indicates the number of MB is concealed by hardware. This field is clear at the start of decoding a new frame.

MFX Frame Row-Stored/BitStream Read Count

MFX_ROW-PER-BS_COUNT - MFX Frame Row-Stored/BitStream Read Count

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12880h

This register stores the total number of row-stored/bit-stream read requests made by the pre-fetch engine per frame. This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**MFX row-stored/bit-stream read request Count** Total number of row-stored/bit-stream read requests sent by the memory pre-fetch engine per frame.

MFX PAK MPEG TS STATUS

MFX_PAK_MPEG_TS_STATUS - MFX PAK MPEG TS STATUS

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12950h

This register stores MPEGTS packet status information

DWord	Bit	Description
0	31:28	**Next Continuity Center** Format: U4 HW will update the continuity counter the next MPEGTS packet stream for this stream ID needs to place in the bitstream.
	27:16	**Reserved** Format: MBZ
	15:0	**MPEGTS Packet Count** Format: U16 This field counts the total number of written MPEGTS video packets by PAK HW. The PES header (which contains the PCR and PTS value) is included in this count as well.

MFX Pipeline Status Flags

MFX_STATUS_FLAGS - MFX Pipeline Status Flags	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1C0838h
Description:	For VDBox0
Address:	1C4838h
Description:	For VDBox1
Address:	1D0838h
Description:	For VDBox2
Address:	1D4838h
Description:	For VDBox3
Address:	1E0838h
Description:	For VDBox4
Address:	1E4838h
Description:	For VDBox5
Address:	1F0838h
Description:	For VDBox6
Address:	1F4838h
Description:	For VDBox7
This register stores the various pipeline status flags. This register is not part of hardware context save and restore.	

DWord	Bit	Description

MFX_STATUS_FLAGS - MFX Pipeline Status Flags

0	31:17	**Reserved** Format: MBZ
	16	**MFX Active** Frame decoding/encoding is in progress. Set on frame_start; clear on frame_end.
	15:10	**Reserved** Format: MBZ
	9	**Streamout Enable**
	8	**Reserved**
	7	**Post Deblocking Mode Enable**
	6	**Pre Deblocking Mode Enable**
	5	**Decoder Mode Select** Value: 0 — Configure the MFD Engine for VLD Mode Value: 1 — Configure the MFD Engine for IT Mode
	4	**Codec Select** Value: 0 — Decode Value: 1 — Encode
	3:2	**Video Mode** Value: 00b — MPEG2 Value: 01b — VC1 Value: 10b — AVC Value: 11b — JPEG
	1	**Decoder Short Format Mode** Value: 0 — AVC/VC1 Short Format Mode is in use Value: 1 — AVC/VC1 Long Format Mode is in use
	0	**Stitch Mode** Value: 0b — Not in Stitch Mode Value: 1b — In the Special Stitch Mode

MFX SFC LOCK Request

MFX_SFC_LOCK_REQUEST - MFX SFC LOCK Request

Register Space:	MMIO: 0/2/0
Source:	VideoEnhancementCS
Access:	R/W
Size (in bits):	32
Address:	1C088Ch
Description:	For VDBox0
Address:	1D088Ch
Description:	For VDBox2
Address:	1E088Ch
Description:	For VDBox 4
Address:	1F088Ch
Description:	For VDBox6

DWord	Bit	Description
0	31:1	**Reserved** Format: MBZ
	0	**MFX_SFC_Forced_Lock** Format: U1 This bit can only be set by driver and it has to be clear by driver as well. Driver should set this bit before issuing the software (watchdog timer) reset. It tells MFX that a software reset is going to happen. MFX then issues a forced lock to SFC. If SFC is currently locked to MFX, SFC should not unlock itself from MFX. If SFC is NOT currently locked to MFX, SFC should not accept the lock request from MFX. Driver needs to clear this bit after the software reset sequence is complete.

MFX SFC LOCK Status

MFX_SFC_LOCK_STATUS - MFX SFC LOCK Status

Register Space:	MMIO: 0/2/0
Source:	VideoEnhancementCS
Access:	RO
Size (in bits):	32
Address:	1C0890h
Description:	For VDbox0
Address:	1D0890h
Description:	For VDBox2
Address:	1E0890h
Description:	For VDBox4
Address:	1F0890h
Description:	For VDBox6

DWord	Bit	Description
0	31:2	**Reserved** Format: MBZ
	1	**MFX_SFC_Forced_Act** Format: U1 This bit can only be set by hardware and it has to be clear by hardware as well. This bit is going to be polled by driver. This bit indicates that MFX has received MFX_SFC_Forced_Lock from driver and it has sent that signal to SFC. Once this bit is set, it indicates SFC status (lock or unlock) will not be changed anymore. Driver will be safe to start the reset process after this bit is set. Hardware has to de-assert this bit after driver de-assert MFX_SFC_Forced_Lock as well.
	0	**MFX_SFC_Usage** Format: U1 This bit can only be set by hardware and it has to be clear by hardware as well. This bit indicates SFC is currently locked to MFX. This bit should be set after SFC accepts the lock request from MFX. This bit should be clear once SFC finishes the workload and unlocked from MFX. In case a reset happens on MFX, this bit must be reset once a new workload is received

MFX Slice Performance Count

MFX_SLICE_PERFORM_CT - MFX Slice Performance Count	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1C0864h
Description:	For VDBox0
Address:	1C4864h
Description:	For VDBox1
Address:	1D0864h
Description:	For VDBox2
Address:	1D4864h
Description:	For VDBox3
Address:	1E0864h
Description:	For VDBox4
Address:	1E4864h
Description:	For VDBox5
Address:	1F0864h
Description:	For VDBox6
Address:	1F4864h
Description:	For VDBox7

This register stores the number of clock cycles spent decoding/encoding the current slice. This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:0	**MFX Frame Performance Count** Total number of clocks between slice start and slice end. This count is incremented on crm_clk

MG_CLKHUB

MG_CLKHUB - MG_CLKHUB	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	global
Address:	16839Ch-16839Fh
Name:	MG_CLKHUB_LN0_PORT1
ShortName:	MG_CLKHUB_LN0_PORT1
Power:	PG0
Reset:	global
Address:	16939Ch-16939Fh
Name:	MG_CLKHUB_LN0_PORT2
ShortName:	MG_CLKHUB_LN0_PORT2
Power:	PG0
Reset:	global
Address:	16A39Ch-16A39Fh
Name:	MG_CLKHUB_LN0_PORT3
ShortName:	MG_CLKHUB_LN0_PORT3
Power:	PG0
Reset:	global
Address:	16B39Ch-16B39Fh
Name:	MG_CLKHUB_LN0_PORT4
ShortName:	MG_CLKHUB_LN0_PORT4
Power:	PG0
Reset:	global
Address:	16879Ch-16879Fh
Name:	MG_CLKHUB_LN1_PORT1
ShortName:	MG_CLKHUB_LN1_PORT1

MG_CLKHUB - MG_CLKHUB

Power: PG0
Reset: global

Address: 16979Ch-16979Fh
Name: MG_CLKHUB_LN1_PORT2
ShortName: MG_CLKHUB_LN1_PORT2

Power: PG0
Reset: global

Address: 16A79Ch-16A79Fh
Name: MG_CLKHUB_LN1_PORT3
ShortName: MG_CLKHUB_LN1_PORT3

Power: PG0
Reset: global

Address: 16B79Ch-16B79Fh
Name: MG_CLKHUB_LN1_PORT4
ShortName: MG_CLKHUB_LN1_PORT4

Power: PG0
Reset: global

DWord	Bit	Description
0	31:26	**hsclk_overrides**
	25	**od_clkhub1_rxvhf_selclk1a_h** Default Value: 1b
	24	**od_clkhub2_rxvhf_selclk1a_h** Default Value: 1b
	23:14	**Reserved**
	13	**od_clkhub1_iqgen_en**
	12	**od_clkhub2_iqgen_en**
	11	**cfg_low_rate_lkren** Value: 0b — Name: Disable Value: 1b — Name: Enable
	10:8	**Reserved**
	7:0	**vhfclk_overrides**

MG_CLKTOP_CORECLKCTL1

MG_CLKTOP_CORECLKCTL1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	1688D8h-1688DBh
Name:	MG_CLKTOP2_CORECLKCTL1_PORT1
ShortName:	MG_CLKTOP2_CORECLKCTL1_PORT1
Power:	PG0
Reset:	global
Address:	1698D8h-1698DBh
Name:	MG_CLKTOP2_CORECLKCTL1_PORT2
ShortName:	MG_CLKTOP2_CORECLKCTL1_PORT2
Power:	PG0
Reset:	global
Address:	16A8D8h-16A8DBh
Name:	MG_CLKTOP2_CORECLKCTL1_PORT3
ShortName:	MG_CLKTOP2_CORECLKCTL1_PORT3
Power:	PG0
Reset:	global
Address:	16B8D8h-16B8DBh
Name:	MG_CLKTOP2_CORECLKCTL1_PORT4
ShortName:	MG_CLKTOP2_CORECLKCTL1_PORT4
Power:	PG0
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31:30	**Reserved** Format: MBZ

MG_CLKTOP_CORECLKCTL1

29	**od_clktop_coreclkd_bypass** bypass enable of coreclkd to take input refclk

Value	Name
0b	Disable
1b	Enable

28	**od_clktop_coreclkd_divretimeren_h** retimer enable

Value	Name
0b	odd div ratio
1b	even div ratio **[Default]**

27	**Reserved**

Format:	MBZ

26	**od_clktop_coreclkc_bypass** bypass enable of coreclkc to take input refclk

Value	Name
0b	Disable
1b	Enable

25	**od_clktop_coreclkc_divretimeren_h** retimer enable

Value	Name
0b	odd div ratio
1b	even div ratio

24	**Reserved**

Format:	MBZ

23:16	**od_clktop_coreclkb_divratio**

Default Value:	0x08

divider ratio for coreclkb divider

15:8	**od_clktop_coreclka_divratio**

Default Value:	0x05

divider ratio for coreclka divider

7:6	**Reserved**

Format:	MBZ

5	**od_clktop_coreclkb_bypass** bypass enable of coreclkb to take input refclk

Value	Name

MG_CLKTOP_CORECLKCTL1

		0b: Disable 1b: Enable
	4	**od_clktop_coreclkb_divretimeren_h** retimer enable 0b: odd div ratio 1b: even div ratio **[Default]**
	3	**Reserved** Format: MBZ
	2	**od_clktop_coreclka_bypass** bypass enable of coreclka to take input refclk 0b: Disable 1b: Enable
	1	**od_clktop_coreclka_divretimeren_h** retimer enable 0b: odd div ratio 1b: even div ratio
	0	**Reserved** Format: MBZ

MG_CLKTOP_HSCLKCTL

MG_CLKTOP_HSCLKCTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	1688D4h-1688D7h
Name:	MG_CLKTOP2_HSCLKCTL_PORT1
ShortName:	MG_CLKTOP2_HSCLKCTL_PORT1
Power:	PG0
Reset:	global
Address:	1698D4h-1698D7h
Name:	MG_CLKTOP2_HSCLKCTL_PORT2
ShortName:	MG_CLKTOP2_HSCLKCTL_PORT2
Power:	PG0
Reset:	global
Address:	16A8D4h-16A8D7h
Name:	MG_CLKTOP2_HSCLKCTL_PORT3
ShortName:	MG_CLKTOP2_HSCLKCTL_PORT3
Power:	PG0
Reset:	global
Address:	16B8D4h-16B8D7h
Name:	MG_CLKTOP2_HSCLKCTL_PORT4
ShortName:	MG_CLKTOP2_HSCLKCTL_PORT4
Power:	PG0
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description	
0	31:27	**Reserved**	
		Format:	MBZ

MG_CLKTOP_HSCLKCTL

26:25 od_clktop_clkobs_muxsel

mux select for oc_dfx_ck_clk2obs[0] digobs output

Value	Name
00b	hsdiv output clock
01b	iclk_bypass input from other clktop
10b	dsdiv output clock
11b	non-divided pll clock

24 od_clktop_clk2obs_en_h

enable of oc_dfx_ck_clk2obs[0] digobs output

Value	Name
0b	Disable
1b	Enable **[Default]**

23:22 Reserved

Format:	MBZ

21:20 Reserved

19 Reserved

Format:	MBZ

18 od_clktop_outclk_bypassen_h

enable of bypass clock output to the other clktop

Value	Name
0b	Disable
1b	Enable

17 Reserved

Format:	MBZ

16 od_clktop_coreclk_inputsel

mux select for input clock to coreclk divhub

Value	Name
0b	hsdiv output
1b	dsdiv output

15:14 od_clktop_tlinedrv_clksel

mux select for non-dedicated tlinedrv clock

Value	Name
00b	hsclkdiv output
01b	iclk_bypass input from other clktop
10b	dsdiv output clock
11b	non-divided pll clock

MG_CLKTOP_HSCLKCTL

	13:12	**od_clktop_hsdiv_divratio** Divider ratio for high speed divider. Div1

Value	Name
00b	Divide by 2
01b	Divide by 3
10b	Divide by 5
11b	Divide by 7

	11:8	**od_clktop_dsdiv_divratio** Divider ratio settings for programmable divider. Div2

Value	Name
0000b,0001b	No Div
0010b	Divide by 2
0011b	Divide by 3
0100b	Divide by 4
0101b	Divide by 5
0110b	Divide by 6
0111b	Divide by 7
1000b	Divide by 8
1001b	Divide by 9
1010b	Divide by 10 **[Default]**

	7	**od_clktop_tlinedrv_overrideen** override enable for follwing 4 tlinedrv enables

Value	Name
0b	Disable
1b	Enable

	6	**od_clktop_tlinedrv_enleft_ded_h_ovrd** enable of left side dedicated tlinedrv to output full-rate clock to left lanes

Value	Name
0b	Disable
1b	Enable

	5	**od_clktop_tlinedrv_enright_ded_h_ovrd** enable of right side dedicated tlinedrv to output full-rate clock to right lanes

Value	Name
0b	Disable
1b	Enable

	4	**od_clktop_tlinedrv_enleft_h_ovrd** enable of left side tlinedrv to output divided clock to left lanes

MG_CLKTOP_HSCLKCTL

		Value / **Name** 0b – Disable 1b – Enable **[Default]**
	3	**od_clktop_tlinedrv_enright_h_ovrd** enable of right side tlinedrv to output divided clock to right lanes **Value** / **Name** 0b – Disable 1b – Enable **[Default]**
	2	**od_clktop_dsdiv_en_h** Enable dsdiv clock divider. Div2. **Value** / **Name** 0b – Disable 1b – Enable **[Default]**
	1	**Reserved** Format: MBZ
	0	**od_clktop_hsdiv_en_h** Enable high speed clock divider. Div1 **Value** / **Name** 0b – Disable 1b – Enable **[Default]**

MG_DP_MODE

MG_DP_MODE - MG_DP_MODE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	global
Address:	1683A0h-1683A3h
Name:	MG_DP_MODE_LN0_ACU_PORT1
ShortName:	MG_DP_MODE_LN0_ACU_PORT1
Power:	PG0
Reset:	global
Address:	1693A0h-1693A3h
Name:	MG_DP_MODE_LN0_ACU_PORT2
ShortName:	MG_DP_MODE_LN0_ACU_PORT2
Power:	PG0
Reset:	global
Address:	16A3A0h-16A3A3h
Name:	MG_DP_MODE_LN0_ACU_PORT3
ShortName:	MG_DP_MODE_LN0_ACU_PORT3
Power:	PG0
Reset:	global
Address:	16B3A0h-16B3A3h
Name:	MG_DP_MODE_LN0_ACU_PORT4
ShortName:	MG_DP_MODE_LN0_ACU_PORT4
Power:	PG0
Reset:	global
Address:	1687A0h-1687A3h
Name:	MG_DP_MODE_LN1_ACU_PORT1
ShortName:	MG_DP_MODE_LN1_ACU_PORT1

MG_DP_MODE - MG_DP_MODE

Power:	PG0
Reset:	global

Address:	1697A0h-1697A3h
Name:	MG_DP_MODE_LN1_ACU_PORT2
ShortName:	MG_DP_MODE_LN1_ACU_PORT2
Power:	PG0
Reset:	global

Address:	16A7A0h-16A7A3h
Name:	MG_DP_MODE_LN1_ACU_PORT3
ShortName:	MG_DP_MODE_LN1_ACU_PORT3
Power:	PG0
Reset:	global

Address:	16B7A0h-16B7A3h
Name:	MG_DP_MODE_LN1_ACU_PORT4
ShortName:	MG_DP_MODE_LN1_ACU_PORT4
Power:	PG0
Reset:	global

This register is not reset by device 2 FLR.

DWord	Bit	Description
0	31:24	**cfg_ldo_powerup_timer_7_0** Default Value: 01111101b Timer to decide when LDO would be up, in case pwr_gate is used instead of LDO, it's configured to wait 20us, i.e 9'd500 by default using 25 MHz susclk
	23	**cfg_tr2_pwrgate_timer_bypass**
	22	**cfg_tr_pwrgate_timer_bypass**
	21	**cfg_cl_pwrgate_timer_bypass**
	20	**cfg_dig_pwrgate_timer_bypass**
	19	**crireg_cold_boot_done**
	18	**cfg_vr_pulldwn2gnd_tr2**
	17	**cfg_vr_pulldwn2gnd_tr**
	16	**cfg_ldo_powerup_timer_8**

MG_DP_MODE - MG_DP_MODE

	15	**Reserved**
	14	**cfg_cri_digpwr_req**
	13	**cfg_laneclkreq_force** When cfg_laneclkreq_gating_ctrl is low, this value will be used for the lane sus_clk request **Value** / **Name** 1b / force sus_clk request **[Default]** 0b / do not force sus_clk request
	12	**cfg_laneclkreq_gating_ctrl** 1'b1 - lanesusclk req gating enabled
	11	**cfg_susclk_gating_ctrl** 1'b1 - susclk gating enabled
	10	**cfg_rawpwr_req_override** Keep rawpwr on when this bit is 1
	9	**cfg_digpwr_req_override** Keep digpwr on when this bit is 1
	8	**cfg_rawpwr_gating_ctrl** Power gating enable reg for raw power
	7	**cfg_dp_x2_mode** Indicates x2 mode for DP
	6	**cfg_dp_x1_mode** Indicates x1 mode for DP
	5	**cfg_tr2pwr_gating_ctrl** Power gating enable reg for tr2
	4	**cfg_trpwr_gating_ctrl** Power gating enable reg for tr
	3	**cfg_clnpwr_gating_ctrl** Power gating enable reg for cln
	2	**cfg_digpwr_gating_ctrl** Power gating enable reg for dig
	1	**cfg_gaonpwr_gating_ctrl** Power gating enable reg for gaon
	0	**cfg_suspwr_gating_ctrl** Power gating enable reg for sus

MG_MISC_SUS0

MG_MISC_SUS0 - MG_MISC_SUS0	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	global
Address:	168814h-168817h
Name:	MG_MISC_SUS0_PORT1
ShortName:	MG_MISC_SUS0_PORT1
Power:	PG0
Reset:	global
Address:	169814h-169817h
Name:	MG_MISC_SUS0_PORT2
ShortName:	MG_MISC_SUS0_PORT2
Power:	PG0
Reset:	global
Address:	16A814h-16A817h
Name:	MG_MISC_SUS0_PORT3
ShortName:	MG_MISC_SUS0_PORT3
Power:	PG0
Reset:	global
Address:	16B814h-16B817h
Name:	MG_MISC_SUS0_PORT4
ShortName:	MG_MISC_SUS0_PORT4
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31:16	**Reserved**
	15:14	**os_susclk_dynclkgate_mode**

MG_MISC_SUS0 - MG_MISC_SUS0		
	13	**cfg_calclk_srcsel**
	12	**os_cfg_tr2pwr_gating_ctrl**
	11	**os_cfg_cl2pwr_gating_ctrl**
	10	**os_cfg_gaonpwr_gating_ctrl**
	9	**os_cfg_cl2pwr_pll1en_gating_ctrl** Default Value: 1b
	8	**cfg_calclkgate_dis**
	7	**os_cfg_trpwr_gating_ctrl**
	6	**os_cfg_cl1pwr_gating_ctrl**
	5	**os_cfg_dgpwr_gating_ctrl**
	4:0	**os_cfg_susclk_delay**

MG_PCS_FUSE0

MG_PCS_FUSE0 - MG_PCS_FUSE0	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	global
Address:	168000h-168003h
Name:	MG_LN0_FUSE0_PORT1
ShortName:	MG_LN0_FUSE0_PORT1
Power:	PG0
Reset:	global
Address:	169000h-169003h
Name:	MG_LN0_FUSE0_PORT2
ShortName:	MG_LN0_FUSE0_PORT2
Power:	PG0
Reset:	global
Address:	16A000h-16A003h
Name:	MG_LN0_FUSE0_PORT3
ShortName:	MG_LN0_FUSE0_PORT3
Power:	PG0
Reset:	global
Address:	16B000h-16B003h
Name:	MG_LN0_FUSE0_PORT4
ShortName:	MG_LN0_FUSE0_PORT4
Power:	PG0
Reset:	global
Address:	168400h-168403h
Name:	MG_LN1_FUSE0_PORT1
ShortName:	MG_LN1_FUSE0_PORT1

MG_PCS_FUSE0 - MG_PCS_FUSE0

Power: PG0
Reset: global

Address: 169400h-169403h
Name: MG_LN1_FUSE0_PORT2
ShortName: MG_LN1_FUSE0_PORT2

Power: PG0
Reset: global

Address: 16A400h-16A403h
Name: MG_LN1_FUSE0_PORT3
ShortName: MG_LN1_FUSE0_PORT3

Power: PG0
Reset: global

Address: 16B400h-16B403h
Name: MG_LN1_FUSE0_PORT4
ShortName: MG_LN1_FUSE0_PORT4
Power: PG0
Reset: global

This register is not reset by device 2 FLR.

DWord	Bit	Description
0	31	**reg_accoupled** Line coupling for non MIPI modes Value: 1b — AC coupled **[Default]** Value: 0b — DC coupled
	30	**reg_mipirateb** Controls MIPI rates (implemented with retention in AONwell) Value: 1b — MIPI Rate B **[Default]** Value: 0b — MIPI Rate A
	29:12	**Reserved**
	11	**reg_rxcalbypass_h** Bypass RX upar calibration.(was Implemented with retention in AON)
	10:0	**Reserved**

MG_PLL_BIAS

MG_PLL_BIAS	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	168A14h-168A17h
Name:	MG_PLL1_BIAS_PORT1
ShortName:	MG_PLL1_BIAS_PORT1
Power:	PG0
Reset:	global
Address:	169A14h-169A17h
Name:	MG_PLL1_BIAS_PORT2
ShortName:	MG_PLL1_BIAS_PORT2
Power:	PG0
Reset:	global
Address:	16AA14h-16AA17h
Name:	MG_PLL1_BIAS_PORT3
ShortName:	MG_PLL1_BIAS_PORT3
Power:	PG0
Reset:	global
Address:	16BA14h-16BA17h
Name:	MG_PLL1_BIAS_PORT4
ShortName:	MG_PLL1_BIAS_PORT4
Power:	PG0
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31:30	**i_bias_gb_sel**
	29:24	**i_init_dcoamp**

MG_PLL_BIAS		
		Default Value: 3Fh
	23:16	**i_bias_bonus**
	15	**i_biascal_en_h** Default Value: 1h
	14:13	**i_iref_refclk_mode**
	12:8	**i_ctrim** Default Value: 0Ch
	7:5	**i_vref_rdac** Default Value: 4h
	4:0	**i_ireftrim** Default Value: 04h

MG_PLL_DIV0

MG_PLL_DIV0	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	168A00h-168A03h
Name:	MG_PLL1_DIV0_PORT1
ShortName:	MG_PLL1_DIV0_PORT1
Power:	PG0
Reset:	global
Address:	169A00h-169A03h
Name:	MG_PLL1_DIV0_PORT2
ShortName:	MG_PLL1_DIV0_PORT2
Power:	PG0
Reset:	global
Address:	16AA00h-16AA03h
Name:	MG_PLL1_DIV0_PORT3
ShortName:	MG_PLL1_DIV0_PORT3
Power:	PG0
Reset:	global
Address:	16BA00h-16BA03h
Name:	MG_PLL1_DIV0_PORT4
ShortName:	MG_PLL1_DIV0_PORT4
Power:	PG0
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31	**i_direct_pin_if_en** retimer enable

Value	Name
0b	register IF
1b	direct pin IF

MG_PLL_DIV0

	30	**i_fracnen_h** Enables fractional modulator. For SSC, this bit needs to be set to '1', even though it starts with integer division ratio. **Value** / **Name** 0b – Disable 1b – Enable **[Default]**
	29:8	**i_fbdiv_frac** Default Value: 1E00h Fractional Modulator settings (M2 fraction)
	7:0	**i_fbdiv_intgr** Default Value: 69h Feedback divider post division (M2 integer)

MG_PLL_DIV1

MG_PLL_DIV1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	168A04h-168A07h
Name:	MG_PLL1_DIV1_PORT1
ShortName:	MG_PLL1_DIV1_PORT1
Power:	PG0
Reset:	global
Address:	169A04h-169A07h
Name:	MG_PLL1_DIV1_PORT2
ShortName:	MG_PLL1_DIV1_PORT2
Power:	PG0
Reset:	global
Address:	16AA04h-16AA07h
Name:	MG_PLL1_DIV1_PORT3
ShortName:	MG_PLL1_DIV1_PORT3
Power:	PG0
Reset:	global
Address:	16BA04h-16BA07h
Name:	MG_PLL1_DIV1_PORT4
ShortName:	MG_PLL1_DIV1_PORT4
Power:	PG0
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31:30	**Reserved**
	29:28	**Reserved**

MG_PLL_DIV1

27:24	**i_rodiv_sel** Ring Oscillator Divider setting
23:19	**Reserved** Format: MBZ
18:16	**i_iref_ndivratio** irefBias refclock divider control, which sets the divide ratio for the PLL input reference clock

Value	Name
001b	Div1
010b	Div2 **[Default]**
100b	Div4

15:14	**Reserved** Format: MBZ
13:12	**i_dither_div** Dither Divider Setting for prediv output

Value	Name
00b	1
01b	2 **[Default]**
10b	4
11b	8

11	**i_divretimeren** Retiming of feedback clock

Value	Name
0b	Disable
1b	Enable

10	**i_plllc_reg_longloopclk_sel** long loop select

Value	Name
0b	DCO clk from PLL core for tight loop
1b	External divided DCO clock for long loop

9	**i_plllc_reg_fbclkext_sel** select for feedback clock mux

Value	Name
0b	fbclk from pll core
1b	extfbclk

8	**i_dutycyccorr_en_h** duty cycle correction enable

Value	Name

MG_PLL_DIV1

	0b	Disable
	1b	Enable

7:4 **i_ndivratio**

Refclk input divider control, which sets the divide ratio for the PLL input (N)

Value	Name
0000b	Div1
0001b	Div1default **[Default]**
0010b	Div2
0011b	Div3
0101b	Div5
0111b	Div7

3:0 **i_fbprediv**

Predivider ratio (M1)

Value	Name
0010b	Div2 **[Default]**
0100b	Div4

MG_PLL_FRAC_LOCK

MG_PLL_FRAC_LOCK	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	168A0Ch-168A0Fh
Name:	MG_PLL1_FRAC_LOCK_PORT1
ShortName:	MG_PLL1_FRAC_LOCK_PORT1
Power:	PG0
Reset:	global
Address:	169A0Ch-169A0Fh
Name:	MG_PLL1_FRAC_LOCK_PORT2
ShortName:	MG_PLL1_FRAC_LOCK_PORT2
Power:	PG0
Reset:	global
Address:	16AA0Ch-16AA0Fh
Name:	MG_PLL1_FRAC_LOCK_PORT3
ShortName:	MG_PLL1_FRAC_LOCK_PORT3
Power:	PG0
Reset:	global
Address:	16BA0Ch-16BA0Fh
Name:	MG_PLL1_FRAC_LOCK_PORT4
ShortName:	MG_PLL1_FRAC_LOCK_PORT4
Power:	PG0
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31:27	**i_dither_value** DCO Dither Override Value
	26	**i_ovc_snapshot_h**

MG_PLL_FRAC_LOCK

	This bit enables for LCPLL to take snapshot of PLL calibration states and integral component.
25	**i_fbdiv_strobe_h** Propagate bit for LCPLL to capture feedback divider ratio settings and feedfwrd gain for dynamic PLL frequency update. This bit is automatically cleared after divratio ratio settings captured. (hw clear).
24	**i_pllrampen_h** This need to be asserted for dynamically updating PLL frequency configuration. In normal POR mode, i_pllrampen_h = 0, and no register update is allowed while PLL is running. This needs to be set for dynamic PPM shift. User needs to disable this register after PPM change, to prevent auto change of AFC code when fine is code below 1/4 or above 3/4 due to PVT variation.

Value	Name
0b	Disable
1b	Enable

23	**i_plllc_restore_mode_ctrl** Mode control signal for ro direct pin vs reg pin

Value	Name
0b	Direct pin IF
1b	Register IF

22	**i_plllc_restore_reg** Register control for restoring PLL state with earlier snapshot
21	**i_dither_ovrd** Dither Override enable

Value	Name
0b	Disable
1b	Enable

20	**i_lf_half_cyc_en** DCO dithering enable (1st order dithering)
19:18	**i_truelock_criteria** True lock indicator criteria. After early lock generation, external PLL lock indicator asserted high when phase error is less than threshold value for this many cycles

Value	Name
00b	16
01b	32 **[Default]**
10b	48
11b	64

17:16	**i_earlylock_criteria** Early lock indicator criteria. Early PLL lock indicator asserted high when phase error is less than threshold value for this many cycles

Value	Name

MG_PLL_FRAC_LOCK

	00b	16
	01b	32 **[Default]**
	10b	48
	11b	64

15 **i_dcodither_config**

Value	Name
0b	No floating dither
1b	floating dither

14:11 **i_lockthresh**

Default Value:	0101b

Digital lock detect threshold, the PLL will generate plllockout when the phase error detected by TDC is within lockthresh number of TDC counts for 64 consecutive cycles.

10 **i_dcoditheren_h**

DCO dithering enable (1st order dithering)

Value	Name
0b	Disable
1b	Enable **[Default]**

9 **i_feedfwrdcal_pause_h**

This bit is for dynamically turning on and off feed forward gain calibration, when i_feedfwrdcal_en_h is enabled to take care of dynamic feedfwrdgain calculation during SSC mode

Value	Name
0b	Disable
1b	Enable

8 **i_feedfwrdcal_en_h**

Background feedfward gain calibration enable

Value	Name
0b	Disable
1b	Enable **[Default]**

7:0 **i_feedfwrdgain**

Default Value:	52h

Feedforwad gain for fractional mode/SSC mode PLL. This setting is needed whenever PLL is configured in fractional mode or configured for SSC clock generation.

MG_PLL_LF

MG_PLL_LF	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	168A08h-168A0Bh
Name:	MG_PLL1_LF_PORT1
ShortName:	MG_PLL1_LF_PORT1
Power:	PG0
Reset:	global
Address:	169A08h-169A0Bh
Name:	MG_PLL1_LF_PORT2
ShortName:	MG_PLL1_LF_PORT2
Power:	PG0
Reset:	global
Address:	16AA08h-16AA0Bh
Name:	MG_PLL1_LF_PORT3
ShortName:	MG_PLL1_LF_PORT3
Power:	PG0
Reset:	global
Address:	16BA08h-16BA0Bh
Name:	MG_PLL1_LF_PORT4
ShortName:	MG_PLL1_LF_PORT4
Power:	PG0
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31:24	**i_tdctargetcnt** Default Value: 27h TDC tristate buffer calibration counter value. Delay line loop oscillation is counted over two

	refclk cycles. This is used for TDC coarse code calibration
23	**i_dcofine_resolution** DCO 10b fine split
22:21	**i_afc_startup** AFC startpoint

Value	Name
00b	Mid
01b	Upper 3/4
10b	Upper 1/4
11b	Lower 1/4

20	**i_afccntsel** AFC counter target

Value	Name
0b	256
1b	512 **[Default]**

19	**i_afc_divratio** AFC divder ratio

Value	Name
0b	DCO div 4
1b	DCO div 8

18:16	**i_gainctrl** Adjustable gain for loop filter. Both coefficients shifted right by gainctrl before lock
15	**Reserved**

Format:	MBZ

14	**i_tdc_fine_res** TDC fine resolution select

Value	Name
0b	Coarse resolution div 8
1b	Coarse resolution div 4

13	**i_fll_en_h** FLL enable

Value	Name
0b	Disable
1b	Enable

12:8	**i_int_coeff**

Default Value:	00111b

MG_PLL_LF		
		integral coeff. = 2^(-int_coeff), tageting up to 2^-11
	7:4	**i_fll_int_coeff** FLL integral coefficient
	3:0	**i_prop_coeff** Default Value: 0011b proportional coeff. = 2^(-prop_coeff+1)

MG_PLL_SSC

MG_PLL_SSC	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	168A10h-168A13h
Name:	MG_PLL1_SSC_PORT1
ShortName:	MG_PLL1_SSC_PORT1
Power:	PG0
Reset:	global
Address:	169A10h-169A13h
Name:	MG_PLL1_SSC_PORT2
ShortName:	MG_PLL1_SSC_PORT2
Power:	PG0
Reset:	global
Address:	16AA10h-16AA13h
Name:	MG_PLL1_SSC_PORT3
ShortName:	MG_PLL1_SSC_PORT3
Power:	PG0
Reset:	global
Address:	16BA10h-16BA13h
Name:	MG_PLL1_SSC_PORT4
ShortName:	MG_PLL1_SSC_PORT4
Power:	PG0
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31	**i_ssc_openloop_en_h**
	30	**i_ssc_strobe_h**

MG_PLL_SSC		
	29	**i_rampafc_sscen_h**
	28	**i_sscen_h** Default Value: 1h
	27:26	**i_ssctype** Default Value: 2h
	25:16	**i_sscsteplength** Default Value: 13h
	15:13	**Reserved**
	12:10	**i_sscstepnum** Default Value: 4h
	9	**i_s_sscfll_en_h** Default Value: 1b
	8	**i_afc_startup2**
	7:0	**i_sscstepsize** Default Value: 0Fh

MG_PLL_TDC_COLDST_BIAS

MG_PLL_TDC_COLDST_BIAS	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	168A18h-168A1Bh
Name:	MG_PLL1_TDC_COLDST_BIAS_PORT1
ShortName:	MG_PLL1_TDC_COLDST_BIAS_PORT1
Power:	PG0
Reset:	global
Address:	169A18h-169A1Bh
Name:	MG_PLL1_TDC_COLDST_BIAS_PORT2
ShortName:	MG_PLL1_TDC_COLDST_BIAS_PORT2
Power:	PG0
Reset:	global
Address:	16AA18h-16AA1Bh
Name:	MG_PLL1_TDC_COLDST_BIAS_PORT3
ShortName:	MG_PLL1_TDC_COLDST_BIAS_PORT3
Power:	PG0
Reset:	global
Address:	16BA18h-16BA1Bh
Name:	MG_PLL1_TDC_COLDST_BIAS_PORT4
ShortName:	MG_PLL1_TDC_COLDST_BIAS_PORT4
Power:	PG0
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31	**i_iref_refclk_inv_en**
	30	**i_irefdigdften**

MG_PLL_TDC_COLDST_BIAS		
	29	**i_digdftswep**
	28	**i_vgsbufen**
	27	**i_irefint_en** Default Value: 1h
	26	**i_irefext_en**
	25:24	**i_bias_calib_stepsize**
	23	**i_irefbias_startup_pulse_bypass**
	22:19	**i_dco_settling_time_cntr**
	18:17	**i_irefbias_startup_pulse_width** Default Value: 1h
	16	**i_coldstart**
	15	**i_bbinlock_h**
	14:11	**i_bbthresh**
	10:8	**i_bb_gain**
	7:6	**i_swcap_irefgen_clkmode**
	5:4	**i_tdc_offset_lock**
	3	**i_tdcdc_en_h**
	2	**i_tdcovccorr_en_h** Default Value: 1h
	1:0	**i_tdcsel** Default Value: 3h

MG_REFCLKIN_CTL

MG_REFCLKIN_CTL - MG_REFCLKIN_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	global
Address:	16892Ch-16892Fh
Name:	MG_REFCLKIN_CTL_PORT1
ShortName:	MG_REFCLKIN_CTL_PORT1
Power:	PG0
Reset:	global
Address:	16992Ch-16992Fh
Name:	MG_REFCLKIN_CTL_PORT2
ShortName:	MG_REFCLKIN_CTL_PORT2
Power:	PG0
Reset:	global
Address:	16A92Ch-16A92Fh
Name:	MG_REFCLKIN_CTL_PORT3
ShortName:	MG_REFCLKIN_CTL_PORT3
Power:	PG0
Reset:	global
Address:	16B92Ch-16B92Fh
Name:	MG_REFCLKIN_CTL_PORT4
ShortName:	MG_REFCLKIN_CTL_PORT4
Power:	PG0
Reset:	global
This register is not reset by device 2 FLR.	

DWord	Bit	Description
0	31:12	**Reserved**

MG_REFCLKIN_CTL - MG_REFCLKIN_CTL		
	11	**od_refclkin2_refclkinjmux** mux select of external injection refclk inputs: 0 to select amonrefclkinj 1 to select rcomprefclkinj
	10:8	**od_refclkin2_refclkmux** mux select for refclk output 3'b000: external injection refclk 3'b001: xtalinrefclk 3'b010:mgrefclkin 3'b011: socrefclk1 3'b100:socrefclk2 3'b101:socrefclk3 3'b110:socrefclk4 3'b111:socrefclk5
	7:4	**Reserved**
	3	**od_refclkin1_refclkinjmux** mux select of external injection refclk inputs: 0 to select amonrefclkinj 1 to select rcomprefclkinj
	2:0	**od_refclkin1_refclkmux** mux select for refclk output. 3'b000: external injection refclk 3'b001: xtalinrefclk 3'b010:mgrefclkin 3'b011: socrefclk1 3'100:socrefclk2 3'b101:socrefclk3 3'b110:socrefclk4 3'b111:socrefclk5

MG_TX_DCC

MG_TX_DCC - MG_TX_DCC	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	global
Address:	168110h-168113h
Name:	MG_TX_DCC_TX1LN0_PORT1
ShortName:	MG_TX_DCC_TX1_LN0_PORT1
Power:	PG0
Reset:	global
Address:	169110h-169113h
Name:	MG_TX_DCC_TX1LN0_PORT2
ShortName:	MG_TX_DCC_TX1_LN0_PORT2
Power:	PG0
Reset:	global
Address:	16A110h-16A113h
Name:	MG_TX_DCC_TX1LN0_PORT3
ShortName:	MG_TX_DCC_TX1_LN0_PORT3
Power:	PG0
Reset:	global
Address:	16B110h-16B113h
Name:	MG_TX_DCC_TX1LN0_PORT4
ShortName:	MG_TX_DCC_TX1_LN0_PORT4
Power:	PG0
Reset:	global
Address:	168090h-168093h
Name:	MG_TX_DCC_TX2LN0_PORT1
ShortName:	MG_TX_DCC_TX2_LN0_PORT1

MG_TX_DCC - MG_TX_DCC

Power:	PG0
Reset:	global
Address:	169090h-169093h
Name:	MG_TX_DCC_TX2LN0_PORT2
ShortName:	MG_TX_DCC_TX2_LN0_PORT2
Power:	PG0
Reset:	global
Address:	16A090h-16A093h
Name:	MG_TX_DCC_TX2LN0_PORT3
ShortName:	MG_TX_DCC_TX2_LN0_PORT3
Power:	PG0
Reset:	global
Address:	16B090h-16B093h
Name:	MG_TX_DCC_TX2LN0_PORT4
ShortName:	MG_TX_DCC_TX2_LN0_PORT4
Power:	PG0
Reset:	global
Address:	168510h-168513h
Name:	MG_TX_DCC_TX1LN1_PORT1
ShortName:	MG_TX_DCC_TX1_LN1_PORT1
Power:	PG0
Reset:	global
Address:	169510h-169513h
Name:	MG_TX_DCC_TX1LN1_PORT2
ShortName:	MG_TX_DCC_TX1_LN1_PORT2
Power:	PG0
Reset:	global
Address:	16A510h-16A513h
Name:	MG_TX_DCC_TX1LN1_PORT3
ShortName:	MG_TX_DCC_TX1_LN1_PORT3

MG_TX_DCC - MG_TX_DCC

Power: PG0
Reset: global

Address: 16B510h-16B513h
Name: MG_TX_DCC_TX1LN1_PORT4
ShortName: MG_TX_DCC_TX1_LN1_PORT4

Power: PG0
Reset: global

Address: 168490h-168493h
Name: MG_TX_DCC_TX2LN1_PORT1
ShortName: MG_TX_DCC_TX2_LN1_PORT1

Power: PG0
Reset: global

Address: 169490h-169493h
Name: MG_TX_DCC_TX2LN1_PORT2
ShortName: MG_TX_DCC_TX2_LN1_PORT2

Power: PG0
Reset: global

Address: 16A490h-16A493h
Name: MG_TX_DCC_TX2LN1_PORT3
ShortName: MG_TX_DCC_TX2_LN1_PORT3

Power: PG0
Reset: global

Address: 16B490h-16B493h
Name: MG_TX_DCC_TX2LN1_PORT4
ShortName: MG_TX_DCC_TX2_LN1_PORT4

Power: PG0
Reset: global

DWord	Bit	Description
0	31:29	**Reserved**
	28:27	**cri_periodicdcc_timersel**

MG_TX_DCC - MG_TX_DCC

		Value: 00b — Name: 0.1ms Value: 01b — Name: 1ms **[Default]** Value: 10b — Name: 5ms Value: 11b — Name: 10ms
	26:25	**cfg_ami_ck_div_override_value**
	24	**cfg_ami_ck_div_override_en** Value: 0b — Name: Disable Value: 1b — Name: Enable
	23:22	**cri_ami_ck_div_sel_le_1000mhz** Value: 00b — Name: div1 Value: 01b — Name: div2 Value: 10b — Name: div4 **[Default]** Value: 11b — Name: div8
	21:20	**cri_ami_ck_div_sel_gt_500mhz** Value: 00b — Name: div1 Value: 01b — Name: div2 **[Default]** Value: 10b — Name: div4 Value: 11b — Name: div8
	19:18	**cri_ami_ck_div_sel_le_500mhz** Value: 00b — Name: div1 Value: 01b — Name: div2 Value: 10b — Name: div4 Value: 11b — Name: div8
	17:16	**cri_codeupdate_sel**
	15	**cri_frcdcccmpout_value**
	14	**cri_frcdcccmpout_en**
	13:11	**o_dcc_periodic_code** Access: RO
	10:8	**o_dcc_fine_code** Access: RO

MG_TX_DCC - MG_TX_DCC		
	7:4	**o_dcc_coarse_n_h** Access: RO
	3:0	**o_dcc_coarse_p_l** Access: RO

MG_TX_DRVCTRL

MG_TX_DRVCTRL - MG_TX_DRVCTRL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	global
Address:	168144h-168147h
Name:	MG_TX_DRVCTRL_TX1LN0_TXPORT1
ShortName:	MG_TX_DRVCTRL_TX1LN0_TXPORT1
Power:	PG0
Reset:	global
Address:	169144h-169147h
Name:	MG_TX_DRVCTRL_TX1LN0_TXPORT2
ShortName:	MG_TX_DRVCTRL_TX1LN0_TXPORT2
Power:	PG0
Reset:	global
Address:	16A144h-16A147h
Name:	MG_TX_DRVCTRL_TX1LN0_TXPORT3
ShortName:	MG_TX_DRVCTRL_TX1LN0_TXPORT3
Power:	PG0
Reset:	global
Address:	16B144h-16B147h
Name:	MG_TX_DRVCTRL_TX1LN0_TXPORT4
ShortName:	MG_TX_DRVCTRL_TX1LN0_TXPORT4
Power:	PG0
Reset:	global
Address:	1680C4h-1680C7h
Name:	MG_TX_DRVCTRL_TX2LN0_TXPORT1
ShortName:	MG_TX_DRVCTRL_TX2LN0_TXPORT1

MG_TX_DRVCTRL - MG_TX_DRVCTRL	
Power:	PG0
Reset:	global
Address:	1690C4h-1690C7h
Name:	MG_TX_DRVCTRL_TX2LN0_TXPORT2
ShortName:	MG_TX_DRVCTRL_TX2LN0_TXPORT2
Power:	PG0
Reset:	global
Address:	16A0C4h-16A0C7h
Name:	MG_TX_DRVCTRL_TX2LN0_TXPORT3
ShortName:	MG_TX_DRVCTRL_TX2LN0_TXPORT3
Power:	PG0
Reset:	global
Address:	16B0C4h-16B0C7h
Name:	MG_TX_DRVCTRL_TX2LN0_TXPORT4
ShortName:	MG_TX_DRVCTRL_TX2LN0_TXPORT4
Power:	PG0
Reset:	global
Address:	168544h-168547h
Name:	MG_TX_DRVCTRL_TX1LN1_TXPORT1
ShortName:	MG_TX_DRVCTRL_TX1LN1_TXPORT1
Power:	PG0
Reset:	global
Address:	169544h-169547h
Name:	MG_TX_DRVCTRL_TX1LN1_TXPORT2
ShortName:	MG_TX_DRVCTRL_TX1LN1_TXPORT2
Power:	PG0
Reset:	global
Address:	16A544h-16A547h
Name:	MG_TX_DRVCTRL_TX1LN1_TXPORT3
ShortName:	MG_TX_DRVCTRL_TX1LN1_TXPORT3

MG_TX_DRVCTRL - MG_TX_DRVCTRL

Power: PG0
Reset: global

Address: 16B544h-16B547h
Name: MG_TX_DRVCTRL_TX1LN1_TXPORT4
ShortName: MG_TX_DRVCTRL_TX1LN1_TXPORT4

Power: PG0
Reset: global

Address: 1684C4h-1684C7h
Name: MG_TX_DRVCTRL_TX2LN1_TXPORT1
ShortName: MG_TX_DRVCTRL_TX2LN1_TXPORT1

Power: PG0
Reset: global

Address: 1694C4h-1694C7h
Name: MG_TX_DRVCTRL_TX2LN1_TXPORT2
ShortName: MG_TX_DRVCTRL_TX2LN1_TXPORT2

Power: PG0
Reset: global

Address: 16A4C4h-16A4C7h
Name: MG_TX_DRVCTRL_TX2LN1_TXPORT3
ShortName: MG_TX_DRVCTRL_TX2LN1_TXPORT3

Power: PG0
Reset: global

Address: 16B4C4h-16B4C7h
Name: MG_TX_DRVCTRL_TX2LN1_TXPORT4
ShortName: MG_TX_DRVCTRL_TX2LN1_TXPORT4

Power: PG0
Reset: global

This register is not reset by device 2 FLR.

DWord	Bit	Description
0	31:30	**Reserved**

MG_TX_DRVCTRL - MG_TX_DRVCTRL		
	29:24	**cri_txdeemph_override_11_6** cursor deemph override value when enable bit is set, or cri_txdeemph_override[11:6]
	23	**Reserved**
	22	**cri_txdeemph_override_en** txdeemph override enable bit
	21:16	**cri_txdeemph_override_5_0** precursor deemph override value when enable bit is set, or cri_txdeemph_override[5:0]
	15	**Reserved**
	14	**continuous_rcomp_mode_h** enable continous rcomp mode in drvctrltherm
	13:12	**cri_loadgen_sel** loadgen select for datapath2ui
	11	**o_use_rcomp_in_bypass_h** use rcomp in bypass mode in drvctrlsync
	10:9	**Reserved**
	8	**o_frcstrongcmen** force strong common mode enable
	7:5	**prec_bypassen_h** bin-coded precursor bypass bin slices async enable
	4:2	**postc_bypassen_h** bin-coded postcursor bypass bin slices async enable
	1	**onehot_bypass_mode_h** 1: enable data inputs of 1 extra therm slice and all bin slices to protect against glitches, 0: don't enable
	0	**bin_bypassdata** bypass bin slices async data

MG_TX_LINK_PARAMS

MG_TX_LINK_PARAMS - MG_TX_LINK_PARAMS	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	global
Address:	16812Ch-16812Fh
Name:	MG_TX_LINK_PARAMS_TX1LN0_PORT1
ShortName:	MG_TX_LINK_PARAMS_TX1LN0_PORT1
Power:	PG0
Reset:	global
Address:	16912Ch-16912Fh
Name:	MG_TX_LINK_PARAMS_TX1LN0_PORT2
ShortName:	MG_TX_LINK_PARAMS_TX1LN0_PORT2
Power:	PG0
Reset:	global
Address:	16A12Ch-16A12Fh
Name:	MG_TX_LINK_PARAMS_TX1LN0_PORT3
ShortName:	MG_TX_LINK_PARAMS_TX1LN0_PORT3
Power:	PG0
Reset:	global
Address:	16B12Ch-16B12Fh
Name:	MG_TX_LINK_PARAMS_TX1LN0_PORT4
ShortName:	MG_TX_LINK_PARAMS_TX1LN0_PORT4
Power:	PG0
Reset:	global
Address:	1680ACh-1680AFh
Name:	MG_TX_LINK_PARAMS_TX2LN0_PORT1
ShortName:	MG_TX_LINK_PARAMS_TX2LN0_PORT1

MG_TX_LINK_PARAMS - MG_TX_LINK_PARAMS	
Power:	PG0
Reset:	global
Address:	1690ACh-1690AFh
Name:	MG_TX_LINK_PARAMS_TX2LN0_PORT2
ShortName:	MG_TX_LINK_PARAMS_TX2LN0_PORT2
Power:	PG0
Reset:	global
Address:	16A0ACh-16A0AFh
Name:	MG_TX_LINK_PARAMS_TX2LN0_PORT3
ShortName:	MG_TX_LINK_PARAMS_TX2LN0_PORT3
Power:	PG0
Reset:	global
Address:	16B0ACh-16B0AFh
Name:	MG_TX_LINK_PARAMS_TX2LN0_PORT4
ShortName:	MG_TX_LINK_PARAMS_TX2LN0_PORT4
Power:	PG0
Reset:	global
Address:	16852Ch-16852Fh
Name:	MG_TX_LINK_PARAMS_TX1LN1_PORT1
ShortName:	MG_TX_LINK_PARAMS_TX1LN1_PORT1
Power:	PG0
Reset:	global
Address:	16952Ch-16952Fh
Name:	MG_TX_LINK_PARAMS_TX1LN1_PORT2
ShortName:	MG_TX_LINK_PARAMS_TX1LN1_PORT2
Power:	PG0
Reset:	global
Address:	16A52Ch-16A52Fh
Name:	MG_TX_LINK_PARAMS_TX1LN1_PORT3
ShortName:	MG_TX_LINK_PARAMS_TX1LN1_PORT3

MG_TX_LINK_PARAMS - MG_TX_LINK_PARAMS

Power: PG0
Reset: global

Address: 16B52Ch-16B52Fh
Name: MG_TX_LINK_PARAMS_TX1LN1_PORT4
ShortName: MG_TX_LINK_PARAMS_TX1LN1_PORT4

Power: PG0
Reset: global

Address: 1684ACh-1684AFh
Name: MG_TX_LINK_PARAMS_TX2LN1_PORT1
ShortName: MG_TX_LINK_PARAMS_TX2LN1_PORT1

Power: PG0
Reset: global

Address: 1694ACh-1694AFh
Name: MG_TX_LINK_PARAMS_TX2LN1_PORT2
ShortName: MG_TX_LINK_PARAMS_TX2LN1_PORT2

Power: PG0
Reset: global

Address: 16A4ACh-16A4AFh
Name: MG_TX_LINK_PARAMS_TX2LN1_PORT3
ShortName: MG_TX_LINK_PARAMS_TX2LN1_PORT3

Power: PG0
Reset: global

Address: 16B4ACh-16B4AFh
Name: MG_TX_LINK_PARAMS_TX2LN1_PORT4
ShortName: MG_TX_LINK_PARAMS_TX2LN1_PORT4

Power: PG0
Reset: global

This register is not reset by device 2 FLR.

DWord	Bit	Description
0	31	**Reserved**

MG_TX_LINK_PARAMS - MG_TX_LINK_PARAMS

30	**cri_reversedeemph_en** reverse deemphasis enable 0: normal 1: swap r?level0 with r?level3 and r?level1 with r?level2

Value	Name
0b	Normal
1b	Swap

29	**cri_prepostcurswap** Swap the Post and Pre Cursor for i_txdeemphasis
28	**cri_prepostpresetcurswap** Swap the Post and Pre Cursor for Preset
27	**autoswingdone** Status of the AutoSwingMargin Operation
26	**cri_autoswingen** Enables the Rx eye Height Auto margin FSM to perform eye height margining
25	**cri_autoswingup** Tells the auto margin FSM whether we need to increment/decrement from the user specified starting value
24	**cri_autoswingsqlch** If bit is 0, then the FSM would perform Rx Eye Height checking by using LCE error output in Tx swing margin mode. If bit is 1, then the FSM would be used for squelch testing and use o_rxelectidle output from PCS squelch logic.
23:22	**Reserved**
21:16	**Auto Swing Margin** output from autoswingmargining logic that contains last margin000 +/- count
15:14	**Reserved**
13:8	**CurPreset** computed CurPreset Coefficient from PreCurPreset and PostCurPreset per advertised FS.
7	**cri_precur_coeff_sign**

Value	Name	Description
1b	Negative **[Default]**	TX EQ coefficient pre-cursor sign. C-1 is a negative value. 2's complement version of the preset or iTxdeemph[5:0] will be used.
0b	as is	TX EQ coefficient pre-cursor sign. Value will be used "as is".

6	**cri_postcur_coeff_sign**

Value	Name	Description
1b	Negative **[Default]**	TX EQ coefficient post-cursor sign. C+1 is a negative value. 2's complement version of the preset or iTxdeemph[17:12] will be used.

		0b: as is — TX EQ coefficient post-cursor value. Value will be used "as is".
	5	**cri_use_fs32** 1b: FS32 **[Default]** — TX EQ advertised full-scale value. Advertised full-scale value is set to 32. 0b: FS63 — TX EQ advertised full-scale value. Advertised full-scale value is set to63.
	4:0	**Reserved**

MG_TX_OBSDIG

MG_TX_OBSDIG - MG_TX_OBSDIG		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Access:	R/W	
Size (in bits):	32	
Reset:	global	
DWord	**Bit**	**Description**
0	31:24	**cri_drvhalfslice_threshold** Default Value: 5Ah
	23:21	**Reserved**
	20	**o_obsv01sel**
	19:16	**cri_dfxanaobssel**
	15	**Reserved**
	14:12	**o_obsdigselectupn**
	11	**Reserved**
	10:8	**o_obsdigselectupp**
	7	**Reserved**
	6:4	**o_obsdigselectdownn**
	3	**Reserved**
	2:0	**o_obsdigselectdownp**

MG_TX_PISO_READLOAD

MG_TX_PISO_READLOAD - MG_TX_PISO_READLOAD	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	global
Address:	16814Ch-16814Fh
Name:	MG_TX_PISO_READLOAD_TX1LN0_PORT1
ShortName:	MG_TX_PISO_READLOAD_TX1LN0_PORT1
Power:	PG0
Reset:	global
Address:	16914Ch-16914Fh
Name:	MG_TX_PISO_READLOAD_TX1LN0_PORT2
ShortName:	MG_TX_PISO_READLOAD_TX1LN0_PORT2
Power:	PG0
Reset:	global
Address:	16A14Ch-16A14Fh
Name:	MG_TX_PISO_READLOAD_TX1LN0_PORT3
ShortName:	MG_TX_PISO_READLOAD_TX1LN0_PORT3
Power:	PG0
Reset:	global
Address:	16B14Ch-16B14Fh
Name:	MG_TX_PISO_READLOAD_TX1LN0_PORT4
ShortName:	MG_TX_PISO_READLOAD_TX1LN0_PORT4
Power:	PG0
Reset:	global
Address:	1680CCh-1680CFh
Name:	MG_TX_PISO_READLOAD_TX2LN0_PORT1
ShortName:	MG_TX_PISO_READLOAD_TX2LN0_PORT1

MG_TX_PISO_READLOAD - MG_TX_PISO_READLOAD	
Power:	PG0
Reset:	global
Address:	1690CCh-1690CFh
Name:	MG_TX_PISO_READLOAD_TX2LN0_PORT2
ShortName:	MG_TX_PISO_READLOAD_TX2LN0_PORT2
Power:	PG0
Reset:	global
Address:	16A0CCh-16A0CFh
Name:	MG_TX_PISO_READLOAD_TX2LN0_PORT3
ShortName:	MG_TX_PISO_READLOAD_TX2LN0_PORT3
Power:	PG0
Reset:	global
Address:	16B0CCh-16B0CFh
Name:	MG_TX_PISO_READLOAD_TX2LN0_PORT4
ShortName:	MG_TX_PISO_READLOAD_TX2LN0_PORT4
Power:	PG0
Reset:	global
Address:	16854Ch-16854Fh
Name:	MG_TX_PISO_READLOAD_TX1LN1_PORT1
ShortName:	MG_TX_PISO_READLOAD_TX1LN1_PORT1
Power:	PG0
Reset:	global
Address:	16954Ch-16954Fh
Name:	MG_TX_PISO_READLOAD_TX1LN1_PORT2
ShortName:	MG_TX_PISO_READLOAD_TX1LN1_PORT2
Power:	PG0
Reset:	global
Address:	16A54Ch-16A54Fh
Name:	MG_TX_PISO_READLOAD_TX1LN1_PORT3
ShortName:	MG_TX_PISO_READLOAD_TX1LN1_PORT3

MG_TX_PISO_READLOAD - MG_TX_PISO_READLOAD

Power: PG0
Reset: global

Address: 16B54Ch-16B54Fh
Name: MG_TX_PISO_READLOAD_TX1LN1_PORT4
ShortName: MG_TX_PISO_READLOAD_TX1LN1_PORT4

Power: PG0
Reset: global

Address: 1684CCh-1684CFh
Name: MG_TX_PISO_READLOAD_TX2LN1_PORT1
ShortName: MG_TX_PISO_READLOAD_TX2LN1_PORT1

Power: PG0
Reset: global

Address: 1694CCh-1694CFh
Name: MG_TX_PISO_READLOAD_TX2LN1_PORT2
ShortName: MG_TX_PISO_READLOAD_TX2LN1_PORT2

Power: PG0
Reset: global

Address: 16A4CCh-16A4CFh
Name: MG_TX_PISO_READLOAD_TX2LN1_PORT3
ShortName: MG_TX_PISO_READLOAD_TX2LN1_PORT3

Power: PG0
Reset: global

Address: 16B4CCh-16B4CFh
Name: MG_TX_PISO_READLOAD_TX2LN1_PORT4
ShortName: MG_TX_PISO_READLOAD_TX2LN1_PORT4

Power: PG0
Reset: global

This register is not reset by device 2 FLR.

DWord	Bit	Description
0	31:30	**Reserved**

MG_TX_PISO_READLOAD - MG_TX_PISO_READLOAD

<table>
<tr><td>29</td><td>cri_bypbycomp
Number of slices in R2 in EI - is also affected by this bit
<table>
<tr><th>Value</th><th>Name</th><th>Description</th></tr>
<tr><td>0b</td><td></td><td>The amount of slices used in dftbypmode is by nswbypass, pswbypass and r2bypass registers</td></tr>
<tr><td>1b</td><td>[Default]</td><td>The amount of slices used is by 'slices' from swing-control block.</td></tr>
</table></td></tr>
<tr><td>28:24</td><td>cri_bypdftmode
selects the DFT mode.
DFT_OFF = 5'h00 // default
DFT_HIGHZ = 5'h01 // force bypassen=0
DFT_EIWEAK = 5'h02 // force rcvdtct cmkeep on
DFT_EISTRONG = 5'h03 // force txSWING into strongcm bypass mode
DFT_ALL1DIF = 5'h04 // padp: all 1's, padn: all 0's
DFT_ALL0DIF = 5'h05 // padp: all 0's, padn: all 1's
DFT_ALL1SE = 5'h06 // padp: all 1's, padn: all 1's
DFT_ALL0SE = 5'h07 // padp: all 0's, padn: all 0's
DFT_LFPS = 5'h08 // force susclk lfps
DFT_HSOBS = 5'h09 // put txSWING in hsobs bypass mode
DFT_DAC = 5'h0A // padp: p_bypassdata register, padn: n_bypassdata register
DFT_ASYNCOUT = 5'h0B // padp: bssb/exi data or gpio data p, padn: bssb/exi ~data or gpio data n
DFT_ASYNCIN = 5'h0C // enable input buffer in rcvdtct and force bypassen=0
DFT_ASYNCIO = 5'h0D // enable input buffer in rcvdtct and padp: gpio data p, padn: gpio data n
DFT_PISOLOAD = 5'h0E // force datapath enable and load piso data from cri reg
DFT_OBS = 5'h0F // put txSWING in hsobs bypass mode</td></tr>
<tr><td>23</td><td>cri_bssb_gpio_out_cri_cfg
Config bit: 0: (default) allow EXI controller to enable Tx output of BSSB data 1: force i_tx_bssb_gpio_out_en signal to 0, this blocks EXI controller enabling of Tx output path.</td></tr>
<tr><td>22</td><td>cri_beacondivratio
When bit value = 0 then beacon signal frequency is same as ick_sus when bit value = 1 then low clock Beacon freq 1/4 of sus clock freq (10-50MHz)</td></tr>
<tr><td>21</td><td>cri_neloopbacken
Near-End LoopBack enable 1- enable loopback 0- disable loopback</td></tr>
<tr><td>20:17</td><td>Reserved</td></tr>
<tr><td>16</td><td>cri_dnelb_en
enable dnelb output from TX</td></tr>
<tr><td>15:14</td><td>Reserved</td></tr>
<tr><td>13</td><td>cri_pisorate8bit_ovrd
value used for pisorate_8b when pisorate8bit_overden = 1.</td></tr>
<tr><td>12</td><td>cri_pisorate8bit_ovrd_en
8bit override enable. The pisorate_8b signal is normally decoded from PHYMODE and RATE.</td></tr>
</table>

MG_TX_PISO_READLOAD - MG_TX_PISO_READLOAD		
		When 1, the pisorate_8b signal will take with pisorate8bit_ovrd value.
	11:8	**Reserved**
	7:6	**Reserved**
	5	**cri_mediumcmrcompdis** This register bit is used to disable the rcomp slice value and enable the slice vales from the register define above. 1'b1 indicates rcomp slices disabled; 1'b0 indicates rcomp slice values enabled.
	4	**cri_use_preset_coef** Tx EQ Coefficient Source 0 - Tx equalization coefficients are driven by the controller. 1 - Tx equalization coefficients are determined by the Tx EQ Preset (1 of 11 possible presets).
	3	**cri_rounding_disable** 0 - use normal rounding in swing control calculation 1 - KG/LPT compatible mode, rounding is disabled in swing control calculation
	2	**cri_frcpresetcalc** Initiates a calculation to the 3-tap tx coefficients driven by the Preset.
	1	**cri_calcinit** initiate calculation of swing-control rewrite to '0' and '1' to re-initiate the calculation (self-clear)
	0	**cri_calccont** initiate calculation of swing-control while '1' the calculation is done consecutively

MG_TX_RCOMP1

MG_TX_RCOMP1 - MG_TX_RCOMP1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Access:	R/W	
Size (in bits):	32	
Reset:	global	
DWord	**Bit**	**Description**
0	31:24	**cri_rcomp_pulldn_offset**
	23:16	**cri_rcomp_pullup_offset**
	15:8	**cri_rcomp_pulldn_scale** Default Value: 80h
	7:0	**cri_rcomp_pullup_scale** Default Value: 80h

MG_TX_RCVDTCT

MG_TX_RCVDTCT - MG_TX_RCVDTCT		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Access:	R/W	
Size (in bits):	32	
Reset:	global	
DWord	**Bit**	**Description**
0	31:30	**Reserved**
	29	**i_crireg_drvhalfslice_inv** Default Value: 1b
	28	**o_frcrcvdtctrefen**
	27	**i_dftrcvdetectfinished** Access: RO
	26	**i_rcvdtctcmpout** Access: RO
	25	**i_crireg_simmode**
	24	**o_frcrcvdtcten**
	23	**i_dftrcvdetectedtxn** Access: RO
	22	**i_dftrcvdetectedtxp** Access: RO
	21:19	**i_crireg_rcvdtctrefsel_vss_vcm** Default Value: 010b
	18:16	**i_crireg_rcvdtctrefsel_vcm_vcc** Default Value: 010b
	15:8	**i_crireg_rcvdtctputime** Default Value: 25h
	7:4	**i_crireg_nswoverride**
	3:0	**i_crireg_pswoverride**

MG_TX_SWINGCTRL

MG_TX_SWINGCTRL - MG_TX_SWINGCTRL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	global
Address:	168148h-16814Bh
Name:	MG_TX_SWINGCTRL_TX1LN0_PORT1
ShortName:	MG_TX_SWINGCTRL_TX1LN0_PORT1
Power:	PG0
Reset:	global
Address:	169148h-16914Bh
Name:	MG_TX_SWINGCTRL_TX1LN0_PORT2
ShortName:	MG_TX_SWINGCTRL_TX1LN0_PORT2
Power:	PG0
Reset:	global
Address:	16A148h-16A14Bh
Name:	MG_TX_SWINGCTRL_TX1LN0_PORT3
ShortName:	MG_TX_SWINGCTRL_TX1LN0_PORT3
Power:	PG0
Reset:	global
Address:	16B148h-16B14Bh
Name:	MG_TX_SWINGCTRL_TX1LN0_PORT4
ShortName:	MG_TX_SWINGCTRL_TX1LN0_PORT4
Power:	PG0
Reset:	global
Address:	1680C8h-1680CBh
Name:	MG_TX_SWINGCTRL_TX2LN0_PORT1
ShortName:	MG_TX_SWINGCTRL_TX2LN0_PORT1

MG_TX_SWINGCTRL - MG_TX_SWINGCTRL	
Power:	PG0
Reset:	global
Address:	1690C8h-1690CBh
Name:	MG_TX_SWINGCTRL_TX2LN0_PORT2
ShortName:	MG_TX_SWINGCTRL_TX2LN0_PORT2
Power:	PG0
Reset:	global
Address:	16A0C8h-16A0CBh
Name:	MG_TX_SWINGCTRL_TX2LN0_PORT3
ShortName:	MG_TX_SWINGCTRL_TX2LN0_PORT3
Power:	PG0
Reset:	global
Address:	16B0C8h-16B0CBh
Name:	MG_TX_SWINGCTRL_TX2LN0_PORT4
ShortName:	MG_TX_SWINGCTRL_TX2LN0_PORT4
Power:	PG0
Reset:	global
Address:	168548h-16854Bh
Name:	MG_TX_SWINGCTRL_TX1LN1_PORT1
ShortName:	MG_TX_SWINGCTRL_TX1LN1_PORT1
Power:	PG0
Reset:	global
Address:	169548h-16954Bh
Name:	MG_TX_SWINGCTRL_TX1LN1_PORT2
ShortName:	MG_TX_SWINGCTRL_TX1LN1_PORT2
Power:	PG0
Reset:	global
Address:	16A548h-16A54Bh
Name:	MG_TX_SWINGCTRL_TX1LN1_PORT3
ShortName:	MG_TX_SWINGCTRL_TX1LN1_PORT3

MG_TX_SWINGCTRL - MG_TX_SWINGCTRL

Power: PG0
Reset: global

Address: 16B548h-16B54Bh
Name: MG_TX_SWINGCTRL_TX1LN1_PORT4
ShortName: MG_TX_SWINGCTRL_TX1LN1_PORT4

Power: PG0
Reset: global

Address: 1684C8h-1684CBh
Name: MG_TX_SWINGCTRL_TX2LN1_PORT1
ShortName: MG_TX_SWINGCTRL_TX2LN1_PORT1

Power: PG0
Reset: global

Address: 1694C8h-1694CBh
Name: MG_TX_SWINGCTRL_TX2LN1_PORT2
ShortName: MG_TX_SWINGCTRL_TX2LN1_PORT2

Power: PG0
Reset: global

Address: 16A4C8h-16A4CBh
Name: MG_TX_SWINGCTRL_TX2LN1_PORT3
ShortName: MG_TX_SWINGCTRL_TX2LN1_PORT3

Power: PG0
Reset: global

Address: 16B4C8h-16B4CBh
Name: MG_TX_SWINGCTRL_TX2LN1_PORT4
ShortName: MG_TX_SWINGCTRL_TX2LN1_PORT4

Power: PG0
Reset: global

This register is not reset by device 2 FLR.

DWord	Bit	Description
0	31:24	**Reserved**

MG_TX_SWINGCTRL - MG_TX_SWINGCTRL		
	23:16	**rcomp_pulldown_h** bin-coded cursor bypass therm slice and bin slice async pulldown data
	15:8	**rcomp_pullup_h** bin-coded cursor bypass therm slice and bin slice async pullup data
	7:6	**Reserved**
	5:0	**cri_txdeemph_override17_12** postcursor deemph override value when enable bit is set, or cri_txdeemph_override[17:12]

MGSR GTI PD Control

GTIPD_CTRL - MGSR GTI PD Control

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00E04h-00E07h

DWord	Bit	Description
0	31:16	**Mask Bits** Access: RO Mask bits apply to [15:0] of same register. If mask is set to 1, corresponding bit in [15:0] is written. If mask is set to 0, corresponding bit in [15:0] is unaffected.
	15:3	**Reserved** Access: RO
	2	**Render Unblock** Default Value: 0b Access: R/WC Render unblock (1) or block (0)
	1	**GT Block Mode** Default Value: 1b Access: R/WC Set GT C6 Standby mode (1) or CPD (0)
	0	**GT Unblock** Default Value: 0b Access: R/WC GT unblock (1) or block (0)

MGSR Media PD Control

MEDIAPD_CTRL - MGSR Media PD Control		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00E00h-00E03h	
DWord	**Bit**	**Description**
0	31:16	**Mask Bits** Access: RO Mask bits applied to [15:0] of same register. If mask is set to 1, corresponding bit in [15:0] is written. If mask is set to 0, corresponding bit in [15:0] is unaffected.
	15:12	**Reserved** Access: RO
	11:8	**VEBOX Unblock** Default Value: 0b Access: R/WC VEBOX unblock indications for VEBOX[3:0] (1) or block (0)
	7:0	**VDBOX Unblock** Default Value: 0b Access: R/WC VDBOX unblock indications for VDBOX[7:0] (1) or block (0) VDBOX[1:0] reside in Media slice0, VDBOX[3:2] in slice1, VDBOX[5:4] in slice2, VDBOX[7:6] in slice3

MGSR Programmable Shadow 0

PROGSHADOW_0 - MGSR Programmable Shadow 0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00EE0h-00EE3h	
DWord	**Bit**	**Description**
0	31:26	**Reserved** Access: RO
	25:0	**Shadow Address** Default Value: 00000h Access: R/W Programmable shadow register address.

MGSR Programmable Shadow 1

PROGSHADOW_1 - MGSR Programmable Shadow 1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00EE4h-00EE7h	
DWord	**Bit**	**Description**
0	31:26	**Reserved** Access: RO
	25:0	**Shadow Address** Default Value: 00000h Access: R/W Programmable shadow register address.

Mirror of DPRB

MDPRB - Mirror of DPRB		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	64	
Address:	090E8h	
DWord	**Bit**	**Description**
0	31:20	**DPRBASE** Access: RO
	19:0	**Spares** Access: RO
1	31:0	**DPRBASE** Access: RO Bits 63:32 of the DPRbase.

Mirror of DSMBASE

MBDSM - Mirror of DSMBASE		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	64	
Address:	090D0h	
DSM Base		
DWord	**Bit**	**Description**
0	63:20	**DSM Base Register** Access: RO This register contains the base address of stolen DRAM memory.
	19:0	**Spares** Access: RO

Mirror of EMRR Base LSB

EMRRBASE_LSB - Mirror of EMRR Base LSB		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	09200h	
Mirror of EMRR Base		
DWord	**Bit**	**Description**
0	31:12	**EMRR Base LSB** Access: RO EMRR Base Value.
	11:0	**Spares** Access: RO

Mirror of EMRR Base MSB

EMRRBASE_MSB - Mirror of EMRR Base MSB		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	09204h	
Mirror of EMRR Base		
DWord	**Bit**	**Description**
0	31:0	**EMRR Base MSB** Access: RO EMRR Base Value.

Mirror of EU Disable Fuses - Register0

MIRROR_EU_DISABLE0 - Mirror of EU Disable Fuses - Register0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	09134h

DWord	Bit	Description
0	31:8	**RSVD**
	7:0	**EU Disable Fuses** One Bit per EU In a sub-slice. Enable/Disable the same EU# in all the Sub-Slices. **Programming Notes** Bit values of 0 indicate enabled; Bit values of 1 indicate disabled.

Mirror of FUSE1 Control DW

FUSE1 - Mirror of FUSE1 Control DW		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	0911Ch	
DWord	**Bit**	**Description**
0	31:27	**Spares** Access: RO
	26	**VA DISABLE** Access: RO
	25:24	**SFC DISABLE**
	23	**Reserved**
	22	**Reserved**
	21	**Reserved**
	20	**Reserved**
	19	**Reserved**
	18	**Reserved**
	17:16	**Spares1** Access: RO
	15	**Authentication Bypass** Access: RO
	14	**Reserved**
	13	**Spares2** Access: RO
	12	**Reserved**
	11	**Render Disable**

FUSE1 - Mirror of FUSE1 Control DW			
		Access:	RO
	10:9	**Spares3**	
		Access:	RO
	8	**VME IME Enable**	
		Access:	RO
	7	**VME CRE Enable**	
		Access:	RO
	6:5	**Media Decode**	
		Access:	RO
		Applicable to Media - Fuse to disable VIN from processing media_objs or turn off the entire crclk tree trunk.	
	4	**Disable GT3 Slice Shutdown**	
		Access:	RO
		N/A -- Not used by GT hardware: This fuse is actually enforced by the PCU; it is reflected here for driver information only.	
	3	**Reserved**	
	2	**Spares4**	
		Access:	RO
	1:0	**Media Encode**	
		Access:	RO
		Applicable to Media - One fuse to disable VIN from processing Pak_obj. Second fuse to disable VME.	

Mirror of Fuse 3 control DW

FUSE3 - Mirror of Fuse 3 control DW

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	09118h

FUSE MIRROR 3

DWord	Bit	Description
0	28	**GT L3 HASH MODE FUSE** Access: RO L3 Bank Hash Mode (used in certain dynamic slice configurations) 0b = Use safe mode, hashing to fewer banks in specific cases 1b = Use all banks when possible
	27:26	**RSVD**
	25:24	**GT WGBox Configuration Fuse** Access: RO WGBox configuration 00b = Both WGBOXes enabled 01b = WGBOX1 enabled 10b = WGBOX0 enabled
	3:0	**GT L3 MODE FUSE** Access: RO L3 Bank Disable Select (only used in certain dynamic slice configurations and sub-single slice SKUs) 0001b = Bank0 , Bank4 0010b = Bank1 , Bank5 0100b = Bank2, Bank6 1000b = Bank3, Bank7 Note: L3 Banks are always disabled in pairs.

Mirror of Global Command Register

GCMD - Mirror of Global Command Register		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	090CCh	
DWord	**Bit**	**Description**
0	31	**Translation Enable** Access: RO Software writes to this field to request hardware to enable/disable DMA-remapping hardware. 0: Disable DMA-remapping hardware. 1: Enable DMA-remapping hardware. Hardware reports the status of the translation enable operation through the TES field in the Global Status register. Before enabling (or re-enabling) DMA-remapping hardware through this field, software must: • Setup the DMA-remapping structures in memory. • Flush the write buffers (through WBF field), if write buffer flushing is reported as required. • Set the root-entry table pointer in hardware (through SRTP field). • Perform global invalidation of the context-cache and global invalidation of IOTLB • If advanced fault logging supported, setup fault log pointer (through SFL field) and enable advanced fault logging (through EAFL field). Refer to Section 9 for detailed software requirements. There may be active DMA requests in the platform when software updates this field. Hardware must enable or disable remapping logic only at deterministic transaction boundaries, so that any in-flight transaction is either subject to remapping or not at all. Hardware implementations supporting DMA draining must drain any in-flight translated DMA read/write requests queued within the root complex before completing the translation enable command and reflecting the status of the command through the TES field in the GSTS_REG. Value returned on read of this field is undefined.
	30	**Set Root Table Pointer** Access: RO Software sets this field to set/update the root-entry table pointer used by hardware. The root-entry table pointer is specified through the Root-entry Table Address register. Hardware reports the status of the "root table pointer set" operation through the RTPS field in the Global Status register. The root table pointer set operation must be performed before enabling or re-enabling (after disabling) DMA remapping through the TE field. After a "root table pointer set" operation, software must globally invalidate the context cache and

GCMD - Mirror of Global Command Register

		then globally invalidate the IOTLB. This is required to ensure hardware uses only the remapping structures referenced by the new root table pointer, and not any stale cached entries. While DMA remapping is active, software may update the root table pointer through this field. However, to ensure valid in-flight DMA requests are deterministically remapped, software must ensure that the structures referenced by the new root table pointer are programmed to provide the same remapping results as the structures referenced by the previous root-table pointer. Clearing this bit has no effect. The value returned on a read of this field is undefined.
	29	**Set Fault Log** Access: RO This field is valid only for implementations supporting advanced fault logging. Software sets this field to request hardware to set/update the fault-log pointer used by hardware. The fault-log pointer is specified through Advanced Fault Log register. Hardware reports the status of the fault log set operation through the FLS field in the Global Status register. The fault log pointer must be set before enabling advanced fault logging (through EAFL field). Once advanced fault logging is enabled, the fault log pointer may be updated through this field while DMA remapping is active. Clearing this bit has no effect. The value returned on read of this field is undefined.
	28	**Enable Fault Logging** Access: RO This field is valid only for implementations supporting advanced fault logging. Software writes to this field to request hardware to enable or disable advanced fault logging. 0: Disable advanced fault logging. In this case, translation faults are reported through the Fault Recording registers. 1: Enable use of memory-resident fault log. When enabled, translation faults are recorded in the memory-resident log. The fault log pointer must be set in hardware (through SFL field) before enabling advanced fault logging. Hardware reports the status of the advanced fault logging enable operation through the AFLS field in the Global Status register. Value returned on read of this field is undefined.
	27	**Write Buffer Flush** Access: RO This bit is valid only for implementations requiring write buffer flushing. Software sets this field to request hardware to flush the root-complex internal write buffers. This is done to ensure any updates to the memory-resident remapping structures are not held in any internal write posting buffers. Refer to Section 11.1 for details on write-buffer flushing requirements. Hardware reports the status of the write buffer flushing operation through the WBFS field in the Global Status register. Clearing this bit has no effect.

GCMD - Mirror of Global Command Register

		Value returned on read of this field is undefined.
	26	**Queued Invalidation Enable** Access: RO This field is valid only for implementations supporting queued invalidations. Software writes to this field to enable or disable queued invalidations. 0: Disable queued invalidations. 1: Enable use of queued invalidations. Hardware reports the status of queued invalidation enable operation through QIES field in the Global Status register. Refer to Section 6.2.2 for software requirements for enabling/disabling queued invalidations. The value returned on a read of this field is undefined.
	25	**Interrupt Remapping Enable** Access: RO This field is valid only for implementations supporting interrupt remapping. 0: Disable interrupt-remapping hardware 1: Enable interrupt-remapping hardware Hardware reports the status of the interrupt remapping enable operation through the IRES field in the Global Status register. There may be active interrupt requests in the platform when software updates this field. Hardware must enable or disable interrupt-remapping logic only at deterministic transaction boundaries, so that any in-flight interrupts are either subject to remapping or not at all. Hardware implementations must drain any in-flight interrupts requests queued in the Root-Complex before completing the interrupt-remapping enable command and reflecting the status of the command through the IRES field in the Global Status register. The value returned on a read of this field is undefined.
	24	**Set Interrupt Remap Table Pointer** Access: RO This field is valid only for implementations supporting interrupt-remapping. Software sets this field to set/update the interrupt remapping table pointer used by hardware. The interrupt remapping table pointer is specified through the Interrupt Remapping Table Address register. Hardware reports the status of the interrupt remapping table pointer set operation through the IRTPS field in the Global Status register. The interrupt remap table pointer set operation must be performed before enabling or re-enabling (after disabling) interrupt-remapping hardware through the IRE field. After an interrupt remap table pointer set operation, software must globally invalidate the interrupt entry cache. This is required to ensure hardware uses only the interrupt-remapping entries referenced by the new interrupt remap table pointer, and not any stale cached entries. While interrupt remapping is active, software may update the interrupt remapping table pointer through this field. However, to ensure valid in-flight interrupt requests are deterministically remapped, software must ensure that the structures referenced by the new interrupt remap table

GCMD - Mirror of Global Command Register

		pointer are programmed to provide the same remapping results as the structures referenced by the previous interrupt remap table pointer. Clearing this bit has no effect. The value returned on a read of this field is undefined.
	23	**Compatibility Format Interrupt** Access: RO This field is valid only for Intel(R)64 implementations supporting interrupt-remapping. Software writes to this field to enable or disable Compatibility Format interrupts on Intel(R)64 platforms. The value in this field is effective only when interrupt-remapping is enabled and Legacy Interrupt Mode is active. 0: Block Compatibility format interrupts. 1: Process Compatibility format interrupts as pass-through (bypass interrupt remapping). Hardware reports the status of updating this field through the CFIS field in the Global Status register. Refer to Section 5.4.1 for details on Compatibility Format interrupt requests. The value returned on a read of this field is undefined. This field is not implemented on Itanium(TM) implementations.
	22:0	**Spares** Access: RO

Mirror of GMCH Graphics Control Register

MGGC - Mirror of GMCH Graphics Control Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	09094h

Mirror of GMCH Graphics Control Register.

DWord	Bit	Description
0	31:16	**Spares** Access: RO
	15:8	**Graphics Mode Select** Default Value: 3h Access: RO This field selects the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. 0h: No memory pre-allocated. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device 2 function 0 Class Code register is 80. 1h-4h: Reserved. 5h-Dh: DVMT (UMA) mode, memory pre-allocated for frame buffer, in quantities as shown in the Encoding table. Eh-Fh: Reserved. NOTE: This register is locked and becomes Read Only when the D_LCK bit in the SMRAMC register is set. This register is also LT lockable. Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled. BIOS Requirement: BIOS must not set this field to 0h if IVD (bit 1 of this register) is 0.
	7:6	**GTT Graphics Memory Size** Access: RO This field selects the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. GSM is assumed to be a contiguous physical DRAM space with DSM, and BIOS needs to allocate a contiguous memory chunk. Hardware derives the base of GSM from DSM only using the GSM size programmed in the register. 0h: No memory pre-allocated. GTT cycles (Mem and IO) are not claimed. 1h: 2 MB of memory pre-allocated for GTT. 2h: 4 MB of memory pre-allocated for GTT.

		3h: 8 MB of memory pre-allocated for GTT. Hardware functionality in case of programming this value to Reserved is not guaranteed. This register is locked and becomes Read Only when the D_LCK bit in the SMRAMC register is set.
	5:3	**Spares2** Access: RO
	2	**Versatile Acceleration Mode Enable** Access: RO Enables the use of the iGFX engines for Versatile Acceleration. 1 - iGFX engines are in Versatile Acceleration Mode. Device 2 Class Code is 048000h. 0 - iGFX engines are in iGFX Mode. Device 2 Class Code is 030000h.
	1	**IGD VGA Disable** Access: RO 0: Enable. Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00. 1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device 2 function 0 Class Code register is 80. BIOS Requirement: BIOS must not set this bit to 0 if the GMS field (bits 6:4 of this register) pre-allocates no memory. This bit MUST be set to 1 if Device 2 is disabled either via a fuse or fuse override (CAPID0[46] = 1) or via a register (DEVEN[3] = 0). This register is locked by LT lock.
	0	**Spares3** Access: RO

Mirror of Graphics Translation Table and Memory Mapped Range Address (31:0)

GTTMMADR_LSB - Mirror of Graphics Translation Table and Memory Mapped Range Address (31:0)

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	09124h

This register requests allocation for the combined Graphics Translation Table Modification Range and Memory Mapped Range. The range requires 4 MB combined for MMIO and Global GTT aperture, with 2MB of that used by MMIO and 2MB used by GTT. GTTADR begins at (GTTMMADR + 2 MB) while the MMIO base address is the same as GTTMMADR.
For the Global GTT, this range is defined as a memory BAR in graphics device config space. It is an alias into which software is required to write Page Table Entry values (PTEs). Software may read PTE values from the global Graphics Translation Table (GTT). PTEs cannot be written directly into the global GTT memory area.
The device snoops writes to this region in order to invalidate any cached translations within the various TLBs implemented on-chip. There are some exceptions to this - see GTT-TLB in the Programming Interface chapter.
The allocation is for 4MB and the base address is defined by bits [38:22].

DWord	Bit	Description
0	31:22	**Memory Base Address (LSB - 31:22 of 38:22)** Access: RO Set by the OS, these bits correspond to address signals [38:22]. 4MB combined for MMIO and Global GTT table aperture (2MB for MMIO and 2 MB for GTT).
	21:4	**Spares** Access: RO
	3	**Prefetchable Memory** Access: RO Hardwired to 0 to prevent prefetching.
	2:1	**Memory Type** Access: RO 00b: To indicate 32 bit base address. 01b: Reserved. 10b: To indicate 64 bit base address. 11b: Reserved.

GTTMMADR_LSB - Mirror of Graphics Translation Table and Memory Mapped Range Address (31:0)		
	0	**Memory I/O Space** Access: RO Hardwired to 0 to indicate memory space.

Mirror of Graphics Translation Table and Memory Mapped Range Address UDW

GTTMMADR_MSB - Mirror of Graphics Translation Table and Memory Mapped Range Address UDW

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	09128h

This register requests allocation for the combined Graphics Translation Table Modification Range and Memory Mapped Range. The range requires 4 MB combined for MMIO and Global GTT aperture, with 2MB of that used by MMIO and 2MB used by GTT. GTTADR begins at (GTTMMADR + 2 MB) while the MMIO base address is the same as GTTMMADR.
For the Global GTT, this range is defined as a memory BAR in graphics device config space. It is an alias into which software is required to write Page Table Entry values (PTEs). Software may read PTE values from the global Graphics Translation Table (GTT). PTEs cannot be written directly into the global GTT memory area.
The device snoops writes to this region in order to invalidate any cached translations within the various TLBs implemented on-chip. There are some exceptions to this - see GTT-TLB in the Programming Interface chapter.
The allocation is for 4MB and the base address is defined by bits [38:22].

DWord	Bit	Description
0	31:7	**Spares** Access: RO
	6:0	**Memory Base Address (MSB - 38:32 of 38:22)** Access: RO Set by the OS, these bits correspond to address signals [38:22]. 4MB combined for MMIO and Global GTT table aperture (2MB for MMIO and 2 MB for GTT).

Mirror of GSMBASE

MBGSM - Mirror of GSMBASE		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	64	
Address:	090D8h	
This register contains the base address of stolen DRAM memory for the GTT.		
DWord	**Bit**	**Description**
0	63:20	**GSM Base** Access: RO This register contains the base address of stolen DRAM memory for the GTT.
	19:0	**Spares** Access: RO

Mirror of GT Slice Enable Fuses

MIRROR_GT_SLICE_EN - Mirror of GT Slice Enable Fuses

Register Space: MMIO: 0/2/0

Source: BSpec

Size (in bits): 32

Address: 09138h

DWord	Bit	Description
0	31:8	**RSVD**
	7:0	**GT slice Enable Fuses** Access: RO **Description** Slice Enable Fuses Bit0 - Slice 0 Enabled Bit1 - Slice;1 Enabled Likewise; Bit7 - Slice;7 Enabled **Programming Notes** Bit values of;1 indicate enabled. Bit values of;0 indicate disabled.

Mirror of GT Sub Slice Disable Fuses

MIRROR_GT_SUBSLICE_DISABLE - Mirror of GT Sub Slice Disable Fuses

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0913Ch

DWord	Bit	Description
0	31:0	**GT sub slice disable Fuses** Access: RO **Description** Sub SliceDisable Fuses Encoding for PBY:- 32'h0000 = All Sub-Slices Enabled Note: Encoding starts with bit 0 mapped to sub-slice0 of slice0 and goes on. See below for elaborated mapping note- bit0 - Sub Slice 0 of Slice 0 bit1 - Sub Slice 1 of Slice 0 Likewise - bit7- Sub Slice 7 of Slice 0 **Programming Notes** Bit values of 1 indicate disabled. Bit values of 0 indicate Enabled

Mirror of GT VEBOX and VDBOX Disable

MIRROR_GT_VEBOX_VDBOX_DISABLE - Mirror of GT VEBOX and VDBOX Disable

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	09140h

Mirror of GT VEBOX and VDBOX Disable

DWord	Bit	Description
0	31:20	**RSVD** Access: RO
	19:16	**GT VEBOX DISABLE** VEBOX config fuses encoding:- bit 0 = VEBOX 0 disabled bit 1 = VEBOX 1 disabled bit 2 = VEBOX 2 disabled bit 3 = VEBOX 3 disabled **Programming Notes** Bit values of 0 indicate enabled. Bit values of 1 indicate disabled.
	15:8	**RSVD**
	7:0	**GT VDBOX DISABLE** Access: RO VDBOX config fuses encoding:- bit 0 = VDBOX 0 disabled bit 1 = VDBOX 1 disabled Likewise, bit 7 = VDBOX 7 disabled **Programming Notes** Bit values of 0 indicate enabled. Bit values of 1 indicate disabled.

Mirror of PCICMD MAE/BME

PCICMD - Mirror of PCICMD MAE/BME

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0912Ch

DWord	Bit	Description
0	31:11	**Spare** Access: R/W
	10	**Interrupt Disable** Access: R/W This bit disables the device from asserting INTx#. 0: Enable the assertion of this device's INTx# signal. 1: Disable the assertion of this device's INTx# signal. DO_INTx messages are not sent to DMI. GSA Implementation: When 1, blocks the sending of an MSI interrupt and blocks the sending of a Line interrupt. (The interrupt status is not blocked from being reflected in the INTSTS bit.) When 0, permits the sending of an MSI interrupt or Line interrupt.
	9	**Fast Back to Back** Access: R/W Not Implemented. Hardwired to 0.
	8	**SERR Enable** Access: R/W Not Implemented. Hardwired to 0.
	7	**Address/Data Stepping Enable** Access: R/W Not Implemented. Hardwired to 0.
	6	**Parity Error Enable** Access: R/W Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.
	5	**Video Pallete Snooping**

PCICMD - Mirror of PCICMD MAE/BME

		Access: R/W This bit is hardwired to 0 to disable snooping.
	4	**Memory Write and Invalidate Enable** Access: R/W Hardwired to 0. The IGD does not support memory write and invalidate commands.
	3	**Special Cycle Enable** Access: R/W This bit is hardwired to 0. The IGD ignores Special cycles.
	2	**Bus Master Enable** Access: R/W 0: Disable IGD bus mastering. 1: Enable the IGD to function as a PCI compliant master. GSA Implementation: When 0, blocks the sending of MSI interrupts. When 1, permits the sending of above. (Note: See descriptions of the INTDIS, MSE, and INTSTS bits.)
	1	**Memory Access Enable** Access: R/W This bit controls the IGD's response to memory space accesses. 0: Disable. 1: Enable.
	0	**I/O Access Enable** Access: R/W This bit controls the IGD's response to I/O space accesses. 0: Disable. 1: Enable.

Misc Clocking Reset Control Registers

MISCCPCTL - Misc Clocking Reset Control Registers

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	09424h

Miscellaneous Clocking / Reset Control Registers

DWord	Bit	Description
0	31	**clock gate control Lock** Access: R/W Lock 0 = Bits of MISCCPCTL register are R/W 1 = All bits of MISCCPCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:24	**Bonus ECO bits** Access: R/W Bonus ECO bits
	23:20	**DOP clock gating enable for VEbox clks** Access: R/W Controls the Enabling of the DOP-level Vebox (cv0clk) Clock Gating via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled Bit20 : vebox(cvclk) clock gate control for vesfcbox0 Bit21 : vebox(cvclk) clock gate control for vesfcbox1 Bit22 : vebox(cvclk) clock gate control for vesfcbox2 Bit23 : vebox(cvclk) clock gate control for vesfcbox3
	19:16	**DOP clock gating enable for SFC media clks** Access: R/W Controls the Enabling of the DOP-level SFC (csfcclk) Clock Gating in media1 via PM event messages 1 - Clock gating is enabled

		0 - Clock gating is disabled Bit16 : SFC clock gate control for vesfcbox0 Bit17 : SFC clock gate control for vesfcbox1 Bit18 : SFC clock gate control for vesfcbox2 Bit19 : SFC clock gate control for vesfcbox3
	15:8	**DOP clock gate enable for Media Clocks** Access: R/W Controls the Enabling of the DOP-level Render (cmclk) Clock Gating via PM event messages Bit8 : media clock gate control for vdbox0 Bit9 : media clock gate control for vdbox1 Bit10 : media clock gate control for vdbox2 Bit11 : media clock gate control for vdbox3 Bit12 : media clock gate control for vdbox4 Bit13 : media clock gate control for vdbox5 Bit14 : media clock gate control for vdbox6 Bit15 : media clock gate control for vdbox7 1 - Clock gating is enabled 0 - Clock gating is disabled
	7	**DOP clock gating enable for posh clks** Access: R/W Controls the Enabling of the DOP-level posh (cposclk) Clock Gating via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled
	6	**DOP clock gating enable for Media ampler clks** Access: R/W Controls the Enabling of the DOP-level Media sampler (scmsclk) Clock Gating via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled
	5	**WIDI1 DOP clock gating enable** Access: R/W Controls the Enabling of the DOP-level Media sampler (cw1clk) Clock Gating via PM event messages 1 - Clock gating is enabled

		0 - Clock gating is disabled
	4	**DOP CLock gating Enable for Widi 0 clocks** Access: R/W Controls the Enabling of the DOP-level Render (cwclk) Clock Gating via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled
	3	**Reserved**
	2	**DOP clock gating Enable for Fix clocks (cfclk)** Access: R/W Controls the Enabling of the DOP-level Render (cfclk/cf2xclk) Clock Gating via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled
	1	**DOP Clock Gating Enable for Render Clocks** Access: R/W Controls the Enabling of the DOP-level Render (crclk/cr2xclk) Clock Gating via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled
	0	**L1 Clock Ungate Enabling Control During Reset** Default Value: 1b Access: R/W Control to enable/disable L1 clock gating during soft resets and FLR reset processing '0' : Clock Gating Enabled during reset flows (i.e., clocks can be gated when they are not required to toggle for functionality, NOT Recommended) '1' : Clock Gating Disabled during reset flows. (i.e., clocks are toggling, always) Register bit defaults to value 1'b1, which is a requirement due to Synchronous reset flops Randomizing this bit will result in X flush not completing during the simulation

MMIO_INDEX

MMIO_INDEX - MMIO_INDEX

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00000h

Contains address and target.
Punit cannot access IO space from message channel.
A 32 bit IO write to this port loads the offset of the MMIO register or offset into the GTT that needs to be accessed.
An IO Read returns the current value of this register. An 8/16 bit IO write to this register is completed but does not update this register.
This mechanism to access internal graphics MMIO registers must not be used to access VGA IO registers which are mapped through the MMIO space. VGA registers must be accessed directly through the dedicated VGA IO ports. This is used by SBIOS. It is not used by graphics driver.
This register is only accessible through the IOSF Primary bus. The base register is defined by IOBAR.

DWord	Bit	Description
0	31:2	**Register_offset** Default Value: 00000000h Access: R/W This field selects GTT entry or any one of the Dword registers within the MMIO register space of this device.
	1:0	**Target** Default Value: 00b Access: R/W 00 = MMIO Registers, 01 = GTT, 1X = Reserved

Mode Register for GAB

GAB_MODE - Mode Register for GAB

Register Space:	MMIO: 0/2/0
Source:	BlitterCS
Access:	R/W
Size (in bits):	32
Address:	220A0h-220A3h

The GAB_MODE register contains information that controls configurations in the GAB.

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask
	15:7	**Reserved** Format: PBC Read/Write
	5:3	**BLB Arbitration Priority** Format: U3
	2:0	**BCS Arbitration Priority** Format: U3

Mode Register for GAC

GAC_MODE - Mode Register for GAC	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	R/W
Size (in bits):	32
Address:	1C00A0h-1C00A3h
Name:	Mode Register for GAC
ShortName:	GAC_MODE_VCSUNIT0
Address:	1C40A0h-1C40A3h
Name:	Mode Register for GAC
ShortName:	GAC_MODE_VCSUNIT1
Address:	1D00A0h-1D00A3h
Name:	Mode Register for GAC
ShortName:	GAC_MODE_VCSUNIT2
Address:	1D40A0h-1D40A3h
Name:	Mode Register for GAC
ShortName:	GAC_MODE_VCSUNIT3
Address:	1E00A0h-1E00A3h
Name:	Mode Register for GAC
ShortName:	GAC_MODE_VCSUNIT4
Address:	1E40A0h-1E40A3h
Name:	Mode Register for GAC
ShortName:	GAC_MODE_VCSUNIT5
Address:	1F00A0h-1F00A3h
Name:	Mode Register for GAC
ShortName:	GAC_MODE_VCSUNIT6

GAC_MODE - Mode Register for GAC

Address: 1F40A0h-1F40A3h
Name: Mode Register for GAC
ShortName: GAC_MODE_VCSUNIT7

The GAC_MODE register contains information that controls configurations in the GAC.

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask
	15:1	**Reserved** Access: R/W
	0	**GACunit VCS Fence Performance fix Override** Format: Disable

Value	Name	Description
0	**[Default]**	Performance fix **enabled** to block client credits until VCS fence advances.
1		Performance fix to block credits until VCS fence advances, **disabled.** Fence will not block input traffic from clients and will advance only after ingress FIFOs are empty (Legacy behavior.)

Mode Register for GAFS

GAFS_MODE - Mode Register for GAFS

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	0212Ch

DWord	Bit	Description
0	31:16	**Mask Bits** Access: WO Format: Mask Masks: These bits serve as write enables for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.
	15:13	**Reserved** Format: PBC
	12:11	**CLR0 clients ROB low priority threshold Control** This bit field is used to control the threshold at which CLR0 clients will move to the low priority group in the GAFS ROB arbiter. 00b **[Default]** Low priority threshold value = 'd12 01b Low priority threshold value = 'd24 10b Low priority threshold value = 'd36 11b Low priority threshold value = 'd48
	10	**Reserved** Format: PBC
	9	**Min Alloc Configuration** This field can be used to adjust min alloc settings in the read ROB structure in GAFS. This is used in conjunction with bit [2] of this register. {Bit[9], Bit[2]} = 2'b00 : Original values

GAFS_MODE - Mode Register for GAFS

		{Bit[9], Bit[2]} = 2'b01 : Override original values to gain 12 ROB locations for generic use {Bit[9], Bit[2]} = 2'b10 :Override original values to gain 22 ROB locations for generic use {Bit[9], Bit[2]} = 2'b11 : Original values **Programming Notes** This bit must be programmed to 1 for achieving performance targets.
	8:3	**Reserved** Format: PBC
	2	**Min Alloc Configuration control0** This field can be used to adjust min alloc settings in the read ROB structure in GAFS. This is used in conjunction with bit [9] of this register. {Bit[9], Bit[2]} = 2'b00 : Original values {Bit[9], Bit[2]} = 2'b01 : Override original values to gain 12 ROB locations for generic use {Bit[9], Bit[2]} = 2'b10 :Override original values to gain 22 ROB locations for generic use {Bit[9], Bit[2]} = 2'b11 : Original values **Programming Notes** This bit must be programmed to 0 for achieving performance targets.
	1:0	**Reserved** Format: PBC

Mode Register for Software Interface

MI_MODE - Mode Register for Software Interface	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0209Ch-0209Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_RCSUNIT
Address:	1809Ch-1809Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_POCSUNIT
Address:	2209Ch-2209Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_BCSUNIT
Address:	1C009Ch-1C009Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_VCSUNIT0
Address:	1C409Ch-1C409Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_VCSUNIT1
Address:	1C809Ch-1C809Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_VECSUNIT0
Address:	1D009Ch-1D009Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_VCSUNIT2
Address:	1D409Ch-1D409Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_VCSUNIT3
Address:	1D809Ch-1D809Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_VECSUNIT1

MI_MODE - Mode Register for Software Interface

Address:	1E009Ch-1E009Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_VCSUNIT4

Address:	1E409Ch-1E409Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_VCSUNIT5

Address:	1E809Ch-1E809Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_VECSUNIT2

Address:	1F009Ch-1F009Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_VCSUNIT6

Address:	1F409Ch-1F409Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_VCSUNIT7

Address:	1F809Ch-1F809Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_VECSUNIT3

The MI_MODE register contains information that controls software interface aspects of the Memory Interface function.

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask A 1 in a bit in this field allows the modification of the corresponding bit in Bits 15:0
	15	**Suspend Flush** Format: U1

Value	Name	Description
0h	No Delay **[Default]**	HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well
1h	Delay Flush	Suspend flush is active

Programming Notes
This should only be written to from the ring using MI_SUSPEND_FLUSH. It is considered undefined if written by software through MMIO

MI_MODE - Mode Register for Software Interface

14 **RCS POSH LRCA Disable**

Source:	RenderCS
Exists If:	//RCS

This bit controls the context save of the MI_LOAD_REGISTER_IMM command corresponding to POSH_LRCA as part of the RCS context image. This primary purpose of this bit is for backward compatibility for the render context image.

Value	Name	Description
1		RCS saves the MI_LOAD_REGISTER_IMM command corresponding to POSH_LRCA in context image as NOOPs.
0	**[Default]**	RCS saves the MI_LOAD_REGISTER_IMM command corresponding to POSH_LRCA as part of the context image.

13 **Disable MI_SET_CONTEXT for Execution List**

Format:	U1

Value	Name	Description
0h	Allow **[Default]**	Allow MI_SET_CONTEXT in Execlist mode
1h	Disable	Disable MI_SET_CONTEXT in Execlist Mode

12 **Reserved**

Format:	PBC

11 **Invalidate UHPTR enable**

Source:	RenderCS, VideoCS, VideoCS2, VideoEnhancementCS
Exists If:	//RCS, VCS, VECS, BCS
Format:	Enable

If bit set H/W clears the valid bit of UHPTR (2134h, bit 0) when current active head pointer is equal to UHPTR.

11 **Reserved**

Source:	PositionCS
Exists If:	//POCS

10 **Atomic Read Return for MI_COPY_MEM_MEM**

Format:	U1

Value	Name	Description
0h	Disable	Hardware does a regular memory fence write to complete the write to

	[Default]	the destination address before moving to the next instruction.
1h	Enable	Hardware does Atomic Move with Read Return to complete the write to the destination address before moving to the next instruction.

9 **Rings Idle**

Format:	U1

Read Only Status bit

Value	Name	Description
0h	Not Idle **[Default]**	Parser not Idle or Ring Arbiter not Idle.
1h	Idle	Parser Idle and Ring Arbiter Idle.

Programming Notes
Writes to this bit are not allowed.

8 **Stop Rings**

Format:	U1

Value	Name	Description
0h	**[Default]**	Normal Operation.
1h		Parser is turned off and Ring arbitration is turned off.

Programming Notes
Software must set this bit to force the Rings and Command Parser to Idle. Software must read a 1 in the Ring Idle bit after setting this bit to ensure that the hardware is idle.
Software must clear this bit for Rings to resume normal operation.

7:5 **Reserved**

Format:	PBC

4:2 **Reserved**

Source:	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS
Format:	PBC

4:1 **Predicate Enable**

Source:	RenderCS, PositionCS

This field gets set when "MI_SET_PREDICATE" command is parsed by render command streamer. Predicate Disable is the default mode of operation.

Value	Name	Description
0h	Predicate Disable	Predication is Disabled and RCS will process commands as usual.
1h	Predicate on	Following Commands will be NOOPED by RCS only if the

	Result2 clear	MI_PREDICATE_RESULT_2 is clear.
2h	Predicate on Result2 set	Following Commands will be NOOPED by RCS only if the MI_PREDICATE_RESULT_2 is set.
3h	Predicate on Result clear	Following Commands will be NOOPED by RCS only if the MI_PREDICATE_RESULT is clear.
4h	Predicate on Result set	Following Commands will be NOOPED by RCS only if the MI_PREDICATE_RESULT is set.
5h	Predicate when two or more slices enabled	Following Commands will be NOOPED by RCS only when one slice is enabled, NOOPED when more than one slice is enabled.
6h	Predicate when one or three slices enabled	Following Commands will be Executed by RCS only when two slices are enabled, NOOPED when one or three slices are enabled.
7h	Predicate when one or two slices enabled	Following Commands will be Executed by RCS only when all the three slices are enabled, NOOPED when less than three slices are enabled.
Bh	NOOP in RenderCS	When RenderCS parses MI_SET_PREDICATE command with “Predicate Enable” set to “NOOP in RenderCS”, RenderCS NOOP’s all the subsequent commands parsed unconditionally until the predication is disabled/modified using MI_SET_PREDICATE command. Other command streamers (non RenderCS) on parsing MI_SET_PREDICATE command with “Predicate Enable” set to “NOOP in RenderCS” don’t take any action and is equivalent to parsing MI_NOOP command.
Ch	NOOP in PositionCS	When PositionCS parses MI_SET_PREDICATE command with “Predicate Enable” set to “NOOP in PositionCS”, PositionCS NOOP’s all the subsequent commands parsed unconditionally until the predication is disabled/modified using MI_SET_PREDICATE command. Other command streamers (non PositionCS) on parsing MI_SET_PREDICATE command with “Predicate Enable” set to “NOOP in PositionCS” don’t take any action and is equivalent to parsing MI_NOOP command.
8h, 9h, Ah	Reserved	
Dh, Eh	Reserved	
Fh	Predicate Always	Following Commands will be NOOPED by RCS unconditionally.

MI_MODE - Mode Register for Software Interface

		Programming Notes SW must use MI_SET_PREDICATE instead of MMIO access.
	1	**Reserved** Source: BlitterCS Format: PBC
	1	**Reserved** Source: VideoCS, VideoCS2, VideoEnhancementCS Format: PBC
	0	**Reserved** Source: CommandStreamer Format: PBC

NDE_RSTWRN_OPT

NDE_RSTWRN_OPT

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	46408h-4640Bh
Name:	North Display Reset Warn Options
ShortName:	NDE_RSTWRN_OPT
Power:	PG0
Reset:	global

This register is used to control the display behavior on receiving a Reset Warning.

DWord	Bit	Description
0	31:7	**Reserved** Format: MBZ
	6	**Reserved** Format: MBZ
	5	**Reserved**
	4	**RST PCH Handshake En** This field enables the handshake with south display when processing the reset. This applies to all types of DE resets. By default it is disabled and the north display will not wait for south display to acknowledge the reset. Value / Name: 0b – Disable 1b – Enable Programming Notes: This must be set to 1b as part of the display initialization sequence.
	3:0	**Reserved**

NOP Identification Register

NOPID - NOP Identification Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Trusted Type:	1
Address:	02094h-02097h
Name:	NOP Identification Register
ShortName:	NOPID_RCSUNIT
Address:	18094h-18097h
Name:	NOP Identification Register
ShortName:	NOPID_POCSUNIT
Address:	22094h-22097h
Name:	NOP Identification Register
ShortName:	NOPID_BCSUNIT
Address:	1C0094h-1C0097h
Name:	NOP Identification Register
ShortName:	NOPID_VCSUNIT0
Address:	1C4094h-1C4097h
Name:	NOP Identification Register
ShortName:	NOPID_VCSUNIT1
Address:	1C8094h-1C8097h
Name:	NOP Identification Register
ShortName:	NOPID_VECSUNIT0
Address:	1D0094h-1D0097h
Name:	NOP Identification Register
ShortName:	NOPID_VCSUNIT2
Address:	1D4094h-1D4097h
Name:	NOP Identification Register
ShortName:	NOPID_VCSUNIT3
Address:	1D8094h-1D8097h
Name:	NOP Identification Register
ShortName:	NOPID_VECSUNIT1

NOPID - NOP Identification Register

Address:	1E0094h-1E0097h
Name:	NOP Identification Register
ShortName:	NOPID_VCSUNIT4

Address:	1E4094h-1E4097h
Name:	NOP Identification Register
ShortName:	NOPID_VCSUNIT5

Address:	1E8094h-1E8097h
Name:	NOP Identification Register
ShortName:	NOPID_VECSUNIT2

Address:	1F0094h-1F0097h
Name:	NOP Identification Register
ShortName:	NOPID_VCSUNIT6

Address:	1F4094h-1F4097h
Name:	NOP Identification Register
ShortName:	NOPID_VCSUNIT7

Address:	1F8094h-1F8097h
Name:	NOP Identification Register
ShortName:	NOPID_VECSUNIT3

The NOPID register contains the Noop Identification value specified by the last MI_NOOP instruction that enabled this register to be updated.

DWord	Bit	Description
0	31:22	**Reserved** Format: MBZ
	21:0	**Reserved**

Null Range 0 Base Register

NULL_BASE_0 - Null Range 0 Base Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	04050h

DWord	Bit	Description
0	31:21	**Null Range Base Address** Default Value: 00000000000b Access: R/W Lock Base address contents of the Null Range that has to be checked against.
	20:2	**Reserved** Default Value: 00000000000000000b Access: RO
	1	**Null Range Register Lock** Default Value: 0b Access: R/W When set, The null range register is locked. Writes have no impact on the register and reads continue to return the contents. Note that enable and lock can be written in the same cycle, as lock taking effect, the accompanying update to the register will take effect as well.
	0	**Null Range Enable** Default Value: 0b Access: R/W Lock When set, The null range register is enabled. Hardware will detect the accesses falling into null range and treat then as invalid access where writes are dropped and reads are returned with all zero's.

Null Range 1 Base Register

NULL_BASE_1 - Null Range 1 Base Register		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	04054h	
DWord	**Bit**	**Description**
0	31:7	**Reserved** Default Value: 00000000000000000000000b Access: RO
	6:0	**Null Range Base Address** Default Value: 0000000b Access: R/W Lock Base address contents of the Null Range that has to be checked against.

OAG Interrupt Mask Register

OAG_OA_IMR - OAG Interrupt Mask Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0DB14h

The OAIMR register is used by software to control whether OA generates an interrupt or not.

DWord	Bit	Description
0	31:29	**Reserved** Default Value: 7h Format: PBC
	28	**Mask Bit** 0h – Not Masked – May generate an interrupt 1h – Masked **[Default]** – Will not generate an interrupt
	27:0	**Reserved** Default Value: FFFFFFFh Format: PBC

OA Interrupt Mask Register

OA_IMR - OA Interrupt Mask Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02B20h

The OAIMR register is used by software to control whether OA generates an interrupt or not.

DWord	Bit	Description
0	31:29	**Reserved** Default Value: 7h Format: PBC
	28	**Mask Bit** 0h – Not Masked – May generate an interrupt 1h – Masked **[Default]** – Will not generate an interrupt
	27:0	**Reserved** Default Value: FFFFFFFh Format: PBC

Observation Architecture Buffer

OABUFFER - Observation Architecture Buffer

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	02B14h
Access:	R/W

This register is used to program the OA unit.

Programming Notes

This MMIO must be set before the OATAILPTR register and set after the OAHEADPTR register. This is to enable proper functionality of the overflow bit.

DWord	Bit	Description
0	31:6	**Report Buffer Offset** This field specifies 64B aligned GFX MEM address where the chap counter values are reported.
	5:3	**Inter Trigger Report Buffer Size** This field indicates the size of report buffer for time/event-based report trigger mechanisms. This field is programmed in terms of multiple of 128KB.

Value	Name	Description
0h	128 KB **[Default]**	All context considered
1h	256 KB	
2h	512 KB	
3h	1 MB	
4h	2 MB	
5h	4 MB	
6h	8 MB	
7h	16 MB	

	2	**OA Report Trigger Select**

Value	Name	Description
0		Level Report trigger
1		Edge Report trigger

	1	**Disable Overrun Mode**

Format:	Enable

This field defines the mode of reporting for internal trigger/timer based reporting. When this bit is set, overrun does not lose reports but stops reporting. Based on the head and tail pointer, when HW detects room for the report, it would resume reporting to the buffer. This mode would not set the over-run bit in the register. When this mode bit is reset, buffer overrun can happen and lose the reports while setting the buffer over-run bit.

Value	Name	Description
0h	Disable **[Default]**	Counter gets written out on regular intervals, defined by the Timer Period
1h	Enable	Counter does not get written out on regular interval

0 **Memory Select PPGTT/GGTT Access**

Value	Name
0h	PPGTT
1h	GGTT **[Default]**

Programming Notes
When each context has its own Per Process GTT, this field should be always set to GGTT. Since all known drivers use PPGTT today, OABUFFER using PPGTT memory is a deprecated configuration.

Observation Architecture Control

OACONTROL - Observation Architecture Control

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02B00h
Name:	Observation Architecture Control
ShortName:	OACONTROL

This register controls global OA functionality, report format, interrupt steering and context filtering.

DWord	Bit	Description
0	31:6	**Reserved** Format: PBC
	5	**Reserved**
	4:2	**Counter Select** This field selects which performance counter report format to use, please refer to Performance Counter Report Formats section for more details on the structure of the format.
	1	**Specific Context Enable** Format: Enable **Description** Enables counters to work on a context specific workload. The context is given by bits 31:12. OA unit level clock gating must be ENABLED when using specific ContextID feature. When "Specific Context Enable" bit is set to '1' in OACONTROL register, Boolean/Threshold report trigger function gets enabled only for the selected context. When "Specific Context Enable" bit is set to '0' in OACONTROL register, Boolean/Threshold report trigger function gets enabled for all contexts. When "Specific Context Enable" bit is set to '1' in OACONTROL register, Timer based report trigger function gets enabled only for the selected context. When "Specific Context Enable" bit is set to '0' in OACONTROL register, Timer based report trigger function gets enabled for all

contexts.

Value	Name	Description
0h	Disable **[Default]**	All contexts are considered
1h	Enable	Only the contexts with the Select Context ID field in OACTXID are considered

0 **Performance Counter Enable**

Format:	Enable

Global performance counter enable. If clear, no counting will occur. MI_REPORT_PERF_COUNT is undefined when clear.

Programming Notes
When this bit is set, OABUFFER, OAHEADPTR and OATAILPTR must be programmed correctly to ensure report triggers due to Context Switch and GO transition happen correctly.

Observation Architecture Control Context ID

OACTXID - Observation Architecture Control Context ID	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	32
Address:	02364h
Name:	Observation Architecture Control Context ID
ShortName:	OACTXID

This register has the context details when Specific context Enable is set. This register is implemented in render command streamer and render context save/restored. This register should be initialized by SW appropriately on the very first submission of a context when OA is enabled.

DWord	Bit	Description
0	31:0	**Select Context ID** Specifies the context ID of the one context that affects the performance counters when "Specific Context Enable" bit is set. All other contexts are ignored. **Ring Buffer Mode of Scheduling:** Bits[31:12] represent the CCID and bits [11:0] must be zero. **Execlist mode of scheduling:** Bits[31:0] represent the context id.

Observation Architecture Control per Context

OACTXCONTROL - Observation Architecture Control per Context

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	32
Address:	02360h
Name:	Observation Architecture Control per Context
ShortName:	OACTXCONTROL

This register is implemented in render command streamer and render context save/restored. This register should be initialized by SW appropriately on the very first submission of a context when OA is enabled.

DWord	Bit	Description
0	31	**Reserved** Format: PBC
	30:8	**Reserved** Format: PBC
	7:2	**Timer Period** Specifies the period of the timer strobe as a function of the minimum TIME_STAMP resolution. The period is determined by selecting a specified bit from the TIME_STAMP register as follows: StrobePeriod = MinimumTimeStampPeriod * 2 **(TimerPeriod + 1)** The exponent is defined by this field. **Note:** The TIME_STAMP is not reset at start time so the phase of the strobe is not synchronized with the enable of the OA unit. This could result in approximately a full StrobePeriod elapsing prior to the first trigger. Usage for this mechanism should be time based periodic triggering, typically.
	1	**Timer Enable** **Description** This field enables the timer logic to output a periodic strobe, as defined by the Timer Period. When disabled the timer output is not asserted. Users should be aware that the timer-based report logic and the Boolean report trigger logic are logically OR'd together with no buffering of report triggers. This implies that only one performance counter report will be generated for clocks where both the timer-based report logic and the Boolean report trigger logic trigger a performance counter report. When "Specific Context Enable" bit is set to '1' in OACONTROL register, Timer based report trigger function gets enabled only for the selected context. When "Specific Context Enable" bit is

set to '0' in OACONTROL register, Timer based report trigger function gets enabled for all contexts.

Value	Name	Description
0h	Disable **[Default]**	Counter does not get written out on regular interval
1h	Enable	Counter gets written out on regular intervals, defined by the Timer Period

0 **Counter Stop-Resume Mechanism**

Value	Name	Description
1h		resume counting for all counters

Observation Architecture Head Pointer

OAHEADPTR - Observation Architecture Head Pointer		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Access:	R/W	
Size (in bits):	32	
Address:	02B0Ch	
This register allows SW to program head pointer.		
DWord	**Bit**	**Description**
0	31:6	**Head Pointer** Virtual address of the internal trigger based buffer that is updated by software after consuming reports from the report buffer. This pointer must be updated by SW only when using time or event-based report triggering. **Programming Notes** SW must ensure that Head Pointer and the Tail Pointer match before enabling internally triggered performance counter reporting.
	5:0	**Reserved** Format: PBC

Observation Architecture Report Trigger 2

OAREPORTTRIG2 - Observation Architecture Report Trigger 2

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02744h

Description
This register controls some of the Boolean logic defining Boolean/threshold report trigger 0. The bit definitions in this register refer to the stages in the report trigger block diagram in the Performance Counter Reporting section.
Report triggers generated from OAREPORTTRIG 1-4 and OAREPORTTRIG 5-8 are ORed to form a new report trigger. Report trigger behavior can be derived by programming these two sets of OA REPORT registers with the same value. Users should be aware that while programming Timer based and Threshold Counter based triggers simultaneously for internal reporting, they should be programmed such way that they are not consecutively triggered. If programmed simultaneously, RTL pulse detection logic will have problem when these triggers occur in consecutive clock cycles.

DWord	Bit	Description
0	31	**Report Trigger Enable** Format: Enable **Description** Enable Boolean/threshold report trigger 0. Users should be aware that the timer-based report logic and the Boolean report trigger logic are logically OR'd together with no buffering of report triggers. This implies that only one performance counter report will be generated for clocks where both the timer-based report logic and the Boolean report trigger logic trigger a performance counter report. When "Specific Context Enable" bit set to '1' in OACONTROL register, Boolean/Threshold report trigger function gets enabled only for the selected context. When "Specific Context Enable" bit set to '0' in OACONTROL register, Boolean/Threshold report trigger function gets enabled for all contexts.
	30:24	**Reserved** Format: PBC
	23	**Threshold Enable** Format: Enable Enable the threshold compare logic within the Boolean/threshold report trigger 0 logic (see

OAREPORTTRIG2 - Observation Architecture Report Trigger 2

		block diagram in the Performance Counter Reporting section).
	22	**Invert D Enable 0** Format: Enable Invert the specified signal at the D stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	21	**Invert C Enable 1** Format: Enable Invert the specified signal at the C stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	20	**Invert C Enable 0** Format: Enable Invert the specified signal at the C stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	19	**Invert B Enable 3** Format: Enable Invert the specified signal at the B stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	18	**Invert B Enable 2** Format: Enable Invert the specified signal at the B stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	17	**Invert B Enable 1** Format: Enable Invert the specified signal at the B stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	16	**Invert B Enable 0** Format: Enable Invert the specified signal at the B stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	15	**Invert A Enable 15** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).

OAREPORTTRIG2 - Observation Architecture Report Trigger 2

14	**Invert A Enable 14** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
13	**Invert A Enable 13** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
12	**Invert A Enable 12** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
11	**Invert A Enable 11** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
10	**Invert A Enable 10** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
9	**Invert A Enable 9** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
8	**Invert A Enable 8** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
7	**Invert A Enable 7** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).

OAREPORTTRIG2 - Observation Architecture Report Trigger 2

	6	**Invert A Enable 6** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	5	**Invert A Enable 5** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	4	**Invert A Enable 4** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	3	**Invert A Enable 3** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	2	**Invert A Enable 2** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	1	**Invert A Enable 1** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	0	**Invert A Enable 0** Format: Enable Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).

Observation Architecture Report Trigger 6

OAREPORTTRIG6 - Observation Architecture Report Trigger 6

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02754h

Description

This register controls some of the Boolean logic defining Boolean/threshold report trigger 1. Note that Boolean report triggers 0 and 1 are logically OR'd together without buffering, this implies that only one performance counter report will be generated for clocks where both Boolean report triggers evaluate true. The bit definitions in this register refer to the stages in the report trigger block diagram in the Performance Counter Reporting section.

Report triggers generated from OAREPORTTRIG 1-4 and OAREPORTTRIG 5-8 are ORed to form a new report trigger. Report trigger behavior can be derived by programming these two sets of OA REPORT registers with the same value. Users should be aware that while programming Timer based and Threshold Counter based triggers simultaneously for internal reporting, they should be programmed such way that they are not consecutively triggered. If programmed simultaneously, RTL pulse detection logic will have problem when these triggers occur in consecutive clock cycles.

DWord	Bit	Description
0	31	**Report Trigger Enable** **Description** Enable Boolean/threshold report trigger 0. Users should be aware that the timer-based report logic and the Boolean report trigger logic are logically OR'd together with no buffering of report triggers. This implies that only one performance counter report will be generated for clocks where both the timer-based report logic and the Boolean report trigger logic trigger a performance counter report. When "Specific Context Enable" bit set to '1' in OACONTROL register, Boolean/Threshold report trigger function gets enabled only for the selected context. When "Specific Context Enable" bit set to '0' in OACONTROL register, Boolean/Threshold report trigger function gets enabled for all contexts.
	30:24	**Reserved** Format: PBC
	23	**Threshold Enable** Enable the threshold compare logic within the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	22	**Invert D Enable 0** Invert the specified signal at the D stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).

OAREPORTTRIG6 - Observation Architecture Report Trigger 6		
	21	**Invert C Enable 1** Invert the specified signal at the C stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	20	**Invert C Enable 0** Invert the specified signal at the C stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	19	**Invert B Enable 3** Invert the specified signal at the B stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	18	**Invert B Enable 2** Invert the specified signal at the B stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	17	**Invert B Enable 1** Invert the specified signal at the B stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	16	**Invert B Enable 0** Invert the specified signal at the B stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	15	**Invert A Enable 15** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	14	**Invert A Enable 14** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	13	**Invert A Enable 13** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	12	**Invert A Enable 12** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	11	**Invert A Enable 11** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	10	**Invert A Enable 10** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	9	**Invert A Enable 9** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	8	**Invert A Enable 8** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).

OAREPORTTRIG6 - Observation Architecture Report Trigger 6		
	7	**Invert A Enable 7** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	6	**Invert A Enable 6** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	5	**Invert A Enable 5** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	4	**Invert A Enable 4** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	3	**Invert A Enable 3** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	2	**Invert A Enable 2** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	1	**Invert A Enable 1** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	0	**Invert A Enable 0** Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).

Observation Architecture Report Trigger Counter

OARPTTRIG_COUNTER - Observation Architecture Report Trigger Counter

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02B1Ch

This register provides status of report trigger threshold count 1 and 2. This register is for HW internal purpose and power context save/restored. This register must not be programmed by SW.

DWord	Bit	Description
0	31:16	**Report Trig Threshold Count 1 Status** **Programming Notes** This field is for HW internal use to context save/restore rpt trigger threshold count 1. It always indicates current value of HW's internal report trigger count. SW should not program these bits.
	15:0	**Report Trig Threshold count 2 status** **Programming Notes** This field is for HW internal use to context save/restore rpt trigger threshold count 2. It always indicates current value of HW's internal report trigger count. SW should not program these bits.

Observation Architecture Start Trigger 5

OASTARTTRIG5 - Observation Architecture Start Trigger 5	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02720h

This register provides the threshold value optionally used to define the start trigger for B7-B4 counters. Note that the value in this register must match the value in OASTARTTRIG1 to have B7-B0 start at the same time. The bit definition in this register refers to the stages in the start trigger block diagram in the Performance Counter Reporting section.

DWord	Bit	Description
0	31:16	**Reserved** Format: PBC
	15:0	**Threshold Value** Format: U16 **Programming Notes** Threshold value for the compare logic within the start trigger logic for B7-B4 counters.

Observation Architecture Start Trigger Counter

OASTARTTRIG_COUNTER - Observation Architecture Start Trigger Counter

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02B18h

This register provides status of start trigger threshold count 1 and 2. This register is for HW internal purpose.

DWord	Bit	Description
0	31:16	**Start Trig Threshold Count 1 Status** **Programming Notes** This field is for HW internal use to context save/restore start trigger threshold count 1. It always indicates current value of HW's internal start trigger count. SW should not program these bits.
	15:0	**Start Trig Threshold count 2 status** **Programming Notes** : This field is for HW internal use to context save/restore start trigger threshold count 2. It always indicates current value of HW's internal start trigger count. SW should not program these bits.

Observation Architecture Status Register

OASTATUS - Observation Architecture Status Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02B08h

This register provides status of report buffer and overflow conditions as well as status of some flags which hardware needs for internal purpose. Software should not program these status bits.

DWord	Bit	Description
0	31:22	**Reserved** Default Value: 0 Format: PBC
	21	**Start Trigger Flag 1** Value / Name: 0 **[Default]** 1 **Programming Notes** This bit is for HW internal use to context save /restore Start Trigger 1 occurrence On RC6 entry. Software should not program this bit.
	20	**Start Trigger Flag 2** Value / Name: 0 **[Default]** 1 **Programming Notes** This bit is for HW internal use to context save /restore Start Trigger 2 occurrence On RC6 entry. Software should not program this bit.
	19	**Report Trigger Flag 1** Value / Name: 0 **[Default]** 1 **Programming Notes**

OASTATUS - Observation Architecture Status Register

	This bit is for HW internal use to context save /restore Report Trigger 1 occurrence On RC6 entry. Software should not program this bit.
18	**Report Trigger Flag 2** **Value** / **Name** 0 / **[Default]** 1 / **Programming Notes** This bit is for HW internal use to context save /restore Report Trigger 2 occurrence On RC6 entry. Software should not program this bit.
17	**Tail Pointer Wrap Flag** Format: U1 **Value** / **Name** 0 / 1 / **[Default]** **Programming Notes** This bit is for HW internal use to context save /restore Tail Pointer Wrap Flag. SW should not program this bit. This bit gets programmed only when Tail Pointer Wrap Mask bit is set.
16	**Head Pointer Wrap Flag** Format: U1 **Value** / **Name** 0 / 1 / **[Default]** **Programming Notes** This bit is for HW internal use to context save /restore Head Pointer Wrap Flag. SW should not program this bit. This bit gets programmed only when Head Pointer Wrap Mask bit is set.
15:6	**Reserved** Default Value: 0 Format: PBC
5	**Reserved** Default Value: 0 Format: PBC
4	**Accumulator Overflow** This field indicates that the one or more event accumulator inside the slice-OAunit has

OASTATUS - Observation Architecture Status Register

overflowed. Once set, this bit will remain set, until SW resets it by either soft reset or writing a 0 to it.

Value	Name	Description
0	**[Default]**	No overflow has occurred.
1		Overflow has occurred.

3 Overrun Status

This field indicates the status of overrun. This bit is read only and writing to this bit will have no effect. This bit will reflect the status of overrun irrespective of Overrun Mode enabled or disabled.

Value	Name
0	**[Default]**
1	

2 Counter Overflow

This bit is set if any of the counters overflows. This bit can be reset by SW by either soft reset or writing a 1 to it.

Value	Name
0	**[Default]**
1	

1 Buffer Overflow

This bit is set when the Tail-pointer - Head pointer > max internal trigger buffer size

Value	Name
0h	**[Default]**
1	

0 Report Lost Error

Format:	Enable

This bit is set if the Report Trigger due to "Internal Report Trigger-1", "Internal Report Trigger-2" or "Timer Triggered" to write out the counter values is dropped, while there is an ongoing report in progress. The report request is ignored and the counter continue to count.

Value	Name
0	**[Default]**
1	

Programming Notes
This bit can be reset by SW by either soft reset or writing a 1 to it.

Observation Architecture Tail Pointer

OATAILPTR - Observation Architecture Tail Pointer		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Access:	R/W	
Size (in bits):	32	
Address:	02B10h	
This register allows software to program tail pointer and also indicates current tail pointer value.		
DWord	**Bit**	**Description**
0	31:6	**Tail Pointer** Virtual address of the internal trigger based buffer that is updated for every 64B cacheline write to memory when reporting via internal report trigger. This pointer will not be updated for MI_REPORT_PERF_COUNT command based writes. **Programming Notes** Before enabling internally triggered performance counter reporting, SW must ensure that this address matches the Report Buffer Offset programmed in OABUFFER register (i.e. tail pointer must start at the beginning of the report buffer). SW must ensure that Tail pointer and the Head Pointer match before enabling internally triggered performance counter reporting.
	5:0	**Reserved** Format: PBC

OUTPUT_CSC_COEFF

OUTPUT_CSC_COEFF		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Access:	Double Buffered	
Size (in bits):	192	
Double Buffer Update Point:	Start of vertical blank after armed	
Double Buffer Armed By:	Write to CSC_MODE	
Address:	49050h-49067h	
Name:	Pipe Output CSC Coefficients	
ShortName:	OUTPUT_CSC_COEFF_A	
Power:	PG1	
Reset:	soft	
Address:	49150h-49167h	
Name:	Pipe Output CSC Coefficients	
ShortName:	OUTPUT_CSC_COEFF_B	
Power:	PG2	
Reset:	soft	
Address:	49250h-49267h	
Name:	Pipe Output CSC Coefficients	
ShortName:	OUTPUT_CSC_COEFF_C	
Power:	PG2	
Reset:	soft	

DWord	Bit	Description
0	31:16	**RY** Format: CSC COEFFICIENT FORMAT
	15:0	**GY** Format: CSC COEFFICIENT FORMAT
1	31:16	**BY** Format: CSC COEFFICIENT FORMAT
	15:0	**Reserved**

OUTPUT_CSC_COEFF		
		Format: MBZ
2	31:16	**RU** Format: CSC COEFFICIENT FORMAT
	15:0	**GU** Format: CSC COEFFICIENT FORMAT
3	31:16	**BU** Format: CSC COEFFICIENT FORMAT
	15:0	**Reserved** Format: MBZ
4	31:16	**RV** Format: CSC COEFFICIENT FORMAT
	15:0	**GV** Format: CSC COEFFICIENT FORMAT
5	31:16	**BV** Format: CSC COEFFICIENT FORMAT
	15:0	**Reserved** Format: MBZ

OUTPUT_CSC_POSTOFF

OUTPUT_CSC_POSTOFF	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	96
Double Buffer Update Point:	Start of vertical blank after armed
Double Buffer Armed By:	Write to CSC_MODE
Address:	49074h-4907Fh
Name:	Pipe Output CSC Post-Offsets
ShortName:	OUTPUT_CSC_POSTOFF_A
Power:	PG1
Reset:	soft
Address:	49174h-4917Fh
Name:	Pipe Output CSC Post-Offsets
ShortName:	OUTPUT_CSC_POSTOFF_B
Power:	PG2
Reset:	soft
Address:	49274h-4927Fh
Name:	Pipe Output CSC Post-Offsets
ShortName:	OUTPUT_CSC_POSTOFF_C
Power:	PG2
Reset:	soft

The post-offset is intended to add an offset from 0 on the Y or RGB channels and to convert UV channels from 2's complement to excess 0.5 as they exit pipe output color space conversion (CSC).

DWord	Bit	Description
0	31:13	**Reserved** Format: MBZ
	12:0	**PostCSC High Offset** This value is used to give an offset to the high color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).

OUTPUT_CSC_POSTOFF		
1	31:13	**Reserved** Format: MBZ
	12:0	**PostCSC Medium Offset** This value is used to give an offset to the medium color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
2	31:13	**Reserved** Format: MBZ
	12:0	**PostCSC Low Offset** This value is used to give an offset to the low color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).

OUTPUT_CSC_PREOFF

OUTPUT_CSC_PREOFF	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	96
Double Buffer Update Point:	Start of vertical blank after armed
Double Buffer Armed By:	Write to CSC_MODE
Address:	49068h-49073h
Name:	Pipe Output CSC Pre-Offsets
ShortName:	OUTPUT_CSC_PREOFF_A
Power:	PG1
Reset:	soft
Address:	49168h-49173h
Name:	Pipe Output CSC Pre-Offsets
ShortName:	OUTPUT_CSC_PREOFF_B
Power:	PG2
Reset:	soft
Address:	49268h-49273h
Name:	Pipe Output CSC Pre-Offsets
ShortName:	OUTPUT_CSC_PREOFF_C
Power:	PG2
Reset:	soft

The pre-offset is intended to remove an offset from 0 on the Y or RGB channels and to convert UV channels from excess 0.5 to 2's complement as they enter pipe output color space conversion (CSC).

DWord	Bit	Description
0	31:13	**Reserved** Format: MBZ
	12:0	**PreCSC High Offset** This value is used to give an offset to the high color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).

OUTPUT_CSC_PREOFF		
1	31:13	**Reserved** Format: MBZ
	12:0	**PreCSC Medium Offset** This value is used to give an offset to the medium color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
2	31:13	**Reserved** Format: MBZ
	12:0	**PreCSC Low Offset** This value is used to give an offset to the low color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).

Outstanding Page Request Capacity

OPRC_0_2_0_PCI - Outstanding Page Request Capacity

Register Space:	PCI: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00308h

DWord	Bit	Description
0	31:0	**Outstanding Page Request Capacity** Default Value: 00000000000000001000000000000000b Access: RO This register contains the number of outstanding page request messages the associated Page Request Interface physically supports. This is the upper limit on the number of pages that can be usefully allocated to the Page Request Interface. Hardwired to 32,768 requests.

PAGE_FAULT_MODE

PAGE_FAULT_MODE - PAGE_FAULT_MODE

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0E454h
Name:	PAGE_FAULT_MODE
ShortName:	PAGE_FAULT_MODE

This register is written as part of Context Submission to TDL. The data written is the lower 32 bits of the Context Descriptor Format structure.

DWord	Bit	Description
0	31:8	**Reserved** Default Value: 000000000000000b Access: RO
	7:6	**FAULT_MODE** Access: WO **Fault Model:** Applicable only in advanced context
		Value / Name / Description
		00b / Fault and Hang **[Default]** / In Legacy Context mode, this is the only valid encoding.
		01b / Fault and Halt / Restriction : Only valid in Advanced Context mode.
		010b / Fault and Stream / Restriction : Only valid in Advanced Context mode.
		Others / Reserved /
	5:0	**Reserved**

Page Directory Pointer Descriptor - PDP0/PML4/PASID

PDP0 - Page Directory Pointer Descriptor - PDP0/PML4/PASID	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	64
Address:	02270h-02277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_RCSUNIT
Address:	18270h-18277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_POCSUNIT
Address:	22270h-22277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_BCSUNIT
Address:	1C0270h-1C0277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VCSUNIT0
Address:	1C4270h-1C4277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VCSUNIT1
Address:	1C8270h-1C8277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VECSUNIT0
Address:	1D0270h-1D0277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VCSUNIT2
Address:	1D4270h-1D4277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VCSUNIT3
Address:	1D8270h-1D8277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VECSUNIT1
Address:	1E0270h-1E0277h

PDP0 - Page Directory Pointer Descriptor - PDP0/PML4/PASID

Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VCSUNIT4
Address:	1E4270h-1E4277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VCSUNIT5
Address:	1E8270h-1E8277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VECSUNIT2
Address:	1F0270h-1F0277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VCSUNIT6
Address:	1F4270h-1F4277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VCSUNIT7
Address:	1F8270h-1F8277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VECSUNIT3

PDP0/PML4/PASID: This register can contain three values which depend on the element descriptor definition. **PASID[19:0]:** Populated in the first 20bits of the register and selected when Advanced Context flag is set in the element descriptor in execlist mode of submission. This is not valid in ring buffer mode of scheduling. **PML4[38:12]:** Pointer to base address of PML4 and selected when Legacy Context flag is set and 64b address support is selected. **PDP0[38:12]:** Pointer to one of the four page directory pointer (lowest) and defines the first 0-1GB of memory mapping. This is valid when Legacy Context Flag is set and 64bit virtual addressing is not supported. *Note: This is a guest physical address.*

Programming Notes

Execlist Based Scheduling: SW should update PDP0/12/3 registers in context image with proper values before submitting the context to HW in execlist mode of scheduling. HW restores these registers as part of context restore to set the PPGTT access accordingly. PPGTT is always enabled in advanced context mode of execlist based scheduling and can be disabled only in legacy context mode. Privilege Access Bit in Element Descriptor controls the PPGTT enabling in legacy context mode.

Ring Buffer Based Scheduling: A write via MMIO to PDP0_DESCRIPROR (lower Dword) triggers the Page Directory Restore in HW when PPGTT is enabled. SW should ensure PDP1/2/3 registers are programmed appropriately prior to programming PDP0. PDP0_DESCRIPTOR lower dword should be programmed at the end. Per-Process GTT Enable Bit in GFX_MODE register controls the PPGTT enabling and disabling. Programming Per-Process GTT Enable Bit in GFX_MODE register doesn't enable/disable the PPGTT translation of memory access immediately; the change comes in to affect only when the Page Directory registers are programmed. Programming Per-Process GTT Enable Bit in GFX_MODE register bit must be followed by programming Page Directory Registers in order to enable or disable the PPGTT translation of memory access. PDP* DESCRIPTOR registers must always be programmed through MI_LOAD_REGISTER_IMMEDIATE command in ring buffer with

PDP0 - Page Directory Pointer Descriptor - PDP0/PML4/PASID

PDP0_DESCRIPRTOR lower dword written at the end. PDP0/12/3 registers are context save restored. PDP descriptors are context save restored per render context in RCS and must be programmed following MI_SET_CONTEXT command, in case of PDP descriptors programmed without context set (MI_SET_CONTEXT) will get lost on C6 entry/exit. PDP descriptors are context save restored in VCS, BCS and VECS engines and must be programmed following setup of CCID register, in case of PDP descriptors programmed without CCID set will get lost on C6 entry/exit. PDP descriptor registers should be programmed after ensuring the pipe is completely flushed and TLB's invalidated.

DWord	Bit	Description
0	63	**PD Load Busy** Access: RO This read-only field gets set when PDP0 is written to indicating Page Directory Restore activity is in progress and will get reset once the activity is completed.
	62:0	**PDP0 Descriptor**

Page Directory Pointer Descriptor - PDP1

PDP1 - Page Directory Pointer Descriptor - PDP1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	64
Address:	02278h-0227Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_RCSUNIT
Address:	18278h-1827Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_POCSUNIT
Address:	22278h-2227Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_BCSUNIT
Address:	1C0278h-1C027Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_VCSUNIT0
Address:	1C4278h-1C427Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_VCSUNIT1
Address:	1C8278h-1C827Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_VECSUNIT0
Address:	1D0278h-1D027Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_VCSUNIT2
Address:	1D4278h-1D427Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_VCSUNIT3
Address:	1D8278h-1D827Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_VECSUNIT1
Address:	1E0278h-1E027Fh

PDP1 - Page Directory Pointer Descriptor - PDP1

Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_VCSUNIT4
Address:	1E4278h-1E427Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_VCSUNIT5
Address:	1E8278h-1E827Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_VECSUNIT2
Address:	1F0278h-1F027Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_VCSUNIT6
Address:	1F4278h-1F427Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_VCSUNIT7
Address:	1F8278h-1F827Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_VECSUNIT3

PDP1[38:12]: Pointer to one of the four page directory pointer (lowest+1) and defines the first 1-2GB of memory mapping. This is valid when Legacy Context Flag is set and 64bit virtual addressing is not supported. *Note: This is a guest physical address.*

DWord	Bit	Description
0	63:0	**PDP1 Descriptor**

Page Directory Pointer Descriptor - PDP2

PDP2 - Page Directory Pointer Descriptor - PDP2	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	64
Address:	02280h-02287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_RCSUNIT
Address:	18280h-18287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_POCSUNIT
Address:	22280h-22287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_BCSUNIT
Address:	1C0280h-1C0287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VCSUNIT0
Address:	1C4280h-1C4287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VCSUNIT1
Address:	1C8280h-1C8287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VECSUNIT0
Address:	1D0280h-1D0287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VCSUNIT2
Address:	1D4280h-1D4287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VCSUNIT3
Address:	1D8280h-1D8287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VECSUNIT1
Address:	1E0280h-1E0287h

PDP2 - Page Directory Pointer Descriptor - PDP2

Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VCSUNIT4
Address:	1E4280h-1E4287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VCSUNIT5
Address:	1E8280h-1E8287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VECSUNIT2
Address:	1F0280h-1F0287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VCSUNIT6
Address:	1F4280h-1F4287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VCSUNIT7
Address:	1F8280h-1F8287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VECSUNIT3

PDP2[38:12]: Pointer to one of the four page directory pointer (lowest+2) and defines the first 2-3GB of memory mapping. This is valid when Legacy Context Flag is set and 64bit virtual addressing is not supported. *Note: This is a guest physical address.*

DWord	Bit	Description
0	63:0	**PDP2 Descriptor**

Page Directory Pointer Descriptor - PDP3

PDP3 - Page Directory Pointer Descriptor - PDP3	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	64
Address:	02288h-0228Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_RCSUNIT
Address:	18288h-1828Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_POCSUNIT
Address:	22288h-2228Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_BCSUNIT
Address:	1C0288h-1C028Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VCSUNIT0
Address:	1C4288h-1C428Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VCSUNIT1
Address:	1C8288h-1C828Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VECSUNIT0
Address:	1D0288h-1D028Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VCSUNIT2
Address:	1D4288h-1D428Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VCSUNIT3
Address:	1D8288h-1D828Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VECSUNIT1
Address:	1E0288h-1E028Fh

PDP3 - Page Directory Pointer Descriptor - PDP3

Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VCSUNIT4
Address:	1E4288h-1E428Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VCSUNIT5
Address:	1E8288h-1E828Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VECSUNIT2
Address:	1F0288h-1F028Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VCSUNIT6
Address:	1F4288h-1F428Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VCSUNIT7
Address:	1F8288h-1F828Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VECSUNIT3

PDP3[38:12]: Pointer to one of the four page directory pointer (lowest+3) and defines the first 3-4GB of memory mapping. This is valid when Legacy Context Flag is set and 64bit virtual addressing is not supported. *Note: This is a guest physical address.*

DWord	Bit	Description
0	63:0	**PDP3 Descriptor**

Page Req Queue Tail Shadow Register DW0

PRQTP_DW0 - Page Req Queue Tail Shadow Register DW0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00EC4h-00EC7h	
DWord	**Bit**	**Description**
0	31:0	**TailPtr** Access: R/W Shadow register for Page Req Queue Tail register DW0. Usage: GAM will provide the data which is readable via address F0C8.

Page Req Queue Tail Shadow Register DW1

PRQTP_DW1 - Page Req Queue Tail Shadow Register DW1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00EC8h-00ECBh	
DWord	**Bit**	**Description**
0	31:0	**TailPtr** Access: R/W Shadow register for Page Req Queue Tail register DW1. Usage: GAM will provide the data which is readable via address F0CC.

PAK_NUM_OF_SLICES

PAK_NUM_OF_SLICES - PAK_NUM_OF_SLICES	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12954h
ShortName:	PAK_NUM_OF_SLICES1
Address:	1C954h
ShortName:	PAK_NUM_OF_SLICES2

DWord	Bit	Description
0	31:16	**Reserved** This is Read only register. Read value is zero.
	15:0	**Number of slices in a frame.** This field indicates number of slices in the current frame. This register is updated at the end of each slice.

PAK_Stream-Out Report (Errors)

PAK_ERR - PAK_Stream-Out Report (Errors)	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	128E8h

DWord	Bit	Description
0	31:22	**Reserved** Format: MBZ
	21	**Incorrect IntraMBFlag in I-slice(AVCf)**
	20	**Out of Range Symbol Code(AVC/mpeg2)**
	19	**Incorrect MBType(AVC/mpeg2**
	18	**Motion Vectors are not inside the frame boundary(mpeg2)**
	17	**Scale code is zero(mpeg2)**
	16	**Incorrect DCTtype for given motionType(mpeg2)**
	15:8	**MB Y-position** This field indicates Macro Block(MB) Y- position where an error occurred while encoding.
	7:0	**MB X-position** This field indicates Macro Block(MB) X- position where an error occurred while encoding.

PAK_Stream-Out Report (Warnings)

PAK_WARN - PAK_Stream-Out Report (Warnings)	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	128E4h

DWord	Bit	Description
0	31:22	**Reserved** Format: MBZ
	21	**Skip Run > 8192 (AVC)**
	20	**Incorrect SkipMB (AVC and mpeg2)**
	19	**Incorrect MV difference for dual-prime MB (mpeg2)**
	18	**End of Slice signal missing on last MB of a Row(mpeg2)**
	17	**Incorrect DCT type for field picture**
	16	**MVs are not within defined range by fcode**
	15:8	**MB Y-position**
	7:0	**MB X-position**

PAK Report Running Status

PAK_REPORT_STAT - PAK Report Running Status	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	128ECh

DWord	Bit	Description
0	31:1	**Reserved**
	0	**PAK Status** Value / Name / Description 0 / / PAK engine is IDLE 1 / / PAK engine is currently generating bit stream.

PAL_EXT_GC_MAX

PAL_EXT_GC_MAX	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	96
Address:	4A420h-4A42Bh
Name:	Pipe Extended Gamma Correction Max
ShortName:	PAL_EXT_GC_MAX_A
Power:	PG1
Reset:	soft
Address:	4AC20h-4AC2Bh
Name:	Pipe Extended Gamma Correction Max
ShortName:	PAL_EXT_GC_MAX_B
Power:	PG2
Reset:	soft
Address:	4B420h-4B42Bh
Name:	Pipe Extended Gamma Correction Max
ShortName:	PAL_EXT_GC_MAX_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31:19	**Reserved** Format: MBZ
	18:0	**Red Ext Max GC Point** Default Value: 11111111111111111b Format: U3.16 The extended point for red color channel gamma correction. This value is represented in a 3.16 format with 3 integer and 16 fractional bits.
1	31:19	**Reserved** Format: MBZ
	18:0	**Green Ext Max GC Point** Default Value: 11111111111111111b Format: U3.16 The extended point for green color channel gamma correction. This value is represented in a

PAL_EXT_GC_MAX		
		3.16 format with 3 integer and 16 fractional bits.
2	31:19	**Reserved** Format: MBZ
	18:0	**Blue Ext Max GC Point** Default Value: 11111111111111111b Format: U3.16 The extended point for blue color channel gamma correction. This value is represented in a 3.16 format with 3 integer and 16 fractional bits.

PAL_EXT2_GC_MAX

PAL_EXT2_GC_MAX	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	96
Address:	4A430h-4A43Bh
Name:	Pipe Extended Second Gamma Correction Max
ShortName:	PAL_EXT2_GC_MAX_A
Power:	PG1
Reset:	soft
Address:	4AC30h-4AC3Bh
Name:	Pipe Extended Second Gamma Correction Max
ShortName:	PAL_EXT2_GC_MAX_B
Power:	PG2
Reset:	soft
Address:	4B430h-4B43Bh
Name:	Pipe Extended Second Gamma Correction Max
ShortName:	PAL_EXT2_GC_MAX_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31:19	**Reserved** Format: MBZ
	18:0	**Red Ext Max GC Point** Default Value: 1111111111111111b Format: U3.16 The extended point for red color channel gamma correction. This value is represented in a 3.16 format with 3 integer and 16 fractional bits.
1	31:19	**Reserved** Format: MBZ
	18:0	**Green Ext Max GC Point**

PAL_EXT2_GC_MAX

		Default Value: 1111111111111111b Format: U3.16 The extended point for green color channel gamma correction. This value is represented in a 3.16 format with 3 integer and 16 fractional bits.
2	31:19	**Reserved** Format: MBZ
	18:0	**Blue Ext Max GC Point** Default Value: 1111111111111111b Format: U3.16 The extended point for blue color channel gamma correction. This value is represented in a 3.16 format with 3 integer and 16 fractional bits.

PAL_GC_MAX

PAL_GC_MAX	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	96
Address:	4A410h-4A41Bh
Name:	Pipe Gamma Correction Max
ShortName:	PAL_GC_MAX_A
Power:	PG1
Reset:	soft
Address:	4AC10h-4AC1Bh
Name:	Pipe Gamma Correction Max
ShortName:	PAL_GC_MAX_B
Power:	PG2
Reset:	soft
Address:	4B410h-4B41Bh
Name:	Pipe Gamma Correction Max
ShortName:	PAL_GC_MAX_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31:17	**Reserved** Format: MBZ
	16:0	**Red Max GC Point** Default Value: 10000000000000000b Format: U1.16 **Description** The 513th entry for the red color channel of the 12 bit interpolated gamma correction. This value is represented in a 1.16 format with 1 integer and 16 fractional bits. **Restriction** The value should always be programmed to be less than or equal to 1.0.
1	31:17	**Reserved** Format: MBZ

PAL_GC_MAX

	16:0	**Green Max GC Point** Default Value: 10000000000000000b Format: U1.16 **Description** The 513th entry for the green color channel of the 12 bit interpolated gamma correction. This value is represented in a 1.16 format with 1 integer and 16 fractional bits. **Restriction** The value should always be programmed to be less than or equal to 1.0.
2	31:17	**Reserved** Format: MBZ
	16:0	**Blue Max GC Point** Default Value: 10000000000000000b Format: U1.16 **Description** The 513th entry for the blue color channel of the 12 bit interpolated gamma correction. This value is represented in a 1.16 format with 1 integer and 16 fractional bits. **Restriction** The value should always be programmed to be less than or equal to 1.0.

PAL_LGC

PAL_LGC	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	4A000h-4A3FFh
Name:	Pipe A Legacy Palette
ShortName:	PAL_LGC_A_*
Power:	PG1
Reset:	soft
Address:	4A800h-4ABFFh
Name:	Pipe B Legacy Palette
ShortName:	PAL_LGC_B_*
Power:	PG2
Reset:	soft
Address:	4B000h-4B3FFh
Name:	Pipe C Legacy Palette
ShortName:	PAL_LGC_C_*
Power:	PG2
Reset:	soft

There are 256 instances of this register format per display pipe.

Restriction
This register must be written only as a full 32 bit dword. Byte or word writes are not supported.

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:16	**Red Legacy Palette Entry** Default Value: UUh Red legacy palette entry value.
	15:8	**Green Legacy Palette Entry**

PAL_LGC		
		Default Value: UUh Green legacy palette entry value.
	7:0	**Blue Legacy Palette Entry** Default Value: UUh Blue legacy palette entry value.

PAL_PREC_DATA

PAL_PREC_DATA	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	4A404h-4A407h
Name:	Pipe Precision Palette Data
ShortName:	PAL_PREC_DATA_A
Power:	PG1
Reset:	soft
Address:	4AC04h-4AC07h
Name:	Pipe Precision Palette Data
ShortName:	PAL_PREC_DATA_B
Power:	PG2
Reset:	soft
Address:	4B404h-4B407h
Name:	Pipe Precision Palette Data
ShortName:	PAL_PREC_DATA_C
Power:	PG2
Reset:	soft

These are the precision palette entries used for the 10 bpc, split, and 12 bpc gamma. The Precision Palette Index Value indicates the precision palette location to be accessed through this register.

Programming Notes

For 10 bpc, program with the color 10 bit palette entry fraction value. For 12 bpc gamma odd indexes, program with the upper 10 bits of the color palette entry fraction value. For 12 bpc gamma even indexes, program the MSbs with the lower 6 bits of the color palette entry fraction value, then program all 0s in the LSbs. For split gamma indexes 0 to 511, program with the first gamma (before CSC) color 10 bit palette entry fraction value. For split gamma indexes 512 to 1023, program with the second gamma (after CSC) color 10 bit palette entry fraction value.

Restriction

This register must be written only as a full 32 bit dword. Byte or word writes are not supported.

DWord	Bit	Description
0	31:30	**Reserved**
	29:20	**Red Precision Palette Entry**

PAL_PREC_DATA		
		Default Value: UUUUUUUUUUb Red precision palette entry value.
	19:10	**Green Precision Palette Entry** Default Value: UUUUUUUUUUb Green precision palette entry value.
	9:0	**Blue Precision Palette Entry** Default Value: UUUUUUUUUUb Blue precision palette entry value.

PAL_PREC_INDEX

PAL_PREC_INDEX

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	4A400h-4A403h
Name:	Pipe Precision Palette Index
ShortName:	PAL_PREC_INDEX_A
Power:	PG1
Reset:	soft
Address:	4AC00h-4AC03h
Name:	Pipe Precision Palette Index
ShortName:	PAL_PREC_INDEX_B
Power:	PG2
Reset:	soft
Address:	4B400h-4B403h
Name:	Pipe Precision Palette Index
ShortName:	PAL_PREC_INDEX_C
Power:	PG2
Reset:	soft

This index controls access to the array of precision palette data values.

DWord	Bit	Description
0	31	**Reserved** Format: MBZ
	30:16	**Reserved** Format: MBZ
	15	**Index Auto Increment** This field enables the index auto increment. Value / Name / Description: 0b / No Increment / Do not automatically increment the index value. 1b / Auto Increment / Increment the index value with each read or write to the data register.
	14:10	**Reserved** Format: MBZ
	9:0	**Index Value**

PAL_PREC_INDEX		
		This field indicates the data location to be accessed through the data register. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set. When automatically incrementing, the current automatically calculated index value can be read here, and the index will roll over to 0 after reaching the end of the allowed range.

Value	Name
[0,1023]	

PAL_PREC_MULTI_SEG_DATA

PAL_PREC_MULTI_SEG_DATA	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	4A40Ch-4A40Fh
Name:	Pipe Precision Multi Segment Palette Data
ShortName:	PAL_PREC_MULTI_SEG_DATA_A
Power:	PG1
Reset:	soft
Address:	4AC0Ch-4AC0Fh
Name:	Pipe Precision Multi Segment Palette Data
ShortName:	PAL_PREC_MULTI_SEG_DATA_B
Power:	PG2
Reset:	soft
Address:	4B40Ch-4B40Fh
Name:	Pipe Precision Multi Segment Palette Data
ShortName:	PAL_PREC_MULTI_SEG_DATA_C
Power:	PG2
Reset:	soft

These are the precision palette entries used for the multi segment gamma. The Precision Palette Index Value indicates the precision palette location to be accessed through this register.

Programming Notes

For 10 bpc, program with the color 10 bit palette entry fraction value. For 12 bpc gamma odd indexes, program with the upper 10 bits of the color palette entry fraction value. For 12 bpc gamma even indexes, program the MSbs with the lower 6 bits of the color palette entry fraction value, then program all 0s in the LSbs.

Restriction

This register must be written only as a full 32 bit dword. Byte or word writes are not supported.

DWord	Bit	Description
0	31:30	**Reserved**
	29:20	**Red Precision Palette Entry**

PAL_PREC_MULTI_SEG_DATA		
		Default Value: UUUUUUUUUUb Red precision palette entry value.
	19:10	**Green Precision Palette Entry** Default Value: UUUUUUUUUUb Green precision palette entry value.
	9:0	**Blue Precision Palette Entry** Default Value: UUUUUUUUUUb Blue precision palette entry value.

PAL_PREC_MULTI_SEG_INDEX

PAL_PREC_MULTI_SEG_INDEX	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	4A408h-4A40Bh
Name:	Pipe Precision Multi Segment Palette Index
ShortName:	PAL_PREC_MULTI_SEG_INDEX_A
Power:	PG1
Reset:	soft
Address:	4AC08h-4AC0Bh
Name:	Pipe Precision Multi Segment Palette Index
ShortName:	PAL_PREC_MULTI_SEG_INDEX_B
Power:	PG2
Reset:	soft
Address:	4B408h-4B40Bh
Name:	Pipe Precision Multi Segment Palette Index
ShortName:	PAL_PREC_MULTI_SEG_INDEX_C
Power:	PG2
Reset:	soft

This index controls access to the array of precision palette data values used in the multi-segment gamma mode.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15	**Index Auto Increment** This field enables the index auto increment. Value 0b: No Increment — Do not automatically increment the index value. Value 1b: Auto Increment — Increment the index value with each read or write to the data register.
	14:5	**Reserved** Format: MBZ

PAL_PREC_MULTI_SEG_INDEX		
	4:0	**Index Value** This field indicates the data location to be accessed through the data register. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set. When automatically incrementing, the current automatically calculated index value can be read here, and the index will roll over to 0 after reaching the end of the allowed range. **Value** / **Name** [0,17] /

Performance Counter 1 LSB

PERFCNT1_LSB - Performance Counter 1 LSB	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	091B8h

GT implements 2 general purpose counters each with 44-bits, each counter can be programmed to count one main event out of set of events (see the event list). Some events are simple duration events and some are edge detects (0=>1 transition is counted). The nature of the event is also programmed to the register that allocates the counter value.

DWord	Bit	Description
0	31:0	**Counter Value (LSB - 31:0 of 43:0)** Access: RO The Counter Value: This is the field where the counter value can be observed via a simple read to the register.

Performance Counter 1 MSB

PERFCNT1_MSB - Performance Counter 1 MSB	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	091BCh

GT implements 2 general purpose counters each with 44-bits, each counter can be programmed to count one main event out of set of events (see the event list). Some events are simple duration events and some are edge detects (0=>1 transition is counted). The nature of the event is also programmed to the register that allocates the counter value.

DWord	Bit	Description
0	31	**Counter 1 Enable** Access: R/W Counter#1 Enable. 0: Counter is disabled. The count value is not deterministic. 1: Counter is enabled. Once enabled, the counter is activated if the global enable (from NCU) is also asserted.
	30	**Overflow Enable** Access: R/W Overflow Enable. 0: Overflow reporting is enabled. 1: Overflow reporting is disabled.
	29	**Edge Detect** Access: R/W Edge Detect: 0: Edge detect is enabled. 1: Edge detect is disabled.
	28	**Counter Clear** Access: R/W Counter Clear.
	27:20	**Event Selection** Access: R/W Event Selection: The event list (see attached). Used as a MUX control to select the event to Counter.

PERFCNT1_MSB - Performance Counter 1 MSB		
	19:12	**RSVD** Access: RO
	11:0	**Counter Value (MSB - 43:32 of 43:0)** Access: RO The Counter Value: This is the field where the counter value can be observed via a simple read to the register.

Performance Counter 2 LSB

PERFCNT2_LSB - Performance Counter 2 LSB	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	091C0h

GT implements 2 general purpose counters each with 44-bits, each counter can be programmed to count one main event out of set of events (see the event list). Some events are simple duration events and some are edge detects (0=>1 transition is counted). The nature of the event is also programmed to the register that allocates the counter value.

DWord	Bit	Description
0	31:0	**Counter Value (LSB - 31:0 of 43:0)** Access: RO The Counter Value: This is the field where the counter value can be observed via a simple read to the register.

Performance Counter 2 MSB

PERFCNT2_MSB - Performance Counter 2 MSB	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	091C4h

GT implements 2 general purpose counters each with 44-bits, each counter can be programmed to count one main event out of set of events (see the event list). Some events are simple duration events and some are edge detects (0=>1 transition is counted). The nature of the event is also programmed to the register that allocates the counter value.

DWord	Bit	Description
0	31	**Counter 2 Enable** Access: R/W Counter#2 Enable. 0: Counter is disabled. The count value is not deterministic. 1: Counter is enabled. Once enabled, the counter is activated if the global enable (from NCU) is also asserted.
	30	**Overflow Enable** Access: R/W Overflow Enable. 0: Overflow reporting is enabled. 1: Overflow reporting is disabled.
	29	**Edge Detect** Access: R/W Edge Detect. 0: Edge detect is enabled. 1: Edge detect is disabled.
	28	**Counter Clear** Access: R/W Counter Clear.
	27:20	**Event Selection** Access: R/W Event Selection: The event list (see attached). Used as a MUX control to select the event to Counter.

PERFCNT2_MSB - Performance Counter 2 MSB		
	19:12	**RSVD** Access: RO
	11:0	**Counter Value (MSB - 43:32 of 43:0)** Access: RO The Counter Value: This is the field where the counter value can be observed via a simple read to the register.

Performance Counter 3 LSB

PERFCNT3_LSB - Performance Counter 3 LSB	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	091C8h

GT implements 4 general purpose counters each with 44-bits, each counter can be programmed to count one main event out of set of events (see the event list). Some events are simple duration events and some are edge detects (0=>1 transition is counted). The nature of the event is also programmed to the register that allocates the counter value.

DWord	Bit	Description
0	31:0	**Counter Value (LSB - 31:0 of 43:0)** Access: RO The Counter Value: This is the field where the counter value can be observed via a simple read to the register.

Performance Counter 3 MSB

PERFCNT3_MSB - Performance Counter 3 MSB	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	091CCh

GT implements 4 general purpose counters each with 44-bits, each counter can be programmed to count one main event out of set of events (see the event list). Some events are simple duration events and some are edge detects (0=>1 transition is counted). The nature of the event is also programmed to the register that allocates the counter value.

DWord	Bit	Description
0	31	**Counter 3 Enable** Access: R/W Counter#3 Enable. 0: Counter is disabled. The count value is not deterministic. 1: Counter is enabled. Once enabled, the counter is activated if the global enable (from NCU) is also asserted.
	30	**Overflow Enable** Access: R/W Overflow Enable. 0: Overflow reporting is enabled. 1: Overflow reporting is disabled.
	29	**Edge Detect** Access: R/W Edge Detect: 0: Edge detect is enabled. 1: Edge detect is disabled.
	28	**Counter Clear** Access: R/W Counter Clear.
	27:20	**Event Selection** Access: R/W Event Selection: The event list (see attached). Used as a MUX control to select the event to Counter.

PERFCNT3_MSB - Performance Counter 3 MSB		
	19:12	**RSVD** Access: RO
	11:0	**Counter Value (MSB - 43:32 of 43:0)** Access: RO The Counter Value: This is the field where the counter value can be observed via a simple read to the register.

Performance Counter 4 LSB

PERFCNT4_LSB - Performance Counter 4 LSB	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	091D8h

GT implements 4 general purpose counters each with 44-bits, each counter can be programmed to count one main event out of set of events (see the event list). Some events are simple duration events and some are edge detects (0=>1 transition is counted). The nature of the event is also programmed to the register that allocates the counter value.

DWord	Bit	Description
0	31:0	**Counter Value (LSB - 31:0 of 43:0)** Access: RO The Counter Value: This is the field where the counter value can be observed via a simple read to the register.

Performance Counter 4 MSB

PERFCNT4_MSB - Performance Counter 4 MSB	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	091DCh

GT implements 4 general purpose counters each with 44-bits, each counter can be programmed to count one main event out of set of events (see the event list). Some events are simple duration events and some are edge detects (0=>1 transition is counted). The nature of the event is also programmed to the register that allocates the counter value.

DWord	Bit	Description
0	31	**Counter 4 Enable** Access: R/W Counter#4 Enable. 0: Counter is disabled. The count value is not deterministic. 1: Counter is enabled. Once enabled, the counter is activated if the global enable (from NCU) is also asserted.
	30	**Overflow Enable** Access: R/W Overflow Enable. 0: Overflow reporting is enabled. 1: Overflow reporting is disabled.
	29	**Edge Detect** Access: R/W Edge Detect: 0: Edge detect is enabled. 1: Edge detect is disabled.
	28	**Counter Clear** Access: R/W Counter Clear.
	27:20	**Event Selection** Access: R/W Event Selection: The event list (see attached). Used as a MUX control to select the event to Counter.

PERFCNT4_MSB - Performance Counter 4 MSB		
	19:12	**RSVD** Access: RO
	11:0	**Counter Value (MSB - 43:32 of 43:0)** Access: RO The Counter Value: This is the field where the counter value can be observed via a simple read to the register.

PHY_MISC

PHY_MISC	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	64C00h-64C03h
Name:	PHY_MISC_A
ShortName:	PHY_MISC_A
Power:	PG0
Reset:	global
Address:	64C04h-64C07h
Name:	PHY_MISC_B
ShortName:	PHY_MISC_B
Power:	PG0
Reset:	global

This register is on the ungated clock and the chip reset, not the FLR.

DWord	Bit	Description
0	31:28	**DE to IO Misc** Default Value: 0010b
	27:24	**IO to DE Misc** Access: RO
	23	**DE to IO Comp Pwr Down**
	22	**Spare 22**
	21	**Spare 21**
	20	**Spare 20**
	19:0	**Reserved** Format: MBZ

PIPE_ARB_CTL

PIPE_ARB_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank OR pipe disabled
Address:	70028h-7002Bh
Name:	Pipe Arbiter Control
ShortName:	PIPE_ARB_CTL_A
Power:	PG1
Reset:	soft
Address:	71028h-7102Bh
Name:	Pipe Arbiter Control
ShortName:	PIPE_ARB_CTL_B
Power:	PG2
Reset:	soft
Address:	72028h-7202Bh
Name:	Pipe Arbiter Control
ShortName:	PIPE_ARB_CTL_C
Power:	PG2
Reset:	soft

There is one instance of this register per pipe.

DWord	Bit	Description
0	31:21	**Reserved** Format: MBZ
	20	**Disable Weighted Arbitration** This field disables the weighted pipe slice arbitration. 0b: Enable **[Default]** 1b: Disable
	19	**Reserved**

PIPE_ARB_CTL

	Format:	MBZ

18:16 Additional Slots

These additional Slots gets added to each arbitration cycle during which the clients gets serviced in a round robin manner.A programmed value of 1b results in 1 additional slot.

15:14 Reserved

Format:	MBZ

13 Use Programmed Slots

When this field is set, HW uses the Slots programmed in the PLANE_CTL register instead of the HW defaults.

12 Disable Block Valid Check

The field disables the block valid check done at pipe arbiter.

Value	Name
0b	Enable
1b	Disable

11:10 Reserved

Format:	MBZ

9:8 Request Vs Data Arbitration

This field selects the arbitration weightage for the Streamer and the DDB requests.

Value	Name	Description
00b		Allow 1 Streamer requests every 2 DDB requests.
01b		Allow 1 Streamer requests every 4 DDB requests.
10b	**[Default]**	Allow 1 Streamer requests every 8 DDB requests.
11b		Allow 1 Streamer requests every 16 DDB requests.

7:6 Reserved

Format:	MBZ

5:0 Frame Start Drain Delay

This field contains the time, in microseconds, the pipe waits before draining the data from the Display Buffer.

Value	Name
[0-31]	
15	**[Default]**

PIPE_BOTTOM_COLOR

PIPE_BOTTOM_COLOR

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank OR pipe disabled

Address:	70034h-70037h
Name:	Pipe Bottom Color
ShortName:	PIPE_BOTTOM_COLOR_A
Power:	PG1
Reset:	soft

Address:	71034h-71037h
Name:	Pipe Bottom Color
ShortName:	PIPE_BOTTOM_COLOR_B
Power:	PG2
Reset:	soft

Address:	72034h-72037h
Name:	Pipe Bottom Color
ShortName:	PIPE_BOTTOM_COLOR_C
Power:	PG2
Reset:	soft

This register sets the color that appears underneath the bottom most plane in the pipe blender Z-order. The value for each color channel is represented in an unsigned 0.10 format with 0 integer and 10 fractional bits.

DWord	Bit	Description
0	31	**Pipe Gamma Enable** This bit enables pipe gamma correction for the bottom color. Value: 0b – Disable; 1b – Enable
	30	**Pipe CSC Enable** This bit enables pipe color space conversion for the bottom color. Value: 0b – Disable; 1b – Enable

PIPE_BOTTOM_COLOR		
	29:20	**V R Bottom Color** Format: U0.10 This field sets the bottom color for the V or Red channel.
	19:10	**Y G Bottom Color** Format: U0.10 This field sets the bottom color for the Y or Green channel.
	9:0	**U B Bottom Color** Format: U0.10 This field sets the bottom color for the U or Blue channel.

PIPE_DSS_CTL1

PIPE_DSS_CTL1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	78200h-78203h
Name:	PIPE DSS Control 1_PB
ShortName:	PIPE_DSS_CTL1_PB
Power:	PG3
Reset:	soft
Address:	78400h-78403h
Name:	PIPE DSS Control 1_PC
ShortName:	PIPE_DSS_CTL1_PC
Power:	PG4
Reset:	soft

Display stream splitter

DWord	Bit	Description
0	31	**Splitter Enable** This field enables stream splitting. Value: 0b — Name: Disable Value: 1b — Name: Enable
	30	**Joiner Enable** This field enables stream joiner after compression. Value: 0b — Name: Disable Value: 1b — Name: Enable
	29	**Big_Joiner_Enable** When big_joiner_enable is '1', this dssunit will be working with another dssunit in adjacent pipe either as a master or as a slave. Value: 0b — Name: Disable

PIPE_DSS_CTL1

	1b	Enable

28 Master_Big_Joiner_Enable

This bit indicates that this pipe is the master/slave when Big_Joiner_Enable bit is set in this register.

Value	Name
0b	Slave
1b	Master

27 Reserved

26 Reserved

25 Reserved

24 Dual Link Mode

This field selects the split pattern. Applicable only if splitter mode is enabled through DSS configuration bits.

Value	Name
0b	Front-Back mode
1b	Interleave mode

23:22 Reserved

21:20 Reserved

Format:	MBZ

19:16 Overlap

MIPI use case (mainly dual link mode):
This field specifies the number of pixels of overlap.
1 to 15 = valid integer number of overlap pixels.
0 = Sink device requires no overlap pixels.
eDP use case:
This field specifies the number of overlap pixels the sink device uses in the active data.
1 to 8 = valid integer number of overlap pixels.
0 = Sink device requires no overlap pixels.

15:12 Reserved

Format:	MBZ

11:0 Left DL buffer Target Depth

This field indicates the number of pixels to hold in the slave link buffer before enabling the timing generator, so the Master and Slave client controllers are in sync.
Valid only when operating in front back dual link mode.
Value should only be programmed for the Slave client controller. If bit 31 is set then the target for the Salve controller must be non-zero.

PIPE_DSS_CTL1		
		Maximum value is 1440 decimal.

PIPE_DSS_CTL2

PIPE_DSS_CTL2	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	78204h-78207h
Name:	PIPE DSS Control 2_PB
ShortName:	PIPE_DSS_CTL2_PB
Power:	PG3
Reset:	soft
Address:	78404h-78407h
Name:	PIPE DSS Control 2_PC
ShortName:	PIPE_DSS_CTL2_PC
Power:	PG4
Reset:	soft

Display stream splitter

DWord	Bit	Description
0	31	**Left Branch VDSC Enable** Description: This bit enables Display Stream Compression on left branch. Its double buffered to rising edge of vblank. Restriction : Display stream compression is supported for pipe active sizes up to 4096 pixels. 0b: Disable 1b: Enable
	30:27	**Reserved** Format: MBZ
	26	**Spare 26**
	25	**Spare 25**
	24	**Spare 24**
	23:16	**Reserved** Format: MBZ

PIPE_DSS_CTL2

	15	**Right Branch VDSC Enable** **Description** Display stream compression on right branch enable/disable. It is double buffered on rising edge of vblank. Restriction : Display stream compression is supported for pipe active sizes up to 4096 pixels. **Value** / **Name** 0b – Disable 1b – Enable
	14	**Spare 14**
	13	**Spare 13**
	12	**Spare 12**
	11:0	**Right DL Buffer Target Depth** This field indicates the number of pixels to hold in the slave link buffer before enabling the timing generator, so the Master and Slave client controllers are in sync. Valid only when operating in front back dual link mode. Value should only be programmed for the Slave controller. If bit 31 is set then the target for the Slave controller must be non-zero. Maximum value is 1440 decimal. Default is 0.

PIPE_FLIPCNT

PIPE_FLIPCNT	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	70044h-70047h
Name:	Pipe Flip Count
ShortName:	PIPE_FLIPCNT_A
Power:	PG1
Reset:	soft
Address:	71044h-71047h
Name:	Pipe Flip Count
ShortName:	PIPE_FLIPCNT_B
Power:	PG2
Reset:	soft
Address:	72044h-72047h
Name:	Pipe Flip Count
ShortName:	PIPE_FLIPCNT_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31:0	**Pipe Flip Counter** **Description** This field provides read back of the display pipe flip counter. The counter increments on the start of each flip to plane 1 of this pipe. The start of flip is when the plane surface address is updated, not when the flip completes. The flip can be through command streamer asynchronous and synchronous flips or MMIO writes to the plane 1 surface address. It rolls over back to 0 after (2^32)-1 flips.

PIPE_FLIPTMSTMP

PIPE_FLIPTMSTMP	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	7004Ch-7004Fh
Name:	Pipe Flip Time Stamp
ShortName:	PIPE_FLIPTMSTMP_A
Power:	PG1
Reset:	soft
Address:	7104Ch-7104Fh
Name:	Pipe Flip Time Stamp
ShortName:	PIPE_FLIPTMSTMP_B
Power:	PG2
Reset:	soft
Address:	7204Ch-7204Fh
Name:	Pipe Flip Time Stamp
ShortName:	PIPE_FLIPTMSTMP_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31:0	**Pipe Flip Time Stamp** **Description** This field provides read back of the display pipe flip time stamp. The time stamp value is sampled on the start of each flip to plane 1 of this pipe. The start of flip is when the plane surface address is updated, not when the flip completes. The flip can be through command streamer asynchronous and synchronous flips or MMIO writes to the plane 1 surface address. The TIMESTAMP_CTR register has the current time stamp value. Writes to this register do not update the value.

PIPE_FRMCNT

PIPE_FRMCNT	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	70040h-70043h
Name:	Pipe Frame Count
ShortName:	PIPE_FRMCNT_A
Power:	PG1
Reset:	soft
Address:	71040h-71043h
Name:	Pipe Frame Count
ShortName:	PIPE_FRMCNT_B
Power:	PG2
Reset:	soft
Address:	72040h-72043h
Name:	Pipe Frame Count
ShortName:	PIPE_FRMCNT_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31:0	**Pipe Frame Counter** Provides read back of the display pipe frame counter. This counter increments on every start of vertical blank and rolls over back to 0 after (2^32)-1 frames.

PIPE_FRMTMSTMP

PIPE_FRMTMSTMP	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	70048h-7004Bh
Name:	Pipe Frame Time Stamp
ShortName:	PIPE_FRMTMSTMP_A
Power:	PG1
Reset:	soft
Address:	71048h-7104Bh
Name:	Pipe Frame Time Stamp
ShortName:	PIPE_FRMTMSTMP_B
Power:	PG2
Reset:	soft
Address:	72048h-7204Bh
Name:	Pipe Frame Time Stamp
ShortName:	PIPE_FRMTMSTMP_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31:0	**Pipe Frame Time Stamp** **Description** This field provides read back of the display pipe frame time stamp. The time stamp value is sampled at every start of vertical blank. The TIMESTAMP_CTR register has the current time stamp value. Writes to this register do not update the value.

PIPE_MISC

PIPE_MISC	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank OR pipe disabled
Address:	70030h-70033h
Name:	Pipe Miscellaneous
ShortName:	PIPE_MISC_A
Power:	PG1
Reset:	soft
Address:	71030h-71033h
Name:	Pipe Miscellaneous
ShortName:	PIPE_MISC_B
Power:	PG2
Reset:	soft
Address:	72030h-72033h
Name:	Pipe Miscellaneous
ShortName:	PIPE_MISC_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31:30	**Stereo Mask Pipe Int** This field controls which pipe vertical timing (vertical blank, scan line, and vertical sync) events will be reported in interrupts during stereo 3D mode.

Value	Name	Description
00b	Mask None	No masking. Report both the left and right eye vertical events.
01b	Mask Left	Mask the left eye vertical events. Only report right eye events.
10b	Mask Right	Mask the right eye vertical events. Only report left eye events.
11b	Reserved	Reserved

Restriction

		This field must be programmed prior to enabling stereo 3D mode and must not be changed while stereo 3D is enabled. In the stacked frame mode the vertical sync is not generated in the gap between left and right eye images, and the scan line count increments across the entire tall frame, so masking may cause unexpected behavior for those events.
	29:28	**Stereo Mask Pipe Render** This field controls which pipe vertical timing (vertical blank, scan line, and vertical sync) events will be reported in render responses during stereo 3D mode. **Value** / **Name** / **Description** 00b / Mask None / No masking. Report both the left and right eye vertical events. 01b / Mask Left / Mask the left eye vertical events. Only report right eye events. 10b / Mask Right / Mask the right eye vertical events. Only report left eye events. 11b / Reserved / Reserved **Restriction** This field must be programmed prior to enabling stereo 3D mode and must not be changed while stereo 3D is enabled. In the stacked frame mode the vertical sync is not generated in the gap between left and right eye images, and the scan line count increments across the entire tall frame, so masking may cause unexpected behavior for those events.
	27	**YUV420 Enable** **Description** This field enables YUV420 output from this pipe. This is only for use with HDMI and DP. **Value** / **Name** 0b / Disable 1b / Enable **Restriction** This field must be programmed prior to enabling the transcoder attached to this pipe.
	26	**YUV420 Mode** This field specifies the mode in which YUV420 pixels are generated by this pipe. **Value** / **Name** 0b / Bypass 1b / Full blend
	25:24	**Reserved**

PIPE_MISC

23	**HDR Mode**

Description
This field enables the HDR mode, allowing for higher precision output from the HDR supporting planes and bypassing the SDR planes in blending.
In addition to setting bit 15 of register offset 0x70038 (pipe A), 0x71038 (pipe B), 0x72038 (pipe C), or 0x73038 (pipe D), this bit must be set to 1b to passthrough the frame buffer pixels unmodified across the pipe.

Value	Name
0b	Disable
1b	Enable

22	**Change Mask for LDPST**

This field controls the change tracking for the LACE. Change tracking can be used by PSR/SRD and WD

Value	Name
0b	Not Masked
1b	Masked

21	**Change Mask for Register Write**

This field controls change tracking for the pipe register write. Change tracking can be used by PSR/SRD and WD.

Value	Name
0b	Not Masked
1b	Masked

20	**Change Mask for Vblank Vsync Int**

This field controls change tracking for the vblank or vsync interrupt enable. Change tracking can be used by PSR/SRD and WD.

Value	Name
0b	Not Masked
1b	Masked

19	**Reserved**
18	**Reserved**
17	**Reserved**
16	**Reserved**

PIPE_MISC

15:14 **Rotation Info**

This field indicates to internal KVMR screen capture that the display has been rotated through software or hardware rotation. Select the closest value if the rotation is not an exact multiple of 90 degrees. Hardware rotation of the display output is controlled through the plane control registers, not through this field.

Value	Name	Description
00b	None	No rotation on this pipe
01b	90	90 degree rotation on this pipe
10b	180	180 degree rotation on this pipe
11b	270	270 degree rotation on this pipe

Restriction
This field must be programmed in order for internal KVMR screen capture to work correctly when display is rotated by software or hardware.

13 **Reserved**

Format:	MBZ

12 **OLED Compensation**

Description
This field enables the OLED compensation on the pipe. When this bit is set, plane 5 is used as the OLED compensation plane with up to 10 bits per channel precision. OLED compensation must be used only when the pipe is configured to output RGB format.
The OLED compensation plane size must be same as the pipe active size.

Value	Name
0b	Disable
1b	Enable

11 **Pipe output color space select**

This field indicates the output color space. This field affects the values of the pipe border and some capture functions. This field does not affect the planes, pipe CSC, or ports.

Value	Name
0b	RGB
1b	YUV

Restriction
This field must be set to match the color space that will be output from the pipe CSC or output from the planes if they pipe CSC is bypassed.

PIPE_MISC

10 — xvYCC Color Range Limit

This field limits the color range of the pipe output to 1 to 254 for 8-bit components, 4 to 1019 for 10bit components, and 16 to 4079 for 12-bit components. Values outside of the range will be clamped to fit within the range.

Value	Name	Description
0b	Full	Do not limit the range
1b	Limit	Limit range

9:8 — Reserved

Format:	MBZ

7:5 — Dithering BPC

This field selects the number of bits per color to be used in dithering.

Value	Name	Description
000b	8 bpc	8 bits per color
001b	10 bpc	10 bits per color
010b	6 bpc	6 bits per color
Others	Reserved	Reserved

Programming Notes
When dithering is enabled, the value selected here should match the bits per color selected in the Transcoder DDI Function Control register attached to this pipe.

4 — Dithering enable

This field enables dithering.

Value	Name
0b	Disable
1b	Enable

3:2 — Dithering type

This field selects the dithering type.

Value	Name	Description
00b	Spatial	Spatial
01b	ST1	Spatio-Temporal 1
10b	ST2	Spatio-Temporal 2
11b	Temporal	Temporal

1 — Reserved

Format:	MBZ

0 — Reserved

PIPE_MISC2

PIPE_MISC2	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank OR pipe disabled
Address:	7002Ch-7002Fh
Name:	Pipe Miscellaneous 2
ShortName:	PIPE_MISC2_A
Power:	PG1
Reset:	soft
Address:	7102Ch-7102Fh
Name:	Pipe Miscellaneous 2
ShortName:	PIPE_MISC2_B
Power:	PG2
Reset:	soft
Address:	7202Ch-7202Fh
Name:	Pipe Miscellaneous 2
ShortName:	PIPE_MISC2_C
Power:	PG2
Reset:	soft

There is one instance of this register per pipe.

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:20	**TLB Throttle** Default Value: 8 This field specifies how often the TLB requests are sent. If the programmed value is x, TLBs requests are sent once in x clocks if there are competing data requests.

PIPE_MISC2

	19:16	**Reserved** Format: MBZ
	15:12	**IPC Demote Req Chunk Size** Default Value: 8 This field specifies the request chunk size during IPC Demote. This field is 0 based.
	11:9	**Reserved** Format: MBZ
	8	**ASFU Flip exception** Value / Name / Description: 1b / mask / Add exception for Flip for global register update event and Pipe register update event. 0b / No mask / Do not add exception for Flip for global register update event and Pipe register update event.
	7:3	**Reserved** Format: MBZ
	2:0	**Reserved** Format: MBZ

PIPE_SCANLINE

PIPE_SCANLINE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	70000h-70003h
Name:	Pipe Scan Line
ShortName:	PIPE_SCANLINE_A
Power:	PG1
Reset:	soft
Address:	71000h-71003h
Name:	Pipe Scan Line
ShortName:	PIPE_SCANLINE_B
Power:	PG2
Reset:	soft
Address:	72000h-72003h
Name:	Pipe Scan Line
ShortName:	PIPE_SCANLINE_C
Power:	PG2
Reset:	soft

This register enables the read back of the pipe vertical line counter. The value increments at the leading edge of HSYNC. The value resets to line zero at the first active line of the display. In interlaced display timings, the scan line counter provides the current line in the field. One field can have a total number of lines that is one greater than the other field.

DWord	Bit	Description
0	31	**Current Field** This is an indication of the current display field. Value / Name / Description: 0b / Odd / First field (odd field) 1b / Even / Second field (even field)
	30:20	**Reserved**
	19:13	**Reserved**
	12:0	**Line Counter for Display**

PIPE_SCANLINE		
		This is an indication of the current display scan line. **Programming Notes** The line count value is from the display output timing generator, representing the scan line currently being output to a receiver. Due to buffering within the display engine, the line being fetched (read) from the frame buffer is not directly linked to the line being output. It is possible for the fetched line to be hundreds of lines ahead of the timing generator output line.

PIPE_SCANLINECOMP

PIPE_SCANLINECOMP	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	70004h-70007h
Name:	Pipe Scan Line Compare
ShortName:	PIPE_SCANLINECOMP_A
Power:	PG1
Reset:	soft
Address:	71004h-71007h
Name:	Pipe Scan Line Compare
ShortName:	PIPE_SCANLINECOMP_B
Power:	PG2
Reset:	soft
Address:	72004h-72007h
Name:	Pipe Scan Line Compare
ShortName:	PIPE_SCANLINECOMP_C
Power:	PG2
Reset:	soft

This register is used to initiate a display scan line compare. This MMIO driven scan line compare can not be used at the same time as the command streamer driven scan line compare on the same pipe. When this register is written with the Initiate Compare bit set to 1b, the Display Engine (DE) will start comparing the display pipe or plane (selectable) current scan line value (current scan line) with the start scan line value (current scan line >= start scan line) and the end scan line value (current scan line <= end scan line) to decide if the pipe scan line is inside or outside the scan line window of interest. DE will wait until the current scan line is either outside (Inclusive mode) or inside (Exclusive mode) the scan line window, then trigger a scan line event and stop any further comparing. The scan line event can cause display to send a scan line compare response to the command streamer, (used for releasing a MI_WAIT_FOR_EVENT on scan line window), if unmasked in the DERRMR mask register 0x44050. The scan line event can also cause display to generate a scan line compare interrupt, if the interrupt registers are configured for that. The value programmed should be the desired value - 1, so for scan line 0, the value programmed is vertical total, and for scan line 1, the value programmed is 0. The programmable range can include the vertical blank. In interlaced display timings, the current scan line is the current line of the current interlaced field. Either MMIO or a MI_LOAD_REGISTER_IMM command can be used to unmask the scan line render response 0x44050. That can be done anytime before programming this register. There is one instance of this register per pipe.

PIPE_SCANLINECOMP

Restriction
A new scan line compare must not be started until after the previous compare has finished. The end scan line value must be greater than or equal to the start scan line value. When using LRI care must be taken to follow all the programming rules for LRI targetting the display engine.

DWord	Bit	Description
0	31	**Initiate Compare** This field initiates the scan line compare. When this register is written with this bit set to 1b, the display engine will do one complete comparison cycle, trigger a scan line event, then stop comparing. **Value** / **Name** 0b – Do nothing 1b – Initiate compare **Restriction** Do not write this register again until after any previous scan line compare has completed.
	30	**Inclusive Exclusive Select** This field selects whether the scan line compare is done in inclusive mode, where display triggers the scan line event when outside the scan line window, or inclusive mode, where display triggers when inside the window. **Value** / **Name** / **Description** 0b / Exclusive / Exclusive mode: trigger scan line event when inside the scan line window 1b / Inclusive / Inclusive mode: trigger scan line event when outside the scan line window
	29	**Counter Select** This field selects whether the scan line compare is done using the pipe timing generator scanline counter or a plane scanline counter. The pipe timing generator counts the scanlines being output from display. The plane counts the scan lines being fetched from the frame buffer. **Value** / **Name** / **Description** 0b / Timing generator / Use the scanline count from the pipe timing generator 1b / Plane 1 / Use the scanline count from plane 1 **Programming Notes** Due to buffering within the display engine, the line being fetched from the frame buffer is not directly linked to the line being output. It is possible for the fetched line to be hundreds of lines ahead of the timing generator output line. The plane scan line count more closely represents what data is currently being fetched by the plane.
	28:16	**Start Scan Line** This field specifies the starting scan line number of the scan line window.
	15	**Render Response Destination** This bit indicates what destination to send the scan line event render response to.

PIPE_SCANLINECOMP

	15	**Value** / **Name** / **Description** 0b / CS / Send scan line event response to CS 1b / BCS / Send scan line event response to BCS
	14:13	**Reserved**
	12:0	**End Scan Line** This field specifies the ending scan line number of the scan line window.

PIPE_SEAM_EXCESS

PIPE_SEAM_EXCESS - PIPE_SEAM_EXCESS	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank OR pipe disabled
Address:	60020h-60023h
Name:	Pipe Seam Excess
ShortName:	PIPE_SEAM_EXCESS_A
Power:	PG1
Reset:	soft
Address:	61020h-61023h
Name:	Pipe Seam Excess
ShortName:	PIPE_SEAM_EXCESS_B
Power:	PG2
Reset:	soft
Address:	62020h-62023h
Name:	Pipe Seam Excess
ShortName:	PIPE_SEAM_EXCESS_C
Power:	PG2
Reset:	soft

This register defines the number of excess pixels within the Pipe window (on the right or left) that the Scaler will need to remove from the post scaled image.
When an image is split across two Pipes, scaled, and then joined at the Port, the Scalers within each Pipe will operate on a splitimage that contains overlap pixels around where the final seam will be to facilitate a seamless join at the Port. For example, if the left portion of an image is being scaled in Pipe A and the right portion of the image is being scaled in Pipe B, then there will be an excess number of pixels (i.e. overlap pixels) on the right side of the Pipe A image and an excess number of pixels on the left side of the Pipe B image. The overlap pixels of the window within each of the Pipes need to be dropped by the Scaler before they are delivered to the Port.
Notes:

PIPE_SEAM_EXCESS - PIPE_SEAM_EXCESS

1. Dropping of the overlap/excess pixels is done at the very end of the Pipe within the Scaler regardless of whether a Scaler is bound to the Pipe, or not.
2. The values programmed within this register are one-based (i.e. a programming of 1 equals 1 pixel of excess)
3. The values programmed within this register will be added to the Horizontal Active programming of the TRANS_HTOTAL register of the port bound to this pipe. I.e. the pipe will see a Horizontal size equal toHorizontal Active + Left Excess Amount + Right Excess Amount

Restriction :

1. The number of excess pixels cannot exceed the size of the horizontal blank, otherwise there will not be enough time to throw them away before starting the next line and the image will be corrupted
2. Pillarbox boarders must be even
3. The source size on each pipe, including pre-scale excess, must be a multiple of 2. When the Pipe output format is YUV 420 with full blend, the source size is required to be a multiple of 4.

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28:16	**Right Excess Amount** Access: R/W This field defines the number of excess pixels to drop, if any, on the right side of the Pipe window
	15:13	**Reserved**
	12:0	**Left Excess Amount** Access: R/W This field defines the number of excess pixels to drop, if any, on the left side of the Pipe window

PIPE_SRCSZ

PIPE_SRCSZ	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank
Address:	6001Ch-6001Fh
Name:	Pipe Source Image Size
ShortName:	PIPE_SRCSZ_A
Power:	PG1
Reset:	soft
Address:	6101Ch-6101Fh
Name:	Pipe Source Image Size
ShortName:	PIPE_SRCSZ_B
Power:	PG2
Reset:	soft
Address:	6201Ch-6201Fh
Name:	Pipe Source Image Size
ShortName:	PIPE_SRCSZ_C
Power:	PG2
Reset:	soft

There is one instance of this register for each pipe.

Programming Notes

In VGA display mode, this register is ignored and the VGA size from the VGA registers is used instead.

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28:16	**Horizontal Source Size** This field specifies Horizontal Source Size. This determines the horizontal size of the image created by the display planes. This field is programmed to the number of pixels desired minus one. **Restriction** This register must always be programmed to the same value as the Horizontal Active, except

PIPE_SRCSZ		
		when panel fitting is enabled. Refer to PS_CTRL for size restrictions when panel fitting is enabled. Horizintal source size must always be even. The programmed value must be odd.
	15:13	**Reserved** Format: MBZ
	12:0	**Vertical Source Size** This field specifies Vertical Source Size. This determines the vertical size of the image created by the display planes. This field is programmed to the number of lines desired minus one. **Restriction** Vertical source sizes larger than 4320 lines are not supported. This register must always be programmed to the same value as the Vertical Active, except when panel fitting is enabled. Refer to PS_CTRL for size restrictions when panel fitting is enabled.

PIPE_STATUS

PIPE_STATUS	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/WC
Size (in bits):	32
Address:	70058h-7005Bh
Name:	Pipe Status
ShortName:	PIPE_STATUS_A
Power:	PG1
Reset:	soft
Address:	71058h-7105Bh
Name:	Pipe Status
ShortName:	PIPE_STATUS_B
Power:	PG2
Reset:	soft
Address:	72058h-7205Bh
Name:	Pipe Status
ShortName:	PIPE_STATUS_C
Power:	PG2
Reset:	soft

There is one instance of this register per pipe.

DWord	Bit	Description
0	31	**Underrun** Access: R/WC This field indicates that there is an underrun on the transcoder attached to this pipe.
	30	**Vblank** Access: R/WC The field is set at the start of the vertical blank of the transcoder attached to this pipe.
	29	**Frame start**

PIPE_STATUS

	Access:	R/WC
	The field is set at the frame start of the transcoder attached to this pipe.	
28	**Not Used**	
27	**Not Used**	
26	**Not Used**	
	Access:	R/WC
25	**Not Used**	
	Access:	R/WC
24	**Not Used**	
	Access:	R/WC
23	**Not Used**	
	Access:	R/WC
22	**Not Used**	
	Access:	R/WC
21	**Not Used**	
	Access:	R/WC
20	**Not Used**	
	Access:	R/WC
19	**Not Used**	
	Access:	R/WC
18	**Not Used**	
	Access:	R/WC
17	**Not Used**	
	Access:	R/WC
16	**Not Used**	
	Access:	R/WC
15	**Not Used**	
	Access:	R/WC
14	**Not Used**	
	Access:	R/WC
13	**Not Used**	
	Access:	R/WC

PIPE_STATUS

	12	**Not Used** Access: R/WC
	11	**Not Used** Access: R/WC
	10	**Not Used** Access: R/WC
	9	**Not Used** Access: R/WC
	8	**Not Used** Access: R/WC
	7	**Not Used** Access: R/WC
	6	**Not Used** Access: R/WC
	5	**B Credits Pending At VBlank** Access: R/WC A '1' indicates that the there are some pending MBUS B-Credits at the start of VBlank. Sticky bit cleared by a write of '1'
	4	**A Credits Pending At VBlank** Access: R/WC A '1' indicates that the there are some pending MBUS A-Credits at the start of VBlank. Sticky bit cleared by a write of '1'
	3	**Not Used** Access: R/WC
	2	**Not used** Access: R/WC
	1	**Valid Block At FrameStart** Access: R/WC A '1' indicates that a valid block is still present in Display Buffer at frame start. Sticky bit cleared by a write of '1'.
	0	**Valid Block Overwritten** Access: R/WC A '1' indicates that a valid block in Display Buffer was overwritten. Sticky bit cleared by a write of

PIPE_STATUS		
		'1'.

PLANE_AUX_DIST

PLANE_AUX_DIST	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed
Double Buffer Armed By:	Write to PLANE_SURF or plane not enabled
Address:	704C0h-704C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_4_A
Power:	PG1
Reset:	soft
Address:	705C0h-705C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_5_A
Power:	PG1
Reset:	soft
Address:	706C0h-706C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_6_A
Power:	PG1
Reset:	soft
Address:	707C0h-707C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_7_A
Power:	PG1
Reset:	soft
Address:	714C0h-714C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_4_B
Power:	PG2
Reset:	soft

PLANE_AUX_DIST	
Address:	715C0h-715C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_5_B
Power:	PG2
Reset:	soft
Address:	716C0h-716C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_6_B
Power:	PG2
Reset:	soft
Address:	717C0h-717C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_7_B
Power:	PG2
Reset:	soft
Address:	724C0h-724C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_4_C
Power:	PG2
Reset:	soft
Address:	725C0h-725C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_5_C
Power:	PG2
Reset:	soft
Address:	726C0h-726C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_6_C
Power:	PG2
Reset:	soft
Address:	727C0h-727C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_7_C
Power:	PG2
Reset:	soft

PLANE_AUX_DIST	
Address:	701C0h-701C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_1_A
Power:	PG1
Reset:	soft
Address:	702C0h-702C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_2_A
Power:	PG1
Reset:	soft
Address:	703C0h-703C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_3_A
Power:	PG1
Reset:	soft
Address:	711C0h-711C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_1_B
Power:	PG2
Reset:	soft
Address:	712C0h-712C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_2_B
Power:	PG2
Reset:	soft
Address:	713C0h-713C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_3_B
Power:	PG2
Reset:	soft
Address:	721C0h-721C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_1_C
Power:	PG2
Reset:	soft

PLANE_AUX_DIST

Address:	722C0h-722C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_2_C
Power:	PG2
Reset:	soft

Address:	723C0h-723C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_3_C
Power:	PG2
Reset:	soft

This register is used to specify the distance from the main surface base address and the stride of the auxiliary surface. Unlike the surface base address, this register value cannot be updated through flips.

DWord	Bit	Description
0	31:12	**Auxiliary Surface Distance** **Description** When using a compressed surface, this field represents the distance of the control surface in 4K pages, where a value of [31:12] = 1 represents one 4K page. **Restriction** It must be 4K page aligned. Allocate an extra 136 Page Table Entries (PTEs) beyond the end of the displayed surface. If 180 or 270 plane rotation capability is required, allocate an extra 136 PTEs before the beginning of the surface. When address range limits are reached, wrap around to finish allocating the extra PTEs. Only the PTEs will be used, not the pages themselves. The end of the surface cannot be within 136 PTEs of the end of the graphics memory.
	11:10	**Reserved**
	9:0	**Auxiliary Surface Stride** **Description** When using compressed surface this field represents the stride of the control surface. Refer to PLANE_STRIDE register for stride programming details. Restriction : When using render compressed surfaces, the programmed auxiliary surface stride should not exceed 8 (8 * 128 = 1024 bytes).

PLANE_BUF_CFG

PLANE_BUF_CFG	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank, plane not enabled, or pipe not enabled
Double Buffer Armed By:	Write to PLANE_SURF or plane not enabled
Address:	7017Ch-7017Fh
Name:	Cursor Buffer Config
ShortName:	CUR_BUF_CFG_A
Power:	PG1
Reset:	soft
Address:	7117Ch-7117Fh
Name:	Cursor Buffer Config
ShortName:	CUR_BUF_CFG_B
Power:	PG2
Reset:	soft
Address:	7217Ch-7217Fh
Name:	Cursor Buffer Config
ShortName:	CUR_BUF_CFG_C
Power:	PG2
Reset:	soft
Address:	7057Ch-7057Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_4_A
Power:	PG1
Reset:	soft
Address:	7067Ch-7067Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_5_A
Power:	PG1
Reset:	soft

PLANE_BUF_CFG	
Address:	7077Ch-7077Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_6_A
Power:	PG1
Reset:	soft
Address:	7087Ch-7087Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_7_A
Power:	PG1
Reset:	soft
Address:	7157Ch-7157Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_4_B
Power:	PG2
Reset:	soft
Address:	7167Ch-7167Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_5_B
Power:	PG2
Reset:	soft
Address:	7177Ch-7177Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_6_B
Power:	PG2
Reset:	soft
Address:	7187Ch-7187Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_7_B
Power:	PG2
Reset:	soft
Address:	7257Ch-7257Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_4_C
Power:	PG2
Reset:	soft

PLANE_BUF_CFG	
Address:	7267Ch-7267Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_5_C
Power:	PG2
Reset:	soft
Address:	7277Ch-7277Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_6_C
Power:	PG2
Reset:	soft
Address:	7287Ch-7287Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_7_C
Power:	PG2
Reset:	soft
Address:	7027Ch-7027Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_1_A
Power:	PG1
Reset:	soft
Address:	7037Ch-7037Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_2_A
Power:	PG1
Reset:	soft
Address:	7047Ch-7047Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_3_A
Power:	PG1
Reset:	soft
Address:	7127Ch-7127Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_1_B
Power:	PG2
Reset:	soft

PLANE_BUF_CFG

Address:	7137Ch-7137Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_2_B
Power:	PG2
Reset:	soft

Address:	7147Ch-7147Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_3_B
Power:	PG2
Reset:	soft

Address:	7227Ch-7227Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_1_C
Power:	PG2
Reset:	soft

Address:	7237Ch-7237Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_2_C
Power:	PG2
Reset:	soft

Address:	7247Ch-7247Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_3_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31:27	**Reserved**
	26:16	**Buffer End** Default Value: 000h This field contains the buffer end position for this plane.
	15:11	**Reserved**
	10:0	**Buffer Start**

PLANE_BUF_CFG			
		Default Value:	000h
		This field contains the buffer start position for this plane.	

PLANE_COLOR_CTL

PLANE_COLOR_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed
Double Buffer Armed By:	Write to PLANE_SURF or plane not enabled
Address:	704CCh-704CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_4_A
Power:	PG1
Reset:	soft
Address:	705CCh-705CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_5_A
Power:	PG1
Reset:	soft
Address:	706CCh-706CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_6_A
Power:	PG1
Reset:	soft
Address:	707CCh-707CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_7_A
Power:	PG1
Reset:	soft
Address:	714CCh-714CFh

PLANE_COLOR_CTL	
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_4_B
Power:	PG1
Reset:	soft
Address:	715CCh-715CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_5_B
Power:	PG1
Reset:	soft
Address:	716CCh-716CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_6_B
Power:	PG1
Reset:	soft
Address:	717CCh-717CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_7_B
Power:	PG1
Reset:	soft
Address:	724CCh-724CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_4_C
Power:	PG1
Reset:	soft
Address:	725CCh-725CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_5_C
Power:	PG1
Reset:	soft
Address:	726CCh-726CFh

PLANE_COLOR_CTL	
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_6_C
Power:	PG1
Reset:	soft
Address:	727CCh-727CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_7_C
Power:	PG1
Reset:	soft
Address:	701CCh-701CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_1_A
Power:	PG1
Reset:	soft
Address:	702CCh-702CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_2_A
Power:	PG1
Reset:	soft
Address:	703CCh-703CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_3_A
Power:	PG1
Reset:	soft
Address:	711CCh-711CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_1_B
Power:	PG1
Reset:	soft
Address:	712CCh-712CFh

PLANE_COLOR_CTL

Name: Plane Color Control
ShortName: PLANE_COLOR_CTL_2_B

Power: PG1
Reset: soft

Address: 713CCh-713CFh
Name: Plane Color Control
ShortName: PLANE_COLOR_CTL_3_B

Power: PG1
Reset: soft

Address: 721CCh-721CFh
Name: Plane Color Control
ShortName: PLANE_COLOR_CTL_1_C

Power: PG1
Reset: soft

Address: 722CCh-722CFh
Name: Plane Color Control
ShortName: PLANE_COLOR_CTL_2_C

Power: PG1
Reset: soft

Address: 723CCh-723CFh
Name: Plane Color Control
ShortName: PLANE_COLOR_CTL_3_C

Power: PG1
Reset: soft

DWord	Bit	Description
0	31	**Reserved** Format: MBZ
	30	**Pipe Gamma Enable** Description This bit enables pipe gamma correction for the plane pixel data. This field is deprecated.

Use 'GAMMA_MODE.Post CSC Gamma Enable' for enabling pipe gamma across all pixels from all planes.

Value	Name
0b	Disable
1b	Enable

29 **Remove YUV Offset**

This field controls whether the plane removes or preserves the 1/2 offset on U and V components when the source pixel format is YUV and the plane YUV to RGB CSC is disabled. This bit has no effect on RGB source pixel formats

Value	Name	Description
0b	Remove	Remove 1/2 offset on UV components
1b	Preserve	Preserve 1/2 offset on UV components

28 **YUV Range Correction Disable**

Setting this bit disables the YUV range correction logic inside the plane. The range correction logic is used to expand the compressed range YUV to full range YUV. The Y channel is expanded from the 8 bit +16 to +235 range to full range. The U and V channels are expanded from the 8 bit -112 to +112 range to full range. Extended range values will be preserved after the expansion. This bit has no effect on RGB source pixel formats since they automatically bypass range correction.

Value	Name
0b	Enable
1b	Disable

27:24 **Reserved**

Format:	MBZ

23 **Pipe CSC Enable**

Description
This bit enables pipe color space conversion and the pipe pre color space conversion gamma for the plane pixel data. This is separate from the color conversion logic within the plane.
This field is deprecated. Use 'CSC_MODE.Pipe CSC Enable', 'GAMMA_MODE.Pre CSC Gamma Enable' for enabling pipe color space conversion and gamma respectively across all pixels from all planes. Plane CSC must be used for plane specific color space conversion.

Value	Name
0b	Disable
1b	Enable

22 **Reserved**

PLANE_COLOR_CTL

21 Plane CSC Enable

This field enables the plane color space conversion. This field applies only to planes 1 through 3.

Value	Name
0b	Disable
1b	Enable

20 Plane Input CSC Enable

This field enables the plane input color space conversion.This field applies only to planes 1 through 3.

Value	Name
0b	Disable
1b	Enable

19:17 Plane CSC Mode

Description
This field specifies the mode of plane color space conversion operation.
This is used only for planes 4 through 7. For planes 1 through 3, CSC is programmed in PLANE_CSC_* registers.

Value	Name	Description
000b	Bypass	Pixel data bypasses the plane color space conversion
001b	YUV601 to RGB601	YUV BT.601 to RGB BT.601 conversion.
010b	YUV709 to RGB709	YUV BT.709 to RGB BT.709 conversion.
011b	YUV2020 to RGB2020	YUV BT.2020 to RGB BT.2020 conversion.
100b	RGB709 to RGB2020	RGB BT.709 to RGB BT.2020 conversion.

16 Reserved

Format:	MBZ

15 Reserved

Format:	MBZ

14 Plane Pre CSC Gamma Enable

This bit controls plane internal pre-CSC gamma correction.

Value	Name
1b	Enable
0b	Disable

13 Plane Gamma Disable

This bit controls plane internal post-CSC gamma correction.

Value	Name
1b	Disable
0b	Enable

12 **Plane Gamma Mode**

This field specifies the plane gamma mode of operation. This field is ignored if plane gamma is disabled.

Value	Name	Description
0b	Direct **[Default]**	Direct mode is used for regular plane gamma programming. Lookup is based on incoming pixel individual r, g, b values. The output is a computed by lookup of two nearest points and interpolation.
1b	Multiply	Multiple mode is used when plane gamma is used for HDR tone mapping. Lookup is based on a pseudo luminance of the incoming pixel calculated using Lin = 0.25*Red input + 0.625*Green input + 0.125*Blue input. An adjustment factor 'F' is computed by lookup of two nearest points and interpolation. Output is computed by multiplying each color channel with the adjustment factor F.

11:6 **Reserved**

Format:	MBZ

5:4 **Alpha Mode**

Description
This field controls how the plane will use per pixel alpha data from frame buffer. Constant plane alpha is defined in PLANE_KEYMSK and PLANE_KEYMAX registers.
RGB 64-bit - only alpha in 0-1 range supported with 8 bit granularity. RGB 64-bit UINT - only 8 upper bits of alpha used. RGB 2:10:10:10 - 2 bit alpha expanded out to 8 bit to give full range of opacity. XR_BIAS 10:10:10 - 2 bit alpha expanded out to 8 bit to give full range of opacity.

Value	Name	Description
00b	Disable	Alpha channel ignored.
10b	Enable with SW pre-multiply	Alpha channel used. Color channels should be pre-multiplied with alpha by software.
11b	Enable with HW pre-multiply	Alpha channel used. Color channels will be pre-multiplied with alpha by hardware.

Restriction

PLANE_COLOR_CTL			
		Per pixel alpha is supported only with RGB pixel formats. FBC is not compatible with per pixel alpha.	
	3:0	**Reserved**	
		Format:	MBZ

PLANE_CSC_COEFF

PLANE_CSC_COEFF	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	192
Double Buffer Update Point:	Start of vertical blank after armed
Double Buffer Armed By:	Write to PLANE_SURF
Address:	70210h-70227h
Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_1_A
Power:	PG1
Reset:	soft
Address:	70310h-70327h
Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_2_A
Power:	PG1
Reset:	soft
Address:	70410h-70427h
Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_3_A
Power:	PG1
Reset:	soft
Address:	71210h-71227h
Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_1_B
Power:	PG2
Reset:	soft
Address:	71310h-71327h

PLANE_CSC_COEFF

Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_2_B
Power:	PG2
Reset:	soft

Address:	71410h-71427h
Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_3_B
Power:	PG2
Reset:	soft

Address:	72210h-72227h
Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_1_C
Power:	PG2
Reset:	soft

Address:	72310h-72327h
Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_2_C
Power:	PG2
Reset:	soft

Address:	72410h-72427h
Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_3_C
Power:	PG2
Reset:	soft

Programming Notes

Refer to Color Space Conversion page for programming details and examples.

DWord	Bit	Description
0	31:16	**RY** Format: CSC COEFFICIENT FORMAT
	15:0	**GY**

PLANE_CSC_COEFF		
		Format: CSC COEFFICIENT FORMAT
1	31:16	**BY** Format: CSC COEFFICIENT FORMAT
	15:0	**Reserved** Format: MBZ
2	31:16	**RU** Format: CSC COEFFICIENT FORMAT
	15:0	**GU** Format: CSC COEFFICIENT FORMAT
3	31:16	**BU** Format: CSC COEFFICIENT FORMAT
	15:0	**Reserved** Format: MBZ
4	31:16	**RV** Format: CSC COEFFICIENT FORMAT
	15:0	**GV** Format: CSC COEFFICIENT FORMAT
5	31:16	**BV** Format: CSC COEFFICIENT FORMAT
	15:0	**Reserved** Format: MBZ

PLANE_CSC_POSTOFF

PLANE_CSC_POSTOFF	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	96
Double Buffer Update Point:	Start of vertical blank after armed
Double Buffer Armed By:	Write to PLANE_SURF
Address:	70234h-7023Fh
Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_1_A
Power:	PG1
Reset:	soft
Address:	70334h-7033Fh
Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_2_A
Power:	PG1
Reset:	soft
Address:	70434h-7043Fh
Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_3_A
Power:	PG1
Reset:	soft
Address:	71234h-7123Fh
Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_1_B
Power:	PG2
Reset:	soft
Address:	71334h-7133Fh

PLANE_CSC_POSTOFF

Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_2_B
Power:	PG2
Reset:	soft

Address:	71434h-7143Fh
Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_3_B
Power:	PG2
Reset:	soft

Address:	72234h-7223Fh
Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_1_C
Power:	PG2
Reset:	soft

Address:	72334h-7233Fh
Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_2_C
Power:	PG2
Reset:	soft

Address:	72434h-7243Fh
Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_3_C
Power:	PG2
Reset:	soft

The post-offset is intended to add an offset from 0 on the Y or RGB channels and to convert UV channels from 2's complement to excess 0.5 as they exit plane color space conversion (CSC).

DWord	Bit	Description
0	31:13	**Reserved** Format: MBZ
	12:0	**PostCSC High Offset** This value is used to give an offset to the high color channel as it exits CSC logic. The value is a

PLANE_CSC_POSTOFF		
		2's complement fraction allowing offsets between -1 and +1 (exclusive).
1	31:13	**Reserved** Format: MBZ
	12:0	**PostCSC Medium Offset** This value is used to give an offset to the medium color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
2	31:13	**Reserved** Format: MBZ
	12:0	**PostCSC Low Offset** This value is used to give an offset to the low color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).

PLANE_CSC_PREOFF

PLANE_CSC_PREOFF	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	96
Double Buffer Update Point:	Start of vertical blank after armed
Double Buffer Armed By:	Write to PLANE_SURF
Address:	70228h-70233h
Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_1_A
Power:	PG1
Reset:	soft
Address:	70328h-70333h
Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_2_A
Power:	PG1
Reset:	soft
Address:	70428h-70433h
Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_3_A
Power:	PG1
Reset:	soft
Address:	71228h-71233h
Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_1_B
Power:	PG2
Reset:	soft
Address:	71328h-71333h

PLANE_CSC_PREOFF

Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_2_B
Power:	PG2
Reset:	soft

Address:	71428h-71433h
Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_3_B
Power:	PG2
Reset:	soft

Address:	72228h-72233h
Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_1_C
Power:	PG2
Reset:	soft

Address:	72328h-72333h
Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_2_C
Power:	PG2
Reset:	soft

Address:	72428h-72433h
Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_3_C
Power:	PG2
Reset:	soft

The pre-offset is intended to remove an offset from 0 on the Y or RGB channels and to convert UV channels from excess 0.5 to 2's complement as they enter plane color space conversion (CSC).
RGB modes:Red is in the High channel, Green in Medium, and Blue in Low.
YUV modes:V is in the High channel, Y in Medium, and U in Low.

DWord	Bit	Description
0	31:13	**Reserved** Format: MBZ

PLANE_CSC_PREOFF		
	12:0	**PreCSC High Offset** This value is used to give an offset to the high color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
1	31:13	**Reserved** Format: MBZ
	12:0	**PreCSC Medium Offset** This value is used to give an offset to the medium color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
2	31:13	**Reserved** Format: MBZ
	12:0	**PreCSC Low Offset** This value is used to give an offset to the low color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).

PLANE_CTL

PLANE_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed
Double Buffer Armed By:	Write to PLANE_SURF or plane not enabled
Address:	70480h-70483h
Name:	Plane Control
ShortName:	PLANE_CTL_4_A
Power:	PG1
Reset:	soft
Address:	70580h-70583h
Name:	Plane Control
ShortName:	PLANE_CTL_5_A
Power:	PG1
Reset:	soft
Address:	70680h-70683h
Name:	Plane Control
ShortName:	PLANE_CTL_6_A
Power:	PG1
Reset:	soft
Address:	70780h-70783h
Name:	Plane Control
ShortName:	PLANE_CTL_7_A
Power:	PG1
Reset:	soft
Address:	71480h-71483h
Name:	Plane Control
ShortName:	PLANE_CTL_4_B
Power:	PG2
Reset:	soft

PLANE_CTL	
Address:	71580h-71583h
Name:	Plane Control
ShortName:	PLANE_CTL_5_B
Power:	PG2
Reset:	soft
Address:	71680h-71683h
Name:	Plane Control
ShortName:	PLANE_CTL_6_B
Power:	PG2
Reset:	soft
Address:	71780h-71783h
Name:	Plane Control
ShortName:	PLANE_CTL_7_B
Power:	PG2
Reset:	soft
Address:	72480h-72483h
Name:	Plane Control
ShortName:	PLANE_CTL_4_C
Power:	PG2
Reset:	soft
Address:	72580h-72583h
Name:	Plane Control
ShortName:	PLANE_CTL_5_C
Power:	PG2
Reset:	soft
Address:	72680h-72683h
Name:	Plane Control
ShortName:	PLANE_CTL_6_C
Power:	PG2
Reset:	soft
Address:	72780h-72783h
Name:	Plane Control
ShortName:	PLANE_CTL_7_C
Power:	PG2
Reset:	soft

PLANE_CTL	
Address:	70180h-70183h
Name:	Plane Control
ShortName:	PLANE_CTL_1_A
Power:	PG1
Reset:	soft
Address:	70280h-70283h
Name:	Plane Control
ShortName:	PLANE_CTL_2_A
Power:	PG1
Reset:	soft
Address:	70380h-70383h
Name:	Plane Control
ShortName:	PLANE_CTL_3_A
Power:	PG1
Reset:	soft
Address:	71180h-71183h
Name:	Plane Control
ShortName:	PLANE_CTL_1_B
Power:	PG2
Reset:	soft
Address:	71280h-71283h
Name:	Plane Control
ShortName:	PLANE_CTL_2_B
Power:	PG2
Reset:	soft
Address:	71380h-71383h
Name:	Plane Control
ShortName:	PLANE_CTL_3_B
Power:	PG2
Reset:	soft
Address:	72180h-72183h
Name:	Plane Control
ShortName:	PLANE_CTL_1_C
Power:	PG2
Reset:	soft

PLANE_CTL

Address:	72280h-72283h
Name:	Plane Control
ShortName:	PLANE_CTL_2_C
Power:	PG2
Reset:	soft

Address:	72380h-72383h
Name:	Plane Control
ShortName:	PLANE_CTL_3_C
Power:	PG2
Reset:	soft

The pipe scaler can be attached to a plane to scale the plane output before blending.

Restriction
Refer to 'Plane Capability and Interoperability' page for plane capabilities and restrictions.

DWord	Bit	Description
0	31	**Plane Enable** When this bit is set, the plane will generate pixels for display. When cleared to zero, plane memory fetches cease and plane output is transparent. Value: 0b — Name: Disable Value: 1b — Name: Enable
	30:28	**Pipe Slice Arbitration Slots** This field specifies the number of slots allocated to this plane in pipe slice request arbitration. This field is ignored when the 'PIPE_SLICE_ARBITRATION_CTL->Use Programmed Slots' is not set. This field is zero based; a programmed value of 0 results in 1 slot allocation.
	27:23	**Source Pixel Format** This field selects the source pixel format for the plane. Before entering the blender, each source format is converted to the pipe pixel format. The 8-bpp indexed format will always use the pipe palette. In planar YUV formats Y samples appear first in memory followed by interleaved UV samples. YUV 4:2:2 byte order is programmed separately. YUV 4:2:0 and YUV 4:4:4 byte order is not programmable. RGB color order is programmed separately for some formats. Refer to Universal Plane, Plane Pixel Formats section for color channel bit mappings. YUV 4:2:0 P010, P012 and P016 formats share the same 16 bpc memory layout but use 10, 12 and 16 bits per channel respectively. The color values are stored in the most significant bits.

64-bit formats supported only on the HDR planes.
P01x output is only allowed from HDR planes.

Value	Name	Description
00000b	YUV 422 Packed 8 bpc	YUV 4:2:2 packed, 8 bpc
00010b	YUV 420 Planar 8 bpc	YUV 4:2:0 Planar, 8 bpc - NV12
00100b	RGB 2101010	RGB 2:10:10:10, 32 bit.
00110b	YUV 420 Planar 10 bpc	YUV 4:2:0 Planar, 10 bpc - P010
01000b	RGB 8888	RGB 8:8:8:8, 32 bit
01010b	YUV 420 Planar 12 bpc	YUV 4:2:0 Planar 12 bpc - P012
01100b	RGB 16161616 Float	RGB 16:16:16:16 Floating Point, 64 bit (FP16)
01110b	YUV 420 Planar 16 bpc	YUV 4:2:0 Planar, 16 bpc - P016
10000b	YUV 444 Packed 8 bpc	YUV 4:4:4 packed (MSB-X:Y:U:V), 8bpc
10100b	RGB 2101010 XR_BIAS	RGB 2:10:10:10 Extended Range Bias (MSB-X:B:G:R), 32 bit
11000b	Indexed 8 bit	Indexed 8-bit
11100b	RGB 565	RGB 5:6:5 (MSB-R:G:B), 16 bit
00001b	YUV 422 Packed 10 bpc	YUV 4:2:2 packed, 10 bpc - Y210
00011b	YUV 422 Packed 12 bpc	YUV 4:2:2 packed, 12 bpc - Y212
00101b	YUV 422 Packed 16 bpc	YUV 4:2:2 packed, 16 bpc - Y216
00111b	YUV 444 Packed 10 bpc	YUV 4:4:4 packed (MSB-X:V:Y:U), 10 bpc - Y410
01001b	YUV 444 Packed 12 bpc	YUV 4:4:4 packed (MSB-X:V:Y:U), 12 bpc - Y412
01011b	YUV 444 Packed 16 bpc	YUV 4:4:4 packed (MSB-X:V:Y:U), 16 bpc - Y416

Restriction
Plane scaling is not compatible with the Indexed 8-bit, XR_BIAS source pixel formats.

22:21 **Key Enable**
This field enables color keying. The key color, range, channel enables, and mask are programmed in PLANE_KEYVAL, PLANE_KEYMSK, and PLANE_KEYMAX.

Value	Name	Description
00b	Disable	Disable keying for this plane.
01b	Source Key Enable	This plane's pixels will be checked for a key match. The blend between this plane and the plane below will treat the key matched pixels as transparent.
10b	Destination Key Enable	This plane's pixels will be checked for a key match. The blend between this plane and the plane above will treat the pixels above as opaque only where this plane is key matched and the plane above is opaque. When plane gamma is enabled, the gamma processing may shift the pixel color values sent to blender and may cause it to not match the

		key color as desired. The recommendation is to use the pipe gamma when destination keying is enabled.
11b	Source Key Window Enable	This plane's pixels will be checked for a key match. The blend between this plane and the plane below will treat the key matched pixels as transparent only where the plane below is opaque.

Restriction
Plane color keying is not compatible with the Indexed 8-bit pixel format. Destination key/Source Key Window should be enabled only on one set (a pair) of planes, per pipe, at a time. Source key and Source Key Window must not be enabled on the bottom most active plane. Destination key must not be enabled on the top most active plane.

20 **RGB Color Order**

This field is used to select the color order when using RGB data formats, except RGB 32-bit XR_BIAS 10:10:10 and 16-bit BGRX 5:6:5. For other formats, this field is ignored.

Value	Name	Description
0b	BGRX	BGRX (MSB-X:R:G:B)
1b	RGBX	RGBX (MSB-X:B:G:R)

19 **Planar YUV420 component**

This field selects the planar YUV420 component for the plane when NV12/P0xx source pixel formats is used. This field must be set to '0b' for other (YUV non-planar/RGB) surface formats.

Value	Name	Description
0b	UV	Planes 1 to 5 can be configured as UV plane. Planes 6 and 7 must not be configured as a UV plane.
1b	Y	Planes 6 and 7 can be configured as Y plane. Planes 1 to 5 must not be configured as a Y plane.

18 **Reserved**

Format:	MBZ

17:16 **YUV 422 Byte Order**

This field is used to select the byte order for YUV 4:2:2 data formats. For other formats, this field is ignored.

Value	Name	Description
00b	YUYV	YUYV (MSB-V:Y2:U:Y1)
01b	UYVY	UYVY (MSB-Y2:V:Y1:U)
10b	YVYU	YVYU (MSB-U:Y2:V:Y1)
11b	VYUY	VYUY (MSB-Y2:U:Y1:V)

15 **Render Decomp**

This bit enables the Display decompression of Render compressed surfaces.

Value	Name
0b	Disable
1b	Enable

Restriction
Color Clear is not supported.
Only the Left-right cache-line pair decompression is supported. The compressed surface should be Y (Legacy) or Y F Tiled. Decompression is not supported with 90/270 degree rotation.
Decompression is supported with RGB8888 and RGB1010102 formats.
Decompression is supported on all planes and pipes.

14 **Trickle Feed Enable**

Value	Name
0b	Enable
1b	Disable

Restriction
Do not program this field to 1b.

13 **Reserved**

Format:	MBZ

12:10 **Tiled Surface**

This field indicates that the surface data is in tiled memory. This bit may be updated through MMIO writes or through a command streamer initiated synchronous flip.

Value	Name
000b	Linear memory
001b	Tile X memory
100b	Tile Y (Legacy) memory
101b	Tile Y F memory

Restriction
Interlaced mode is not supported with Y Tiling. Tile Ys is not supported.

9 **Async Address Update Enable**

Access:	R/W

This bit will enable asynchronous updates of the plane surface address when written by MMIO (MMIO asynchronous flips). The surface address will change as soon as possible. This bit is not double buffered and the changes will apply immediately. When performing an asynchronous update, only the plane surface can be updated. Changes to stride, pixel, format, RenderCompression, FBC, etc. are not allowed.

Value	Name	Description
0b	Sync	Surface Address MMIO writes will update synchronous to start of vertical blank
1b	Async	Surface Address MMIO writes will update asynchronous to start of vertical blank

Restriction
No command streamer (ring) flips to this plane are allowed when this bit is enabled. Each surface address write must be followed by a wait for flip done indication before writing the surface address register again.

8 **Horizontal Flip**

This field controls the horizontal flipping of the plane. When horizontal flipping is enabled with rotation, the horizontal flip operation is logically performed first followed by rotation. For further information refer to "Universal Plane" section.

Value	Name
0b	Disable **[Default]**
1b	Enable

Restriction
Horizontal flip is not supported with linear surface formats.

7:6 **Stereo Surface Vblank Mask**

This field controls which vertical blank (left eye, right eye, or both) will be used for the plane surface address double-buffering during stereo 3D mode. This field is ignored when not in stereo 3D mode.

Value	Name	Description
00b	Mask None	Both the left and right eye vertical blanks will be used.
01b	Mask Left	Mask the left eye vertical blank. Only the right eye vertical blank will be used.
10b	Mask Right	Mask the right eye vertical blank. Only the left eye vertical blank will be used.

5:4 **Reserved**

Format:	MBZ

3 **Allow Double Buffer Update Disable**

Access:	R/W	

This field controls whether double buffer updates are allowed to be disabled for this plane. The DOUBLE_BUFFER_CTL register can be configured to globally disable double buffer updates for resources that allow them to be disabled. This field applies only to the plane registers that supports double buffering. Scaler registers used for plane scaling purposes are not included in this.

Value	Name
0b	Not Allowed
1b	Allowed

2 **Reserved**

Format:	MBZ

1:0 **Plane Rotation**

This field controls hardware rotation of the plane.

Value	Name
00b	No rotation
01b	90 degree rotation
10b	180 degree rotation
11b	270 degree rotation

Programming Notes
Hardware does not change the plane position when rotation is enabled. Software may need to adjust the plane position to match the physical orientation of the display.

Restriction
90/270 degree rotation requires the surface to be Y Tiled. Interlaced mode is not supported with 90/270 degree rotation. Render-Display decompression is not supported with 90/270 degree rotation.
90/270 rotation is supported with plane width (pre-rotation) up to 4096 pixels.

PLANE_CUS_CTL

PLANE_CUS_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed
Double Buffer Armed By:	Write to PLANE_SURF or plane not enabled
Address:	701C8h-701CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_1_A
Power:	PG1
Reset:	soft
Address:	702C8h-702CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_2_A
Power:	PG1
Reset:	soft
Address:	703C8h-703CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_3_A
Power:	PG1
Reset:	soft
Address:	711C8h-711CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_1_B
Power:	PG2
Reset:	soft
Address:	712C8h-712CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_2_B
Power:	PG2
Reset:	soft

PLANE_CUS_CTL

Address:	713C8h-713CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_3_B
Power:	PG2
Reset:	soft

Address:	721C8h-721CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_1_C
Power:	PG2
Reset:	soft

Address:	722C8h-722CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_2_C
Power:	PG2
Reset:	soft

Address:	723C8h-723CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_3_C
Power:	PG2
Reset:	soft

Description

This register programs the chroma upsampler for processing pixel streams from hybrid planar YUV 420 (NV12, P0xx) surfaces.
This dedicated chroma upsampling capability is available only in Planes 1 through 3. Planes 4 and 5 must use plane scaler (PS_CTRL) for chroma upsampling.
The following table shows phase programming for frequently used YUV420 to YUV444 chroma upsampling scenarios.

YUV 420Chroma Siting	Horz Phase	Vert Phase	Programmed Horz Initial Phase	Programmed Horz Initial Phase Sign	Programmed Vert Initial Phase	Programmed Vert Initial Phase Sign
Top Left	0	0	0	0	0	0
Top	-0.25	0	0.25	1	0	0
Left (MPEG-2)	0	-0.25	0	0	0.25	1
Center (MPEG-1)	-0.25	-0.25	0.25	1	0.25	1

Restriction :
When the Chroma upsampler is enabled, then:

PLANE_CUS_CTL

1. The maximum horizontal plane size allowed is 4096 pixels
2. The minimum horizontal plane size allowed is 8 pixels
3. The minimum vertical plane size allowed is 4 lines
4. The horizontal and vertical plane size should be even

DWord	Bit	Description
0	31	**Chroma Upsampler Enable** This field enables the plane chroma upsampler for handling hybrid planar YUV 420 (NV12, P0xx) formats. Value: 0b = Disable; 1b = Enable
	30	**Y Binding** This field defines the Y plane from where the chroma upsampler will receive the Y pixels stream when processing hybrid planar YUV 420 (NV12, P0xx) formats. Value: 0b = Plane 6; 1b = Plane 7
	29:20	**Reserved** Format: MBZ
	19	**Horz Initial Phase Sign** This field is defines the direction of the horizontal initial phase adjustment on the UV stream during upsampling. A positive initial phase will have an effect of shifting the UV pixels to the right with respect to the Y pixels whereas a negative initial phase will have an effect of shifting left. The sign bit must be zero if the initial phase is zero. Value: 0b = Positive Initial Phase; 1b = Negative Initial Phase
	18	**Reserved** Format: MBZ
	17:16	**Horz Initial Phase** This field defines the horizontal initial phase adjustment required on the UV stream during upsampling. This field should be programmed based on the YUV 420 chroma siting. Value: 00b = 0; 01b = 0.25

PLANE_CUS_CTL

	10b	0.5
	11b	Reserved

15 — Vert Initial Phase Sign

This field is defines the direction of the vertical initial phase adjustment on the UV stream during upsampling.
A positive initial phase will have an effect of shifting the UV pixels down with respect to the Y pixels whereas a negative initial phase will have an effect of shifting up.
The sign bit must be zero if the initial phase is zero.

Value	Name
0b	Positive Initial Phase
1b	Negative Initial Phase

14 — Reserved

Format:	MBZ

13:12 — Vert Initial Phase

This field defines the vertical initial phase adjustment required on the UV stream during upsampling. This field should be programmed based on the YUV 420 chroma siting.

Value	Name
00b	0
01b	0.25
10b	0.5
11b	Reserved

11 — Reserved

10:9 — Power Up Delay

This field indicates the wait (in CD clocks) between powering up the line buffer arrays.

8 — Reserved

7:6 — Reserved

Format:	MBZ

5 — ECC Single Error

Access:	R/WC

This field indicates that an single bit error encountered at the ECC logic. Hardware will correct the single bit errors. Hardware will set the bit; SW can clear with a write of 1.

4 — ECC Double Error

Access:	R/WC

This field indicates that an double bit error encountered at the ECC logic. Hardware will not correct the double bit errors. Hardware will set the bit; SW can clear with a write of 1.

3:1 — Reserved

PLANE_CUS_CTL			
		Format:	MBZ
	0	**Power Up In Progress** Access: RO This field is set when the chroma upsampler line buffers are being powered up. Chroma upsampler cannot handle pixel traffic when this bit is set.	

PLANE_INPUT_CSC_COEFF

PLANE_INPUT_CSC_COEFF	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	192
Double Buffer Update Point:	Start of vertical blank after armed
Double Buffer Armed By:	Write to PLANE_SURF
Address:	701E0h-701F7h
Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_1_A
Power:	PG1
Reset:	soft
Address:	702E0h-702F7h
Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_2_A
Power:	PG1
Reset:	soft
Address:	703E0h-703F7h
Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_3_A
Power:	PG1
Reset:	soft
Address:	711E0h-711F7h
Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_1_B
Power:	PG2
Reset:	soft
Address:	712E0h-712F7h

PLANE_INPUT_CSC_COEFF

Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_2_B
Power:	PG2
Reset:	soft

Address:	713E0h-713F7h
Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_3_B
Power:	PG2
Reset:	soft

Address:	721E0h-721F7h
Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_1_C
Power:	PG2
Reset:	soft

Address:	722E0h-722F7h
Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_2_C
Power:	PG2
Reset:	soft

Address:	723E0h-723F7h
Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_3_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31:16	**RY** Format: CSC COEFFICIENT FORMAT
	15:0	**GY** Format: CSC COEFFICIENT FORMAT
1	31:16	**BY** Format: CSC COEFFICIENT FORMAT

PLANE_INPUT_CSC_COEFF		
	15:0	**Reserved** Format: MBZ
2	31:16	**RU** Format: CSC COEFFICIENT FORMAT
	15:0	**GU** Format: CSC COEFFICIENT FORMAT
3	31:16	**BU** Format: CSC COEFFICIENT FORMAT
	15:0	**Reserved** Format: MBZ
4	31:16	**RV** Format: CSC COEFFICIENT FORMAT
	15:0	**GV** Format: CSC COEFFICIENT FORMAT
5	31:16	**BV** Format: CSC COEFFICIENT FORMAT
	15:0	**Reserved** Format: MBZ

PLANE_INPUT_CSC_POSTOFF

PLANE_INPUT_CSC_POSTOFF	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	96
Double Buffer Update Point:	Start of vertical blank after armed
Double Buffer Armed By:	Write to PLANE_SURF
Address:	70204h-7020Fh
Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_1_A
Power:	PG1
Reset:	soft
Address:	70304h-7030Fh
Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_2_A
Power:	PG1
Reset:	soft
Address:	70404h-7040Fh
Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_3_A
Power:	PG1
Reset:	soft
Address:	71204h-7120Fh
Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_1_B
Power:	PG2
Reset:	soft
Address:	71304h-7130Fh

PLANE_INPUT_CSC_POSTOFF

Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_2_B
Power:	PG2
Reset:	soft
Address:	71404h-7140Fh
Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_3_B
Power:	PG2
Reset:	soft
Address:	72204h-7220Fh
Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_1_C
Power:	PG2
Reset:	soft
Address:	72304h-7230Fh
Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_2_C
Power:	PG2
Reset:	soft
Address:	72404h-7240Fh
Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_3_C
Power:	PG2
Reset:	soft

The post-offset is intended to add an offset from 0 on the Y or RGB channels and to convert UV channels from 2's complement to excess 0.5 as they exit plane input color space conversion (CSC).

DWord	Bit	Description
0	31:13	**Reserved** Format: MBZ
	12:0	**PostCSC High Offset** This value is used to give an offset to the high color channel as it exits CSC logic. The value is a

PLANE_INPUT_CSC_POSTOFF		
		2's complement fraction allowing offsets between -1 and +1 (exclusive).
1	31:13	**Reserved** Format: MBZ
	12:0	**PostCSC Medium Offset** This value is used to give an offset to the medium color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
2	31:13	**Reserved** Format: MBZ
	12:0	**PostCSC Low Offset** This value is used to give an offset to the low color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).

PLANE_INPUT_CSC_PREOFF

PLANE_INPUT_CSC_PREOFF	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	96
Double Buffer Update Point:	Start of vertical blank after armed
Double Buffer Armed By:	Write to PLANE_SURF
Address:	701F8h-70203h
Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_1_A
Power:	PG1
Reset:	soft
Address:	702F8h-70303h
Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_2_A
Power:	PG1
Reset:	soft
Address:	703F8h-70403h
Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_3_A
Power:	PG1
Reset:	soft
Address:	711F8h-71203h
Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_1_B
Power:	PG2
Reset:	soft
Address:	712F8h-71303h

PLANE_INPUT_CSC_PREOFF

Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_2_B
Power:	PG2
Reset:	soft

Address:	713F8h-71403h
Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_3_B
Power:	PG2
Reset:	soft

Address:	721F8h-72203h
Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_1_C
Power:	PG2
Reset:	soft

Address:	722F8h-72303h
Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_2_C
Power:	PG2
Reset:	soft

Address:	723F8h-72403h
Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_3_C
Power:	PG2
Reset:	soft

The pre-offset is intended to remove an offset from 0 on the Y or RGB channels and to convert UV channels from excess 0.5 to 2's complement as they enter plane input color space conversion (CSC).

DWord	Bit	Description
0	31:13	**Reserved** Format: MBZ
	12:0	**PreCSC High Offset** This value is used to give an offset to the high color channel as it enters CSC logic. The value is a

PLANE_INPUT_CSC_PREOFF		
		2's complement fraction allowing offsets between -1 and +1 (exclusive).
1	31:13	**Reserved** Format: MBZ
	12:0	**PreCSC Medium Offset** This value is used to give an offset to the medium color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
2	31:13	**Reserved** Format: MBZ
	12:0	**PreCSC Low Offset** This value is used to give an offset to the low color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).

PLANE_KEYMAX

PLANE_KEYMAX	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank, pipe not enabled, or plane not enabled
Address:	704A0h-704A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_4_A
Power:	PG1
Reset:	soft
Address:	705A0h-705A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_5_A
Power:	PG1
Reset:	soft
Address:	706A0h-706A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_6_A
Power:	PG1
Reset:	soft
Address:	707A0h-707A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_7_A
Power:	PG1
Reset:	soft
Address:	714A0h-714A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_4_B
Power:	PG2
Reset:	soft
Address:	715A0h-715A3h

PLANE_KEYMAX	
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_5_B
Power:	PG2
Reset:	soft
Address:	716A0h-716A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_6_B
Power:	PG2
Reset:	soft
Address:	717A0h-717A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_7_B
Power:	PG2
Reset:	soft
Address:	724A0h-724A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_4_C
Power:	PG2
Reset:	soft
Address:	725A0h-725A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_5_C
Power:	PG2
Reset:	soft
Address:	726A0h-726A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_6_C
Power:	PG2
Reset:	soft
Address:	727A0h-727A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_7_C
Power:	PG2
Reset:	soft
Address:	701A0h-701A3h

PLANE_KEYMAX	
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_1_A
Power:	PG1
Reset:	soft
Address:	702A0h-702A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_2_A
Power:	PG1
Reset:	soft
Address:	703A0h-703A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_3_A
Power:	PG1
Reset:	soft
Address:	711A0h-711A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_1_B
Power:	PG2
Reset:	soft
Address:	712A0h-712A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_2_B
Power:	PG2
Reset:	soft
Address:	713A0h-713A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_3_B
Power:	PG2
Reset:	soft
Address:	721A0h-721A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_1_C
Power:	PG2
Reset:	soft
Address:	722A0h-722A3h

PLANE_KEYMAX

Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_2_C
Power:	PG2
Reset:	soft

Address:	723A0h-723A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_3_C
Power:	PG2
Reset:	soft

Key Max Value fields: When plane source is YUV, this register specifies the maximum YUV key value to be used together with the minimum YUV key value and the channel enables to determine if the plane matches the key. When plane source is RGB, these fields are not used.

DWord	Bit	Description
0	31:24	**Plane Alpha Value** Specifies the plane alpha value when plane alpha is enabled in PLANE_KEYMSK register.
	23:16	**V Key Max Value** Specifies the maximum key value for the V channel.
	15:8	**Y Key Max Value** Specifies the maximum key value for the Y channel.
	7:0	**U Key Max Value** Specifies the maximum key value for the U channel.

PLANE_KEYMSK

PLANE_KEYMSK	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank, pipe not enabled, or plane not enabled
Address:	70498h-7049Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_4_A
Power:	PG1
Reset:	soft
Address:	70598h-7059Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_5_A
Power:	PG1
Reset:	soft
Address:	70698h-7069Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_6_A
Power:	PG1
Reset:	soft
Address:	70798h-7079Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_7_A
Power:	PG1
Reset:	soft
Address:	71498h-7149Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_4_B
Power:	PG2
Reset:	soft
Address:	71598h-7159Bh

PLANE_KEYMSK	
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_5_B
Power:	PG2
Reset:	soft
Address:	71698h-7169Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_6_B
Power:	PG2
Reset:	soft
Address:	71798h-7179Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_7_B
Power:	PG2
Reset:	soft
Address:	72498h-7249Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_4_C
Power:	PG2
Reset:	soft
Address:	72598h-7259Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_5_C
Power:	PG2
Reset:	soft
Address:	72698h-7269Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_6_C
Power:	PG2
Reset:	soft
Address:	72798h-7279Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_7_C
Power:	PG2
Reset:	soft
Address:	70198h-7019Bh

PLANE_KEYMSK	
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_1_A
Power:	PG1
Reset:	soft
Address:	70298h-7029Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_2_A
Power:	PG1
Reset:	soft
Address:	70398h-7039Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_3_A
Power:	PG1
Reset:	soft
Address:	71198h-7119Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_1_B
Power:	PG2
Reset:	soft
Address:	71298h-7129Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_2_B
Power:	PG2
Reset:	soft
Address:	71398h-7139Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_3_B
Power:	PG2
Reset:	soft
Address:	72198h-7219Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_1_C
Power:	PG2
Reset:	soft
Address:	72298h-7229Bh

PLANE_KEYMSK

Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_2_C
Power:	PG2
Reset:	soft

Address:	72398h-7239Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_3_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31	**Plane Alpha Enable** Description: Enables the plane alpha. Color channels will be pre-multiplied by hardware with the plane alpha value from PLANE_KEYMAX register. Per-pixel alpha is defined in the PLANE_COLOR_CTL register. Value: 0b — Name: Disable Value: 1b — Name: Enable
	30:27	**Reserved** Format: MBZ
	26	**V or R Key Channel Enable** Enables the V/Red channel for key comparison. A disabled channel will be ignored when determining a key match. Value: 0b — Name: Disable Value: 1b — Name: Enable
	25	**Y or G Key Channel Enable** Enables the Y/Green channel for key comparison. A disabled channel will be ignored when determining a key match. Value: 0b — Name: Disable Value: 1b — Name: Enable
	24	**U or B Key Channel Enable** Enables the U/Blue channel for key comparison. A disabled channel will be ignored when determining a key match. Value — Name

PLANE_KEYMSK			
		0b	Disable
		1b	Enable
	23:16	**R Key Mask Value** Specifies the key mask for the Red channel. A zero bit in the mask indicates that the corresponding bit will be ignored when determining a key match.	
	15:8	**G Key Mask Value** Specifies the key mask for the Green channel. A zero bit in the mask indicates that the corresponding bit will be ignored when determining a key match.	
	7:0	**B Key Mask Value** Specifies the key mask for the Blue channel. A zero bit in the mask indicates that the corresponding bit will be ignored when determining a key match.	

PLANE_KEYVAL

PLANE_KEYVAL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank, pipe not enabled, or plane not enabled
Address:	70494h-70497h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_4_A
Power:	PG1
Reset:	soft
Address:	70594h-70597h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_5_A
Power:	PG1
Reset:	soft
Address:	70694h-70697h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_6_A
Power:	PG1
Reset:	soft
Address:	70794h-70797h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_7_A
Power:	PG1
Reset:	soft
Address:	71494h-71497h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_4_B
Power:	PG2
Reset:	soft
Address:	71594h-71597h

PLANE_KEYVAL	
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_5_B
Power:	PG2
Reset:	soft
Address:	71694h-71697h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_6_B
Power:	PG2
Reset:	soft
Address:	71794h-71797h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_7_B
Power:	PG2
Reset:	soft
Address:	72494h-72497h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_4_C
Power:	PG2
Reset:	soft
Address:	72594h-72597h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_5_C
Power:	PG2
Reset:	soft
Address:	72694h-72697h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_6_C
Power:	PG2
Reset:	soft
Address:	72794h-72797h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_7_C
Power:	PG2
Reset:	soft
Address:	70194h-70197h

PLANE_KEYVAL	
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_1_A
Power:	PG1
Reset:	soft
Address:	70294h-70297h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_2_A
Power:	PG1
Reset:	soft
Address:	70394h-70397h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_3_A
Power:	PG1
Reset:	soft
Address:	71194h-71197h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_1_B
Power:	PG2
Reset:	soft
Address:	71294h-71297h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_2_B
Power:	PG2
Reset:	soft
Address:	71394h-71397h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_3_B
Power:	PG2
Reset:	soft
Address:	72194h-72197h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_1_C
Power:	PG2
Reset:	soft
Address:	72294h-72297h

PLANE_KEYVAL

Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_2_C
Power:	PG2
Reset:	soft

Address:	72394h-72397h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_3_C
Power:	PG2
Reset:	soft

When plane source is YUV, this register specifies the minimum YUV key value to be used together with the maximum YUV key value and the channel enables to determine if the plane matches the key. When plane source is RGB, this register specifies the RGB key value to be used together with the channel masks to determine if the plane matches the key. RGB key matches can only occur for positive pixel values in the 0 to 1 range. Extended range pixel values will not match. MSB bits are used for comparison.

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:16	**V Min or R Key Value** Specifies the minimum key value for the V channel or the compare value for Red channel.
	15:8	**Y Min or G Key Value** Specifies the minimum key value for the Y channel or the compare value for Green channel.
	7:0	**U Min or B Key Value** Specifies the minimum key value for the U channel or the compare value for Blue channel.

PLANE_LEFT_SURF

PLANE_LEFT_SURF	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of left or right eye vertical blank (selectable), pipe not enabled. or plane not enabled; after armed
Double Buffer Armed By:	Write to PLANE_SURF or plane not enabled
Address:	704B0h-704B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_4_A
Power:	PG1
Reset:	soft
Address:	705B0h-705B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_5_A
Power:	PG1
Reset:	soft
Address:	706B0h-706B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_6_A
Power:	PG1
Reset:	soft
Address:	707B0h-707B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_7_A
Power:	PG1
Reset:	soft
Address:	714B0h-714B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_4_B
Power:	PG2
Reset:	soft

PLANE_LEFT_SURF	
Address:	715B0h-715B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_5_B
Power:	PG2
Reset:	soft
Address:	716B0h-716B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_6_B
Power:	PG2
Reset:	soft
Address:	717B0h-717B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_7_B
Power:	PG2
Reset:	soft
Address:	724B0h-724B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_4_C
Power:	PG2
Reset:	soft
Address:	725B0h-725B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_5_C
Power:	PG2
Reset:	soft
Address:	726B0h-726B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_6_C
Power:	PG2
Reset:	soft
Address:	727B0h-727B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_7_C
Power:	PG2
Reset:	soft

PLANE_LEFT_SURF	
Address:	701B0h-701B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_1_A
Power:	PG1
Reset:	soft
Address:	702B0h-702B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_2_A
Power:	PG1
Reset:	soft
Address:	703B0h-703B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_3_A
Power:	PG1
Reset:	soft
Address:	711B0h-711B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_1_B
Power:	PG2
Reset:	soft
Address:	712B0h-712B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_2_B
Power:	PG2
Reset:	soft
Address:	713B0h-713B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_3_B
Power:	PG2
Reset:	soft
Address:	721B0h-721B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_1_C
Power:	PG2
Reset:	soft

PLANE_LEFT_SURF

Address:	722B0h-722B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_2_C
Power:	PG2
Reset:	soft

Address:	723B0h-723B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_3_C
Power:	PG2
Reset:	soft

Restriction

This register must be programmed with a valid address prior to enabling stereo 3D on this pipe.

DWord	Bit	Description
0	31:12	**Left Surface Base Address** Format: GraphicsAddress[31:12] This address specifies the stereo 3D left eye surface base address bits 31:12. **Restriction** This surface must have the same stride, tiling, and panning offset parameters as the right eye surface and meet all the same restrictions.
	11:0	**Reserved**

PLANE_OFFSET

PLANE_OFFSET	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank, pipe not enabled, or plane not enabled
Address:	704A4h-704A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_4_A
Power:	PG1
Reset:	soft
Address:	705A4h-705A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_5_A
Power:	PG1
Reset:	soft
Address:	706A4h-706A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_6_A
Power:	PG1
Reset:	soft
Address:	707A4h-707A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_7_A
Power:	PG1
Reset:	soft
Address:	714A4h-714A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_4_B
Power:	PG2
Reset:	soft
Address:	715A4h-715A7h

PLANE_OFFSET	
Name:	Plane Offset
ShortName:	PLANE_OFFSET_5_B
Power:	PG2
Reset:	soft
Address:	716A4h-716A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_6_B
Power:	PG2
Reset:	soft
Address:	717A4h-717A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_7_B
Power:	PG2
Reset:	soft
Address:	724A4h-724A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_4_C
Power:	PG2
Reset:	soft
Address:	725A4h-725A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_5_C
Power:	PG2
Reset:	soft
Address:	726A4h-726A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_6_C
Power:	PG2
Reset:	soft
Address:	727A4h-727A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_7_C
Power:	PG2
Reset:	soft
Address:	701A4h-701A7h

PLANE_OFFSET	
Name:	Plane Offset
ShortName:	PLANE_OFFSET_1_A
Power:	PG1
Reset:	soft
Address:	702A4h-702A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_2_A
Power:	PG1
Reset:	soft
Address:	703A4h-703A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_3_A
Power:	PG1
Reset:	soft
Address:	711A4h-711A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_1_B
Power:	PG2
Reset:	soft
Address:	712A4h-712A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_2_B
Power:	PG2
Reset:	soft
Address:	713A4h-713A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_3_B
Power:	PG2
Reset:	soft
Address:	721A4h-721A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_1_C
Power:	PG2
Reset:	soft
Address:	722A4h-722A7h

PLANE_OFFSET

Name:	Plane Offset
ShortName:	PLANE_OFFSET_2_C
Power:	PG2
Reset:	soft

Address:	723A4h-723A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_3_C
Power:	PG2
Reset:	soft

This register specifies the panning for the plane surface. The start position is specified in this register as a (x, y) offset from the beginning of the surface. When performing 180 rotation, hardware will internally add the plane size to the offsets so the plane will start displaying from the bottom right corner of the image. When performing 90 rotation, the offset programmed should take the rotation in to consideration. X offset = (Surface height in tiles * tile height) - Y offset - Y Size, Y offset = X offset When performing 270 rotation, use the same programming as 90 rotation. For YUV planar format non-rotate cases, the UV surface offsets should be half of the Y surface offsets when the UV surface is tile row aligned. When the UV surface is not tile row aligned, the UV surface Y offset should also include the lines from the previous nearest tile row aligned address.

Restriction
The plane size + offset must not exceed the maximum supported plane size.

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28:16	**Start Y Position** The Start Y Position or the Y Offset is the vertical offset in lines of the beginning of the active display plane relative to the display surface. **Restriction** In 90/270 rotation modes, this offset must be even lines aligned for YUV 4:2:2, YUV 4:2:0 formats.
	15:13	**Reserved** Format: MBZ
	12:0	**Start X Position** The Start X Position or the X Offset is the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. **Restriction** In 0/180 rotation modes, this offset must be even pixel aligned for YUV 4:2:2, YUV 4:2:0 formats.

PLANE_PIXEL_NORMALIZE

PLANE_PIXEL_NORMALIZE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank after armed
Double Buffer Armed By:	Write to PLANE_SURF
Address:	701A8h-701ABh
Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_1_A
Power:	PG1
Reset:	soft
Address:	702A8h-702ABh
Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_2_A
Power:	PG1
Reset:	soft
Address:	703A8h-703ABh
Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_3_A
Power:	PG1
Reset:	soft
Address:	711A8h-711ABh
Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_1_B
Power:	PG2
Reset:	soft
Address:	712A8h-712ABh

PLANE_PIXEL_NORMALIZE

Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_2_B
Power:	PG2
Reset:	soft

Address:	713A8h-713ABh
Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_3_B
Power:	PG2
Reset:	soft

Address:	721A8h-721ABh
Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_1_C
Power:	PG2
Reset:	soft

Address:	722A8h-722ABh
Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_2_C
Power:	PG2
Reset:	soft

Address:	723A8h-723ABh
Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_3_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31	**Enable** This field enables the normalization of FP16 pixels with the specified normalization factor.
	30:16	**Reserved** Format: MBZ
	15:0	**Normalization Factor** This field specifies the normalization factor in the FP16 format. This programmed value is

PLANE_PIXEL_NORMALIZE		
		multipled with the input pixel value and normalized to range -1.0 to 1.0, exclusive.Out of bound values get clamped to be within the range from -1.0 to 1.0, exclusive.The programmed half float value must be a positive and not de-normalized, zero or NAN.

PLANE_POS

PLANE_POS	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed
Double Buffer Armed By:	Write to PLANE_SURF or plane not enabled
Address:	7048Ch-7048Fh
Name:	Plane Position
ShortName:	PLANE_POS_4_A
Power:	PG1
Reset:	soft
Address:	7058Ch-7058Fh
Name:	Plane Position
ShortName:	PLANE_POS_5_A
Power:	PG1
Reset:	soft
Address:	7068Ch-7068Fh
Name:	Plane Position
ShortName:	PLANE_POS_6_A
Power:	PG1
Reset:	soft
Address:	7078Ch-7078Fh
Name:	Plane Position
ShortName:	PLANE_POS_7_A
Power:	PG1
Reset:	soft
Address:	7148Ch-7148Fh
Name:	Plane Position
ShortName:	PLANE_POS_4_B
Power:	PG2
Reset:	soft

PLANE_POS	
Address:	7158Ch-7158Fh
Name:	Plane Position
ShortName:	PLANE_POS_5_B
Power:	PG2
Reset:	soft
Address:	7168Ch-7168Fh
Name:	Plane Position
ShortName:	PLANE_POS_6_B
Power:	PG2
Reset:	soft
Address:	7178Ch-7178Fh
Name:	Plane Position
ShortName:	PLANE_POS_7_B
Power:	PG2
Reset:	soft
Address:	7248Ch-7248Fh
Name:	Plane Position
ShortName:	PLANE_POS_4_C
Power:	PG2
Reset:	soft
Address:	7258Ch-7258Fh
Name:	Plane Position
ShortName:	PLANE_POS_5_C
Power:	PG2
Reset:	soft
Address:	7268Ch-7268Fh
Name:	Plane Position
ShortName:	PLANE_POS_6_C
Power:	PG2
Reset:	soft
Address:	7278Ch-7278Fh
Name:	Plane Position
ShortName:	PLANE_POS_7_C
Power:	PG2
Reset:	soft

PLANE_POS	
Address:	7018Ch-7018Fh
Name:	Plane Position
ShortName:	PLANE_POS_1_A
Power:	PG1
Reset:	soft
Address:	7028Ch-7028Fh
Name:	Plane Position
ShortName:	PLANE_POS_2_A
Power:	PG1
Reset:	soft
Address:	7038Ch-7038Fh
Name:	Plane Position
ShortName:	PLANE_POS_3_A
Power:	PG1
Reset:	soft
Address:	7118Ch-7118Fh
Name:	Plane Position
ShortName:	PLANE_POS_1_B
Power:	PG2
Reset:	soft
Address:	7128Ch-7128Fh
Name:	Plane Position
ShortName:	PLANE_POS_2_B
Power:	PG2
Reset:	soft
Address:	7138Ch-7138Fh
Name:	Plane Position
ShortName:	PLANE_POS_3_B
Power:	PG2
Reset:	soft
Address:	7218Ch-7218Fh
Name:	Plane Position
ShortName:	PLANE_POS_1_C
Power:	PG2
Reset:	soft

PLANE_POS

Address:	7228Ch-7228Fh
Name:	Plane Position
ShortName:	PLANE_POS_2_C
Power:	PG2
Reset:	soft

Address:	7238Ch-7238Fh
Name:	Plane Position
ShortName:	PLANE_POS_3_C
Power:	PG2
Reset:	soft

This register specifies the screen position of the plane. The origin of the plane position is always the upper left corner of the display pipe source image area. When plane scaling is not enabled on this plane, this is the position of the plane when blended with other planes on this pipe. When plane scaling is enabled on this plane, the scaler window position is the position of the plane when blended with other planes on this pipe. When performing rotation, the plane image is rotated by hardware, but the position is not, so it must be adjusted if it is desired to maintain the same apparent position on a physically rotated display.

Restriction

When plane scaling is not enabled on this plane, the plane must be completely contained within the pipe source area. Pipe source size >= plane position + plane size. When plane scaling is enabled on this plane, the X and Y positions must be programmed to 0.

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28:16	**Y Position** This specifies the vertical position of the plane upper left corner in lines.
	15:13	**Reserved** Format: MBZ
	12:0	**X Position** This specifies the horizontal position of the plane upper left corner in pixels.

PLANE_POST_CSC_GAMC_DATA_ENH

PLANE_POST_CSC_GAMC_DATA_ENH	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	701DCh-701DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_1_A
Power:	PG1
Reset:	soft
Address:	702DCh-702DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_2_A
Power:	PG1
Reset:	soft
Address:	703DCh-703DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_3_A
Power:	PG1
Reset:	soft
Address:	711DCh-711DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_1_B
Power:	PG2
Reset:	soft
Address:	712DCh-712DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_2_B

PLANE_POST_CSC_GAMC_DATA_ENH	
Power:	PG2
Reset:	soft
Address:	713DCh-713DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_3_B
Power:	PG2
Reset:	soft
Address:	721DCh-721DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_1_C
Power:	PG2
Reset:	soft
Address:	722DCh-722DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_2_C
Power:	PG2
Reset:	soft
Address:	723DCh-723DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_3_C
Power:	PG2
Reset:	soft

PLANE_POST_CSC_GAMC_INDEX and PLANE_POST_CSC_GAMC_DATA registers are used to program the values that determine the characteristics of the gamma correction for the plane pixel data before Color Space Conversion. Additional gamma correction can be done after the Color Space Conversion, if needed.
The gamma correction curve is represented by specifying a set of gamma entry reference points spaced equally along the curve for values between -1 and 1. For extended values there are extended gamma entry reference points. All input values are clamped to the greater than -7.0 and less than 7.0 range before the gamma calculation.
For input values greater than or equal to 0 and less than 1.0, the input value is used to linearly interpolate between two adjacent points of the first 33 gamma entries to create the result value. The first 32 entries are stored as 24 bits per color in an unsigned 0.24 format with 0 integer and 24 fractional. The 33rd, 34th and 35th entries are stored as27 bits per color in an unsigned 3.24 format with 3 integer and 24 fractional bits.
For input values greater than or equal to 1.0 and less than 3.0, the input value is used to linearly interpolate

PLANE_POST_CSC_GAMC_DATA_ENH

between the 33rd and 34th gamma entries to create the result value.
For input values greater than or equal to 3.0 and less than 7.0, the input value is used to linearly interpolate between the 34th and 35th gamma entries to create the result value.
For negative input values, gamma is mirrored along the X-axis, giving the same result as positive input values, except for a negative sign. When gamma input may be negative, the first gamma point should be programmed to a value of 0.0 in order to have a symmetric mirroring.
Pre-CSC Gamma correction gets enabled or disabled based on the "Pipe CSC Enable" bit in the plane control register. The same set of values is used for gamma correction of the red, blue and green channels.
See Pipe Gamma for an example gamma curve diagram.
To program the gamma correction entries, calculate the desired gamma curve for inputs from 0 to 7.0. For inputs of 0 to 1.0, multiply the input value by 32 to find the gamma entry number, then store the desired gamma result in that entry. For inputs greater than 1.0 and less than or equal to 3.0, store the result for an input of 3.0 in the 34th gamma entry. For inputs greater than 3.0 and less than or equal to 7.0, store the result for an input of 7.0 in the 35th gamma entry.
For HDR tone mapping usages, only the first 33 entries gets used. The entries are used either in an unsigned 0.24 format or unsigned 8.16 format based on PLANE_COLOR_CTL->Plane Gamma Multiplier Precision programming.

Restriction
The gamma curve must be flat or increasing, never decreasing when used in the direct lookup mode. The gamma correction registers should only be updated when the plane is off, otherwise screen artifacts may show temporarily.

DWord	Bit	Description
0	31:27	**Reserved** Format: MBZ
	26:0	**Gamma Value** Default Value: 00000000000000000000000000b Format: U3.24

PLANE_POST_CSC_GAMC_DATA

PLANE_POST_CSC_GAMC_DATA	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed
Double Buffer Armed By:	Write to PLANE_SURF or plane not enabled
Address:	704DCh-704DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_4_A
Power:	PG1
Reset:	soft
Address:	705DCh-705DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_5_A
Power:	PG1
Reset:	soft
Address:	706DCh-706DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_6_A
Power:	PG1
Reset:	soft
Address:	707DCh-707DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_7_A
Power:	PG1
Reset:	soft
Address:	714DCh-714DFh

PLANE_POST_CSC_GAMC_DATA	
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_4_B
Power:	PG2
Reset:	soft
Address:	715DCh-715DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_5_B
Power:	PG2
Reset:	soft
Address:	716DCh-716DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_6_B
Power:	PG2
Reset:	soft
Address:	717DCh-717DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_7_B
Power:	PG2
Reset:	soft
Address:	724DCh-724DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_4_C
Power:	PG2
Reset:	soft
Address:	725DCh-725DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_5_C
Power:	PG2
Reset:	soft
Address:	726DCh-726DFh

PLANE_POST_CSC_GAMC_DATA

Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_6_C
Power:	PG2
Reset:	soft

Address:	727DCh-727DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_7_C
Power:	PG2
Reset:	soft

PLANE_POST_CSC_GAMC_INDEX and PLANE_POST_CSC_GAMC_DATA registers are used to program the values that determine the characteristics of the gamma correction for the plane pixel data after plane Color Space Conversion.
The gamma correction curve is represented by specifying a set of gamma entry reference points spaced equally along the curve for values between -1 and 1. For extended values there are extended gamma entry reference points. All input values are clamped to the greater than -7.0 and less than 7.0 range before the gamma calculation.
For input values greater than or equal to 0 and less than 1.0, the input value is used to linearly interpolate between two adjacent points of the first 33 gamma entries to create the result value. The first 32 entries are stored as 16 bits per color in an unsigned 0.16 format with 0 integer and16 fractional. The 33rd, 34th and 35th entries are stored as19 bits per color in an unsigned 3.16 format with 3 integer and16 fractional bits.
For input values greater than or equal to 1.0 and less than 3.0, the input value is used to linearly interpolate between the 33rd and 34th gamma entries to create the result value.
For input values greater than or equal to 3.0 and less than 7.0, the input value is used to linearly interpolate between the 34th and 35th gamma entries to create the result value.
For negative input values, gamma is mirrored along the X-axis, giving the same result as positive input values, except for a negative sign. When gamma input may be negative, the first gamma point should be programmed to a value of 0.0 in order to have a symmetric mirroring.
Plane Post-CSC Gamma correction gets enabled or disabled based on the 'Plane Gamma Disable' bit in the 'PLANE_COLOR_CTL' register. The same set of values is used for gamma correction of the red, blue and green channels.

Programming Notes

To program the gamma correction entries, calculate the desired gamma curve for inputs from 0 to 7.0. For inputs of 0 to 1.0, multiply the input value by 32 to find the gamma entry number, then store the desired gamma result in that entry. For inputs greater than 1.0 and less than or equal to 3.0, store the result for an input of 3.0 in the 34th gamma entry. For inputs greater than 3.0 and less than or equal to 7.0, store the result for an input of 7.0 in the 35th gamma entry.

Restriction

The gamma curve must be flat or increasing, never decreasing in Direct mode. The gamma correction registers

PLANE_POST_CSC_GAMC_DATA

should only be updated when the plane is off, otherwise screen artifacts may show temporarily.

DWord	Bit	Description
0	31:19	**Reserved** Format: MBZ
	18:0	**Gamma Value** Default Value: 0000000000000000000b Format: U3.16

PLANE_POST_CSC_GAMC_INDEX_ENH

PLANE_POST_CSC_GAMC_INDEX_ENH	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	701D8h-701DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_1_A
Power:	PG1
Reset:	soft
Address:	702D8h-702DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_2_A
Power:	PG1
Reset:	soft
Address:	703D8h-703DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_3_A
Power:	PG1
Reset:	soft
Address:	711D8h-711DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_1_B
Power:	PG2
Reset:	soft
Address:	712D8h-712DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_2_B

PLANE_POST_CSC_GAMC_INDEX_ENH

Power:	PG2
Reset:	soft

Address:	713D8h-713DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_3_B
Power:	PG2
Reset:	soft

Address:	721D8h-721DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_1_C
Power:	PG2
Reset:	soft

Address:	722D8h-722DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_2_C
Power:	PG2
Reset:	soft

Address:	723D8h-723DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_3_C
Power:	PG2
Reset:	soft

<table>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td rowspan="3">0</td><td>31:11</td><td>Reserved
Format: MBZ</td></tr>
<tr><td>10</td><td>Index Auto Increment
This field enables the index auto increment.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th></tr>
<tr><td>0b</td><td>No Increment</td><td>Do not automatically increment the index value.</td></tr>
<tr><td>1b</td><td>Auto Increment
[Default]</td><td>Increment the index value with each read or write to the data register.</td></tr>
</table></td></tr>
<tr><td>9:6</td><td>Reserved</td></tr>
</table>

PLANE_POST_CSC_GAMC_INDEX_ENH

		Format: MBZ
	5:0	**Index Value** Access: Write/Read Status This index controls access to the array of plane pre color space conversion gamma values. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set. When automatically incrementing, the current automatically calculated index value can be read here, and the index will roll over to 0 after reaching the end of the allowed range. While in auto increment mode, after performing reads or writes to only part of the range, the auto increment bit must be cleared before resetting the index value. **Value** / **Name** [0,34]

PLANE_POST_CSC_GAMC_INDEX

PLANE_POST_CSC_GAMC_INDEX	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed
Double Buffer Armed By:	Write to PLANE_SURF or plane not enabled
Address:	704D8h-704DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_4_A
Power:	PG1
Reset:	soft
Address:	705D8h-705DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_5_A
Power:	PG1
Reset:	soft
Address:	706D8h-706DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_6_A
Power:	PG1
Reset:	soft
Address:	707D8h-707DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_7_A
Power:	PG1
Reset:	soft
Address:	714D8h-714DBh

PLANE_POST_CSC_GAMC_INDEX	
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_4_B
Power:	PG2
Reset:	soft
Address:	715D8h-715DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_5_B
Power:	PG2
Reset:	soft
Address:	716D8h-716DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_6_B
Power:	PG2
Reset:	soft
Address:	717D8h-717DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_7_B
Power:	PG2
Reset:	soft
Address:	724D8h-724DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_4_C
Power:	PG2
Reset:	soft
Address:	725D8h-725DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_5_C
Power:	PG2
Reset:	soft
Address:	726D8h-726DBh

PLANE_POST_CSC_GAMC_INDEX

Name: Plane Post CSC Gamma Index
ShortName: PLANE_POST_CSC_GAMC_INDEX_6_C

Power: PG2
Reset: soft

Address: 727D8h-727DBh
Name: Plane Post CSC Gamma Index
ShortName: PLANE_POST_CSC_GAMC_INDEX_7_C

Power: PG2
Reset: soft

DWord	Bit	Description
0	31:11	**Reserved** Format: MBZ
	10	**Index Auto Increment** This field enables the index auto increment. Value / Name / Description: 0b / No Increment / Do not automatically increment the index value. 1b / Auto Increment **[Default]** / Increment the index value with each read or write to the data register.
	9:6	**Reserved** Format: MBZ
	5:0	**Index Value** Access: Write/Read Status This index controls access to the array of plane pre color space conversion gamma values. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set. When automatically incrementing, the index will roll over to 0 after writing or reading the entire allowed range. While in auto increment mode, after performing reads or writes to only part of the range, the auto increment bit must be cleared before resetting the index value. Value / Name: [0,34] /

PLANE_PRE_CSC_GAMC_DATA_ENH

PLANE_PRE_CSC_GAMC_DATA_ENH	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Address:	701D4h-701D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_1_A
Power:	PG1
Reset:	soft
Address:	702D4h-702D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_2_A
Power:	PG1
Reset:	soft
Address:	703D4h-703D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_3_A
Power:	PG1
Reset:	soft
Address:	711D4h-711D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_1_B
Power:	PG2
Reset:	soft
Address:	712D4h-712D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_2_B

PLANE_PRE_CSC_GAMC_DATA_ENH

Power:	PG2
Reset:	soft
Address:	713D4h-713D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_3_B
Power:	PG2
Reset:	soft
Address:	721D4h-721D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_1_C
Power:	PG2
Reset:	soft
Address:	722D4h-722D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_2_C
Power:	PG2
Reset:	soft
Address:	723D4h-723D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_3_C
Power:	PG2
Reset:	soft

PLANE_PRE_CSC_GAMC_INDEX and PLANE_PRE_CSC_GAMC_DATA registers are used to program the values that determine the characteristics of the gamma correction for the plane pixel data before Color Space Conversion. Additional gamma correction can be done after the Color Space Conversion, if needed.

The gamma correction curve is represented by specifying a set of gamma entry reference points spaced equally along the curve for values between -1 and 1. For extended values there are extended gamma entry reference points. All input values are clamped to the greater than -7.0 and less than 7.0 range before the gamma calculation.

For input values greater than or equal to 0 and less than 1.0, the input value is used to linearly interpolate between two adjacent points of the first 129 gamma entries to create the result value. The first 128 entries are stored as 24 bits per color in an unsigned 0.24 format with 0 integer and 24 fractional. The 129th, 130th and 131th entries are stored as 27 bits per color in an unsigned 3.24 format with 3 integer and 24 fractional bits.

For input values greater than or equal to 1.0 and less than 3.0, the input value is used to linearly interpolate

PLANE_PRE_CSC_GAMC_DATA_ENH

between the 129th and 130th gamma entries to create the result value.
For input values greater than or equal to 3.0 and less than 7.0, the input value is used to linearly interpolate between the 130th and 131st gamma entries to create the result value.
For negative input values, gamma is mirrored along the X-axis, giving the same result as positive input values, except for a negative sign. When gamma input may be negative, the first gamma point should be programmed to a value of 0.0 in order to have a symmetric mirroring.
Pre-CSC Gamma correction gets enabled or disabled based on the "Plane Pre CSC Gamma Enable" bit in the plane color control register. The same set of values is used for gamma correction of the red, blue and green channels.
See Pipe Gamma for an example gamma curve diagram.

Programming Notes

To program the gamma correction entries, calculate the desired gamma curve for inputs from 0 to 7.0. For inputs of 0 to 1.0, multiply the input value by 128 to find the gamma entry number, then store the desired gamma result in that entry. For inputs greater than 1.0 and less than or equal to 3.0, store the result for an input of 3.0 in the 129th gamma entry. For inputs greater than 3.0 and less than or equal to 7.0, store the result for an input of 7.0 in the 130th gamma entry.

Restriction

The gamma curve must be flat or increasing, never decreasing. The gamma correction registers should only be updated when the plane is off, otherwise screen artifacts may show temporarily.

DWord	Bit	Description
0	31:27	**Reserved** Format: MBZ
	26:0	**Gamma Value** Default Value: 00000000000000000000000000b Format: U3.24

PLANE_PRE_CSC_GAMC_DATA

PLANE_PRE_CSC_GAMC_DATA	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed
Double Buffer Armed By:	Write to PLANE_SURF or plane not enabled
Address:	704D4h-704D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_4_A
Power:	PG1
Reset:	soft
Address:	705D4h-705D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_5_A
Power:	PG1
Reset:	soft
Address:	706D4h-706D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_6_A
Power:	PG1
Reset:	soft
Address:	707D4h-707D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_7_A
Power:	PG1
Reset:	soft
Address:	714D4h-714D7h

PLANE_PRE_CSC_GAMC_DATA	
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_4_B
Power:	PG2
Reset:	soft
Address:	715D4h-715D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_5_B
Power:	PG2
Reset:	soft
Address:	716D4h-716D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_6_B
Power:	PG2
Reset:	soft
Address:	717D4h-717D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_7_B
Power:	PG2
Reset:	soft
Address:	724D4h-724D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_4_C
Power:	PG2
Reset:	soft
Address:	725D4h-725D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_5_C
Power:	PG2
Reset:	soft
Address:	726D4h-726D7h

PLANE_PRE_CSC_GAMC_DATA

Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_6_C
Power:	PG2
Reset:	soft

Address:	727D4h-727D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_7_C
Power:	PG2
Reset:	soft

PLANE_PRE_CSC_GAMC_INDEX and PLANE_PRE_CSC_GAMC_DATA registers are used to program the values that determine the characteristics of the gamma correction for the plane pixel data before Color Space Conversion. Additional gamma correction can be done after the Color Space Conversion, if needed.
The gamma correction curve is represented by specifying a set of gamma entry reference points spaced equally along the curve for values between -1 and 1. For extended values there are extended gamma entry reference points. All input values are clamped to the greater than -7.0 and less than 7.0 range before the gamma calculation.
For input values greater than or equal to 0 and less than 1.0, the input value is used to linearly interpolate between two adjacent points of the first 33 gamma entries to create the result value. The first 32 entries are stored as16 bits per color in an unsigned 0.16 format with 0 integer and 16 fractional. The 33rd, 34th and 35th entries are stored as 19 bits per color in an unsigned 3.16 format with 3 integer and 16 fractional bits.
For input values greater than or equal to 1.0 and less than 3.0, the input value is used to linearly interpolate between the 33rd and 34th gamma entries to create the result value.
For input values greater than or equal to 3.0 and less than 7.0, the input value is used to linearly interpolate between the 34th and 35th gamma entries to create the result value.
For negative input values, gamma is mirrored along the X-axis, giving the same result as positive input values, except for a negative sign. When gamma input may be negative, the first gamma point should be programmed to a value of 0.0 in order to have a symmetric mirroring.
Plane Pre-CSC Gamma correction gets enabled or disabled based on the 'Plane Pre CSC Gamma Enable'bit in the 'PLANE_COLOR_CTL'register. The same set of values is used for gamma correction of the red, blue and green channels.

Programming Notes

To program the gamma correction entries, calculate the desired gamma curve for inputs from 0 to 7.0. For inputs of 0 to 1.0, multiply the input value by 32 to find the gamma entry number, then store the desired gamma result in that entry. For inputs greater than 1.0 and less than or equal to 3.0, store the result for an input of 3.0 in the 34th gamma entry. For inputs greater than 3.0 and less than or equal to 7.0, store the result for an input of 7.0 in the 35th gamma entry.

Restriction

The gamma curve must be flat or increasing, never decreasing. The gamma correction registers should only be

PLANE_PRE_CSC_GAMC_DATA

updated when the plane is off, otherwise screen artifacts may show temporarily.

DWord	Bit	Description
0	31:19	**Reserved** Format: MBZ
	18:0	**Gamma Value** Default Value: 00000000000000000b Format: U3.16

PLANE_PRE_CSC_GAMC_INDEX_ENH

PLANE_PRE_CSC_GAMC_INDEX_ENH	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Address:	701D0h-701D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_1_A
Power:	PG1
Reset:	soft
Address:	702D0h-702D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_2_A
Power:	PG1
Reset:	soft
Address:	703D0h-703D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_3_A
Power:	PG1
Reset:	soft
Address:	711D0h-711D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_1_B
Power:	PG2
Reset:	soft
Address:	712D0h-712D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_2_B

PLANE_PRE_CSC_GAMC_INDEX_ENH

Power: PG2
Reset: soft

Address: 713D0h-713D3h
Name: Plane Pre CSC Gamma Index
ShortName: PLANE_PRE_CSC_GAMC_INDEX_ENH_3_B

Power: PG2
Reset: soft

Address: 721D0h-721D3h
Name: Plane Pre CSC Gamma Index
ShortName: PLANE_PRE_CSC_GAMC_INDEX_ENH_1_C

Power: PG2
Reset: soft

Address: 722D0h-722D3h
Name: Plane Pre CSC Gamma Index
ShortName: PLANE_PRE_CSC_GAMC_INDEX_ENH_2_C

Power: PG2
Reset: soft

Address: 723D0h-723D3h
Name: Plane Pre CSC Gamma Index
ShortName: PLANE_PRE_CSC_GAMC_INDEX_ENH_3_C

Power: PG2
Reset: soft

DWord	Bit	Description
0	31:11	**Reserved** Format: MBZ
	10	**Index Auto Increment** This field enables the index auto increment. 0b – No Increment – Do not automatically increment the index value. 1b – Auto Increment **[Default]** – Increment the index value with each read or write to the data register.
	9:8	**Reserved**

PLANE_PRE_CSC_GAMC_INDEX_ENH

		Format:	MBZ
	7:0	**Index Value** Access: Write/Read Status This index controls access to the array of plane pre color space conversion gamma values. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set. When automatically incrementing, the index will roll over to 0 after writing or reading the entire allowed range. While in auto increment mode, after performing reads or writes to only part of the range, the auto increment bit must be cleared before resetting the index value. **Value**: [0,130] **Name**:

PLANE_PRE_CSC_GAMC_INDEX

PLANE_PRE_CSC_GAMC_INDEX	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed
Double Buffer Armed By:	Write to PLANE_SURF or plane not enabled
Address:	704D0h-704D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_4_A
Power:	PG1
Reset:	soft
Address:	705D0h-705D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_5_A
Power:	PG1
Reset:	soft
Address:	706D0h-706D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_6_A
Power:	PG1
Reset:	soft
Address:	707D0h-707D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_7_A
Power:	PG1
Reset:	soft
Address:	714D0h-714D3h

PLANE_PRE_CSC_GAMC_INDEX	
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_4_B
Power:	PG2
Reset:	soft
Address:	715D0h-715D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_5_B
Power:	PG2
Reset:	soft
Address:	716D0h-716D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_6_B
Power:	PG2
Reset:	soft
Address:	717D0h-717D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_7_B
Power:	PG2
Reset:	soft
Address:	724D0h-724D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_4_C
Power:	PG2
Reset:	soft
Address:	725D0h-725D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_5_C
Power:	PG2
Reset:	soft
Address:	726D0h-726D3h

PLANE_PRE_CSC_GAMC_INDEX

Name: Plane Pre CSC Gamma Index
ShortName: PLANE_PRE_CSC_GAMC_INDEX_6_C

Power: PG2
Reset: soft

Address: 727D0h-727D3h
Name: Plane Pre CSC Gamma Index
ShortName: PLANE_PRE_CSC_GAMC_INDEX_7_C

Power: PG2
Reset: soft

DWord	Bit	Description
0	31:11	**Reserved** Format: MBZ
	10	**Index Auto Increment** This field enables the index auto increment. 0b – No Increment – Do not automatically increment the index value. 1b – Auto Increment **[Default]** – Increment the index value with each read or write to the data register.
	9:6	**Reserved** Format: MBZ
	5:0	**Index Value** Access: Write/Read Status This index controls access to the array of plane pre color space conversion gamma values. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set. When automatically incrementing, the index will roll over to 0 after writing or reading the entire allowed range. While in auto increment mode, after performing reads or writes to only part of the range, the auto increment bit must be cleared before resetting the index value. Value: [0,34]

PLANE_SIZE

PLANE_SIZE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed
Double Buffer Armed By:	Write to PLANE_SURF or plane not enabled
Address:	70490h-70493h
Name:	Plane Size
ShortName:	PLANE_SIZE_4_A
Power:	PG1
Reset:	soft
Address:	70590h-70593h
Name:	Plane Size
ShortName:	PLANE_SIZE_5_A
Power:	PG1
Reset:	soft
Address:	70690h-70693h
Name:	Plane Size
ShortName:	PLANE_SIZE_6_A
Power:	PG1
Reset:	soft
Address:	70790h-70793h
Name:	Plane Size
ShortName:	PLANE_SIZE_7_A
Power:	PG1
Reset:	soft
Address:	71490h-71493h
Name:	Plane Size
ShortName:	PLANE_SIZE_4_B
Power:	PG2
Reset:	soft

PLANE_SIZE	
Address:	71590h-71593h
Name:	Plane Size
ShortName:	PLANE_SIZE_5_B
Power:	PG2
Reset:	soft
Address:	71690h-71693h
Name:	Plane Size
ShortName:	PLANE_SIZE_6_B
Power:	PG2
Reset:	soft
Address:	71790h-71793h
Name:	Plane Size
ShortName:	PLANE_SIZE_7_B
Power:	PG2
Reset:	soft
Address:	72490h-72493h
Name:	Plane Size
ShortName:	PLANE_SIZE_4_C
Power:	PG2
Reset:	soft
Address:	72590h-72593h
Name:	Plane Size
ShortName:	PLANE_SIZE_5_C
Power:	PG2
Reset:	soft
Address:	72690h-72693h
Name:	Plane Size
ShortName:	PLANE_SIZE_6_C
Power:	PG2
Reset:	soft
Address:	72790h-72793h
Name:	Plane Size
ShortName:	PLANE_SIZE_7_C
Power:	PG2
Reset:	soft

PLANE_SIZE	
Address:	70190h-70193h
Name:	Plane Size
ShortName:	PLANE_SIZE_1_A
Power:	PG1
Reset:	soft
Address:	70290h-70293h
Name:	Plane Size
ShortName:	PLANE_SIZE_2_A
Power:	PG1
Reset:	soft
Address:	70390h-70393h
Name:	Plane Size
ShortName:	PLANE_SIZE_3_A
Power:	PG1
Reset:	soft
Address:	71190h-71193h
Name:	Plane Size
ShortName:	PLANE_SIZE_1_B
Power:	PG2
Reset:	soft
Address:	71290h-71293h
Name:	Plane Size
ShortName:	PLANE_SIZE_2_B
Power:	PG2
Reset:	soft
Address:	71390h-71393h
Name:	Plane Size
ShortName:	PLANE_SIZE_3_B
Power:	PG2
Reset:	soft
Address:	72190h-72193h
Name:	Plane Size
ShortName:	PLANE_SIZE_1_C
Power:	PG2
Reset:	soft

PLANE_SIZE

Address:	72290h-72293h
Name:	Plane Size
ShortName:	PLANE_SIZE_2_C
Power:	PG2
Reset:	soft

Address:	72390h-72393h
Name:	Plane Size
ShortName:	PLANE_SIZE_3_C
Power:	PG2
Reset:	soft

This register specifies the plane source size, the size of the image fetched from the frame buffer. When plane scaling is not enabled on this plane, this is the size of the plane when blended with other planes on this pipe. When plane scaling is enabled on this plane, the scaler window size is the size of the plane when blended with other planes on this pipe.

Restriction

When plane scaling is not enabled on this plane, the plane must be completely contained within the pipe source area. Pipe source size >= plane position + plane size.

For OLED compensation plane size restrictions, refer to PIPE_MISC->OLED Compensation (bit[12]).

Height and Width restrictions are specified in the following table. For formats not specified in the table, both odd and even sizes are supported.

PixelFormat	Rotate	Width	Height
YUV 420 Planar - NV12	All	Even	Even
YUV 420 Planar - P01x	All	Even	Even
YUV 422	All	Even	Even
RGB565	90, 270	Even	Even

If Plane Scaling or using the Chroma Up-Sampler (CUS) for this plane, please refer to**PS_CTRL**or**PLANE_CUS_CTL**respectively, for further size restrictions.

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28:16	**Height** This specifies the height of the plane in lines. The value in the register is the height minus one. **Restriction** The height must be at least one line when non-interlaced, two lines when interlaced. The

PLANE_SIZE

		height is limited to maximum of 4320 lines. Refer to size restrictions within PS_CTRL when plane scaling is enabled.
	15:13	**Reserved** Format: MBZ
	12:0	**Width** This specifies the width of the plane in pixels. The value in the register is the width minus one. **Restriction** The width must be even (programmed value odd) when YUV 4:2:2 or YUV 4:2:0 source pixel format is used. The width must not be 0. The width should be less than or equal to the stride in pixels. For YUV4:2:0(NV12), the UV plane must be greater than or equal to 8 and the Y plane must be greater than or equal to 16. The width must be greater than or equal to4 for 32bpp formats, greater than or equal to 8 for 16bpp formats, and greater than or equal to 16 for 8bpp formats. The width must be greater than or equal to 2 for 64bpp formats. The width should be less than or equal to the stride in pixels. For planar YUV 420 formats, refer to chroma upsampler size restrictions in PLANE_CUS_CTL register.

Tiling format	Bytes per pixel	Max Width supported in pixels
Linear, X Tiling	1,2,4,8	5120
Y Tiling	1,2,4,8	5120
Yf Tiling	8	Not supported
	1,2,4	5120

PLANE_STRIDE

PLANE_STRIDE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed
Double Buffer Armed By:	Write to PLANE_SURF or plane not enabled
Address:	70488h-7048Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_4_A
Power:	PG1
Reset:	soft
Address:	70588h-7058Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_5_A
Power:	PG1
Reset:	soft
Address:	70688h-7068Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_6_A
Power:	PG1
Reset:	soft
Address:	70788h-7078Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_7_A
Power:	PG1
Reset:	soft
Address:	71488h-7148Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_4_B
Power:	PG2
Reset:	soft

PLANE_STRIDE	
Address:	71588h-7158Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_5_B
Power:	PG2
Reset:	soft
Address:	71688h-7168Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_6_B
Power:	PG2
Reset:	soft
Address:	71788h-7178Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_7_B
Power:	PG2
Reset:	soft
Address:	72488h-7248Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_4_C
Power:	PG2
Reset:	soft
Address:	72588h-7258Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_5_C
Power:	PG2
Reset:	soft
Address:	72688h-7268Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_6_C
Power:	PG2
Reset:	soft
Address:	72788h-7278Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_7_C
Power:	PG2
Reset:	soft

PLANE_STRIDE	
Address:	70188h-7018Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_1_A
Power:	PG1
Reset:	soft
Address:	70288h-7028Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_2_A
Power:	PG1
Reset:	soft
Address:	70388h-7038Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_3_A
Power:	PG1
Reset:	soft
Address:	71188h-7118Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_1_B
Power:	PG2
Reset:	soft
Address:	71288h-7128Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_2_B
Power:	PG2
Reset:	soft
Address:	71388h-7138Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_3_B
Power:	PG2
Reset:	soft
Address:	72188h-7218Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_1_C
Power:	PG2
Reset:	soft

PLANE_STRIDE

Address:	72288h-7228Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_2_C
Power:	PG2
Reset:	soft

Address:	72388h-7238Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_3_C
Power:	PG2
Reset:	soft

This register may be updated through MMIO writes or through command streamer initiated synchronous flips.

DWord	Bit	Description
0	31:10	**Reserved**
	9:0	**Stride** This field specifies the stride for the plane. The field is used to determine the line to line increment for the plane. For Linear memory, this field specifies the stride in chunks of 64 bytes (1 cache line). If the programmed value is 100, the actual stride = 100 * 64 = 6400 bytes. For X-Tiled & Y-Tiled memory, this field specifies the stride in number of tiles. For Tile X, if the programmed value is 10, the actual stride = 10 * 512 (X tile width) = 5120 bytes. For Tile Y legacy, if the programmed value is 10, the actual stride = 10 * 128 (Y tile width) = 1280 bytes.

Tile Format	Width in bytes
Tile X	512
Tile Y (legacy)	128
Tile YF (8 bpp)	64
Tile YF (16 bpp, 32 bpp, 64 bpp)	128

Restriction

For YUV planar (NV12 or P0xx) plane pixel formats, the stride calculated in bytes should be equal for the Y and UV surfaces. In Tile Yf format, the stride value programmed for YUV planar - Y surface should be an even number of tiles in the non-rotate mode.
The stride in bytes must not exceed the of the size of 8K pixels.

Tile Format	Pixel Format	Maximum Stride in tiles	Render Decompression Maximum Auxiliary surface stride in tiles
Linear	64 bpp pixel format	1023	NA

PLANE_STRIDE				
			32 bpp pixel format	512	NA
			16 bpp pixel format	256	NA
			8 bpp pixel format	128	NA
		X Tiling	64 bpp pixel format	128	NA
			32 bpp pixel format	64	NA
			16 bpp pixel format	32	NA
			8 bpp pixel format	16	NA
		Y Tiling (Legacy)	64 bpp pixel format	512	NA
			32 bpp pixel format	256	8
			16 bpp pixel format	128	NA
			8 bpp pixel format	64	NA
		YF Tiling	32 bpp pixel format	256	8
			16 bpp Pixel format	128	NA
			8 bpp pixel format	128	NA

PLANE_SURF

PLANE_SURF	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of left or right eye vertical blank (selectable), pipe not enabled, or plane not enabled
Address:	7049Ch-7049Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_4_A
Power:	PG1
Reset:	soft
Address:	7059Ch-7059Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_5_A
Power:	PG1
Reset:	soft
Address:	7069Ch-7069Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_6_A
Power:	PG1
Reset:	soft
Address:	7079Ch-7079Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_7_A
Power:	PG1
Reset:	soft
Address:	7149Ch-7149Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_4_B
Power:	PG2
Reset:	soft
Address:	7159Ch-7159Fh

PLANE_SURF	
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_5_B
Power:	PG2
Reset:	soft
Address:	7169Ch-7169Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_6_B
Power:	PG2
Reset:	soft
Address:	7179Ch-7179Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_7_B
Power:	PG2
Reset:	soft
Address:	7249Ch-7249Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_4_C
Power:	PG2
Reset:	soft
Address:	7259Ch-7259Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_5_C
Power:	PG2
Reset:	soft
Address:	7269Ch-7269Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_6_C
Power:	PG2
Reset:	soft
Address:	7279Ch-7279Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_7_C
Power:	PG2
Reset:	soft
Address:	7019Ch-7019Fh

PLANE_SURF	
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_1_A
Power:	PG1
Reset:	soft
Address:	7029Ch-7029Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_2_A
Power:	PG1
Reset:	soft
Address:	7039Ch-7039Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_3_A
Power:	PG1
Reset:	soft
Address:	7119Ch-7119Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_1_B
Power:	PG2
Reset:	soft
Address:	7129Ch-7129Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_2_B
Power:	PG2
Reset:	soft
Address:	7139Ch-7139Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_3_B
Power:	PG2
Reset:	soft
Address:	7219Ch-7219Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_1_C
Power:	PG2
Reset:	soft
Address:	7229Ch-7229Fh

PLANE_SURF

Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_2_C
Power:	PG2
Reset:	soft

Address:	7239Ch-7239Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_3_C
Power:	PG2
Reset:	soft

Writes to this register arm primary registers for this pipe. A write to this register is considered a flip and can cause a flip done interrupt if the interrupt registers are configured for that. The values in this register may be updated through MMIO writes or through command streamer initiated flips. Synchronous updates (synchronous command streamer flips or synchronous MMIO writes) will update the plane surface values at the start of the next vertical blank. Asynchronous updates (asynchronous command streamer flips or asynchronous MMIO writes) will update the plane surface values at the next TLB request or at the start of the next vertical blank. Stereo 3D synchronous updates (stereo 3D command streamer flips or synchronous MMIO writes while stereo 3D is enabled) will update at the start of either the left or right eye vertical blank, selectable by the plane control register stereo surface vblank mask.
Double buffering control does not apply to PLANE_SURF updates that occur when the plane is disabled. An interrupt event is generated immediately when the PLANE_SURF is written. If the interrupt is unmasked, the interrupt is logged in the IIR.

Asynchronous flip completion time depends greatly on how much data has been prefetched for power savings, and can take up to 1 full frame to complete. For faster flip completion, disable FBC and render compression and allocate a small amount of data buffer for the plane.

DWord	Bit	Description
0	31:12	**Surface Base Address** Format: GraphicsAddress[31:12] This address specifies the surface base address bits 31:12. In stereo 3D mode this is the right eye base address. In non-stereo 3D mode this is the only base address. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. **Restriction** The surface base address must be at least 256KB aligned in the Linear or X-tiling modes and must be at least 1MB aligned in the Y-tiling mode. With planar YUV 420 formats, the alignment restrictions apply only for the Y surface. Allocate either an extra 168 Page Table Entries (PTEs) or tile row worth of PTEs beyond the end of the displayed surface. If 180 or 270 plane rotation capability is required, allocate an extra 168 PTEs or a tile row worth of PTEs before the beginning of the surface. When address range limits are reached, wrap around to finish allocating the extra PTEs. Only the PTEs will be used, not the pages themselves. The graphics address of the next usable surface must start after the padding. All the extra entries shall map to the same dummy page.
	11	**Reserved**

	10	**Reserved**
	9	**Reserved**
	8:7	**Reserved**
	6:4	**Reserved**
	3	**Ring Flip Source** This bit indicates if the source of the last ring flip was CS or BCS. This will determine where the flip done response is sent. **Value** / **Name** 0b / CS 1b / BCS
	2	**Reserved**
	1:0	**Reserved**

PLANE_SURFLIVE

PLANE_SURFLIVE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	704ACh-704AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_4_A
Power:	PG1
Reset:	soft
Address:	704BCh-704BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_4_A
Power:	PG1
Reset:	soft
Address:	705ACh-705AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_5_A
Power:	PG1
Reset:	soft
Address:	705BCh-705BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_5_A
Power:	PG1
Reset:	soft
Address:	706ACh-706AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_6_A
Power:	PG1
Reset:	soft
Address:	706BCh-706BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_6_A
Power:	PG1

PLANE_SURFLIVE	
Reset:	soft
Address:	707ACh-707AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_7_A
Power:	PG1
Reset:	soft
Address:	707BCh-707BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_7_A
Power:	PG1
Reset:	soft
Address:	714ACh-714AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_4_B
Power:	PG2
Reset:	soft
Address:	714BCh-714BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_4_B
Power:	PG2
Reset:	soft
Address:	715ACh-715AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_5_B
Power:	PG2
Reset:	soft
Address:	715BCh-715BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_5_B
Power:	PG2
Reset:	soft
Address:	716ACh-716AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_6_B
Power:	PG2

PLANE_SURFLIVE	
Reset:	soft
Address:	716BCh-716BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_6_B
Power:	PG2
Reset:	soft
Address:	717ACh-717AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_7_B
Power:	PG2
Reset:	soft
Address:	717BCh-717BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_7_B
Power:	PG2
Reset:	soft
Address:	724ACh-724AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_4_C
Power:	PG2
Reset:	soft
Address:	724BCh-724BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_4_C
Power:	PG2
Reset:	soft
Address:	725ACh-725AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_5_C
Power:	PG2
Reset:	soft
Address:	725BCh-725BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_5_C
Power:	PG2

PLANE_SURFLIVE	
Reset:	soft
Address:	726ACh-726AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_6_C
Power:	PG2
Reset:	soft
Address:	726BCh-726BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_6_C
Power:	PG2
Reset:	soft
Address:	727ACh-727AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_7_C
Power:	PG2
Reset:	soft
Address:	727BCh-727BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_7_C
Power:	PG2
Reset:	soft
Address:	701ACh-701AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_1_A
Power:	PG1
Reset:	soft
Address:	701BCh-701BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_1_A
Power:	PG1
Reset:	soft
Address:	702ACh-702AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_2_A
Power:	PG1

PLANE_SURFLIVE	
Reset:	soft
Address:	702BCh-702BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_2_A
Power:	PG1
Reset:	soft
Address:	703ACh-703AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_3_A
Power:	PG1
Reset:	soft
Address:	703BCh-703BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_3_A
Power:	PG1
Reset:	soft
Address:	711ACh-711AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_1_B
Power:	PG2
Reset:	soft
Address:	711BCh-711BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_1_B
Power:	PG2
Reset:	soft
Address:	712ACh-712AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_2_B
Power:	PG2
Reset:	soft
Address:	712BCh-712BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_2_B
Power:	PG2

PLANE_SURFLIVE	
Reset:	soft
Address:	713ACh-713AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_3_B
Power:	PG2
Reset:	soft
Address:	713BCh-713BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_3_B
Power:	PG2
Reset:	soft
Address:	721ACh-721AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_1_C
Power:	PG2
Reset:	soft
Address:	721BCh-721BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_1_C
Power:	PG2
Reset:	soft
Address:	722ACh-722AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_2_C
Power:	PG2
Reset:	soft
Address:	722BCh-722BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_2_C
Power:	PG2
Reset:	soft
Address:	723ACh-723AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_3_C
Power:	PG2

PLANE_SURFLIVE

Reset:	soft
Address:	723BCh-723BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_3_C
Power:	PG2
Reset:	soft

There is one instance of this register for each plane.

DWord	Bit	Description
0	31:12	**Live Surface Base Address** Access: RO This gives the live value of the surface base address as being currently used for the plane.
	11	**Reserved** Format: MBZ
	10:9	**Reserved**
	8:6	**Reserved**
	5	**Reserved**
	4	**Reserved**
	3:0	**Reserved** Format: MBZ

PLANE_WM

PLANE_WM	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank, plane not enabled, or pipe not enabled
Double Buffer Armed By:	Write to PLANE_SURF/CUR_BASE or plane/cursor not enabled
Address:	70140h-7015Fh
Name:	Cursor A Watermarks
ShortName:	CUR_WM_A_*
Power:	PG1
Reset:	soft
Address:	71140h-7115Fh
Name:	Cursor B Watermarks
ShortName:	CUR_WM_B_*
Power:	PG2
Reset:	soft
Address:	72140h-7215Fh
Name:	Cursor C Watermarks
ShortName:	CUR_WM_C_*
Power:	PG2
Reset:	soft
Address:	70168h-7016Bh
Name:	Cursor Transition Watermarks
ShortName:	CUR_WM_TRANS_A
Power:	PG1
Reset:	soft
Address:	71168h-7116Bh
Name:	Cursor Transition Watermarks

PLANE_WM	
ShortName:	CUR_WM_TRANS_B
Power:	PG2
Reset:	soft
Address:	72168h-7216Bh
Name:	Cursor Transition Watermarks
ShortName:	CUR_WM_TRANS_C
Power:	PG2
Reset:	soft
Address:	70540h-70543h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_4_A
Power:	PG1
Reset:	soft
Address:	70544h-70547h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_4_A
Power:	PG1
Reset:	soft
Address:	70548h-7054Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_4_A
Power:	PG1
Reset:	soft
Address:	7054Ch-7054Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_4_A
Power:	PG1
Reset:	soft
Address:	70550h-70553h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_4_A

PLANE_WM	
Power:	PG1
Reset:	soft
Address:	70554h-70557h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_4_A
Power:	PG1
Reset:	soft
Address:	70558h-7055Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_4_A
Power:	PG1
Reset:	soft
Address:	7055Ch-7055Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_4_A
Power:	PG1
Reset:	soft
Address:	70568h-7056Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_4_A
Power:	PG1
Reset:	soft
Address:	70640h-70643h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_5_A
Power:	PG1
Reset:	soft
Address:	70644h-70647h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_5_A
Power:	PG1

PLANE_WM	
Reset:	soft
Address:	70648h-7064Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_5_A
Power:	PG1
Reset:	soft
Address:	7064Ch-7064Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_5_A
Power:	PG1
Reset:	soft
Address:	70650h-70653h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_5_A
Power:	PG1
Reset:	soft
Address:	70654h-70657h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_5_A
Power:	PG1
Reset:	soft
Address:	70658h-7065Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_5_A
Power:	PG1
Reset:	soft
Address:	7065Ch-7065Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_5_A
Power:	PG1

PLANE_WM	
Reset:	soft
Address:	70668h-7066Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_5_A
Power:	PG1
Reset:	soft
Address:	70740h-70743h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_6_A
Power:	PG1
Reset:	soft
Address:	70744h-70747h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_6_A
Power:	PG1
Reset:	soft
Address:	70748h-7074Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_6_A
Power:	PG1
Reset:	soft
Address:	7074Ch-7074Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_6_A
Power:	PG1
Reset:	soft
Address:	70750h-70753h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_6_A
Power:	PG1
Reset:	soft

PLANE_WM	
Address:	70754h-70757h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_6_A
Power:	PG1
Reset:	soft
Address:	70758h-7075Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_6_A
Power:	PG1
Reset:	soft
Address:	7075Ch-7075Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_6_A
Power:	PG1
Reset:	soft
Address:	70768h-7076Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_6_A
Power:	PG1
Reset:	soft
Address:	70840h-70843h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_7_A
Power:	PG1
Reset:	soft
Address:	70844h-70847h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_7_A
Power:	PG1
Reset:	soft
Address:	70848h-7084Bh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_7_A
Power:	PG1
Reset:	soft
Address:	7084Ch-7084Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_7_A
Power:	PG1
Reset:	soft
Address:	70850h-70853h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_7_A
Power:	PG1
Reset:	soft
Address:	70854h-70857h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_7_A
Power:	PG1
Reset:	soft
Address:	70858h-7085Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_7_A
Power:	PG1
Reset:	soft
Address:	7085Ch-7085Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_7_A
Power:	PG1
Reset:	soft
Address:	70868h-7086Bh

PLANE_WM	
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_7_A
Power:	PG1
Reset:	soft
Address:	71540h-71543h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_4_B
Power:	PG2
Reset:	soft
Address:	71544h-71547h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_4_B
Power:	PG2
Reset:	soft
Address:	71548h-7154Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_4_B
Power:	PG2
Reset:	soft
Address:	7154Ch-7154Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_4_B
Power:	PG2
Reset:	soft
Address:	71550h-71553h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_4_B
Power:	PG2
Reset:	soft
Address:	71554h-71557h
Name:	Plane Watermarks

PLANE_WM	
ShortName:	PLANE_WM_5_4_B
Power:	PG2
Reset:	soft
Address:	71558h-7155Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_4_B
Power:	PG2
Reset:	soft
Address:	7155Ch-7155Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_4_B
Power:	PG2
Reset:	soft
Address:	71568h-7156Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_4_B
Power:	PG2
Reset:	soft
Address:	71640h-71643h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_5_B
Power:	PG2
Reset:	soft
Address:	71644h-71647h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_5_B
Power:	PG2
Reset:	soft
Address:	71648h-7164Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_5_B

PLANE_WM	
Power:	PG2
Reset:	soft
Address:	7164Ch-7164Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_5_B
Power:	PG2
Reset:	soft
Address:	71650h-71653h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_5_B
Power:	PG2
Reset:	soft
Address:	71654h-71657h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_5_B
Power:	PG2
Reset:	soft
Address:	71658h-7165Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_5_B
Power:	PG2
Reset:	soft
Address:	7165Ch-7165Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_5_B
Power:	PG2
Reset:	soft
Address:	71668h-7166Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_5_B

PLANE_WM	
Power:	PG2
Reset:	soft
Address:	71740h-71743h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_6_B
Power:	PG2
Reset:	soft
Address:	71744h-71747h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_6_B
Power:	PG2
Reset:	soft
Address:	71748h-7174Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_6_B
Power:	PG2
Reset:	soft
Address:	7174Ch-7174Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_6_B
Power:	PG2
Reset:	soft
Address:	71750h-71753h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_6_B
Power:	PG2
Reset:	soft
Address:	71754h-71757h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_6_B

PLANE_WM	
Power:	PG2
Reset:	soft
Address:	71758h-7175Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_6_B
Power:	PG2
Reset:	soft
Address:	7175Ch-7175Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_6_B
Power:	PG2
Reset:	soft
Address:	71768h-7176Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_6_B
Power:	PG2
Reset:	soft
Address:	71840h-71843h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_7_B
Power:	PG2
Reset:	soft
Address:	71844h-71847h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_7_B
Power:	PG2
Reset:	soft
Address:	71848h-7184Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_7_B
Power:	PG2

PLANE_WM	
Reset:	soft
Address:	7184Ch-7184Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_7_B
Power:	PG2
Reset:	soft
Address:	71850h-71853h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_7_B
Power:	PG2
Reset:	soft
Address:	71854h-71857h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_7_B
Power:	PG2
Reset:	soft
Address:	71858h-7185Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_7_B
Power:	PG2
Reset:	soft
Address:	7185Ch-7185Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_7_B
Power:	PG2
Reset:	soft
Address:	71868h-7186Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_7_B
Power:	PG2
Reset:	soft

PLANE_WM	
Address:	72540h-72543h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_4_C
Power:	PG2
Reset:	soft
Address:	72544h-72547h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_4_C
Power:	PG2
Reset:	soft
Address:	72548h-7254Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_4_C
Power:	PG2
Reset:	soft
Address:	7254Ch-7254Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_4_C
Power:	PG2
Reset:	soft
Address:	72550h-72553h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_4_C
Power:	PG2
Reset:	soft
Address:	72554h-72557h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_4_C
Power:	PG2
Reset:	soft

PLANE_WM	
Address:	72558h-7255Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_4_C
Power:	PG2
Reset:	soft
Address:	7255Ch-7255Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_4_C
Power:	PG2
Reset:	soft
Address:	72568h-7256Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_4_C
Power:	PG2
Reset:	soft
Address:	72640h-72643h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_5_C
Power:	PG2
Reset:	soft
Address:	72644h-72647h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_5_C
Power:	PG2
Reset:	soft
Address:	72648h-7264Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_5_C
Power:	PG2
Reset:	soft
Address:	7264Ch-7264Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_5_C
Power:	PG2
Reset:	soft
Address:	72650h-72653h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_5_C
Power:	PG2
Reset:	soft
Address:	72654h-72657h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_5_C
Power:	PG2
Reset:	soft
Address:	72658h-7265Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_5_C
Power:	PG2
Reset:	soft
Address:	7265Ch-7265Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_5_C
Power:	PG2
Reset:	soft
Address:	72668h-7266Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_5_C
Power:	PG2
Reset:	soft
Address:	72740h-72743h
Name:	Plane Watermarks

PLANE_WM	
ShortName:	PLANE_WM_0_6_C
Power:	PG2
Reset:	soft
Address:	72744h-72747h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_6_C
Power:	PG2
Reset:	soft
Address:	72748h-7274Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_6_C
Power:	PG2
Reset:	soft
Address:	7274Ch-7274Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_6_C
Power:	PG2
Reset:	soft
Address:	72750h-72753h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_6_C
Power:	PG2
Reset:	soft
Address:	72754h-72757h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_6_C
Power:	PG2
Reset:	soft
Address:	72758h-7275Bh
Name:	Plane Watermarks

PLANE_WM	
ShortName:	PLANE_WM_6_6_C
Power:	PG2
Reset:	soft
Address:	7275Ch-7275Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_6_C
Power:	PG2
Reset:	soft
Address:	72768h-7276Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_6_C
Power:	PG2
Reset:	soft
Address:	72840h-72843h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_7_C
Power:	PG2
Reset:	soft
Address:	72844h-72847h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_7_C
Power:	PG2
Reset:	soft
Address:	72848h-7284Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_7_C
Power:	PG2
Reset:	soft
Address:	7284Ch-7284Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_7_C

PLANE_WM

Power:	PG2
Reset:	soft
Address:	72850h-72853h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_7_C
Power:	PG2
Reset:	soft
Address:	72854h-72857h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_7_C
Power:	PG2
Reset:	soft
Address:	72858h-7285Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_7_C
Power:	PG2
Reset:	soft
Address:	7285Ch-7285Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_7_C
Power:	PG2
Reset:	soft
Address:	72868h-7286Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_7_C
Power:	PG2
Reset:	soft
Address:	70240h-70243h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_1_A

PLANE_WM	
Power:	PG1
Reset:	soft
Address:	70244h-70247h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_1_A
Power:	PG1
Reset:	soft
Address:	70248h-7024Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_1_A
Power:	PG1
Reset:	soft
Address:	7024Ch-7024Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_1_A
Power:	PG1
Reset:	soft
Address:	70250h-70253h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_1_A
Power:	PG1
Reset:	soft
Address:	70254h-70257h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_1_A
Power:	PG1
Reset:	soft
Address:	70258h-7025Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_1_A

PLANE_WM	
Power:	PG1
Reset:	soft
Address:	7025Ch-7025Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_1_A
Power:	PG1
Reset:	soft
Address:	70268h-7026Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_1_A
Power:	PG1
Reset:	soft
Address:	70340h-70343h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_2_A
Power:	PG1
Reset:	soft
Address:	70344h-70347h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_2_A
Power:	PG1
Reset:	soft
Address:	70348h-7034Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_2_A
Power:	PG1
Reset:	soft
Address:	7034Ch-7034Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_2_A
Power:	PG1

PLANE_WM	
Reset:	soft
Address:	70350h-70353h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_2_A
Power:	PG1
Reset:	soft
Address:	70354h-70357h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_2_A
Power:	PG1
Reset:	soft
Address:	70358h-7035Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_2_A
Power:	PG1
Reset:	soft
Address:	7035Ch-7035Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_2_A
Power:	PG1
Reset:	soft
Address:	70368h-7036Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_2_A
Power:	PG1
Reset:	soft
Address:	70440h-70443h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_3_A
Power:	PG1
Reset:	soft

PLANE_WM	
Address:	70444h-70447h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_3_A
Power:	PG1
Reset:	soft
Address:	70448h-7044Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_3_A
Power:	PG1
Reset:	soft
Address:	7044Ch-7044Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_3_A
Power:	PG1
Reset:	soft
Address:	70450h-70453h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_3_A
Power:	PG1
Reset:	soft
Address:	70454h-70457h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_3_A
Power:	PG1
Reset:	soft
Address:	70458h-7045Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_3_A
Power:	PG1
Reset:	soft

PLANE_WM	
Address:	7045Ch-7045Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_3_A
Power:	PG1
Reset:	soft
Address:	70468h-7046Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_3_A
Power:	PG1
Reset:	soft
Address:	71240h-71243h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_1_B
Power:	PG2
Reset:	soft
Address:	71244h-71247h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_1_B
Power:	PG2
Reset:	soft
Address:	71248h-7124Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_1_B
Power:	PG2
Reset:	soft
Address:	7124Ch-7124Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_1_B
Power:	PG2
Reset:	soft
Address:	71250h-71253h

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_1_B
Power:	PG2
Reset:	soft
Address:	71254h-71257h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_1_B
Power:	PG2
Reset:	soft
Address:	71258h-7125Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_1_B
Power:	PG2
Reset:	soft
Address:	7125Ch-7125Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_1_B
Power:	PG2
Reset:	soft
Address:	71268h-7126Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_1_B
Power:	PG2
Reset:	soft
Address:	71340h-71343h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_2_B
Power:	PG2
Reset:	soft
Address:	71344h-71347h
Name:	Plane Watermarks

PLANE_WM	
ShortName:	PLANE_WM_1_2_B
Power:	PG2
Reset:	soft
Address:	71348h-7134Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_2_B
Power:	PG2
Reset:	soft
Address:	7134Ch-7134Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_2_B
Power:	PG2
Reset:	soft
Address:	71350h-71353h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_2_B
Power:	PG2
Reset:	soft
Address:	71354h-71357h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_2_B
Power:	PG2
Reset:	soft
Address:	71358h-7135Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_2_B
Power:	PG2
Reset:	soft
Address:	7135Ch-7135Fh
Name:	Plane Watermarks

PLANE_WM	
ShortName:	PLANE_WM_7_2_B
Power:	PG2
Reset:	soft
Address:	71368h-7136Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_2_B
Power:	PG2
Reset:	soft
Address:	71440h-71443h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_3_B
Power:	PG2
Reset:	soft
Address:	71444h-71447h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_3_B
Power:	PG2
Reset:	soft
Address:	71448h-7144Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_3_B
Power:	PG2
Reset:	soft
Address:	7144Ch-7144Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_3_B
Power:	PG2
Reset:	soft
Address:	71450h-71453h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_3_B

PLANE_WM	
Power:	PG2
Reset:	soft
Address:	71454h-71457h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_3_B
Power:	PG2
Reset:	soft
Address:	71458h-7145Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_3_B
Power:	PG2
Reset:	soft
Address:	7145Ch-7145Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_3_B
Power:	PG2
Reset:	soft
Address:	71468h-7146Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_3_B
Power:	PG2
Reset:	soft
Address:	72240h-72243h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_1_C
Power:	PG2
Reset:	soft
Address:	72244h-72247h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_1_C

PLANE_WM	
Power:	PG2
Reset:	soft
Address:	72248h-7224Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_1_C
Power:	PG2
Reset:	soft
Address:	7224Ch-7224Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_1_C
Power:	PG2
Reset:	soft
Address:	72250h-72253h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_1_C
Power:	PG2
Reset:	soft
Address:	72254h-72257h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_1_C
Power:	PG2
Reset:	soft
Address:	72258h-7225Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_1_C
Power:	PG2
Reset:	soft
Address:	7225Ch-7225Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_1_C

PLANE_WM	
Power:	PG2
Reset:	soft
Address:	72268h-7226Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_1_C
Power:	PG2
Reset:	soft
Address:	72340h-72343h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_2_C
Power:	PG2
Reset:	soft
Address:	72344h-72347h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_2_C
Power:	PG2
Reset:	soft
Address:	72348h-7234Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_2_C
Power:	PG2
Reset:	soft
Address:	7234Ch-7234Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_2_C
Power:	PG2
Reset:	soft
Address:	72350h-72353h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_2_C
Power:	PG2

PLANE_WM	
Reset:	soft
Address:	72354h-72357h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_2_C
Power:	PG2
Reset:	soft
Address:	72358h-7235Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_2_C
Power:	PG2
Reset:	soft
Address:	7235Ch-7235Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_2_C
Power:	PG2
Reset:	soft
Address:	72368h-7236Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_2_C
Power:	PG2
Reset:	soft
Address:	72440h-72443h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_3_C
Power:	PG2
Reset:	soft
Address:	72444h-72447h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_3_C
Power:	PG2
Reset:	soft

PLANE_WM	
Address:	72448h-7244Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_3_C
Power:	PG2
Reset:	soft
Address:	7244Ch-7244Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_3_C
Power:	PG2
Reset:	soft
Address:	72450h-72453h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_3_C
Power:	PG2
Reset:	soft
Address:	72454h-72457h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_3_C
Power:	PG2
Reset:	soft
Address:	72458h-7245Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_3_C
Power:	PG2
Reset:	soft
Address:	7245Ch-7245Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_3_C
Power:	PG2
Reset:	soft

PLANE_WM

Address:	72468h-7246Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_3_C
Power:	PG2
Reset:	soft

Programming Notes

There are eight regular watermarks and a transition watermark per plane/cursor. For YUV planar source formats, only the Y surface watermark value should be programmed. Watermark programming instructions are documented separately.

Restriction

For minimum watermark requirements refer to Display Watermark Programming section.

DWord	Bit	Description
0	31	**Enable** This field enables this watermark. All the watermarks at this level for all enabled planes must be enabled before the level will be used. Value: 1b — Name: Enable Value: 0b — Name: Disable
	30	**Reserved**
	29:19	**Reserved** Format: MBZ
	18:14	**Lines** Default Value: 01h This field contains the watermark value in lines. Hardware ignores the lines for the the transition watermark.
	13:11	**Reserved**
	10:0	**Blocks** Default Value: 007h This field contains the watermark value in blocks of 8 cachelines.

PORT_CL_DW5

PORT_CL_DW5		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Access:	R/W	
Size (in bits):	32	
Address:	162014h-162017h	
Name:	PORT_CL_DW5_A	
ShortName:	PORT_CL_DW5_A	
Power:	PG0	
Reset:	global	
Address:	6C014h-6C017h	
Name:	PORT_CL_DW5_B	
ShortName:	PORT_CL_DW5_B	
Power:	PG0	
Reset:	global	

DWord	Bit	Description
0	31:24	**Force** Default Value: 00010010b
	23	**Reserved** Format: MBZ
	22	**Fusevalid Reset**
	21	**Fusevalid Override**
	20	**Fuse Repull**
	19:16	**CRI Clock Count Max** Default Value: 0100b
	15	**Reserved** Format: MBZ
	14:13	**IOSF PD Count**
	12	**Reserved** Format: MBZ
	11:9	**IOSF ClkDiv Sel**

PORT_CL_DW5

	Default Value:	010b
8	**DL Broadcast Enable** This field causes all Tx's to get programmed when writing to a group access offset for a single Tx.	
7	**Reserved**	
	Format:	MBZ
6	**Enable Port Staggering**	
	Default Value:	1b
5	**PG Staggering Control Disable**	
	Default Value:	1b
4	**CL Power Down Enable**	

Value	Name
0b	Disable
1b	Enable

3	**CRI Clock Select**	
	Default Value:	1b
2	**Phy Power Ack Override**	
1:0	**SUS Clock Config**	

PORT_CL_DW10

PORT_CL_DW10	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	162028h-16202Bh
Name:	PORT_CL_DW10_A
ShortName:	PORT_CL_DW10_A
Power:	PG0
Reset:	global
Address:	6C028h-6C02Bh
Name:	PORT_CL_DW10_B
ShortName:	PORT_CL_DW10_B
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31:28	**Reserved**
	27	**Reserved**
	26:25	**PG Seq Delay Override** PG Sequential Delay Override
	24	**PG Seq Delay Override Enable** PG Sequential Delay Override Enable 0b – Disable 1b – Enable
	23	**ohvpg_ctrl_mipia**

PORT_CL_DW10

		Non-MIPI dies: ospare_cri_ret[7] **MIPI dies where multiple IOs shared one common lane:** MIPI A HVPG Control **MIPI dies where each IO has own common lane:** MIPI HVPG Control
	22	**ohvpg_ctrl_mipic** **Non-MIPI dies**: ospare_cri_ret[6] **MIPI dies where multiple IOs shared one common lane:** MIPI CHVPG Control **MIPI dies where each IO has own common lane:** ospare_cri_ret[6]
	21:16	**ospare_cri_ret_5_0** Default Value: 000011b
	15:8	**Reserved** Format: MBZ
	7:4	**Static Power Down DDI** This field powers down individual lanes. To save power, unused lanes should be powered down after link training is complete.
	3:0	**Reserved** Format: MBZ

Value	Name	Description
0000b	Power up all lanes	Enable x4
1100b	Power down lanes 3,2	Enable x2
1110b	Power down lanes 3,2,1	Enable x1
0011b	Power down lanes 1,0	Enable x2 Reversed
0111b	Power down lanes 2,1,0	Enable x1 Reversed
1000b	Power down lanes 3	Enable DSI x3
1010b	Power down lanes 3,1	Enable DSI x2
1011b	Power down lanes 3,1,0	Enable DSI x1

PORT_CL_DW12

PORT_CL_DW12

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	162030h-162033h
Name:	PORT_CL_DW12_A
ShortName:	PORT_CL_DW12_A
Power:	PG0
Reset:	global
Address:	6C030h-6C033h
Name:	PORT_CL_DW12_B
ShortName:	PORT_CL_DW12_B
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31:30	**Reserved** Format: MBZ
	29	**MIPI Lane Enable** 0b: Disable 1b: Enable
	28	**Reserved** Format: MBZ
	27	**MIPI Mode Override Enable** 0b:

PORT_CL_DW12

		1b
	26	**MIPI Mode Override** Value: Name 0b 1b
	25:12	**Reserved** Format: MBZ
	11	**Pwr Req Override AUX** Value: Name 0b 1b
	10	**Pwr Req Override Enable AUX** Value: Name 0b: Disable 1b: Enable
	9:7	**Reserved** Format: MBZ
	6	**Phy Status AUX** Access: RO
	5	**Reserved** Format: MBZ
	4	**Power Ack AUX** Access: RO
	3:1	**Reserved**

PORT_CL_DW12

		Format: MBZ
	0	**Lane Enable AUX** **Value** / **Name** 0b – Disable 1b – Enable

PORT_CL_DW15

PORT_CL_DW15

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32

Address:	16203Ch-16203Fh
Name:	PORT_CL_DW15_A
ShortName:	PORT_CL_DW15_A
Power:	PG0
Reset:	global

Address:	6C03Ch-6C03Fh
Name:	PORT_CL_DW15_B
ShortName:	PORT_CL_DW15_B
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31:30	**Reserved** Format: MBZ
	29	**HVPG Power Ack** Access: RO Value / Name 0b 1b
	28	**HVPG Enable Status** Access: RO Value / Name 0b

PORT_CL_DW15

		1b
	27	**Power Ack MIPI** Access: RO 0b 1b
	26:22	**Reserved** Format: MBZ
	21	**Power Req AUX** Access: RO 0b 1b
	20:18	**Reserved** Format: MBZ
	17	**Power Ack AUX** Access: RO 0b 1b
	16:0	**Reserved** Format: MBZ

PORT_CL_DW16

PORT_CL_DW16		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Access:	R/W	
Size (in bits):	32	
Address:	162040h-162043h	
Name:	PORT_CL_DW16	
ShortName:	PORT_CL_DW16	
Power:	PG0	
Reset:	global	
DWord	**Bit**	**Description**
0	31:16	**Reserved** Format: MBZ
	15	**o_hd_ddib_sel_ovrden** DDI B HD Port select override enable
	14	**o_hd_ddib_sel_ovrd** DDI B HD Port select override
	13	**o_hd_ddic_sel_ovrden** DDI C HD Port select override enable
	12	**o_hd_ddic_sel_ovrd** DDI C HD Port select override
	11	**o_hd_ddid_sel_ovrden** DDI D HD Port select override enable
	10	**o_hd_ddid_sel_ovrd** DDI D HD Port select override
	9:8	**reserved**
	7:4	**ospare_cri[3:0]** reserved
	3	**o_comp_pwrdown_ovrd** Comp Power Down Override
	2	**o_comp_pwrdown_ovrden** Comp Power Down Override Enable
	1	**o_cri_wake_ovrd** CRI Wake Override

PORT_CL_DW16		
	0	**o_cri_wake_ovrden** CRI Wake Override Enable

PORT_COMP_DW0

PORT_COMP_DW0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	162100h-162103h
Name:	PORT_COMP_DW0_A
ShortName:	PORT_COMP_DW0_A
Power:	PG0
Reset:	global
Address:	6C100h-6C103h
Name:	PORT_COMP_DW0_B
ShortName:	PORT_COMP_DW0_B
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31	**Comp Init**
	30:29	**Tx Slew Ctl**
	28:27	**Tx Drvsw On**
	26	**Tx Drvsw Ctl**
	25:24	**Comp Spare**
	23	**Procmon clock Sel**
	22:20	**Reserved** Format: MBZ
	19:8	**Periodic Comp Counter** Periodic comp programmable counter. Value: 05Fh — Name: 1.25ms **[Default]** — Description: Period of ~ 1.25ms w.r.t sus clock frequency of 19.2MHz.
	7:0	**Reserved** Format: MBZ

PORT_COMP_DW1

PORT_COMP_DW1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	162104h-162107h
Name:	PORT_COMP_DW1_A
ShortName:	PORT_COMP_DW1_A
Power:	PG0
Reset:	global
Address:	6C104h-6C107h
Name:	PORT_COMP_DW1_B
ShortName:	PORT_COMP_DW1_B
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31	**ldo_bypass** Default Value: 1b
	30	**fcomp_ovrd_en**
	29	**fcomp_capratio**
	28	**fcomp_bias_sel**
	27:26	**fcomp_inputsel_ovrd**
	25	**fcomp_polaritysel**
	24	**rcomp_en** Default Value: 1b
	23:22	**p_ref_highval[9:8]** Default Value: 01b
	21:20	**p_ref_lowval[9:8]**
	19:18	**n_ref_highval[9:8]** Default Value: 01b
	17:16	**n_ref_lowval[9:8]**

PORT_COMP_DW1		
	15:14	**phvt_ref_highval[9:8]**
	13:12	**phvt_ref_lowval[9:8]**
	11:10	**nhvt_ref_highval[9:8]** Default Value: 01h
	9:8	**nhvt_ref_lowval[9:8]**
	7:6	**plvt_ref_highval[9:8]** Default Value: 01b
	5:4	**plvt_ref_lowval[9:8]**
	3:2	**nlvt_ref_highval[9:8]** Default Value: 01b
	1:0	**nlvt_ref_lowval[9:8]**

PORT_COMP_DW3

PORT_COMP_DW3

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	16210Ch-16210Fh
Name:	PORT_COMP_DW3_A
ShortName:	PORT_COMP_DW3_A
Power:	PG0
Reset:	global
Address:	6C10Ch-6C10Fh
Name:	PORT_COMP_DW3_B
ShortName:	PORT_COMP_DW3_B
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28:26	**Process Info** 000b: dot-0 001b: dot-1 010b: dot-4
	25:24	**Voltage Info** 00b: 0.85V 01b: 0.95V 10b: 1.05
	23	**PLL DDI Pwr Ack**
	22	**First Comp Done**
	21	**Procmon Done**

PORT_COMP_DW3		
	20	**Icomp Code Maxout**
	19	**Icomp Code Minout**
	18:15	**Reserved** Format: MBZ
	14:8	**Icomp Code**
	7	**Lpdn Code Maxout**
	6	**Lpdn Code Minout**
	5:0	**MIPI Lpdn Code**

PORT_COMP_DW8

PORT_COMP_DW8

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	162120h-162123h
Name:	PORT_COMP_DW8_A
ShortName:	PORT_COMP_DW8_A
Power:	PG0
Reset:	global
Address:	6C120h-6C123h
Name:	PORT_COMP_DW8_B
ShortName:	PORT_COMP_DW8_B
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31:25	**Reserved** Format: PBZ The values in this field must not be changed. Use read/modify/write to update this register.
	24	**irefgen** Value: 1b — Name: Enable Value: 0b — Name: Disable
	23:15	**Reserved** Format: PBZ The values in this field must not be changed. Use read/modify/write to update this register.
	14	**prdic_icomp_dis** disable periodic icomp Value: 0b — Name: Enable

PORT_COMP_DW8			
		1b	Disable
	13:0	**Reserved** Format: PBZ The values in this field must not be changed. Use read/modify/write to update this register.	

PORT_COMP_DW9

PORT_COMP_DW9	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	162124h-162127h
Name:	PORT_COMP_DW9_A
ShortName:	PORT_COMP_DW9_A
Power:	PG0
Reset:	global
Address:	6C124h-6C127h
Name:	PORT_COMP_DW9_B
ShortName:	PORT_COMP_DW9_B
Power:	PG0
Reset:	global

DWord	Bit	Description	
0	31:24	**n_ref_lowval[7:0]**	
		Default Value:	11011010b
	23:16	**n_ref_highval[7:0]**	
		Default Value:	10001100b
	15:8	**p_ref_lowval[7:0]**	
		Default Value:	11011100b
	7:0	**p_ref_highval[7:0]**	
		Default Value:	10100101b

PORT_COMP_DW10

PORT_COMP_DW10	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	162128h-16212Bh
Name:	PORT_COMP_DW10_A
ShortName:	PORT_COMP_DW10_A
Power:	PG0
Reset:	global
Address:	6C128h-6C12Bh
Name:	PORT_COMP_DW10_B
ShortName:	PORT_COMP_DW10_B
Power:	PG0
Reset:	global

DWord	Bit	Description	
0	31:24	**nlvt_ref_lowval[7:0]**	
		Default Value:	10101010b
	23:16	**nlvt_ref_highval[7:0]**	
		Default Value:	00111101b
	15:8	**plvt_ref_lowval[7:0]**	
		Default Value:	10101000b
	7:0	**plvt_ref_highval[7:0]**	
		Default Value:	01010011b

PORT_PCS_DW1

PORT_PCS_DW1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	162604h-162607h
Name:	PORT_PCS_DW1_GRP_A
ShortName:	PORT_PCS_DW1_GRP_A
Power:	PG0
Reset:	global
Address:	162804h-162807h
Name:	PORT_PCS_DW1_LN0_A
ShortName:	PORT_PCS_DW1_LN0_A
Power:	PG0
Reset:	global
Address:	162304h-162307h
Name:	PORT_PCS_DW1_AUX_A
ShortName:	PORT_PCS_DW1_AUX_A
Power:	PG0
Reset:	global
Address:	6C604h-6C607h
Name:	PORT_PCS_DW1_GRP_B
ShortName:	PORT_PCS_DW1_GRP_B
Power:	PG0
Reset:	global
Address:	6C804h-6C807h
Name:	PORT_PCS_DW1_LN0_B
ShortName:	PORT_PCS_DW1_LN0_B

PORT_PCS_DW1

Power: PG0
Reset: global

Address: 6C304h-6C307h
Name: PORT_PCS_DW1_AUX_B
ShortName: PORT_PCS_DW1_AUX_B

Power: PG0
Reset: global

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28	**cmnkeeper_enable_in_pg** 1b: enable **[Default]** 0b: disable
	27	**pg_pwrdownen** PG Power Down Enable 1b: enable **[Default]** 0b: disable
	26	**cmnkeeper_enable** Common Keeper Enable 1b: enable **[Default]** 0b: disable
	25:24	**cmnkeep_biasctr** Common Keeper Bias Control
	23:22	**Reserved**
	21:16	**dcc**
	15:14	**Reserved**
	13:12	**txhigh**
	11:10	**Reserved**
	9:8	**clkreq**
	7	**tbc_as_symbclk** Select tbc clock to be used as symbol clock internal to the data lane
	6	**txfifo_rst_master_ovrden**

		Override enable for Tx master resets
	5	**txfifo_rst_master_ovrd** Reset Master Override for Tx
	4	**txdeemp** Deemphasis Value
	3:2	**latencyoptim** Default Value: 01b Latency Optim
	1	**softreset_enable** Allow soft_reset_n to reset the lanes Value: 1b — Name: enable Value: 0b — Name: disable
	0	**soft_reset_n** Default Value: 1b Active low soft reset override

PORT_PCS_DW9

PORT_PCS_DW9	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	162624h-162627h
Name:	PORT_PCS_DW9_GRP_A
ShortName:	PORT_PCS_DW9_GRP_A
Power:	PG0
Reset:	global
Address:	162824h-162827h
Name:	PORT_PCS_DW9_LN0_A
ShortName:	PORT_PCS_DW9_LN0_A
Power:	PG0
Reset:	global
Address:	162324h-162327h
Name:	PORT_PCS_DW9_AUX_A
ShortName:	PORT_PCS_DW9_AUX_A
Power:	PG0
Reset:	global
Address:	6C624h-6C627h
Name:	PORT_PCS_DW9_GRP_B
ShortName:	PORT_PCS_DW9_GRP_B
Power:	PG0
Reset:	global
Address:	6C824h-6C827h
Name:	PORT_PCS_DW9_LN0_B
ShortName:	PORT_PCS_DW9_LN0_B

PORT_PCS_DW9

Power:	PG0
Reset:	global
Address:	6C324h-6C327h
Name:	PORT_PCS_DW9_AUX_B
ShortName:	PORT_PCS_DW9_AUX_B
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31:28	**Reserved** Format: MBZ
	27:16	**Strong CM Count Ovrd** Default Value: 301h
	15:11	**Reserved** Format: MBZ
	10:8	**Stagger Mult** Default Value: 001b
	7:6	**Reserved** Format: MBZ
	5	**Stagger Override**
	4:0	**Stagger**

PORT_TX_DFLEXDPCSSS

PORT_TX_DFLEXDPCSSS	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	163894h-163897h
Name:	PORT_TX_DFLEXDPCSSS
ShortName:	PORT_TX_DFLEXDPCSSS
Power:	PG0
Reset:	global

The Type-C Connector number (e.g. "0" in register DPPMSTC0) is logical number.

DWord	Bit	Description
0	31:8	**Reserved** Format: MBZ
	7	**Displayport Phy Mode Status for Type-C Connector 7** Similar to register DFLEXDPCSSS.DPPMSTC0 but this register is for Type-C Connector 7.
	6	**Displayport Phy Mode Status for Type-C Connector 6** Similar to register DFLEXDPCSSS.DPPMSTC0 but this register is for Type-C Connector 6.
	5	**Displayport Phy Mode Status for Type-C Connector 5** Similar to register DFLEXDPCSSS.DPPMSTC0 but this register is for Type-C Connector 5.
	4	**Displayport Phy Mode Status for Type-C Connector 4** Similar to register DFLEXDPCSSS.DPPMSTC0 but this register is for Type-C Connector 4.
	3	**Displayport Phy Mode Status for Type-C Connector 3** Similar to register DFLEXDPCSSS.DPPMSTC0 but this register is for Type-C Connector 3.
	2	**Displayport Phy Mode Status for Type-C Connector 2** Similar to register DFLEXDPCSSS.DPPMSTC0 but this register is for Type-C Connector 2.
	1	**Displayport Phy Mode Status for Type-C Connector 1** Similar to register DFLEXDPCSSS.DPPMSTC0 but this register is for Type-C Connector 1.
	0	**Displayport Phy Mode Status for Type-C Connector 0** Displayport Phy Mode Status for Type-C Connector 0 (DPPMSTC0): The Type-C Connector number is logical number. It is not physical lane numbers. Refer to the SoC block diagram for the mapping of Type-C Connector number to the actual physical lane number of the PHY. Value: 1b — Name: DP Controller is not in safe state

PORT_TX_DFLEXDPCSSS			
		0b	DP controller is in safe state

PORT_TX_DFLEXDPMLE1

PORT_TX_DFLEXDPMLE1 - PORT_TX_DFLEXDPMLE1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	soft
Address:	1638C0h-1638C3h
Name:	PORT_TX_DFLEXDPMLE1
ShortName:	PORT_TX_DFLEXDPMLE1
Power:	PG0
Reset:	soft

Display Driver writes to these bits to tell FIA hardware which Main Links of the Display Port are enabled on Type-C Connector 0. FIA hardware uses this information for PHY to Controller signal mapping.
For example, in DP Pin Assignment C, the register DFLEXDPSP1.DPX4TXLATC0 tells Display Driver that all the 4 TX Lanes in PHY can be used. However, Display Driver may choose to use only x1, i.e. for ML0. Then Display Driver will program “0001b” to this register. For x2 and x4, Display Driver will program “0011b” and “1111b”, respectively.
In the case of "No pin assignment" (fixed or static DP connection in MG PHY programming page), if display driver chooses to use only x2 with no lane reversal, then display driver will program "0011" to this register. If display driver chooses to use only x2 with lane reversal, then display driver will program "1100" to this register. If display driver chooses to use only x1 with no lane reversal, then display driver will program "0001" to this register. If display driver chooses to use only x1 with lane reversal, then display driver will program "1000" to this register.
Display Driver is expected to write to this register when the DDI Interface between DP Controller and FIA is in the Safe Mode, e.g. pllen=pwrreq=lane_enable=0. Display Driver writes to this register and then only it brings up the DP Controller, i.e. to bring the DDI interface out from Safe Mode.
A mode set is required to switch the number of DP lanes.
This register is applicable in both Type-C connector's Alternate mode and also DP connector mode.

DWord	Bit	Description
0	31:28	**Displayport Main Link Enable for Type-C Connector 7** Similar to register DFLEXDPMLE1.DPMLETC0 but this register is for Type-C Connector 7.

Value	Name
0001b	ML0
0011b	ML[1:0]
1100b	ML[3:2]
1111b	ML[3:0]

PORT_TX_DFLEXDPMLE1 - PORT_TX_DFLEXDPMLE1

	27:24	**Displayport Main Link Enable for Type-C Connector 6** Similar to register DFLEXDPMLE1.DPMLETC0 but this register is for Type-C Connector 6.

Value	Name
0001b	ML0
0011b	ML[1:0]
1100b	ML[3:2]
1111b	ML[3:0]

	23:20	**Displayport Main Link Enable for Type-C Connector 5** Similar to register DFLEXDPMLE1.DPMLETC0 but this register is for Type-C Connector 5.

Value	Name
0001b	ML0
0011b	ML[1:0]
1100b	ML[3:2]
1111b	ML[3:0]

	19:16	**Displayport Main Link Enable for Type-C Connector 4** Similar to register DFLEXDPMLE1.DPMLETC0 but this register is for Type-C Connector 4.

Value	Name
0001b	ML0
0011b	ML[1:0]
1100b	ML[3:2]
1111b	ML[3:0]

	15:12	**Displayport Main Link Enable for Type-C Connector 3** Similar to register DFLEXDPMLE1.DPMLETC0 but this register is for Type-C Connector 3.

Value	Name
0001b	ML0
0011b	ML[1:0]
1100b	ML[3:2]
1111b	ML[3:0]

	11:8	**Displayport Main Link Enable for Type-C Connector 2** Similar to register DFLEXDPMLE1.DPMLETC0 but this register is for Type-C Connector 2.

Value	Name
0001b	ML0
0011b	ML[1:0]
1100b	ML[3:2]
1111b	ML[3:0]

	7:4	**Displayport Main Link Enable for Type-C Connector 1** Similar to register DFLEXDPMLE1.DPMLETC0 but this register is for Type-C Connector 1.

PORT_TX_DFLEXDPMLE1 - PORT_TX_DFLEXDPMLE1

		Value / **Name**
		0001b — ML0
		0011b — ML[1:0]
		1100b — ML[3:2]
		1111b — ML[3:0]
	3:0	**Displayport Main Link Enable for Type-C Connector 0** Display Port Main Link Enable for Type-C Connector 0 (DPMLETC0): 4 bits correspond to 4 Main Link in DP Controller. Bit [0] is ML0,bit [1] is ML1 and so on. The Type-C Connector number is logical number. It's not physical lane numbers. Refer to the SOC block diagram for the mapping of Type-C Connector number to the actual physical lane number of the PHY. Display Driver writes to these bits to tell FIA hardware which Main Links of the Display Port are enabled on Type-C Connector 0. FIA hardware use this information for PHY to Controller signal mapping. For example, in DP Pin Assignment C, the register DFLEXDPSP1.DPX4TXLATC0 tells Display Driver that all the 4 TX Lane in PHY can be used. However, Display Driver may choose to use only x1, i.e. for ML0. Then Display Driver will program "0001b" to this register. For x2 and x4, Display Driver will program "0011b" and "1111b", respectively.

Value	Name
0001b	ML0
0011b	ML[1:0]
1100b	ML[3:2]
1111b	ML[3:0]

PORT_TX_DFLEXDPPMS

PORT_TX_DFLEXDPPMS - PORT_TX_DFLEXDPPMS	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	soft
Address:	163890h-163893h
Name:	PORT_TX_DFLEXDPPMS
ShortName:	PORT_TX_DFLEXDPPMS
Power:	PG0
Reset:	soft

DWord	Bit	Description
0	31:16	**Reserved**
	15	**Display Port PHY Mode status for Type-C connector 15** Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 15.
	14	**Display Port PHY Mode status for Type-C connector 14** Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 14.
	13	**Display Port PHY Mode status for Type-C connector 13** Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 13.
	12	**Display Port PHY Mode status for Type-C connector 12** Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 12.
	11	**Display Port PHY Mode status for Type-C connector 11** Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 11.
	10	**Display Port PHY Mode status for Type-C connector 10** Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 10.
	9	**Display Port PHY Mode status for Type-C connector 9** Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 9.
	8	**Display Port PHY Mode status for Type-C connector 8** Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 8.
	7	**Display Port PHY Mode status for Type-C connector 7** Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 7.
	6	**Display Port PHY Mode status for Type-C connector 6** Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 6.
	5	**Display Port PHY Mode status for Type-C connector 5** Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 5.

PORT_TX_DFLEXDPPMS - PORT_TX_DFLEXDPPMS

	4	**Display Port PHY Mode status for Type-C connector 4** Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 4.
	3	**Display Port PHY Mode status for Type-C connector 3** Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 3.
	2	**Display Port PHY Mode status for Type-C connector 2** Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 2.
	1	**Display Port PHY Mode status for Type-C connector 1** Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 1.
	0	**Display Port PHY Mode status for Type-C connector 0** DFLEXDPPMS.DPPMSTC0 PD FW writes '1' to this bit to tell DP Driver that PHY is ready. PD FW writes '0' to this bit to tell DP Driver that PHY is not ready.

Value	Name
0b	Not Completed
1b	Completed

PORT_TX_DFLEXDPSP

PORT_TX_DFLEXDPSP - PORT_TX_DFLEXDPSP	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	soft
Address:	1638A0h-1638A3h
Name:	PORT_TX_DFLEXDPSP1
ShortName:	PORT_TX_DFLEXDPSP1
Power:	PG0
Reset:	soft
Address:	1638A4h-1638A7h
Name:	PORT_TX_DFLEXDPSP2
ShortName:	PORT_TX_DFLEXDPSP2
Power:	PG0
Reset:	soft
Address:	1638A8h-1638ABh
Name:	PORT_TX_DFLEXDPSP3
ShortName:	PORT_TX_DFLEXDPSP3
Power:	PG0
Reset:	soft
Address:	1638ACh-1638AFh
Name:	PORT_TX_DFLEXDPSP4
ShortName:	PORT_TX_DFLEXDPSP4
Power:	PG0
Reset:	soft
Dynamic FlexIO DP Scratch Pad (Type-C) There are up to 4 instances of this register per FIA. DFLEXDPSP1 supports connectors 0-3 (logical number). DFLEXDPSP2 supports connectors 4-7 (logical number).	

PORT_TX_DFLEXDPSP - PORT_TX_DFLEXDPSP

DFLEXDPSP3 supports connectors 8-11 (logical number).
DFLEXDPSP4 supports connectors 12-15 (logical number).
The connector number specified in these fields is relative to the connector supported by this register instance. ie. DFLEXDPSP2 field Display Port x4 TX Lane Assignment for Type-C Connector 0 is referring to connector 4 (logical number), and DFLEXDPSP4 field Display Port x4 TX Lane Assignment for Type-C Connector 3 is referring to connector 15 (local number).

When module FIA is enabled i.e., PORT_TX_DFLEXDPSP[MF] = 1,
Ports 1 and 2 live state would be reported to FIA0.DFLEXDPSP1 (bits 5, 6, 13, 14) from FIA0.
Ports 3 and 4 live state would be reported to FIA1.DFLEXDPSP1(bits 5, 6, 13, 14) from FIA1.

DWord	Bit	Description
0	31	**Reserved**
	30:29	**TC3 Live State** 00b – No HPD – No HPD connect for TypeC (DP alternate) or TBT 01b – TypeC HPD – HPD connect for TypeC (DP alternate) 10b – TBT HPD – HPD connect for TBT 11b – Invalid – Invalid
	28	**Reserved**
	27:24	**Display Port x4 TX Lane Assignment for Type-C Connector 3** Same definition as DFLEXDPSP1.DPX4TXLATC0, but this register is for Type-C Connector 3. 0001b – PHY TX[0] 0010b – PHY TX[1] 0011b – PHY TX[1:0] 0100b – PHY TX[2] 0101b – PHY TX[2] TX[0] 1000b – PHY TX[3] 1100b – PHY TX[3:2] 1111b – PHY TX[3:0]
	23	**Reserved**
	22:21	**TC2 Live State** 00b – No HPD – No HPD connect for TypeC (DP alternate) or TBT 01b – TypeC HPD – HPD connect for TypeC (DP alternate) 10b – TBT HPD – HPD connect for TBT 11b – Invalid – Invalid
	20	**Reserved**

PORT_TX_DFLEXDPSP - PORT_TX_DFLEXDPSP

19:16 Display Port x4 TX Lane Assignment for Type-C Connector 2

Same definition as DFLEXDPSP1.DPX4TXLATC0, but this register is for Type-C Connector 2.

Value	Name
0001b	PHY TX[0]
0010b	PHY TX[1]
0011b	PHY TX[1:0]
0100b	PHY TX[2]
0101b	PHY TX[2] TX[0]
1000b	PHY TX[3]
1100b	PHY TX[3:2]
1111b	PHY TX[3:0]

15 Reserved

14:13 TC1 Live State

Value	Name	Description
00b	No HPD	No HPD connect for TypeC (DP alternate) or TBT
01b	TypeC HPD	HPD connect for TypeC (DP alternate)
10b	TBT HPD	HPD connect for TBT
11b	Invalid	Invalid

12 Reserved

11:8 Display Port x4 TX Lane Assignment for Type-C Connector 1

Same definition as DFLEXDPSP1.DPX4TXLATC0, but this register is for Type-C Connector 1.

Value	Name
0001b	PHY TX[0]
0010b	PHY TX[1]
0011b	PHY TX[1:0]
0100b	PHY TX[2]
0101b	PHY TX[2] TX[0]
1000b	PHY TX[3]
1100b	PHY TX[3:2]
1111b	PHY TX[3:0]

7 Reserved

6:5 TC0 Live state

Value	Name	Description
00b	No HPD	No HPD connect for TypeC (DP alternate) or TBT
01b	TypeC HPD	HPD connect for TypeC (DP alternate)
10b	TBT HPD	HPD connect for TBT

11b	Invalid	Invalid

4 DP Scratch Pad TC0LSB (DPSPTC0LSB)

3:0 Display Port x4 TX Lane Assignment for Type-C Connector 0

DPX4TXLATC0

SOC FW writes to these bits to tell display software the Lane Assignment, which it generatesbased on the DP Pin Assignment and the Connector Orientation. Display software uses this value to determine the number of lanes that can be enabled, and along with other registers, to determine the DP mode programming. See the Typec PHY DDI Buffer page for DP mode programming.

The 4 bits correspond to 4 TX, i.e. TX[3:0] Lane in PHY.

Lower 2 bits correspond to the 2 lower TX lane on the PHY of Type-C connector.

Upper 2 bits correspond to the upper 2 TX lane on the PHY of Type-C connector.

For example, in DP Pin Assignment D (Multi function) and Flip case, the x2 TX lane are on the upper TypeC Lane, hence the value written into this register will be 1100b.

Another example, in DP Pin Assignment B (Multi function) Active Gen2 cable and Flip case, the x1 TX lane is on the 1st TX of upper TypeC Lane, hence the value written into this register will be 0100b.

This register is not used by HW.

Value	Name
0001b	PHY TX[0]
0010b	PHY TX[1]
0011b	PHY TX[1:0]
0100b	PHY TX[2]
0101b	PHY TX[2] TX[0]
1000b	PHY TX[3]
1100b	PHY TX[3:2]
1111b	PHY TX[3:0]

PORT_TX_DFLEXNPCPMS

PORT_TX_DFLEXNPCPMS - PORT_TX_DFLEXNPCPMS	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	soft
Address:	163480h-163483h
Name:	PORT_TX_DFLEXNPCPMS
ShortName:	PORT_TX_DFLEXNPCPMS
Power:	PG0
Reset:	soft

SW writes to these bits to control the Combo Port's mode. This register governs the Phy status tracking handling that could be different for different controllers.

DWord	Bit	Description
0	31:28	**Combo Port 7 Next Phy Combo Port Mode Select (CP7NPCPMS):** Similar to register DFLEXNPCPMS1.CP0NPCPMS but this register is for Combo Port 7.
	27:24	**Combo Port 6 Next Phy Combo Port Mode Select (CP6NPCPMS):** Similar to register DFLEXNPCPMS1.CP0NPCPMS but this register is for Combo Port 6.
	23:20	**Combo Port 5 Next Phy Combo Port Mode Select (CP5NPCPMS):** Similar to register DFLEXNPCPMS1.CP0NPCPMS but this register is for Combo Port 5.
	19:16	**Combo Port 4 Next Phy Combo Port Mode Select (CP4NPCPMS):** Similar to register DFLEXNPCPMS1.CP0NPCPMS but this register is for Combo Port 4.
	15:12	**Combo Port 3 Next Phy Combo Port Mode Select (CP3NPCPMS):** Similar to register DFLEXNPCPMS1.CP0NPCPMS but this register is for Combo Port 3.
	11:8	**Combo Port 2 Next Phy Combo Port Mode Select (CP2NPCPMS):** Similar to register DFLEXNPCPMS1.CP0NPCPMS but this register is for Combo Port 2.
	7:4	**Combo Port 1 Next Phy Combo Port Mode Select (CP1NPCPMS):** Similar to register DFLEXNPCPMS1.CP0NPCPMS but this register is for Combo Port 1.
	3:0	**Combo Port 0 Next Phy Combo Port Mode Select (CP0NPCPMS):** The Combo Port number is logical. It's not physical lane numbers. 0h: Port Mode is NoOwner_USB3. FIA will keep the Lane in Reset state. PhyMode=USB3 1h: Port Mode is Owner 1 (default owner) 2h: Port Mode is Owner 2 3h: Port Mode is Owner 3 4h: Port Mode is Owner 4 5h: Port Mode is Owner 5

PORT_TX_DFLEXNPCPMS - PORT_TX_DFLEXNPCPMS		
		6h-Fh: Reserved Others: Reserved SW mode: SW writes to these bits to control the Combo Port's mode. This register governs the Phy status tracking handling that could be different for different controller. HW mode: These bits have no impact to HW when written. The reset default is dependent on the internal HW mux select bits though it's being indicated as soft-straps. The mux select bits retain their context across Sx and will be reloaded back into this field.

PORT_TX_DFLEXOLEN1

PORT_TX_DFLEXOLEN1 - PORT_TX_DFLEXOLEN1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	soft
Address:	163400h-163403h
Name:	PORT_TX_DFLEXOLEN1
ShortName:	PORT_TX_DFLEXOLEN1
Power:	PG0
Reset:	soft

THIS REGISTER IS ADDED FOR STANDALONE TESTING ONLY.
Dynamic FlexIO Owner's Lane Enable.

DWord	Bit	Description
0	31:28	**Combo Port 7 Owner's Lane Enable (CP7OLEN):** Similar to register DFLEXOLE1.CP0OLEN but this register is for Combo Port 7.
	27:24	**Combo Port 6 Owner's Lane Enable (CP6OLEN):** Similar to register DFLEXOLE1.CP0OLEN but this register is for Combo Port 6.
	23:20	**Combo Port 5 Owner's Lane Enable (CP5OLEN):** Similar to register DFLEXOLE1.CP0OLEN but this register is for Combo Port 5.
	19:16	**Combo Port 4 Owner's Lane Enable (CP4OLEN):** Similar to register DFLEXOLE1.CP0OLEN but this register is for Combo Port 4.
	15:12	**Combo Port 3 Owner's Lane Enable (CP3OLEN):** Similar to register DFLEXOLE1.CP0OLEN but this register is for Combo Port 3.
	11:8	**Combo Port 2 Owner's Lane Enable (CP2OLEN):** Similar to register DFLEXOLE1.CP0OLEN but this register is for Combo Port 2.
	7:4	**Combo Port 1 Owner's Lane Enable (CP1OLEN):** The Combo Port number is logical. It's not physical lane numbers. 0h: Port Mode is NoOwner_USB3 1h: Port Mode is Owner 1 (default owner) 2h: Port Mode is Owner 2 3h: Port Mode is Owner 3 4h: Port Mode is Owner 4 5h: Port Mode is Owner 5 6h-Fh: Reserved When this register is choosing Owner 1, the lane_en signal to Owner 1 of Lane 0 is asserted while

PORT_TX_DFLEXOLEN1 - PORT_TX_DFLEXOLEN1		
		the lane_en signals to other Owners of Lane 0 are deasserted. When this register is choosing Owner 2 of Lane 0, the lane_en signal to Owner 2 of Lane 0 is asserted while the lane_en signals to other Owners of Lane 0 are deasserted, and so on. When this register is choosing NoOwner_USB3, the lane_en signals to all the Owners of Lane 0 are deasserted. SW writes to these bits to control the lane_en signal to all the Owners. Register Attribute: Dynamic Implementation Note: If this register is programmed to a value correspond to the Alternate Protocol that is disabled by the fuse (refer to FC1.*APDF), the effective value used by the Type-C Switching logic is 0h, i.e. NoOwner_USB3 Note: For ICL: Owner 1 is USB3; Owner 2 is TBT; Owner 3 is DP/HDMI Owner 4 is HTI.
	3:0	**Combo Port 0 Owner's Lane Enable (CP0OLEN):** The Combo Port number is logical. It's not physical lane numbers. 0h: Port Mode is NoOwner_USB3 1h: Port Mode is Owner 1 (default owner) 2h: Port Mode is Owner 2 3h: Port Mode is Owner 3 4h: Port Mode is Owner 4 5h: Port Mode is Owner 5 6h-Fh: Reserved When this register is choosing Owner 1, the lane_en signal to Owner 1 of Lane 0 is asserted while the lane_en signals to other Owners of Lane 0 are deasserted. When this register is choosing Owner 2 of Lane 0, the lane_en signal to Owner 2 of Lane 0 is asserted while the lane_en signals to other Owners of Lane 0 are deasserted, and so on. When this register is choosing NoOwner_USB3, the lane_en signals to all the Owners of Lane 0 are deasserted. SW writes to these bits to control the lane_en signal to all the Owners. Register Attribute: Dynamic Implementation Note: If this register is programmed to a value correspond to the Alternate Protocol that is disabled by the fuse (refer to FC1.*APDF), the effective value used by the Type-C Switching logic is 0h, i.e. NoOwner_USB3 Note: For ICL: Owner 1 is USB3; Owner 2 is TBT; Owner 3 is DP/HDMI Owner 4 is HTI.

PORT_TX_DFLEXORMP

PORT_TX_DFLEXORMP - PORT_TX_DFLEXORMP	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	soft
Address:	1633E0h-1633E3h
Name:	PORT_TX_DFLEXORMP
ShortName:	PORT_TX_DFLEXORMP
Power:	PG0
Reset:	soft

DFLEXORMP register supports different polarity of Receptacle by OEM.

DWord	Bit	Description
0	31:16	**Reserved** Default Value: 0000000000000000b Access: RO
	15	**Orientation Muxing Policy Connector 15** Similar to register DFLEXORMP.ORMPTC0 but this register is for Type-C Connector 15.
	14	**Orientation Muxing Policy Connector 14** Similar to register DFLEXORMP.ORMPTC0 but this register is for Type-C Connector 14.
	13	**Orientation Muxing Policy Connector 13** Similar to register DFLEXORMP.ORMPTC0 but this register is for Type-C Connector 13.
	12	**Orientation Muxing Policy Connector 12** Similar to register DFLEXORMP.ORMPTC0 but this register is for Type-C Connector 12.
	11	**Orientation Muxing Policy Connector 11** Similar to register DFLEXORMP.ORMPTC0 but this register is for Type-C Connector 11.
	10	**Orientation Muxing Policy Connector 10** Similar to register DFLEXORMP.ORMPTC0 but this register is for Type-C Connector 10.
	9	**Orientation Muxing Policy Connector 9** Similar to register DFLEXORMP.ORMPTC0 but this register is for Type-C Connector 9.
	8	**Orientation Muxing Policy Connector 8** Similar to register DFLEXORMP.ORMPTC0 but this register is for Type-C Connector 8.
	7	**Orientation Muxing Policy Connector 7** Similar to register DFLEXORMP.ORMPTC0 but this register is for Type-C Connector 7.

PORT_TX_DFLEXORMP - PORT_TX_DFLEXORMP

	6	**Orientation Muxing Policy Connector 6** Similar to register DFLEXORMP.ORMPTC0 but this register is for Type-C Connector 6.
	5	**Orientation Muxing Policy Connector 5** Similar to register DFLEXORMP.ORMPTC0 but this register is for Type-C Connector 5.
	4	**Orientation Muxing Policy Connector 4** Similar to register DFLEXORMP.ORMPTC0 but this register is for Type-C Connector 4.
	3	**Orientation Muxing Policy Connector 3** Similar to register DFLEXORMP.ORMPTC0 but this register is for Type-C Connector 3.
	2	**Orientation Muxing Policy Connector 2** Similar to register DFLEXORMP.ORMPTC0 but this register is for Type-C Connector 2.
	1	**Orientation Muxing Policy Connector 1** Value / Name / Description 0 / Clear / When cleared, no lane swapping occurs. 1 / Set / When set, the x2 lanes associated with Type-C Connector 1 is swapped.
	0	**Orientation Muxing Policy Connector 0** Value / Name / Description 0 / Clear / The first Super Speed lanes pair on the Type-C Receptacle is connected to PHY Lane 0 while the second Super Speed lanes pair on the Type-C Receptacle is connected to PHY Lane 1. 1 / Set / The first Super Speed lanes pair on the Type-C Receptacle is connected to PHY Lane 1 while the second Super Speed lanes pair on the Type-C Receptacle is connected to PHY Lane 0.

PORT_TX_DFLEXPA1

PORT_TX_DFLEXPA1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	163880h-163883h
Name:	PORT_TX_DFLEXPA1
ShortName:	PORT_TX_DFLEXPA1
Power:	PG0
Reset:	global

FIA has per Connector register to govern the Pin Assignment of each Type-C Connector. For example, DFLEXPA1.DPPATC0 is used to govern the Pin Assignment of Type-C Connector 0. The Type-C Connector number (e.g. "0" in register DPPATC0) is logical number.

DWord	Bit	Description
0	31:28	**Displayport Pin Assignment for Type-C Connector 7** Similar to register DFLEXPA1.DPPATC0 but this register is for Type-C Connector 7.
	27:24	**Displayport Pin Assignment for Type-C Connector 6** Similar to register DFLEXPA1.DPPATC0 but this register is for Type-C Connector 6.
	23:20	**Displayport Pin Assignment for Type-C Connector 5** Similar to register DFLEXPA1.DPPATC0 but this register is for Type-C Connector 5.
	19:16	**Displayport Pin Assignment for Type-C Connector 4** Similar to register DFLEXPA1.DPPATC0 but this register is for Type-C Connector 4.
	15:12	**Displayport Pin Assignment for Type-C Connector 3** Similar to register DFLEXPA1.DPPATC0 but this register is for Type-C Connector 3.
	11:8	**Displayport Pin Assignment for Type-C Connector 2** Similar to register DFLEXPA1.DPPATC0 but this register is for Type-C Connector 2.
	7:4	**Displayport Pin Assignment for Type-C Connector 1** Similar to register DFLEXPA1.DPPATC0 but this register is for Type-C Connector 1.
	3:0	**Displayport Pin Assignment for Type-C Connector 0** Display Port Pin Assignment for Type-C Connector 0 (DPPATC0): Assignments A, C, and E have 4 lanes for DP alternate mode. Assignments B, D, and F have 2 lanes for DP alternate mode.

Value	Name
0000b	No Pin Assignment (For Non Type-C DP)
0001b	Pin Assignment A

PORT_TX_DFLEXPA1			
		0010b	Pin Assignment B
		0011b	Pin Assignment C
		0100b	Pin Assignment D
		0101b	Pin Assignment E
		0110b	Pin Assignment F

PORT_TX_DFLEXPA2

PORT_TX_DFLEXPA2 - PORT_TX_DFLEXPA2	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	soft
Address:	163884h-163887h
Name:	PORT_TX_DFLEXPA2
ShortName:	PORT_TX_DFLEXPA2
Power:	PG0
Reset:	soft

FIA has per Connector register to govern the Pin Assignment of each Type-C Connector. For example, DFLEXPA1.DPPATC0 is used to govern the Pin Assignment of Type-C Connector 0. The Type-C Connector number (e.g. “0” in register DPPATC0) is logical number.

DWord	Bit	Description
0	31:28	**Displayport Pin Assignment for Type-C Connector 15** Similar to register DFLEXPA2.DPPATC8 but this register is for Type-C Connector 15.
	27:24	**Displayport Pin Assignment for Type-C Connector 14** Similar to register DFLEXPA2.DPPATC8 but this register is for Type-C Connector 14.
	23:20	**Displayport Pin Assignment for Type-C Connector 13** Similar to register DFLEXPA2.DPPATC8 but this register is for Type-C Connector 13.
	19:16	**Displayport Pin Assignment for Type-C Connector 12** Similar to register DFLEXPA2.DPPATC8 but this register is for Type-C Connector 12.
	15:12	**Displayport Pin Assignment for Type-C Connector 11** Similar to register DFLEXPA2.DPPATC8 but this register is for Type-C Connector 11.
	11:8	**Displayport Pin Assignment for Type-C Connector 10** Similar to register DFLEXPA2.DPPATC8 but this register is for Type-C Connector 10.
	7:4	**Displayport Pin Assignment for Type-C Connector 9** Similar to register DFLEXPA2.DPPATC8 but this register is for Type-C Connector 9.
	3:0	**Displayport Pin Assignment for Type-C Connector 8** Display Port Pin Assignment for Type-C Connector 8 (DPPATC8): 0000 : No Pin Assignment (For Non Type-C DP) 0001 : Pin Assignment A 0010 : Pin Assignment B 0011 : Pin Assignment C 0100 : Pin Assignment D

PORT_TX_DFLEXPA2 - PORT_TX_DFLEXPA2		
		0101 : Pin Assignment E 0110 : Pin Assignment F 0111-1111 : Reserved

PORT_TX_DFLEXPCPMS1

PORT_TX_DFLEXPCPMS1 - PORT_TX_DFLEXPCPMS1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	soft
Address:	1634A0h-1634A3h
Name:	PORT_TX_DFLEXPCPMS1
ShortName:	PORT_TX_DFLEXPCPMS1
Power:	PG0
Reset:	soft

THIS REGISTER IS ADDED FOR STANDALONE TESTING PURPOSE ONLY!
Dynamic FlexIO Owner's Lane Enable

DWord	Bit	Description
0	31:28	**Combo Port 7 Next Phy Combo Port Mode Select (CP0NPCPMS):** Similar to register DFLEXNPCPMS1.CP0NPCPMS but this register is for Combo Port 7.
	27:24	**Combo Port 6 Next Phy Combo Port Mode Select (CP0NPCPMS):** Similar to register DFLEXNPCPMS1.CP0NPCPMS but this register is for Combo Port 6.
	23:20	**Combo Port 5 Next Phy Combo Port Mode Select (CP0NPCPMS):** Similar to register DFLEXNPCPMS1.CP0NPCPMS but this register is for Combo Port 5.
	19:16	**Combo Port 4 Next Phy Combo Port Mode Select (CP0NPCPMS):** Similar to register DFLEXNPCPMS1.CP0NPCPMS but this register is for Combo Port 4.
	15:12	**Combo Port 3 Next Phy Combo Port Mode Select (CP0NPCPMS):** Similar to register DFLEXNPCPMS1.CP0NPCPMS but this register is for Combo Port 3.
	11:8	**Combo Port 2 Next Phy Combo Port Mode Select (CP0NPCPMS):** Similar to register DFLEXNPCPMS1.CP0NPCPMS but this register is for Combo Port 2.
	7:4	**Combo Port 1 Next Phy Combo Port Mode Select (CP0NPCPMS):** The Combo Port number is logical. It's not physical lane numbers. 0h: Port Mode is NoOwner_USB3. FIA will keep the Lane in Reset state. PhyMode=USB3 1h: Port Mode is Owner 1 (default owner) 2h: Port Mode is Owner 2 3h: Port Mode is Owner 3 4h: Port Mode is Owner 4 5h: Port Mode is Owner 5 6h-Fh: Reserved Others: Reserved

PORT_TX_DFLEXPCPMS1 - PORT_TX_DFLEXPCPMS1		
		SW mode: SW writes to these bits to control the Combo Port's mode. This register governs the Phy status tracking handling that could be different for different controller. HW mode: These bits have no impact to HW when written. The reset default is dependent on the internal HW mux select bits though it's being indicated as soft-straps. The mux select bits retain their context across Sx and will be reloaded back into this field. Register Attribute: Static Implementation Note: If this register is programmed to a value correspond to the Alternate Protocol that is disabled by the fuse (refer to FC1.*APDF), the effective value used by the Type-C Switching logic is 0h, i.e. NoOwner_USB3 Note: For ICL: Owner 1 is USB3 Owner 2 is TBT Owner 3 is DP/HDMI Owner 4 is HTI
	3:0	**Combo Port 0 Next Phy Combo Port Mode Select (CP0NPCPMS):** The Combo Port number is logical. It's not physical lane numbers. 0h: Port Mode is NoOwner_USB3. FIA will keep the Lane in Reset state. PhyMode=USB3 1h: Port Mode is Owner 1 (default owner) 2h: Port Mode is Owner 2 3h: Port Mode is Owner 3 4h: Port Mode is Owner 4 5h: Port Mode is Owner 5 6h-Fh: Reserved Others: Reserved SW mode: SW writes to these bits to control the Combo Port's mode. This register governs the Phy status tracking handling that could be different for different controller. HW mode: These bits have no impact to HW when written. The reset default is dependent on the internal HW mux select bits though it's being indicated as soft-straps. The mux select bits retain their context across Sx and will be reloaded back into this field. Register Attribute: Static Implementation Note: If this register is programmed to a value correspond to the Alternate Protocol that is disabled by the fuse (refer to FC1.*APDF), the effective value used by the Type-C Switching logic is 0h, i.e. NoOwner_USB3 Note: For ICL: Owner 1 is USB3 Owner 2 is TBT Owner 3 is DP/HDMI Owner 4 is HTI

PORT_TX_DFLEXPCPROE1

PORT_TX_DFLEXPCPROE1 - PORT_TX_DFLEXPCPROE1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	soft
Address:	163450h-163453h
Name:	PORT_TX_DFLEXPCPROE1
ShortName:	PORT_TX_DFLEXPCPROE1
Power:	PG0
Reset:	soft

PD FW writes to this register bits to override the Combo Port reset to assertion, and clear this bit to remove the override, as part of the Swithing flow.

DWord	Bit	Description
0	31	**Combo Port 31 Phy Combo Port Reset Override Enable** Similar to register DFLEXPCPROE1.CP0PCPROE but this register is for Type-C Connector 31.
	30	**Combo Port 30 Phy Combo Port Reset Override Enable** Similar to register DFLEXPCPROE1.CP0PCPROE but this register is for Type-C Connector 30.
	29	**Combo Port 29 Phy Combo Port Reset Override Enable** Similar to register DFLEXPCPROE1.CP0PCPROE but this register is for Type-C Connector 29.
	28	**Combo Port 28 Phy Combo Port Reset Override Enable** Similar to register DFLEXPCPROE1.CP0PCPROE but this register is for Type-C Connector 28.
	27	**Combo Port 27 Phy Combo Port Reset Override Enable** Similar to register DFLEXPCPROE1.CP0PCPROE but this register is for Type-C Connector 27.
	26	**Combo Port 26 Phy Combo Port Reset Override Enable** Similar to register DFLEXPCPROE1.CP0PCPROE but this register is for Type-C Connector 26.
	25	**Combo Port 25 Phy Combo Port Reset Override Enable** Similar to register DFLEXPCPROE1.CP0PCPROE but this register is for Type-C Connector 25.
	24	**Combo Port 24 Phy Combo Port Reset Override Enable** Similar to register DFLEXPCPROE1.CP0PCPROE but this register is for Type-C Connector 24.
	23	**Combo Port 23 Phy Combo Port Reset Override Enable** Similar to register DFLEXPCPROE1.CP0PCPROE but this register is for Type-C Connector 23.
	22	**Combo Port 22 Phy Combo Port Reset Override Enable** Similar to register DFLEXPCPROE1.CP0PCPROE but this register is for Type-C Connector 22.
	21	**Combo Port 21 Phy Combo Port Reset Override Enable**

PORT_TX_DFLEXPCPROE1 - PORT_TX_DFLEXPCPROE1		
		Similar to register DFLEXPCPROE1.CP0PCPROE but this register is for Type-C Connector 21.
	20	**Combo Port 20 Phy Combo Port Reset Override Enable** Similar to register DFLEXPCPROE1.CP0PCPROE but this register is for Type-C Connector 20.
	19	**Combo Port 19 Phy Combo Port Reset Override Enable** Similar to register DFLEXPCPROE1.CP0PCPROE but this register is for Type-C Connector 19.
	18	**Combo Port 18 Phy Combo Port Reset Override Enable** Similar to register DFLEXPCPROE1.CP0PCPROE but this register is for Type-C Connector 18.
	17	**Combo Port 17 Phy Combo Port Reset Override Enable** Similar to register DFLEXPCPROE1.CP0PCPROE but this register is for Type-C Connector 17.
	16	**Combo Port 16 Phy Combo Port Reset Override Enable** Similar to register DFLEXPCPROE1.CP0PCPROE but this register is for Type-C Connector 16.
	15	**Combo Port 15 Phy Combo Port Reset Override Enable** Similar to register DFLEXPCPROE1.CP0PCPROE but this register is for Type-C Connector 15.
	14	**Combo Port 14 Phy Combo Port Reset Override Enable** Similar to register DFLEXPCPROE1.CP0PCPROE but this register is for Type-C Connector 14.
	13	**Combo Port 13 Phy Combo Port Reset Override Enable** Similar to register DFLEXPCPROE1.CP0PCPROE but this register is for Type-C Connector 13.
	12	**Combo Port 12 Phy Combo Port Reset Override Enable** Similar to register DFLEXPCPROE1.CP0PCPROE but this register is for Type-C Connector 12.
	11	**Combo Port 11 Phy Combo Port Reset Override Enable** Similar to register DFLEXPCPROE1.CP0PCPROE but this register is for Type-C Connector 11.
	10	**Combo Port 10 Phy Combo Port Reset Override Enable** Similar to register DFLEXPCPROE1.CP0PCPROE but this register is for Type-C Connector 10.
	9	**Combo Port 9 Phy Combo Port Reset Override Enable** Similar to register DFLEXPCPROE1.CP0PCPROE but this register is for Type-C Connector 9.
	8	**Combo Port 8 Phy Combo Port Reset Override Enable** Similar to register DFLEXPCPROE1.CP0PCPROE but this register is for Type-C Connector 8.
	7	**Combo Port 7 Phy Combo Port Reset Override Enable** Similar to register DFLEXPCPROE1.CP0PCPROE but this register is for Type-C Connector 7.
	6	**Combo Port 6 Phy Combo Port Reset Override Enable** Similar to register DFLEXPCPROE1.CP0PCPROE but this register is for Type-C Connector 6.
	5	**Combo Port 5 Phy Combo Port Reset Override Enable** Similar to register DFLEXPCPROE1.CP0PCPROE but this register is for Type-C Connector 5.
	4	**Combo Port 4 Phy Combo Port Reset Override Enable** Similar to register DFLEXPCPROE1.CP0PCPROE but this register is for Type-C Connector 4.
	3	**Combo Port 3 Phy Combo Port Reset Override Enable** Similar to register DFLEXPCPROE1.CP0PCPROE but this register is for Type-C Connector 3.
	2	**Combo Port 2 Phy Combo Port Reset Override Enable** Similar to register DFLEXPCPROE1.CP0PCPROE but this register is for Type-C Connector 2.
	1	**Combo Port 1 Phy Combo Port Reset Override Enable**

		Similar to register DFLEXPCPROE1.CP0PCPROE but this register is for Type-C Connector 1.
	0	**Combo Port 0 Phy Combo Port Reset Override Enable** PD FW writes '1' to this bit to tell DP Driver that it had put the FIA and PHY into DP PHY Mode and it's safe now for DP Driver to proceed to bring up the DP Controller. Once DP Driver poll a value '1' in this register, DP Driver write '0' to clear this bit for PD FW to use it in the next round.

Value	Name
0b	Port reset is not overridden
1b	Port reset is overriden to asserted

PORT_TX_DFLEXPCPROIP1

PORT_TX_DFLEXPCPROIP1 - PORT_TX_DFLEXPCPROIP1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	soft
Address:	163458h-16345Bh
Name:	PORT_TX_DFLEXPCPROIP1
ShortName:	PORT_TX_DFLEXPCPROIP1
Power:	PG0
Reset:	soft

HW set this bit to '1' when PD FW set the PCPROE bit in DFLEXPCPROE* register to '1'. HW clear this bit to '0' after PD FW clear PCPROE bit to '0' and FIA dFLEX logic had ensured that the tracking of phystatus tracking is settle down at the desired state.

DWord	Bit	Description
0	31	**Combo Port 31 Phy Combo Port Reset Override In Progress (CP31PCPROIP)** Similar to register DFLEXPCPROIP1.CP0PCPROIP but this register is for Combo Port 31.
	30	**Combo Port 30 Phy Combo Port Reset Override In Progress (CP31PCPROIP)** Similar to register DFLEXPCPROIP1.CP0PCPROIP but this register is for Combo Port 30.
	29	**Combo Port 29 Phy Combo Port Reset Override In Progress (CP31PCPROIP)** Similar to register DFLEXPCPROIP1.CP0PCPROIP but this register is for Combo Port 29.
	28	**Combo Port 28 Phy Combo Port Reset Override In Progress (CP31PCPROIP)** Similar to register DFLEXPCPROIP1.CP0PCPROIP but this register is for Combo Port 28.
	27	**Combo Port 27 Phy Combo Port Reset Override In Progress (CP31PCPROIP)** Similar to register DFLEXPCPROIP1.CP0PCPROIP but this register is for Combo Port 27.
	26	**Combo Port 26 Phy Combo Port Reset Override In Progress (CP31PCPROIP)** Similar to register DFLEXPCPROIP1.CP0PCPROIP but this register is for Combo Port 26.
	25	**Combo Port 25 Phy Combo Port Reset Override In Progress (CP31PCPROIP)** Similar to register DFLEXPCPROIP1.CP0PCPROIP but this register is for Combo Port 25.
	24	**Combo Port 24 Phy Combo Port Reset Override In Progress (CP31PCPROIP)** Similar to register DFLEXPCPROIP1.CP0PCPROIP but this register is for Combo Port 24.
	23	**Combo Port 23 Phy Combo Port Reset Override In Progress (CP31PCPROIP)** Similar to register DFLEXPCPROIP1.CP0PCPROIP but this register is for Combo Port 23.
	22	**Combo Port 22 Phy Combo Port Reset Override In Progress (CP31PCPROIP)** Similar to register DFLEXPCPROIP1.CP0PCPROIP but this register is for Combo Port 22.

PORT_TX_DFLEXPCPROIP1 - PORT_TX_DFLEXPCPROIP1		
	21	**Combo Port 21 Phy Combo Port Reset Override In Progress (CP31PCPROIP)** Similar to register DFLEXPCPROIP1.CP0PCPROIP but this register is for Combo Port 21.
	20	**Combo Port 20 Phy Combo Port Reset Override In Progress (CP31PCPROIP)** Similar to register DFLEXPCPROIP1.CP0PCPROIP but this register is for Combo Port 20.
	19	**Combo Port 19 Phy Combo Port Reset Override In Progress (CP31PCPROIP)** Similar to register DFLEXPCPROIP1.CP0PCPROIP but this register is for Combo Port 19.
	18	**Combo Port 18 Phy Combo Port Reset Override In Progress (CP31PCPROIP)** Similar to register DFLEXPCPROIP1.CP0PCPROIP but this register is for Combo Port 18.
	17	**Combo Port 17 Phy Combo Port Reset Override In Progress (CP31PCPROIP)** Similar to register DFLEXPCPROIP1.CP0PCPROIP but this register is for Combo Port 17.
	16	**Combo Port 16 Phy Combo Port Reset Override In Progress (CP31PCPROIP)** Similar to register DFLEXPCPROIP1.CP0PCPROIP but this register is for Combo Port 16.
	15	**Combo Port 15 Phy Combo Port Reset Override In Progress (CP31PCPROIP)** Similar to register DFLEXPCPROIP1.CP0PCPROIP but this register is for Combo Port 15.
	14	**Combo Port 14 Phy Combo Port Reset Override In Progress (CP31PCPROIP)** Similar to register DFLEXPCPROIP1.CP0PCPROIP but this register is for Combo Port 14.
	13	**Combo Port 13 Phy Combo Port Reset Override In Progress (CP31PCPROIP)** Similar to register DFLEXPCPROIP1.CP0PCPROIP but this register is for Combo Port 13.
	12	**Combo Port 12 Phy Combo Port Reset Override In Progress (CP31PCPROIP)** Similar to register DFLEXPCPROIP1.CP0PCPROIP but this register is for Combo Port 12.
	11	**Combo Port 11 Phy Combo Port Reset Override In Progress (CP31PCPROIP)** Similar to register DFLEXPCPROIP1.CP0PCPROIP but this register is for Combo Port 11.
	10	**Combo Port 10 Phy Combo Port Reset Override In Progress (CP31PCPROIP)** Similar to register DFLEXPCPROIP1.CP0PCPROIP but this register is for Combo Port 10.
	9	**Combo Port 9 Phy Combo Port Reset Override In Progress (CP31PCPROIP)** Similar to register DFLEXPCPROIP1.CP0PCPROIP but this register is for Combo Port 9.
	8	**Combo Port 8 Phy Combo Port Reset Override In Progress (CP31PCPROIP)** Similar to register DFLEXPCPROIP1.CP0PCPROIP but this register is for Combo Port 8.
	7	**Combo Port 7 Phy Combo Port Reset Override In Progress (CP31PCPROIP)** Similar to register DFLEXPCPROIP1.CP0PCPROIP but this register is for Combo Port 7.
	6	**Combo Port 6 Phy Combo Port Reset Override In Progress (CP31PCPROIP)** Similar to register DFLEXPCPROIP1.CP0PCPROIP but this register is for Combo Port 6.
	5	**Combo Port 5 Phy Combo Port Reset Override In Progress (CP31PCPROIP)** Similar to register DFLEXPCPROIP1.CP0PCPROIP but this register is for Combo Port 5.
	4	**Combo Port 4 Phy Combo Port Reset Override In Progress (CP31PCPROIP)** Similar to register DFLEXPCPROIP1.CP0PCPROIP but this register is for Combo Port 4.
	3	**Combo Port 3 Phy Combo Port Reset Override In Progress (CP31PCPROIP)** Similar to register DFLEXPCPROIP1.CP0PCPROIP but this register is for Combo Port 3.
	2	**Combo Port 2 Phy Combo Port Reset Override In Progress (CP31PCPROIP)** Similar to register DFLEXPCPROIP1.CP0PCPROIP but this register is for Combo Port 2.

PORT_TX_DFLEXPCPROIP1 - PORT_TX_DFLEXPCPROIP1

	1	**Combo Port 1 Phy Combo Port Reset Override In Progress (CP31PCPROIP)** Similar to register DFLEXPCPROIP1.CP0PCPROIP but this register is for Combo Port 1.
	0	**Combo Port 0 Phy Combo Port Reset Override In Progress (CP31PCPROIP)** HW set this bit to '1' when PD FW set the PCPROE bit in DFLEXPCPROE* register to '1'. HW clear this bit to '0' after PD FW clear PCPROE bit to '0' and FIA dFLEX logic had ensure that the tracking of phystatus tracking is settle down at the desired state.

Value	Name
0b	Lane Reset Override is in not process or it is done
1b	Lane Reset Override is in process.

PORT_TX_DFLEXPLL1S

PORT_TX_DFLEXPLL1S - PORT_TX_DFLEXPLL1S	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	soft
Address:	1634C0h-1634C3h
Name:	PORT_TX_DFLEXPLL1S
ShortName:	PORT_TX_DFLEXPLL1S
Power:	PG0
Reset:	soft

This register reflects the current status of PHY PLL1 based on the pllen-pllok handshake between FIA and PHY.

DWord	Bit	Description
0	31:16	**Reserved**
	15	**PLL1 status for Type-C connector 15** Similar to register DFLEXPLL1S.PLL1STC0 but this register is for Type-C Connector 15.
	14	**PLL1 status for Type-C connector 14** Similar to register DFLEXPLL1S.PLL1STC0 but this register is for Type-C Connector 14.
	13	**PLL1 status for Type-C connector 13** Similar to register DFLEXPLL1S.PLL1STC0 but this register is for Type-C Connector 13.
	12	**PLL1 status for Type-C connector 12** Similar to register DFLEXPLL1S.PLL1STC0 but this register is for Type-C Connector 12.
	11	**PLL1 status for Type-C connector 11** Similar to register DFLEXPLL1S.PLL1STC0 but this register is for Type-C Connector 11.
	10	**PLL1 status for Type-C connector 10** Similar to register DFLEXPLL1S.PLL1STC0 but this register is for Type-C Connector 10.
	9	**PLL1 status for Type-C connector 9** Similar to register DFLEXPLL1S.PLL1STC0 but this register is for Type-C Connector 9.
	8	**PLL1 status for Type-C connector 8** Similar to register DFLEXPLL1S.PLL1STC0 but this register is for Type-C Connector 8.
	7	**PLL1 status for Type-C connector 7** Similar to register DFLEXPLL1S.PLL1STC0 but this register is for Type-C Connector 7.
	6	**PLL1 status for Type-C connector 6** Similar to register DFLEXPLL1S.PLL1STC0 but this register is for Type-C Connector 6.

PORT_TX_DFLEXPLL1S - PORT_TX_DFLEXPLL1S

	5	**PLL1 status for Type-C connector 5** Similar to register DFLEXPLL1S.PLL1STC0 but this register is for Type-C Connector 5.
	4	**PLL1 status for Type-C connector 4** Similar to register DFLEXPLL1S.PLL1STC0 but this register is for Type-C Connector 4.
	3	**PLL1 status for Type-C connector 3** Similar to register DFLEXPLL1S.PLL1STC0 but this register is for Type-C Connector 3.
	2	**PLL1 status for Type-C connector 2** Similar to register DFLEXPLL1S.PLL1STC0 but this register is for Type-C Connector 2.
	1	**PLL1 status for Type-C connector 1** Similar to register DFLEXPLL1S.PLL1STC0 but this register is for Type-C Connector 1.
	0	**PLL1 status for Type-C connector 0** This register reflects the current status of PHY PLL1 based on the pllen-pllok handshake between FIA and PHY. It's '0' when pllen=pllok=0. It's '1' otherwise. This register is N/A in non PHY.

Value	Name
0b	PLL1 is disabled
1b	PLL1 is not disabled

PORT_TX_DFLEXPLL2S

PORT_TX_DFLEXPLL2S - PORT_TX_DFLEXPLL2S	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	soft
Address:	1634C4h-1634C7h
Name:	PORT_TX_DFLEXPLL2S
ShortName:	PORT_TX_DFLEXPLL2S
Power:	PG0
Reset:	soft

This register reflects the current status of PHY PLL2 based on the pllen-pllok handshake between FIA and PHY.

DWord	Bit	Description
0	31:16	**Reserved**
	15	**PLL2 status for Type-C connector 15** Similar to register DFLEXPLL2S.PLL2STC0 but this register is for Type-C Connector 15.
	14	**PLL2 status for Type-C connector 14** Similar to register DFLEXPLL2S.PLL2STC0 but this register is for Type-C Connector 14.
	13	**PLL2 status for Type-C connector 13** Similar to register DFLEXPLL2S.PLL2STC0 but this register is for Type-C Connector 13.
	12	**PLL2 status for Type-C connector 12** Similar to register DFLEXPLL2S.PLL2STC0 but this register is for Type-C Connector 12.
	11	**PLL2 status for Type-C connector 11** Similar to register DFLEXPLL2S.PLL2STC0 but this register is for Type-C Connector 11.
	10	**PLL2 status for Type-C connector 10** Similar to register DFLEXPLL2S.PLL2STC0 but this register is for Type-C Connector 10.
	9	**PLL2 status for Type-C connector 9** Similar to register DFLEXPLL2S.PLL2STC0 but this register is for Type-C Connector 9.
	8	**PLL2 status for Type-C connector 8** Similar to register DFLEXPLL2S.PLL2STC0 but this register is for Type-C Connector 8.
	7	**PLL2 status for Type-C connector 7** Similar to register DFLEXPLL2S.PLL2STC0 but this register is for Type-C Connector 7.
	6	**PLL2 status for Type-C connector 6** Similar to register DFLEXPLL2S.PLL2STC0 but this register is for Type-C Connector 6.

PORT_TX_DFLEXPLL2S - PORT_TX_DFLEXPLL2S		
	5	**PLL2 status for Type-C connector 5** Similar to register DFLEXPLL2S.PLL2STC0 but this register is for Type-C Connector 5.
	4	**PLL2 status for Type-C connector 4** Similar to register DFLEXPLL2S.PLL2STC0 but this register is for Type-C Connector 4.
	3	**PLL2 status for Type-C connector 3** Similar to register DFLEXPLL2S.PLL2STC0 but this register is for Type-C Connector 3.
	2	**PLL2 status for Type-C connector 2** Similar to register DFLEXPLL2S.PLL2STC0 but this register is for Type-C Connector 2.
	1	**PLL2 status for Type-C connector 1** Similar to register DFLEXPLL2S.PLL2STC0 but this register is for Type-C Connector 1.
	0	**PLL2 status for Type-C connector 0** This register reflects the current status of PHY PLL2 based on the pllen-pllok handshake between FIA and PHY. It's '0' when pllen=pllok=0. It's '1' otherwise. This register is N/A in non PHY.

Value	Name
0b	PLL2 is disabled
1b	PLL2 is not disabled

PORT_TX_DFLEXUSSRTOE

PORT_TX_DFLEXUSSRTOE - PORT_TX_DFLEXUSSRTOE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	soft
Address:	163460h-163463h
Name:	PORT_TX_DFLEXUSSRTOE
ShortName:	PORT_TX_DFLEXUSSRTOE
Power:	PG0
Reset:	soft

PD FW set this register bit to '1' to enable the USB Safe State Rx Termination Override as part of the Controller Enter Safe Mode flow.
PD FW set this bit to '0' to disable USB Safe State Rx Termination Override as part of the FIA Change Mode flow.

DWord	Bit	Description
0	31	**Combo Port 31 USB Safe State Rx Termination Override Enable** Similar to register DFLEXUSSRTOE1.CP0USSRTOE but this register is for Combo Port 31.
	30	**Combo Port 30 USB Safe State Rx Termination Override Enable** Similar to register DFLEXUSSRTOE1.CP0USSRTOE but this register is for Combo Port 30.
	29	**Combo Port 29 USB Safe State Rx Termination Override Enable** Similar to register DFLEXUSSRTOE1.CP0USSRTOE but this register is for Combo Port 29.
	28	**Combo Port 28 USB Safe State Rx Termination Override Enable** Similar to register DFLEXUSSRTOE1.CP0USSRTOE but this register is for Combo Port 28.
	27	**Combo Port 27 USB Safe State Rx Termination Override Enable** Similar to register DFLEXUSSRTOE1.CP0USSRTOE but this register is for Combo Port 27.
	26	**Combo Port 26 USB Safe State Rx Termination Override Enable** Similar to register DFLEXUSSRTOE1.CP0USSRTOE but this register is for Combo Port 26.
	25	**Combo Port 25 USB Safe State Rx Termination Override Enable** Similar to register DFLEXUSSRTOE1.CP0USSRTOE but this register is for Combo Port 25.
	24	**Combo Port 24 USB Safe State Rx Termination Override Enable** Similar to register DFLEXUSSRTOE1.CP0USSRTOE but this register is for Combo Port 24.
	23	**Combo Port 23 USB Safe State Rx Termination Override Enable** Similar to register DFLEXUSSRTOE1.CP0USSRTOE but this register is for Combo Port 23.
	22	**Combo Port 22 USB Safe State Rx Termination Override Enable** Similar to register DFLEXUSSRTOE1.CP0USSRTOE but this register is for Combo Port 22.

PORT_TX_DFLEXUSSRTOE - PORT_TX_DFLEXUSSRTOE		
	21	**Combo Port 21 USB Safe State Rx Termination Override Enable** Similar to register DFLEXUSSRTOE1.CP0USSRTOE but this register is for Combo Port 21.
	20	**Combo Port 20 USB Safe State Rx Termination Override Enable** Similar to register DFLEXUSSRTOE1.CP0USSRTOE but this register is for Combo Port 20.
	19	**Combo Port 19 USB Safe State Rx Termination Override Enable** Similar to register DFLEXUSSRTOE1.CP0USSRTOE but this register is for Combo Port 19.
	18	**Combo Port 18 USB Safe State Rx Termination Override Enable** Similar to register DFLEXUSSRTOE1.CP0USSRTOE but this register is for Combo Port 18.
	17	**Combo Port 17 USB Safe State Rx Termination Override Enable** Similar to register DFLEXUSSRTOE1.CP0USSRTOE but this register is for Combo Port 17.
	16	**Combo Port 16 USB Safe State Rx Termination Override Enable** Similar to register DFLEXUSSRTOE1.CP0USSRTOE but this register is for Combo Port 16.
	15	**Combo Port 15 USB Safe State Rx Termination Override Enable** Similar to register DFLEXUSSRTOE1.CP0USSRTOE but this register is for Combo Port 15.
	14	**Combo Port 14 USB Safe State Rx Termination Override Enable** Similar to register DFLEXUSSRTOE1.CP0USSRTOE but this register is for Combo Port 14.
	13	**Combo Port 13 USB Safe State Rx Termination Override Enable** Similar to register DFLEXUSSRTOE1.CP0USSRTOE but this register is for Combo Port 13.
	12	**Combo Port 12 USB Safe State Rx Termination Override Enable** Similar to register DFLEXUSSRTOE1.CP0USSRTOE but this register is for Combo Port 12.
	11	**Combo Port 11 USB Safe State Rx Termination Override Enable** Similar to register DFLEXUSSRTOE1.CP0USSRTOE but this register is for Combo Port 11.
	10	**Combo Port 10 USB Safe State Rx Termination Override Enable** Similar to register DFLEXUSSRTOE1.CP0USSRTOE but this register is for Combo Port 10.
	9	**Combo Port 9 USB Safe State Rx Termination Override Enable** Similar to register DFLEXUSSRTOE1.CP0USSRTOE but this register is for Combo Port 9.
	8	**Combo Port 8 USB Safe State Rx Termination Override Enable** Similar to register DFLEXUSSRTOE1.CP0USSRTOE but this register is for Combo Port 8.
	7	**Combo Port 7 USB Safe State Rx Termination Override Enable** Similar to register DFLEXUSSRTOE1.CP0USSRTOE but this register is for Combo Port 7.
	6	**Combo Port 6 USB Safe State Rx Termination Override Enable** Similar to register DFLEXUSSRTOE1.CP0USSRTOE but this register is for Combo Port 6.
	5	**Combo Port 5 USB Safe State Rx Termination Override Enable** Similar to register DFLEXUSSRTOE1.CP0USSRTOE but this register is for Combo Port 5.
	4	**Combo Port 4 USB Safe State Rx Termination Override Enable** Similar to register DFLEXUSSRTOE1.CP0USSRTOE but this register is for Combo Port 4.
	3	**Combo Port 3 USB Safe State Rx Termination Override Enable** Similar to register DFLEXUSSRTOE1.CP0USSRTOE but this register is for Combo Port 3.
	2	**Combo Port 2 USB Safe State Rx Termination Override Enable** Similar to register DFLEXUSSRTOE1.CP0USSRTOE but this register is for Combo Port 2.

PORT_TX_DFLEXUSSRTOE - PORT_TX_DFLEXUSSRTOE		
	1	**Combo Port 1 USB Safe State Rx Termination Override Enable** Similar to register DFLEXUSSRTOE1.CP0USSRTOE but this register is for Combo Port 1.
	0	**Combo Port 0 USB Safe State Rx Termination Override Enable** PD FW set this bit to '1' to enable the USB Safe State Rx Termination Override as part of the Controller Enter Safe Mode flow. PD FW set this bit to '0' to disable USB Safe State Rx Termination Override as part of the FIA Change Mode flow.

Value	Name
0b	Disable the USB Safe State Rx Termination Override
1b	Enable the USB Safe State Rx Termination Override

PORT_TX_DW1

PORT_TX_DW1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
DWord	**Bit**	**Description**
0	31:8	**Reserved** Format: PBZ The values in this field must not be changed. Use read/modify/write to update this register.
	7	**o_iref_config** ICOMP Config bit from COMP routed to Txana
	6:5	**o_iref_ctrl** control to change the ratio of tx iboost
	4:3	**o_tx_slew_ctrl** Used for MIPI HSTX Slew rate control config
	2	**o_vref_low_en** LDO Feedback path enable for low vref
	1	**o_vref_hi_en** LDO Feedback path enable for hi vref
	0	**o_vref_nom_en** LDO Feedback path enable for nominal vref

PORT_TX_DW2

PORT_TX_DW2	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	162688h-16268Bh
Name:	PORT_TX_DW2_GRP_A
ShortName:	PORT_TX_DW2_GRP_A
Power:	PG0
Reset:	global
Address:	162888h-16288Bh
Name:	PORT_TX_DW2_LN0_A
ShortName:	PORT_TX_DW2_LN0_A
Power:	PG0
Reset:	global
Address:	162988h-16298Bh
Name:	PORT_TX_DW2_LN1_A
ShortName:	PORT_TX_DW2_LN1_A
Power:	PG0
Reset:	global
Address:	162A88h-162A8Bh
Name:	PORT_TX_DW2_LN2_A
ShortName:	PORT_TX_DW2_LN2_A
Power:	PG0
Reset:	global
Address:	162B88h-162B8Bh
Name:	PORT_TX_DW2_LN3_A
ShortName:	PORT_TX_DW2_LN3_A

PORT_TX_DW2

Power:	PG0
Reset:	global

Address:	162388h-16238Bh
Name:	PORT_TX_DW2_AUX_A
ShortName:	PORT_TX_DW2_AUX_A
Power:	PG0
Reset:	global

Address:	6C688h-6C68Bh
Name:	PORT_TX_DW2_GRP_B
ShortName:	PORT_TX_DW2_GRP_B
Power:	PG0
Reset:	global

Address:	6C888h-6C88Bh
Name:	PORT_TX_DW2_LN0_B
ShortName:	PORT_TX_DW2_LN0_B
Power:	PG0
Reset:	global

Address:	6C988h-6C98Bh
Name:	PORT_TX_DW2_LN1_B
ShortName:	PORT_TX_DW2_LN1_B
Power:	PG0
Reset:	global

Address:	6CA88h-6CA8Bh
Name:	PORT_TX_DW2_LN2_B
ShortName:	PORT_TX_DW2_LN2_B
Power:	PG0
Reset:	global

Address:	6CB88h-6CB8Bh
Name:	PORT_TX_DW2_LN3_B
ShortName:	PORT_TX_DW2_LN3_B

PORT_TX_DW2

Power:	PG0
Reset:	global
Address:	6C388h-6C38Bh
Name:	PORT_TX_DW2_AUX_B
ShortName:	PORT_TX_DW2_AUX_B
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31:16	**Reserved** Format: PBZ The values in this field must not be changed. Use read/modify/write to update this register.
	15	**swing_sel upper** Swing_sel bit 3
	14	**cmnmode_sel** Select one of the weak common modes.
	13:11	**swing_sel lower** Default Value: 010b Select the voltage swing level. Note that this field has swing_sel bits 2:0 and bit 3 is in swing_sel upper, which is not adjacent.
	10:8	**frclatencyoptim** Enables forcing the latency optimized value for the FIFO.
	7:0	**Rcomp scalar** Default Value: 10011000b Also called Swing Scalar. Scalar to be applied to comp code to get required termination.

PORT_TX_DW4

PORT_TX_DW4	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	162690h-162693h
Name:	PORT_TX_DW4_GRP_A
ShortName:	PORT_TX_DW4_GRP_A
Power:	PG0
Reset:	global
Address:	162890h-162893h
Name:	PORT_TX_DW4_LN0_A
ShortName:	PORT_TX_DW4_LN0_A
Power:	PG0
Reset:	global
Address:	162990h-162993h
Name:	PORT_TX_DW4_LN1_A
ShortName:	PORT_TX_DW4_LN1_A
Power:	PG0
Reset:	global
Address:	162A90h-162A93h
Name:	PORT_TX_DW4_LN2_A
ShortName:	PORT_TX_DW4_LN2_A
Power:	PG0
Reset:	global
Address:	162B90h-162B93h
Name:	PORT_TX_DW4_LN3_A
ShortName:	PORT_TX_DW4_LN3_A

PORT_TX_DW4	
Power:	PG0
Reset:	global
Address:	162390h-162393h
Name:	PORT_TX_DW4_AUX_A
ShortName:	PORT_TX_DW4_AUX_A
Power:	PG0
Reset:	global
Address:	6C690h-6C693h
Name:	PORT_TX_DW4_GRP_B
ShortName:	PORT_TX_DW4_GRP_B
Power:	PG0
Reset:	global
Address:	6C890h-6C893h
Name:	PORT_TX_DW4_LN0_B
ShortName:	PORT_TX_DW4_LN0_B
Power:	PG0
Reset:	global
Address:	6C990h-6C993h
Name:	PORT_TX_DW4_LN1_B
ShortName:	PORT_TX_DW4_LN1_B
Power:	PG0
Reset:	global
Address:	6CA90h-6CA93h
Name:	PORT_TX_DW4_LN2_B
ShortName:	PORT_TX_DW4_LN2_B
Power:	PG0
Reset:	global
Address:	6CB90h-6CB93h
Name:	PORT_TX_DW4_LN3_B
ShortName:	PORT_TX_DW4_LN3_B

PORT_TX_DW4

Power:	PG0
Reset:	global
Address:	6C390h-6C393h
Name:	PORT_TX_DW4_AUX_B
ShortName:	PORT_TX_DW4_AUX_B
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31	**Loadgen Select**
	30:24	**Spare**
	23	**BS Comp Ovrd**
	22:18	**Rterm Limit** Default Value: 10000b
	17:12	**Post Cursor 1** o_txscaling_coeff[17:12]
	11:6	**Post Cursor 2** o_txscaling_coeff[11:6]
	5:0	**Cursor Coeff** Default Value: 011000b o_txscaling_coeff[5:0]

PORT_TX_DW5

PORT_TX_DW5	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	162694h-162697h
Name:	PORT_TX_DW5_GRP_A
ShortName:	PORT_TX_DW5_GRP_A
Power:	PG0
Reset:	global
Address:	162894h-162897h
Name:	PORT_TX_DW5_LN0_A
ShortName:	PORT_TX_DW5_LN0_A
Power:	PG0
Reset:	global
Address:	162994h-162997h
Name:	PORT_TX_DW5_LN1_A
ShortName:	PORT_TX_DW5_LN1_A
Power:	PG0
Reset:	global
Address:	162A94h-162A97h
Name:	PORT_TX_DW5_LN2_A
ShortName:	PORT_TX_DW5_LN2_A
Power:	PG0
Reset:	global
Address:	162B94h-162B97h
Name:	PORT_TX_DW5_LN3_A
ShortName:	PORT_TX_DW5_LN3_A

PORT_TX_DW5

Power:	PG0
Reset:	global
Address:	162394h-162397h
Name:	PORT_TX_DW5_AUX_A
ShortName:	PORT_TX_DW5_AUX_A
Power:	PG0
Reset:	global
Address:	6C694h-6C697h
Name:	PORT_TX_DW5_GRP_B
ShortName:	PORT_TX_DW5_GRP_B
Power:	PG0
Reset:	global
Address:	6C894h-6C897h
Name:	PORT_TX_DW5_LN0_B
ShortName:	PORT_TX_DW5_LN0_B
Power:	PG0
Reset:	global
Address:	6C994h-6C997h
Name:	PORT_TX_DW5_LN1_B
ShortName:	PORT_TX_DW5_LN1_B
Power:	PG0
Reset:	global
Address:	6CA94h-6CA97h
Name:	PORT_TX_DW5_LN2_B
ShortName:	PORT_TX_DW5_LN2_B
Power:	PG0
Reset:	global
Address:	6CB94h-6CB97h
Name:	PORT_TX_DW5_LN3_B
ShortName:	PORT_TX_DW5_LN3_B

PORT_TX_DW5

Power: PG0
Reset: global

Address: 6C394h-6C397h
Name: PORT_TX_DW5_AUX_B
ShortName: PORT_TX_DW5_AUX_B

Power: PG0
Reset: global

DWord	Bit	Description
0	31	**TX Training Enable** Value: 1b = enable; 0b = disable
	30	**Disable 2tap** ospare2[5] Value: 0b = Enable; 1b = Disable
	29	**Disable 3tap** ospare2[5] Value: 0b = Enable; 1b = Disable
	28:27	**Spare 28 27** ospare2[4:3]
	26	**Cursor Program** ospare2[2] Value: 0b = Enable; 1b = Disable
	25	**Coeff Polarity** ospare2[1] Value: 0b = Enable; 1b = Disable
	24	**Spare 24** ospare2[0]

PORT_TX_DW5		
	23:21	**Reserved** Format: MBZ
	20:18	**Scaling Mode Sel** Default Value: 010b
	17:16	**Decode Timer Sel** Default Value: 01b
	15:11	**CR Scaling Coef**
	10:6	**Spare 10 6** o_tx_vswing[10:6]
	5:3	**Rterm Select** o_tx_vswing[5:3]
	2:0	**Spare 2 0** o_tx_vswing[2:0]

PORT_TX_DW6

PORT_TX_DW6 - PORT_TX_DW6		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Access:	R/W	
Size (in bits):	32	
DWord	**Bit**	**Description**
0	31:8	**Reserved** Format: PBZ The values in this field must not be changed. Use read/modify/write to update this register.
	7	**o_func_ovrd_en** ovrd enable signal
	6:1	**o_ldo_ref_sel_cri** ovrd for ldo_ref_sel
	0	**o_ldo_bypass_cri** ovrd for ldo bypass

PORT_TX_DW7

PORT_TX_DW7	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	16269Ch-16269Fh
Name:	PORT_TX_DW7_GRP_A
ShortName:	PORT_TX_DW7_GRP_A
Power:	PG0
Reset:	global
Address:	16289Ch-16289Fh
Name:	PORT_TX_DW7_LN0_A
ShortName:	PORT_TX_DW7_LN0_A
Power:	PG0
Reset:	global
Address:	16299Ch-16299Fh
Name:	PORT_TX_DW7_LN1_A
ShortName:	PORT_TX_DW7_LN1_A
Power:	PG0
Reset:	global
Address:	162A9Ch-162A9Fh
Name:	PORT_TX_DW7_LN2_A
ShortName:	PORT_TX_DW7_LN2_A
Power:	PG0
Reset:	global
Address:	162B9Ch-162B9Fh
Name:	PORT_TX_DW7_LN3_A
ShortName:	PORT_TX_DW7_LN3_A

PORT_TX_DW7	
Power:	PG0
Reset:	global
Address:	16239Ch-16239Fh
Name:	PORT_TX_DW7_AUX_A
ShortName:	PORT_TX_DW7_AUX_A
Power:	PG0
Reset:	global
Address:	6C69Ch-6C69Fh
Name:	PORT_TX_DW7_GRP_B
ShortName:	PORT_TX_DW7_GRP_B
Power:	PG0
Reset:	global
Address:	6C89Ch-6C89Fh
Name:	PORT_TX_DW7_LN0_B
ShortName:	PORT_TX_DW7_LN0_B
Power:	PG0
Reset:	global
Address:	6C99Ch-6C99Fh
Name:	PORT_TX_DW7_LN1_B
ShortName:	PORT_TX_DW7_LN1_B
Power:	PG0
Reset:	global
Address:	6CA9Ch-6CA9Fh
Name:	PORT_TX_DW7_LN2_B
ShortName:	PORT_TX_DW7_LN2_B
Power:	PG0
Reset:	global
Address:	6CB9Ch-6CB9Fh
Name:	PORT_TX_DW7_LN3_B
ShortName:	PORT_TX_DW7_LN3_B

PORT_TX_DW7

Power:	PG0
Reset:	global
Address:	6C39Ch-6C39Fh
Name:	PORT_TX_DW7_AUX_B
ShortName:	PORT_TX_DW7_AUX_B
Power:	PG0
Reset:	global

DWord	Bit	Description
0	31	**Spare 31**
	30:24	**N Scalar** Default Value: 7Fh
	23:0	**Spare 23 0**

PORT_TX_FC2

PORT_TX_FC2 - PORT_TX_FC2	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	global
Address:	163204h-163207h
Name:	PORT_TX_FC2
ShortName:	PORT_TX_FC2
Power:	PG0
Reset:	global

This register is not reset by device 2 FLR.

DWord	Bit	Description
0	31:28	**Lane ownership fuse for lane7** Lane Ownership Fuse for Lane 7 (LOFL7): Similar to register FC2.LOFL0 but this register is for PHY Lane 7.
	27:24	**Lane ownership fuse for lane6** Lane Ownership Fuse for Lane 6 (LOFL6): Similar to register FC2.LOFL0 but this register is for PHY Lane 6.
	23:20	**Lane ownership fuse for lane5** Lane Ownership Fuse for Lane 3 (LOFL5): Similar to register FC2.LOFL0 but this register is for PHY Lane 5.
	19:16	**Lane ownership fuse for lane4** Lane Ownership Fuse for Lane 3 (LOFL4): Similar to register FC2.LOFL0 but this register is for PHY Lane 4.
	15:12	**Lane ownership fuse for lane3** Lane Ownership Fuse for Lane 3 (LOFL3): Similar to register FC2.LOFL0 but this register is for PHY Lane 3.
	11:8	**Lane ownership fuse for lane2** Lane Ownership Fuse for Lane 2 (LOFL2): Similar to register FC2.LOFL0 but this register is for PHY Lane 2.
	7:4	**Lane ownership fuse for lane1** “0h”: Statically assigned to NoOwner_USB3. FIA will keep the Lane in Reset state. PhyMode=USB3 “1h”: Statically assigned to Owner 1 of Lane 1 “2h”: Statically assigned to Owner 2 of Lane 1

PORT_TX_FC2 - PORT_TX_FC2		
		"3h": Statically assigned to Owner 3 of Lane 1 "4h": Statically assigned to Owner 4 of Lane 1 "5h": Statically assigned to Owner 5 of Lane 1 "6h-Dh": Reserved "Eh": Lane ownership is assigned based dFLEX for Lane 1 "Fh": Lane ownership is assigned based on the Lane Ownership Softstrap for Lane 1. The default value will reflect the fuse value once fuse pull is done. Unfused Part Default value: Fh Register Attribute: Static Note: For ICL: Owner 1 is USB3 Owner 2 is TBT Owner 3 is DP/HDMI Owner 4 is HTI
	3:0	**Lane ownership fuse for lane0** "0h": Statically assigned to NoOwner_USB3. FIA will keep the Lane in Reset state. PhyMode=USB3 "1h": Statically assigned to Owner 1 of Lane 0 "2h": Statically assigned to Owner 2 of Lane 0 "3h": Statically assigned to Owner 3 of Lane 0 "4h": Statically assigned to Owner 4 of Lane 0 "5h": Statically assigned to Owner 5 of Lane 0 "6h-Dh": Reserved "Eh": Lane ownership is assigned based dFLEX for Lane 0 "Fh": Lane ownership is assigned based on the Lane Ownership Softstrap for Lane 0. The default value will reflect the fuse value once fuse pull is done. Unfused Part Default value: Fh Register Attribute: Static Note: For ICL: Owner 1 is USB3 Owner 2 is TBT Owner 3 is DP/HDMI Owner 4 is HTI

POSH LRCA

POSH_LRCA - POSH LRCA	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	021B0h-021B3h
Name:	POSH LRCA
ShortName:	POSH_LRCA_RCSUNIT
Address:	181B0h-181B3h
Name:	POSH LRCA
ShortName:	POSH_LRCA_POCSUNIT
Address:	221B0h-221B3h
Name:	POSH LRCA
ShortName:	POSH_LRCA_BCSUNIT
Address:	1C01B0h-1C01B3h
Name:	POSH LRCA
ShortName:	POSH_LRCA_VCSUNIT0
Address:	1C41B0h-1C41B3h
Name:	POSH LRCA
ShortName:	POSH_LRCA_VCSUNIT1
Address:	1C81B0h-1C81B3h
Name:	POSH LRCA
ShortName:	POSH_LRCA_VECSUNIT0
Address:	1D01B0h-1D01B3h
Name:	POSH LRCA
ShortName:	POSH_LRCA_VCSUNIT2

POSH_LRCA - POSH LRCA

Address:	1D41B0h-1D41B3h
Name:	POSH LRCA
ShortName:	POSH_LRCA_VCSUNIT3

Address:	1D81B0h-1D81B3h
Name:	POSH LRCA
ShortName:	POSH_LRCA_VECSUNIT1

Address:	1E01B0h-1E01B3h
Name:	POSH LRCA
ShortName:	POSH_LRCA_VCSUNIT4

Address:	1E41B0h-1E41B3h
Name:	POSH LRCA
ShortName:	POSH_LRCA_VCSUNIT5

Address:	1E81B0h-1E81B3h
Name:	POSH LRCA
ShortName:	POSH_LRCA_VECSUNIT2

Address:	1F01B0h-1F01B3h
Name:	POSH LRCA
ShortName:	POSH_LRCA_VCSUNIT6

Address:	1F41B0h-1F41B3h
Name:	POSH LRCA
ShortName:	POSH_LRCA_VCSUNIT7

Address:	1F81B0h-1F81B3h
Name:	POSH LRCA
ShortName:	POSH_LRCA_VECSUNIT3

This register contains the LRCA address for the POSH pipe to which POCS does context save/restore. LRCA address programmed in this register is only effective when "POSH Enable" field is set in CTX_SR_CTL register. This register is not functional and must not be programmed for VideoCS, VideoEnhacementCS, BlitterCS.

DWord	Bit	Description

POSH_LRCA - POSH LRCA		
0	31:12	**POSH Logical Ring Context Address**
	11:0	**Reserved** Format: MBZ

Power Clock State Register

PWR_CLK_STATE - Power Clock State Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	020C8h
Name:	Render Power Clock State Register
ShortName:	R_PWR_CLK_STATE
Address:	220C8h
Name:	BCS Power Clock State Register
ShortName:	BCS_PWR_CLK_STATE
Address:	120C8h
Name:	VCS Power Clock State Register
ShortName:	VCS_PWR_CLK_STATE
Address:	1A0C8h
Name:	VECS Power Clock State Register
ShortName:	VECS_PWR_CLK_STATE

This register contains the mode selection for configuring render engine to attain desired performance and power requirements for a given context. This register is render context save/restored. This register must be initialized correctly when the context is submitted for the first time. This register is context save/restored as part of Exec-List context image in both Exec-List and Ring-Buffer mode of scheduling. This register contents are valid only when "Enable" bit [31] of the register is set.

Programming Notes
This register is only functional for RenderCS. This register must not be exercised in VideoCS, BlitterCS and VideoEnhancementCS.
This register must not be programmed directly through CPU MMIO cycle. **Exec-List Scheduling Mode:** Every context can have its own required render engine configuration by programming this register appropriately in the logical render context image in memory (LRCA) before submitting the context to the execlist submit port. This register must not be programmed using MI_LOAD_REGISTER_IMM command in ring buffer or in batch buffer.

DWord	Bit	Description

PWR_CLK_STATE - Power Clock State Register

0	31	**Power Clock State Enable** Format: U1 **Value** / **Name** / **Description** 0h / Power Clock State Disabled / No specific power state set, bits[30:0] are ignored. 1h / Power Clock State Enabled / Power Clock is set and bit[30:0] are valid and have the desired state.
	30:0	**Power Clock State** Format: **Power Clock State Format**

Power context Save Register for LPFC

LPCSR - Power context Save Register for LPFC		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	0B408h	

DWord	Bit	Description
0	31:10	**Reserved** Access: RO Reserved.
	9:0	**Power Context Save Request + Credits** Access: R/W Hardware Clear Bit[9]. Power Context Save Request. 1'b0: Power context save is not being requested (default). 1'b1: Power context save is being requested. Unit needs to self-clear this bit upon sampling. Bits[8:0]. QWord Credits for Power Context Save Request. Minimum Credits = 1: Unit may send 1 QWord pair (enough for first LRI at least). Maximum Credits = 511: Unit may send 511 QWord pairs. A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

PRE_CSC_GAMC_DATA

PRE_CSC_GAMC_DATA	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	4A488h-4A48Bh
Name:	Pipe Pre CSC Gamma Data
ShortName:	PRE_CSC_GAMC_DATA_A
Power:	PG1
Reset:	soft
Address:	4AC88h-4AC8Bh
Name:	Pipe Pre CSC Gamma Data
ShortName:	PRE_CSC_GAMC_DATA_B
Power:	PG2
Reset:	soft
Address:	4B488h-4B48Bh
Name:	Pipe Pre CSC Gamma Data
ShortName:	PRE_CSC_GAMC_DATA_C
Power:	PG2
Reset:	soft

Description

PRE_CSC_GAMC_INDEX and PRE_CSC_GAMC_DATA registers are used to program the values that determine the characteristics of the gamma correction for the pipe pixel data before Color Space Conversion. Additional gamma correction can be done after the Color Space Conversion Gamma if desired.
The gamma correction curve is represented by specifying a set of gamma entry reference points spaced equally along the curve for values between -1 and 1. For extended values there are extended gamma entry reference points. All input values are clamped to the greater than -7.0 and less than 7.0 range before the gamma calculation.
For input values greater than or equal to 0 and less than 1.0, the input value is used to linearly interpolate between two adjacent points of the first 33 gamma entries to create the result value. The first 32 entries are stored as16 bits per color in an unsigned 0.16 format with 0 integer and 16 fractional. The 33rd, 34th and 35th entries are storedas 19 bits per color in an unsigned 3.16 format with 3 integer and 16 fractional bits.

PRE_CSC_GAMC_DATA

For input values greater than or equal to 1.0 and less than 3.0, the input value is used to linearly interpolate between the 33rd and 34th gamma entries to create the result value.
For input values greater than or equal to 3.0 and less than 7.0, the input value is used to linearly interpolate between the 34th and 35th gamma entries to create the result value.
For negative input values, gamma is mirrored along the X-axis, giving the same result as positive input values, except for a negative sign. When gamma input may be negative, the first gamma point should be programmed to a value of 0.0 in order to have a symmetric mirroring.
Pre-CSC Gamma correction gets enabled or disabled based on the "Pipe CSC Enable" bit in the PLANE_COLOR_CTL register. The same set of values is used for gamma correction of the red, blue and green channels.
See Pipe Gamma for an example gamma curve diagram.

Programming Notes

To program the gamma correction entries, calculate the desired gamma curve for inputs from 0 to 7.0. For inputs of 0 to 1.0, multiply the input value by 32 to find the gamma entry number, then store the desired gamma result in that entry. For inputs greater than 1.0 and less than or equal to 3.0, store the result for an input of 3.0 in the 34th gamma entry. For inputs greater than 3.0 and less than or equal to 7.0, store the result for an input of 7.0 in the 35th gamma entry.

Restriction

The gamma curve must be flat or increasing, never decreasing. The gamma correction registers should only be updated when the plane is off, otherwise screen artifacts may show temporarily.

DWord	Bit	Description
0	31:19	**Reserved** Format: MBZ
	18:0	**Gamma Value** Default Value: 00000000000000000b Format: U3.16

PRE_CSC_GAMC_INDEX

PRE_CSC_GAMC_INDEX

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	4A484h-4A487h
Name:	Pipe Pre CSC Gamma Index
ShortName:	PRE_CSC_GAMC_INDEX_A
Power:	PG1
Reset:	soft
Address:	4AC84h-4AC87h
Name:	Pipe Pre CSC Gamma Index
ShortName:	PRE_CSC_GAMC_INDEX_B
Power:	PG2
Reset:	soft
Address:	4B484h-4B487h
Name:	Pipe Pre CSC Gamma Index
ShortName:	PRE_CSC_GAMC_INDEX_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31:11	**Reserved** Format: MBZ
	10	**Index Auto Increment** This field enables the index auto increment. Value / Name / Description 0b / No Increment / Do not automatically increment the index value. 1b / Auto Increment **[Default]** / Increment the index value with each read or write to the data register.
	9:6	**Reserved**

PRE_CSC_GAMC_INDEX

		Format: MBZ
	5:0	**Index Value** Access: Write/Read Status This index controls access to the array of pipe pre color space conversion gamma values. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set. When automatically incrementing, the index will roll over to 0 after writing or reading the entire allowed range. While in auto increment mode, after performing reads or writes to only part of the range, the auto increment bit must be cleared before resetting the index value.

Value	Name
[0,34]	

Predicate Rendering Data Result

MI_PREDICATE_RESULT - Predicate Rendering Data Result	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	32
Address:	02418h-0241Bh
Name:	Predicate Rendering Data Result
ShortName:	MI_PREDICATE_RESULT_RCSUNIT_BE
Address:	18418h-1841Bh
Name:	Predicate Rendering Data Result
ShortName:	MI_PREDICATE_RESULT_POCSUNIT_BE

DWord	Bit	Description
0	31:1	**Reserved** Format: PBC
	0	**MI_PREDICATE_RESULT** This bit is the result of the last MI_PREDICATE.

Predicate Rendering Data Result 1

MI_PREDICATE_RESULT_1 - Predicate Rendering Data Result 1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0241Ch-0241Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_RCSUNIT
Address:	1841Ch-1841Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_POCSUNIT
Address:	2241Ch-2241Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_BCSUNIT
Address:	1C041Ch-1C041Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VCSUNIT0
Address:	1C441Ch-1C441Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VCSUNIT1
Address:	1C841Ch-1C841Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VECSUNIT0
Address:	1D041Ch-1D041Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VCSUNIT2
Address:	1D441Ch-1D441Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VCSUNIT3
Address:	1D841Ch-1D841Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VECSUNIT1

MI_PREDICATE_RESULT_1 - Predicate Rendering Data Result 1

Address:	1E041Ch-1E041Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VCSUNIT4

Address:	1E441Ch-1E441Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VCSUNIT5

Address:	1E841Ch-1E841Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VECSUNIT2

Address:	1F041Ch-1F041Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VCSUNIT6

Address:	1F441Ch-1F441Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VCSUNIT7

Address:	1F841Ch-1F841Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VECSUNIT3

DWord	Bit	Description
0	31:1	**Reserved** Format: PBC
	0	**MI_PREDICATE_RESULT_1** This bit is used to predicate MI_BATCH_BUFFER_START commands in the RCS command stream. Usage Model: MI_MATH command will be used to do some ALU operations over GPR followed by a MI_LOAD_REGISTER_REGISTER to move the result from GPR to MI_PREDICATE_RESULT_1.

Predicate Rendering Data Result 2

MI_PREDICATE_RESULT_2 - Predicate Rendering Data Result 2	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	023BCh-023BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_RCSUNIT
Address:	183BCh-183BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_POCSUNIT
Address:	223BCh-223BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_BCSUNIT
Address:	1C03BCh-1C03BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VCSUNIT0
Address:	1C43BCh-1C43BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VCSUNIT1
Address:	1C83BCh-1C83BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VECSUNIT0
Address:	1D03BCh-1D03BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VCSUNIT2

MI_PREDICATE_RESULT_2 - Predicate Rendering Data Result 2

Address:	1D43BCh-1D43BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VCSUNIT3

Address:	1D83BCh-1D83BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VECSUNIT1

Address:	1E03BCh-1E03BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VCSUNIT4

Address:	1E43BCh-1E43BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VCSUNIT5

Address:	1E83BCh-1E83BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VECSUNIT2

Address:	1F03BCh-1F03BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VCSUNIT6

Address:	1F43BCh-1F43BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VCSUNIT7

Address:	1F83BCh-1F83BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VECSUNIT3

DWord	Bit	Description
0	31:1	**Reserved** Format: MBZ

MI_PREDICATE_RESULT_2 - Predicate Rendering Data Result 2

	0	**MI_PREDICATE_RESULT_2** This bit must be loaded with by SW based on GT mode of operation. This register must be loaded appropriately before using MI_SET_PREDICATE command.

Value	Name	Description
0h	**[Default]**	Indicates GT2 mode and lower slice is disabled.
1h		Indicates GT3 mode and lower slice is enabled.

Predicate Rendering Data Storage

MI_PREDICATE_DATA - Predicate Rendering Data Storage	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Address:	02410h-02417h
Name:	Predicate Rendering Data Storage
ShortName:	MI_PREDICATE_DATA_RCSUNIT_BE
Address:	18410h-18417h
Name:	Predicate Rendering Data Storage
ShortName:	MI_PREDICATE_DATA_POCSUNIT_BE

DWord	Bit	Description
0	63:32	**MI_PREDICATE_DATA_UDW** This register is used either as computed value based off the MI_PREDICATE_SRC0 and MI_PREDICATE_SRC1 or a temporary register. See Predicate Rendering section for more details.
	31:0	**MI_PREDICATE_DATA_LDW** This register is used either as computed value based off the MI_PREDICATE_SRC0 and MI_PREDICATE_SRC1 or a temporary register. See Predicate Rendering section for more details.

Predicate Rendering Temporary Register0

MI_PREDICATE_SRC0 - Predicate Rendering Temporary Register0	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Address:	02400h-02407h
Name:	Predicate Rendering Temporary Register0
ShortName:	MI_PREDICATE_SRC0_RCSUNIT_BE
Address:	18400h-18407h
Name:	Predicate Rendering Temporary Register0
ShortName:	MI_PREDICATE_SRC0_POCSUNIT_BE

DWord	Bit	Description
0	63:0	**MI_PREDICATE_SRC0** This register is a temporary register for Predicate Rendering. See Predicate Rendering section for more details.

Predicate Rendering Temporary Register1

MI_PREDICATE_SRC1 - Predicate Rendering Temporary Register1	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Address:	02408h-0240Fh
Name:	Predicate Rendering Temporary Register1
ShortName:	MI_PREDICATE_SRC1_RCSUNIT_BE
Address:	18408h-1840Fh
Name:	Predicate Rendering Temporary Register1
ShortName:	MI_PREDICATE_SRC1_POCSUNIT_BE

DWord	Bit	Description
0	63:0	**MI_PREDICATE_SRC1** This register is a temporary register for Predicate Rendering. See Predicate Rendering section for more details.

Preemption Hint

PREEMPTION_HINT - Preemption Hint	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	024BCh-024BFh
Name:	Preemption Hint
ShortName:	PREEMPTION_HINT_RCSUNIT
Address:	184BCh-184BFh
Name:	Preemption Hint
ShortName:	PREEMPTION_HINT_POCSUNIT
Address:	224BCh-224BFh
Name:	Preemption Hint
ShortName:	PREEMPTION_HINT_BCSUNIT
Address:	1C04BCh-1C04BFh
Name:	Preemption Hint
ShortName:	PREEMPTION_HINT_VCSUNIT0
Address:	1C44BCh-1C44BFh
Name:	Preemption Hint
ShortName:	PREEMPTION_HINT_VCSUNIT1
Address:	1C84BCh-1C84BFh
Name:	Preemption Hint
ShortName:	PREEMPTION_HINT_VECSUNIT0
Address:	1D04BCh-1D04BFh
Name:	Preemption Hint
ShortName:	PREEMPTION_HINT_VCSUNIT2
Address:	1D44BCh-1D44BFh
Name:	Preemption Hint
ShortName:	PREEMPTION_HINT_VCSUNIT3
Address:	1D84BCh-1D84BFh
Name:	Preemption Hint
ShortName:	PREEMPTION_HINT_VECSUNIT1

PREEMPTION_HINT - Preemption Hint

Address:	1E04BCh-1E04BFh
Name:	Preemption Hint
ShortName:	PREEMPTION_HINT_VCSUNIT4
Address:	1E44BCh-1E44BFh
Name:	Preemption Hint
ShortName:	PREEMPTION_HINT_VCSUNIT5
Address:	1E84BCh-1E84BFh
Name:	Preemption Hint
ShortName:	PREEMPTION_HINT_VECSUNIT2
Address:	1F04BCh-1F04BFh
Name:	Preemption Hint
ShortName:	PREEMPTION_HINT_VCSUNIT6
Address:	1F44BCh-1F44BFh
Name:	Preemption Hint
ShortName:	PREEMPTION_HINT_VCSUNIT7
Address:	1F84BCh-1F84BFh
Name:	Preemption Hint
ShortName:	PREEMPTION_HINT_VECSUNIT3

Description	Source
This register contains the Head pointer offset in to the Ring Buffer or the Dword aligned Graphics address in to the Batch Buffer corresponding to either MI_ARB_CHECK called Preemption Hint Address. When Preemption Hint Address is enabled, RCS will honor UHPTR only on parsing MI_ARB_CHK at Preemption Hint Address.	
This register contains the Head pointer offset into the Ring Buffer or the Dword aligned Graphics address into the Batch Buffer corresponding to the below listed commands in execlist mode of operation • MI_ARB_CHECK • MI_WAIT_FOR_EVENT • MI_SEMAPHORE_WAIT • 3D_PRIMITIVE • GPGPU_WALKER • MEDIA_STATE_FLUSH • PIPE_CONTROL (Only in GPGPU mode of pipeline selection) • MI_ATOMIC (Post Sync Operation set in GPGPU mode of pipeline selection) • MI_SEMAPHORE_SIGNAL (Post Sync Operation set in GPGPU mode of	RenderCS

PREEMPTION_HINT - Preemption Hint

pipeline selection)	
This register contains the Head pointer offset into the Ring Buffer or the Dword aligned Graphics address into the Batch Buffer corresponding to the below listed commands in execlist mode of operation • MI_ARB_CHECK • MI_SEMAPHORE_WAIT • 3D_PRIMITIVE • 3DSTATE_PTBR_TILE_PASS_INFO	PositionCS
This register contains the Head pointer offset into the Ring Buffer or the Dword aligned Graphics address into the Batch Buffer corresponding to the below listed commands in execlist mode of operation • MI_ARB_CHECK • MI_WAIT_FOR_EVENT • MI_SEMAPHORE_WAIT	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS

Programming Notes

Programming Restriction:
Ring BUffer Mode Of Scheduling: This register must NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of UHPTR being sampled by a given MI_ARB_CHECK in command stream. Programmer has to ensure that RCS Preemption Hint register gets programmed before UHPTR is programmed and well before RCS crosses the corresponding execution point. Preemption hint for both RingBuffer and Batch Buffer can't be enabled simultaneously.

This register must NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of preemption to match behavioral functional models.
User must ensure the Preempted Hint Address programmed matches either Ring Head Offset or Batch Buffer Graphics Virtual Address and not both of them.
User must also ensure the Preempted Hint Address[19:0] programmed matches either Ring Head Offset[19:0] or Batch Buffer Graphics Virtual Address[19:0] and not both of them.

DWord	Bit	Description
0	31:2	**Preempted Hint Address** Format: U30 Format: GraphicsAddress[31:2] This field contains the Head offset in to the Ring Buffer when Preemption Hint is set to Ring Buffer and Dword aligned Graphics Address in to the batch buffer when Preemption Hint is set to Batch Buffer.
	1	**Batch Buffer Preemption Hint** Value / Name / Description

PREEMPTION_HINT - Preemption Hint

		0h	Disabled	Preemption hint is disabled in batch buffer.
		1h	Enabled	Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Batch Buffer.
	0	**Ring Preemption Hint**		
		Value	**Name**	**Description**
		0h	Disable	Preemption hint is disabled in ring buffer.
		1h	Enabled	Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Ring Buffer.

Preemption Hint Upper DWord

PREEMPTION_HINT_UDW - Preemption Hint Upper DWord	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	024C8h-024CBh
Name:	Preemption Hint Upper DWord
ShortName:	PREEMPTION_HINT_UDW_RCSUNIT
Address:	184C8h-184CBh
Name:	Preemption Hint Upper DWord
ShortName:	PREEMPTION_HINT_UDW_POCSUNIT
Address:	224C8h-224CBh
Name:	Preemption Hint Upper DWord
ShortName:	PREEMPTION_HINT_UDW_BCSUNIT
Address:	1C04C8h-1C04CBh
Name:	Preemption Hint Upper DWord
ShortName:	PREEMPTION_HINT_UDW_VCSUNIT0
Address:	1C44C8h-1C44CBh
Name:	Preemption Hint Upper DWord
ShortName:	PREEMPTION_HINT_UDW_VCSUNIT1
Address:	1C84C8h-1C84CBh
Name:	Preemption Hint Upper DWord
ShortName:	PREEMPTION_HINT_UDW_VECSUNIT0
Address:	1D04C8h-1D04CBh
Name:	Preemption Hint Upper DWord
ShortName:	PREEMPTION_HINT_UDW_VCSUNIT2
Address:	1D44C8h-1D44CBh
Name:	Preemption Hint Upper DWord
ShortName:	PREEMPTION_HINT_UDW_VCSUNIT3
Address:	1D84C8h-1D84CBh
Name:	Preemption Hint Upper DWord
ShortName:	PREEMPTION_HINT_UDW_VECSUNIT1

PREEMPTION_HINT_UDW - Preemption Hint Upper DWord

Address:	1E04C8h-1E04CBh
Name:	Preemption Hint Upper DWord
ShortName:	PREEMPTION_HINT_UDW_VCSUNIT4

Address:	1E44C8h-1E44CBh
Name:	Preemption Hint Upper DWord
ShortName:	PREEMPTION_HINT_UDW_VCSUNIT5

Address:	1E84C8h-1E84CBh
Name:	Preemption Hint Upper DWord
ShortName:	PREEMPTION_HINT_UDW_VECSUNIT2

Address:	1F04C8h-1F04CBh
Name:	Preemption Hint Upper DWord
ShortName:	PREEMPTION_HINT_UDW_VCSUNIT6

Address:	1F44C8h-1F44CBh
Name:	Preemption Hint Upper DWord
ShortName:	PREEMPTION_HINT_UDW_VCSUNIT7

Address:	1F84C8h-1F84CBh
Name:	Preemption Hint Upper DWord
ShortName:	PREEMPTION_HINT_UDW_VECSUNIT3

This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the Batch Buffer corresponding to MI_ARB_CHECK command called Preemption Hint Address.

Programming Notes

This register should NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of UHPTR being sampled by a given MI_ARB_CHK in command stream.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**Preempted Hint Address Upper DWORD** Format: GraphicsAddress[47:32]

Primitives Generated By VF

IA_PRIMITIVES_COUNT - Primitives Generated By VF	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02318h-0231Fh
Name:	Primitives Generated By VF
ShortName:	IA_PRIMITIVES_COUNT_RCSUNIT_BE_GEOMETRY
Address:	18318h-1831Fh
Name:	Primitives Generated By VF
ShortName:	IA_PRIMITIVES_COUNT_POCSUNIT_BE_GEOMETRY
Address:	02318h-0231Fh
Name:	Primitives Generated By VF
ShortName:	IA_PRIMITIVES_COUNT_RCSUNIT_BE
Address:	18318h-1831Fh
Name:	Primitives Generated By VF
ShortName:	IA_PRIMITIVES_COUNT_POCSUNIT_BE

This register stores the count of primitives generated by VF. This register is part of the context save and restore.

DWord	Bit	Description
0	63:32	**IA Primitives Count Report UDW** Total number of primitives output by the Vertex Fetch (IA) stage. This count is updated for every primitive output by the VF stage, as long as Statistics Enable is set in VF_STATE (see the Vertex Fetch Chapter in the 3D Volume.)
	31:0	**IA Primitives Count Report LDW** Total number of primitives output by the Vertex Fetch (IA) stage. This count is updated for every primitive output by the VF stage, as long as Statistics Enable is set in VF_STATE (see the Vertex Fetch Chapter in the 3D Volume.)

PS_ADAPTIVE_CTRL

PS_ADAPTIVE_CTRL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of horizontal blank after armed
Double Buffer Armed By:	Write to PS_WIN_SZ
Address:	681A8h-681ABh
Name:	PS Adaptive Control Set 0 1
ShortName:	PS_ADAPTIVE_CTRL_SET_0_1_A
Power:	PG1
Reset:	soft
Address:	681ACh-681AFh
Name:	PS Adaptive Control Set 1 1
ShortName:	PS_ADAPTIVE_CTRL_SET_1_1_A
Power:	PG1
Reset:	soft
Address:	682A8h-682ABh
Name:	PS Adaptive Control Set 0 1
ShortName:	PS_ADAPTIVE_CTRL_SET_0_2_A
Power:	PG1
Reset:	soft
Address:	682ACh-682AFh
Name:	PS Adaptive Control Set 1 1
ShortName:	PS_ADAPTIVE_CTRL_SET_1_2_A
Power:	PG1
Reset:	soft
Address:	689A8h-689ABh

PS_ADAPTIVE_CTRL	
Name:	PS Adaptive Control Set 0 1
ShortName:	PS_ADAPTIVE_CTRL_SET_0_1_B
Power:	PG2
Reset:	soft
Address:	689ACh-689AFh
Name:	PS Adaptive Control Set 1 1
ShortName:	PS_ADAPTIVE_CTRL_SET_1_1_B
Power:	PG2
Reset:	soft
Address:	68AA8h-68AABh
Name:	PS Adaptive Control Set 0 1
ShortName:	PS_ADAPTIVE_CTRL_SET_0_2_B
Power:	PG2
Reset:	soft
Address:	68AACh-68AAFh
Name:	PS Adaptive Control Set 1 1
ShortName:	PS_ADAPTIVE_CTRL_SET_1_2_B
Power:	PG2
Reset:	soft
Address:	691A8h-691ABh
Name:	PS Adaptive Control Set 0 1
ShortName:	PS_ADAPTIVE_CTRL_SET_0_1_C
Power:	PG2
Reset:	soft
Address:	691ACh-691AFh
Name:	PS Adaptive Control Set 1 1
ShortName:	PS_ADAPTIVE_CTRL_SET_1_1_C
Power:	PG2
Reset:	soft
Address:	692A8h-692ABh

PS_ADAPTIVE_CTRL

Name:	PS Adaptive Control Set 0 1
ShortName:	PS_ADAPTIVE_CTRL_SET_0_2_C
Power:	PG2
Reset:	soft

Address:	692ACh-692AFh
Name:	PS Adaptive Control Set 1 1
ShortName:	PS_ADAPTIVE_CTRL_SET_1_2_C
Power:	PG2
Reset:	soft

Programming Notes

Recommended threshold programming:
Threshold 1: 1Eh
Threshold 2: 2Dh
Threshold 3: 3Ch

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:16	**Threshold 3** This field specifies the third threshold value used in adaptive filtering.
	15:8	**Threshold 2** This field specifies the second threshold value used in adaptive filtering.
	7:0	**Threshold 1** This field specifies the first threshold value used in adaptive filtering.

PS_COEF_DATA

PS_COEF_DATA	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of horizontal blank after armed
Double Buffer Armed By:	Write to PS_WIN_SZ
Address:	6819Ch-6819Fh
Name:	PS Coeffecient Set 0 Data 1
ShortName:	PS_COEF_SET_0_DATA_1_A
Power:	PG1
Reset:	soft
Address:	681A4h-681A7h
Name:	PS Coeffecient Set 1 Data 1
ShortName:	PS_COEF_SET_1_DATA_1_A
Power:	PG1
Reset:	soft
Address:	6829Ch-6829Fh
Name:	PS Coeffecient Set 0 Data 1
ShortName:	PS_COEF_SET_0_DATA_2_A
Power:	PG1
Reset:	soft
Address:	682A4h-682A7h
Name:	PS Coeffecient Set 1 Data 1
ShortName:	PS_COEF_SET_1_DATA_2_A
Power:	PG1
Reset:	soft
Address:	6899Ch-6899Fh

PS_COEF_DATA	
Name:	PS Coeffecient Set 0 Data 1
ShortName:	PS_COEF_SET_0_DATA_1_B
Power:	PG2
Reset:	soft
Address:	689A4h-689A7h
Name:	PS Coeffecient Set 1 Data 1
ShortName:	PS_COEF_SET_1_DATA_1_B
Power:	PG2
Reset:	soft
Address:	68A9Ch-68A9Fh
Name:	PS Coeffecient Set 0 Data 1
ShortName:	PS_COEF_SET_0_DATA_2_B
Power:	PG2
Reset:	soft
Address:	68AA4h-68AA7h
Name:	PS Coeffecient Set 1 Data 1
ShortName:	PS_COEF_SET_1_DATA_2_B
Power:	PG2
Reset:	soft
Address:	6919Ch-6919Fh
Name:	PS Coeffecient Set 0 Data 1
ShortName:	PS_COEF_SET_0_DATA_1_C
Power:	PG2
Reset:	soft
Address:	691A4h-691A7h
Name:	PS Coeffecient Set 1 Data 1
ShortName:	PS_COEF_SET_1_DATA_1_C
Power:	PG2
Reset:	soft
Address:	6929Ch-6929Fh

PS_COEF_DATA

Name:	PS Coeffecient Set 0 Data 1
ShortName:	PS_COEF_SET_0_DATA_2_C
Power:	PG2
Reset:	soft
Address:	692A4h-692A7h
Name:	PS Coeffecient Set 1 Data 1
ShortName:	PS_COEF_SET_1_DATA_2_C
Power:	PG2
Reset:	soft

These are the coefficient values for scaler.
The scaler coefficient Index indicates the coefficients array location to be accessed through this register.
The contents of the coefficient array is uninitialized until Software loads the array (i.e. the array is not resetable).
Use of the coefficient array or reading from the coefficient array before Software has initialized it will result in non-deterministic behavior or read back data.

Restriction
This register must be written only as a full 32 bit dword. Byte or word writes are not supported.

DWord	Bit	Description
0	31:16	**Coefficient2** Format: SCALER_COEFFICIENT_FORMAT Specifies the value for the second coefficient stored in this dword.
	15:0	**Coefficient1** Format: SCALER_COEFFICIENT_FORMAT Specifies the value for the first coefficient stored in this dword.

PS_COEF_INDEX

PS_COEF_INDEX	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	68198h-6819Bh
Name:	PS Coeffecient Set 0 Index 1
ShortName:	PS_COEF_SET_0_INDEX_1_A
Power:	PG1
Reset:	soft
Address:	681A0h-681A3h
Name:	PS Coeffecient Set 1 Index 1
ShortName:	PS_COEF_SET_1_INDEX_1_A
Power:	PG1
Reset:	soft
Address:	68298h-6829Bh
Name:	PS Coeffecient Set 0 Index 1
ShortName:	PS_COEF_SET_0_INDEX_2_A
Power:	PG1
Reset:	soft
Address:	682A0h-682A3h
Name:	PS Coeffecient Set 1 Index 1
ShortName:	PS_COEF_SET_1_INDEX_2_A
Power:	PG1
Reset:	soft
Address:	68998h-6899Bh
Name:	PS Coeffecient Set 0 Index 1
ShortName:	PS_COEF_SET_0_INDEX_1_B

PS_COEF_INDEX	
Power:	PG2
Reset:	soft
Address:	689A0h-689A3h
Name:	PS Coeffecient Set 1 Index 1
ShortName:	PS_COEF_SET_1_INDEX_1_B
Power:	PG2
Reset:	soft
Address:	68A98h-68A9Bh
Name:	PS Coeffecient Set 0 Index 1
ShortName:	PS_COEF_SET_0_INDEX_2_B
Power:	PG2
Reset:	soft
Address:	68AA0h-68AA3h
Name:	PS Coeffecient Set 1 Index 1
ShortName:	PS_COEF_SET_1_INDEX_2_B
Power:	PG2
Reset:	soft
Address:	69198h-6919Bh
Name:	PS Coeffecient Set 0 Index 1
ShortName:	PS_COEF_SET_0_INDEX_1_C
Power:	PG2
Reset:	soft
Address:	691A0h-691A3h
Name:	PS Coeffecient Set 1 Index 1
ShortName:	PS_COEF_SET_1_INDEX_1_C
Power:	PG2
Reset:	soft
Address:	69298h-6929Bh
Name:	PS Coeffecient Set 0 Index 1
ShortName:	PS_COEF_SET_0_INDEX_2_C

PS_COEF_INDEX

Power:	PG2
Reset:	soft
Address:	692A0h-692A3h
Name:	PS Coeffecient Set 1 Index 1
ShortName:	PS_COEF_SET_1_INDEX_2_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31:11	**Reserved** Format: MBZ
	10	**Index Auto Increment** Access: R/W This field enables the index auto increment. 0b – No Increment – Do not automatically increment the index value. 1b – Auto Increment **[Default]** – Increment the index value with each read or write to the data register.
	9:6	**Reserved** Format: MBZ
	5:0	**Index Value** Access: R/W This index controls access to the array of scaler coefficient values. Value: [0,59]

PS_CTRL

PS_CTRL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank after armed
Double Buffer Armed By:	Write to PS_WIN_SZ
Address:	68180h-68183h
Name:	PS Control 1
ShortName:	PS_CTRL_1_A
Power:	PG1
Reset:	soft
Address:	68280h-68283h
Name:	PS Control 1
ShortName:	PS_CTRL_2_A
Power:	PG1
Reset:	soft
Address:	68980h-68983h
Name:	PS Control 1
ShortName:	PS_CTRL_1_B
Power:	PG2
Reset:	soft
Address:	68A80h-68A83h
Name:	PS Control 1
ShortName:	PS_CTRL_2_B
Power:	PG2
Reset:	soft
Address:	69180h-69183h
Name:	PS Control 1
ShortName:	PS_CTRL_1_C
Power:	PG2
Reset:	soft

PS_CTRL

Address:	69280h-69283h
Name:	PS Control 1
ShortName:	PS_CTRL_2_C
Power:	PG2
Reset:	soft

Description

The pipe scalers are used to scale the output of a display pipe or of a display plane. All pipes have two scalers each.
The scaler preserves 8 bits of alpha and 10 bits of each color channel for plane scaling and 12 bits of each color channel for pipe scaling.
The scalers can be assigned to any plane (except cursor) output or the output of the display pipe (after blending and color correction, before dithering and color clamping).
Downscale usages have scale factor restrictions:

- All scaler modes support a downscale factor of less than3.0 in each direction.
- Pipe YUV 420 encoding for port output supports Y downscale factor of less than 1.5 in each direction.

The scalers support horizontal source sizes up to 5120 and vertical source sizes up to 4096.

Programming Notes

The scalers must not be enabled when the horizontal source sizes are greater than 5120 and the vertical sizes greater than 4320.

Driver is responsible for making sure all the plane, pipe, and scaler size registers are programmed appropriately and gets applied atomically to the same frame since hardware does not ensure an atomic update of plane, scaler, and pipe source size registers.

When scaling a pipe, the scaler window size and position must fit within the pipe active size. If there is a seam present (i.e. PIPE_SEAM_EXCESS is non-zero), then the pipe's horizontal active size that the scaler sees is the horizontal active size defined within the TRANS_HTOTAL register plus the amount(s) specified within the PIPE_SEAM_EXCESS.
Pipe Horizontal Active = Horizontal Active + Left Excess Amount + Right Excess Amount

Refer to 'YUV 420 Support' page for scaler restrictions with YUV 420 pipe output.

Restriction

Down scaling (scaler input size is larger than scaler window size) can reduce the maximum supported pixel rate for a pipe as well as increase the watermark and data buffer requirements. Refer to the Display Resolution Support page and Watermark Calculations page for detailed calculations.

Scaler 1 and 2 must not be both scaling the same plane output.
When scaling a pipe, the scaler window size and position must fit within the pipe active size.
When scaling a plane, the plane position must be programmed to 0 and the scaler window size and position must fit within the pipe source size.
When scaling is enabled, the scaler input width should be a minimum of 8 pixels and the height should be minimum of 8 scanlines.

PS_CTRL

When the plane scaling is used with YUV 420 planar formats, the height should be a minimum of 16 scanlines. When using down scaling (scaler input size is larger than scaler output size) the maximum supported pixel rate will be reduced by the down scale amount.

DWord	Bit	Description
0	31	**Enable Scaler** This field enables the scaler. Value: 0b — Disable; 1b — Enable
	30	**Scaler Type** This field selects the scaler type. Value: 0b — Non Linear **[Default]**; 1b — Linear
	29	**Scaler Mode** Description: The Planar mode must be used when non-HDR capable planes are using YUV 420 planar surface formats. In this configuration, the scaler takes care of both the chroma upsampling and scaling. The Planar mode must not be used for the HDR capable planes. They have dedicated chroma upsamplers and only use the scaler in Normal mode for scaling. Value: 0b — Normal; 1b — Planar
	28	**Adaptive Filtering** This field enables the scaler adaptive vertical and horizontal filtering. When adaptive filtering is enabled, the adaptive threshold values must be programmed in the PS_ADAPTIVE_CTRL register and the Filter Set Select bits should be programmed. Value: 0h — Disable; 1h — Enable
	27:25	**Scaler Binding** This field selects the where the scaling operation is done. When scaling a pipe, the pipe source size specifies the input size to the scaler. When scaling a plane, the PLANE_SIZE specifies the input size to the scaler. Any border around a scaled plane window will become transparent at the

plane blender.

Value	Name
000b	Pipe Scaler
001b	Plane 1 Scaler
010b	Plane 2 Scaler
011b	Plane 3 Scaler
100b	Plane 4 Scaler
101b	Plane 5 Scaler
110b	Plane 6 Scaler
111b	Plane 7 Scaler

Programming Notes
When plane scaling is enabled on planes 1 through 3, make sure that the *PLANE_CUS_CTL.Plane Scaling Enabled* (bit 30) is programmed correctly.

Restriction
The scaler input size should be at least 8 scanlines. Plane/Pipe scaling is not compatible with interlaced fetch mode. Plane up and down scaling is not compatible with keying. Keying can be enabled with 1:1 plane scaling. Plane scaling is not compatible with the Indexed 8-bit, XR_BIAS, or any pixel values less than 0 or greater than 1.

24:23 **FILTER SELECT**

Description
This field selects filter coefficients. The medium coefficients will provide an unfiltered image when the scale factor is 1:1.
In the programmed mode, the filter coefficients must be programmed using the PS_COEF_INDEX and PS_COEF_DATA registers and the Filter Set Select bits should be programmed.

Value	Name
00b	Medium
01b	Programmed
10b	Edge Enhance
11b	Bilinear

22 **ADAPTIVE FILTER SELECT**

This field selects the filter coefficients used for adaptive filtering. The field is ignored when adaptive filtering is not enabled.

Value	Name

0b	Medium
1b	Edge Enhance

21 Pipe Scaler Location

This field selects where the pipe scaling is done in the pipe.

Value	Name	Description
0b	After Output CSC	This is a non-linear tap point
1b	After CSC	This is a linear tap point

20 Reserved

19 Reserved

Format:	MBZ

18 Reserved

Format:	MBZ

17 Reserved

16:10 Reserved

Format:	MBZ

9 Allow Double Buffer Update Disable

This field controls whether double buffer updates are allowed to be disabled for this scaler. The DOUBLE_BUFFER_CTL register can be configured to globally disable double buffer updates for resources that allow them to be disabled

Value	Name
0b	Not Allowed
1b	Allowed

8 Reserved

7:5 Scaler Binding Y

Description
This field selects where the planar YUV420 Y plane scaling operation is done. This field is ignored if planar YUV420 plane scaling is not used.
This field is used only for planes 4-7 when the plane scaler is used for chroma upsampling. Planes 1-3 must use the dedicated chroma up sampler (programmed in PLANE_CUS_CTL)for YUV 444 up conversion.

PS_CTRL

Value	Name
110b	Plane 6 Scaler
111b	Plane 7 Scaler

Restriction
The scaler input size should be at least 16 scanlines.

4 **Y Vert Filter Set Sel**

This field selects the programmed coefficient set and/or the adaptive threshold set used by the Y component vertical filter when filtering YUV planar formats. This field is ignored with other formats.

Value	Name
0b	Set 0 **[Default]**
1b	Set 1

3 **Y Horz Filter Set Sel**

This field selects the programmed coefficient set and/or the adaptive threshold set used by the Y component horizontal filter when filtering YUV hybrid planar formats. This field is ignored with other formats.

Value	Name
0b	Set 0 **[Default]**
1b	Set 1

2 **UV Vert Filter Set Sel**

This field selects the programmed coefficient set and/or the adaptive threshold set used by the UV component vertical filter when filtering YUV hybrid planar formats. With other formats, this field selects the coefficient set and/or the adaptive threshold set used by the vertical filter.

Value	Name
0b	Set 0 **[Default]**
1b	Set 1

1 **UV Horz Filter Set Sel**

This field selects the programmed coefficient set and/or the adaptive threshold set used by the UV component horizontal filter when filtering YUV hybrid planar formats. With other formats, this field selects the coefficient set and/or the adaptive threshold set used by the horizontal filter.

Value	Name
0b	Set 0 **[Default]**
1b	Set 1

0 **Reserved**

PS_CTRL			
		Format:	MBZ

PS_ECC_STAT

PS_ECC_STAT	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/WC
Size (in bits):	32
Address:	681D0h-681D3h
Name:	PS ECC Status 1
ShortName:	PS_ECC_STAT_1_A
Power:	PG1
Reset:	soft
Address:	682D0h-682D3h
Name:	PS ECC Status 1
ShortName:	PS_ECC_STAT_2_A
Power:	PG1
Reset:	soft
Address:	689D0h-689D3h
Name:	PS ECC Status 1
ShortName:	PS_ECC_STAT_1_B
Power:	PG2
Reset:	soft
Address:	68AD0h-68AD3h
Name:	PS ECC Status 1
ShortName:	PS_ECC_STAT_2_B
Power:	PG2
Reset:	soft
Address:	691D0h-691D3h
Name:	PS ECC Status 1
ShortName:	PS_ECC_STAT_1_C
Power:	PG2
Reset:	soft
Address:	692D0h-692D3h
Name:	PS ECC Status 1
ShortName:	PS_ECC_STAT_2_C

PS_ECC_STAT

Power: PG2

Reset: soft

Each of these fields is a sticky bit that gives the ECC error status for a particular memory bank. A '1' in a bit indicates that ECC detected an error. A write of '1' to a bit will clear the bit. Single errors are corrected by ECC. Double errors are not correctable.

DWord	Bit	Description
0	31:17	**Reserved** Format: MBZ
	16	**Double Error Detected**
	15:1	**Reserved** Format: MBZ
	0	**Single Error Detected**

PS_HPHASE

PS_HPHASE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of horizontal blank after armed
Double Buffer Armed By:	Write to PS_WIN_SZ
Address:	68194h-68197h
Name:	PS Horizontal Phase 1
ShortName:	PS_HPHASE_1_A
Power:	PG1
Reset:	soft
Address:	68294h-68297h
Name:	PS Horizontal Phase 1
ShortName:	PS_HPHASE_2_A
Power:	PG1
Reset:	soft
Address:	68994h-68997h
Name:	PS Horizontal Phase 1
ShortName:	PS_HPHASE_1_B
Power:	PG2
Reset:	soft
Address:	68A94h-68A97h
Name:	PS Horizontal Phase 1
ShortName:	PS_HPHASE_2_B
Power:	PG2
Reset:	soft
Address:	69194h-69197h
Name:	PS Horizontal Phase 1
ShortName:	PS_HPHASE_1_C
Power:	PG2
Reset:	soft

PS_HPHASE

Address:	69294h-69297h
Name:	PS Horizontal Phase 1
ShortName:	PS_HPHASE_2_C
Power:	PG2
Reset:	soft

Description
This register programs the scaler horizontal filtering initial phase. The initial phase within the -0.5 to 1.5 range is supported. Refer to PS_VPHASE for programming details.
The programming of this register is ignored by the pipe scaler when the pipe is in the Full Blend YUV420 mode. The scaler hardware is responsible for calculating and applying the appropriate horizontal phase when encoding the YUV420 format.

DWord	Bit	Description
0	31:30	**Y Initial HPhase Int** This field specifies the integer part of the Y horizontal filtering initial phase when the scaler is operating on YUV420 hybrid planar formats. This field is ignored for non-YUV420 pixel formats.
	29:17	**Y Initial HPhase Frac** This field specifiesthe most significant 13 bits of the fractional part of the Y horizontal filtering initial phase when the scaler is operating onYUV420 hybrid planar formats. This field should be programmed with the fractional portion of the initial phase multiplied by 2^13. This field is ignored for non-YUV420 pixel formats.
	16	**Y Initial HPhase Trip** This field specifies whether the initial trip, that may occur while applying the initial phase, is used in Y horizontal filtering. This field is ignored for non-YUV420 pixel formats. Value: 1b — Name: Enable Value: 0b — Name: Disable
	15:14	**UV or RGB Initial HPhase Int** This field specifies the integer part of the UV or RGB horizontal filtering initial phase.
	13:1	**UV or RGB Initial HPhase Frac** This field specifies the most significant 13 bits of the fractional part of the UV or RGB horizontal filtering initial phase. This field should be programmed with the fractional portion of the initial phase multiplied by 2^13.
	0	**UV or RGB Initial HPhase Trip** This field specifies whether the initial trip, that may occur while applying the initial phase, is used in UV or RGB horizontal filtering. Value: 1b — Name: Enable

PS_HPHASE			
		0b	Disable

PS_HSCALE

PS_HSCALE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	68190h-68193h
Name:	PS Horizontal Scale 1
ShortName:	PS_HSCALE_1_A
Power:	PG1
Reset:	soft
Address:	68290h-68293h
Name:	PS Horizontal Scale 1
ShortName:	PS_HSCALE_2_A
Power:	PG1
Reset:	soft
Address:	68990h-68993h
Name:	PS Horizontal Scale 1
ShortName:	PS_HSCALE_1_B
Power:	PG2
Reset:	soft
Address:	68A90h-68A93h
Name:	PS Horizontal Scale 1
ShortName:	PS_HSCALE_2_B
Power:	PG2
Reset:	soft
Address:	69190h-69193h
Name:	PS Horizontal Scale 1
ShortName:	PS_HSCALE_1_C
Power:	PG2
Reset:	soft
Address:	69290h-69293h
Name:	PS Horizontal Scale 1
ShortName:	PS_HSCALE_2_C

PS_HSCALE

Power: PG2

Reset: soft

DWord	Bit	Description
0	31:18	**Reserved** Format: MBZ
	17:15	**HScale Int** Access: RO This field gives the integer part of the horizontal scaling factor divided by the oversampling rate. HSCALE_INT = int(src width/dest width)
	14:0	**HScale Frac** Access: RO This field gives the fractional part of the horizontal scaling factor divided by the oversampling rate. HSCALE_FRAC = int((((src width/dest width)-HSCALE_INT) * 2^^15) + 0.5)

PS_PWR_GATE

PS_PWR_GATE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank after armed
Double Buffer Armed By:	Write to PS_WIN_SZ
Address:	68160h-68163h
Name:	Power Gate Control 1
ShortName:	PS_PWR_GATE_1_A
Power:	PG1
Reset:	soft
Address:	68260h-68263h
Name:	Power Gate Control 1
ShortName:	PS_PWR_GATE_2_A
Power:	PG1
Reset:	soft
Address:	68960h-68963h
Name:	Power Gate Control 1
ShortName:	PS_PWR_GATE_1_B
Power:	PG2
Reset:	soft
Address:	68A60h-68A63h
Name:	Power Gate Control 1
ShortName:	PS_PWR_GATE_2_B
Power:	PG2
Reset:	soft
Address:	69160h-69163h
Name:	Power Gate Control 1
ShortName:	PS_PWR_GATE_1_C
Power:	PG2
Reset:	soft

PS_PWR_GATE

Address: 69260h-69263h
Name: Power Gate Control 1
ShortName: PS_PWR_GATE_2_C
Power: PG2
Reset: soft

DWord	Bit	Description
0	31	**Reserved**
	30:6	**Reserved** Format: MBZ
	5	**Dynamic Pwr Gate Disable** Disables the dynamic power gate of unused EBB's when processing low resolution source images. 0b: Do Not Disable **[Default]** 1b: Disable
	4:3	**Reserved**
	2	**Reserved** Format: MBZ
	1:0	**Reserved**

PS_VPHASE

PS_VPHASE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank after armed
Double Buffer Armed By:	Write to PS_WIN_SZ
Address:	68188h-6818Bh
Name:	PS Vertical Phase 1
ShortName:	PS_VPHASE_1_A
Power:	PG1
Reset:	soft
Address:	68288h-6828Bh
Name:	PS Vertical Phase 1
ShortName:	PS_VPHASE_2_A
Power:	PG1
Reset:	soft
Address:	68988h-6898Bh
Name:	PS Vertical Phase 1
ShortName:	PS_VPHASE_1_B
Power:	PG2
Reset:	soft
Address:	68A88h-68A8Bh
Name:	PS Vertical Phase 1
ShortName:	PS_VPHASE_2_B
Power:	PG2
Reset:	soft
Address:	69188h-6918Bh
Name:	PS Vertical Phase 1
ShortName:	PS_VPHASE_1_C
Power:	PG2
Reset:	soft

PS_VPHASE

Address:	69288h-6928Bh
Name:	PS Vertical Phase 1
ShortName:	PS_VPHASE_2_C
Power:	PG2
Reset:	soft

Description

This register programs the scaler vertical filtering initial phase. The programming of this register is ignored in the pipe scaler PF/ID fetch mode, and the pipe scaler is responsible for applying the appropriate vertical phase to the proper frame when interlacing.
The initial phase within the -0.5 to 1.5 range is supported.
Programming +ve intital phase:

- Initial Phase Trip = 1b
- Initial Phase Int = Desired Initial Phase Int
- Initial Phase Frac = Desired Initial Phase Frac

Programming -ve initial phase:

- Initial Phase Trip = 0b
- Initial Phase Int = 00b
- Initial Phase Frac = 1 - Desired Initial Phase Frac

For example, -0.25 initial phase should be programmed as

- Initial Phase Trip = 0b
- Initial Phase Int = 00b
- Initial Phase Frac = 1 - 0.25 = 0.75

The following table shows phase programming for frequently used YUV420 to YUV444 chroma upsampling scenarios (chroma being filtered to the center of the pixel).

YUV 420 Chroma Siting	H Phase	V Phase	Programmed H Initial Phase	Programmed H Initial Trip	Programmed V Initial Phase	Programmed V Initial Trip
Top Left	0.25	0.25	0.25	1	0.25	1
Bottom Right (MPEG-1)	-0.25	-0.25	0.75	0	0.75	0
Bottom Center (MPEG-2)	0	-0.25	0	0	0.75	0

The programming of this register is ignored by a pipe scaler when the pipe is in the Full Blend YUV420 mode. The scaler hardware is responsible for calculating and applying the appropriate vertical phase when encoding the YUV420 format.

DWord	Bit	Description

PS_VPHASE		
0	31:30	**Y Initial VPhase Int** This field specifies the integer part of the Y vertical filtering initial phase when the scaler is operating on YUV420 hybrid planar formats. This field is ignored for non-YUV420 pixel formats.
	29:17	**Y Initial VPhase Frac** This field specifies the most significant 13 bits of the fractional part of the Y vertical filtering initial phase when the scaler is operating on YUV420 hybrid planar formats. This field should be programmed with the fractional portion of the initial phase multiplied by 2^13. This field is ignored for non-YUV420 pixel formats.
	16	**Y Initial VPhase Trip** This field specifies the whether the initial trip, that may occur while applying the initial phase, is used in Y vertical filtering. This field is ignored for non-YUV420 pixel formats. Value: 1b — Name: Used Value: 0b — Name: Not Used
	15:14	**UV or RGB Initial VPhase Int** This field specifies the integer part of the UV or RGB vertical filtering initial phase.
	13:1	**UV or RGB Initial VPhase Frac** This field specifies the most significant 13 bits of the fractional part of the UV or RGB vertical filtering initial phase. This field should be programmed with the fractional portion of the initial phase multiplied by 2^13.
	0	**UV or RGB Initial VPhase Trip** This field specifies whether the initial trip, that may occur while applying the initial phase, is used in UV or RGB vertical filtering. Value: 1b — Name: Used Value: 0b — Name: Not Used

PS_VSCALE

PS_VSCALE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	68184h-68187h
Name:	PS Vertical Scale 1
ShortName:	PS_VSCALE_1_A
Power:	PG1
Reset:	soft
Address:	68284h-68287h
Name:	PS Vertical Scale 1
ShortName:	PS_VSCALE_2_A
Power:	PG1
Reset:	soft
Address:	68984h-68987h
Name:	PS Vertical Scale 1
ShortName:	PS_VSCALE_1_B
Power:	PG2
Reset:	soft
Address:	68A84h-68A87h
Name:	PS Vertical Scale 1
ShortName:	PS_VSCALE_2_B
Power:	PG2
Reset:	soft
Address:	69184h-69187h
Name:	PS Vertical Scale 1
ShortName:	PS_VSCALE_1_C
Power:	PG2
Reset:	soft
Address:	69284h-69287h
Name:	PS Vertical Scale 1
ShortName:	PS_VSCALE_2_C

PS_VSCALE

Power: PG2

Reset: soft

DWord	Bit	Description
0	31:18	**Reserved** Format: MBZ
	17:15	**VScale Int** Access: RO This field gives the integer part of the vertical scale factor. VSCALE_INT = int(src height/(interlace x dest height)) Interlace = 1/2 in interlace modes, 1 in progressive modes.
	14:0	**VScale Frac** Access: RO This field gives the fractional part of the vertical scale factor. VSCALE_FRAC = int(((src height/(interlace x dest height)-VSCALE_INT) * 2^^15) + 0.5) Interlace = 1/2 in interlace modes, 1 in progressive modes.

PS_WIN_POS

PS_WIN_POS	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank after armed
Double Buffer Armed By:	Write to PS_WIN_SZ
Address:	68170h-68173h
Name:	PS Window Position 1
ShortName:	PS_WIN_POS_1_A
Power:	PG1
Reset:	soft
Address:	68270h-68273h
Name:	PS Window Position 1
ShortName:	PS_WIN_POS_2_A
Power:	PG1
Reset:	soft
Address:	68970h-68973h
Name:	PS Window Position 1
ShortName:	PS_WIN_POS_1_B
Power:	PG2
Reset:	soft
Address:	68A70h-68A73h
Name:	PS Window Position 1
ShortName:	PS_WIN_POS_2_B
Power:	PG2
Reset:	soft
Address:	69170h-69173h
Name:	PS Window Position 1
ShortName:	PS_WIN_POS_1_C
Power:	PG2
Reset:	soft

PS_WIN_POS

Address:	69270h-69273h
Name:	PS Window Position 1
ShortName:	PS_WIN_POS_2_C
Power:	PG2
Reset:	soft

Coordinates are determined with a value of (0,0) being the upper left corner of the display device (rotation does not affect this).

Restriction
When scaling a pipe, the scaled output must fit inside the pipe active area, so Pipe active size >= PS window position + PS window size. When scaling a plane, the scaled output must fit inside the pipe source area, so Pipe source size >= PS window position + PS window size.

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28:16	**XPOS** **Description** This field specifies the horizontal coordinate in pixels of the upper left most pixel of the scaled output window. Restriction : This field must be even when the scaler is delivering YUV420 format for HDMI output.
	15:13	**Reserved** Format: MBZ
	12:0	**YPOS** This field specifies the vertical coordinate in lines of the upper left most pixel of the scaled output window. **Restriction** Bit 0 must be zero for interlaced modes. This field must be even when the scaler is delivering YUV420 format for HDMI output.

PS_WIN_SZ

PS_WIN_SZ	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank
Address:	68174h-68177h
Name:	PS Window Size 1
ShortName:	PS_WIN_SZ_1_A
Power:	PG1
Reset:	soft
Address:	68274h-68277h
Name:	PS Window Size 1
ShortName:	PS_WIN_SZ_2_A
Power:	PG1
Reset:	soft
Address:	68974h-68977h
Name:	PS Window Size 1
ShortName:	PS_WIN_SZ_1_B
Power:	PG2
Reset:	soft
Address:	68A74h-68A77h
Name:	PS Window Size 1
ShortName:	PS_WIN_SZ_2_B
Power:	PG2
Reset:	soft
Address:	69174h-69177h
Name:	PS Window Size 1
ShortName:	PS_WIN_SZ_1_C
Power:	PG2
Reset:	soft
Address:	69274h-69277h

PS_WIN_SZ

Name: PS Window Size 1
ShortName: PS_WIN_SZ_2_C
Power: PG2
Reset: soft

This register specifies the size in pixels of the scaled output window. A programmed value of (100, 100) will result in scaled output window of size 100x100 pixels.
Writes to this register arm PS registers on this pipe. After arming, any write to other PS registers will disarm all PS registers. Subsequent write to this register will arm them again.

Restriction

When scaling a pipe, the scaled output must fit inside the pipe active area, so Pipe active size >= PS window position + PS window size. When scaling a plane, the scaled output must fit inside the pipe source area, so Pipe source size >= PS window position + PS window size.

DWord	Bit	Description
0	31:30	**Reserved** Format: MBZ
	29:16	**XSIZE** **Description** This field specifies the horizontal size in pixels of the scaled output window. Restriction : When the pipe scalar is configured to output YUV 420, the X size must be even.
	15:13	**Reserved** Format: MBZ
	12:0	**YSIZE** This field specifies the vertical size in scan lines of the scaled output window. Restriction : Bit 0 must be zero for interlaced modes. **Restriction** When the pipe scalar is configured to output YUV 420, the Y size must be even.

PS Depth Count

PS_DEPTH_COUNT - PS Depth Count	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02350h

This register stores the value of the count of samples that have passed the depth test. This register is part of the context save and restore. Note that the value of this register can be obtained in a pipeline-synchronous fashion without a pipeline flush by using the 3DCONTROL command. See 3D Overview in the 3D volume.

DWord	Bit	Description
0..1	63:32	**Depth Count UDW** This register reflects the total number of samples that have passed the depth test (i.e., will be visible). All samples are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Samples that pass the depth test but fail the stencil test will not be counted.
	31:0	**Depth Count LDW** This register reflects the total number of samples that have passed the depth test (i.e., will be visible). All samples are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Samples that pass the depth test but fail the stencil test will not be counted.

PS Depth Count for Slice0

PS_DEPTH_COUNT_SLICE0 - PS Depth Count for Slice0

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	022D8h
Name:	PS Depth Count for Slice0
ShortName:	PS_DEPTH_COUNT_SLICE0

This register stores the value of the count of pixels that have passed the depth test in Slice0. This register is part of the context save and restore. This register should not be programmed by SW.Note: In GT3 mode there are two slices Slice0 (Upper Slice) and Slice1 (Lower slice).

DWord	Bit	Description
0..1	63:32	**Depth Count UDW** This register reflects the total number of pixels that have passed the depth test in Slice0(i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.
	31:0	**Depth Count LDW** This register reflects the total number of pixels that have passed the depth test in Slice0(i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.

PS Depth Count for Slice1

PS_DEPTH_COUNT_SLICE1 - PS Depth Count for Slice1	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	022F8h
Name:	PS Depth Count for Slice1
ShortName:	PS_DEPTH_COUNT_SLICE1

This register stores the value of the count of pixels that have passed the depth test in Slice1. This register is part of the context save and restore. This register should not be programmed by SW.Note: In GT3 mode there are two slices Slice0 (Upper Slice) and Slice1 (Lower slice).

DWord	Bit	Description
0..1	63:32	**Depth Count UDW** This register reflects the total number of pixels that have passed the depth test in Slice1(i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.
	31:0	**Depth Count LDW** This register reflects the total number of pixels that have passed the depth test in Slice1(i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.

PS Depth Count for Slice2

PS_DEPTH_COUNT_SLICE2 - PS Depth Count for Slice2	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02450h
Name:	PS Depth Count for Slice2
ShortName:	PS_DEPTH_COUNT_SLICE2

This register stores the value of the count of pixels that have passed the depth test in Slice2. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0..1	63:32	**Depth Count UDW** This register reflects the depth test in slice2 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.
	31:0	**Depth Count LDW** This register reflects the depth test in slice2 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.

PS Depth Count for Slice3

PS_DEPTH_COUNT_SLICE3 - PS Depth Count for Slice3	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02460h
Name:	PS Depth Count for Slice3
ShortName:	PS_DEPTH_COUNT_SLICE3

This register stores the value of the count of pixels that have passed the depth test in Slice3. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0..1	63:32	**Depth Count UDW** This register reflects the depth test in slice3 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.
	31:0	**Depth Count LDW** This register reflects the depth test in slice3 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.

PS Depth Count for Slice4

PS_DEPTH_COUNT_SLICE4 - PS Depth Count for Slice4

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02470h
Name:	PS Depth Count for Slice4
ShortName:	PS_DEPTH_COUNT_SLICE4

This register stores the value of the count of pixels that have passed the depth test in Slice4. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0..1	63:32	**Depth Count UDW** This register reflects the depth test in slice4 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.
	31:0	**Depth Count LDW** This register reflects the depth test in slice4 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.

PS Depth Count for Slice5

PS_DEPTH_COUNT_SLICE5 - PS Depth Count for Slice5	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	024A8h
Name:	PS Depth Count for Slice5
ShortName:	PS_DEPTH_COUNT_SLICE5

This register stores the value of the count of pixels that have passed the depth test in Slice5. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0..1	63:32	**Depth Count UDW** This register reflects the depth test in slice5 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.
	31:0	**Depth Count LDW** This register reflects the depth test in slice5 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.

PS Depth Count for Slice6

PS_DEPTH_COUNT_SLICE6 - PS Depth Count for Slice6	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	025B0h
Name:	PS Depth Count for Slice6
ShortName:	PS_DEPTH_COUNT_SLICE6

This register stores the value of the count of pixels that have passed the depth test in Slice6. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0..1	63:32	**Depth Count UDW** This register reflects the depth test in slice5 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.
	31:0	**Depth Count LDW** This register reflects the depth test in slice5 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.

PS Depth Count for Slice7

PS_DEPTH_COUNT_SLICE7 - PS Depth Count for Slice7	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	025B8h
Name:	PS Depth Count for Slice7
ShortName:	PS_DEPTH_COUNT_SLICE7

This register stores the value of the count of pixels that have passed the depth test in Slice7. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0..1	63:32	**Depth Count UDW** This register reflects the depth test in slice5 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.
	31:0	**Depth Count LDW** This register reflects the depth test in slice5 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.

PS Invocation Count

PS_INVOCATION_COUNT - PS Invocation Count	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02348h

DWord	Bit	Description
0..1	63:32	**PS Invocation Count UDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	**PS Invocation Count LDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Invocation Count for Slice0

PS_INVOCATION_COUNT_SLICE0 - PS Invocation Count for Slice0

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	022C8h
Name:	PS Invocation Count for Slice0
ShortName:	PS_INVOCATION_COUNT_SLICE0

This register stores the value of the count of pixels that get shaded in Slice0. This register is part of the context save and restore. This register should not be programmed by SW.Note: In GT3 mode there are two slices Slice0 (Upper Slice) and Slice1 (Lower slice).

DWord	Bit	Description
0..1	63:32	**PS Invocation Count UDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice0. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	**PS Invocation Count LDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice0. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Invocation Count for Slice1

PS_INVOCATION_COUNT_SLICE1 - PS Invocation Count for Slice1

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	022F0h
Name:	PS Invocation Count for Slice1
ShortName:	PS_INVOCATION_COUNT_SLICE1

This register stores the value of the count of pixels that get shaded in Slice0. This register is part of the context save and restore. This register should not be programmed by SW.Note: In GT3 mode there are two slices Slice0 (Upper Slice) and Slice1 (Lower slice).

DWord	Bit	Description
0..1	63:32	**PS Invocation Count UDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice1. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	**PS Invocation Count LDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice1. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Invocation Count for Slice2

PS_INVOCATION_COUNT_SLICE2 - PS Invocation Count for Slice2

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02448h
Name:	PS Invocation Count for Slice2
ShortName:	PS_INVOCATION_COUNT_SLICE2

This register stores the value of the count of pixels that get shaded in Slice2. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0..1	63:32	**PS Invocation Count UDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice2. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	**PS Invocation Count LDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice2. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Invocation Count for Slice3

PS_INVOCATION_COUNT_SLICE3 - PS Invocation Count for Slice3

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02458h
Name:	PS Invocation Count for Slice3
ShortName:	PS_INVOCATION_COUNT_SLICE3

This register stores the value of the count of pixels that get shaded in Slice3. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0..1	63:32	**PS Invocation Count UDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice3. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	**PS Invocation Count LDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice3. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Invocation Count for Slice4

PS_INVOCATION_COUNT_SLICE4 - PS Invocation Count for Slice4

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02468h
Name:	PS Invocation Count for Slice4
ShortName:	PS_INVOCATION_COUNT_SLICE4

This register stores the value of the count of pixels that get shaded in Slice4. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0..1	63:32	**PS Invocation Count UDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice4. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	**PS Invocation Count LDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice4. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Invocation Count for Slice5

PS_INVOCATION_COUNT_SLICE5 - PS Invocation Count for Slice5

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	024A0h
Name:	PS Invocation Count for Slice5
ShortName:	PS_INVOCATION_COUNT_SLICE5

This register stores the value of the count of pixels that get shaded in Slice5. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0..1	63:32	**PS Invocation Count UDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice4. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	**PS Invocation Count LDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice4. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Invocation Count for Slice6

PS_INVOCATION_COUNT_SLICE6 - PS Invocation Count for Slice6

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	025D0h
Name:	PS Invocation Count for Slice6
ShortName:	PS_INVOCATION_COUNT_SLICE6

This register stores the value of the count of pixels that get shaded in Slice6. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0..1	63:32	**PS Invocation Count UDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice4. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	**PS Invocation Count LDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice4. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Invocation Count for Slice7

PS_INVOCATION_COUNT_SLICE7 - PS Invocation Count for Slice7

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	025D8h
Name:	PS Invocation Count for Slice7
ShortName:	PS_INVOCATION_COUNT_SLICE7

This register stores the value of the count of pixels that get shaded in Slice7. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0..1	63:32	**PS Invocation Count UDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice4. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	**PS Invocation Count LDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice4. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PSR_EVENT

PSR_EVENT

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/WC
Size (in bits):	32
Address:	6F848h-6F84Bh
Name:	Transcoder EDP PSR Event Mask
ShortName:	PSR_EVENT_EDP
Power:	PG1
Reset:	soft

This register captures the event that caused an exit from PSR or PSR2. The exit events will be set by hardware. Software will need to clear these events.

DWord	Bit	Description
0	31:18	**Reserved** Format: MBZ
	17	**PSR2 watch dog timer expire** Access: R/WC This is a sticky bit which is set when the PSR2 watch dog timer expires, causing PSR exit. Clear by writing with a 1. Value 0b: Condition Not Detected Value 1b: Condition Detected
	16	**PSR2 Disable** Access: R/WC This is a sticky bit which is set when the PSR2 is disabled, causing PSR exit. Clear by writing with a 1. Value 0b: Condition Not Detected Value 1b: Condition Detected
	15	**Selective Update Dirty FIFO Underrun** Access: R/WC This is a sticky bit which is set when the selective update dirty/clean FIFO Underruns, causing PSR exit. Clear by writing with a 1.

PSR_EVENT

Value	Name
0b	Condition Not Detected
1b	Condition Detected

14 **Selective Update CRC FIFO Underrun**

Access:	R/WC

This is a sticky bit which is set when the selective update CRC FIFO Underruns, causing PSR exit. Clear by writing with a 1.

Value	Name
0b	Condition Not Detected
1b	Condition Detected

13 **Reserved**

Format:	MBZ

12 **Graphics Reset**

Access:	R/WC

This is a sticky bit which is set when a graphics reset causes PSR exit. Clear by writing with a 1.

Value	Name
0b	Condition Not Detected
1b	Condition Detected

11 **PCH Interrupt**

Access:	R/WC

This is a sticky bit which is set when a PCH Interrupt causes PSR exit. Clear by writing with a 1.

Value	Name
0b	Condition Not Detected
1b	Condition Detected

10 **Memory Up**

Access:	R/WC

This is a sticky bit which is set when a PCU memup up event causes PSR exit. Clear by writing with a 1.

Value	Name
0b	Condition Not Detected
1b	Condition Detected

9 **Front Buffer Modify**

Access:	R/WC

This is a sticky bit which is set when a front buffer modify causes PSR exit. Clear by writing with a 1.

Value	Name

PSR_EVENT

	0b	Condition Not Detected
	1b	Condition Detected

8 Watch dog timer expire

Access:	R/WC

This is a sticky bit which is set when the PSR watch dog timer expires, causing PSR exit. Clear by writing with a 1.

Value	Name
0b	Condition Not Detected
1b	Condition Detected

7 Reserved

Format:	MBZ

6 Pipe Registers Update

Access:	R/WC

This is a sticky bit which is set when a display pipe register update causes PSR exit. Clear by writing with a 1.

5 Reserved

4 Reserved

3 KVMR session enable

Access:	R/WC

This is a sticky bit which is set when a KVMR session is enabled, causing PSR exit. Clear by writing with a 1.

Value	Name
0b	Condition Not Detected
1b	Condition Detected

2 VBI enable

Access:	R/WC

This is a sticky bit which is set when vblank or vsync interrupt is enabled, causing PSR exit. Clear by writing with a 1.

Value	Name
0b	Condition Not Detected
1b	Condition Detected

1 LPSP mode exit

Access:	R/WC

This is a sticky bit which is set when LPSP mode is exited, causing PSR exit. This bit is reserved for DDIs Clear by writing with a 1.

PSR_EVENT

Value	Name
0b	Condition Not Detected
1b	Condition Detected

0

SRD disable

Access:	R/WC

This is a sticky bit which is set when SRD enable is cleared, causing PSR exit. Clear by writing with a 1.

Value	Name
0b	Condition Not Detected
1b	Condition Detected

PSR_MASK

PSR_MASK	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	60860h-60863h
Name:	Transcoder A PSR Event Mask
ShortName:	PSR_MASK_A
Power:	PG2
Reset:	soft
Address:	61860h-61863h
Name:	Transcoder B PSR Event Mask
ShortName:	PSR_MASK_B
Power:	PG2
Reset:	soft
Address:	62860h-62863h
Name:	Transcoder C PSR Event Mask
ShortName:	PSR_MASK_C
Power:	PG2
Reset:	soft
Address:	6F860h-6F863h
Name:	Transcoder EDP PSR Event Mask
ShortName:	PSR_MASK_EDP
Power:	PG1
Reset:	soft
Some of the masking is controlled here and some in the PIPE_MISC register.	

Restriction
Only bit 30 (Idle Frame Override) can be changed while PSR or PSR2 is enabled. The other fields must not be changed while PSR or PSR2 is enabled.

<table>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td rowspan="8">0</td><td>31:30</td><td>Idle Frame Override
This field overrides the entry/exit conditions to force PSR or PSR2 Deep Sleep entry/exit.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th></tr>
<tr><td>00b,01b</td><td>No Override</td><td>Do not override. Use regular entry and exit conditions.</td></tr>
<tr><td>10b</td><td>Force Idle Frame</td><td>Force Idle Frames to force PSR entry or PSR2 Deep Sleep</td></tr>
<tr><td>11b</td><td>Force Non-Idle Frame</td><td>Force Non-Idle Frames to force PSR exit or exit from PSR2 Deep Sleep</td></tr>
</table></td></tr>
<tr><td>29</td><td>Reserved
<table>
<tr><td>Format:</td><td>MBZ</td></tr>
</table></td></tr>
<tr><td>28</td><td>Mask Max Sleep
This field controls the mask for the max sleep time event.
<table>
<tr><th>Value</th><th>Name</th></tr>
<tr><td>0b</td><td>Not Masked</td></tr>
<tr><td>1b</td><td>Masked</td></tr>
</table></td></tr>
<tr><td>27</td><td>Mask LPSP
<table>
<tr><td></td><td></td></tr>
</table>
This field controls the mask for the low power single pipe event. This field is ignored by transcoder A/B/C.
<table>
<tr><th>Value</th><th>Name</th></tr>
<tr><td>0b</td><td>Not Masked</td></tr>
<tr><td>1b</td><td>Masked</td></tr>
</table></td></tr>
<tr><td>26</td><td>Mask Memup
This field controls the mask for the memory up event.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th></tr>
<tr><td>0b</td><td>Not Masked</td><td></td></tr>
<tr><td>1b</td><td>Masked [Default]</td><td>Masked - will not be considered in PSR idleness tracking (default)</td></tr>
</table></td></tr>
<tr><td>25</td><td>Mask Hotplug
This field controls the mask for the hotplug event.Not used in PSR2 Deep Sleep entry/exit.
<table>
<tr><th>Value</th><th>Name</th></tr>
<tr><td>0b</td><td>Not Masked</td></tr>
<tr><td>1b</td><td>Masked</td></tr>
</table></td></tr>
<tr><td>24</td><td>Mask FBC Modify
This field controls the mask for the FBC front buffer modify event.
<table>
<tr><th>Value</th><th>Name</th></tr>
<tr><td>0b</td><td>Not Masked</td></tr>
<tr><td>1b</td><td>Masked</td></tr>
</table></td></tr>
<tr><td>23:17</td><td>Reserved</td></tr>
</table>

PSR_MASK

	Format:	MBZ

16 Reserved

15 Exit on Pixel Underrun

This field controls the mask for exit on pixel underrun.

Value	Name
0b	Not Masked
1b	Masked **[Default]**

14:1 Reserved

Format:	MBZ

0 Global Mask

This field is no longer used. The global mask function moved to 0x42084 bit 0.

Value	Name
0b	Not Masked
1b	Masked

PSR2_CTL

PSR2_CTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6F900h-6F903h
Name:	Transcoder EDP PSR2 Control
ShortName:	PSR2_CTL_EDP
Power:	PG1
Reset:	soft

Programming Notes

To use FBC modification tracking for idleness calculations when FBC is disabled, program FBC_CTL CPU Fence Enable, FBC_CONTROL_SA_REGISTER, FBC_CPU_FENCE_OFFSET_REGISTER, FBC_RT_BASE_ADDR_REGISTER, and BLITTER_TRACKING_REGISTER as they are programmed when FBC is enabled.

Restriction

- PSR needs to be enabled only when at least one plane is enabled.
- PSR2 is limited to 24bpp 8:8:8, even when using the manual tracking mode.
- Only the PSR2 Enable can be changed while PSR2 is enabled. The other fields must not be changed while PSR2 is enabled. Selective Update Tracking Enable must be set before or along with PSR2 enable
- PSR2 is supported for pipe active sizes up to 4096 pixels wide and 2304 lines tall.

DWord	Bit	Description
0	31	**PSR2 Enable** This bit enables Revision 2.0 of the Panel Self Refresh function. Updates will take place at the start of the next vertical blank. The port will send PSR2 VDMs while enabled.

Value	Name
0b	Disable
1b	Enable

Restriction

- PSR2 must not be enabled when the PSR Setup time from DPCD 00071h is greater than the time for vertical blank minus one line.
- PSR2 must not be enabled together with Interlacing, Black Frame Insertion (BFI), Compression Mode, or S3D.

PSR2_CTL

30	**Selective Update Tracking Enable** Access: Double Buffered Double Buffer Update Point: Start of vertical blank OR transcoder disabled This field enables the Selective Update Tracking Mechanism. Updates to this field will take effect at the next vertical blank. 0b Disable 1b Enable **Restriction** This field must be enabled anytime before PSR2 Enable. It must be disabled anytime after PSR2 disable.
29	**Context restore to PSR2 Deep Sleep State** This field restores PSR2 into Deep Sleep State 0b Disable 1b Enable **Restriction** This bit should only be used with context save restore.
28	**Reserved** Format: MBZ
27	**Reserved** Format: MBZ
26	**Y-coordinate valid** This field selects whether PSR2 Y-coordinate valid behaves as per eDP 1.4a 0b Include Y-coordinate valid eDP1.4a 1b Do not include Y-coordinate valid eDP 1.4
25	**Y-coordinate enable** This field selects whether PSR2 VSC packet will include vertical line count.

	0b	Do not include count
	1b	Include count

24:20 Max SU Disable Time

Default Value:	00000b Disabled

This field is the maximum time to spend in PSR2 Selective update without fetching a full frame. It is programmed in increments of sixty frames. Programming all 1s gives 31x60 frames time.

Restriction
Programming all 0s disable the forced fetch of a full frame in SU.

19:16 Reserved

Format:	MBZ

15 Reserved

Format:	MBZ

14:13 IO buffer Wake

This field selects the number of lines before the Selective Update Region to wake the IO Buffers.

Value	Name
00b	8 lines
01b	7 lines **[Default]**
10b	6 lines
11b	5 lines

12:11 Fast Wake

This field selects the number of lines before the Selective Update Region to send the Fast Wake.

Value	Name
00b	8 lines
01b	7 lines **[Default]**
10b	6 lines
11b	5 lines

10 Reserved

Format:	MBZ

9:8 TP2 Time

PSR2_CTL

This field selects the TP2 time when training the link on exit from PSR2 DeepSleep (waking).

Value	Name
00b	500us
01b	100us
10b	2.5ms
11b	50us

7:4 **Frames Before SU Entry**

Default Value:	0001b 1 Frames Before SU Entry

This field is the number of frames it takes to enter into Selective Update when PSR2 is enabled.

3:0 **Idle Frames**

This field is the number of idle frames required before entering PSR2 Deep Sleep.

Value	Name
0000b	Deep Sleep Disabled
0001b	1 idle frame **[Default]**

PSR2_MAN_TRK_CTL

PSR2_MAN_TRK_CTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6F910h-6F913h
Name:	Transcoder EDP PSR2 Manual Tracking Control
ShortName:	PSR2_MAN_TRK_CTL_EDP
Power:	PG1
Reset:	soft

Programming Notes

The frame is divided into blocks of four scan lines each. Software must provide starting and ending block address of the selective update region. There can be only one selective update region in a frame.

DWord	Bit	Description
0	31	**PSR2 Manual Tracking Enable** **Description** This bit enables the manual tracking mode for PSR2 Selective Update. Register 0x42080 bit 1 controls how hardware tracking is used when manual tracking is enabled. 0x42080 bit 1 = 0; Hardware tracking of the selective update region is still used when manual tracking is enabled. Selective update will use the logical OR of the hardware detected update regions and the manual tracking region. 0x42080 bit 1 = 1; Hardware tracking of the selective update region will be ignored when manual tracking is enabled. Selective update will use only the manual tracking region. **Value** / **Name** 0b – Disable 1b – Enable
	30:21	**SU Region Start Address** This field indicates the starting block address of the selective update region.

PSR2_MAN_TRK_CTL		
	20:11	**SU Region End Address** This field indicates the ending block address of the selective update region.
	10:0	**Reserved** Format: MBZ

PSR2_STATUS

PSR2_STATUS

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	6F940h-6F943h
Name:	Transcoder EDP PSR2 Status
ShortName:	PSR2_STATUS_EDP
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:28	**PSR2 State** Access: RO This field indicates the live state of PSR2

Value	Name	Description
0000b	IDLE	Reset state
0001b	CAPTURE	Send capture frame
0010b	CPTURE_FS	Fast sleep after capture frame is sent
0011b	SLEEP	Selective Update
0100b	BUFON_FW	Turn Buffer on and Send Fast wake
0101b	ML_UP	Turn Main link up and send SR
0110b	SU_STANDBY	Selective update or Standby state
0111b	FAST_SLEEP	Send Fast sleep
1000b	DEEP_SLEEP	Enter Deep sleep
1001b	BUF_ON	Turn ON IO Buffer
1010b	TG_ON	Turn ON Timing Generator
Others	Reserved	Reserved

	27:26	**Link Status** Access: RO This field indicates the live status of the link.

Value	Name	Description
00b	Full Off	Link is fully off

PSR2_STATUS

01b	Full On	Link is fully on
10b	Standby	Link is in standby
11b	Reserved	Reserved

25 Reserved

Format:	MBZ

24:20 Max Sleep Time Counter

Access:	RO

This field provides the live status of the sleep time counter.

19:16 PSR2 Deep Sleep Entry Count

Access:	RO

The value in this register represents the number of times PSR2 Deep Sleep has been entered. The count will increment with each entry. After reaching the maximum count value the counter will rollover and continue from 0.

15:10 Reserved

Format:	MBZ

9 Reserved

8 Sending TP2

Access:	RO

This field indicates if TP2 is currently being sent.

Value	Name	Description
0b	Not Sending	Not sending TP2
1b	Sending	Sending TP2

7 Reserved

6 Reserved

5 PSR2 deep Sleep Entry Completion

Access:	R/WC

This is a sticky bit which is set on PSR2 deep sleep entry completion.Clear this bit by writing a 1b to it.

Value	Name
0b	Not complete
1b	Complete

4 PSR2 SU Entry Completion

PSR2_STATUS

		Access: R/WC This is a sticky bit which is set on PSR2 SU entry completion.Clear this bit by writing a 1b to it. **Value** / **Name** 0b – Not complete 1b – Complete
	3:0	**Idle Frame Counter** Access: RO This field provides the live status of the idle frame counter.

PSR2_SU_ECC_STAT

PSR2_SU_ECC_STAT	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/WC
Size (in bits):	32
Address:	6FA64h-6FA67h
Name:	PSR2_SU ECC Status
ShortName:	PSR2_SU_ECC_STAT
Power:	PG1
Reset:	soft

Description
Each of these fields is a sticky bit that gives the ECC error status for a particular PSR2 memory bank.
A '1' in a bit indicates that ECC detected an error. A write of '1' to a bit will clear the bit. Single errors are corrected by ECC. Double errors are not correctable.

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23	**Double Error Bank 7**
	22	**Double Error Bank 6**
	21	**Double Error Bank 5**
	20	**Double Error Bank 4**
	19	**Double Error Bank 3**
	18	**Double Error Bank 2**
	17	**Double Error Bank 1**
	16	**Double Error Bank 0**

PSR2_SU_ECC_STAT		
	15:8	**Reserved** Format: MBZ
	7	**Single Error Bank 7**
	6	**Single Error Bank 6**
	5	**Single Error Bank 5**
	4	**Single Error Bank 4**
	3	**Single Error Bank 3**
	2	**Single Error Bank 2**
	1	**Single Error Bank 1**
	0	**Single Error Bank 0**

PSR2_SU_STATUS

PSR2_SU_STATUS	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	96
Address:	6F914h-6F91Fh
Name:	Transcoder EDP PSR2 Selective Update Status
ShortName:	PSR2_SU_STATUS
Power:	PG1
Reset:	soft

A frame is divided into selective update blocks of four scan lines each. This register provies the count of the number of selective update blocks per frame, for the last eight frames

DWord	Bit	Description
0	31:30	**Reserved** Format: MBZ
	29:20	**Number of SU blocks in frame N - 2** This field indicates the number of selective update blocks in frame N - 1.
	19:10	**Number of SU blocks in frame N - 1** This field indicates the number of selective update blocks in frame N - 1.
	9:0	**Number of SU blocks in frame N** This field indicates the number of selective update blocks in frame N.
1	31:30	**Reserved** Format: MBZ
	29:20	**Number of SU blocks in frame N - 5** This field indicates the number of selective update blocks in frame N - 1.
	19:10	**Number of SU blocks in frame N - 4** This field indicates the number of selective update blocks in frame N - 1.
	9:0	**Number of SU blocks in frame N - 3** This field indicates the number of selective update blocks in frame N.
2	31:20	**Reserved** Format: MBZ
	19:10	**Number of SU blocks in frame N - 7** This field indicates the number of selective update blocks in frame N - 1.
	9:0	**Number of SU blocks in frame N - 6**

PSR2_SU_STATUS		
		This field indicates the number of selective update blocks in frame N.

PTBR Number Of Pages Recorded

PTBR_NUM_PAGES_RECORDED_REGISTER - PTBR Number Of Pages Recorded

Register Space:	MMIO: 0/2/0
Source:	PositionCS
Size (in bits):	32
Address:	18594h
Name:	Register Template Address
ShortName:	PTBR_NUM_PAGES_RECORDED_REGISTER

This is a running count of number of pages allocated by the OVR unit for the visibility data. This includes pages that could have been allocated but were not allocated because the OVR unit early terminated the pages with "out of memory" marker. This register is engine context save/restored.

DWord	Bit	Description
0	31:17	**Reserved** Default Value: 000000000000000b Access: RO
	16:0	**PTBR_NUM_PAGES_RECORDED** Default Value: 0h Access: R/W Format: U17 This is a running count of number of pages allocated by the OVR unit for the visibility data. This includes pages that could have been allocated but were not allocated because the OVR unit early terminated the pages with "out of memory" marker. **Programming Notes** SW must not write to this register.

PTBR Page Pool Size Register

PTBR_PAGE_POOL_SIZE_REGISTER - PTBR Page Pool Size Register

Register Space:	MMIO: 0/2/0
Source:	PositionCS
Size (in bits):	32
Address:	18590h
Name:	Register Template Address
ShortName:	PTBR_PAGE_POOL_SIZE_REGISTER

Indicates the size of the PTBR Page Pool Size allocated by SW. The page pool size is with respect to the PTBR_PAGE_POOL_BASE_ADDRESS programmed through 3DSTATE_PTBR_PAGE_POOL_BASE_ADDRESS command. SW can do multiple writes to this register with the increased page pool size as it allocates more pages to the PTBR page pool.
Coming out of reset or on executing PTBR_PAGE_POOL_RESTART by 3DSTATE_PTRB_PAGE_POOL_BASE_ADDRESS command, HW initializes PTBR_PAGE_POOL_SIZE to 0x0. HW on detecting a write to this register compares its current PTBR_PAGE_POOL_SIZE with that of the value programmed in this register to add more pages to the Free-List and updates itself with the latest value.
This is an non-privileged register and engine context save/restored by HW.

Programming Notes

- SW must not write a value to this register less than the existing value. SW must use the 'Restart' field of the 3DSTATE_PTBR_PAGE_POOL_ADDRESS command to decrease the size of the pool.
- SW must always program PTBR_PAGE_POOL_SIZE_REGISTER through MI_LOAD_REGISTER_IMM command or anyother MI command to load register in the command sequence.
- SW must ensure following state are set in HW prior to programming this register: 3DSTATE_PTBR_PAGE_POOL_BASE_ADDRESS 3DSTATE_PTBR_FEE_LIST_BASE_ADDRESS

DWord	Bit	Description
0	31:16	**Reserved** Default Value: 0000000000000000b Access: RO
	15:0	**PTBR_PAGE_POOL_SIZE** Default Value: 0h Access: R/W Format: U16-1 Indicates the PTBR page pool size (4KB granularity). A value of '0x0' indicates a single page and a value of 99h indicates 154 pages are available in the page pool for use by HW. Valid

PTBR_PAGE_POOL_SIZE_REGISTER - PTBR Page Pool Size Register		
		Range [0..65534].

PTE SW Fault Repair High

PTESWC_H - PTE SW Fault Repair High		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	04104h	
DWord	**Bit**	**Description**
0	31:0	**PTE SW Fault Repair High** Default Value: 00000000h Access: R/W Fixed PTE entry is written by SW here.

PTE SW Fault Repair Low

PTESWC_L - PTE SW Fault Repair Low		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	04100h	
DWord	**Bit**	**Description**
0	31:0	**PTE SW Fault Repair Low** Access: R/W Fixed PTE entry is written by SW here.

PWR_WELL_CTL_AUX

PWR_WELL_CTL_AUX

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32

Address:	45440h-45443h
Name:	Power Well Control AUX 1
ShortName:	PWR_WELL_CTL_AUX1
Power:	PG0
Reset:	soft

Address:	45444h-45447h
Name:	Power Well Control AUX 2
ShortName:	PWR_WELL_CTL_AUX2
Power:	PG0
Reset:	soft

This register is used for display power control. There are multiple instances of this register format to allow software components to have parallel control of the display power.
PWR_WELL_CTL_AUX1 is generally used for BIOS to control power.
PWR_WELL_CTL_AUX2 is generally used for driver to control power.
The power enable requests from all sources are logically ORd together to enable the power, so the power will only disable after all sources have requested the power to disable.
When a power well is disabled (powered down), access to any registers in the power well will complete, but write data will be dropped and read data will be all zeroes.
The display connections diagram indicates which functional blocks are contained in each power well. The display MMIO register specification has a field for each register to indicate which power well it is in.

Restriction
The power request field must not be changed for a resource while a power enable/disable for that resource is currently in progress, as indicated by power well state for that resource.

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23	**AUX TBT4 IO Power Request** Access: R/W

This field requests power for this Thunderbolt Aux IO to enable or disable. This is used for typeC ports that are in thunderbolt mode.

Value	Name
0b	Disable
1b	Enable

22 **AUX TBT4 IO Power State**

Access:	RO

This field indicates the status of power for this Thunderbolt Aux IO.

Value	Name
0b	Disable
1b	Enable

21 **AUX TBT3 IO Power Request**

Access:	R/W

This field requests power for this Thunderbolt Aux IO to enable or disable. This is used for typeC ports that are in thunderbolt mode.

Value	Name
0b	Disable
1b	Enable

20 **AUX TBT3 IO Power State**

Access:	RO

This field indicates the status of power for this Thunderbolt Aux IO.

Value	Name
0b	Disable
1b	Enable

19 **AUX TBT2 IO Power Request**

Access:	R/W

This field requests power for this Thunderbolt Aux IO to enable or disable. This is used for typeC ports that are in thunderbolt mode.

Value	Name
0b	Disable
1b	Enable

18 **AUX TBT2 IO Power State**

PWR_WELL_CTL_AUX

		Access: RO This field indicates the status of power for this Thunderbolt Aux IO. Value: 0b – Disable Value: 1b – Enable
	17	**AUX TBT1 IO Power Request** Access: R/W This field requests power for this Thunderbolt Aux IO to enable or disable. This is used for typeC ports that are in thunderbolt mode. Value: 0b – Disable Value: 1b – Enable
	16	**AUX TBT1 IO Power State** Access: RO This field indicates the status of power for this Thunderbolt Aux IO. Value: 0b – Disable Value: 1b – Enable
	15:12	**Reserved** Format: MBZ
	11	**AUX F IO Power Request** Access: R/W This field requests power for this USBC Aux IO to enable or disable. This is used for typeC ports that are not in thunderbolt mode. Value: 0b – Disable Value: 1b – Enable
	10	**AUX F IO Power State** Access: RO This field indicates the status of power for this USBC Aux IO. Value: Name

0b	Disable
1b	Enable

9 AUX E IO Power Request

Access:	R/W

This field requests power for this USBC Aux IO to enable or disable. This is used for typeC ports that are not in thunderbolt mode.

Value	Name
0b	Disable
1b	Enable

8 AUX E IO Power State

Access:	RO

This field indicates the status of power for this USBC Aux IO.

Value	Name
0b	Disable
1b	Enable

7 AUX D IO Power Request

Access:	R/W

This field requests power for this USBC Aux IO to enable or disable. This is used for typeC ports that are not in thunderbolt mode.

Value	Name
0b	Disable
1b	Enable

6 AUX D IO Power State

Access:	RO

This field indicates the status of power for this USBC Aux IO.

Value	Name
0b	Disabled
1b	Enabled

5 AUX C IO Power Request

Access:	R/W

This field requests power for this USBC Aux IO to enable or disable. This is used for typeC ports that are not in thunderbolt mode.

PWR_WELL_CTL_AUX

Value	Name
0b	Disable
1b	Enable

4 AUX C IO Power State

Access:	RO

This field indicates the status of power for this USBC Aux IO.

Value	Name
0b	Disabled
1b	Enabled

3 AUX B IO Power Request

Access:	R/W

This field requests power for this Aux IO to enable or disable.

Value	Name
0b	Disable
1b	Enable

2 AUX B IO Power State

Access:	RO

This field indicates the status of power for this Aux IO.

Value	Name
0b	Disabled
1b	Enabled

1 AUX A IO Power Request

Access:	R/W

This field requests power for this Aux IO to enable or disable.

Value	Name
0b	Disable
1b	Enable

0 AUX A IO Power State

Access:	RO

This field indicates the status of power for this Aux IO.

Value	Name

PWR_WELL_CTL_AUX			
		0b	Disabled
		1b	Enabled

PWR_WELL_CTL_DDI

PWR_WELL_CTL_DDI

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32

Address:	45450h-45453h
Name:	Power Well Control DDI 1
ShortName:	PWR_WELL_CTL_DDI1
Power:	PG0
Reset:	soft

Address:	45454h-45457h
Name:	Power Well Control DDI 2
ShortName:	PWR_WELL_CTL_DDI2
Power:	PG0
Reset:	soft

This register is used for display power control. There are multiple instances of this register format to allow software components to have parallel control of the display power.
PWR_WELL_CTL _DDI1 is generally used for BIOS to control power.
PWR_WELL_CTL_DDI2 is generally used for driver to control power.
The power enable requests from all sources are logically ORd together to enable the power, so the power will only disable after all sources have requested the power to disable.
When a power well is disabled (powered down), access to any registers in the power well will complete, but write data will be dropped and read data will be all zeroes.
The display connections diagram indicates which functional blocks are contained in each power well. The display MMIO register specification has a field for each register to indicate which power well it is in.

Restriction
The power request field must not be changed for a resource while a power enable/disable for that resource is currently in progress, as indicated by power well state for that resource.

DWord	Bit	Description
0	31:12	**Reserved** Format: MBZ
	11	**DDI F IO Power Request** Access: R/W

This field requests power for DDI F IO to enable or disable.

Value	Name
0b	Disable
1b	Enable

10 **DDI F IO Power State**

Access:	RO

This field indicates the status of power for DDI F IO.

Value	Name
0b	Disable
1b	Enable

9 **DDI E IO Power Request**

Access:	R/W

This field requests power for DDI E IO to enable or disable.

Value	Name
0b	Disable
1b	Enable

8 **DDI E IO Power State**

Access:	RO

This field indicates the status of power for DDI E IO.

Value	Name
0b	Disabled
1b	Enabled

7 **DDI D IO Power Request**

Access:	R/W

This field requests power for DDI D IO to enable or disable.

Value	Name
0b	Disable
1b	Enable

6 **DDI D IO Power State**

Access:	RO

This field indicates the status of power for DDI D IO.

PWR_WELL_CTL_DDI

Value	Name
0b	Disabled
1b	Enabled

5 DDI C IO Power Request

Access:	R/W

This field requests power for DDI C IO to enable or disable.

Value	Name
0b	Disable
1b	Enable

4 DDI C IO Power State

Access:	RO

This field indicates the status of power for DDI C IO.

Value	Name
0b	Disabled
1b	Enabled

3 DDI B IO Power Request

Access:	R/W

This field requests power for DDI B IO to enable or disable.

Value	Name
0b	Disable
1b	Enable

2 DDI B IO Power State

Access:	RO

This field indicates the status of power for DDI B IO.

Value	Name
0b	Disabled
1b	Enabled

1 DDI A IO Power Request

Access:	R/W

This field requests power for DDI A IO to enable or disable.

Value	Name
0b	Disable
1b	Enable

0 DDI A IO Power State

PWR_WELL_CTL_DDI

Access:	RO

This field indicates the status of power for DDI A IO.

Value	Name
0b	Disabled
1b	Enabled

PWR_WELL_CTL

PWR_WELL_CTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	45400h-45403h
Name:	Power Well Control 1
ShortName:	PWR_WELL_CTL1
Power:	PG0
Reset:	soft
Address:	45404h-45407h
Name:	Power Well Control 2
ShortName:	PWR_WELL_CTL2
Power:	PG0
Reset:	soft

This register is used for display power control. There are multiple instances of this register format to allow software components to have parallel control of the display power.
PWR_WELL_CTL1 is generally used for BIOS to control power.
PWR_WELL_CTL2 is generally used for driver to control power.
The power enable requests from all sources are logically ORd together to enable the power, so the power will only disable after all sources have requested the power to disable.
When a power well is disabled (powered down), access to any registers in the power well will complete, but write data will be dropped and read data will be all zeroes.
The display connections diagram indicates which functional blocks are contained in each power well. The display MMIO register specification has a field for each register to indicate which power well it is in.

Restriction
The power request field must not be changed for a resource while a power enable/disable for that resource is currently in progress, as indicated by power well state for that resource.
Power wells must be enabled and disabled following the display initialization and mode set sequences.

DWord	Bit	Description
0	31:8	**Reserved** Format: MBZ

PWR_WELL_CTL

	7	**Power Well 4 Request** Access: R/W This field requests power well #4 to enable or disable. 0b – Disable 1b – Enable
	6	**Power Well 4 State** Access: RO This field indicates the status of power well #4. 0b – Disabled 1b – Enabled
	5	**Power Well 3 Request** Access: R/W This field requests power well #3 to enable or disable. 0b – Disable 1b – Enable
	4	**Power Well 3 State** Access: RO This field indicates the status of power well #3. 0b – Disabled 1b – Enabled
	3	**Power Well 2 Request** Access: R/W This field requests power well #2 to enable or disable. 0b – Disable 1b – Enable
	2	**Power Well 2 State**

PWR_WELL_CTL

		Access: RO

This field indicates the status of power well #2.

Value	Name
0b	Disabled
1b	Enabled

1 — Power Well 1 Request

Access: R/W

This field requests power well #1 to enable or disable.

Value	Name
0b	Disable
1b	Enable

0 — Power Well 1 State

Access: RO

This field indicates the status of power well #1.

Value	Name
0b	Disabled
1b	Enabled

PWRCTXSAVE Message Register for Boot Controller Unit

MSG_PWRCTXSAVE_MBC - PWRCTXSAVE Message Register for Boot Controller Unit

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0850Ch

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].
To **set** bit0, for example, the data would be 0x0001_0001.
To **clear** bit0, for example, the data would be 0x0001_0000.
Note that mask bit is the data bit offset + 16.
Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description
0	15:10	**RSVD** Access: RO
	9	**Power Context Save Request** Access: R/W Power Context Save Request 1'b0: Power context save is not being requested (default). 1'b1: Power context save is being requested. Unit needs to self-clear this bit upon sampling.
	8:0	**QWord Credits for Power Context Save Request** Access: R/W QWord Credits for Power Context Save Request. Minimum Credits = 1: Unit may send 1 QWord pair (enough for first LRI at least). Maximum Credits = 511: Unit may send 511 QWord pairs. A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and consume one QWord credit. Only valid with PWRCTXSAVE_REQ (Bit9).

RC6 Context Base

RC6CTXBASE - RC6 Context Base		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	64	
Address:	00D48h	
RC6 Location		
DWord	**Bit**	**Description**
0	31:12	**RC6 Memory Base Low** Access: R/W Lock This field is used to set the base of memory where the RC6 power context will be saved This value MUST be above the base and below the top of stolen memory This register is locked (becomes read-only) when RC6MEMLOCK is 1
	11:1	**Reserved** Access: RO
	0	**RC6Context Base Register Lock** Access: R/W Lock 1'b0 : All fields of this register are writable (default) 1'b1 : This register is Read Only BIOS must set this bit to prevent further changes
1	31:0	**RC6 Memory Base High** Access: R/W Lock This field is used to set the base of memory where the RC6 power context will be saved. This value MUST be above the base and below the top of stolen memory. This High Dword must be written before the low word is written with RC6MEMLOCK of 1. This register is locked (becomes read-only) when RC6MEMLOCK is 1

RC6 LOCATION

RC6LOCATION - RC6 LOCATION		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	00D40h	
RC6 Location		
DWord	**Bit**	**Description**
0	31	**RC6Context Location Lock** Access: R/W Lock 1'b0 : All fields of this register are writable (default) 1'b1 : This register is Read Only
	30:1	**Reserved** Access: RO
	0	**RC6Context Location** Access: RO 1'b1 : Send context data to DRAM location specified in RC6MEMBASE (default) This will be tied to 1 with as there is no option to save context to a SRAM

Reported BitRateControl Convergence Status

MFX_VP8_BRC_CONVERGENCE_STATUS - Reported BitRateControl Convergence Status

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	1C928h
ShortName:	MFX_VP8_BRC_CONVERGENCE_STATUS_VD2

This register stores BitRateControl Convergence Status.

DWord	Bit	Description
0	31	**Segment3 Qindex Polarity Change** Format: U1 This bit indicates current pass has CumulativeDeltaQindex Polarity Change. This feature is not validated.
	30:28	**Segment3 Num-Pass with Polarity Change** Format: U3 This bit indicates the number of Multipass with CumulativeDeltaQindex Polarity Change in segment3. This feature is not validated.
	27	**Segment2 Qindex Polarity Change** Format: U1 This bit indicates current pass has CumulativeDeltaQindex Polarity Change. This feature is not validated.
	26:24	**Segment2 Num-Pass with Polarity Change** Format: U3 This bit indicates the number of Multipass with CumulativeDeltaQindex Polarity Change in segment2. This feature is not validated.
	23	**Segment1 Qindex Polarity Change** Format: U1 This bit indicates current pass has CumulativeDeltaQindex Polarity Change. This feature is not validated.

MFX_VP8_BRC_CONVERGENCE_STATUS - Reported BitRateControl Convergence Status

	22:20	**Segment1 Num-Pass with Polarity Change** Format: U3 This bit indicates the number of Multipass with CumulativeDeltaQindex Polarity Change in segment1. This feature is not validated.
	19	**Segment0 Qindex Polarity Change** Format: U1 This bit indicates current pass has CumulativeDeltaQindex Polarity Change. This feature is not validated.
	18:16	**Segment0 Num-Pass with Polarity Change** Format: U3 This bit indicates the number of Multipass with CumulativeDeltaQindex Polarity Change in segment0. This feature is not validated.
	15:12	**Reserved** Format: MBZ
	11:8	**Total Num of Pass** Format: U4 This bit indicates the number of Multipass including current frame. Note that Initial Pass is not counted.
	7:2	**Reserved** Format: MBZ
	1	**Overflow OR Underflow Flag** Format: U1 This bit indicates the current frame has BRC overflow OR underflow.
	0	**MB Max. Conformance Flag** Format: U1 This contains flag that indicate Inter MB or Intra MB Max. Conformance is not met. This is legacy support and this feature is not validated.

Reported BitRateControl CumulativeDeltaLoopFilter and LoopFilter 01

MFX_VP8_BRC_CUMULATIVE_D_LOOP_FILTER01 - Reported BitRateControl CumulativeDeltaLoopFilter and LoopFilter 01

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	1C920h

This register stores per segement Bit Rate Control DeltaLoopFilter.

DWord	Bit	Description
0	31	**Reserved** Format: MBZ
	30:24	**Segment1 CumulativeDeltaLoopFilter** Format: S6 This contains Segment1 CumulativeDeltaLoopFilter in Bit Rate Control. It accumulates all Segment1 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done.
	23:22	**Reserved** Format: MBZ
	21:16	**Segment1 LoopFilter** Format: U6 This contains Segment1 LoopFilter used in current frame. This register is valid after a BRC pass is done.
	15	**Reserved** Format: MBZ
	14:8	**Segment0 CumulativeDeltaLoopFilter** Format: S6 This contains Segment0 CumulativeDeltaLoopFilter in Bit Rate Control. It accumulates all Segment0 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done. If

MFX_VP8_BRC_CUMULATIVE_D_LOOP_FILTER01 - Reported BitRateControl CumulativeDeltaLoopFilter and LoopFilter 01		
		Segmentation is not enabled, this field reflects CumulativeDeltaLoopFilter. If Segmentation is enabled, this field reflects Segment0 CumulativeDeltaLoopFilter.
	7:6	**Reserved** Format: MBZ
	5:0	**Segment0 LoopFilter** Format: U6 This contains Segment0 LoopFilter used in current frame. This register is valid after a BRC pass is done. If Segmentation is not enabled, this field reflects LoopFilter. If Segmentation is enabled, this field reflects Segment0 LoopFilter.

Reported BitRateControl CumulativeDeltaLoopFilter and LoopFilter 23

MFX_VP8_BRC_CUMULATIVE_D_LOOP_FILTER23 - Reported BitRateControl CumulativeDeltaLoopFilter and LoopFilter 23

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	1C924h

This register stores per segement Bit Rate Control DeltaLoopFilter.

DWord	Bit	Description
0	31	**Reserved** Format: MBZ
	30:24	**Segment3 CumulativeDeltaLoopFilter** Format: S6 This contains Segment3 CumulativeDeltaLoopFilter in Bit Rate Control. It accumulates all Segment3 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done.
	23:22	**Reserved** Format: MBZ
	21:16	**Segment3 LoopFilter** Format: U6 This contains Segment3 LoopFilter used in current frame. This register is valid after a BRC pass is done.
	15	**Reserved** Format: MBZ
	14:8	**Segment2 CumulativeDeltaLoopFilter** Format: S6 This contains Segment2 CumulativeDeltaLoopFilter in Bit Rate Control. It accumulates all Segment2 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done.
	7:6	**Reserved**

MFX_VP8_BRC_CUMULATIVE_D_LOOP_FILTER23 - Reported BitRateControl CumulativeDeltaLoopFilter and LoopFilter 23			
		Format:	MBZ
	5:0	**Segment2 LoopFilter** Format: U6 This contains Segment2 LoopFilter used in current frame. This register is valid after a BRC pass is done.	

Reported BitRateControl CumulativeDeltaQindex and Qindex 01

MFX_VP8_BRC_CUMULATIVE_DQ_INDEX01 - Reported BitRateControl CumulativeDeltaQindex and Qindex 01

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	12918h
ShortName:	MFX_VP8_BRC_CUMULATIVE_DQ_INDEX01_VB0
Address:	1C918h
ShortName:	MFX_VP8_BRC_CUMULATIVE_DQ_INDEX01_VB1

This register stores per segement Bit Rate Control CumulativeDeltaQindex.

DWord	Bit	Description
0	31:24	**Segment1 CumulativeDeltaQindex** Format: S7 This contains Segment1 CumulativeDeltaQindex in Bit Rate Control. It accumulates all Segment1 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done.
	23	**Reserved** Format: MBZ
	22:16	**Segment1 Qindex** Format: U7 This contains Segment1 Qindex used in current frame. This register is valid after a BRC pass is done.
	15:8	**Segment0 CumulativeDeltaQindex** Format: S7 TThis contains Segment0 CumulativeDeltaQindex in Bit Rate Control. It accumulates all Segment0 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done. If Segmentation is not enabled, this field reflects CumulativeDeltaQindex. If Segmentation is enabled, this field reflects Segment0 CumulativeDeltaQindex.

MFX_VP8_BRC_CUMULATIVE_DQ_INDEX01 - Reported BitRateControl CumulativeDeltaQindex and Qindex 01

	7	**Reserved** Format: MBZ
	6:0	**Segment0 Qindex** Format: U7 This contains Segment0 Qindex used in current frame. This register is valid after a BRC pass is done. If Segmentation is not enabled, this field reflects Qindex. If Segmentation is enabled, this field reflects Segment0 Qindex.

Reported BitRateControl CumulativeDeltaQindex and Qindex 23

MFX_VP8_BRC_CUMULATIVE_DQ_INDEX23 - Reported BitRateControl CumulativeDeltaQindex and Qindex 23

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	1291Ch
ShortName:	MFX_VP8_BRC_CUMULATIVE_DQ_INDEX23_VB0
Address:	1C91Ch
ShortName:	MFX_VP8_BRC_CUMULATIVE_DQ_INDEX23_VB1

This register stores per segement Bit Rate Control CumulativeDeltaQindex and Qindex.

DWord	Bit	Description
0	31:24	**Segment3 CumulativeDeltaQindex** Format: S7 This contains Segment3 CumulativeDeltaQindex in Bit Rate Control. It accumulates all Segment3 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done.
	23	**Reserved** Format: MBZ
	22:16	**Segment3 Qindex** Format: U7 This contains Segment3 Qindex used in current frame. This register is valid after a BRC pass is done.
	15:8	**Segment2 CumulativeDeltaQindex** Format: S7 This contains Segment2 CumulativeDeltaQindex in Bit Rate Control. It accumulates all Segment2 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done.
	7	**Reserved** Format: MBZ
	6:0	**Segment2 Qindex**

MFX_VP8_BRC_CUMULATIVE_DQ_INDEX23 - Reported BitRateControl CumulativeDeltaQindex and Qindex 23			
		Format:	U7
		This contains Segment2 Qindex used in current frame. This register is valid after a BRC pass is done.	

Reported BitRateControl DeltaLoopFilter

MFX_VP8_BRC_D_LOOP_FILTER - Reported BitRateControl DeltaLoopFilter

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12914h
ShortName:	MFX_VP8_BRC_D_LOOP_FILTER_VB0
Address:	1C914h
ShortName:	MFX_VP8_BRC_D_LOOP_FILTER_VB1

This register stores per segement Bit Rate Control DeltaLoopFilter.

DWord	Bit	Description
0	31	**Reserved** Format: MBZ
	30:24	**Segment3 DeltaLoopFilter** Format: S6 This contains Segment3 DeltaLoopFilter in Bit Rate Control. This register is valid after a BRC pass is done
	23	**Reserved** Format: MBZ
	22:16	**Segment2 DeltaLoopFilter** Format: S6 This contains Segment2 DeltaLoopFilter in Bit Rate Control. This register is valid after a BRC pass is done
	15	**Reserved** Format: MBZ
	14:8	**Segment1 DeltaLoopFilter**

MFX_VP8_BRC_D_LOOP_FILTER - Reported BitRateControl DeltaLoopFilter

		Format: S6 This contains Segment1 DeltaLoopFilter in Bit Rate Control. This register is valid after a BRC pass is done.
	7	**Reserved** Format: MBZ
	6:0	**Segment0 DeltaLoopFilter** Format: S6 This contains Segment0 DeltaLoopFilter in Bit Rate Control. This register is valid after a BRC pass is done. If Segmentation is not enabled, this field reflects DeltaLoopFilter. If Segmentation is enabled, this field reflects Segment0 DeltaLoopFilter.

Reported BitRateControl DeltaQindex

MFX_VP8_BRC_DQ_INDEX - Reported BitRateControl DeltaQindex

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12910h
ShortName:	MFX_VP8_BRC_DQ_INDEX_VB0
Address:	1C910h
ShortName:	MFX_VP8_BRC_DQ_INDEX_VB1

This register stores per segement Bit Rate Control DeltaQindex.

DWord	Bit	Description
0	31:24	**Segment3 DeltaQindex** Format: S7 This contains Segment3 DeltaQindex in Bit Rate Control. This register is valid after a BRC pass is done
	23:16	**Segment2 DeltaQindex** Format: S7 This contains Segment2 DeltaQindex in Bit Rate Control. This register is valid after a BRC pass is done
	15:8	**Segment1 DeltaQindex** Format: S7 This contains Segment1 DeltaQindex in Bit Rate Control. This register is valid after a BRC pass is done.
	7:0	**Segment0 DeltaQindex** Format: S7 This contains Segment0 DeltaQindex in Bit Rate Control. This register is valid after a BRC pass is

MFX_VP8_BRC_DQ_INDEX - Reported BitRateControl DeltaQindex		
		done. If Segmentation is not enabled, this field reflects DeltaQindex. If Segmentation is enabled, this field reflects Segment0 DeltaQindex.

Reported BitRateControl parameter Mask

MFX_VP8_CNTRL_MASK - Reported BitRateControl parameter Mask

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12900h
ShortName:	MFX_VP8_CNTRL_MASK_VB0
Address:	1C900h
ShortName:	MFX_VP8_CNTRL_MASK_VB1

This register stores the count of bytes of the bitstream output per frame

DWord	Bit	Description
0	31:6	**Reserved** Format: MBZ
	5	**Final Bitstream Buffer Overrun Mask** Format: U1 This is same bit reflected in MFX_VP8_ENC_CFG DW2 bit5. This denotes Final bitstream buffer overrun feature is enabled.
	4	**Intermediate Bitstream Buffer Overrun Mask** Format: U1 This is same bit reflected in MFX_VP8_ENC_CFG DW2 bit4. This denotes intermediate bitstream buffer overrun feature is enabled.
	3	**Intra MB Bit Count Conformance Mask** Format: U1 This is legacy support as AVC for Intra MB Bit Count conformance. This is same bit reflected in MFX_VP8_ENC_CFG DW2 bit3. This feature is not validated.
	2	**Inter MB Bit Count Conformance Mask** Format: U1 This is legacy support as AVC for Inter MB Bit Count conformance. This is same bit reflected in

MFX_VP8_CNTRL_MASK - Reported BitRateControl parameter Mask		
		MFX_VP8_ENC_CFG DW2 bit2. This feature is not validated.
	1	**Frame Bit Rate Overflow Mask** Format: U1 This is same bit reflected in MFX_VP8_ENC_CFG DW2 bit0. It denotes if Frame Bit Rate Overflow is enabled for Bit Rate Control
	0	**Frame Bit Rate Underflow Mask** Format: U1 This is same bit reflected in MFX_VP8_ENC_CFG DW2 bit1. It denotes if Frame Bit Rate Underflow is enabled for Bit Rate Control

Reported BitRateControl parameter Status

MFX_VP8_CNTRL_STATUS - Reported BitRateControl parameter Status

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12904h
ShortName:	MFX_VP8_CNTRL_STATUS_VB0
Address:	1C904h
ShortName:	MFX_VP8_CNTRL_STATUS_VB1

This register stores the count of bytes of the bitstream output per frame

DWord	Bit	Description
0	31:8	**Reserved** Format: MBZ
	7	**QindexClampHigh Status** Format: U1 This denotes if Qindex is clamped by QindexClampHigh value programmed in MFX_VP8_PIC_STATE.DW7.
	6	**QindexClampLow Status** Format: U1 This denotes if Qindex is clamped by QindexClampLow value programmed in MFX_VP8_PIC_STATE.DW7.
	5	**Final Bitstream Buffer Overrun Status** Format: U1 This denotes if Final bitstream buffer overrun.
	4	**Intermediate Bitstream Buffer Overrun Status** Format: U1 This denotes if any of the Intermediate bitstream buffer overrun. (including FrameHeader, Partition1 to Partition8)

MFX_VP8_CNTRL_STATUS - Reported BitRateControl parameter Status

	3	**Intra MB Bit Count Conformance Status** Format: U1 This is legacy support as AVC for Intra MB Bit Count conformance. It denotes if Intra MB Bit Count meets conformance size. This feature is not validated.
	2	**Inter MB Bit Count Conformance Status** Format: U1 This is legacy support as AVC for Inter MB Bit Count conformance. It denotes if Inter MB Bit Count meets conformance size. This feature is not validated.
	1	**Frame Bit Rate Overflow Status** Format: U1 It denotes if Frame Bit Rate Overflow in current frame
	0	**Frame Bit Rate Underflow Status** Format: U1 It denotes if Frame Bit Rate Underflow in current frame

Reported Bitstream Output Bit Count for Syntax Elements Only

HCP_BITSTREAMSE_BITCOUNT_FRAME - Reported Bitstream Output Bit Count for Syntax Elements Only

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1E9A8h

This register stores the count of number of bits in the bitstream due to syntax elements only. This excludes header/ byte alignment /tail/EMU/CABAC-0word/padding bits but includes the stop-one-bit. This register is part of the context save and restore.

DWord	Bit	Description
0	31:0	**HCP Bitstream Syntax Element Only Bit Count** Format: U32 Total number of bits in the bitstream output due to syntax elements only. It includes the data bytes only. This count is updated for every time the internal bitstream counter is incremented and its reset at image start.

Reported Bitstream Output Bit Count for Syntax Elements Only Register

MFC_BITSTREAM_SE_BITCOUNT_FRAME - Reported Bitstream Output Bit Count for Syntax Elements Only Register	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	128A4h

This register stores the count of number of bits in the bitstream due to syntax elements only. This excludes header/ byte alignment /tail/EMU/CABAC-0word/padding bits but includes the stop-one-bit. This register is part of the context save and restore.

DWord	Bit	Description
0	31:0	**MFC Bitstream Syntax Element Only Bit Count** Total number of bits in the bitstream output due to syntax elements only. It includes the data bytes only. This count is updated for every time the internal bitstream counter is incremented and its reset at image start.

Reported Bitstream Output Byte Count per Frame Register

MFC_BITSTREAM_BYTECOUNT_FRAME - Reported Bitstream Output Byte Count per Frame Register	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	128A0h

This register stores the count of bytes of the bitstream output per frame

DWord	Bit	Description
0	31:0	**MFC Bitstream Byte Count per Frame** Total number of bytes in the bitstream output per frame from the encoder. This includes header/tail/byte alignment/data bytes/EMU (emulation) bytes/cabac-zero word insertion/padding insertion. This count is updated for every time the internal bitstream counter is incremented and its reset at image start.

Reported Bitstream Output Byte Count per Tile

HCP_BITSTREAM_BYTECOUNT_TILE - Reported Bitstream Output Byte Count per Tile

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1E9CCh

This register stores the count of bytes of the bitstream output per tile.

DWord	Bit	Description
0	31:0	**HCP Bitstream Byte Count per Tile** Format: U32 Total number of bytes in the bitstream output per Tile from the encoder. This includes header/byte alignment/data bytes/EMU (emulation) bytes/. This count is updated for every time the internal bitstream counter is incremented and its reset at tile start.

Reported Bitstream Output CABAC Bin Count Register

MFC_AVC_CABAC_BIN_COUNT_FRAME - Reported Bitstream Output CABAC Bin Count Register	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	128A8h

This register stores the count of number of bins per frame.

DWord	Bit	Description
0	31:0	**MFC AVC Cabac Bin Count** Total number of BINs in the bitstream output per frame from the encoder. This count is updated for every time the bin counter is incremented and its reset at image start.

Reported Bitstream Output CABAC Insertion Count

HCP_CABAC_INSERTION_COUNT - Reported Bitstream Output CABAC Insertion Count	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1E9B0h

This register stores the count in bytes of **CABAC ZERO_WORD insertion. It is primarily provided for statistical data gathering.**

DWord	Bit	Description
0	31:0	**HCP Cabac Insertion Count** Format: U32 Total number of bytes in the bitstream output before for the CABAC zero word insertion. This count is updated each time when the insertion count is incremented.

Reported Final Bitstream Byte Count

MFX_VP8_FRM_BYTE_CNT - Reported Final Bitstream Byte Count	
Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12908h
Address:	1C908h

This register stores the count of bytes of the bitstream output per frame

DWord	Bit	Description
0	31:0	**Final BitStream Byte Count** Format: U32 This register contains Final Bitstream byte count

Reported Frame Zero Padding Byte Count

MFX_VP8_FRM_ZERO_PAD - Reported Frame Zero Padding Byte Count

Register Space:	MMIO: 0/2/0
Source:	VideoCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1290Ch
ShortName:	MFX_VP8_FRM_ZERO_PAD_VB0
Address:	1C90Ch
ShortName:	MFX_VP8_FRM_ZERO_PAD_VB1

This register stores Frame Zero Padding Byte Count

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**Frame Zero Padding Byte Count** Format: U16 This register contains Frame Zero Padding byte count This is legacy support. This feature is not validated.

Reported Timestamp Count

TIMESTAMP - Reported Timestamp Count	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	64
Address:	02358h-0235Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_RCSUNIT
Address:	18358h-1835Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_POCSUNIT
Address:	22358h-2235Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_BCSUNIT
Address:	1C0358h-1C035Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VCSUNIT0
Address:	1C4358h-1C435Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VCSUNIT1
Address:	1C8358h-1C835Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VECSUNIT0
Address:	1D0358h-1D035Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VCSUNIT2
Address:	1D4358h-1D435Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VCSUNIT3
Address:	1D8358h-1D835Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VECSUNIT1

TIMESTAMP - Reported Timestamp Count

Address:	1E0358h-1E035Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VCSUNIT4

Address:	1E4358h-1E435Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VCSUNIT5

Address:	1E8358h-1E835Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VECSUNIT2

Address:	1F0358h-1F035Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VCSUNIT6

Address:	1F4358h-1F435Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VCSUNIT7

Address:	1F8358h-1F835Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VECSUNIT3

Description	Source
This register provides an elapsed real-time value that can be used as a timestamp for GPU events over short periods of time. Note that the value of this register can be obtained in a 3D pipeline-synchronous fashion without a pipeline flush by using the PIPE_CONTROL command. See 3D Geometry Pipeline in the "3D and Media" volume. This register (effectively) counts at a constant frequency by adjusting the increment amount according to the actual reference clock frequency. SW therefore does not need to know the reference clock frequency.	RenderCS
This register provides an elapsed real-time value that can be used as a timestamp. The accumulated value in this register is of the timestamp stamp granularity (base unit) defined in the “Time Stamp Bases” subsection in Power Management chapter.	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS
This register is *not* reset by a graphics reset. It will maintain its value unless a full chipset reset is performed.	

DWord	Bit	Description
0..1	63:36	**Reserved** Format: MBZ
	35:32	**Timestamp Value UN** Format: U4

TIMESTAMP - Reported Timestamp Count		
		This register increment's for every timestamp base unit. The granularity of the time stamp base unit is defined in the "Time Stamp Bases" subsection in Power Management chapter. Note: This is the Upper Nibble of the Timestamp Value, a 36-bit signal.
	31:0	**Timestamp Value LDW** Format: U32 This register increment's for every timestamp base unit. The granularity of the time stamp base unit is defined in the "Time Stamp Bases" subsection in Power Management chapter.

Reset Control Register

RESET_CTRL - Reset Control Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	020D0h-020D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_RCSUNIT
Address:	180D0h-180D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_POCSUNIT
Address:	220D0h-220D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_BCSUNIT
Address:	1C00D0h-1C00D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_VCSUNIT0
Address:	1C40D0h-1C40D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_VCSUNIT1
Address:	1C80D0h-1C80D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_VECSUNIT0
Address:	1D00D0h-1D00D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_VCSUNIT2
Address:	1D40D0h-1D40D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_VCSUNIT3
Address:	1D80D0h-1D80D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_VECSUNIT1

RESET_CTRL - Reset Control Register

Address:	1E00D0h-1E00D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_VCSUNIT4

Address:	1E40D0h-1E40D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_VCSUNIT5

Address:	1E80D0h-1E80D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_VECSUNIT2

Address:	1F00D0h-1F00D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_VCSUNIT6

Address:	1F40D0h-1F40D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_VCSUNIT7

Address:	1F80D0h-1F80D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_VECSUNIT3

Soft reset flow for an engine (Render, Blitter, Video, Video Enhancement) is asynchronous to the context execution in HW. SW needs a deterministic way to ensure it resets the context it intends to. One way to achieve this is to ensure HW doesn't switch out the context while SW is doing a soft reset. This is achieved by having an explicit interface between HW-SW to prepare the engine prior to the soft reset. SW sets the "Request Reset" in RESET_CTRL register of an engine indicating SW wants to initiate a soft reset flow for the corresponding engine. In response to "Request Reset" bit set, HW sets "Ready for Reset" bit of RESET_CTRL register indicating engine readiness for reset. As part of the reset readiness HW will not allow any context switch to take place and also ensure any ongoing context switch is paused on a clean context boundary (context save in progress is completed, Context Switch Status Buffer updates are allowed to complete).
SW polls for "Ready for Reset" bit to be set before it does soft reset for the corresponding engine. Reading EXECLIST_STATUS register at this point provides the active context in HW that will get reset. On engine reset "Request Reset" bit will get reset with rest of the engine logic.
Upon polling EXECLIST_STATUS register for active context SW might decide not to reset the engine and can reset the "Request Reset" in RESET_CTRL register. On "Request Reset" getting reset by SW, HW must continue with execution.
SW setting "Ready for Reset" bit in RESET_CTRL register of an engine need not be followed by the corresponding engine reset.
SW writing to "Request Reset" bit in RESET_CTRL register is preparing the engine for reset whereas SW writing to GDRST triggers the actual reset flow in HW.

Programming Notes
SW must not do Reset Readiness Handshake as part of the reset recovery on an CAT error.

RESET_CTRL - Reset Control Register

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15:3	**Reserved** Format: MBZ
	2	**Reserved**
	1	**Ready for Reset** Format: U1 When set indicates render engine is ready for reset. This bit gets cleared on engine reset or when Soft Reset In progress is cleared.
	0	**Request Reset** Format: U1 "Request Reset" bit must be read as "Readyness for Reset". When set indicates SW wishes to reset the render engine. On seeing this bit set Command Streamer will take appropriate action and set Ready For Reset status bit. This bit gets cleared on engine reset. This bit can also be cleared by writing "0" to this bit.

Reset Flow Control Messages 0

RSTFCTLMSG0 - Reset Flow Control Messages 0

Register Space: MMIO: 0/2/0

Source: BSpec

Size (in bits): 32

Address: 08108h

Soft-Reset and FLR Flow Control Message Registers

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:3	**Reserved** Access: RO Reserved
	2	**FLR Done ack from Pmunit** Access: R/W Set FLR Done ack from Pmunit: 1: PM unit sets this bit to acknowledge the FLR done message has been forwarded to SA through GAM interface. 0: Default Value. If the bit was set by PM then Cpunit hardware clears it once FLR is completed.
	1	**Global Resource Arbitration Acknowledgement Messages** Access: R/W Global Resource Arbitration Acknowledgement Message from PM: '1' : CP_ARB_REQ_ACK - Acknowledgement for CPunit's global resource arbitration request '0' : CP_ARB_RELEASE_ACK - Acknowledgement to CPunit's release of global resources
	0	**CP Busy / Idle Status Acknowledgement Messages** Access: R/W CP Busy / Idle Status Acknowledgement Message from PM: '0' : CP_NOT_BUSY_ACK - Acknowledgement that the CPunit is idle. '1' : CP_BUSY_ACK - Acknowledgement that the CPunit is busy.

Reset Flow Control Messages 1

RSTFCTLMSG1 - Reset Flow Control Messages 1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	08114h	
Soft-Reset and FLR Flow Control Message Registers		
DWord	**Bit**	**Description**
0	31:16	**Message Mask** Access: RO Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15	**Vebox 3 Reset flow Acknowledge Message** Access: R/W PM Acknowledgement Messages for Vebox reset: '1' : PREP_RST_VEBOX_ACK - Acknowledgement that graphics VE is prepared for reset assertion. '0' : DONE_VEBOX_RST_ACK - Acknowledgement that graphics VE reset is de-asserted
	14	**Vebox 2 Reset flow Acknowledge Message** Access: R/W PM Acknowledgement Messages for Vebox reset: '1' : PREP_RST_VEBOX_ACK - Acknowledgement that graphics VE is prepared for reset assertion. '0' : DONE_VEBOX_RST_ACK - Acknowledgement that graphics VE reset is de-asserted
	13	**Vebox 1 Reset flow Acknowledge Message** Access: R/W PM Acknowledgement Messages for Vebox reset: '1' : PREP_RST_VEBOX_ACK - Acknowledgement that graphics VE is prepared for reset assertion. '0' : DONE_VEBOX_RST_ACK - Acknowledgement that graphics VE reset is de-asserted
	12	**Vebox 0 Reset flow Acknowledge Message**

RSTFCTLMSG1 - Reset Flow Control Messages 1

		Access: R/W PM Acknowledgement Messages for Vebox reset: '1' : PREP_RST_VEBOX_ACK - Acknowledgement that graphics VE is prepared for reset assertion. '0' : DONE_VEBOX_RST_ACK - Acknowledgement that graphics VE reset is de-asserted
	11	**Media 7 Reset Flow Acknowledgement Messages** Access: R/W PM Acknowledgement Messages for Media reset: '1' : PREP_RST_MEDIA_ACK - Acknowledgement that graphics media block is prepared for reset assertion. '0' : DONE_MEDIA_RST_ACK - Acknowledgement that the graphics media reset is de-asserted
	10	**Media 6 Reset Flow Acknowledgement Messages** Access: R/W PM Acknowledgement Messages for Media reset: '1' : PREP_RST_MEDIA_ACK - Acknowledgement that graphics media block is prepared for reset assertion. '0' : DONE_MEDIA_RST_ACK - Acknowledgement that the graphics media reset is de-asserted
	9	**Media 5 Reset Flow Acknowledgement Messages** Access: R/W PM Acknowledgement Messages for Media reset: '1' : PREP_RST_MEDIA_ACK - Acknowledgement that graphics media block is prepared for reset assertion. '0' : DONE_MEDIA_RST_ACK - Acknowledgement that the graphics media reset is de-asserted
	8	**Media 4 Reset Flow Acknowledgement Messages** Access: R/W PM Acknowledgement Messages for Media reset: '1' : PREP_RST_MEDIA_ACK - Acknowledgement that graphics media block is prepared for reset assertion. '0' : DONE_MEDIA_RST_ACK - Acknowledgement that the graphics media reset is de-asserted
	7	**Media 3 Reset Flow Acknowledgement Messages** Access: R/W PM Acknowledgement Messages for Media reset:

RSTFCTLMSG1 - Reset Flow Control Messages 1

		'1' : PREP_RST_MEDIA_ACK - Acknowledgement that graphics media block is prepared for reset assertion. '0' : DONE_MEDIA_RST_ACK - Acknowledgement that the graphics media reset is de-asserted
	6	**Media 2 Reset Flow Acknowledgement Messages** Access: R/W PM Acknowledgement Messages for Media reset: '1' : PREP_RST_MEDIA_ACK - Acknowledgement that graphics media block is prepared for reset assertion. '0' : DONE_MEDIA_RST_ACK - Acknowledgement that the graphics media reset is de-asserted
	5	**Media 1 Reset Flow Acknowledgement Messages** Access: R/W PM Acknowledgement Messages for Media reset: '1' : PREP_RST_MEDIA_ACK - Acknowledgement that graphics media block is prepared for reset assertion. '0' : DONE_MEDIA_RST_ACK - Acknowledgement that the graphics media reset is de-asserted
	4	**Media 0 Reset Flow Acknowledgement Messages** Access: R/W PM Acknowledgement Messages for Media reset: '1' : PREP_RST_MEDIA_ACK - Acknowledgement that graphics media block is prepared for reset assertion. '0' : DONE_MEDIA_RST_ACK - Acknowledgement that the graphics media reset is de-asserted
	3	**Reserved**
	2	**Blitter Reset Flow Acknowledgement Messages** Access: R/W PM Acknowledgement Messages for Blitter reset: '1' : PREP_RST_BLIT_ACK - Acknowledgement that graphics blitter is prepared for reset assertion. '0' : DONE_BLIT_RST_ACK - Acknowledgement that graphics blitter reset is de-asserted
	1	**Render Reset Flow Acknowledgement Messages** Access: R/W PM Acknowledgement Messages for Render reset: '1' : PREP_RST_RENDER_ACK

RSTFCTLMSG1 - Reset Flow Control Messages 1		
		- Acknowledgement that the graphics render block is prepared for reset assertion. '0' : DONE_RENDER_RST_ACK - Acknowledgement that the graphics render reset is de-asserted
	0	**GTI-Device Reset Flow Acknowledgement Messages** Access: R/W PM Acknowledgement Messages for GTI-Device reset: '1' : PREP_RST_GTIDEV_ACK - Acknowledgement that the GTI device is prepared for reset assertion. '0' : DONE_GTIDEV_RST_ACK - Acknowledgement that the GTI device reset is de-asserted

Revision Identification and Class Code register

RID2_CC_0_2_0_PCI - Revision Identification and Class Code register

Register Space:	PCI: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00008h

This register contains the revision number for Device #2 Functions 0 and contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the IGD. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

DWord	Bit	Description
0	31:24	**Base Class Code** Default Value: 00000011b Access: RO Variant This is an 8-bit value that indicates the base class code. When MGGC0[VAMEN] is 0 this code has the value 03h, indicating a Display Controller. When MGGC0[VAMEN] is 1 this code has the value 03h, indicating a Display Controller Device.
	23:16	**Sub-Class Code** Default Value: 00000000b Access: RO Variant When MGGC0[VAMEN] is 0, this value is 00h. When MGGC0[VAMEN] is 1, this value is 80h, indicating other display device.
	15:8	**Programming Interface** Default Value: 00000000b Access: RO When MGGC0[VAMEN] is 0 this value is 00h, indicating a Display Controller. When MGGC0[VAMEN] is 1 this value is 00h, indicating a NOP.
	7:4	**Revision Identification Number MSB** Default Value: 0000b Access: R/W Four MSB of RID
	3:0	**Revision Identification Number**

RID2_CC_0_2_0_PCI - Revision Identification and Class Code register

		Default Value:	0000b
		Access:	R/W
		Four LSB of RID	

RING_BUFFER_HEAD_PREEMPT_REG

RING_BUFFER_HEAD_PREEMPT_REG - RING_BUFFER_HEAD_PREEMPT_REG	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0214Ch-0214Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_RCSUNIT
Address:	1814Ch-1814Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_POCSUNIT
Address:	2214Ch-2214Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_BCSUNIT
Address:	1C014Ch-1C014Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VCSUNIT0
Address:	1C414Ch-1C414Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VCSUNIT1
Address:	1C814Ch-1C814Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VECSUNIT0
Address:	1D014Ch-1D014Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VCSUNIT2
Address:	1D414Ch-1D414Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VCSUNIT3
Address:	1D814Ch-1D814Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG

RING_BUFFER_HEAD_PREEMPT_REG - RING_BUFFER_HEAD_PREEMPT_REG

ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VECSUNIT1
Address:	1E014Ch-1E014Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VCSUNIT4
Address:	1E414Ch-1E414Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VCSUNIT5
Address:	1E814Ch-1E814Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VECSUNIT2
Address:	1F014Ch-1F014Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VCSUNIT6
Address:	1F414Ch-1F414Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VCSUNIT7
Address:	1F814Ch-1F814Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VECSUNIT3

Description

This register contains the Head pointer offset in the ring when the last PREEMPTABLE command was executed and caused the head pointer to move due to the UHPTR register being valid. If the PREEMPTABLE command is executed as part of the batch buffer then the value of the register will be the offset in the ring of the command past the batch buffer start that contained the preemptable command.
This is a global register and context save/restored as part of power context image.

Preemptable Commands	Source
• MI_ARB_CHECK • 3D_PRIMITIVE • GPGPU_WALKER • MEDIA_STATE_FLUSH • PIPE_CONTROL (Only in GPGPU mode of pipeline selection) • MI_ATOMIC (Post Sync Operation set in GPGPU mode of pipeline selection) • MI_SEMAPHORE_SIGNAL (Post Sync Operation set in GPGPU mode of pipeline selection)	RenderCS

RING_BUFFER_HEAD_PREEMPT_REG - RING_BUFFER_HEAD_PREEMPT_REG

Preemptable Commands	Source
MI_ARB_CHECK	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS

Programming Notes

Programming Restriction:
This register should NEVER be programmed by driver. This is for HW internal use only.

DWord	Bit	Description
0	31:21	**Last Wrap Count**
	20:2	**Preempted Head Offset** Format: U19 This field contains the Head pointer offset in the ring when the last MI_ARB_CHECK command was executed and caused the head pointer to move due to the UHPTR register being valid.
	1:0	**Ring/Batch Indicator** Value / Name / Description 0h / Ring / Preemptable command was executed in ring and caused head pointer to be updated. 1h / Batch / Preemptable command was executed in batch and caused head pointer to be updated. 2h / 2nd level batch / Preemptable command was executed in second level batch and caused head pointer to be updated.

Ring Buffer Control

RING_BUFFER_CTL - Ring Buffer Control	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0203Ch-0203Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_RCSUNIT
Address:	1803Ch-1803Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_POCSUNIT
Address:	2203Ch-2203Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_BCSUNIT
Address:	1C003Ch-1C003Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_VCSUNIT0
Address:	1C403Ch-1C403Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_VCSUNIT1
Address:	1C803Ch-1C803Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_VECSUNIT0
Address:	1D003Ch-1D003Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_VCSUNIT2
Address:	1D403Ch-1D403Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_VCSUNIT3
Address:	1D803Ch-1D803Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_VECSUNIT1

RING_BUFFER_CTL - Ring Buffer Control

Address:	1E003Ch-1E003Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_VCSUNIT4

Address:	1E403Ch-1E403Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_VCSUNIT5

Address:	1E803Ch-1E803Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_VECSUNIT2

Address:	1F003Ch-1F003Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_VCSUNIT6

Address:	1F403Ch-1F403Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_VCSUNIT7

Address:	1F803Ch-1F803Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_VECSUNIT3

Description

These registers are used to define and operate the "ring buffer" mechanism which can be used to pass instructions to the command interface. The buffer itself is located in a linear memory region. The ring buffer is defined by a 4 Dword register set that includes starting address, length, head offset, tail offset, and control information. These registers can only be updated through a restore of a context thru execution list submission.

DWord	Bit	Description
0	31:21	**Reserved** Format: MBZ
	20:12	**Buffer Length** Format: U9-1 in 4 KB pages - 1 This field is written by SW to specify the length of the ring buffer in 4 KB Pages.Range = [0 = 1 page = 4 KB, 1FFh = 512 pages = 2 MB]
	11	**RBWait** Indicates that this ring has executed a WAIT_FOR_EVENT instruction and is currently waiting. Software can write a "1" to clear this bit, write of "0" has no effect. When the RB is waiting for an

Value	Name	Description
0		1 page = 4 KB
1FFh		512 pages = 2 MB

event and this bit is cleared, the wait will be terminated and the RB will be returned to arbitration.

10 Semaphore Wait

Description
Indicates that this ring has executed a MI_SEMAPHORE_WAIT instruction and is currently waiting for wait condition to satisfy. Software can write a "1" to clear this bit, write of "0" has no effect.

Programming Notes
Writing a value of '1' will unconditionally cancel the semaphore wait on the next memory comparison. Memory comparison is triggered in signal mode on receiving a semaphore signal and in poll mode on wait timer getting expired.

9 Reserved

Format:	MBZ

8 Reserved

Format:	MBZ

7:3 Reserved

Format:	MBZ

2:1 Automatic Report Head Pointer

Source:	BSpec

Description
This field is written by software to control the automatic reporting (write) of this ring buffer's Head Pointer register (register DWord 1) to the corresponding location within the Hardware Status Page. Automatic reporting can either be disabled or enabled at 4KB, 64KB or 128KB boundaries within the ring buffer.
When **Execlist Enable** bit is set the head pointer will be reported to the head pointer location in the Per-Process Hardware Status Page.

Value	Name	Description
0	MI_AUTOREPORT_OFF	Automatic reporting disabled
1	MI_AUTOREPORT_64KB	Report every 16 pages (64KB)
2	MI_AUTOREPORT_4KB	Report every page (4KB) This mode must not be enabled in Ring Buffer mode of scheduling to minimize the auto reports.
3	MI_AUTO_REPORT_128KB	Report every 32 pages (128KB).

0 Ring Buffer Enable

RING_BUFFER_CTL - Ring Buffer Control

Format:	Enable

This field is used to enable or disable this ring buffer. It can be enabled or disabled regardless of whether there are valid instructions pending. If disabled and the ring head equals ring tail, all state currently loaded in hardware is considered invalid.

Programming Notes	Source
Ring Buffer Mode of Scheduling: SW must follow the below programming notes during SW initialization phase or while enabling render engine's ring buffer for the first time, this would be coming out of boot, standby, hibernate or reset. This flow must be also followed during ring replay when ring buffer is disabled. • SW must set the Force Wakeup bit to prevent GT from entering C6. • SW must dispatch workload (dummy context) to initialize render engine with default state such that any context switches that occur subsequently (Power Save) will save and restore coherent device state. Indirect pointers used in 3D states must point to valid graphics surface existing in memory. PP_DCLV followed by PP_DIR_BASE register should be programmed as part of initialization workload if PPGTT is enabled in GFX_MODE register. • SW must ensure all the register (MMIO) initialization/programming through CPU happens in this block or latter, this ensures the MMIO state is save/restored on subsequent context switches (Power Sequences). • Once the render engine is programmed with valid state and the configuration, Force Wakeup bit should be reset to enable C6 entry.	RenderCS

Ring Buffer Head

RING_BUFFER_HEAD - Ring Buffer Head	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02034h-02037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_RCSUNIT
Address:	18034h-18037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_POCSUNIT
Address:	22034h-22037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_BCSUNIT
Address:	1C0034h-1C0037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VCSUNIT0
Address:	1C4034h-1C4037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VCSUNIT1
Address:	1C8034h-1C8037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VECSUNIT0
Address:	1D0034h-1D0037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VCSUNIT2
Address:	1D4034h-1D4037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VCSUNIT3
Address:	1D8034h-1D8037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VECSUNIT1

RING_BUFFER_HEAD - Ring Buffer Head

Address:	1E0034h-1E0037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VCSUNIT4

Address:	1E4034h-1E4037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VCSUNIT5

Address:	1E8034h-1E8037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VECSUNIT2

Address:	1F0034h-1F0037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VCSUNIT6

Address:	1F4034h-1F4037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VCSUNIT7

Address:	1F8034h-1F8037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VECSUNIT3

Description

These registers are used to define and operate the "ring buffer" mechanism which can be used to pass instructions to the command interface. The buffer itself is located in a linear memory region. The ring buffer is defined by a 4 Dword register set that includes starting address, length, head offset, tail offset, and control information. These registers can only be updated through a restore of a context thru execution list submission.

DWord	Bit	Description
0	31:21	**Wrap Count** Format: U11 count of ring buffer wraps This field is incremented by 1 whenever the **Head Offset** wraps from the end of the buffer back to the start (i.e., whenever it wraps back to 0). Appending this field to the **Head Offset** field effectively creates a virtual 4GB Head "Pointer" which can be used as a tag associated with instructions placed in a ring buffer. The Wrap Count itself will wrap to 0 upon overflow.
	20:2	**Head Offset** Format: GraphicsAddress[20:2] DWord Offset This field indicates the offset of the *next* instruction DWord to be parsed. Software will initialize this field to select the first DWord to be parsed once the RB is enabled. (Writing the Head Offset while the RB is enabled is UNDEFINED). Subsequently, the device will increment this offset as it executes instructions - until it reaches the QWord specified by the **Tail Offset**. At this point the ring buffer is considered "empty".

RING_BUFFER_HEAD - Ring Buffer Head

		Programming Notes A RB can be enabled empty or containing some number of valid instructions.
	1	**Reserved** Format: MBZ
	0	**Reserved** Format: MBZ

Ring Buffer Start

RING_BUFFER_START - Ring Buffer Start	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02038h-0203Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_RCSUNIT
Address:	18038h-1803Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_POCSUNIT
Address:	22038h-2203Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_BCSUNIT
Address:	1C0038h-1C003Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VCSUNIT0
Address:	1C4038h-1C403Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VCSUNIT1
Address:	1C8038h-1C803Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VECSUNIT0
Address:	1D0038h-1D003Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VCSUNIT2
Address:	1D4038h-1D403Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VCSUNIT3
Address:	1D8038h-1D803Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VECSUNIT1

RING_BUFFER_START - Ring Buffer Start

Address:	1E0038h-1E003Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VCSUNIT4

Address:	1E4038h-1E403Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VCSUNIT5

Address:	1E8038h-1E803Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VECSUNIT2

Address:	1F0038h-1F003Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VCSUNIT6

Address:	1F4038h-1F403Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VCSUNIT7

Address:	1F8038h-1F803Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VECSUNIT3

Description

These registers are used to define and operate the "ring buffer" mechanism which can be used to pass instructions to the command interface. The buffer itself is located in a linear memory region. The ring buffer is defined by a 4 Dword register set that includes starting address, length, head offset, tail offset, and control information. These registers can only be updated through a restore of a context thru execution list submission.

DWord	Bit	Description
0	31:12	**Starting Address** Format: GraphicsAddress[31:12] This field specifies Bits 31:12 of the 4KB-aligned starting Graphics Address of the ring buffer. Address bits 31 down to 29 must be zero. All ring buffer pages must map to Main Memory (uncached) pages. Ring Buffer addresses are always translated through the global GTT.
	11:0	**Reserved** Format: MBZ

Ring Buffer Tail

RING_BUFFER_TAIL - Ring Buffer Tail	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02030h-02033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_RCSUNIT
Address:	18030h-18033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_POCSUNIT
Address:	22030h-22033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_BCSUNIT
Address:	1C0030h-1C0033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VCSUNIT0
Address:	1C4030h-1C4033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VCSUNIT1
Address:	1C8030h-1C8033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VECSUNIT0
Address:	1D0030h-1D0033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VCSUNIT2
Address:	1D4030h-1D4033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VCSUNIT3
Address:	1D8030h-1D8033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VECSUNIT1

RING_BUFFER_TAIL - Ring Buffer Tail

Address:	1E0030h-1E0033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VCSUNIT4

Address:	1E4030h-1E4033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VCSUNIT5

Address:	1E8030h-1E8033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VECSUNIT2

Address:	1F0030h-1F0033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VCSUNIT6

Address:	1F4030h-1F4033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VCSUNIT7

Address:	1F8030h-1F8033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VECSUNIT3

Description

These registers are used to define and operate the "ring buffer" mechanism which can be used to pass instructions to the command interface. The buffer itself is located in a linear memory region. The ring buffer is defined by a 4 Dword register set that includes starting address, length, head offset, tail offset, and control information. These registers can only be updated through a restore of a context thru execution list submission.

DWord	Bit	Description
0	31	**POSH Freeze** Source: RenderCS This bit provides a mechanism for SW to freeze POCS execution on context switch boundaries. POCS on sampling tail pointer with POSH Freeze set will not fetch and parse any commands from the command buffer until “POSH Freeze” gets reset on subsequent tail pointer updates. Tail pointer is programmed to PositionCS by RenderCS on a full restore or on a lite restore. **Value** / **Name** / **Description** 0 / **[Default]** / POCS on sampling tail pointer with POSH Freeze set will not fetch and parse any commands from the command buffer until “POSH Freeze” gets reset on subsequent tail pointer updates. 1 / / POCS on sampling tail pointer with POSH Freeze reset will resume regular execution flow.

		Programming Notes "POSH Freeze" bit must be only programmed through RenderCS tail pointer in logical render context area (LRCA). "POSH Freeze" must be set for an context only when it is not active in hardware. "POSH Freeze" can be reset independent of context execution status in hardware. Once reset the updated value will get sampled by POCS only on subsequent context submission to hardware. This bit must not be set for VideoCS, PositionCS, BlitterCS, PinningCS and VideoEnhancementCS.
	30:21	**Reserved** Format: MBZ
	20:3	**Tail Offset** Format: GraphicsAddress[20:3] This field is written by software to specify where the valid instructions placed in the ring buffer end. The value written points to the QWord past the last valid QWord of instructions. In other words, it can be defined as the next QWord that software will write instructions into. Software must write subsequent instructions to QWords following the Tail Offset, possibly wrapping around to the top of the buffer (i.e., software can't skip around within the buffer). Note that all DWords prior to the location indicated by the **Tail Offset** must contain valid instruction data - which may require instruction padding by software. See **Head Offset** for more information.
	2:0	**Reserved** Format: MBZ

RPM Context Image Interface

MSG_RPM_CTXBASE - RPM Context Image Interface

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	08518h

This register is written by RPMunit, the content is provided to msqcunit in rc6 context address decode

DWord	Bit	Description
0	31:30	**Reserved** Access: RO
	29:22	**RC6 Context Base High** Access: R/W This field corresponds to bits [39:32] of RC6MEMBASE Use above 4GB is not currently supported, and these bits must be set to 0
	21:2	**RC6 Context Base Low** Access: R/W This field is used to set the base of memory where the RC6 power context will be saved This value MUST be above the base and below the top of stolen memory
	1	**RC6 DRAM Only** Access: R/W
	0	**RC6 Location** Access: R/W 1'b0 : Send context data to C6SRAM (default) 1'b1 : Send context data to DRAM location specified in RC6CTXBASE

Sampler control register

SAMPLER_CTL - Sampler control register	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	32
Address:	0E140h

DWord	Bit	Description
0	31:16	**ECO Reserved 1** Reserved: MBZ
	15:8	**Reserved**
	7:3	**Sampler unit select** 00000 ? SIUnit 00001 ? PLUnit 00010 ? DGUnit 00011 ? QCUnit 00100 ? FTUnit 00101 ? DMUnit 00110 ? SCUnit 00111 ? FLUnit 01000 ? SOUnit 01001 - AVSunit
	2	**ECO Reserved 2** Reserved MBZ (These bits are moved to CS unit MMIO register section at 0x208c, bit 2)
	1:0	**ECO Reserved 3** Reserved MBZ

Sampler Dummy Register

SMP_DUMMY - Sampler Dummy Register		
Register Space:	MMIO: 0/2/0	
Source:	RenderCS	
Size (in bits):	32	
Address:	0E000h	
Name:	Sampler Dummy Address	
ShortName:	Sampler_Dummy_Address	
This register is defined so that a non-posted MMIO cycle to this destination would ensure all cycles are flushed on the message channel between the source and destination. This register is used in the engine context to ensure all state is delivered. The value programmed in this register must not change the behavior of the GPU.		
DWord	**Bit**	**Description**
0	31:0	**Reserved** Default Value: 0000000000000000b Access: RO

SAMPLER Mode Register

SAMPLER_MODE - SAMPLER Mode Register

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	0E18Ch
Name:	SAMPLER Mode Register
ShortName:	SAMPLER_MODE

This register has bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. To set bit0, for example, the data would be 0x0001_0001. To clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16.

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask[15:0]
	15	**enble smallPL** Format: enable **Programming Notes** This bit MUST be set to ensure optimal power in 3D Sampler. Must not be enabled if **cache_flush** message is sent to sampler.
	14	**ECO Reserved 1B** Format: MBZ
	13:12	**Sampler Cache Set XOR selection** Format: U2 These bits have an impact only when the Sampler cache is configured in 16 way set associative mode. If the cache is being used for immediate data or for blitter data these bits have no effect. Value / Name / Description 00b / None / No XOR.

01b	Scheme 1	New_set_mask[3:0] = Tiled_address[16:13]. New_set[3:0] less than or = New_set_mask[3:0] ^Old_set[3:0]. Rationale: These bits can distinguish among 16 different equivalent classes of virtual pages. These bits also represent the lsb for tile rows ranging from a pitch of 1 tile to 16 tiles.
10b	Scheme 2	New_set_mask[3] = Tiled_address[17] ^ Tiled_address[16]. New_set_mask[2] = Tiled_address[16] ^ Tiled_address[15]. New_set_mask[1] = Tiled_address[15] ^ Tiled_address[14]. New_set_mask[0] = Tiled_address[14] ^ Tiled_address[13]. New_set[3:0] less than or = New_set_mask[3:0] ^ Old_set[3:0]. Rationale: More bits on each XOR can give better statistical uniformity on sets and since two lsbs are taken for each tile row size, it reduces the chance of aliasing on sets.
11b	Scheme 3 **[Default]**	New_set_mask[3] = Tiled_address[22] ^ Tiled_address[21] ^ Tiled_address[20] ^ Tiled_address[19]. New_set_mask[2] = Tiled_address[18] ^ Tiled_address[17] ^ Tiled_address[16]. New_set_mask[1] = Tiled_address[15] ^ Tiled_address[14]. New_set_mask[0] = Tiled_address[13]. New_set[3:0] less than or = New_set_mask[3:0] ^ Old_set[3:0]. Rationale: More bits on each XOR can give better statistical uniformity on sets and since each XOR has different bits, it reduces the chance of aliasing on sets even more.

Programming Notes

This field should be programmed as "00b" corresponding to NO XOR option when 3D map performance fix in MT is enabled using the field "Sampler Set Remapping for 3D Disable" in the SAMPLER Mode Register.

11:10 **ECO Reserved 2b**

Format:	MBZ

9 **Sampler Set Remmapping for 3D Disable**

Value	Name	Description
0h	Enable Set Remap **[Default]**	Set remapping for 3d enabled
1h	Disable Set Remap	Set remapping for 3d disabled

8 **Sampler L2 Disable**

Format:	Disable

Will disable the L2 cache and force all access to be misses

SAMPLER_MODE - SAMPLER Mode Register

7 **ECO Reserved 3**

Format:	MBZ

6 **Compressed Overfill disable**

Format:	disable

5 **Headerless Message for Pre-emptable Contexts**

Format:	Enable

When set to 1h, this bit forces sampler to receive the Binding Table Pointer (BTP) directly from the incoming message rather than from the Header Bypass Ram which is written at thread dispatch. This enables sampler to support headerless messages for pre-emptable GPGPU contexts. When set to 0h, it reverts to the previous behavior where BTP is taken from the Header Bypass RAM for headerless messages and pre-emptable GPGPU contexts must have headers on all sampler messages. This bit is ignored for messages with headers.

Value	Name	Description
0h	**[Default]**	For headerless messages sampler will take Binding Table Pointer (BTP) from the Header Bypass RAM written by the thread dispatch and message headers must be used on all sampler messages for Pre-emptable contexts.
1h		For headerless messages sampler will take Binding Table Pointer (BTP) from the incoming message and sampler may be used for pre-emptable contexts.

4 **Lossless Overfetch Disable**

This bit,controls the amount of data fetched per texel for losslessly compressed surfaces which are non-expandable formats.
An expandable format is a format where the color channels are expanded to a power-of-2 number of bits when fetched from memory.
R8G8B8A8_UNORM is an example of a non-expandable format.
R10G10B10A2_UNORM is an example of an expandable format.

Value	Name	Description
0h	En_ovf_dis	When programmed to 0h, over fetching is enabled for all losslessly compressed surfaces
1h	Dis_ovf_dis **[Default]**	When programming to 1h, overfetch is disabled only for losslessly compressed surfaces which are non- expandable formats. A non-expandable format is a format where the color channels are not expanded to a power-of-2 number of bits when fetched from memory. R8G8B8A8_UNORM is an example of a non-expandable format. R10G10B10A2_UNORM is an example of an expandable format.

Programming Notes

SAMPLER_MODE - SAMPLER Mode Register

		This bit should be programmed to 1h (disabled) by software to ensure optimal performance.
	3	**ECO Reserved 5** Format: MBZ
	2	**ECO Reserved 4-2**
	1	**Overfetch Heuristic Enable** Format: Enable When disabled sampler will perform a heuristic analysis of the spread of pixels within a sampled subspan and disable overfetching for uncompressed lines of a losslessly compressed surface
	0	**Indirect State Base Addr Override** Format: Enable This bit is used to control whether Indirect State (Border Color) to be relative to same base address as SAMPLER_STATE or relative to the DYNAMIC_STATE_BASE_ADDR

SAMPLER READ DATA

SAMPLER_RDATA - SAMPLER READ DATA	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	RO Variant
Size (in bits):	32
Address:	0E144h

DWord	Bit	Description
0	31:0	**Reserved**

SCRATCH1

SCRATCH1 - SCRATCH1

Register Space: MMIO: 0/2/0

Source: BSpec

Size (in bits): 32

Address: 0B11Ch

DWord	Bit	Description
0	31:12	**SCRATCH** Access: R/W
	11	**Snoop SLM Save Restore Fix Disable** Access: R/W 0 (default): Snoop fix during SLM Save Restore is enabled 1 : Snoop fix in LTCD during SLM Save Restore is disabled lbcf_ltcd_snpfix_dis
	10	**SCRATCH_1** Access: R/W This register field is not to be allocated.
	9	**LSQC RORW Performance Fix Disable** Access: R/W 0 (default) : Order cam match should not be qualified with destination for read serialization fix. 1 : Order cam match will be qualified with destination for read serialization fix. lbcf_csr_lsqc_rorwperf_dis
	8	**Eviction Performance Fix Enable** Access: R/W Disable Eviction Performance fix 0 (default) - Enable Eviction Performance Fix in LSQC 1 - Disable Eviction Performance Fix in LSQC lbcf_csr_evict_perf_fix_en
	7	**Prefetch Page Fault Hang Fix Enable**

	Access:	R/W

0 (default) - State/URB prefetch request does not hang for page fault,but no cache fill is done
1 - State/URB prefetch request hangs for page fault.
lbcf_csr_cfg_pf_pgflt_fix_en

6 **Coherent SQCAM Disable**

Access:	R/W

0 (default) - Enable sqcam look up for coh cycles
1 - Disable sqcam look up for coh cycles
lbcf_csr_coh_sqcam_en

5 **SLM/Non-SLM Fair Arbitration Fix Disable**

Access:	R/W

0 (default) - SLM/non-SLM Fair arbitration fix is enabled
1 - SLM/non-SLM Fair arbitration fix is disabled
lbcf_lslm_fairarb_crdt_fix_dis

4 **DC Non coherent pm flush**

Access:	R/W

0:(default) When PM flush is sent to L3, LSQC will generate Query to flush coherent and DC Non coherent Linesfrom L3.
1: When PM flush is sent to L3, LSQC will generate Query to flush only the Coherent Lines (DC/L3 ways) from L3.
lbcf_csr_lsqc_flush_nc_on_pm_flush_dis

3 **ROINV Stall Deassert**

Default Value:	0b
Access:	R/W

0 : When any of the text, const, state or inst ROINV flags are set in LTCD, stall from LTCD (ltcd_ltcc_l3_stall) is not deasserted
1 : Even if any of the text, const, state,or inst ROINV flags are set in LTCD, stall from LTCD (ltcd_ltcc_l3_stall) is deasserted after servicing the current ROINV and before moving on to servicing pending ROINVs
lbcf_ltcd_roinv_stall_deassert
Additional comment: If ROINV's are pending when the current ROINV is in progress, LTCD will service the current ROINV, deassert the stall for one 1x clock and move on to service the pending

		ROINV's. When this bit is set to 1'b0, LTCD will prevent the stall from deasserting between these ROINV's. Instead the stall will be asserted until all the ROINV's complete. This helps in preventing cycles from sneaking into LTCD during the clock where the stall is deasserted
	2	**LBS SLA Retry Timer Decrement** Default Value: 1b Access: R/W 1: LBS SLA Retry Timer Decrement is enabled 0: LBS SLA Retry Timer Decrement is disabled lbcf_lbs_sla_retry_timer_dec_en
	1	**LSQC COH SNOOP COAMA STREAM FIX EN** Default Value: 0b Access: R/W 1: Coherent Snoop Coama Stream related fix is enabled. 0: Fix is disabled lbcf_lsqc_coh_snp_coama_stream_fix_en
	0	**Reserved**

SCRATCH 1 from LPFCunit

SCRATCH_LPFC1 - SCRATCH 1 from LPFCunit		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Access:	R/W	
Size (in bits):	32	
Address:	0B474h	
DWord	**Bit**	**Description**
0	31:0	**SCRATCH bits from LPFCunit** Access: R/W

SCRATCH 2 for LNCFunit

SCRATCH_LNCF2 - SCRATCH 2 for LNCFunit

Register Space: MMIO: 0/2/0

Source: BSpec

Size (in bits): 32

Address: 0B0A0h

DWord	Bit	Description
0	31:23	**Reserved**
	22:21	**SCRATCH 2 Field for LNCFUNIT** Access: R/W
	22:0	**SCRATCH 2 field for LNCFunit** Access: R/W
	20	**PM Flush Done LNI Cross Slice Ingress Traffic Drop Disable** Access: R/W 0h : LNI will NOT drop all cross slice ingress traffic, that follow a PM Flush Request. 1h : LNI will drop all cross slice ingress traffic, that follow a PM Flush Request, assuming the condition to be a soft-reset. **Value** / **Name** 1 / **[Default]** [0,1] / **Programming Notes** This bit has to be programmed to 1h in order to avoid a lock up during soft reset.
	19	**LSN Flush All Trackers Disable** Access: R/W 0h (default) : LSN will flush all trackers. 1h :LSN will flush only Eviction trackers.
	18:3	**SCRATCH 2 field for LNCFunit**

SCRATCH_LNCF2 - SCRATCH 2 for LNCFunit

		Access: R/W
	2	**Colored GSYNC Disable** Access: R/W Format: Disable
	1	**LNI Cross-Slice Tracking Queue Disable** Access: R/W 0 - (default) LNI will only use the fifth tracking queue, allow two tracking queues for cross-slice cycles 1 - LNI will only allocate one tracking queue for cross-slice cycles
	0	**Reserved**

SCRATCH2 Register

SCRATCH2 - SCRATCH2 Register

Register Space: MMIO: 0/2/0

Source: BSpec
Access: R/W
Size (in bits): 32

Address: 0B140h

DWord	Bit	Description
0	31	**Uncacheable Coherent Fix Disable** This bitfield will be used to disable uncacheable coherent fix in LSQC. **Value / Name / Description** 0 / **[Default]** / Uncacheable coherent cycles do not rely on self-snoop to guarantee coherence 1 / / Ucacheable coherent cycles rely on self-snoop to guarantee coherence **Programming Notes** This bitfield cannot be programmed to 0 if COHSQCAMEN of SCRATCH1 register is programmed to 1. If this bitifeld is set to 1, I2MWDIS in L3CHMD must be set to 1. If set to 0, I2MWDIS in L3CHMD may be set to either 0/1.
	30	**Smart-Repeater Bypass Enable** This bitfield will be used to bypass the FIFO structures in the smart-repeater and instead flop incoming requests. **Value / Name / Description** 0 / **[Default]** / Smart-repeater will be used, i.e. the FIFO structures for GP/HP cycles will be used 1 / / FIFO structures will be bypassed and all incoming requests will be flopped
	29	**GAM Deadlock Fix Dis** This bit will be used to disable GAM deadlock DCN fix in L3 bank logic **Value / Name / Description** 0 / **[Default]** / GAM deadlock DCN fix is enabled 1 / / GAM deadlock DCN fix is disabled
	28	**Snoop Self-init Bypass Disable**

This bit-field will disable the performance fix that lets snoop cycles bypass the SLM-self init phase (4KB array initialization). The performance fix forwards snoops to LTCD during SLM self-init.

Value	Name	Description
0	**[Default]**	Enable snoop-selfinit bypass
1		Disable snoop-selfinit bypass

27 **Snoop Init Bypass Disable**

This bit-field will disable the performance fix that lets snoop cycles bypass the data-array init phase following reset and EBB clear. The performance fix forwards snoops to LTCD during data-array initialization following reset and EBB clear.

Value	Name	Description
0	**[Default]**	Enable snoop-init bypass
1		Disable snoop-init bypass

26 **SBFT Physical Override**

This bit-field will enable DFT to control the physical(coherent) attribute of cacheline being loaded into L3 during SBFT loading. This bit-field can be set to 1 only during SBFT loading/testing. DFX will handle making sure these get set properly (ie take care of race conditions between loading and setting the bits, etc) L3 can make the assumption that no cycles will be in-flight when the values are changing. DFX will only change the value when transactions are idle.

Value	Name	Description
0	**[Default]**	Physical Vs. Virtual indication sent by LSQC will be used
1		Coherent lines will be loaded in L3 during SBFT loading. L3 is in SBFT loading/testing phase. Can be set to 1 only during SBFT loading/testing

25 **Enable Voltage Level Check**

Enable voltage level check to determine the valid range of EBB accesses.

Value	Name	Description
0	**[Default]**	Ignore voltage level
1		Honor voltage level to determine range of EBB operations

24 **Disable B2B Reads Only**

Used to disable B2B reads to the EBB's.

Value	Name	Description
0	**[Default]**	B2B reads to the EBB's are enabled

SCRATCH2 - SCRATCH2 Register

	1		B2B reads to the EBB's are disabled

23 Disable B2B Writes Only

Used to disable B2B writes to the EBB's.

Value	Name	Description
0	**[Default]**	B2B writes to the EBB's are enabled
1		B2B writes to the EBB's are disabled

22 Disable B2B Read-Writes or Write-Reads Only

Used to disable B2B read-writes and write-reads to the EBB's.

Value	Name	Description
0	**[Default]**	B2B read-writes and write-reads to the EBB's are enabled
1		B2B read-writes and write-reads to the EBB's are disabled

21 Non-Coherent Completion Generation Control

Controls whether LNI or LSQC will generate completions for non-coherent cycles.

Value	Name	Description
0	**[Default]**	LNI will generate completions.
1		LSQC will generate completions.

Programming Notes
Programming this bit also requires setting the corresponding NCCG bitfield in register LNICHKNREG3 in LNCF to the same value.

20 Last Read Fix Disable

Access:	R/W

Value	Name	Description
0	default **[Default]**	Disables the last read fix

19 Coherent Partial Write Merge Enable

Default Value:	1
Access:	R/W

Workaround
Due to issue involving snoops + partial write merging, this bit should be set to 0 for all ICL products with coherency support.

SCRATCH2 - SCRATCH2 Register

	18:15	**SCRATCH18**
	14:10	**LTCD EBB Conflict URB-Read Aging count**
		This bit-field is no longer used as an aging counter since hardware consuming this field doesn't exist anymore. Instead it will be used to improve visibility in LTCC and LTCD.
		Value / **Name** 31 / **[Default]** [0,31] /
	9	**LTCD EBB Conflict URB-Read Aging enable**
		This bit-field is no longer used as an aging counter enable since hardware consuming this field doesn't exist anymore. Retaining bitfield definition for future use.
		Value / **Name** 1 / **[Default]** 0 /
	8:4	**LTCD EBB Conflict L3-Read Aging count**
		This bit-field will determine the number of EBB conflicts experienced by the L3-read in order to age in the L3 FIFO.
		Value / **Name** 10 / **[Default]** [1,31] /
	3	**LTCD EBB Conflict L3-Read Aging enable**
		This bit-field will enable L3-Read aging in LTCD dataunit due to EBB conflicts. During EBB conflicts, L3-fill will be preferred over L3-reads, and this aggressive fill selection can hold up the reads in L3 FIFO depending on the duration of EBB conflicts. L3-read aging will ensure fairness to an L3-read cycle that has been held back due to EBB conflicts by making the L3-fills ineligible once the read has aged.
		Value / **Name** / **Description** 1 / **[Default]** / LTCD EBB conflict L3-Read aging is enabled 0 / / LTCD EBB conflict L3-Read aging is disabled
	2	**LTCD URB FIFO OOO Disable**
		This bit-field will disable URB FIFO OOO implementation in LTCD-dataunit and revert to an implementation where only one URB FIFO was used.
		Value / **Name** / **Description**

SCRATCH2 - SCRATCH2 Register

		0	**[Default]**	LTCD URB FIFO OOO implementation is enabled
		1		LTCD URB FIFO OOO implementation is disabled
	1	**LTCD L3 FIFO OOO Disable**		
		This bit-field will disable L3 FIFO OOO implementation in LTCD-dataunit and revert to an implementation where only one L3 FIFO was used.		
		Value	**Name**	**Description**
		0	**[Default]**	LTCD L3 FIFO OOO implementation is enabled
		1		LTCD L3 FIFO OOO implementation is disabled
	0	**Block L3 Config**		
		Value	**Name**	**Description**
		0	**[Default]**	Enables LBI to send an indication to LTCD which will ignore L3 config reprogramming during a workload

SCRATCH 3 for LNCFunit

SCRATCH_LNCF3 - SCRATCH 3 for LNCFunit		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	0B0A8h	
DWord	**Bit**	**Description**
0	31:0	**SCRATCH 3 field for LNCFunit** Access: R/W Bit[0] : LSN VR MARK Performance fix Disable. 0 : (Default) Performance fix is enabled. 1 : Disables performance fix.

SCRATCH3 Register

SCRATCH3 - SCRATCH3 Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0B154h

DWord	Bit	Description
0	31:11	**SPARE FIELDS**
	10:8	**LTCD TAG ROINV FSM WAIT TIME** Used to derive the number of clocks for which the ROINV FSM will wait, in a “WAIT” state, prior to invalidating the state arrays. Valid values start from 4 to account for time it takes ltcc to receive roinv in progress and stall its pipeline towards LTCD-TAGUNIT, to ensure that any functional cycles that sneaks in TAG for those clocks are serviced gracefully. Value: 4 — default **[Default]** Value: [4,7] — range
	7:4	**LTCD DATA INIT FSM WAIT TIME** Used to derive the number of 2x clocks for which the DATA-INIT FSM will wait, in a “WAIT” state, prior to initializing the data arrays. Final-wait time = 2**this-reg-fields-value. Value: 4 — default **[Default]** Value: [0,15] — range
	3	**OOO IDI response and Data response handling fix disable** Disables the out-of-order handling of IDI response and Data response in LSQC. Value: 1 — Name: — Description: Fix is disabled Value: 0 — Name: **[Default]** — Description: Fix is enabled
	2	**LSQD FIFO-0 Read to LNE Port1 Fix Disable** This register field determines whether LSQD FIFO-0 reads will go on lne port1 if lneport0 doesn't have credits.

SCRATCH3 - SCRATCH3 Register

Value	Name	Description
1		LSQD FIFO-0 reads will not go on lne port1 if lneport0 doesn't have credits
0	**[Default]**	LSQD FIFO-0 reads will go on lne port1 if lneport0 doesn't have credits

1 **Memory Read Return Port1 Stall Fix Disable**

This register field determines stalling behavior of LTCD/LSQD when memory read returns on port1 conflict with data-response from LTCD.

Value	Name	Description
1		LTCD stalls DRSP on phase0 and phase1 when memory read return happens on port1
0	**[Default]**	LTCD stalls DRSP on phase1 when memory read return happens on port1

Programming Notes
This register field cannot be programmed to 0 if PARWRFIXDIS bitfield in register SCRATCH3 in LBCF is programmed to 1.

0 **Early recycle on eviction response**

When enabled forces the broadcast of early recycle event when the tag response is an eviction even if early recycling is disable via the early recycle bit.

Value	Name	Description
1	**[Default]**	Forces the broadcast of early recycle event when the tag response is an eviction
0		Early recycle broadcast is based on the early recycle bit and the snoop pending status

SCRATCH for LNCFunit

SCRATCH_LNCF1 - SCRATCH for LNCFunit

Register Space: MMIO: 0/2/0

Source: BSpec

Size (in bits): 32

Address: 0B008h

DWord	Bit	Description
0	31:29	**Reserved**
	28	**LNI First Arbiter Stack Arbitration Enable** Default Value: 0 0 - Disable LNI First Arbiter Stack based arbitration between Local and Cross Bank Transactions 1 -EnableLNI First Arbiter Stack based arbitration between Local and Cross Bank Transactions lncf_csr_ing_stk_pri_arb_en
	27	**LNI VC1 Flush Done Check Enable** Default Value: 0 0 - LNI does not wait for LSN VC1 Flush done while forwarding flush requests to Bank. 1 - LNI waits for LSN VC1 Flush done before forwarding flush requests to Bank. lncf_csr_lni_vc1_flush_done_check_en lncf_csr_lsn_vc1_flush_done_check_en This register field should not be changed from the default value.
	26:23	**LNE Read Return Aging Count** Default Value: 0110b 0 - LNE Read Return Aging is disabled Non-Zero Value - Count signifies Aging Count of LNE-client Read ReturnTransactions lncf_csr_lnerdrtn_count
	22:20	**LNI FSTARB C CLIENTS AGING COUNT** Default Value: 010b Number of Grants in FST Arbiter for C clients before proceeding to the next priority pool. 0,1 - 1 Grant.

SCRATCH_LNCF1 - SCRATCH for LNCFunit

		2 - 2 Grants. 3- 3 Grants.< /p> 4 - Grants. ... 7 - 7 Grants. lncf_csr_lni_c_cnt
	19:17	**LNI FSTARB Z CLIENTS AGING COUNT** Default Value: 010b Number of Grants in FST Arbiter for Z clients before proceeding to the next priority pool. 0,1- 1Grant. 2 - 2 Grants. 3- 3 Grants. 4 - Grants. ... 7 - 7 Grants. lncf_csr_lni_z_cnt
	16:14	**LNI FSTARB POOL1 AGING COUNT** Default Value: 100b Number of Grants in FST Arbiter for Pool1 clients (DSS/HDC) before proceeding to the next priority pool. 0,1,2- 2 Grants 3- 3 Grants. 4 - Grants. ... 7 - 7 Grants. lncf_csr_lni_hs_cnt
	13	**LNI FSTARB C/Z Fixed Priority Enable** 0 - Z Transactionshavehigher priority than C Transactions. Z PRIORITY > C PRIORITY 1 - C and Z Transaction have equal priority.C PRIORITY = Z PRIORITY This bit is valid only when SCRATCH_LNCF1[LNIFXARBPRIEN] = 1. lncf_csr_lni_Z_C_pri_enable
	12	**LNI FSTARB Fixed Priority Enable** 0 - Disable FSTARB Fixed Priority Arbitration (PRI0 > PRI1 = PRI2 = PRI3) 1 - Enable FSTARB Fixed Priority Arbitration (PRI0 > PRI1 > PRI2 >= PRI3) lncf_csr_lni_pri_arb_enable

SCRATCH_LNCF1 - SCRATCH for LNCFunit

	11:8	**LNE GAPL3 Aging Count** Default Value: 0011b 0 - GAPL3 Aging is disabled Non-Zero Value - Count signifies Aging Count of GAPL3 Transactions lncf_csr_gapl3_count
	7:0	**Reserved**

Second Level Batch Buffer Head Pointer Preemption Register

SBB_PREEMPT_ADDR - Second Level Batch Buffer Head Pointer Preemption Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	0213Ch-0213Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_RCSUNIT
Address:	1813Ch-1813Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_POCSUNIT
Address:	2213Ch-2213Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_BCSUNIT
Address:	1C013Ch-1C013Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VCSUNIT0
Address:	1C413Ch-1C413Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VCSUNIT1
Address:	1C813Ch-1C813Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VECSUNIT0
Address:	1D013Ch-1D013Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register

SBB_PREEMPT_ADDR - Second Level Batch Buffer Head Pointer Preemption Register

ShortName:	SBB_PREEMPT_ADDR_VCSUNIT2

Address:	1D413Ch-1D413Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VCSUNIT3

Address:	1D813Ch-1D813Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VECSUNIT1

Address:	1E013Ch-1E013Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VCSUNIT4

Address:	1E413Ch-1E413Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VCSUNIT5

Address:	1E813Ch-1E813Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VECSUNIT2

Address:	1F013Ch-1F013Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VCSUNIT6

Address:	1F413Ch-1F413Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VCSUNIT7

Address:	1F813Ch-1F813Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VECSUNIT3

SBB_PREEMPT_ADDR - Second Level Batch Buffer Head Pointer Preemption Register

Description
This register gets updated with the DWord-aligned graphics memory address of the PREEMPTABLE command in the second level batch buffer on which preemption has occurred. This register value should be looked at only when the preemption has occurred in the second level batch buffer. This is indicated by "Ring/Batch Indicator" in "RING_BUFFER_HEAD_PREEMPT_REG". This register value retains its previous value and doesn't change when the preemption occurs on a preemptable command in ring buffer or in batch buffer. Preemption is triggered by valid UHPTR in ring buffer mode of scheduling and by a pending execlist in Exec-List mode of scheduling. This is a global register and context save/restored as part of power context image.
Refer to **Preemption > ExecList Scheduling** for a list of preemptible commands.

Programming Notes
Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description
0	31:2	**Second Level Batch Buffer Head Pointer** Format: GraphicsAddress[31:2] This field specifies the DWord-aligned Graphics Memory Address of the PREEMPTABLE command in a batch buffer where the Preemption has occurred.
	1:0	**Reserved** Format: MBZ

Second Level Batch Buffer Head Pointer Register

SBB_ADDR - Second Level Batch Buffer Head Pointer Register	
Register Space:	MMIO: 0/2/0
Source:	CommandStreamer
Access:	RO
Size (in bits):	32
Address:	02114h-02117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_RCSUNIT
Address:	18114h-18117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_POCSUNIT
Address:	22114h-22117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_BCSUNIT
Address:	1C0114h-1C0117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VCSUNIT0
Address:	1C4114h-1C4117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VCSUNIT1
Address:	1C8114h-1C8117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VECSUNIT0
Address:	1D0114h-1D0117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VCSUNIT2

SBB_ADDR - Second Level Batch Buffer Head Pointer Register

Address:	1D4114h-1D4117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VCSUNIT3

Address:	1D8114h-1D8117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VECSUNIT1

Address:	1E0114h-1E0117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VCSUNIT4

Address:	1E4114h-1E4117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VCSUNIT5

Address:	1E8114h-1E8117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VECSUNIT2

Address:	1F0114h-1F0117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VCSUNIT6

Address:	1F4114h-1F4117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VCSUNIT7

Address:	1F8114h-1F8117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VECSUNIT3

This register contains the current DWord Graphics Memory Address of the last-initiated batch buffer.

Programming Notes

This register should NEVER be programmed by driver, this is for HW internal use only. This register should not

SBB_ADDR - Second Level Batch Buffer Head Pointer Register

be written by software. These fields should only get written by a context restore. Software should always set these fields via the MI_BATCH_BUFFER_START command when initiating a batch buffer. This register is saved and restored with context.

DWord	Bit	Description
0	31:2	**Second Level Batch Buffer Head Pointer** Format: GraphicsAddress[31:2] This field specifies the DWord-aligned Graphics Memory Address where the last initiated Second Level Batch Buffer is currently fetching commands. This field is meaningful only when Valid field is set to "1".
	1	**Reserved** Format: MBZ
	0	**Valid** Format: U1 Value / Name / Description 0h / Invalid **[Default]** / Second Level Batch buffer Invalid 1h / Valid / Second Batch buffer Valid.

Second Level Batch Buffer State Register

SBB_STATE - Second Level Batch Buffer State Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02118h-0211Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_RCSUNIT
Address:	18118h-1811Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_POCSUNIT
Address:	22118h-2211Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_BCSUNIT
Address:	1C0118h-1C011Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VCSUNIT0
Address:	1C4118h-1C411Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VCSUNIT1
Address:	1C8118h-1C811Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VECSUNIT0
Address:	1D0118h-1D011Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VCSUNIT2

SBB_STATE - Second Level Batch Buffer State Register

Address:	1D4118h-1D411Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VCSUNIT3

Address:	1D8118h-1D811Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VECSUNIT1

Address:	1E0118h-1E011Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VCSUNIT4

Address:	1E4118h-1E411Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VCSUNIT5

Address:	1E8118h-1E811Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VECSUNIT2

Address:	1F0118h-1F011Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VCSUNIT6

Address:	1F4118h-1F411Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VCSUNIT7

Address:	1F8118h-1F811Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VECSUNIT3

This register contains the attributes of the second level batch buffer initiated from the batch Buffer.

SBB_STATE - Second Level Batch Buffer State Register

This register should not be written by software. These fields should only get written by a context restore. Software should always set these fields via the MI_BATCH_BUFFER_START command when initiating a batch buffer. This register is saved and restored with context.

DWord	Bit	Description
0	31:10	**Reserved** Format: MBZ
	9	**POSH Start** Exists If: //RCS, POCS This bit reflects the POSH Start value programmed by the active first level MI_BATCH_BUFFER_START command.
	8	**POSH Enable** Exists If: //RCS, POCS This bit reflects the POSH Enable value programmed by the active first level MI_BATCH_BUFFER_START command.
	7	**Reserved** Format: MBZ
	6	**Reserved** Format: MBZ
	5	**Address Space Indicator** Note: This field reflects the effective address space indicator security level and may not be the same as the Address Space Indicator written using MI_BATCH_BUFFER_START. 0h – GGTT **[Default]** – This second level batch buffer is located in GGTT memory and is privileged 1h – PPGTT – This second level batch buffer is located in PPGTT memory and is non-privileged.
	4	**Reserved** Source: RenderCS, BlitterCS Format: MBZ
	4	**Reserved**
	3:0	**Reserved** Format: MBZ

Second Level Batch Buffer Upper Head Pointer Preemption Register

SBB_PREEMPT_ADDR_UDW - Second Level Batch Buffer Upper Head Pointer Preemption Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02138h-0213Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_RCSUNIT
Address:	18138h-1813Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_POCSUNIT
Address:	22138h-2213Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_BCSUNIT
Address:	1C0138h-1C013Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VCSUNIT0
Address:	1C4138h-1C413Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VCSUNIT1
Address:	1C8138h-1C813Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VECSUNIT0
Address:	1D0138h-1D013Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VCSUNIT2

SBB_PREEMPT_ADDR_UDW - Second Level Batch Buffer Upper Head Pointer Preemption Register

Address:	1D4138h-1D413Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VCSUNIT3
Address:	1D8138h-1D813Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VECSUNIT1
Address:	1E0138h-1E013Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VCSUNIT4
Address:	1E4138h-1E413Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VCSUNIT5
Address:	1E8138h-1E813Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VECSUNIT2
Address:	1F0138h-1F013Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VCSUNIT6
Address:	1F4138h-1F413Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VCSUNIT7
Address:	1F8138h-1F813Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VECSUNIT3

Upper 32 bits of the 4GB aligned base address within the host's 64-bit virtual address space of the last

SBB_PREEMPT_ADDR_UDW - Second Level Batch Buffer Upper Head Pointer Preemption Register

preempted second level batch buffer. This register follows the same rules as the SBB_PREEMPT_ADDR register.

Programming Notes

Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**Second Level Batch Buffer Head Pointer Upper DWORD** Format: GraphicsAddress[47:32]

Second Level Batch Buffer Upper Head Pointer Register

SBB_ADDR_UDW - Second Level Batch Buffer Upper Head Pointer Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	0211Ch-0211Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_RCSUNIT
Address:	1811Ch-1811Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_POCSUNIT
Address:	2211Ch-2211Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_BCSUNIT
Address:	1C011Ch-1C011Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VCSUNIT0
Address:	1C411Ch-1C411Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VCSUNIT1
Address:	1C811Ch-1C811Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VECSUNIT0
Address:	1D011Ch-1D011Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VCSUNIT2

SBB_ADDR_UDW - Second Level Batch Buffer Upper Head Pointer Register

Address:	1D411Ch-1D411Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VCSUNIT3
Address:	1D811Ch-1D811Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VECSUNIT1
Address:	1E011Ch-1E011Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VCSUNIT4
Address:	1E411Ch-1E411Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VCSUNIT5
Address:	1E811Ch-1E811Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VECSUNIT2
Address:	1F011Ch-1F011Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VCSUNIT6
Address:	1F411Ch-1F411Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VCSUNIT7
Address:	1F811Ch-1F811Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VECSUNIT3

Upper 32 bits of the 4GB aligned base address within the host's 64-bit virtual address space, where the last

SBB_ADDR_UDW - Second Level Batch Buffer Upper Head Pointer Register

initiated Batch Buffer is currently fetching commands. If no batch buffer is currently active, the Valid bit in BB_ADDR will be 0 and this field is meaningless.

Programming Notes
This register should NEVER be programmed by driver. This is for HW internal use only.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**Batch Buffer Head Pointer Upper DWORD** Format: GraphicsAddress[47:32]

Semaphore Polling Interval on Wait

SEMA_WAIT_POLL - Semaphore Polling Interval on Wait	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0224Ch-0224Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_RCSUNIT
Address:	1824Ch-1824Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_POCSUNIT
Address:	2224Ch-2224Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_BCSUNIT
Address:	1C024Ch-1C024Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VCSUNIT0
Address:	1C424Ch-1C424Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VCSUNIT1
Address:	1C824Ch-1C824Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VECSUNIT0
Address:	1D024Ch-1D024Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VCSUNIT2
Address:	1D424Ch-1D424Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VCSUNIT3
Address:	1D824Ch-1D824Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VECSUNIT1

SEMA_WAIT_POLL - Semaphore Polling Interval on Wait

Address:	1E024Ch-1E024Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VCSUNIT4

Address:	1E424Ch-1E424Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VCSUNIT5

Address:	1E824Ch-1E824Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VECSUNIT2

Address:	1F024Ch-1F024Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VCSUNIT6

Address:	1F424Ch-1F424Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VCSUNIT7

Address:	1F824Ch-1F824Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VECSUNIT3

The SEMA_WAIT_POLL register contains Poll Interval field which specifies the minimum number of microseconds allowed for command streamer to wait before re-fetching the data from the address mentioned in the MI_SEMAPHORE_WAIT command on WAIT Mode set to POLL until the condition is satisfied while the context is not switched out. When a value of 0 is written the poll interval will be equal to the memory latency of the read completion.

DWord	Bit	Description
0	31:21	**Reserved** Format: MBZ
	20:0	**Poll Interval** Minimum number of micro-seconds allowed

SF Context Save Register 0

SF_CTXSAVE_REG0 - SF Context Save Register 0	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00DD0h
Name:	SF Context Save Register 0
ShortName:	SF_CTXSAVE_REG0

This register stores the context from SF corresponding to B04h
The data in this register comes on the Non-Posted Read data bus of Msg Chnl and captured on a set indication from Context Save Restore block

DWord	Bit	Description
0	31:0	**SF Context Save Register 0 Content** Access: R/W

SF Context Save Register 1

SF_CTXSAVE_REG1 - SF Context Save Register 1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00DD4h
Name:	SF Context Save Register 1
ShortName:	SF_CTXSAVE_REG1

This register stores the context from SF corresponding to B10h
The data in this register comes on the Non-Posted Read data bus of Msg Chnl and captured on a set indication from Context Save Restore block

DWord	Bit	Description	
0	31:0	**SF Context Save Register 1 Content**	
		Default Value:	0000000000000000b
		Access:	R/W

SF Context Save Register 2

SF_CTXSAVE_REG2 - SF Context Save Register 2	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00DD8h
Name:	SF Context Save Register 2
ShortName:	SF_CTXSAVE_REG2

This register stores the context from SF corresponding to B14h
The data in this register comes on the Non-Posted Read data bus of Msg Chnl and captured on a set indication from Context Save Restore block

DWord	Bit	Description
0	31:0	**SF Context Save Register 2 Content** Access: R/W

SF Context Save Register 3

SF_CTXSAVE_REG3 - SF Context Save Register 3	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00DDCh
Name:	SF Context Save Register 3
ShortName:	SF_CTXSAVE_REG3

This register stores the context from SF corresponding to B18h
The data in this register comes on the Non-Posted Read data bus of Msg Chnl and captured on a set indication from Context Save Restore block

DWord	Bit	Description
0	31:0	**SF Context Save Register 3 Content** Access: R/W

SF Context Save Register 4

SF_CTXSAVE_REG4 - SF Context Save Register 4	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00DE0h
Name:	SF Context Save Register 4
ShortName:	SF_CTXSAVE_REG4

This register stores the context from SF corresponding to B1Ch
The data in this register comes on the Non-Posted Read data bus of Msg Chnl and captured on a set indication from Context Save Restore block

DWord	Bit	Description
0	31:0	**SF Context Save Register 4 Content** Access: R/W

SF Context Save Register 5

SF_CTXSAVE_REG5 - SF Context Save Register 5	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00DE4h
Name:	SF Context Save Register 5
ShortName:	SF_CTXSAVE_REG5

This register stores the context from SF corresponding to B20h
The data in this register comes on the Non-Posted Read data bus of Msg Chnl and captured on a set indication from Context Save Restore block

DWord	Bit	Description
0	31:0	**SF Context Save Register 5 Content** Access: R/W

SF Context Save Register 6

SF_CTXSAVE_REG6 - SF Context Save Register 6	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00DE8h
Name:	SF Context Save Register 6
ShortName:	SF_CTXSAVE_REG6

This register stores the context from SF corresponding to B24h
The data in this register comes on the Non-Posted Read data bus of Msg Chnl and captured on a set indication from Context Save Restore block

DWord	Bit	Description
0	31:0	**SF Context Save Register 6 Content** Access: R/W

SF Context Save Register 7

SF_CTXSAVE_REG7 - SF Context Save Register 7	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00DECh
Name:	SF Context Save Register 7
ShortName:	SF_CTXSAVE_REG7

This register stores the context from SF corresponding to B28h
The data in this register comes on the Non-Posted Read data bus of Msg Chnl and captured on a set indication from Context Save Restore block

DWord	Bit	Description
0	31:0	**SF Context Save Register 7 Content** Access: R/W

SF Context Save Register 8

SF_CTXSAVE_REG8 - SF Context Save Register 8	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	00DF0h
Name:	SF Context Save Register 8
ShortName:	SF_CTXSAVE_REG8

This register stores the context from SF corresponding to B2Ch
The data in this register comes on the Non-Posted Read data bus of Msg Chnl and captured on a set indication from Context Save Restore block

DWord	Bit	Description
0	31:0	**SF Context Save Register 8 Content** Access: R/W

Slice 0 BONUS1 Reg

SL0SPCBONUS1 - Slice 0 BONUS1 Reg		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	24194h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:8	**Reserved** Access: RO Reserved
	7	**BONUS1 BIT 7** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS1 BIT 6** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS1 BIT 5** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS1 BIT 4** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	3	**BONUS1 BIT 3** Access: R/W

SL0SPCBONUS1 - Slice 0 BONUS1 Reg

		SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS1 BIT 2** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS1 BIT 1** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS1 BIT 0** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

Slice 0 BONUS2 Reg

SL0SPCBONUS2 - Slice 0 BONUS2 Reg

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	24198h
Clock Gating Messages Register	

DWord	Bit	Description
0	31:8	**Reserved** Access: RO Reserved
	7	**BONUS2 BIT 7** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS2 BIT 6** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS2 BIT 5** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS2 BIT 4** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	3	**BONUS2 BIT 3** Access: R/W

SL0SPCBONUS2 - Slice 0 BONUS2 Reg

		SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS2 BIT 2** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS2 BIT 1** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS2 BIT 0** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

Slice 0 PGFET control register with lock

SL0SPCPFETCTL - Slice 0 PGFET control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	24188h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock 0 = Bits of Slice 0 PGFETCTL register are R/W 1 = All bits of Slice 0 PGFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:24	**Reserved** Access: RO Reserved
	23	**Power Well Status** Access: RO 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	22	**Powergood timer error** Access: RO 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	21:19	**Delay from enabling secondary PFETs to power good.** Default Value: 111b Access: R/W Lock Delay from enabling secondary PFETs to power good

SL0SPCPFETCTL - Slice 0 PGFET control register with lock

		3'b000: 40ns 3'b001: 80ns 3'b010: 160ns 3'b011: 240ns 3'b100: 320ns 3'b101: 480ns 3'b110: 640ns 3'b111: 1280ns
	18:16	**Strobe pulse period** Access: R/W Lock Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk) **Value** / **Name** 011b / **[Default]**
	15:0	**PFET Ladder Step Sequence** Access: R/W Lock PFET Ladder STEP sequence The PFET ladder has 16 steps, each represented by its corresponding bit in pfetlddrstepseq[15:0]. If the bit location is set, it means we must step on that ladder stage before we go to the next stage. The SPC controller will step through all the steps with asserted bits periodically with period equal to strbpulsprd[2:0] Programming Rule: pfetldrstepseq[15] and pfetldrstepseq[0] must be '1; A '0 setting for these bits is illegal. 15'FFFFh: Ladder step (ladder_sel) goes 0, 1, 2, ?.15. 15'FFF1h: Ladder step goes 0, 4, 5, 6,?15; Steps 1, 2, 3 are skipped. 15'D555h: Ladder step goes 0, 2, 4, 6, 8, 10, 12, 14, 15; Steps 1, 3, 5, 7, 9, 11, 13 are skipped. 15'80001h: Ladder step goes 0, 15; Steps 1, 2, 3, 4, ?14 are skipped. **Value** / **Name** 1111111111111111b / **[Default]**

Slice 0 Power Context Save request

SL0PGCTXREQ - Slice 0 Power Context Save request		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	24184h	
DWord	**Bit**	**Description**
0	31:16	**Message Mask** Access: RO Message Mask bots for lower 16 bits
	15:10	**Reserved** Access: RO Reserved
	9	**Power context save request** Access: R/W Set Power Context Save Request 1'b0 : Power context save is not being requested 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

Slice 0 Power Down FSM control register with lock

SL0SPCPOWERDNFSMCTL - Slice 0 Power Down FSM control register with lock

Register Space: MMIO: 0/2/0

Source: BSpec

Size (in bits): 32

Address: 24190h

DWord	Bit	Description
0	31	**power down control Lock** Access: R/W Lock 0 = Bits of Slice 0 POWERDNFSMCTL register are R/W 1 = All bits of Slice 0 POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:13	**Reserved** Access: RO Reserved
	12	**Leave firewall disabled** Access: R/W Lock When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e dont firewall the gated domain, but complete logical flow
	11	**Leave reset de-asserted** Access: R/W Lock When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e dont assert reset, but complete logical flow
	10	**Leave CLKs ON** Access: R/W Lock

SL0SPCPOWERDNFSMCTL - Slice 0 Power Down FSM control register with lock

		When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e dont clock gate, but complete logical flow
	9	**Leave FET On** Access: R/W Lock When This bit is set SPC will not turn off the PFET eventhough it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e dont power off pfet, but complete logical flow
	8:6	**Power Down state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Gate Clocks
	5:3	**Power Down state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default :Firewall ON
	2:0	**Power Down state 1** Default Value: 000b

SL0SPCPOWERDNFSMCTL - Slice 0 Power Down FSM control register with lock

		Access: R/W Lock This will be the 1st state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Assert Reset

Slice 0 Power Gate Control Request

SL0PGCTLREQ - Slice 0 Power Gate Control Request

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	24180h

Clock Gating Messages Register

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:2	**Reserved** Access: RO Reserved
	1	**CLK RST FWE Request** Access: R/W SLICE 0 CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**Power Gate Request** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

Slice 0 Power on FSM control register with lock

SL0SPCPOWERUPFSMCTL - Slice 0 Power on FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	2418Ch

DWord	Bit	Description
0	31	**power up control Lock** Access: R/W Lock 0 = Bits of Slice 0 POWERUPFSMCTL register are R/W 1 = All bits of Slice 0 POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:9	**Reserved** Access: RO Reserved
	8:6	**Power UP state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - De-assert resets 3'b000: 10ns (or 1 bclk)
	5:3	**Power UP state 2** Default Value: 001b Access: R/W Lock

		This will be the 2nd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Firewall OFF
	2:0	**Power UP state 1** Default Value: 000b Access: R/W Lock This will be the 1st state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Clock Ungate

Slice 0 SubSlice 0 PGFET control register with lock

SSM0SPCPFETCTL - Slice 0 SubSlice 0 PGFET control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	24408h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock 0 = Bits of PGFETCTL register are R/W 1 = All bits of PGFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:24	**Reserved** Access: RO Reserved
	23	**Power Well Status** Access: RO 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	22	**Powergood timer error** Access: RO 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	21:19	**Delay from enabling secondary PFETs to power good.** Default Value: 101b

SSM0SPCPFETCTL - Slice 0 SubSlice 0 PGFET control register with lock

		Access: R/W Lock Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns 3'b010: 160ns 3'b011: 240ns 3'b100: 320ns 3'b101: 480ns 3'b110: 640ns 3'b111: 1280ns
	18:16	**Strobe pulse period** Default Value: 011b Access: R/W Lock Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	15:0	**PFET Ladder Step Sequence** Default Value: 1111111111111111b Access: R/W Lock PFET Ladder STEP sequence The PFET ladder has 16 steps, each represented by its corresponding bit in pfetlddrstepseq[15:0]. If the bit location is set, it means we must step on that ladder stage before we go to the next stage. The SPC controller will step through all the steps with asserted bits periodically with period equal to strbpulsprd[2:0] Programming Rule: pfetldrstepseq[15] and pfetldrstepseq[0] must be ‘1; A ‘0 setting for these bits is illegal. 15'FFFFh: Ladder step (ladder_sel) goes 0, 1, 2, ?.15. 15'FFF1h: Ladder step goes 0, 4, 5, 6,?15; Steps 1, 2, 3 are skipped. 15'D555h: Ladder step goes 0, 2, 4, 6, 8, 10, 12, 14, 15; Steps 1, 3, 5, 7, 9, 11, 13 are skipped. 15'80001h: Ladder step goes 0, 15; Steps 1, 2, 3, 4, ?14 are skipped.

Slice 0 SubSlice 1 PGFET control register with lock

SSM1SPCPFETCTL - Slice 0 SubSlice 1 PGFET control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	24488h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock 0 = Bits of PGFETCTL register are R/W 1 = All bits of PGFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:24	**Reserved** Access: RO Reserved
	23	**Power Well Status** Access: RO 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	22	**Powergood timer error** Access: RO 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	21:19	**Delay from enabling secondary PFETs to power good.** Default Value: 101b

SSM1SPCPFETCTL - Slice 0 SubSlice 1 PGFET control register with lock

		Access: R/W Lock Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns 3'b010: 160ns 3'b011: 240ns 3'b100: 320ns 3'b101: 480ns 3'b110: 640ns 3'b111: 1280ns
	18:16	**Strobe pulse period** Default Value: 011b Access: R/W Lock Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	15:0	**PFET Ladder Step Sequence** Default Value: 1111111111111111b Access: R/W Lock PFET Ladder STEP sequence The PFET ladder has 16 steps, each represented by its corresponding bit in pfetlddrstepseq[15:0]. If the bit location is set, it means we must step on that ladder stage before we go to the next stage. The SPC controller will step through all the steps with asserted bits periodically with period equal to strbpulsprd[2:0] Programming Rule: pfetldrstepseq[15] and pfetldrstepseq[0] must be ‘1; A ‘0 setting for these bits is illegal. 15'FFFFh: Ladder step (ladder_sel) goes 0, 1, 2, ?.15. 15'FFF1h: Ladder step goes 0, 4, 5, 6,?15; Steps 1, 2, 3 are skipped. 15'D555h: Ladder step goes 0, 2, 4, 6, 8, 10, 12, 14, 15; Steps 1, 3, 5, 7, 9, 11, 13 are skipped. 15'80001h: Ladder step goes 0, 15; Steps 1, 2, 3, 4, ?14 are skipped.

Slice 0 SubSlice 2 PGFET control register with lock

SSM2SPCPFETCTL - Slice 0 SubSlice 2 PGFET control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	24508h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock 0 = Bits of PGFETCTL register are R/W 1 = All bits of PGFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:24	**Reserved** Access: RO Reserved
	23	**Power Well Status** Access: RO 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	22	**Powergood timer error** Access: RO 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	21:19	**Delay from enabling secondary PFETs to power good.** Default Value: 101b

SSM2SPCPFETCTL - Slice 0 SubSlice 2 PGFET control register with lock

		Access: R/W Lock Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns 3'b010: 160ns 3'b011: 240ns 3'b100: 320ns 3'b101: 480ns 3'b110: 640ns 3'b111: 1280ns
	18:16	**Strobe pulse period** Default Value: 011b Access: R/W Lock Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 23ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	15:0	**PFET Ladder Step Sequence** Default Value: 1111111111111111b Access: R/W Lock PFET Ladder STEP sequence The PFET ladder has 16 steps, each represented by its corresponding bit in pfetlddrstepseq[15:0]. If the bit location is set, it means we must step on that ladder stage before we go to the next stage. The SPC controller will step through all the steps with asserted bits periodically with period equal to strbpulsprd[2:0] Programming Rule: pfetldrstepseq[15] and pfetldrstepseq[0] must be ‘1; A ‘0 setting for these bits is illegal. 15'FFFFh: Ladder step (ladder_sel) goes 0, 1, 2, ?.15. 15'FFF1h: Ladder step goes 0, 4, 5, 6,?15; Steps 1, 2, 3 are skipped. 15'D555h: Ladder step goes 0, 2, 4, 6, 8, 10, 12, 14, 15; Steps 1, 3, 5, 7, 9, 11, 13 are skipped. 15'80001h: Ladder step goes 0, 15; Steps 1, 2, 3, 4, ?14 are skipped.

Slice 1 - 5 BONUS1 Reg

SL15SPCBONUS1 - Slice 1 - 5 BONUS1 Reg		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	24214h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:8	**Reserved** Access: RO Reserved
	7	**BONUS1 BIT 7** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS1 BIT 6** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS1 BIT 5** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS1 BIT 4** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	3	**BONUS1 BIT 3** Access: R/W

SL15SPCBONUS1 - Slice 1 - 5 BONUS1 Reg

		SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS1 BIT 2** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS1 BIT 1** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS1 BIT 0** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

Slice 1 - 5 BONUS2 Reg

SL15SPCBONUS2 - Slice 1 - 5 BONUS2 Reg		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	24218h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:8	**Reserved** Access: RO Reserved
	7	**BONUS2 BIT 7** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS2 BIT 6** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS2 BIT 5** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS2 BIT 4** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	3	**BONUS2 BIT 3** Access: R/W

SL15SPCBONUS2 - Slice 1 - 5 BONUS2 Reg

		SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS2 BIT 2** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS2 BIT 1** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS2 BIT 0** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

Slice 1 - 5 PGFET control register with lock

SL15SPCPFETCTL - Slice 1 - 5 PGFET control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	24208h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock 0 = Bits of Slice 0 PGFETCTL register are R/W 1 = All bits of Slice 0 PGFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:24	**Reserved** Access: RO Reserved
	23	**Power Well Status** Access: R/WC strbpulsprdwered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	22	**Powergood timer error** Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	21:19	**Delay from enabling secondary PFETs to power good.** Default Value: 111b Access: R/W Lock Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns

		3'b010: 160ns 3'b011: 240ns 3'b100: 320ns 3'b101: 480ns 3'b110: 640ns 3'b111: 1280ns
	18:16	**Strobe pulse period** Default Value: 011b Access: R/W Lock Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	15:0	**PFET Ladder Step Sequence** Default Value: 1111111111111111b Access: R/W Lock PFET Ladder STEP sequence The PFET ladder has 16 steps, each represented by its corresponding bit in pfetlddrstepseq[15:0]. If the bit location is set, it means we must step on that ladder stage before we go to the next stage. The SPC controller will step through all the steps with asserted bits periodically with period equal to strbpulsprd[2:0] Programming Rule: pfetldrstepseq[15] and pfetldrstepseq[0] must be '1; A '0 setting for these bits is illegal. 15'FFFFh: Ladder step (ladder_sel) goes 0, 1, 2, ?.15. 15'FFF1h: Ladder step goes 0, 4, 5, 6,?15; Steps 1, 2, 3 are skipped. 15'D555h: Ladder step goes 0, 2, 4, 6, 8, 10, 12, 14, 15; Steps 1, 3, 5, 7, 9, 11, 13 are skipped. 15'80001h: Ladder step goes 0, 15; Steps 1, 2, 3, 4, ?14 are skipped.

Slice 1-5 Power Context Save request

SL15PGCTXREQ - Slice 1-5 Power Context Save request		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	24204h	
DWord	**Bit**	**Description**
0	31:16	**Message Mask** Access: RO Message Mask bots for lower 16 bits
	15:10	**Reserved** Access: RO Reserved
	9	**Power context save request** Access: R/W Set Power Context Save Request 1'b0 : Power context save is not being requested 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

Slice 1 - 5 Power Down FSM control register with lock

SL15SPCPOWERDNFSMCTL - Slice 1 - 5 Power Down FSM control register with lock

Register Space: MMIO: 0/2/0

Source: BSpec

Size (in bits): 32

Address: 24210h

DWord	Bit	Description
0	31	**power down control Lock** Access: R/W Lock 0 = Bits of Slice 1 POWERDNFSMCTL register are R/W 1 = All bits of Slice 1 POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:13	**Reserved** Access: RO Reserved
	12	**Leave firewall disabled** Access: R/W Lock When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e dont firewall the gated domain, but complete logical flow
	11	**Leave reset de-asserted** Access: R/W Lock When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e dont assert reset, but complete logical flow
	10	**Leave CLKs ON** Access: R/W Lock

SL15SPCPOWERDNFSMCTL - Slice 1 - 5 Power Down FSM control register with lock

		When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e dont clock gate, but complete logical flow
	9	**Leave FET On** Access: R/W Lock When This bit is set SPC will not turn off the PFET eventhough it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e dont power off pfet, but complete logical flow
	8:6	**Power Down state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Gate Clocks
	5:3	**Power Down state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default :Firewall ON
	2:0	**Power Down state 1** Default Value: 000b Access: R/W Lock This will be the 1st state before power is turned OFF in the well Encodings: 000 = Assert Reset

SL15SPCPOWERDNFSMCTL - Slice 1 - 5 Power Down FSM control register with lock		
		001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Assert Reset

Slice 1 - 5 Power Gate Control Request

SL15PGCTLREQ - Slice 1 - 5 Power Gate Control Request

Register Space: MMIO: 0/2/0

Source: BSpec

Size (in bits): 32

Address: 24200h

Clock Gating Messages Register

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:2	**Reserved** Access: RO Reserved
	1	**CLK RST FWE Request** Access: R/W SLICE 0 CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**Power Gate Request** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

Slice 1 -5 Power on FSM control register with lock

SL15SPCPOWERUPFSMCTL - Slice 1 -5 Power on FSM control register with lock

Register Space: MMIO: 0/2/0

Source: BSpec

Size (in bits): 32

Address: 2420Ch

DWord	Bit	Description
0	31	**power up control Lock** Access: R/W Lock 0 = Bits of Slice 1 POWERUPFSMCTL register are R/W 1 = All bits of Slice 1 POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:9	**Reserved** Access: RO Reserved
	8:6	**Power UP state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - De-assert resets 3'b000: 10ns (or 1 bclk)
	5:3	**Power UP state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF

		010 = De-assert resets 1xx = Rsvd for future Default - Firewall OFF
	2:0	**Power UP state 1** Default Value: 000b Access: R/W Lock This will be the 1st state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Clock Ungate

Slice Common Power Context Save request

SCPCTXSAVEREQ - Slice Common Power Context Save request		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	08140h	
DWord	**Bit**	**Description**
0	31:16	**Message Mask** Access: RO Message Mask bots for lower 16 bits
	15:10	**Reserved** Access: RO Reserved
	9	**Power context save request** Access: R/W Set Power Context Save Request 1'b0 : Power context save is not being requested 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

Slice unit Level Clock Gating Control 94D0

SCCGCTL94D0 - Slice unit Level Clock Gating Control 94D0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	094D0h	
Unit Level Clock Gating Disable bits		
DWord	**Bit**	**Description**
0	31:2	**Reserved** Access: R/W Reserved
	1	**GCPunit Clock Gating Disable** Default Value: 1b Access: R/W GCPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	0	**SMCRunit Clock Gating Disable** Default Value: 1b Access: R/W SMCRunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Slice unit Level Clock Gating Control 94D4

SCCGCTL94D4 - Slice unit Level Clock Gating Control 94D4		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	094D4h	
Unit Level Clock Gating Disable bits		
DWord	**Bit**	**Description**
0	31	**SPARE Clock Gating Disable 2** Access: R/W SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	30	**lsqcunit Clock Gating Disable** Access: R/W lsqcunit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	29	**ccunit Clock Gating Disable** Access: R/W ccunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	28	**DAPunit Clock Gating Disable** Access: R/W DAPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	27	**GACBunit Clock Gating Disable**

SCCGCTL94D4 - Slice unit Level Clock Gating Control 94D4

		Access: R/W GACBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	26	**GAFSRRB Clock Gating Disable** Access: R/W GAFSRRB Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	25	**GAHSunit Clock Gating Disable** Access: R/W GAHSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	24	**GAPCunit Clock Gating Disable** Access: R/W GAPCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	23	**GAPL3unit Clock Gating Disable** Access: R/W GAPL3unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	22	**GAPSunit Clock Gating Disable** Access: R/W GAPSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	21	**GAPZunit Clock Gating Disable**

SCCGCTL94D4 - Slice unit Level Clock Gating Control 94D4

	Access:	R/W

GAPZunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

20 **gassunit Clock Gating Disable**

Access:	R/W

gassunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

19 **HIZunit Clock Gating Disable**

Access:	R/W

HIZunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

18 **IZunit Clock Gating Disable**

Access:	R/W

IZunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

17 **L3 Clock Gating Disable**

Access:	R/W

L3 Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Workaround
The L3 clock gating should be kept disabled by programming this bit to 'b1

16 **L3 Clock Gating Disable cr2x**

Access:	R/W

L3 Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)

SCCGCTL94D4 - Slice unit Level Clock Gating Control 94D4

'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Workaround
The L3 clock gating should be kept disabled by programming this bit to 'b1

15	**L3Bank Clock Gating Disable cr**
	Access: R/W
	L3 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
14	**L3Bank Clock Gating Disable cr2x**
	Access: R/W
	L3 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
13	**L3BANK Clock Gating Disable cu**
	Access: R/W
	l3bank L3BANK Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
12	**L3BANK Clock Gating Disable cu2x**
	Access: R/W
	L3BANK Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
11	**lsnunit Clock Gating Disable**
	Access: R/W
	lsnunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
10	**MSCunit Clock Gating Disable**
	Access: R/W

SCCGCTL94D4 - Slice unit Level Clock Gating Control 94D4

		MSCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Programming Notes** For A step MSC Clock gating need to be disabled. This issue is fixed for B Step.
	9	**OAADDRunit Clock Gating Disable** Access: R/W OAADDRunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	8	**OASCREP Clock Gating Disable** Access: R/W OASCREP Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	7	**RCCunit Clock Gating Disable** Access: R/W RCCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	6	**RCZunit Clock Gating Disable** Access: R/W RCZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	5	**Sarbunit Clock Gating Disable** Access: R/W Sarbunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	4	**SBEunit Clock Gating Disable**

SCCGCTL94D4 - Slice unit Level Clock Gating Control 94D4

		Access: R/W SBEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	3	**STCunit Clock Gating Disable** Access: R/W STCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	2	**SVLunit Clock Gating Disable** Access: R/W SVLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	1	**WMBE Clock Gating Disable** Access: R/W WMBE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	0	**WMFEunit Clock Gating Disable** Access: R/W WMFEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Slice unit Level Clock Gating Control 94D8

SCCGCTL94D8 - Slice unit Level Clock Gating Control 94D8		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	094D8h	
Unit Level Clock Gating Disable bits		
DWord	**Bit**	**Description**
0	31:13	**Reserved** Format: MBZ
	12	**AMFS unit Clock Gating Disable f** Access: R/W AMFS unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	11	**AMFS unit Clock Gating Disable c** Access: R/W AMFS unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	10	**AMFS unit Clock Gating Disable d** Access: R/W AMFS unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	9	**GADSS unit Clock Gating Disable** Access: R/W

SCCGCTL94D8 - Slice unit Level Clock Gating Control 94D8

		SLMBE unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	8	**SLMBE unit Clock Gating Disable** Access: R/W SLMBE unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	7	**SFBEunit Clock Gating Disable** Access: R/W SFBEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	6	**LNEunit Clock Gating Disable** Access: R/W LNEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	5	**LNIunit Clock Gating Disable** Access: R/W LNIunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	4	**RCPBunit Clock Gating Disable** Access: R/W RCPBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	3	**RCPBEunit Clock Gating Disable**

SCCGCTL94D8 - Slice unit Level Clock Gating Control 94D8

		Access: R/W RCPBEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	2	**TDCunit Clock Gating Disable** Access: R/W TDCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	1	**RAMdft Clock Gating Disable** Access: R/W RAMdft Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	0	**Reserved**

Slice unit Level Clock Gating Control 94DC

SCCGCTL94DC - Slice unit Level Clock Gating Control 94DC

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	094DCh

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31:13	**Reserved** Access: R/W Reserved
	12	**CS FE Clock Gating Disable** Access: R/W CS FE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	11	**CS BE Clock Gating Disable** Access: R/W Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	10	**POCS FE Clock Gating Disable** Access: R/W POCS FE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	9	**POCS BE Clock Gating Disable** Access: R/W POCS BE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)

SCCGCTL94DC - Slice unit Level Clock Gating Control 94DC

		'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	8	**CCS FE Clock Gating Disable** Access: R/W CCS FE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	7	**CCS BE Clock Gating Disable** Access: R/W CCS BE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	6	**LTCD_TAG Clock Gating Disable** Access: R/W LTCD_TAG Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	5	**LTCC Clock Gating Disable** Access: R/W LTCC Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	4	**LBS Clock Gating Disable** Access: R/W LBS Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	3	**LBI Clock Gating Disable** Access: R/W LBI Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)

SCCGCTL94DC - Slice unit Level Clock Gating Control 94DC

		'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	2	**LBCF Clock Gating Disable** Access: R/W LBCF Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	1	**LTCD_DATA Clock Gating Disable** Access: R/W LTCD_DATA Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	0	**LSQD Clock Gating Disable** Access: R/W LSQD Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Slice unit Level Clock Gating Control 94E0

SCCGCTL94E0 - Slice unit Level Clock Gating Control 94E0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	094E0h	
Unit Level Clock Gating Disable bits		
DWord	**Bit**	**Description**
0	31	**Reserved** Format: MBZ
	30:13	**Reserved** Format: MBZ
	12	**SPARE Clock Gating Disable** Access: R/W SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	11	**MSCunit Clock Gating Disable** Access: R/W MSCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	10	**RCPFEunit Clock Gating Disable** Access: R/W RCPFEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	9	**AVSunit Clock Gating Disable** Access: R/W AVSunit Clock Gating Disable Control:

SCCGCTL94E0 - Slice unit Level Clock Gating Control 94E0

		'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	8	**daprssunit Clock Gating Disable** Access: R/W daprssunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	7	**HIZunit Clock Gating Disable** Access: R/W HIZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	6	**IZunit Clock Gating Disable** Access: R/W IZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	5	**RCCunit Clock Gating Disable** Access: R/W RCCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	4	**RCZunit Clock Gating Disable** Access: R/W RCZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	3	**SBEunit Clock Gating Disable** Access: R/W

SCCGCTL94E0 - Slice unit Level Clock Gating Control 94E0		
		SBEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	2	**STCunit Clock Gating Disable** Access: R/W STCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	1	**SVLunit Clock Gating Disable** Access: R/W SVLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	0	**WMFEunit Clock Gating Disable** Access: R/W WMFEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Slice unit Level Clock Gating Control 94E4

SCCGCTL94E4 - Slice unit Level Clock Gating Control 94E4

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	094E4h

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31:30	**Reserved** Access: R/W Reserved
	29	**CCS Clock Gating Disable** Access: R/W CCS Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	28	**sdfifo Clock Gating Disable svg** Access: R/W sdfifo Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	27	**sdfifo Clock Gating Disable svl** Access: R/W sdfifo Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	26	**PSS unit Clock Gating Disable** Access: R/W PSS Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)

SCCGCTL94E4 - Slice unit Level Clock Gating Control 94E4

		'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	25	**CARB unit Clock Gating Disable** Access: R/W CARB Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	24	**ZPBE unit Clock Gating Disable** Access: R/W ZPBE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	23	**ZSCBANK unit Clock Gating Disable** Access: R/W ZSCBANK Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	22	**ZSCCOMPUTE unit Clock Gating Disable** Access: R/W ZSCCOMPUTE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	21	**GAFARB unit Clock Gating Disable** Access: R/W GAFARB Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	20	**VSR unit Clock Gating Disable** Access: R/W VSR Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)

SCCGCTL94E4 - Slice unit Level Clock Gating Control 94E4

		'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	19	**VS unit Clock Gating Disable** Access: R/W VS Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	18	**VFR unit Clock Gating Disable** Access: R/W VFR Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	17	**VFE Clock Gating Disable** Access: R/W VFE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	16	**VF unit Clock Gating Disable** Access: R/W VF Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	15	**URBM unit Clock Gating Disable** Access: R/W URBM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	14	**TSG unit Clock Gating Disable** Access: R/W TSG Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)

SCCGCTL94E4 - Slice unit Level Clock Gating Control 94E4

		'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	13	**TETG unit Clock Gating Disable** Access: R/W TETG Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	12	**TE unit Clock Gating Disable** Access: R/W TE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	11	**TDS unit Clock Gating Disable** Access: R/W TDS Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	10	**TDG unit Clock Gating Disable** Access: R/W TDG Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	9	**SVGR unit Clock Gating Disable** Access: R/W SVGR Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	8	**SVG unit Clock Gating Disable** Access: R/W SVG Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)

SCCGCTL94E4 - Slice unit Level Clock Gating Control 94E4

	'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
7	**SOL unit Clock Gating Disable** Access: R/W SOL Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
6	**gwunit Clock Gating Disable** Access: R/W gwunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
5	**psdunit Clock Gating Disable** Access: R/W psdunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
4	**hdcunit Clock Gating Disable** Access: R/W hdcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
3	**cpssunit Clock Gating Disable** Access: R/W cpssunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
2	**besbufunit Clock Gating Disable** Access: R/W besbufunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)

SCCGCTL94E4 - Slice unit Level Clock Gating Control 94E4		
		'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	1	**sbc Clock Gating Disable** Access: R/W sbcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	0	**tdpunit Clock Gating Disable** Access: R/W tdpEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Slice unit Level Clock Gating override during rstflow 94F0

SCMISCCP94F0 - Slice unit Level Clock Gating override during rstflow 94F0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	094F0h

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31	**clock gate control Lock** Access: R/W Lock 0 = Bits of MISCCPCTL register are R/W 1 = All bits of MISCCPCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:1	**Reserved** Access: R/W Reserved
	0	**L1UGT during rst flow** Default Value: 1b Access: R/W misccp Clock Gating Disable Control: '0' : Clock Gating Enabled during reset flows (i.e., clocks can be gated when they are not required to toggle for functionality, NOT Recommended) '1' : Clock Gating Disabled during reset flows. (i.e., clocks are toggling, always) Register bit defaults to value 1'b1, which is a requirement due to Synchronous reset flops Randomizing this bit will result in X flush not completing during the simulation

SLM Bank Hash

SLM_BANKHASH - SLM Bank Hash

Register Space: MMIO: 0/2/0

Source: BSpec

Size (in bits): 32

Address: 0E660h

Register for XOR hashing SLM bank select bits.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:12	**bit5 Hash** Access: R/W Format: U4 This field defines which address bit(s) will be XOR-ed with address bit[5] to produce new address bit[5]. Multiple bits can be set to XOR multiple address bit with bit[5]. **Value** / **Name** / **Description** 1h / A9 / When set, XOR address[5] with address[9] to produce new address[5]. 2h / A13 / When set, XOR address[5] with address[13] to produce new address[5]. 4h / A17 / When set, XOR address[5] with address[6] to produce new address[5]. 8h / A10 / When set, XOR address[5] with address[10] to produce new address[10]. 0h / No XOR **[Default]** / Address[5] is not XOR-ed with any other address bit.
	11:8	**bit4 Hash** Access: R/W Format: U4 This field defines which address bit(s) will be XOR-ed with address bit[4] to produce new address bit[4]. Multiple bits can be set to XOR multiple address bit with bit[4]. **Value** / **Name** / **Description** 1h / A8 / When set, XOR address[4] with address[8] to produce new address[4]. 2h / A12 / When set, XOR address[4] with address[12] to produce new address[4].

4h	A16	When set, XOR address[4] with address[16] to produce new address[4].
8h	A9	When set, XOR address[4] with address[9] to produce new address[4].
0h	No XOR **[Default]**	Address[4] is not XOR-ed with any other address bit.

7:4 **bit3 Hash**

Access:	R/W
Format:	U4

This field defines which address bit(s) will be XOR-ed with address bit[3] to produce new address bit[3]. Multiple bits can be set to XOR multiple address bit with bit[3].

Value	Name	Description
1h	A7	When set, XOR address[3] with address[7] to produce new address[3].
2h	A11	When set, XOR address[3] with address[11] to produce new address[3].
4h	A15	When set, XOR address[3] with address[15] to produce new address[3].
8h	A8	When set, XOR address[3] with address[8] to produce new address[3].
0h	No XOR **[Default]**	Address[3] is not XOR-ed with any other address bit.

3:0 **bit2 Hash**

Access:	R/W
Format:	U4

This field defines which address bit(s) will be XOR-ed with address bit[2] to produce new address bit[2]. Multiple bits can be set to XOR multiple address bit with bit[2].

Value	Name	Description
1h	A6	When set, XOR address[2] with address[6] to produce new address[2].
2h	A10	When set, XOR address[2] with address[10] to produce new address[2].
4h	A14	When set, XOR address[2] with address[14] to produce new address[2].
8h	A7	When set, XOR address[2] with address[7] to produce new address[7].
0h	No XOR **[Default]**	Address[2] is not XOR-ed with any other address bit.

Snoop control register

SNPCR - Snoop control register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0900Ch

Snoop control register

DWord	Bit	Description
0	31:23	**Reserved** Access: RO
	22:21	**Spare**
	20	**Non Temporal** Access: R/W Indication to uncore that - Request is of the type that should get minimal cache resources in the uncore.
	19:17	**RSVD** Access: RO
	16	**Restrict Snoops to MSQC, no forwarding to L3** Access: R/W 1'b0 - Snoops are not restricted. 1'b1 - Restrict snoops to MSQC and do not forward to Node snoop unit (L3).
	15	**Thread ID** Access: R/W 1 bit Thread ID for GT.
	14	**Force Invalidate** Access: R/W Force Invalidate - Forces the invalidate flag to be set with snoop lookups all the time. 0: Normal invalidation (based on req) - Default. 1: Forced invalidation.
	13:11	**IDI Pend Timer** Default Value: 011b

		Access: R/W IDIpend timer - Time to wait before monitoring the sq_snpc_idipend signal. 000b => 0 clocks. 001b => 1 clock. 010b => 2 clocks. 011b => 4 clocks (default.) 100b => 8. 101b => 16. 110b => 32. 111b => 64.
	10:8	**Retry Limit** Default Value: 011b Access: R/W Retry Limit - Number of times to retry before switching to the freeze mechanism. 000b => Always freeze (first shot). 001b => 1 retry. 010b => 2 retry. 011b => 4 retry (default). 100b => 8 retry. 101b => 16 retry. 110b => 32 retry. 111b => infinite (no freeze).
	7:3	**Retry Timer** Default Value: 01000b Access: R/W Retry Timer - Time between receiving a reject from SQ and repeating the monitor sequence. 00000b => 0 clocks. 00001b => 1 clock. 00010b => 2 clocks. 00011b => 3 clocks. 00111b => 7 clocks. 01000b => 8 clocks (Default). ... 11111b => 32 clocks.
	2:0	**MLCSQ Timer** Access: R/W MLC-SQ Timer - Time between doing an MLC lookup and SQ lookup. 000b => 0 clocks (default). 001b => 1 clock. 010b => 2 clocks.

SNPCR - Snoop control register		
		011b => 4 clocks. 100b => 8. 101b => 16. 110b => 32. 111b => 64.

SQ Error Status

SQERR - SQ Error Status

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	09034h

SQ Error Status register

DWord	Bit	Description
0	31:9	**RSVD** Access: RO
	8	**SQ RW Port Address Decode Error** Access: RO Variant SQ RW Address Decode Error. This bit is cleared when SW writes to this bit. SW can not physically write to this bit. Any write (with proper byte enable set) will clear this bit, independent of value attempted to be written. Writing a one will clear the bit and writing a zero will clear this bit. Hardware will only capture the first occurance of address decode error and will not capture subsequent detected errors, until SW clears this bit.
	7:1	**RSVD** Access: RO
	0	**SQ RO Port Address Decode Error** Access: RO Variant SQ RO Address Decode Error. This bit is cleared when SW writes to this bit. SW can not physically write to this bit. Any write (with proper byte enable set) will clear this bit, independent of value attempted to be written. Writing a one will clear the bit and writing a zero will clear this bit. Hardware will only capture the first occurance of address decode error and will not capture subsequent detected errors, until SW clears this bit.

SQ RO Port Decode Error Address LSB

SQROERRADDR_LSB - SQ RO Port Decode Error Address LSB		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	09210h	
SQ RO Port Decode Error Address		
DWord	**Bit**	**Description**
0	31:0	**SQ RO Port Error Address LSB** Access: RO SQ RO Port Decode Error Address.

SQ RO Port Decode Error Address MSB

SQROERRADDR_MSB - SQ RO Port Decode Error Address MSB		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	09214h	
SQ RO Port Decode Error Address		
DWord	**Bit**	**Description**
0	31:8	**RSVD** Access: RO
	7:0	**SQ RO Port Error Address MSB** Access: RO SQ RO Port Decode Error Address.

SQ RW Port Decode Error Address LSB

SQRWERRADDR_LSB - SQ RW Port Decode Error Address LSB		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	09218h	
SQ RW Port Deocde Error Address		
DWord	**Bit**	**Description**
0	31:0	**SQ RW Port Error Address LSB** Access: RO SQ RW Port Error Address.

SQ RW Port Decode Error Address MSB

SQRWERRADDR_MSB - SQ RW Port Decode Error Address MSB		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	0921Ch	
SQ RW Port Deocde Error Address		
DWord	**Bit**	**Description**
0	31:8	**RSVD** Access: RO
	7:0	**SQ RW Port Error Address MSB** Access: RO SQ RW Port Error Address.

SRD_CTL

SRD_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	60800h-60803h
Name:	Transcoder A SRD Control
ShortName:	SRD_CTL_A
Power:	PG2
Reset:	soft
Address:	61800h-61803h
Name:	Transcoder B SRD Control
ShortName:	SRD_CTL_B
Power:	PG2
Reset:	soft
Address:	62800h-62803h
Name:	Transcoder C SRD Control
ShortName:	SRD_CTL_C
Power:	PG2
Reset:	soft
Address:	6F800h-6F803h
Name:	Transcoder EDP SRD Control
ShortName:	SRD_CTL_EDP
Power:	PG1
Reset:	soft

Description
Restriction : PSR needs to be enabled only when at least one plane is enabled.

Programming Notes
To use FBC modification tracking for idleness calculations when FBC is disabled, program FBC_CTL CPU Fence

SRD_CTL

Enable, FBC_CONTROL_SA_REGISTER, FBC_CPU_FENCE_OFFSET_REGISTER, FBC_RT_BASE_ADDR_REGISTER, and BLITTER_TRACKING_REGISTER as they are programmed when FBC is enabled.
Cursor front buffer modifications are not tracked in hardware. If the cursor front buffer is modified, touch (write without changing) any cursor register to trigger the PSR idleness tracking.

Restriction
Only the SRD Enable and Single Frame Update Enable fields can be changed while SRD is enabled. The other fields must not be changed while SRD is enabled.

DWord	Bit	Description
0	31	**SRD Enable** This bit enables the Self Refreshing Display function. Updates will take place at the start of the next vertical blank. The port will send SRD VDMs while enabled. When idleness conditions have been met for the programmed number of idle frames, hardware will enter SRD (sleep) and can disable the link and stop fetching data from memory. When activity occurs, hardware will exit SRD (wake) and re-enable the link and resume fetching data from memory.

Value	Name
0b	Disable
1b	Enable

Restriction
SRD must not be enabled when the PSR Setup time from DPCD 00071h is greater than the time for vertical blank minus one line.
SRD must not be enabled together with Interlacing, Black Frame Insertion (BFI), or audio on the same transcoder.

	30	**Single Frame Update Enable** Access: Double Buffered This field enables the single frame update mode where a plane flip will cause a single frame to be sent to the receiver. Updates to this field will take effect at the next vertical blank.

Value	Name
0b	Disable
1b	Enable

Programming Notes
Set register PIPE_MISC field Change Mask for Vblank Vsync Int to 1b (Masked) if vblank or vsync interrupts will be used together with single frame update.

Workaround
When Single Frame Update is enabled, the CRC must be disabled for panel compatibility.

SRD_CTL

		Restriction This mode should only be enabled with link standby.
	29	**Context restore to PSR Active** This field restores eDP context to PSR Active on a context restore. **Value** / **Name** 0b – Disable 1b – Enable **Restriction** This field is used for hardware communication. Software must not change this field.
	28	**Adaptive Sync Frame Update** This field enables the Adaptive Sync Frame Update mode where a flip will cause a single frame to be sent to the receiver. Updates to this field will take effect at the next vertical blank. This field must be enabled with VRR enable. Restriction : This mode should only be enabled with the SRD Link Disable mode. This mode does not support VRR Max Shift. However, normal and flipline VRR modes are supported. **Value** / **Name** 0b – Disable 1b – Enable **Programming Notes** Set register PIPE_MISC field **Change Mask for Vblank Vsync Int** to 1b (Masked) if vblank or vsync interrupts will be used together with single frame update.
	27	**Link Ctrl** This field controls the behavior of the link when in SRD (sleeping). The timing generator and pixel data fetches are disabled when the link is disabled. Only pixel data fetches are disabled when the link is in standby. This field is ignored by transcoder A/B/C since they only operate in standby. **Value** / **Name** / **Description** 0b – Disable – Link is disabled when in SRD (sleeping) 1b – Standby – Link is in standby when in SRD (sleeping)
	26:25	**Reserved** Format: MBZ
	24:20	**Max Sleep Time**

SRD_CTL

Default Value:	00001b 1/8 second

This field is the maximum time to spend in SRD (sleeping). It is programmed in increments of approximately 1/8 a second. Programming all 1s gives ~3.875 seconds.

Restriction
Programming all 0s is invalid.

19:14 Reserved

Format:	MBZ

13 TPS4 Control

Value	Name	Description
0b	Complete	Completes TPS4 pattern after TP4 counter expires.
1b	Terminate	Terminates TPS4 pattern after TP4 counter expires.

12 Reserved

11 TP2 TP3 Select

This field controls whether TP1 is followed by TP2 or TP3 for training the link on exiting SRD (waking).

Value	Name	Description
0b	TP2	Use TP1 followed by TP2
1b	TP3	Use TP1 followed by TP3

Programming Notes
This bit impacts PSR2. Clear it before enabling PSR2 and do not set it while PSR2 is enabled.

10 CRC Enable

This field controls whether the PSR CRC value will be placed in the VSC packet.

Value	Name	Description
0b	Disable	Disable CRC output in VSC. VSC packet CRC value will be populated by VIDEO_DIP_DATA.
1b	Enable	Enable CRC output in VSC. VSC packet CRC value will be populated by the calculated CRC value.

Programming Notes
When CRC is enabled, the Max Sleep Timer should be disabled to provide additional power savings. Disable the Max Sleep Timer by setting register 0x6F860 bit 28 to 1. Re-enable the Max Sleep Timer by clearing register 0x6F860 bit 28 to 0.

Workaround

SRD_CTL

		When Single Frame Update is enabled, the CRC must be disabled for panel compatibility.
	9:8	**TP2 TP3 Time** This field selects the TP2 or TP3 time when training the link on exiting SRD (waking). **Value** / **Name** 00b: 500us 01b: 100us 10b: 2.5ms 11b: 0us Skip TP2/TP3
	7:6	**TP4 time** This field selects the TP4 time when training the link on exiting SRD (waking). If this field is set to any value other than "11", TP4 pattern will be sent at PSR reentry. **Value** / **Name** / **Description** 00b: 500 us 01b: 100 us 10b: 2.5 ms 11b: 0 us: Skip TP4
	5:4	**TP1 Time** This field selects the TP1 time when training the link on exiting SRD (waking). **Value** / **Name** / **Description** 00b: 500us 01b: 100us 10b: 2.5ms 11b: 0us: Skip TP1
	3:0	**Idle Frames** Default Value: 0001b 1 idle frame This field is the number of idle frames required before entering SRD (sleeping).

SRD_IIR

SRD_IIR	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/WC
Size (in bits):	32
Address:	64838h-6483Bh
Name:	SRD Interrupt Identity
ShortName:	SRD_IIR
Power:	PG1
Reset:	soft

See the SRD interrupt bit definition to find the source event for each interrupt bit.

DWord	Bit	Description
0	31:0	**Interrupt Identity Bits** This field holds the persistent values of the SRD interrupt bits which are unmasked by the SRD_IMR. Bits set in this register will propagate to the SRD interrupt in the Display Engine Miscellaneous Interrupts. Bits set in this register will remain set (persist) until the interrupt condition is cleared by writing a '1' to the appropriate bits

Value	Name
0b	Condition Not Detected
1b	Condition Detected

SRD_IMR

SRD_IMR	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	64834h-64837h
Name:	SRD Interrupt Mask
ShortName:	SRD_IMR
Power:	PG1
Reset:	soft

See the SRD interrupt bit definition to find the source event for each interrupt bit.

DWord	Bit	Description
0	31:0	**Interrupt_Mask_Bits** This field contains a bit mask which selects which SRD events are reported int the SRD_IIR.

Value	Name
0b	Not Masked
1b	Masked
07070707h	All interrupts masked **[Default]**

SRD_PERF_CNT

SRD_PERF_CNT		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Access:	Write/Read Status	
Size (in bits):	32	
Address:	60844h-60847h	
Name:	Transcoder A SRD Performance Counter	
ShortName:	SRD_PERF_CNT_A	
Power:	PG2	
Reset:	soft	
Address:	61844h-61847h	
Name:	Transcoder B SRD Performance Counter	
ShortName:	SRD_PERF_CNT_B	
Power:	PG2	
Reset:	soft	
Address:	62844h-62847h	
Name:	Transcoder C SRD Performance Counter	
ShortName:	SRD_PERF_CNT_C	
Power:	PG2	
Reset:	soft	
Address:	6F844h-6F847h	
Name:	Transcoder EDP SRD Performance Counter	
ShortName:	SRD_PERF_CNT_EDP	
Power:	PG1	
Reset:	soft	

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:0	**SRD Perf Cnt** This field increments every millisecond while in SRD (sleeping) and the display CD clock is

SRD_PERF_CNT		
		running. It will stop incrementing when out of SRD (awake), then resume when back in SRD (sleeping). The value is maintained while SRD is disabled, and counting will resume from the previous value when SRD is re-enabled. Writes to this register will set the count to the written value, then it will increment from that value onwards.

SRD_STATUS

SRD_STATUS		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Access:	RO	
Size (in bits):	32	
Address:	60840h-60843h	
Name:	Transcoder A SRD Status	
ShortName:	SRD_STATUS_A	
Power:	PG2	
Reset:	soft	
Address:	61840h-61843h	
Name:	Transcoder B SRD Status	
ShortName:	SRD_STATUS_B	
Power:	PG2	
Reset:	soft	
Address:	62840h-62843h	
Name:	Transcoder C SRD Status	
ShortName:	SRD_STATUS_C	
Power:	PG2	
Reset:	soft	
Address:	6F840h-6F843h	
Name:	Transcoder EDP SRD Status	
ShortName:	SRD_STATUS_EDP	
Power:	PG1	
Reset:	soft	

DWord	Bit	Description
0	31:29	**SRD State** Access: RO This field indicates the live state of SRD

SRD_STATUS

Value	Name	Description
000b	IDLE	Reset state
001b	SRDONACK	Wait for TG/Stream to send on frame of data after SRD conditions are met
010b	SRDENT	SRD entry with Link OFF
011b	BUFOFF	Wait for buffer turn off
100b	BUFON	Wait for buffer turn on
101b	AUXACK	Wait for AUX to acknowledge on SRD exit
110b	SRDOFFACK	Wait for TG/Stream to acknowledge the SRD VDM exit
111b	SRDENT_ON	SRD entry with Link ON
Others	Reserved	Reserved

28 **Reserved**

Format:	MBZ

27:26 **Link Status**

Access:	RO

This field indicates the live status of the link.

Value	Name	Description
00b	Full Off	Link is fully off
01b	Full On	Link is fully on
10b	Standby	Link is in standby
11b	Reserved	Reserved

25 **Reserved**

Format:	MBZ

24:20 **Max Sleep Time Counter**

Access:	RO

This field provides the live status of the sleep time counter.

19:16 **SRD Entry Count**

Access:	RO

The value in this register represents the number of times SRD has been entered (gone to sleep). The count will increment with each entry. After reaching the maximum count value the counter will rollover and continue from 0.

15 **Aux Error**

Access:	RO

This field indicates an error on the last SRD AUX handshake.

Value	Name	Description

SRD_STATUS

	0b	No Error	AUX had no error
	1b	Error	AUX error (receive error or timeout) occured

14:13 Reserved

Format:	MBZ

12 Sending Aux

Access:	RO

This field indicates if the SRD AUX handshake is currently being sent.

Value	Name	Description
0b	Not Sending	Not sending AUX handshake
1b	Sending	Sending AUX handshake

11:10 Reserved

Format:	MBZ

9 Sending Idle

Access:	RO

This field indicates if idles are currently being sent.

Value	Name	Description
0b	Not Sending	Not sending idle
1b	Sending	Sending idle

8 Sending TP2 TP3

Access:	RO

This field indicates if TP2 or TP3 is currently being sent.

Value	Name	Description
0b	Not Sending	Not sending TP2 or TP3
1b	Sending	Sending TP2 or TP3

7 Sending TP4

Access:	RO

This field indicates if TP4 is currently being sent.

Value	Name
0b	Not Sending
1b	Sending

6:5 Reserved

Format:	MBZ

4 Sending TP1

Access:	RO

This field indicates if TP1 is currently being sent.

SRD_STATUS

Value	Name	Description
0b	Not Sending	Not sending TP1
1b	Sending	Sending TP1

3:0 **Idle Frame Counter**

Access:	RO

This field provides the live status of the idle frame counter.

Programming Notes
The value of this field is not preserved across power down states such as DC5 and up.

SSM0 BONUS1 Reg

SSM0SPCBONUS1 - SSM0 BONUS1 Reg		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	24414h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:8	**Reserved** Access: RO Reserved
	7	**BONUS1 BIT 7** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS1 BIT 6** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS1 BIT 5** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS1 BIT 4** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	3	**BONUS1 BIT 3** Access: R/W

SSM0SPCBONUS1 - SSM0 BONUS1 Reg		
		SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS1 BIT 2** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS1 BIT 1** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS1 BIT 0** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

SSM0 BONUS2 Reg

SSM0SPCBONUS2 - SSM0 BONUS2 Reg		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	24418h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:8	**Reserved** Access: RO Reserved
	7	**BONUS2 BIT 7** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS2 BIT 6** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS2 BIT 5** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS2 BIT 4** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	3	**BONUS2 BIT 3** Access: R/W

SSM0SPCBONUS2 - SSM0 BONUS2 Reg		
		SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS2 BIT 2** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS2 BIT 1** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS2 BIT 0** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

SSM1 BONUS1 Reg

SSM1SPCBONUS1 - SSM1 BONUS1 Reg		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	24494h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:8	**Reserved** Access: RO Reserved
	7	**BONUS1 BIT 7** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS1 BIT 6** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS1 BIT 5** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS1 BIT 4** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	3	**BONUS1 BIT 3** Access: R/W

SSM1SPCBONUS1 - SSM1 BONUS1 Reg

		SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS1 BIT 2** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS1 BIT 1** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS1 BIT 0** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

SSM1 BONUS2 Reg

SSM1SPCBONUS2 - SSM1 BONUS2 Reg		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	24498h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:8	**Reserved** Access: RO Reserved
	7	**BONUS2 BIT 7** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS2 BIT 6** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS2 BIT 5** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS2 BIT 4** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	3	**BONUS2 BIT 3** Access: R/W

SSM1SPCBONUS2 - SSM1 BONUS2 Reg		
		SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS2 BIT 2** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS2 BIT 1** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS2 BIT 0** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

SSM2 BONUS1 Reg

SSM2SPCBONUS1 - SSM2 BONUS1 Reg		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	24514h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:8	**Reserved** Access: RO Reserved
	7	**BONUS1 BIT 7** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS1 BIT 6** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS1 BIT 5** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS1 BIT 4** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	3	**BONUS1 BIT 3** Access: R/W

SSM2SPCBONUS1 - SSM2 BONUS1 Reg		
		SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS1 BIT 2** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS1 BIT 1** Access: R/W SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS1 BIT 0** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

SSM2 BONUS2 Reg

SSM2SPCBONUS2 - SSM2 BONUS2 Reg

Register Space: MMIO: 0/2/0

Source: BSpec

Size (in bits): 32

Address: 24518h

Clock Gating Messages Register

DWord	Bit	Description
0	31:8	**Reserved** Access: RO Reserved
	7	**BONUS2 BIT 7** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS2 BIT 6** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS2 BIT 5** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS2 BIT 4** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	3	**BONUS2 BIT 3** Access: R/W

SSM2SPCBONUS2 - SSM2 BONUS2 Reg

		SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS2 BIT 2** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS2 BIT 1** Access: R/W SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS2 BIT 0** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

State Ack Register Slice3

STATE_ACK_SLICE3 - State Ack Register Slice3

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	02104h-02107h
Name:	State Ack Register Slice3
ShortName:	STATE_ACK_SLICE3_RCSUNIT_BE
Address:	18104h-18107h
Name:	State Ack Register Slice3
ShortName:	STATE_ACK_SLICE3_POCSUNIT_BE

This register is used in HW to receive Acknowledges from State clients in Slice-3 for non-pipeline state. This register can be read on the MMIO for checking if an ACK is not received. This register should not be written by SW. Note that Slices, Half Slices and Sub Slices enabled on a platform are function of GT SKU.

DWord	Bit	Description
0	31:16	**Mask Bits** Access: WO Mask: [15:0] Format: Mask Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15	**TDL3 Ack** Exists If: //SubSlice3
	14	**TDL2 Ack** Exists If: //SubSlice2
	13	**TDL1 Ack** Exists If: //SubSlice1
	12	**TDL0 Ack**

STATE_ACK_SLICE3 - State Ack Register Slice3

		Exists If: //SubSlice0
	11:10	**Reserved** Format: MBZ
	9	**DM2 Ack** Exists If: //SubSlice2
	8	**SC2 Ack** Exists If: //SubSlice2
	7	**DM1 Ack** Exists If: //SubSlice1
	6	**DM0 Ack** Exists If: //SubSlice0
	5	**SC1 Ack** Exists If: //SubSlice1
	4	**SC0 Ack** Exists If: //SubSlice0
	3	**WM Ack** Exists If: //CommonSlice
	2	**SVL Ack** Exists If: //CommonSlice
	1:0	**Reserved** Format: MBZ

State Ack Register Slice4

STATE_ACK_SLICE4 - State Ack Register Slice4

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	02108h-0210Bh
Name:	State Ack Register Slice4
ShortName:	STATE_ACK_SLICE4_RCSUNIT_BE
Address:	18108h-1810Bh
Name:	State Ack Register Slice4
ShortName:	STATE_ACK_SLICE4_POCSUNIT_BE

This register is used in HW to receive Acknowledges from State clients in Slice-4 for non-pipeline state. This register can be read on the MMIO for checking if an ACK is not received. This register should not be written by SW. Note that Slices, Half Slices and Sub Slices enabled on a platform are function of GT SKU.

DWord	Bit	Description
0	31:16	**Mask Bits** Access: WO Mask: [15:0] Format: Mask Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15	**TDL3 Ack** Exists If: //SubSlice3
	14	**TDL2 Ack** Exists If: //SubSlice2
	13	**TDL1 Ack** Exists If: //SubSlice1
	12	**TDL0 Ack**

STATE_ACK_SLICE4 - State Ack Register Slice4

		Exists If: //SubSlice0
	11:10	**Reserved** Format: MBZ
	9	**DM2 Ack** Exists If: //SubSlice2
	8	**SC2 Ack** Exists If: //SubSlice2
	7	**DM1 Ack** Exists If: //SubSlice1
	6	**DM0 Ack** Exists If: //SubSlice0
	5	**SC1 Ack** Exists If: //SubSlice1
	4	**SC0 Ack** Exists If: //SubSlice0
	3	**WM Ack** Exists If: //CommonSlice
	2	**SVL Ack** Exists If: //CommonSlice
	1:0	**Reserved** Format: MBZ

State Ack Register Slice5

STATE_ACK_SLICE5 - State Ack Register Slice5

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	0210Ch-0210Fh
Name:	State Ack Register Slice5
ShortName:	STATE_ACK_SLICE5_RCSUNIT_BE
Address:	1810Ch-1810Fh
Name:	State Ack Register Slice5
ShortName:	STATE_ACK_SLICE5_POCSUNIT_BE

This register is used in HW to receive Acknowledges from State clients in Slice-5 for non-pipeline state. This register can be read on the MMIO for checking if an ACK is not received. This register should not be written by SW. Note that Slices, Half Slices and Sub Slices enabled on a platform are function of GT SKU.

DWord	Bit	Description
0	31:16	**Mask Bits** Access: WO Mask: [15:0] Format: Mask Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15	**TDL3 Ack** Exists If: //SubSlice3
	14	**TDL2 Ack** Exists If: //SubSlice2
	13	**TDL1 Ack** Exists If: //SubSlice1
	12	**TDL0 Ack**

STATE_ACK_SLICE5 - State Ack Register Slice5

		Exists If: //SubSlice0
	11:10	**Reserved** Format: MBZ
	9	**DM2 Ack** Exists If: //SubSlice2
	8	**SC2 Ack** Exists If: //SubSlice2
	7	**DM1 Ack** Exists If: //SubSlice1
	6	**DM0 Ack** Exists If: //SubSlice0
	5	**SC1 Ack** Exists If: //SubSlice1
	4	**SC0 Ack** Exists If: //SubSlice0
	3	**WM Ack** Exists If: //CommonSlice
	2	**SVL Ack** Exists If: //CommonSlice
	1:0	**Reserved** Format: MBZ

State Ack Register Slice6

STATE_ACK_SLICE6 - State Ack Register Slice6

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	02570h-02573h
Name:	State Ack Register Slice6
ShortName:	STATE_ACK_SLICE6_RCSUNIT_BE
Address:	18570h-18573h
Name:	State Ack Register Slice6
ShortName:	STATE_ACK_SLICE6_POCSUNIT_BE

This register is used in HW to receive Acknowledges from State clients in Slice-6 for non-pipeline state. This register can be read on the MMIO for checking if an ACK is not received. This register should not be written by SW. Note that Slices, Half Slices and Sub Slices enabled on a platform are function of GT SKU.

DWord	Bit	Description
0	31:16	**Mask Bits** Access: WO Mask: [15:0] Format: Mask Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15	**TDL3 Ack** Exists If: //SubSlice3
	14	**TDL2 Ack** Exists If: //SubSlice2
	13	**TDL1 Ack** Exists If: //SubSlice1
	12	**TDL0 Ack**

STATE_ACK_SLICE6 - State Ack Register Slice6

	Exists If:	//SubSlice0
11	**DM3 Ack**	
	Exists If:	//SubSlice3
10	**SC3 Ack**	
	Exists If:	//SubSlice3
9	**DM2 Ack**	
	Exists If:	//SubSlice2
8	**SC2 Ack**	
	Exists If:	//SubSlice2
7	**DM1 Ack**	
	Exists If:	//SubSlice1
6	**DM0 Ack**	
	Exists If:	//SubSlice0
5	**SC1 Ack**	
	Exists If:	//SubSlice1
4	**SC0 Ack**	
	Exists If:	//SubSlice0
3	**WM Ack**	
	Exists If:	//CommonSlice
2	**SVL Ack**	
	Exists If:	//CommonSlice
1:0	**Reserved**	
	Format:	MBZ

State Ack Register Slice7

STATE_ACK_SLICE7 - State Ack Register Slice7

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	02574h-02577h
Name:	State Ack Register Slice7
ShortName:	STATE_ACK_SLICE7_RCSUNIT_BE
Address:	18574h-18577h
Name:	State Ack Register Slice7
ShortName:	STATE_ACK_SLICE7_POCSUNIT_BE

This register is used in HW to receive Acknowledges from State clients in Slice-7 for non-pipeline state. This register can be read on the MMIO for checking if an ACK is not received. This register should not be written by SW. Note that Slices, Half Slices and Sub Slices enabled on a platform are function of GT SKU.

DWord	Bit	Description
0	31:16	**Mask Bits** Access: WO Mask: [15:0] Format: Mask Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15	**TDL3 Ack** Exists If: //SubSlice3
	14	**TDL2 Ack** Exists If: //SubSlice2
	13	**TDL1 Ack** Exists If: //SubSlice1
	12	**TDL0 Ack**

STATE_ACK_SLICE7 - State Ack Register Slice7

		Exists If: //SubSlice0
11	**DM3 Ack**	Exists If: //SubSlice3
10	**SC3 Ack**	Exists If: //SubSlice3
9	**DM2 Ack**	Exists If: //SubSlice2
8	**SC2 Ack**	Exists If: //SubSlice2
7	**DM1 Ack**	Exists If: //SubSlice1
6	**DM0 Ack**	Exists If: //SubSlice0
5	**SC1 Ack**	Exists If: //SubSlice1
4	**SC0 Ack**	Exists If: //SubSlice0
3	**WM Ack**	Exists If: //CommonSlice
2	**SVL Ack**	Exists If: //CommonSlice
1:0	**Reserved**	Format: MBZ

Stream Output 0 Num Primitives Written Counter

SO0_NUM_PRIMS_WRITTEN - Stream Output 0 Num Primitives Written Counter

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Address:	05200h-05207h
Name:	Stream Output 0 Num Primitives Written Counter
ShortName:	SO0_NUM_PRIMS_WRITTEN

There is one 64-bit register for each of the 4 supported streams:

- 5200h-5207h SO_NUM_PRIMS_WRITTEN0 (for Stream Out Stream #0)
- 5208h-520Fh SO_NUM_PRIMS_WRITTEN1 (for Stream Out Stream #1)
- 5210h-5217h SO_NUM_PRIMS_WRITTEN2 (for Stream Out Stream #2)
- 5218h-521Fh SO_NUM_PRIMS_WRITTEN3 (for Stream Out Stream #3)

These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has successfully written to a particular "stream's" Streamed Vertex Output buffers, subject to buffer overflow detection. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.

DWord	Bit	Description
0	31:0	**Num Prims Written Count 0** Format: U32 This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)
1	31:0	**Num Prims Written Count 1** Format: U32 This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)

Stream Output 0 Primitive Storage Needed Counter

SO0_PRIM_STORAGE_NEEDED - Stream Output 0 Primitive Storage Needed Counter

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Address:	05240h-05247h
Name:	Stream Output 0 Primitive Storage Needed Counter
ShortName:	SO0_PRIM_STORAGE_NEEDED

There is one 64-bit register for each of the 4 supported streams:

- 5240h-5247h SO_PRIM_STORAGE_NEEDED0 (for Stream Out Stream #0)
- 5248h-524Fh SO_PRIM_STORAGE_NEEDED1 (for Stream Out Stream #1)
- 5250h-5257h SO_PRIM_STORAGE_NEEDED2 (for Stream Out Stream #2)
- 5258h-525Fh SO_PRIM_STORAGE_NEEDED3 (for Stream Out Stream #3)

These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has or would have written to a particular "stream's" Streamed Vertex Output buffers if all buffers had been large enough to accommodate the writes. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.

DWord	Bit	Description
0	31:0	**Prim Storage Needed Count 0** Format: U32 This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.
1	31:0	**Prim Storage Needed Count 1** Format: U32 This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.

Stream Output 0 Write Offset

SO0_WRITE_OFFSET - Stream Output 0 Write Offset

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	32
Address:	05280h-05283h
Name:	Stream Output 0 Write Offset
ShortName:	SO0_WRITE_OFFSET

There is one R/W 32-bit register for each of the 4 supported stream output buffer slots:
5280h-5283h SO_WRITE_OFFSET0 (for Stream Out Buffer #0)
5284h-5287h SO_WRITE_OFFSET1 (for Stream Out Buffer #1)
5288h-528Bh SO_WRITE_OFFSET2 (for Stream Out Buffer #2)
528Ch-528Fh SO_WRITE_OFFSET3 (for Stream Out Buffer #3)
These registers are used to set and track a DWord-granular Write Offset for each of the 4 Stream Output Buffer slots. Software can directly write them via MI_LOAD_REGxxx commands. The SOL stage will increment them as part of stream output processing. Software can cause them to be written to memory via MI_STORE_REGxxx commands. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.

Programming Notes

- Software must ensure that no HW stream output operations can be in process or otherwise pending at the point that the MI_LOAD/STORE commands are processed. This will likely require a pipeline flush.
- The SOL stage will effectively advance the write offset by the buffer's Surface Pitch after each vertex is written (assuming no overflow is detected in any targetted SO buffer). Under "normal" conditions one would expect software to initialize the WriteOffset to some (possibly zero) multiple of Surface Pitch in order to align vertex writes to the buffer's Base Address, though it is not required to do so.

DWord	Bit	Description
0	31:2	**Write Offset** Format: U30 This field contains a DWord offset from the corresponding SO buffer's Base Address value. The SOL stage uses this value as a write offset when performing writes to the buffer. The SOL stage will increment this value as a part of performing stream output to the buffer. Note that the SOL stage uses the buffer's Surface Pitch to advance the Write Offset, without regard to the buffer's Base Address (see Programming Notes above).

SO0_WRITE_OFFSET - Stream Output 0 Write Offset			
	1:0	**Reserved**	
		Format:	MBZ

Stream Output 1 Num Primitives Written Counter

SO1_NUM_PRIMS_WRITTEN - Stream Output 1 Num Primitives Written Counter

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Address:	05208h-0520Fh
Name:	Stream Output 1 Num Primitives Written Counter
ShortName:	SO1_NUM_PRIMS_WRITTEN

There is one 64-bit register for each of the 4 supported streams:
5200h-5207h SO_NUM_PRIMS_WRITTEN0 (for Stream Out Stream #0)
5208h-520Fh SO_NUM_PRIMS_WRITTEN1 (for Stream Out Stream #1)
5210h-5217h SO_NUM_PRIMS_WRITTEN2 (for Stream Out Stream #2)
5218h-521Fh SO_NUM_PRIMS_WRITTEN3 (for Stream Out Stream #3)
These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has successfully written to a particular "stream's" Streamed Vertex Output buffers, subject to buffer overflow detection. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.

DWord	Bit	Description
0	31:0	**Num Prims Written Count 0** Format: U32 This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)
1	31:0	**Num Prims Written Count 1** Format: U32 This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)

Stream Output 1 Primitive Storage Needed Counter

SO1_PRIM_STORAGE_NEEDED - Stream Output 1 Primitive Storage Needed Counter

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Address:	05248h-0524Fh
Name:	Stream Output 1 Primitive Storage Needed Counter
ShortName:	SO1_PRIM_STORAGE_NEEDED

There is one 64-bit register for each of the 4 supported streams:
5240h-5247h SO_PRIM_STORAGE_NEEDED0 (for Stream Out Stream #0)
5248h-524Fh SO_PRIM_STORAGE_NEEDED1 (for Stream Out Stream #1)
5250h-5257h SO_PRIM_STORAGE_NEEDED2 (for Stream Out Stream #2)
5258h-525Fh SO_PRIM_STORAGE_NEEDED3 (for Stream Out Stream #3)
These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has or would have written to a particular "stream's" Streamed Vertex Output buffers if all buffers had been large enough to accommodate the writes. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.

DWord	Bit	Description
0	31:0	**Prim Storage Needed Count 0** Format: U32 This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.
1	31:0	**Prim Storage Needed Count 1** Format: U32 This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.

Stream Output 1 Write Offset

SO1_WRITE_OFFSET - Stream Output 1 Write Offset

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	32
Address:	05284h-05287h
Name:	Stream Output 1 Write Offset
ShortName:	SO1_WRITE_OFFSET

There is one R/W 32-bit register for each of the 4 supported stream output buffer slots:
5280h-5283h SO_WRITE_OFFSET0 (for Stream Out Buffer #0)
5284h-5287h SO_WRITE_OFFSET1 (for Stream Out Buffer #1)
5288h-528Bh SO_WRITE_OFFSET2 (for Stream Out Buffer #2)
528Ch-528Fh SO_WRITE_OFFSET3 (for Stream Out Buffer #3)
These registers are used to set and track a DWord-granular Write Offset for each of the 4 Stream Output Buffer slots. Software can directly write them via MI_LOAD_REGxxx commands. The SOL stage will increment them as part of stream output processing. Software can cause them to be written to memory via MI_STORE_REGxxx commands. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.

Programming Notes

- Software must ensure that no HW stream output operations can be in process or otherwise pending at the point that the MI_LOAD/STORE commands are processed. This will likely require a pipeline flush.
- The SOL stage will effectively advance the write offset by the buffer's Surface Pitch after each vertex is written (assuming no overflow is detected in any targetted SO buffer). Under "normal" conditions one would expect software to initialize the WriteOffset to some (possibly zero) multiple of Surface Pitch in order to align vertex writes to the buffer's Base Address, though it is not required to do so.

DWord	Bit	Description
0	31:2	**Write Offset** Format: U30 This field contains a DWord offset from the corresponding SO buffer's Base Address value. The SOL stage uses this value as a write offset when performing writes to the buffer. The SOL stage will increment this value as a part of performing stream output to the buffer. Note that the SOL stage uses the buffer's Surface Pitch to advance the Write Offset, without regard to the buffer's Base Address (see Programming Notes above).

SO1_WRITE_OFFSET - Stream Output 1 Write Offset			
	1:0	**Reserved**	
		Format:	MBZ

Stream Output 2 Num Primitives Written Counter

SO2_NUM_PRIMS_WRITTEN - Stream Output 2 Num Primitives Written Counter

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Address:	05210h-05217h
Name:	Stream Output 2 Num Primitives Written Counter
ShortName:	SO2_NUM_PRIMS_WRITTEN

There is one 64-bit register for each of the 4 supported streams:
5200h-5207h SO_NUM_PRIMS_WRITTEN0 (for Stream Out Stream #0)
5208h-520Fh SO_NUM_PRIMS_WRITTEN1 (for Stream Out Stream #1)
5210h-5217h SO_NUM_PRIMS_WRITTEN2 (for Stream Out Stream #2)
5218h-521Fh SO_NUM_PRIMS_WRITTEN3 (for Stream Out Stream #3)
These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has successfully written to a particular "stream's" Streamed Vertex Output buffers, subject to buffer overflow detection. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.

DWord	Bit	Description
0	31:0	**Num Prims Written Count 0** Format: U32 This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)
1	31:0	**Num Prims Written Count 1** Format: U32 This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)

Stream Output 2 Primitive Storage Needed Counter

SO2_PRIM_STORAGE_NEEDED - Stream Output 2 Primitive Storage Needed Counter

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Address:	05250h-05257h
Name:	Stream Output 2 Primitive Storage Needed Counter
ShortName:	SO2_PRIM_STORAGE_NEEDED

There is one 64-bit register for each of the 4 supported streams:
5240h-5247h SO_PRIM_STORAGE_NEEDED0 (for Stream Out Stream #0)
5248h-524Fh SO_PRIM_STORAGE_NEEDED1 (for Stream Out Stream #1)
5250h-5257h SO_PRIM_STORAGE_NEEDED2 (for Stream Out Stream #2)
5258h-525Fh SO_PRIM_STORAGE_NEEDED3 (for Stream Out Stream #3)
These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has or would have written to a particular "stream's" Streamed Vertex Output buffers if all buffers had been large enough to accommodate the writes. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.

DWord	Bit	Description
0	31:0	**Prim Storage Needed Count 0** Format: U32 This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.
1	31:0	**Prim Storage Needed Count 1** Format: U32 This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.

Stream Output 2 Write Offset

SO2_WRITE_OFFSET - Stream Output 2 Write Offset

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	32
Address:	05288h-0528Bh
Name:	Stream Output 2 Write Offset
ShortName:	SO2_WRITE_OFFSET

There is one R/W 32-bit register for each of the 4 supported stream output buffer slots:
5280h-5283h SO_WRITE_OFFSET0 (for Stream Out Buffer #0)
5284h-5287h SO_WRITE_OFFSET1 (for Stream Out Buffer #1)
5288h-528Bh SO_WRITE_OFFSET2 (for Stream Out Buffer #2)
528Ch-528Fh SO_WRITE_OFFSET3 (for Stream Out Buffer #3)
These registers are used to set and track a DWord-granular Write Offset for each of the 4 Stream Output Buffer slots. Software can directly write them via MI_LOAD_REGxxx commands. The SOL stage will increment them as part of stream output processing. Software can cause them to be written to memory via MI_STORE_REGxxx commands. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.

Programming Notes

- Software must ensure that no HW stream output operations can be in process or otherwise pending at the point that the MI_LOAD/STORE commands are processed. This will likely require a pipeline flush.
- The SOL stage will effectively advance the write offset by the buffer's Surface Pitch after each vertex is written (assuming no overflow is detected in any targeted SO buffer). Under "normal" conditions one would expect software to initialize the WriteOffset to some (possibly zero) multiple of Surface Pitch in order to align vertex writes to the buffer's Base Address, though it is not required to do so.

DWord	Bit	Description
0	31:2	**Write Offset** Format: U30 This field contains a DWord offset from the corresponding SO buffer's Base Address value. The SOL stage uses this value as a write offset when performing writes to the buffer. The SOL stage will increment this value as a part of performing stream output to the buffer. Note that the SOL stage uses the buffer's Surface Pitch to advance the Write Offset, without regard to the buffer's Base Address (see Programming Notes above).

SO2_WRITE_OFFSET - Stream Output 2 Write Offset			
	1:0	**Reserved**	
		Format:	MBZ

Stream Output 3 Num Primitives Written Counter

SO3_NUM_PRIMS_WRITTEN - Stream Output 3 Num Primitives Written Counter

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Address:	05218h-0521Fh
Name:	Stream Output 3 Num Primitives Written Counter
ShortName:	SO3_NUM_PRIMS_WRITTEN

There is one 64-bit register for each of the 4 supported streams:
5200h-5207h SO_NUM_PRIMS_WRITTEN0 (for Stream Out Stream #0)
5208h-520Fh SO_NUM_PRIMS_WRITTEN1 (for Stream Out Stream #1)
5210h-5217h SO_NUM_PRIMS_WRITTEN2 (for Stream Out Stream #2)
5218h-521Fh SO_NUM_PRIMS_WRITTEN3 (for Stream Out Stream #3)
These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has successfully written to a particular "stream's" Streamed Vertex Output buffers, subject to buffer overflow detection. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.

DWord	Bit	Description
0	31:0	**Num Prims Written Count 0** Format: U32 This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)
1	31:0	**Num Prims Written Count 1** Format: U32 This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)

Stream Output 3 Primitive Storage Needed Counter

SO3_PRIM_STORAGE_NEEDED - Stream Output 3 Primitive Storage Needed Counter

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Address:	05258h-0525Fh
Name:	Stream Output 3 Primitive Storage Needed Counter
ShortName:	SO3_PRIM_STORAGE_NEEDED

There is one 64-bit register for each of the 4 supported streams:
5240h-5247h SO_PRIM_STORAGE_NEEDED0 (for Stream Out Stream #0)
5248h-524Fh SO_PRIM_STORAGE_NEEDED1 (for Stream Out Stream #1)
5250h-5257h SO_PRIM_STORAGE_NEEDED2 (for Stream Out Stream #2)
5258h-525Fh SO_PRIM_STORAGE_NEEDED3 (for Stream Out Stream #3)
These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has or would have written to a particular "stream's" Streamed Vertex Output buffers if all buffers had been large enough to accommodate the writes. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.

DWord	Bit	Description
0	31:0	**Prim Storage Needed Count 0** Format: U32 This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.
1	31:0	**Prim Storage Needed Count 1** Format: U32 This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.

Stream Output 3 Write Offset

SO3_WRITE_OFFSET - Stream Output 3 Write Offset

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	32
Address:	0528Ch-0528Fh
Name:	Stream Output 3 Write Offset
ShortName:	SO3_WRITE_OFFSET

There is one R/W 32-bit register for each of the 4 supported stream output buffer slots:
5280h-5283h SO_WRITE_OFFSET0 (for Stream Out Buffer #0)
5284h-5287h SO_WRITE_OFFSET1 (for Stream Out Buffer #1)
5288h-528Bh SO_WRITE_OFFSET2 (for Stream Out Buffer #2)
528Ch-528Fh SO_WRITE_OFFSET3 (for Stream Out Buffer #3)
These registers are used to set and track a DWord-granular Write Offset for each of the 4 Stream Output Buffer slots. Software can directly write them via MI_LOAD_REGxxx commands. The SOL stage will increment them as part of stream output processing. Software can cause them to be written to memory via MI_STORE_REGxxx commands. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.

Programming Notes

- Software must ensure that no HW stream output operations can be in process or otherwise pending at the point that the MI_LOAD/STORE commands are processed. This will likely require a pipeline flush.
- The SOL stage will effectively advance the write offset by the buffer's Surface Pitch after each vertex is written (assuming no overflow is detected in any targetted SO buffer). Under "normal" conditions one would expect software to initialize the WriteOffset to some (possibly zero) multiple of Surface Pitch in order to align vertex writes to the buffer's Base Address, though it is not required to do so.

DWord	Bit	Description
0	31:2	**Write Offset** Format: U30 This field contains a DWord offset from the corresponding SO buffer's Base Address value. The SOL stage uses this value as a write offset when performing writes to the buffer. The SOL stage will increment this value as a part of performing stream output to the buffer. Note that the SOL stage uses the buffer's Surface Pitch to advance the Write Offset, without regard to the buffer's Base Address (see Programming Notes above).

SO3_WRITE_OFFSET - Stream Output 3 Write Offset			
	1:0	**Reserved**	
		Format:	MBZ

SubSlice 0 Power Context Save request

SSM0PGCTXREQ - SubSlice 0 Power Context Save request

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	24404h

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO Message Mask bots for lower 16 bits
	15:10	**Reserved** Access: RO Reserved
	9	**Power context save request** Access: R/W Set Power Context Save Request 1'b0 : Power context save is not being requested 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

SubSlice0 Power Down FSM control register with lock

SSM0SPCPOWERDNFSMCTL - SubSlice0 Power Down FSM control register with lock

Register Space: MMIO: 0/2/0

Source: BSpec

Size (in bits): 32

Address: 24410h

DWord	Bit	Description
0	31	**power down control Lock** Access: R/W Lock 0 = Bits of POWERDNFSMCTL register are R/W 1 = All bits of POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:13	**Reserved** Access: RO Reserved
	12	**Leave firewall disabled** Access: R/W Lock When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e dont firewall the gated domain, but complete logical flow
	11	**Leave reset de-asserted** Access: R/W Lock When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e dont assert reset, but complete logical flow
	10	**Leave CLKs ON** Access: R/W Lock

SSM0SPCPOWERDNFSMCTL - SubSlice0 Power Down FSM control register with lock

		When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e dont clock gate, but complete logical flow
	9	**Leave FET On** Access: R/W Lock When This bit is set SPC will not turn off the PFET eventhough it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e dont power off pfet, but complete logical flow
	8:6	**Power Down state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Gate Clocks
	5:3	**Power Down state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default :Firewall ON
	2:0	**Power Down state 1** Default Value: 000b Access: R/W Lock This will be the 1st state before power is turned OFF in the well Encodings: 000 = Assert Reset

SSM0SPCPOWERDNFSMCTL - SubSlice0 Power Down FSM control register with lock		
		001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Assert Reset

SubSlice 0 Power Gate Control Request

SSM0PGCTLREQ - SubSlice 0 Power Gate Control Request

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	24400h

Clock Gating Messages Register

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:2	**Reserved** Access: RO Reserved
	1	**CLK RST FWE Request** Access: R/W SLICE 0 CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**Power Gate Request** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

SubSlice 0 Power on FSM control register with lock

SSM0SPCPOWERUPFSMCTL - SubSlice 0 Power on FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	2440Ch

DWord	Bit	Description
0	31	**power up control Lock** Access: R/W Lock 0 = Bits of POWERUPFSMCTL register are R/W 1 = All bits of POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:9	**Reserved** Access: RO Reserved
	8:6	**Power UP state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - De-assert resets 3'b000: 10ns (or 1 bclk)
	5:3	**Power UP state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF

		010 = De-assert resets 1xx = Rsvd for future Default - Firewall OFF
	2:0	**Power UP state 1** Default Value: 000b Access: R/W Lock This will be the 1st state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Clock Ungate

SubSlice 1 Power Context Save request

SSM1PGCTXREQ - SubSlice 1 Power Context Save request		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	24484h	
DWord	**Bit**	**Description**
0	31:16	**Message Mask** Access: RO Message Mask bots for lower 16 bits
	15:10	**Reserved** Access: RO Reserved
	9	**Power context save request** Access: R/W Set Power Context Save Request 1'b0 : Power context save is not being requested 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

SubSlice 1 Power Down FSM control register with lock

SSM1SPCPOWERDNFSMCTL - SubSlice 1 Power Down FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	24490h

DWord	Bit	Description
0	31	**power down control Lock** Access: R/W Lock 0 = Bits of POWERDNFSMCTL register are R/W 1 = All bits of POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:13	**Reserved** Access: RO Reserved
	12	**Leave firewall disabled** Access: R/W Lock When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e dont firewall the gated domain, but complete logical flow
	11	**Leave reset de-asserted** Access: R/W Lock When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e dont assert reset, but complete logical flow
	10	**Leave CLKs ON** Access: R/W Lock

SSM1SPCPOWERDNFSMCTL - SubSlice 1 Power Down FSM control register with lock

		When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e dont clock gate, but complete logical flow
	9	**Leave FET On** Access: R/W Lock When This bit is set SPC will not turn off the PFET eventhough it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e dont power off pfet, but complete logical flow
	8:6	**Power Down state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Gate Clocks
	5:3	**Power Down state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default :Firewall ON
	2:0	**Power Down state 1** Default Value: 000b Access: R/W Lock This will be the 1st state before power is turned OFF in the well Encodings: 000 = Assert Reset

SSM1SPCPOWERDNFSMCTL - SubSlice 1 Power Down FSM control register with lock		
		001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Assert Reset

SubSlice 1 Power Gate Control Request

SSM1PGCTLREQ - SubSlice 1 Power Gate Control Request

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	24480h

Clock Gating Messages Register

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:2	**Reserved** Access: RO Reserved
	1	**CLK RST FWE Request** Access: R/W SLICE 0 CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**Power Gate Request** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

SubSlice 1 Power on FSM control register with lock

SSM1SPCPOWERUPFSMCTL - SubSlice 1 Power on FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	2448Ch

DWord	Bit	Description
0	31	**power up control Lock** Access: R/W Lock 0 = Bits of POWERUPFSMCTL register are R/W 1 = All bits of POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:9	**Reserved** Access: RO Reserved
	8:6	**Power UP state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - De-assert resets 3'b000: 10ns (or 1 bclk)
	5:3	**Power UP state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF

SSM1SPCPOWERUPFSMCTL - SubSlice 1 Power on FSM control register with lock

		010 = De-assert resets 1xx = Rsvd for future Default - Firewall OFF
	2:0	**Power UP state 1** Default Value: 000b Access: R/W Lock This will be the 1st state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Clock Ungate

SubSlice 2 Power Context Save request

SSM2PGCTXREQ - SubSlice 2 Power Context Save request		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	24504h	
DWord	**Bit**	**Description**
0	31:16	**Message Mask** Access: RO Message Mask bots for lower 16 bits
	15:10	**Reserved** Access: RO Reserved
	9	**Power context save request** Access: R/W Set Power Context Save Request 1'b0 : Power context save is not being requested 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

SubSlice 2 Power Down FSM control register with lock

SSM2SPCPOWERDNFSMCTL - SubSlice 2 Power Down FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	24510h

DWord	Bit	Description
0	31	**power down control Lock** Access: R/W Lock 0 = Bits of POWERDNFSMCTL register are R/W 1 = All bits of POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:13	**Reserved** Access: RO Reserved
	12	**Leave firewall disabled** Access: R/W Lock When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e dont firewall the gated domain, but complete logical flow
	11	**Leave reset de-asserted** Access: R/W Lock When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e dont assert reset, but complete logical flow
	10	**Leave CLKs ON** Access: R/W Lock

SSM2SPCPOWERDNFSMCTL - SubSlice 2 Power Down FSM control register with lock

		When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e dont clock gate, but complete logical flow
	9	**Leave FET On** Access: R/W Lock When This bit is set SPC will not turn off the PFET eventhough it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e dont power off pfet, but complete logical flow
	8:6	**Power Down state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Gate Clocks
	5:3	**Power Down state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default :Firewall ON
	2:0	**Power Down state 1** Default Value: 000b Access: R/W Lock This will be the 1st state before power is turned OFF in the well Encodings: 000 = Assert Reset

SSM2SPCPOWERDNFSMCTL - SubSlice 2 Power Down FSM control register with lock		
		001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Assert Reset

SubSlice 2 Power Gate Control Request

SSM2PGCTLREQ - SubSlice 2 Power Gate Control Request

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	24500h

Clock Gating Messages Register

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:2	**Reserved** Access: RO Reserved
	1	**CLK RST FWE Request** Access: R/W SLICE 0 CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**Power Gate Request** Access: R/W SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

SubSlice 2 Power on FSM control register with lock

SSM2SPCPOWERUPFSMCTL - SubSlice 2 Power on FSM control register with lock

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	2450Ch

DWord	Bit	Description
0	31	**power up control Lock** Access: R/W Lock 0 = Bits of POWERUPFSMCTL register are R/W 1 = All bits of POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:9	**Reserved** Access: RO Reserved
	8:6	**Power UP state 3** Default Value: 010b Access: R/W Lock This will be the 3rd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - De-assert resets 3'b000: 10ns (or 1 bclk)
	5:3	**Power UP state 2** Default Value: 001b Access: R/W Lock This will be the 2nd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF

		010 = De-assert resets 1xx = Rsvd for future Default - Firewall OFF
	2:0	**Power UP state 1** Default Value: 000b Access: R/W Lock This will be the 1st state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Clock Ungate

Super Queue GFX cycle Options register

SQCFG - Super Queue GFX cycle Options register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0902Ch

Super Queue GFX Cycle Options register

DWord	Bit	Description
0	31	**SQCFG Lock bit** Access: R/W Lock
	30:14	**Reserved** Access: RO
	13:12	**SQ Bypass Timeout** Access: R/W Lock
	11:10	**Reserved** Access: RO
	9:3	**SQ Full Limit for Performance Monitor** Default Value: 0110000b Access: R/W Lock Watermark for SQ Bank Full Metrics This field sets a watermark where any SQ Bank level above is considered as SQ FULL condition. This is added to compensate for the credit loop between the page walker and GTI which would make the number of active entries oscillate even the pipeline is backed up towards page walker. Power-on default is 48d=0x30. Software Programming Note: LP: Range of allowed programming is 0-80d, but SW should set value to 72d=0x48. HP: Range of allowed programming is 0-56d, but SW should set value to 48d=0x30.
	2	**SQ Read-Only Port Reject Disable** Access: R/W This indicates whether rejections can be issued from the Super Queue to GFX for read cycles on the Read Only port. Rejected cycles are retried at a later time by GFX. By default, read cycles that have a matching address elsewhere in the Super Queue are rejected, and GFX is notified of the rejection.

SQCFG - Super Queue GFX cycle Options register

		If this bit is set, no rejections ever occur on the SQ-GFX interface. SQ accepts all requests, but in the case of a matching address, the SQ stalls the Read-Only port until the address match disappears (matching entry is retired by SQ). 1 = Rejections are disabled, SQ stalls if needed. 0 = Rejections are enabled.
	1	**SQ Read Port GFX Read Ownership** Access: R/W SQ Read Port GFX Read Ownership (SQRWO): SQ Read-Only Port GFX Read Ownership Indication. This indicates the type of request that is issued to uncore for each read cycle from the GFX Read-Only port which produces a miss in the MLC. By default, read cycles that have no matching MLC entry produce a regular read request from uncore through the IDI. If this bit is set, the request is changed from a regular read to a request for ownership (RFO) of the cacheline. This applies for all read requests from the GFX Read-Only port ONLY. 1 = All GFX reads from RO port require ownership of the cacheline. 0 = GFX reads from RO port do.
	0	**MSQD Poisoned Writes Propagation Enable** Access: R/W Lock

Super Queue Internal Cnt Register I

SQCNT1 - Super Queue Internal Cnt Register I

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	09024h

SQ Internal Counter Register

DWord	Bit	Description
0	31:30	**Reserved** Access: RO
	29:28	**SQ Performance Merge IDI.** Access: R/W
	27:26	**SQ Perormance Merge Bank Pairs.** Access: R/W
	25:24	**SQ Performance Merge Banks.** Access: R/W
	23:20	**SQRWCQD** Access: R/W Read-Write Request Queue Command Get Delay: This indicates the number of clocks that are inserted between each GFX cycle being accepted on the GFX Read or GFX Write ports. By default, this is disabled, which means that the RWRQ is able to accept one cycle per clock. By any other value, the RWRQ inserts the number of idle clocks listed in this register before accepting another cycle from GFX, essentially throttling the bandwidth. During each idle clock, RWRQ is guaranteed not to assert its command get to either read or write port. 0000b = Disabled (no additional clocks added). 0001b = One idle clock inserted between command gets. 0010b = Two idle clocks inserted between command gets. ... 1111b = Fifteen idle clocks inserted between command gets.
	19:16	**SQCQD** Access: R/W

SQCNT1 - Super Queue Internal Cnt Register I

		Read-Only Request Queue Command Get Delay: This indicates the number of clocks that are inserted between each GFX cycle being accepted on the GFX Read-Only port. By default, this is disabled, which means that the RORQ will be able to accept one cycle per clock. By any other value, the RORQ inserts the number of idle clocks listed in this register before accepting another cycle from GFX, essentially throttling the bandwidth. During each idle clock, RORQ is guaranteed not to assert its command get. 0000b = Disabled (no additional clocks added). 0001b = One idle clock inserted between command gets. 0010b = Two idle clocks inserted between command gets. ... 1111b = Fifteen idle clocks inserted between command gets.
	15:9	**SQDPTH** Access: R/W Super Queue Depth: 7Fh = SQ Depth of 127. 7Eh = SQ Depth of 126. ... 40h = SQ Depth of 64. 3Fh = SQ Depth of 63. 3Eh = SQ Depth of 62. ... 07h = SQ Depth of 7. 06h = SQ Depth of 6. 05h = SQ Depth of 5. 04h = SQ Depth of 4. 03h = SQ Depth of 3. 02h = SQ Depth of 2. 01h = Reserved. 00h = Disabled (SQ Depth of MAX) (default). For SQ implementations with multiple SQ banks, this field controls the depth per bank, and the total SQ depth is SQDPTH * number of SQ banks. For the sizes that are larger than the physical SQ size, the depth limitation is treated as disabled and SQ Depth will be the maximum supported. if SQDPTH > SQ Depth should be treated as MAX that h/w is capable of.
	8	**Reserved** Access: RO
	7	**Reserved**
	6:0	**SQIDICNT** Access: R/W Outstanding SQ IDI Cycle Counter: This indicates the maximum number of outstanding cycles that are presented to IDI/uncore at any given time by Super Queue. By default, this is 64, but can be throttled back to support fewer

SQCNT1 - Super Queue Internal Cnt Register I		
		IDI cycles. 0 = Disabled (64). 1-63 = Max number of outstanding IDI cycles.

Super Queue Internal Counters Register II

SQCNT2 - Super Queue Internal Counters Register II

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	09028h

Super Queue Internal Counter register

DWord	Bit	Description
0	31	**Lock Bit** Access: R/W Lock
	30	**Reserved** Access: RO
	29	**Enable Promotion on Read** Access: R/W Lock
	28	**Priority 3 Pool Count Disable** Access: R/W Lock
	27:25	**Priority3 Pool Count:** Access: R/W Lock
	24	**Priority2 Pool Count Disable** Access: R/W Lock
	23:21	**Priority2 Pool count** Access: R/W Lock
	20	**Priority1 Pool Count Disable** Access: R/W Lock
	19:17	**Priority1 Pool Count** Access: R/W Lock

SQCNT2 - Super Queue Internal Counters Register II

16	**Priority0 Pool Count Disable**	
	Access:	R/W Lock
15:13	**Priority0 Pool Count**	
	Access:	R/W Lock
12	**Enable Priority Selection**	
	Default Value:	0 Disabled
	Access:	R/W Lock
	As part of bug 1405152537, this bit must be set to zero. That generally means that bits 28:13 become a don't care. Since this change will not force MBC unit to change, the only modification is to show that this bit must be zero. Definition shows that bit must be zero, but realistically, logic is eliminated.	
11:8	**Reserved**	
7:0	**LRU Hint counter**	
	Access:	RO
	Reserved	

Thread Dispatched Count Register

TDL_THR_DISP_COUNT - Thread Dispatched Count Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	0E4BCh

This register provides the count of threads dispatched/valid in the subslice.

DWord	Bit	Description
0	31:6	**Reserved** Format: MBZ
	5:0	**Thread Count** Value: 0-56 — Name: Valid Range

Thread Faulted Count Register

TDL_THR_PF_COUNT - Thread Faulted Count Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	0E5BCh

This register provides the count of threads faulted in each subslice.

DWord	Bit	Description
0	31	**Canonical fault indication bit to CS** The bit is set when a canonical fault on data fetch is reported by EU.
	30:6	**Reserved** Format: MBZ
	5:0	**Thread Count** Value: 0-56 — Name: Valid Range

Thread Fault Status Register 0

TDL_THR_PF_STATUS0 - Thread Fault Status Register 0	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	0E6B8h

This register provides the status of each thread in the SubSlice. A bit set indicates the thread in the specific thread slot is faulted.

DWord	Bit	Description
0	31:24	**Row0, EU3, [Reserved, T6-T0]**
	23:16	**Row0, EU2, [Reserved, T6-T0]**
	15:8	**Row0, EU1, [Reserved, T6-T0]**
	7:0	**Row0, EU0, [Reserved, T6-T0]**

Thread Fault Status Register 1

TDL_THR_PF_STATUS1 - Thread Fault Status Register 1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	0E7B8h

This register provides the status of each thread in the SubSlice. A bit set indicates the thread in the specific thread slot is faulted.

DWord	Bit	Description
0	31:24	**Row1, EU3, [Reserved, T6-T0]**
	23:16	**Row1, EU2, [Reserved, T6-T0]**
	15:8	**Row1, EU1, [Reserved, T6-T0]**
	7:0	**Row1, EU0, [Reserved, T6-T0]**

Thread Load Status Register 0

TDL_THR_STATUS0 - Thread Load Status Register 0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Access:	RO	
Size (in bits):	32	
Address:	0E4B8h	
This register provides the status of each thread in the SubSlice.		
DWord	**Bit**	**Description**
0	31:24	**Row0, EU3, [Reserved, T6-T0]**
	23:16	**Row0, EU2, [Reserved, T6-T0]**
	15:8	**Row0, EU1, [Reserved, T6-T0]**
	7:0	**Row0, EU0, [Reserved, T6-T0]**

Thread Load Status Register 1

TDL_THR_STATUS1 - Thread Load Status Register 1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	0E5B8h

This register provides the status of each thread in the SubSlice. A bit set indicates a valid thread is loaded in the thread slot.

DWord	Bit	Description
0	31:24	**Row1, EU3, [Reserved, T6-T0]**
	23:16	**Row1, EU2, [Reserved, T6-T0]**
	15:8	**Row1, EU1, [Reserved, T6-T0]**
	7:0	**Row1, EU0, [Reserved, T6-T0]**

Thread Mode Register

FF_MODE - Thread Mode Register

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	32
Address:	020A0h-020A3h
Name:	Thread Mode Register
ShortName:	FF_MODE_RCSUNIT_BE
Address:	180A0h-180A3h
Name:	Thread Mode Register
ShortName:	FF_MODE_POCSUNIT_BE

This register is used to program the FF shader Mode.

DWord	Bit	Description
0	31	**TE Autostrip Disable** Format: U1 0h Enable **[Default]** — TE will generate "autostrip" primitives (if/where possible) during tessellation. 1h Disable — TE will not generate "autostrip" primitives.
	30	**TDS external Cache Disable** 0b Enable **[Default]** — The external TDS Cache is enabled if there is enough handles to enable the cache. 1b Disable — The external TDS Cache is disabled even if there is enough handles to enable the cache. Only the internal TDS Cache will be used.
	29:26	**DS Hit Max Value** Format: U4

FF_MODE - Thread Mode Register

Description
If the number of hits reaches the DS Hit Max Value and there is a pending miss to be dispatched, the DS will dispatch the pending miss vertex as a single dispatch.
Programming a value of 0 will disable the DS Hit Max counter logic and therefore partial dispatches will not be forced due to the number of hits seen during the accumulation of inputs for a thread dispatch.

Value	Name
15	**[Default]**
[0,15]	

25:20 **VS Hit Max Value**

Format:	U6

Description
If the number of hits reaches the VS Hit Max Value and there is a pending miss to be dispatched, the VS will dispatch the pending miss vertex as a single dispatch.
Since VS Reference Count Full Force miss enable was removed, the value can be [1,63].

Value	Name
10	**[Default]**
[1,63]	

19 **Tessellation DOP gating Disable**

Format:	Disable

Value	Name	Description
0h	Enable **[Default]**	HS, TE, TETG, DS, GS and SOL units are DOP gated if all units are disabled
1h	Disable	DOP gating is disabled for HS, TE, TETG, DS, GS and SOL units

Programming Notes
Once this bit is set to a 1, it must not be cleared to a 0 until after a reset.

18 **TRI NOINSIDE Autostrip Cache Invalidate Disable**

Format:	Disable

This bit can be used to control the TRI NOINSIDE Autostrip Cache Invalidate feature. By default the invalidation is ENABLED (allowing higher performance).

Value	Name	Description

FF_MODE - Thread Mode Register

0h	Enable **[Default]**	TE will suppress the Autostrip cache invalidate for TRI NOINSIDE patches. This setting may improve performance.
1h	Disable	TE will not suppress the Autostrip cache invalidate for TRI NOINSIDE patches.

Programming Notes

The setting of this field impacts the selection of the "provoking vertex" for the center triangle of TRI domains (if a center triangle exists given the tessellation factors), and this will in turn impact the generated image if any PS attributes are enabled as "flat shaded" and that/those attributes are not identical on all 3 vertices of the triangle. Given the fact that the APIs do not impose requirements on the starting/provoking vertices of the tessellation-generated triangles, the selection of provoking vertices can be arbitrary as long as it is deterministic (i.e., repeated rendering the same patch will yield the same results).
Note: If FF_mode. TE autostrip Disable is set to 1, then TRI NOINSIDE Autostrip Cache Invalidate will also be disabled.

17 **VS DOP Clock gate fix disable**

Value	Name	Description
1h		The VS DOP clock gate fix is disabled. The DOP will not be held until the clocks are sampled off.
0h	**[Default]**	The VS DOP clock gate fix is enabled. The DOP enable will be held asserted until the clocks are sampled off.

16 **Reserved**

Format:	MBZ

15 **TDS Bypass Disable**

Format:	Disable

Value	Name	Description
0h	Enable **[Default]**	Domain Shader logic is bypassed while TDS is disabled
1h	Disable	Domain Shader bypass logic is disabled

14:13 **Reserved**

Format:	PBC

12 **Reserved**

Default Value:	0h
Format:	PBC

FF_MODE - Thread Mode Register

	11:7	**Reserved** Format: PBC
	6:5	**Reserved** Format: PBC
	4	**Reserved** Default Value: 0h Format: PBC
	3	**Reserved** Format: PBC
	2	**TDS Tracking fifo wrap fix disable** Format: Disable

Value	Name	Description
1h		Disable the tds tracking fifo wrap fix.
0h	**[Default]**	Enable the tds tracking fifo wrap fix.

	1	**HS handle ram fix disable**

Value	Name	Description
1h		Disable the HSunit handle ram over flow fix and allow vertices to run at 2 vertex per clock at the inlet of HS.
0h	**[Default]**	Enable the HSunit handle ram over flow fix and allow vertices to run at 1 vertex per clock at the inlet of HS.

	0	**Reserved** Format: PBC

Thread Restart Control Register

TDL_THR_RESTART - Thread Restart Control Register		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Access:	WO	
Size (in bits):	32	
Address:	0E450h	
This register provides control to restart page faulted and halted threads in each subslice.		
DWord	**Bit**	**Description**
0	31:1	**Reserved** Format: MBZ
	0	**Restart All Faulted Threads** A write of 1 to this register restarts all threads that have halted due to page fault.

Tile Cache Control Register

TCCNTLREG - Tile Cache Control Register

Register Space: MMIO: 0/2/0

Source: BSpec

Size (in bits): 32

Address: 0B0A4h

<table>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td>0</td><td>31:25</td><td>Unified Tile Cache Pool
<table>
<tr><td></td><td></td></tr>
<tr><td>Access:</td><td>R/W</td></tr>
</table>
Number of ways allocated for the unified client pool. This is a combined pool for all streams.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th><th>Programming Notes</th></tr>
<tr><td>00h</td><td>[Default]</td><td>Increments of 4KB per bank</td><td>When this field is non-zero, Z tile cache pool and C tile cache pool should be 0KB.</td></tr>
</table></td></tr>
<tr><td></td><td>24:18</td><td>Z Tile Cache Pool
<table>
<tr><td></td><td></td></tr>
<tr><td>Access:</td><td>R/W</td></tr>
</table>
Number of ways allocated for Z streams.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th><th>Programming Notes</th></tr>
<tr><td>00h</td><td>[Default]</td><td>Increments of 4KB per bank</td><td>Note: This field must be 0KB if Unified Tile cache Pool is non-zero.</td></tr>
</table></td></tr>
<tr><td></td><td>17:11</td><td>C Tile Cache Pool
<table>
<tr><td></td><td></td></tr>
<tr><td>Access:</td><td>R/W</td></tr>
</table>
Number of ways allocated for Color Streams
<table>
<tr><th>Value</th><th>Name</th><th>Description</th><th>Programming Notes</th></tr>
<tr><td>00h</td><td>[Default]</td><td>Increments of 4KB per bank</td><td>Note: This field must be 0KB if Unified Tile cache Pool is non-zero.</td></tr>
</table></td></tr>
<tr><td></td><td>10:4</td><td>Command Streamer Allocation
<table>
<tr><td></td><td></td></tr>
<tr><td>Access:</td><td>R/W</td></tr>
</table>
Number of ways allocated for CS(Command Streamer)
<table>
<tr><th>Value</th><th>Name</th><th>Description</th></tr>
<tr><td>00h</td><td>[Default]</td><td>Increments of 4KB per bank</td></tr>
</table></td></tr>
<tr><td></td><td>3</td><td>Tile cache path Disable</td></tr>
</table>

TCCNTLREG - Tile Cache Control Register

	Access:	R/W

Color and Z Caching Disable bit
When caching is disabled, All Z and color requests follow the legacy path to GAM rather than L2 Tile Cache is disabled with default value of this register bit (L3 operate in legacy mode). This register bit value needs to be changed to "0" for caching the C and Z streams in the L3 and forPTBR mode of operation with tile cache.

Value	Name
[0,1]	
0h	**[Default]**

2	**L3 Data partial write merging enable**	
	Default Value:	1
1	**Color/Z write partial write merging enable**	
	Default Value:	0

Disable partial write merging optimization for Color and Z clients. Partial write merging optimization (in SQDB) will be enabled when this bit is set.

0	**URB partial write merging enable**	
	Default Value:	1

TILECTL

TILECTL - TILECTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	101000h

Tile control and TLB control.

DWord	Bit	Description
0	31:3	**Reserved** Default Value: 00000000h Access: RO Reserved
	2	**Reserved** Default Value: 0b Access: RO Reserved.
	1	**TLBPF** Default Value: 0b Access: R/W Store multiple PTE enable. 0: Only one Page Table Entry is stored in the Translation Lookaside Buffer cache. 1: Multiple Page Table Entries (8) are stored in the Translation Lookaside Buffer cache.
	0	**SWZCTL** Default Value: 0b Access: R/W In order to spread DRAM accesses between multiple channels in the most efficient way, address bits can be used as a channel select. The Driver needs to obtain the need for memory address swizzling via DRAM configuration registers and set the following bits. x0b - No Address Swizzling x1b - Address bit [6] needs to be swizzled for tiled surfaces

TiledResources VA Detection Registers

TRVADR - TiledResources VA Detection Registers

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	04DF0h
Name:	TiledResources VA Detection Registers
ShortName:	TRVADR

DWord	Bit	Description
0	31:8	**Reserved** Default Value: 000000h Access: RO
	7:4	**TR - VA Mask Value** Default Value: 0000b Access: R/W 4bit MASK value that is mapped to incoming address bits[47:44] MASK bits are used to identify which address bits need to be considered for compare. If particular mask bit is "1", mapping address bit needs to be compared to DATA value provided. If "0", corresponding address bit is masked which makes it don't care for compare. (This field defaults to "0000" to disable detection.). Note: The only usage model for GFX driver to set this field to "1111". Behavior of h/w for any other setting is not defined. Note: GFX driver shall use same TRVA MASK value for all contexts.
	3:0	**TR- VA Data Value** Access: R/W Value / Name / Description: 0000b **[Default]** 4bit Data value that is mapped to incoming address bits[47:44]. Data bits are used to compare address values that are not filtered by the TRVAMV for match Note: GFX driver shall use same TRVA Data value for all contexts

Tiled Resources VA Translation Table L3 ptr - DW0

TRVATTL3PTRDW0 - Tiled Resources VA Translation Table L3 ptr - DW0

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	04DE0h
Name:	Tiled Resources VA Translation Table L3 ptr - DW0
ShortName:	TRVATTL3PTRDW0

DWord	Bit	Description
0	31:12	**TR - VA transln Table L3 Pointer (Lower Address)** Access: R/W Value / Name / Description: 00000h / **[Default]** / Lower address bits for tiled resource VA to virtual address translation L3 table
	11:0	**Reserved** Default Value: 000h Access: RO Reserved

Tiled Resources VA Translation Table L3 ptr - DW1

TRVATTL3PTRDW1 - Tiled Resources VA Translation Table L3 ptr - DW1

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	04DE4h
Name:	Tiled Resources VA Translation Table L3 ptr - DW1
ShortName:	TRVATTL3PTRDW1

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Value / Name / Description 0000h / **[Default]** / Reserved
	15:0	**TR - VA transln Table L3 Pointer (Upper Address)** Default Value: 0000h Access: R/W Upper address bits for tiled resource VA to virtual address translation L3 table

Tiled Resources Wrapper Write Data Port arbitration

TRWRPARB - Tiled Resources Wrapper Write Data Port arbitration

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	04DF8h
Name:	Tiled Resources Wrapper Write Data Port arbitration
ShortName:	TRWRPARB

DWord	Bit	Description
0	31:13	**Reserved** Default Value: 00000000000000000b Access: R/W Reserved
	12:10	**L3 Max Write Request Limit Count** Default Value: 100b Access: R/W This is the MAX number of Allowed writes from L3 before switching the priority to Z Requests Count - Minimum count value must be 1
	9	**Reserved** Default Value: 0b Access: R/W Reserved
	8:6	**Z Max Write Request Limit Count** Default Value: 010b Access: R/W This is the MAX number of Allowed writes from Z before switching the priority to C Requests Count - Minimum count value must be = 1
	5	**Reserved** Default Value: 0b Access: R/W
	4:2	**C Max Write Request Limit Count** Default Value: 010b

TRWRPARB - Tiled Resources Wrapper Write Data Port arbitration

		Access: R/W This is the MAX number of Allowed writes from C before switching to L3 Request Count - Minimum count value = 1
	1	**Reserved** Default Value: 0b Access: R/W
	0	**Fixed Arbitration enable** Default Value: 1b Access: R/W Fixed Arbitration enable when 1'b1 Programmable arbitration when 1'b0

TIMESTAMP_CTR

TIMESTAMP_CTR	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/WC
Size (in bits):	32
Address:	44070h-44073h
Name:	Time Stamp Counter
ShortName:	TIMESTAMP_CTR
Power:	PG0
Reset:	global

The register is not reset by a FLR or display reset.

DWord	Bit	Description
0	31:0	**TIMESTAMP Counter** This field increments every microsecond. The value in this field is latched in the Pipe Flip TIMESTAMP registers when flips occur, and in the Pipe Frame TIMESTAMP registers at start of vertical blank. The register value will reset if any value is written to it. The register is not reset by a FLR or display reset.

TRANS_CLK_SEL

TRANS_CLK_SEL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	46140h-46143h
Name:	Transcoder A Clock Select
ShortName:	TRANS_CLK_SEL_A
Power:	PG0
Reset:	soft
Address:	46144h-46147h
Name:	Transcoder B Clock Select
ShortName:	TRANS_CLK_SEL_B
Power:	PG0
Reset:	soft
Address:	46148h-4614Bh
Name:	Transcoder C Clock Select
ShortName:	TRANS_CLK_SEL_C
Power:	PG0
Reset:	soft

This register maps the port clock to the transcoder.

DWord	Bit	Description
0	31:29	**Trans Clock Select** Select which DDI clock to use for this transcoder. Transcoder EDP always uses DDIA clock.

Value	Name	Description
000b	None	No PLL selected. Clock is disabled for this transcoder.
010b	DDIB	Select DDIB clock
011b	DDIC	Select DDIC clock
100b	DDID	Select DDID clock.

TRANS_CLK_SEL

		101b DDIE Select DDIE clock 110b DDIF Select DDIF clock **Restriction** This must not be changed while the transcoder is enabled.
	28	**Reserved**
	27:0	**Reserved**

TRANS_CONF

TRANS_CONF	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank (WD cap sync) OR transcoder disabled
Address:	70008h-7000Bh
Name:	Transcoder A Configuration
ShortName:	TRANS_CONF_A
Power:	PG2
Reset:	soft
Address:	71008h-7100Bh
Name:	Transcoder B Configuration
ShortName:	TRANS_CONF_B
Power:	PG2
Reset:	soft
Address:	72008h-7200Bh
Name:	Transcoder C Configuration
ShortName:	TRANS_CONF_C
Power:	PG2
Reset:	soft
Address:	7E008h-7E00Bh
Name:	Transcoder WD0 Configuration
ShortName:	TRANS_CONF_WD0
Power:	PG2
Reset:	soft
Address:	7F008h-7F00Bh
Name:	Transcoder EDP Configuration
ShortName:	TRANS_CONF_EDP

TRANS_CONF

Power: PG1
Reset: soft

Address: 7D008h-7D00Bh
Name: Transcoder WD1 Configuration
ShortName: TRANS_CONF_WD1

Power: PG2
Reset: soft

Address: 7B008h-7B00Bh
Name: Transcoder DSI 0 Configuration
ShortName: TRANS_CONF_DSI0

Power: PG1
Reset: soft

Address: 7B808h-7B80Bh
Name: Transcoder DSI 1 Configuration
ShortName: TRANS_CONF_DSI1

Power: PG1
Reset: soft

DWord	Bit	Description
0	31	**Transcoder Enable** Setting this bit to the value of one, turns on this transcoder. Turning the transcoder off disables the timing generator and synchronization pulses to the display will not be maintained. Enabling the transcoder may be internally delayed for one frame while the display data buffers are re-configured. **Value** / **Name** 0b / Disable 1b / Enable **Restriction** Timing registers must contain valid values before this bit is enabled.
	30	**Transcoder State** Access: RO This read only bit indicates the actual state of the transcoder. **Value** / **Name**

0b	Disabled	
1b	Enabled	

29:23 **Reserved**

22:21 **Interlaced Mode**

These bits control the transcoder interlaced mode. This field is ignored by WD.

Value	Name	Description
00b	PF-PD	Progressive Fetch with Progressive Display
01b	PF-ID	Progressive Fetch with Interlaced Display
11b	IF-ID	Interlaced Fetch with Interlaced Display
Others	Reserved	Reserved

Programming Notes
Progressive Fetch with Interlaced Display requires pipe scaling.

Restriction
VGA display modes do not work while in interlaced fetch mode. Progressive Fetch with Interlaced Display effectively down scales the vertical by 2X, which reduces the maximum supported pixel rate by half.
Interlaced fetch mode is not supported with Y Tiling. Interlaced fetch mode is not supported with 90/270 rotation. Interlaced fetch mode is not supported with scaling. Interlaced fetch mode is not supported with YUV 420 hybrid planar source pixel formats. In Interlaced mode, the plane height must be a minimum of 2 scanlines.

20:7 **Reserved**

Format:	MBZ

6:0 **DP Audio Symbol Watermark**

Default Value:	24h 36 entries

This fields set the level to which the DP audio symbol RAM must fill before it starts to drain during horizontal blank.
The minimum is 2 entries and the maximum is 64.

TRANS_DDI_FUNC_CTL

TRANS_DDI_FUNC_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	60400h-60403h
Name:	Transcoder A DDI Function Control
ShortName:	TRANS_DDI_FUNC_CTL_A
Power:	PG2
Reset:	soft
Address:	61400h-61403h
Name:	Transcoder B DDI Function Control
ShortName:	TRANS_DDI_FUNC_CTL_B
Power:	PG2
Reset:	soft
Address:	62400h-62403h
Name:	Transcoder C DDI Function Control
ShortName:	TRANS_DDI_FUNC_CTL_C
Power:	PG2
Reset:	soft
Address:	6F400h-6F403h
Name:	Transcoder EDP DDI Function Control
ShortName:	TRANS_DDI_FUNC_CTL_EDP
Power:	PG1
Reset:	soft
Address:	6B400h-6B403h
Name:	Transcoder DSI 0 DDI Function Control
ShortName:	TRANS_DDI_FUNC_CTL_DSI0

TRANS_DDI_FUNC_CTL

Power:	PG1
Reset:	soft

Address:	6BC00h-6BC03h
Name:	Transcoder DSI 1 DDI Function Control
ShortName:	TRANS_DDI_FUNC_CTL_DSI1
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31	**TRANS DDI Function Enable** This bit enables the transcoder DDI function. Value: 0b = Disable; 1b = Enable
	30:28	**DDI Select** Description: These bits determine which DDI port this transcoder will connect to. It is not valid to enable and direct more than one transcoder to one DDI, except when using DisplayPort multistreaming. These bits are ignored by transcoder EDP since it can only connect to DDI A (EDP DDI). These bits are ignored by the DSI transcoders since they have a fixed DDI mapping. Restriction: This field must not be changed while the function is enabled.
	27	**Reserved** Format: MBZ

Value	Name	Description
000b	None	No port connected
001b	DDI B	DDI B
010b	DDI C	DDI C
011b	DDI D	DDI D
100b	DDI E	DDI E
Others	Reserved	Reserved
101b	DDI F	

TRANS_DDI_FUNC_CTL

26:24 **TRANS DDI Mode Select**

Description
This field determines the mode of operation. HDMI mode enables a null packet (32 bytes of a value of 0) to be sent when Vsync=1, and also enables preambles and guardbands prior to the null packets, in accordance with the HDMI specification. DVI mode will function as HDMI if DIP packets or audio are enabled.
This field does not apply to the DSI transcoder.

Value	Name	Description
000b	HDMI	Function in HDMI mode
001b	DVI	Function in DVI mode
010b	DP SST	Function in DisplayPort SST mode
011b	DP MST	Function in DisplayPort MST mode
Others	Reserved	Reserved

Restriction
This field must not be changed while the function is enabled. The DisplayPort mode (SST or MST) selected here must match the mode selected in the DisplayPort Transport Control register for the transport attached to this transcoder.
Transcoder EDP and DDI A can only function in DP SST mode.

23 **Reserved**

Format:	MBZ

22:20 **Bits Per Color**

Description
This field selects the number of bits per color output on the DDI connected to this transcoder. Dithering should be enabled when selecting a pixel color depth higher or lower than the pixel color depth of the frame buffer.
This field does not apply to the DSI transcoder. The Pixel Format for the DSI transcoder is defined within the TRANS_DSI_FUNC_CONF register.

Value	Name	Description
000b	8 bpc	
001b	10 bpc	
010b	6 bpc	
011b	12 bpc	
Others	Reserved	Reserved

Restriction

	This field must not be changed while the function is enabled. 6bpc not supported with HDMI.
19:18	**Reserved**
17:16	**Sync Polarity**

Description
This field indicates the polarity of Hsync and Vsync. Field ignored by the DSI transcoder

Value	Name	Description
00b	Low	VS and HS are active low (inverted)
01b	VS Low, HS High	VS is active low (inverted), HS is active high
10b	VS High, HS Low	VS is active high, HS is active low (inverted)
11b	High **[Default]**	VS and HS are active high

15	**Reserved**
14:12	**EDP/DSI Input Select**

These bits determine the input to transcoder EDP or transcoder DSI. These bits are ignored by the other transcoders.

Value	Name
000b	Pipe A
101b	Pipe B
110b	Pipe C
Others	Reserved

Restriction
This field must not be changed while the function is enabled. It is not valid to have the same pipes driving multiple enabled transcoders.

11:10	**Reserved**
	Format: MBZ
9	**Reserved**
8	**DP VC Payload Allocate**

Description

TRANS_DDI_FUNC_CTL

		This bit enables DisplayPort Virtual Channel payload allocation. This bit is ignored by transcoder EDP since it does not support multistreaming. This bit is ignored by transcoder DSI since it does not support multistreaming **Value** / **Name** 0b – Disable 1b – Enable
	7	**HDMI Scrambler CTS Enable** **Description** This bit enables Compliance Test Specification mode on the HDMI scrambler. This bit must be set before the scrambler is enabled. This bit is ignored by transcoder DSI **Value** / **Name** 0b – Disable 1b – True
	6	**HDMI Scrambler Reset frequency** This bit specifies the frequency at which the scrambler is reset when the HDMI Scrambler CTS Enable bit is set. This bit must be set before or along with the HDMI Scrambler CTS Enable bit. **Value** / **Name** / **Description** 0b – Every Line – SSCP sent on hsync of every line 1b – Every Other Line – SSCP sent on hsync of every other line
	5	**Reserved**
	4	**High TMDS Char Rate** This field enables the high TMDS character rate. It must be enabled when the HDMI link symbol rate is greater than 340 MHz. It must be disabled when the HDMI link symbol rate is less than or equal to 340 MHz. **Value** / **Name** / **Description** 0 – Disable – TMDS Character Rate is less than or equal to 340 Mega-characters/second/channel 1 – Enable – TMDS Character Rate is greater than 340 Mega-characters/second/channel
	3:1	**Port Width Selection** This field selects the number of lanes to be enabled on the DDI link for DisplayPort and DSI. for DSI, this field specifies the number of Data lanes to use - the Clock lane is always enabled when the DSI function is enabled. This field is ignored for HDMI and DVI which always use all 4 lanes.

The value selected here must match the value selected in the DDI Buffer Control register for the DDI attached to this pipe.

Value	Name	Description
000b	x1	x1 Mode
001b	x2	x2 Mode
010b	x3	x3 Mode (DSI only)
011b	x4	x4 Mode
Others	Reserved	Reserved

Restriction
This field must not be changed while the DDI is enabled.

0 **HDMI Scrambling Enabled**

Setting this bit enables scrambling over the HDMI link.
Scrambling must be enabled when the HDMI link symbol rate is greater than 340 MHz.
Scrambling should be enabled at lower frequencies if the receiver supports it at that speed.
This must not changed while the port is enabled.

Value	Name
0b	Disable
1b	Enable

TRANS_DDI_FUNC_CTL2

TRANS_DDI_FUNC_CTL2	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	60404h-60407h
Name:	Transcoder A DDI Function Control2
ShortName:	TRANS_DDI_FUNC_CTL2_A
Power:	PG2
Reset:	soft
Address:	61404h-61407h
Name:	Transcoder B DDI Function Control2
ShortName:	TRANS_DDI_FUNC_CTL2_B
Power:	PG2
Reset:	soft
Address:	62404h-62407h
Name:	Transcoder C DDI Function Control2
ShortName:	TRANS_DDI_FUNC_CTL2_C
Power:	PG2
Reset:	soft
Address:	6F404h-6F407h
Name:	Transcoder EDP DDI Function Control2
ShortName:	TRANS_DDI_FUNC_CTL2_EDP
Power:	PG1
Reset:	soft
Address:	6B404h-6B407h
Name:	Transcoder DSI 0 DDI Function Control2
ShortName:	TRANS_DDI_FUNC_CTL2_DSI0

TRANS_DDI_FUNC_CTL2

Power:	PG1
Reset:	soft

Address:	6BC04h-6BC07h
Name:	Transcoder DSI 1 DDI Function Control2
ShortName:	TRANS_DDI_FUNC_CTL2_DSI1
Power:	PG1
Reset:	soft

DWord	Bit	Description
0	31:29	**Reserved**
	28:9	**Reserved**
	8	**Reserved**
	7:6	**Reserved**
	5	**Reserved**
	4	**Port Sync Mode Enable** **Description** This field enables the DisplayPort port sync mode on this transcoder. This mode forces two or more transcoders to be in sync; with one transcoder master and one or more transcoder slaves. The master is unaware that it is operating in this mode. Only the slave is aware that it is operating in this mode. Port sync mode is only enabled in the slave transcoder. This bit is ignored by transcoder EDP since it cannot be slaved to another port. For DSI, this bit enables DSI Transcoder 1 to be a slave to DSI Transcoder 0. DSI Transcoder 0 is unaware that it is the master of DSI Transcoder 1 **Value** / **Name** 0b / Disable 1b / Enable **Restriction** Follow the instructions for enabling and disabling Sync Mode in the Display Mode Set Sequence - Sequence for DisplayPort. Port Sync Mode Master Select must be programmed with a valid value when Port sync Mode is enabled. The slave and master transcoders and associated ports must have identical parameters and properties. They must have the same color format, link width (number of lanes enabled), resolution, refresh rate, dot clock, TU size, M and N

programming, etc.

Port Sync Mode can be enabled with DisplayPort SST and with DisplayPort MST.

3 **Reserved**

2:0 **Port Sync Mode Master Select**

Description
This field indicates which transcoder will be the master to this transcoder when in port sync mode.
This bit is ignored by transcoder EDP since it cannot be slaved to another port.
This field is ignored by the DSI transcoders since only DSI 0 can be the master.

Value	Name
000b	Transcoder EDP
001b	Transcoder A
010b	Transcoder B
011b	Transcoder C

Restriction
A port cannot be slaved to itself.
The DSI transcoders cannot be slaved to a non-DSI transcoder - field ignored by the DSI transcoder.

TRANS_DSI_FUNC_CONF

TRANS_DSI_FUNC_CONF

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32

Address:	6B030h-6B033h
Name:	Transcoder DSI 0 Function Configuration
ShortName:	TRANS_DSI_FUNC_CONF_0
Power:	PG1
Reset:	soft

Address:	6B830h-6B833h
Name:	Transcoder DSI 1 Function Configuration
ShortName:	TRANS_DSI_FUNC_CONF_1
Power:	PG1
Reset:	soft

This register defines the functional transcoder configuration that is specific to the DSI transcoders.

Restriction :
This register must be programmed before the DSI Transcoder function is enabled (i.e. TRANS DDI Function Enable)
The contents of this register must not be changed while the DSI Transcoder function is enabled

DWord	Bit	Description
0	31:30	**Reserved** Format: MBZ
	29:28	**Mode of Operation** Access: R/W This defines whether the DSI transcoder is in Video or Command mode. In addition to the main modes, there are two sub-modes per main mode. For the Command sub-modes, when in the "No Gate" mode, the transcoder will begin transmitting the frame pixels as soon as they are received from the Display Engine. When in the "TE Gate" mode, the transcoder will only start transmitting the frame pixels after a TE event is received. For the Video sub-modes, when in the Sync Event mode only Sync Start packets (VSS/HSS) are sent to the Periphery. When in the Sync Pulse mode, both Sync Start (VSS/HSS) and Sync End (VSE/HSE) packets are sent to the Periphery. Note that regardless of the programming of this field, until the Transcoder Enable bit is set within the TRANS_CONF_DSI register, the DSI transcoder will not generate any timing

TRANS_DSI_FUNC_CONF

information to the Display Engine or timing packets to the Peripharal

Value	Name
00b	Command Mode (No Gate)
01b	Command Mode (TE Gate)
10b	Video Mode (Sync Event)
11b	Video Mode (Sync Pulse)

27 **TE Source**

Access:	R/W

This bit defines the source of the TE events from the Peripheral when the Transcoder is operating in Command Mode

Value	Name
0	In-band TE event source
1	Out-of-band TE event source (i.e. GPIO)

26 **TE Deglitch Enable**

Access:	R/W

When using the GPIO as the source of TE events in Command Mode, this bit will control whether the signaling from the GPIO pin is debounced or not.

Value	Name
0b	Disabled
1b	Enabled

25:21 **Reserved**

Format:	MBZ

20 **Link Ready**

Access:	RO

This bit advertises whether the Link is ready to receive traffic from the DSI transcoder

Value	Name
0	Link is not ready to accept traffic
1	Link is ready to accept traffic

19 **Reserved**

Format:	MBZ

18:16 **Pixel Format**

Access:	R/W

This field defines the pixel format the DSI Transcoder will be operating in

Value	Name
000b	16-bit RGB, 5-6-5

001b	18-bit RGB, 6-6-6 (Packed)
010b	18-bit RGB, 6-6-6 (Loose)
011b	24-bit RGB, 8-8-8
100b	30-bit RGB, 10-10-10
101b	36-bit RGB, 12-12-12
110b	Compressed
Others	Reserved

Restriction
When in the 18-bit RGB (Packed) pixel format, the H. Active Size must be a multiple of 4 pixels

15 **BGR Transmission**

Access:	R/W

This field will reverse the order of the RGB channels within the pixels received from the Display Engine

Value	Name
0	Transmit order is R-G-B
1	Transmit order is B-G-R

14 **Reserved**

Format:	MBZ

13:12 **Pixel Virtual Channel**

Access:	R/W

This field defines the Virtual Channel that HW will bind to all DSI packets carrying pixel data

11:10 **Pixel Buffer Threshold**

Access:	R/W

This field defines the threshold of buffering needed within the Pixel Buffer before the transcoder will start internally processing the pixel stream.

Value	Name
00b	The Pixel Buffer will have to be 1/4 full
01b	The Pixel Buffer will have to be 1/2 full
10b	The Pixel Buffer will have to be 3/4 full
11b	The Pixel Buffer will have to be full

9:8 **Continuous Clock**

Access:	R/W

This field will control the behavior of the Clock Lane and whether it is allowed to enter the LP state.
Keeping the Clock Lane running while letting the Data Lanes go in and out of the LP state keeps the LP to HS turnaround latency to a minimum, but consumes more power.

TRANS_DSI_FUNC_CONF

Certain panels may also require the Clock Lane to continuously run

Value	Name
00b	Always enter LP after Data Lanes
10b	Opportunistically keep Clock in HS or LP
11b	Continuous HS Clock
Others	Reserved

7:6 **Reserved**

Format:	MBZ

5:4 **Link Calibration**

Access:	R/W

This field will control the Link calibration of the DSI Transcoder

Value	Name
00b	Calibration Disabled
10b	Calibration Enabled - Initial only
11b	Calibration Enabled - Initial and Periodic
Others	Reserved

Restriction
Calibration can be enabled for any Link frequency, but it must be enabled when the Link frequency is operating above 1.5 Gbps

3:2 **Reserved**

Format:	MBZ

1 **S3D Orientation**

Access:	R/W

This bit controls the orientation encoding of the 3DMODE field of the Stereoscopic 3D control function sent to a Panel via the Vertical Source Sync (VSS) packet when in Video Mode.

Value	Name
0b	Portrait Orientation
1b	Landscape Orientation

Programming Notes
This bit will only be sampled by the transcoder when Stereoscopic 3D is enabled for the transcoder This bit should be programmed before enabling Stereoscopic 3D for the transcoder (TRANS_STEREO3D_CTL) If Software changes this bit, it must also perform a write to the TRANS_STEREO3D_CTL for the

		change to be sent within the next VSS This bit is only applicable when the transcoder is operating in Video Mode. If the transcoder is operating in Command Mode, then Software will have to communicate the Stereoscopic 3D function information to the Panel through a set_3D_control DCS command using the DCS Long Write DSI packet type.
	0	**EoTp Disabled** Access: R/W When set, the DSI transcoder will not transmit an End of Transmission packet at the end of High Speed bursts Value / Name: 0 – EoTp Enabled 1 – EoTp Disabled

TRANS_FRM_TIME

TRANS_FRM_TIME - TRANS_FRM_TIME

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of capture sync or transcoder not enabled

Address:	6E020h-6E023h
Name:	TRANS_FRM_TIME_WD0
ShortName:	TRANS_FRM_TIME_WD0
Power:	PG2
Reset:	soft

Address:	6E820h-6E823h
Name:	TRANS_FRM_TIME_WD1
ShortName:	TRANS_FRM_TIME_WD1
Power:	PG2
Reset:	soft

This register is only for WD transcoders.

Programming Notes

Examples: For 60Hz the frame time is 16,666.66us, program integer 16,665 and fraction 2/3. For 24Hz the frame time is 41,666.66us, program integer 41,665 and fraction 2/3. For 59.94Hz the frame time is 16,683.33us, program integer 16,682 and fraction 1/3.

The frame time can be changed on the fly.

DWord	Bit	Description
0	31:16	**Frame Time Integer** This field specifies the integer portion of the time in microseconds for a display frame. This is used to determine the rate at which to generate frames when capturing display. This field is programmed to the integer number of microseconds desired minus one. **Restriction** A value of 0 is invalid when the transcoder is enabled.
	15:14	**Frame Time Fraction** This field specifies the fractional portion of the time in microseconds for a display frame. This is used to determine the rate at which to generate frames when capturing display. **Value** / **Name** 00b / 0

TRANS_FRM_TIME - TRANS_FRM_TIME			
		01b	1/3
		10b	2/3
		Others	Reserved
	13:0	**Reserved**	

TRANS_HBLANK

TRANS_HBLANK	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	60004h-60007h
Name:	Transcoder A Horizontal Blank
ShortName:	TRANS_HBLANK_A
Power:	PG2
Reset:	soft
Address:	61004h-61007h
Name:	Transcoder B Horizontal Blank
ShortName:	TRANS_HBLANK_B
Power:	PG2
Reset:	soft
Address:	62004h-62007h
Name:	Transcoder C Horizontal Blank
ShortName:	TRANS_HBLANK_C
Power:	PG2
Reset:	soft
Address:	6F004h-6F007h
Name:	Transcoder EDP Horizontal Blank
ShortName:	TRANS_HBLANK_EDP
Power:	PG1
Reset:	soft

Restriction
This register should not be changed while the transcoder or port are enabled.

DWord	Bit	Description
0	31:30	**Reserved**

TRANS_HBLANK		
	29:16	**Horizontal Blank End** This field specifies Horizontal Blank End position relative to the horizontal active display start. **Restriction** The minimum horizontal blank size is 32 pixels. For HDMI Audio transmission the minimum is 138 pixels. This register must always be programmed to the same value as the Horizontal Total.
	15:14	**Reserved**
	13:0	**Horizontal Blank Start** This field specifies the Horizontal Blank Start position relative to the horizontal active display start. **Restriction** This register must always be programmed to the same value as the Horizontal Active.

TRANS_HSYNC

TRANS_HSYNC	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	60008h-6000Bh
Name:	Transcoder A Horizontal Sync
ShortName:	TRANS_HSYNC_A
Power:	PG2
Reset:	soft
Address:	61008h-6100Bh
Name:	Transcoder B Horizontal Sync
ShortName:	TRANS_HSYNC_B
Power:	PG2
Reset:	soft
Address:	62008h-6200Bh
Name:	Transcoder C Horizontal Sync
ShortName:	TRANS_HSYNC_C
Power:	PG2
Reset:	soft
Address:	6F008h-6F00Bh
Name:	Transcoder EDP Horizontal Sync
ShortName:	TRANS_HSYNC_EDP
Power:	PG1
Reset:	soft
Address:	6B008h-6B00Bh
Name:	Transcoder DSI 0 Horizontal Sync
ShortName:	TRANS_HSYNC_DSI0

TRANS_HSYNC

Power:	PG1
Reset:	soft
Address:	6B808h-6B80Bh
Name:	Transcoder DSI 1 Horizontal Sync
ShortName:	TRANS_HSYNC_DSI1
Power:	PG1
Reset:	soft

Restriction

This register should not be changed while the transcoder or port are enabled.
HSYNC is always programmed to an even number of pixel clock cycles for YUV 4:2:0 pixel format with 10bpc and 12bpc..

DWord	Bit	Description
0	31:30	**Reserved** Format: MBZ
	29:16	**Horizontal Sync End** This field specifies the Horizontal Sync End position relative to the horizontal active display start. It is programmed with HorizontalActive+FrontPorch+Sync-1 **Restriction** This value must be greater than the horizontal sync start and less than Horizontal Total. For the DSI transcoder this field is only relevant if the transcoder is operating in Video Mode (it is ignored in Command Mode). As such, please refer to the "Determining Minimum Horizontal Blanking Regions" section of the Transcoder DSI Function page for minimum programming allowed
	15:14	**Reserved** Format: MBZ
	13:0	**Horizontal Sync Start** This field specifies the Horizontal Sync Start position relative to the horizontal active display start. It is programmed with HorizontalActive + FrontPorch - 1 **Restriction** This value must be greater than Horizontal Active for all non-DSI transcoders, or for DSI transcoders operating with non-compressed pixels in Video Mode. For DSI transcoders operating on a compressed pixel stream in Video Mode, this value should be greater than the Horizontal Active size divided by the Compression Ratio (H. Blank Start = H. Active / Compression Ratio). In HDMI modes the minimum gap between horizontal blank start and horizontal sync start is 16

TRANS_HSYNC		
		pixels. For DSI transcoders, this field is only relevant if the transcoder is operating in Video Mode (it is ignored in Command Mode). When the DSI transcoder is in Video Mode, then please refer to the "Determining Minimum Horizontal Blanking Regions" section of the Transcoder DSI Function page for minimum programming allowed.

TRANS_HTOTAL

TRANS_HTOTAL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	60000h-60003h
Name:	Transcoder A Horizontal Total
ShortName:	TRANS_HTOTAL_A
Power:	PG2
Reset:	soft
Address:	61000h-61003h
Name:	Transcoder B Horizontal Total
ShortName:	TRANS_HTOTAL_B
Power:	PG2
Reset:	soft
Address:	62000h-62003h
Name:	Transcoder C Horizontal Total
ShortName:	TRANS_HTOTAL_C
Power:	PG2
Reset:	soft
Address:	6E000h-6E003h
Name:	Transcoder WD0 Horizontal Total
ShortName:	TRANS_HTOTAL_WD0
Power:	PG2
Reset:	soft
Address:	6F000h-6F003h
Name:	Transcoder EDP Horizontal Total
ShortName:	TRANS_HTOTAL_EDP

TRANS_HTOTAL

Power:	PG1
Reset:	soft

Address:	6E800h-6E803h
Name:	Transcoder WD1 Horizontal Total
ShortName:	TRANS_HTOTAL_WD1
Power:	PG2
Reset:	soft

Address:	6B000h-6B003h
Name:	Transcoder DSI 0 Horizontal Total
ShortName:	TRANS_HTOTAL_DSI0
Power:	PG1
Reset:	soft

Address:	6B800h-6B803h
Name:	Transcoder DSI 1 Horizontal Total
ShortName:	TRANS_HTOTAL_DSI1
Power:	PG1
Reset:	soft

Restriction
This register should not be changed while the transcoder or port are enabled.
The following restriction applies only to HDMI 4:2:0. All horizontal timings should be a multiple of 4 for 8/12/16 bpc cases and multiple of 8 for 10 bpc case. This applies to full blend and bypass modes.

DWord	Bit	Description
0	31:30	**Reserved** Format: MBZ
	29:16	**Horizontal Total** This field specifies Horizontal Total size. This field is programmed to the number of pixels desired minus one. This should be equal to the sum of the horizontal active and the horizontal blank sizes for all non-DSI transcoders, or for DSI transcoders operating with non-compressed pixels in Video Mode. For DSI transcoders operating with compressed pixels in Video Mode, this field should be equal to the sum of the compressed horizontal active size and the horizontal blank size (H. Total = (H.

TRANS_HTOTAL

		Active + H. Blank size) / Compression Ratio) For DSI transcoders operating in Command Mode, there are no restrictions on the programming of this field. This field is ignored by WD transcoders. **Restriction** This register must always be programmed to the same value as the Horizontal Blank End.
	15:14	**Reserved** Format: MBZ
	13:0	**Horizontal Active** This field specifies Horizontal Active Display size. The first horizontal active display pixel is considered pixel number 0. This field is programmed to the number of pixels desired minus one. **Restriction** The minimum horizontal active display size is 64 pixels. In HDMI modes the minimum is 256 pixels. This register must always be programmed to the same value as the Horizontal Blank Start. DSI requires a minimum Horizontal Active Display of, 256 pixels. Also, when transmitting an 18-bit RGB pixel format, the one-based size must be a multiple of 4 pixels

TRANS_MSA_MISC

TRANS_MSA_MISC	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	60410h-60413h
Name:	Transcoder A MSA Misc
ShortName:	TRANS_MSA_MISC_A
Power:	PG2
Reset:	soft
Address:	61410h-61413h
Name:	Transcoder B MSA Misc
ShortName:	TRANS_MSA_MISC_B
Power:	PG2
Reset:	soft
Address:	62410h-62413h
Name:	Transcoder C MSA Misc
ShortName:	TRANS_MSA_MISC_C
Power:	PG2
Reset:	soft
Address:	6F410h-6F413h
Name:	Transcoder EDP MSA Misc
ShortName:	TRANS_MSA_MISC_EDP
Power:	PG1
Reset:	soft

This register selects what value will be sent in the DisplayPort Main Stream Attribute (MSA) Miscellaneous (MISC) fields. The MSA MISC fields are mostly used to indicate the color encoding format and need to be programmed to indicate color space, bits per color, etc.

Programming Notes
See the DisplayPort specification for the details on what to program in these fields.

DWord	Bit	Description
0	31:16	**MSA Unused** This field selects the value that will be sent in the DisplayPort MSA unused fields. **Programming Notes** This should be usually programmed with all 0s.
	15:8	**MSA MISC1** This field selects the value that will be sent in the DisplayPort MSA MISC1 field. When TRANS_STEREO3D_CTL bit FS_MSA_MISC1_Drive_En is enabled, hardware will drive MISC1 bits 2:1 (bits 10:9 of this register) with the field sequential stereo 3D left or right eye indication, and any value written to those bits here will be ignored.
	7:0	**MSA MISC0** This field selects the value that will be sent in the DisplayPort MSA MISC0 field. **Restriction** Before enabling DisplayPort, bit 0 should always be set to 1 to indicate link clock and stream clock are synchronous.

TRANS_MULT

TRANS_MULT	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6002Ch-6002Fh
Name:	Transcoder A Multiply
ShortName:	TRANS_MULT_A
Power:	PG2
Reset:	soft
Address:	6102Ch-6102Fh
Name:	Transcoder B Multiply
ShortName:	TRANS_MULT_B
Power:	PG2
Reset:	soft
Address:	6202Ch-6202Fh
Name:	Transcoder C Multiply
ShortName:	TRANS_MULT_C
Power:	PG2
Reset:	soft

Restriction
This register should not be changed while the transcoder or port are enabled.

DWord	Bit	Description
0	31:3	**Reserved**
	2:0	**Multiplier** This field specifies the data multiplier value used by HDMI and DVI.

Value	Name	Description
000b	X1	Multiply by 1
001b	X2	Multiply by 2
011b	X4	Multiply by 4
Others	Reserved	Reserved

TRANS_PUSH

TRANS_PUSH	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	60A70h-60A73h
Name:	Transcoder A ASFU/VRR Push
ShortName:	TRANS_PUSH_A
Power:	PG2
Reset:	soft
Address:	61A70h-61A73h
Name:	Transcoder B ASFU/VRR Push
ShortName:	TRANS_PUSH_B
Power:	PG2
Reset:	soft
Address:	62A70h-62A73h
Name:	Transcoder C ASFU/VRR Push
ShortName:	TRANS_PUSH_C
Power:	PG2
Reset:	soft
Address:	6FA70h-6FA73h
Name:	Transcoder EDP ASFU/VRR Push
ShortName:	TRANS_PUSH_EDP
Power:	PG1
Reset:	soft

After programming any pipe registers in ASFU/VRR cases, Software can set push bit. H/W will sync all those updates for that frame.

DWord	Bit	Description
0	31	**Push Enable** This bit enables Push frame functionality. This bit should be set before ASFU/VRR enable.

TRANS_PUSH

		Value / **Name** 0b / Disable 1b / Enable
	30	**Send Push** Access: R/W Set Writing a 1b to this field hints that Frame update is desired. Vblank is asserted at the next decision boundary. This is a sticky bit. The bit will be cleared by hardware after double buffer update. Writing a 0b has no effect.
	29:0	**Reserved**

TRANS_SPACE

TRANS_SPACE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	60024h-60027h
Name:	Transcoder A Space
ShortName:	TRANS_SPACE_A
Power:	PG2
Reset:	soft
Address:	61024h-61027h
Name:	Transcoder B Space
ShortName:	TRANS_SPACE_B
Power:	PG2
Reset:	soft
Address:	62024h-62027h
Name:	Transcoder C Space
ShortName:	TRANS_SPACE_C
Power:	PG2
Reset:	soft
Address:	6F024h-6F027h
Name:	Transcoder EDP Space
ShortName:	TRANS_SPACE_EDP
Power:	PG1
Reset:	soft
Address:	6B024h-6B027h
Name:	Transcoder DSI 0 Space
ShortName:	TRANS_SPACE_DSI0

TRANS_SPACE

Power:	PG1
Reset:	soft
Address:	6B824h-6B827h
Name:	Transcoder DSI 1 Space
ShortName:	TRANS_SPACE_DSI1
Power:	PG1
Reset:	soft

Restriction
This register should not be changed while the transcoder or port are enabled.

DWord	Bit	Description
0	31:12	**Reserved**
	11:0	**Vertical Active Space** This field specifies Stereo 3D Vertical Active space. This determines the number of constant pixel value lines inserted between the left and right eye active video regions in the stereo 3D stacked frame mode. This field will only be used when the transcoder is in the stereo 3D stacked frame mode. This field should usually be programmed to be the same as the width of the vertical blank.

TRANS_STEREO3D_CTL

TRANS_STEREO3D_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	70020h-70023h
Name:	Transcoder A Stereo 3D Control
ShortName:	TRANS_STEREO3D_CTL_A
Power:	PG2
Reset:	soft
Address:	71020h-71023h
Name:	Transcoder B Stereo 3D Control
ShortName:	TRANS_STEREO3D_CTL_B
Power:	PG2
Reset:	soft
Address:	72020h-72023h
Name:	Transcoder C Stereo 3D Control
ShortName:	TRANS_STEREO3D_CTL_C
Power:	PG2
Reset:	soft
Address:	7B020h-7B023h
Name:	Transcoder DSI 0 Stereo 3D Control
ShortName:	TRANS_STEREO3D_CTL_DSI0
Power:	PG1
Reset:	soft
Address:	7B820h-7B823h
Name:	Transcoder DSI 1 Stereo 3D Control
ShortName:	TRANS_STEREO3D_CTL_DSI1

TRANS_STEREO3D_CTL

Power:	PG1
Reset:	soft

Address:	7F020h-7F023h
Name:	Transcoder EDP Stereo 3D Control
ShortName:	TRANS_STEREO3D_CTL_EDP
Power:	PG1
Reset:	soft

This register is sampled one line before vertical blank.

DWord	Bit	Description
0	31	**Transcoder S3D Enable** This bit enables the stereo 3D modes on this transcoder. Updates will take place at the start of the next vertical blank. **Value** / **Name**: 0b Disable; 1b Enable **Restriction**: These modes are only for use with DisplayPort, HDMI, and DVI. HDMI/DVI: Stereo 3D can only be enabled with a mode set. It must be enabled before transcoder and port are enabled. It must be disabled after transcoder is disabled. DisplayPort: Stereo 3D can be enabled and disabled with a mode set, like HDMI and DVI, or it can be enabled after an enable mode set is complete and disabled prior to a disable mode set. VGA display modes, interlaced modes, SRD/PSR, WD, and frame buffer compression (FBC) do not work with stereo 3D. The left surface base address registers for the planes going to this transcoder must be programmed with valid addresses prior to enabling stereo 3D.
	30:29	**Reserved**
	28:27	**S3D Mode** This field selects between the stereo 3D modes. The stacked buffer mode combines both stereo 3D fields (left and right eye images) into a single tall frame with the left eye image on top, then a programmable space of black lines, then the right eye image on the bottom. The field sequential mode sends one stereo 3D field (left or right eye image) out per frame. This mode is only for use with DisplayPort. Field sequential hardware controlled mode automatically toggles between left and right eye at the start of each vertical blank. The starting field is selected using the FS_Field_Ctl register bit. Field sequential software controlled mode will manually select left or right eye using the FS_Field_Ctl register bit. **Value** / **Name** / **Description**: 00b FS HW Auto — Hardware controlled auto-toggle between left and right eye on each vertical blank.

01b	FS SW Manual	Software controlled selection between left and right eye
10b	Stacked	Stacked frame mode with both left and right eye images combined in a single tall frame
Others	Reserved	Reserved

Programming Notes

In the stacked frame mode, a vertical sync is not generated in the gap between left and right eye images, and the scan line count increments across the entire tall frame.

Restriction

This field should only be changed when stereo 3D is disabled.

26 **FS Field Ctl**

The operation of this bit depends on the S3D Mode setting. This field is ignored in the S3D stacked mode. In the field sequential software controlled mode this bit selects the field sequential stereo 3D field (left or right eye). In the field sequential hardware controlled mode this bit selects the field sequential stereo 3D starting field, the field used on the frame when field sequential stereo 3D is enabled. Hardware does not wait for a specific eye when disabling.

Value	Name
0b	Right Eye
1b	Left Eye **[Default]**

Restriction

The starting field must be set to the left eye for FS HW Auto usage.

25 **Reserved**

Format:	MBZ

24 **S3D Current Field**

Access:	RO

This read only bit indicates the current stereo 3D field (left or right eye). This bit should be ignored when stereo 3D is not enabled.

Value	Name
0b	Right Eye
1b	Left Eye

23 **FS MSA MISC1 Drive En**

This bit enables hardware to drive the MSA MISC1 bits 2:1 with the internal field sequential stereo 3D left/right eye field indication. Hardware will drive 00 when field sequential 3D stereo mode is not enabled, 01 when enabled and the upcoming video frame is the right eye, 11 when enabled and the upcoming video frame is the left eye. This is based on the internal left/right indication which could be either generated by hardware in the HW auto mode or by software in the SW manual mode. FS_MSA_Drive_Invert can be programmed to invert the left and right eye

selection in the MSA. When this bit is disabled, software may manually program TRANS_MSA_MISC to set MISC1 bits 2:1.

Value	Name	Description
0b	Disable	Disable hardware driving MSA MISC1 bits 2:1. Allow software to manually program MSA MISC1 bits 2:1 through TRANS_MSA_MISC.
1b	Enable	Enable hardware to drive MSA MISC1 bits 2:1 for stereo 3D.

Restriction
This field should only be changed when stereo 3D is disabled and should not be enabled for the stacked frame mode.

22	**Reserved**	
21:0	**Reserved**	
	Format:	MBZ

TRANS_VBLANK

TRANS_VBLANK	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	60010h-60013h
Name:	Transcoder A Vertical Blank
ShortName:	TRANS_VBLANK_A
Power:	PG2
Reset:	soft
Address:	61010h-61013h
Name:	Transcoder B Vertical Blank
ShortName:	TRANS_VBLANK_B
Power:	PG2
Reset:	soft
Address:	62010h-62013h
Name:	Transcoder C Vertical Blank
ShortName:	TRANS_VBLANK_C
Power:	PG2
Reset:	soft
Address:	6F010h-6F013h
Name:	Transcoder EDP Vertical Blank
ShortName:	TRANS_VBLANK_EDP
Power:	PG1
Reset:	soft

Restriction
This register should not be changed while the transcoder or port are enabled.

DWord	Bit	Description
0	31:29	**Reserved**

TRANS_VBLANK		
	28:16	**Vertical Blank End** This field specifies Vertical Blank End position relative to the vertical active display start. **Restriction** This register must always be programmed to the same value as the Vertical Total. The minimum vertical blank size is 5 lines. With SRD/PSR and/or DisplayPort VDIP GMP the minimum is 8 lines.
	15:13	**Reserved**
	12:0	**Vertical Blank Start** This field specifies the Vertical Blank Start position relative to the vertical active display start. **Restriction** This register must always be programmed to the same value as the Vertical Active.

TRANS_VRR_FLIPLINE

TRANS_VRR_FLIPLINE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	60438h-6043Bh
Name:	VRR Flipline Trans A
ShortName:	TRANS_VRR_FLIPLINE_A
Power:	PG2
Reset:	soft
Address:	61438h-6143Bh
Name:	VRR Flipline Trans B
ShortName:	TRANS_VRR_FLIPLINE_B
Power:	PG2
Reset:	soft
Address:	62438h-6243Bh
Name:	VRR Flipline Trans C
ShortName:	TRANS_VRR_FLIPLINE_C
Power:	PG2
Reset:	soft
Address:	6F438h-6F43Bh
Name:	VRR Flipline Trans EDP
ShortName:	TRANS_VRR_FLIPLINE_EDP
Power:	PG1
Reset:	soft

This register defines vertical total size to execute a flip for VRR.

DWord	Bit	Description
0	31:20	**Reserved** Default Value: 000000000000000b Access: RO
	19:0	**VRR FLIPLINE** This field provides the vertical total size to execute flip for VRR.

TRANS_VRR_STATUS2

TRANS_VRR_STATUS2	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6043Ch-6043Fh
Name:	VRR Status2 Trans A
ShortName:	TRANS_VRR_STATUS2_A
Power:	PG2
Reset:	soft
Address:	6143Ch-6143Fh
Name:	VRR Status2 Trans B
ShortName:	TRANS_VRR_STATUS2_B
Power:	PG2
Reset:	soft
Address:	6243Ch-6243Fh
Name:	VRR Status2 Trans C
ShortName:	TRANS_VRR_STATUS2_C
Power:	PG2
Reset:	soft
Address:	6343Ch-6343Fh
Name:	VRR Status2 Trans D
ShortName:	TRANS_VRR_STATUS2_D
Power:	PG2
Reset:	soft
Address:	6F43Ch-6F43Fh
Name:	VRR Status2 Trans EDP
ShortName:	TRANS_VRR_STATUS2_EDP

TRANS_VRR_STATUS2

Power: PG1

Reset: soft

This register provides the live status of vertical line counter. This field should be used to issue flip during VRR Flip Line mode.

DWord	Bit	Description
0	31:20	**Reserved**
	19:0	**Vertical Line Counter Status** Access: RO This field provides the live status of vertical line counter. This field should be used to issue flip during VRR Flip Line mode.

TRANS_VSYNC

TRANS_VSYNC	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	60014h-60017h
Name:	Transcoder A Vertical Sync
ShortName:	TRANS_VSYNC_A
Power:	PG2
Reset:	soft
Address:	61014h-61017h
Name:	Transcoder B Vertical Sync
ShortName:	TRANS_VSYNC_B
Power:	PG2
Reset:	soft
Address:	62014h-62017h
Name:	Transcoder C Vertical Sync
ShortName:	TRANS_VSYNC_C
Power:	PG2
Reset:	soft
Address:	6F014h-6F017h
Name:	Transcoder EDP Vertical Sync
ShortName:	TRANS_VSYNC_EDP
Power:	PG1
Reset:	soft
Address:	6B014h-6B017h
Name:	Transcoder DSI 0 Vertical Sync
ShortName:	TRANS_VSYNC_DSI0

TRANS_VSYNC

Power:	PG1
Reset:	soft
Address:	6B814h-6B817h
Name:	Transcoder DSI 1 Vertical Sync
ShortName:	TRANS_VSYNC_DSI1
Power:	PG1
Reset:	soft

Restriction
This register should not be changed while the transcoder or port are enabled.

DWord	Bit	Description
0	31:29	**Reserved**
	28:16	**Vertical Sync End** This field specifies the Vertical Sync End position relative to the vertical active display start. It is programmed with VerticalActive+FrontPorch+Sync-1 **Restriction** This value must be greater than the vertical sync start and less than Vertical Total.
	15:13	**Reserved**
	12:0	**Vertical Sync Start** This field specifies the Vertical Sync Start position relative to the vertical active display start. It is programmed with VerticalActive+FrontPorch-1 **Restriction** This value must be greater than Vertical Active.

TRANS_VSYNCSHIFT

TRANS_VSYNCSHIFT	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	60028h-6002Bh
Name:	Transcoder A Vertical Sync Shift
ShortName:	TRANS_VSYNCSHIFT_A
Power:	PG2
Reset:	soft
Address:	61028h-6102Bh
Name:	Transcoder B Vertical Sync Shift
ShortName:	TRANS_VSYNCSHIFT_B
Power:	PG2
Reset:	soft
Address:	62028h-6202Bh
Name:	Transcoder C Vertical Sync Shift
ShortName:	TRANS_VSYNCSHIFT_C
Power:	PG2
Reset:	soft
Address:	6F028h-6F02Bh
Name:	Transcoder EDP Vertical Sync Shift
ShortName:	TRANS_VSYNCSHIFT_EDP
Power:	PG1
Reset:	soft
Address:	6B028h-6B02Bh
Name:	Transcoder DSI 0 Vertical Sync Shift
ShortName:	TRANS_VSYNCSHIFT_DSI0

TRANS_VSYNCSHIFT

Power:	PG1
Reset:	soft
Address:	6B828h-6B82Bh
Name:	Transcoder DSI 1 Vertical Sync Shift
ShortName:	TRANS_VSYNCSHIFT_DSI1
Power:	PG1
Reset:	soft

Restriction
This register should not be changed while the transcoder or port are enabled.

DWord	Bit	Description
0	31:13	**Reserved**
	12:0	**Second Field VSync Shift** This value specifies the vertical sync alignment for the start of the interlaced second field, expressed in terms of the absolute pixel number relative to the horizontal active display start. This value will only be used if the transcoder is programmed to an interlaced mode. Typically, the interlaced second field vertical sync should start one pixel after the point halfway between successive horizontal syncs, so the value of this register should be programmed = horizontal sync start - floor[horizontal total / 2] Calculate using the actual horizontal sync start and horizontal total values and not the minus one values programmed into the registers. This vertical sync shift only occurs during the interlaced second field. In all other cases the vertical sync start position is aligned with horizontal sync start.

TRANS_VTOTAL

TRANS_VTOTAL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6000Ch-6000Fh
Name:	Transcoder A Vertical Total
ShortName:	TRANS_VTOTAL_A
Power:	PG2
Reset:	soft
Address:	6100Ch-6100Fh
Name:	Transcoder B Vertical Total
ShortName:	TRANS_VTOTAL_B
Power:	PG2
Reset:	soft
Address:	6200Ch-6200Fh
Name:	Transcoder C Vertical Total
ShortName:	TRANS_VTOTAL_C
Power:	PG2
Reset:	soft
Address:	6E00Ch-6E00Fh
Name:	Transcoder WD0 Vertical Total
ShortName:	TRANS_VTOTAL_WD0
Power:	PG2
Reset:	soft
Address:	6F00Ch-6F00Fh
Name:	Transcoder EDP Vertical Total
ShortName:	TRANS_VTOTAL_EDP

TRANS_VTOTAL

Power:	PG1
Reset:	soft

Address:	6E80Ch-6E80Fh
Name:	Transcoder WD1 Vertical Total
ShortName:	TRANS_VTOTAL_WD1
Power:	PG2
Reset:	soft

Address:	6B00Ch-6B00Fh
Name:	Transcoder DSI 0 Vertical Total
ShortName:	TRANS_VTOTAL_DSI0
Power:	PG1
Reset:	soft

Address:	6B80Ch-6B80Fh
Name:	Transcoder DSI 1 Vertical Total
ShortName:	TRANS_VTOTAL_DSI1
Power:	PG1
Reset:	soft

Restriction
This register should not be changed while the transcoder or port are enabled.

DWord	Bit	Description
0	31:29	**Reserved**
	28:16	**Vertical Total** This field specifies Vertical Total size. This should be equal to the sum of the vertical active and the vertical blank sizes. For progressive display modes, this field is programmed to the number of lines desired minus one. For interlaced display modes, this field is programmed with the number of lines desired minus two. The vertical counter is incremented on the leading edge of the horizontal sync. Both even and odd vertical totals are supported. This field is ignored by WD transcoders. **Restriction** This register must always be programmed to the same value as the Vertical Blank End.
	15:13	**Reserved**
	12:0	**Vertical Active**

TRANS_VTOTAL		
		Description
		This field specifies Vertical Active Display size. The first vertical active display line is considered line number# 0. This field is always programmed to the number of lines desired minus one.
		Restriction : When using the internal panel fitting logic, the minimum vertical active area must be seven lines. This register must always be programmed to the same value as the Vertical Blank Start.

TRANS_WD_FUNC_CTL

TRANS_WD_FUNC_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6E400h-6E403h
Name:	Transcoder WD0 Function Control
ShortName:	TRANS_WD_FUNC_CTL_0
Power:	PG2
Reset:	soft
Address:	6EC00h-6EC03h
Name:	Transcoder WD1 Function Control
ShortName:	TRANS_WD_FUNC_CTL_1
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31	**WD Function Enable** This bit enables the WD function. Value: 0b = Disable; 1b = Enable
	30	**Triggered Capture Mode Enable** This field enables the triggered capture mode where a frame is only captured after the Start Trigger Frame bit is written with 1, and hardware will ignore the transcoder frame time. This must be set before or when WD Function Enable is set. When triggered capture mode is disabled hardware will periodically capture frames following the transcoder frame time. Value: 0b = Disable; 1b = Enable
	29	**Start Trigger Frame**

TRANS_WD_FUNC_CTL

Access:	R/W Set	

Write a 1 to this field to start a software triggered frame capture when Triggered Capture Mode Enable is 1. Hardware will clear the field when the frame starts.

28 Stop Trigger Frame

Access:	R/W Set

Write a 1 to this field to stop a software triggered frame capture when Triggered Capture Mode Enable is 1. Hardware will clear the field when the frame stops. This is only intended for use in case of an error where capture is never completing and software times out.
It must not be set at the same time as Start Trigger Frame.
After a stop trigger, VDenc will be out of sync with WD and also need to be stopped. WD and VDenc then need to start from the same frame number.

27 Reserved

Format:	MBZ

26 Chroma Filtering Enable

This field selects how U and V are downsampled from YUV 444 to 422. This field only applies to the YUV 422 formats.

Value	Name	Description
0	Drop	Drop U2 and V2
1	Filter **[Default]**	Use a 15-34-15 three tap filter

25:23 Reserved

Format:	MBZ

22:20 WD Color Mode

This field selects the capture color format.

Value	Name	Description
000b	YUV 4:4:4	YUV 32-bit 4:4:4 packed (8:8:8:8 MSB-Y:U:X:V)
001b	YUV 4:2:2	YUV 16-bit 4:2:2 packed (8:8:8:8 MSB- Y1:U:Y2:V) Chroma downsampling is programmable according to the Chroma Filtering field.
010b	XYUV 4:4:4	YUV 32-bit 4:4:4 packed (8:8:8:8 MSB-X:Y:U:V)
011b	RGBX	RGBX 32-bit (8:8:8:8 MSB-X:B:G:R)
100b	Y410	YUV 444 10bpc (MSB-X:V:Y:U)
101b	YUY2 8b	8 bit YUV 422 (MSB-V:Y2:U:Y1) Chroma downsampling is programmable

		according to the Chroma Filtering field.
110b	RGB10	RGB1010102 (MSB-X:B:G:R)

Restriction
This field must not be changed while the function is enabled.

19:16 **Reserved**

Format:	MBZ

15 **Reserved**

Format:	MBZ

14:12 **WD Input Select**

These bits determine the input to WD.

Value	Name
000b	Pipe A
101b	Pipe B
110b	Pipe C
Others	Reserved

Restriction
This field must not be changed while the function is enabled. It is not valid to have the same pipes driving multiple enabled transcoders.

11:4 **Reserved**

Format:	MBZ

3:0 **Reserved**

Format:	MBZ

TRNULLDETCT

REG_TEMPLATE - TRNULLDETCT	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	04DE8h
Name:	TiledResources Null Tile Detection Register
ShortName:	TRNULLDETCT

DWord	Bit	Description
0	31:0	**Null Tile Detection Value** Access: R/W **Value** / **Name** / **Description** 00000000h / **[Default]** / A 32bit value programmed to enable h/w to perform a match of TR-VA TT entries to detect Null Tiles. Hardware will flag each entry and space behind it as Null Tile for matched entries.

Unit Level Clock Gating Control 10 for GLV

UCGCTL10_GLV - Unit Level Clock Gating Control 10 for GLV

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	09448h

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31:29	**Reserved** Access: RO Reserved
	28	**Extra Clock Gating Disable** Access: R/W Spare bit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	27	**vsr Clock Gating Disable** Access: R/W Spare bit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	26	**vfr Clock Gating Disable** Access: R/W Spare bit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	25	**svgr Clock Gating Disable**

UCGCTL10_GLV - Unit Level Clock Gating Control 10 for GLV

	Access:	R/W

Spare bit Clock Gating Disable Control:
'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)

24 **OVR Clock Gating Disable**

Access:	R/W

Spare bit Clock Gating Disable Control:
'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)

23 **HTQ Clock Gating Disable**

Access:	R/W

HTQ Clock Gating Disable Control:
'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)

22 **HSSE RAM Clock Gating Disable**

Access:	R/W

HSSE RAM Clock Gating Disable Control:
'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)

21 **HSSE Clock Gating Disable**

Access:	R/W

HSSE Clock Gating Disable Control:
'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)

20 **HSAO RAM Clock Gating Disable**

UCGCTL10_GLV - Unit Level Clock Gating Control 10 for GLV

	Access:	R/W

HSAO RAM Clock Gating Disable Control:
'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)

19 **HSAO Clock Gating Disable**

Access:	R/W

HSAO Clock Gating Disable Control:
'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)

18 **MSQC 1X Clock Gating Disable**

Access:	R/W

MSQC unit 1X Clock Gating Disable Control:
'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)

17 **MSQC 2X Clock Gating Disable**

Access:	R/W

MSQC unit 2X Clock Gating Disable Control:
'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)

16 **HWOP unit Clock Gating Disable**

Access:	R/W

hwop unit Clock Gating Disable Control:
'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)

15 **RAM hvdl1 unit Clock Gating Disable**

Access:	R/W

UCGCTL10_GLV - Unit Level Clock Gating Control 10 for GLV

		hvdl1 unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	14	**hvdl1 unit Clock Gating Disable** Access: R/W hvdl1 unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	13	**hmdc unit Clock Gating Disable** Access: R/W hmdc unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	12	**rdob unit Clock Gating Disable** Access: R/W rdob unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	11	**rdof unit Clock Gating Disable** Access: R/W rdof unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	10	**hcrei unit Clock Gating Disable** Access: R/W hcrei unit Clock Gating Disable Control:

UCGCTL10_GLV - Unit Level Clock Gating Control 10 for GLV

		'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	9	**hcref unit Clock Gating Disable** Access: R/W hcref unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	8	**hcres unit Clock Gating Disable** Access: R/W hcres unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	7	**himeunit Clock Gating Disable** Access: R/W hime unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	6	**SVGR unit Clock Gating Disable** Access: R/W svgr unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	5	**VFR unit Clock Gating Disable** Access: R/W vfr unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for

UCGCTL10_GLV - Unit Level Clock Gating Control 10 for GLV

		functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	4	**SFR unit Clock Gating Disable** Access: R/W sfr unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	3	**CLR unit Clock Gating Disable** Access: R/W clr unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	2	**OVR unit Clock Gating Disable** Access: R/W ovr unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	1	**POCS Clock Gating Disable** Access: R/W pocs unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.;(i.e., clocks are toggling, always)
	0	**VSRBE/VSRFE Clock Gating Disable** Access: R/W vsr*eunit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.;(i.e., clocks are toggling, always)

Unslice unit Level Clock Gating Control 9440

UNSLCGCTL9440 - Unslice unit Level Clock Gating Control 9440

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	09440h

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31:26	**Reserved** Access: R/W Reserved
	25	**gamdrtnunit Clock Gating Disable** Default Value: 1b Access: R/W gamdrtnunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	24	**gamdmrtnunit Clock Gating Disable** Default Value: 1b Access: R/W gamdmrtnunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	23	**gamdmunit Clock Gating Disable** Default Value: 1b Access: R/W gamdmunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for

UNSLCGCTL9440 - Unslice unit Level Clock Gating Control 9440

		functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	22	**gamtm2unit Clock Gating Disable** Default Value: 1b Access: R/W gamtm2unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	21	**gamtm1unit Clock Gating Disable** Default Value: 1b Access: R/W gamtm1unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	20	**SPARE Clock Gating Disable2** Access: R/W SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	19	**SPARE Clock Gating Disable1** Access: R/W SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	18	**SPARE Clock Gating Disable0** Access: R/W SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

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17	**SWRBLK_2x Clock Gating Disable** Access: R/W Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
16	**SWRBLK_WMF Clock Gating Disable** Access: R/W Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
15	**SWRBLK_VF Clock Gating Disable** Access: R/W Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
14	**GAF2XRT Clock Gating Disable** Access: R/W Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
13	**GAF2X Clock Gating Disable** Access: R/W Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
12	**GATRW Clock Gating Disable** Access: R/W Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for

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		functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	11	**GATR Clock Gating Disable** Access: R/W Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	10	**GACFG Clock Gating Disable** Access: R/W CACFG Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	9	**GAVARBunit Clock Gating Disable** Access: R/W GAVARBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	8	**GAMTOunit Clock Gating Disable** Access: R/W GAMTOunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	7	**GAMTGunit Clock Gating Disable** Access: R/W GAMTGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	6	**MARBunit Clock Gating Disable** Access: R/W MARBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for

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		functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	5	**GAMWDunit Clock Gating Disable** Access: R/W GAMWDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	4	**GAMVTunit Clock Gating Disable** Access: R/W GAMVTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	3	**L3_CR Clock Gating Disable** Access: R/W L3_CR Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	2	**GACBunit Clock Gating Disable** Access: R/W GACBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	1	**ramdft Clock Gating Disable** Access: R/W ramdft Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	0	**hwmunit Clock Gating Disable** Access: R/W hwmunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for

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		functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Unslice unit Level Clock Gating Control 9444

UNSLCGCTL9444 - Unslice unit Level Clock Gating Control 9444

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	09444h

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31:8	**Reserved** Access: R/W
	7:4	**Reserved** Access: R/W
	3	**KCRunit Clock Gating Disable** Access: R/W KCRunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	2	**WCRunit Clock Gating Disable** Access: R/W WCRunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	1	**lsnunit Clock Gating Disable** Access: R/W lsnunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	0	**warbunit Clock Gating Disable** Access: R/W

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		warbunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Unslice unit Level Clock Gating Control 9448

UNSLCGCTL9448 - Unslice unit Level Clock Gating Control 9448

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	09448h

Unslice unit Level Clock Gating Control 9448 Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31:11	**Reserved** Access: R/W Reserved
	10	**ram vsr unit Clock Gating Disable** Access: R/W This is added for POSH feature. vsr unit Clock Gating Disable Control for ram: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	9	**ram vfr unit Clock Gating Disable** Access: R/W This is added for POSH feature. vfr unit Clock Gating Disable Control for ram: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	8	**ram svgr unit Clock Gating Disable** Access: R/W This is added for POSH feature. svgr unit Clock Gating Disable Control for ram: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	7	**ram ovr unit Clock Gating Disable**

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	Access:	R/W

This is added for POSH feature. ovr unit Clock Gating Disable Control for ram:
'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)

6 **svgr unit Clock Gating Disable**

Access:	R/W

This is added for POSH feature. svgr unit Clock Gating Disable Control:
'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)

5 **vfr unit Clock Gating Disable**

Access:	R/W

This is added for POSH feature. vfr unit Clock Gating Disable Control:
'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)

4 **sfr unit Clock Gating Disable**

Access:	R/W

This is added for POSH feature. sfr unit Clock Gating Disable Control:
'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)

3 **clr unit Clock Gating Disable**

Access:	R/W

This is added for POSH feature. clr unit Clock Gating Disable Control:
'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)

2 **ovr unit Clock Gating Disable**

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		Access: R/W This is added for POSH feature. ovr unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	1	**pocs unit Clock Gating Disable** Access: R/W This is added for POSH feature. pocs unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	0	**vsr unit Clock Gating Disable** Access: R/W This is added for POSH feature. vsr unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)

Unslice unit Level Clock Gating Control 9450

UNSLCGCTL9450 - Unslice unit Level Clock Gating Control 9450

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	09450h

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31	**TDSunit Clock Gating Disable** Access: R/W TDSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	30	**VFunit Clock Gating Disable** Access: R/W VFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	29	**URBunit Clock Gating Disable** Access: R/W URBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	28	**GAMWunit Clock Gating Disable** Access: R/W GAMWunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

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27	**SVGunit Clock Gating Disable** Access: R/W SVGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
26	**RCPBEunit Clock Gating Disable** Access: R/W RCPBEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
25	**GAMunit Clock Gating Disable** Access: R/W GAMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
24	**HDCunit Clock Gating Disable** Access: R/W HDCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
23	**CSunit Clock Gating Disable** Access: R/W CSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
22	**BLBunit Clock Gating Disable** Access: R/W BLBunit Clock Gating Disable Control:

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		'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	21	**BFunit Clock Gating Disable** Access: R/W BFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	20	**MUCunit Clock Gating Disable** Access: R/W MUCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	19	**WVISunit Clock Gating Disable** Access: R/W WVISunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	18	**WAVM Clock Gating Disable** Access: R/W WAVM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	17	**WHME Clock Gating Disable** Access: R/W WHME Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	16	**WIME Clock Gating Disable** Access: R/W WIME Clock Gating Disable Control:

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		'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	15	**WMPC Clock Gating Disable** Access: R/W WMPC Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	14	**SDEunit Clock Gating Disable** Access: R/W SDEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	13	**VSHM Clock Gating Disable** Access: R/W VSHM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	12	**DAPRTS Clock Gating Disable** Access: R/W DAPRTS Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	11	**GS Clock Gating Disable** Access: R/W GS Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	10	**Reserved**

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	9	**GAMTunit Clock Gating Disable** Access: R/W GAMTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	8	**RSunit Clock Gating Disable** Access: R/W RSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	7	**HSunit Clock Gating Disable** Access: R/W HSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	6	**gamdunit Clock Gating Disable** Access: R/W gamdunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	5	**vdlunit1 Clock Gating Disable** Access: R/W vdlunit1 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	4	**vhmeunit Clock Gating Disable** Access: R/W

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		vhmeunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	3	**vcreunit Clock Gating Disable** Access: R/W vcreunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	2	**hleunit Clock Gating Disable** Access: R/W hleunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	1	**mbdunit Clock Gating Disable** Access: R/W mbdunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	0	**mmxunit Clock Gating Disable** Access: R/W mmxunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Unslice unit Level Clock Gating Control 9454

UNSLCGCTL9454 - Unslice unit Level Clock Gating Control 9454		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	09454h	
Unit Level Clock Gating Disable bits		
DWord	**Bit**	**Description**
0	31:22	**Reserved** Access: R/W Reserved
	21	**SPARE Clock Gating Disable2** Access: R/W SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	20	**ram gamtm2 unit Clock Gating Disable** Access: R/W gamtm2 unit Clock Gating Disable Control for ram: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	19	**ram gamtm1 unit Clock Gating Disable** Access: R/W gamtm1 unit Clock Gating Disable Control for ram: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	18	**VDIunit Clock Gating Disable** Access: R/W VDIunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)

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		'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	17	**GATRWunit Clock Gating Disable** Access: R/W GATRWunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	16	**GATRunit Clock Gating Disable** Access: R/W GATRunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	15	**GAMVTDunit Clock Gating Disable** Access: R/W GAMVTDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	14	**GAMWDunit Clock Gating Disable** Access: R/W GAMWDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	13	**GAMTGunit Clock Gating Disable** Access: R/W GAMTGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

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	12	**GAMTOunit Clock Gating Disable** Access: R/W GAMTOunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	11	**SolLunit Clock Gating Disable** Access: R/W SolLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	10	**VSUnit Clock Gating Disable** Access: R/W VSUnit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	9	**mpdunit Clock Gating Disable** Access: R/W mpdunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	8	**hedunit Clock Gating Disable** Access: R/W hedunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	7	**hlfunit Clock Gating Disable** Access: R/W hlfunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)

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		'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	6	**hmcunit Clock Gating Disable** Access: R/W hmcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	5	**hmxunit Clock Gating Disable** Access: R/W hmxunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	4	**hppunit Clock Gating Disable** Access: R/W hppunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	3	**hprunit Clock Gating Disable** Access: R/W hprunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	2	**Reserved**
	1	**hwmunit Clock Gating Disable** Access: R/W hwmunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	0	**mdcunit Clock Gating Disable** Access: R/W mdcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for

UNSLCGCTL9454 - Unslice unit Level Clock Gating Control 9454		
		functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UTIL_PIN_BUF_CTL

UTIL_PIN_BUF_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	48404h-48407h
Name:	Utility Pin Buffer Control
ShortName:	UTIL_PIN_BUF_CTL
Power:	PG0
Reset:	soft

This register controls the display utility pin I/O buffer.

DWord	Bit	Description
0	31:30	**Reserved**
	29:28	**Hysteresis**
	27	**Reserved**
	26:24	**Spare**
	23:21	**Reserved**
	20:16	**Pulldown Strength**
	15:12	**Pulldown Slew**
	11:9	**Reserved**
	8:4	**Pullup Strength**
	3:0	**Pullup Slew**

UTIL_PIN_CTL

UTIL_PIN_CTL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	48400h-48403h
Name:	Utility Pin Control
ShortName:	UTIL_PIN_CTL
Power:	PG0
Reset:	soft

This register controls the display utility pin. The nominal supply is 1 Volt and can be level shifted depending on usage. The maximum switching frequency is 100 KHz.

DWord	Bit	Description
0	31	**Util Pin Enable** This bit enables the utility pin. Value / Name: 0b – Disable 1b – Enable
	30:29	**Pipe Select** This bit selects which pipe will be used when the utility pin is outputting timing related signals. Value / Name: 00b – Pipe A 01b – Pipe B 10b – Pipe C Restriction: The field should only be changed when the utility pin is disabled or not configured to use any timing signals.
	28	**Reserved**
	27:24	**Util Pin Mode** This bit configures the utility pin mode of operation for output. Value / Name / Description: 0000b – Data – Output the Util_Pin_Output_Data value.

0001b	PWM	Output from the backlight PWM circuit.
0100b	Vblank	Output the vertical blank.
0101b	Vsync	Output the vertical sync.
1000b	Right/Left Eye Level	Output the stereo 3D right/left eye level signal. Asserted for the left eye and de-asserted for the right eye.
Others	Reserved	Reserved

Restriction
The field should only be changed when the utility pin is disabled.

23 Util Pin Output Data

This bit selects what the value to drive as an output when in the data mode.

Value	Name
0b	0
1b	1

22 Util Pin Output Polarity

This bit inverts the polarity of the pin output.

Value	Name
0b	Not inverted
1b	Inverted

21:20 Reserved

19 Util Pin Direction

This bit selects whether the pin is used as an output or an input.

Value	Name
0b	Output
1b	Input

Restriction
The field should only be changed when the utility pin is disabled.

18:17 Reserved

16 Util Pin Input Data

Access:	RO

This bit gives the value received on the pin. This is only valid when the utility pin is enabled and the direction is input.

15:0 Reserved

VCW Clock Count

VCW_CLOCK_CNT - VCW Clock Count	
Register Space:	MMIO: 0/2/0
Source:	VideoEnhancementCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1CA020h
ShortName:	VCW_CLOCK_CNT_VECS0
Address:	1DA020h
ShortName:	VCW_CLOCK_CNT_VECS1
Address:	1EA020h
ShortName:	VCW_CLOCK_CNT_VECS2
Address:	1FA020h
ShortName:	VCW_CLOCK_CNT_VECS3

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:0	**Max clock count** Default Value: 0h Maximum number of clocks taken by VCW to process a column

VCW Internal Latency

VCW_INTERNAL_LAT - VCW Internal Latency

Register Space:	MMIO: 0/2/0
Source:	VideoEnhancementCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1CA024h
ShortName:	VCW_INTERNAL_LAT_VECS0
Address:	1DA024h
ShortName:	VCW_INTERNAL_LAT_VECS1
Address:	1EA024h
ShortName:	VCW_INTERNAL_LAT_VECS2
Address:	1FA024h
ShortName:	VCW_INTERNAL_LAT_VECS3

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:0	**VCW internal data latency count** Default Value: 0h

VCW Min Max Latency

VCW_MINMAX_LAT - VCW Min Max Latency

Register Space:	MMIO: 0/2/0
Source:	VideoEnhancementCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1CA028h
ShortName:	VCW_MINMAX_LAT_VECS0
Address:	1DA028h
ShortName:	VCW_MINMAX_LAT_VECS1
Address:	1EA028h
ShortName:	VCW_MINMAX_LAT_VECS2
Address:	1FA028h
ShortName:	VCW_MINMAX_LAT_VECS3

DWord	Bit	Description
0	31:16	**Current request count** Default Value: 0h
	15:8	**Max latency** Default Value: 0h Maximum number of clocks taken for tag 200h
	7:0	**Min latency** Default Value: 0h Minimum number of clocks taken for tag 200h

VCW Total Latency

VCW_TOTAL_LAT - VCW Total Latency

Register Space:	MMIO: 0/2/0
Source:	VideoEnhancementCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1CA02Ch
ShortName:	VCW_TOTAL_LAT_VECS0
Address:	1DA02Ch
ShortName:	VCW_TOTAL_LAT_VECS1
Address:	1EA02Ch
ShortName:	VCW_TOTAL_LAT_VECS2
Address:	1FA02Ch
ShortName:	VCW_TOTAL_LAT_VECS3

DWord	Bit	Description
0	31:0	**Total latency** Default Value: 0h Accumumation of latency per frame for tag 200h

VCW XY position

VCW_XY_POS - VCW XY position

Register Space:	MMIO: 0/2/0
Source:	VideoEnhancementCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1CA030h
ShortName:	VCW_XY_POS_VECS0
Address:	1DA030h
ShortName:	VCW_XY_POS_VECS1
Address:	1EA030h
ShortName:	VCW_XY_POS_VECS2
Address:	1FA030h
ShortName:	VCW_XY_POS_VECS3

DWord	Bit	Description
0	31:16	**Current Y value** Default Value: 0h Current Y position of VCW walker
	15:0	**Current X value** Default Value: 0h Current X position of VCW walker

Vdbox Power Context Save request

VDCGCTL3F00 - Vdbox Power Context Save request	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	1C3F00h-1C3F03h
Name:	VDbox registers1
ShortName:	VDCGCTL3F00_VDBOX0
Address:	1C7F00h-1C7F03h
Name:	VDbox registers1
ShortName:	VDCGCTL3F00_VDBOX1
Address:	1D3F00h-1D3F03h
Name:	VDbox registers1
ShortName:	VDCGCTL3F00_VDBOX2
Address:	1D7F00h-1D7F03h
Name:	VDbox registers1
ShortName:	VDCGCTL3F00_VDBOX3
Address:	1E3F00h-1E3F03h
Name:	VDbox registers1
ShortName:	VDCGCTL3F00_VDBOX4
Address:	1E7F00h-1E7F03h
Name:	VDbox registers1
ShortName:	VDCGCTL3F00_VDBOX5
Address:	1F3F00h-1F3F03h
Name:	VDbox registers1
ShortName:	VDCGCTL3F00_VDBOX6
Address:	1F7F00h-1F7F03h
Name:	VDbox registers1
ShortName:	VDCGCTL3F00_VDBOX7

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO Message Mask bots for lower 16 bits

VDCGCTL3F00 - Vdbox Power Context Save request

	15:10	**Reserved** Access: RO Reserved
	9	**Power context save request** Access: R/W Set Power Context Save Request 1'b0 : Power context save is not being requested 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

Vdbox unit Level Clock Gating Control 3F0C

VDCGCTL3F0C - Vdbox unit Level Clock Gating Control 3F0C	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	1C3F0Ch-1C3F0Fh
Name:	VDbox registers4
ShortName:	VDCGCTL3F0C_VDBOX0
Address:	1C7F0Ch-1C7F0Fh
Name:	VDbox registers4
ShortName:	VDCGCTL3F0C_VDBOX1
Address:	1D3F0Ch-1D3F0Fh
Name:	VDbox registers4
ShortName:	VDCGCTL3F0C_VDBOX2
Address:	1D7F0Ch-1D7F0Fh
Name:	VDbox registers4
ShortName:	VDCGCTL3F0C_VDBOX3
Address:	1E3F0Ch-1E3F0Fh
Name:	VDbox registers4
ShortName:	VDCGCTL3F0C_VDBOX4
Address:	1E7F0Ch-1E7F0Fh
Name:	VDbox registers4
ShortName:	VDCGCTL3F0C_VDBOX5
Address:	1F3F0Ch-1F3F0Fh
Name:	VDbox registers4
ShortName:	VDCGCTL3F0C_VDBOX6
Address:	1F7F0Ch-1F7F0Fh
Name:	VDbox registers4
ShortName:	VDCGCTL3F0C_VDBOX7
Unit Level Clock Gating Disable bits	

DWord	Bit	Description
0	31	**SPARE Clock Gating Disable12** Access: R/W SPARE Clock Gating Disable Control:

VDCGCTL3F0C - Vdbox unit Level Clock Gating Control 3F0C

		'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	30	**SPARE Clock Gating Disable11** Access: R/W SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	29	**SPARE Clock Gating Disable10** Access: R/W SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	28	**SPARE Clock Gating Disable9** Access: R/W SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	27	**VNCunit Clock Gating Disable** Access: R/W VNCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	26	**VMXunit Clock Gating Disable** Access: R/W VMXunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	25	**VMTSunit Clock Gating Disable** Access: R/W VMTSunit Clock Gating Disable Control:

VDCGCTL3F0C - Vdbox unit Level Clock Gating Control 3F0C

		'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	24	**VMPCunit Clock Gating Disable** Access: R/W VMPCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	23	**VMDunit Clock Gating Disable** Access: R/W VMDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	22	**VMCRunit Clock Gating Disable** Default Value: 1b Access: R/W VMCRunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	21	**VMCunit Clock Gating Disable** Access: R/W VMCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	20	**VMBunit Clock Gating Disable** Access: R/W VMBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	19	**VLFunit Clock Gating Disable** Access: R/W

VDCGCTL3F0C - Vdbox unit Level Clock Gating Control 3F0C

		VLFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	18	**VITunit Clock Gating Disable** Access: R/W VITunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	17	**VISunit Clock Gating Disable** Access: R/W VISunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	16	**VIPunit Clock Gating Disable** Access: R/W VIPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	15	**VID6 Clock Gating Disable** Access: R/W VID6 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	14	**VID5 Clock Gating Disable** Access: R/W VID5 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	13	**VID4 Clock Gating Disable** Access: R/W

VDCGCTL3F0C - Vdbox unit Level Clock Gating Control 3F0C

		VID4 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	12	**VID3 Clock Gating Disable** Access: R/W VID3 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	11	**VID2 Clock Gating Disable** Access: R/W VID2 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	10	**VID1 Clock Gating Disable** Access: R/W VID1 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	9	**VIMEunit Clock Gating Disable** Access: R/W VIMEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	8	**VHRunit's Clock Gating Disable** Access: R/W VHRunit's Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	7	**VHMEunit Clock Gating Disable** Access: R/W

VDCGCTL3F0C - Vdbox unit Level Clock Gating Control 3F0C

		VHMEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	6	**VFTunit Clock Gating Disable** Access: R/W VFTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	5	**VDXunit Clock Gating Disable** Access: R/W VDXunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	4	**VDSunit Clock Gating Disable** Access: R/W VDSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	3	**vdl1unit Clock Gating Disable** Access: R/W vdl1unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	2	**Csunit's Clock Gating Disable** Access: R/W Csunit's Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	1	**VCREunit Clock Gating Disable** Access: R/W

VDCGCTL3F0C - Vdbox unit Level Clock Gating Control 3F0C

		VCREunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	0	**VCPunit Clock Gating Disable** Access: R/W VCPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Vdbox unit Level Clock Gating Control 3F04

VDCGCTL3F04 - Vdbox unit Level Clock Gating Control 3F04	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	1C3F04h-1C3F07h
Name:	VDbox registers2
ShortName:	VDCGCTL3F04_VDBOX0
Address:	1C7F04h-1C7F07h
Name:	VDbox registers2
ShortName:	VDCGCTL3F04_VDBOX1
Address:	1D3F04h-1D3F07h
Name:	VDbox registers2
ShortName:	VDCGCTL3F04_VDBOX2
Address:	1D7F04h-1D7F07h
Name:	VDbox registers2
ShortName:	VDCGCTL3F04_VDBOX3
Address:	1E3F04h-1E3F07h
Name:	VDbox registers2
ShortName:	VDCGCTL3F04_VDBOX4
Address:	1E7F04h-1E7F07h
Name:	VDbox registers2
ShortName:	VDCGCTL3F04_VDBOX5
Address:	1F3F04h-1F3F07h
Name:	VDbox registers2
ShortName:	VDCGCTL3F04_VDBOX6
Address:	1F7F04h-1F7F07h
Name:	VDbox registers2
ShortName:	VDCGCTL3F04_VDBOX7
Unit Level Clock Gating Disable bits	

DWord	Bit	Description
0	31	**spare Clock Gating Disable4** Access: R/W SPARE Clock Gating Disable Control:

VDCGCTL3F04 - Vdbox unit Level Clock Gating Control 3F04

		'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	30	**spare Clock Gating Disable3** Access: R/W SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	29	**spare Clock Gating Disable2** Access: R/W SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	28	**HVSHAREunit Clock Gating Disable** Access: R/W HVSHAREunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	27	**HFTunit Clock Gating Disable** Access: R/W HFTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	26	**HFQunit Clock Gating Disable** Access: R/W HFQunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	25	**HCRESunit Clock Gating Disable** Access: R/W

VDCGCTL3F04 - Vdbox unit Level Clock Gating Control 3F04

		HCRESunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	24	**HCREIunit Clock Gating Disable** Access: R/W HCREIunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	23	**HCREFunit Clock Gating Disable** Access: R/W HCREFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	22	**MEDunit Clock Gating Disable** Access: R/W MEDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	21	**GACXunit Clock Gating Disable** Access: R/W GACXunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	20	**GACunit Clock Gating Disable** Access: R/W GACunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	19	**ECPunit Clock Gating Disable** Access: R/W

VDCGCTL3F04 - Vdbox unit Level Clock Gating Control 3F04

		ECPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	18	**BSPunit Clock Gating Disable** Access: R/W BSPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	17	**vmmunit Clock Gating Disable** Access: R/W vmmunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	16	**VHLFunit Clock Gating Disable** Access: R/W VHLFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	15	**VDKMXunit Clock Gating Disable** Access: R/W VDKMXunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	14	**HWMunit Clock Gating Disable** Access: R/W HWMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	13	**Reserved**
	12	**Reserved**

VDCGCTL3F04 - Vdbox unit Level Clock Gating Control 3F04

	11	**HSSEunit Clock Gating Disable** Access: R/W HSSEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	10	**HSFunit Clock Gating Disable** Access: R/W HSFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	9	**HPRunit Clock Gating Disable** Access: R/W HPRunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	8	**HPPunit Clock Gating Disable** Access: R/W HPPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	7	**HMXFunit Clock Gating Disable** Access: R/W HMXFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	6	**HMXBunit Clock Gating Disable** Access: R/W HMXBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

VDCGCTL3F04 - Vdbox unit Level Clock Gating Control 3F04

	5	**HMCunit Clock Gating Disable** Access: R/W HMCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	4	**HITunit Clock Gating Disable** Access: R/W HITunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	3	**HHLFunit Clock Gating Disable** Access: R/W HHLFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	2	**HFCunit Clock Gating Disable** Access: R/W HFCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	1	**HEDunit Clock Gating Disable** Access: R/W HEDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	0	**HBEunit Clock Gating Disable** Access: R/W HBEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Vdbox unit Level Clock Gating Control 3F08

VDCGCTL3F08 - Vdbox unit Level Clock Gating Control 3F08	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	1C3F08h-1C3F0Bh
Name:	VDbox registers3
ShortName:	VDCGCTL3F08_VDBOX0
Address:	1C7F08h-1C7F0Bh
Name:	VDbox registers3
ShortName:	VDCGCTL3F08_VDBOX1
Address:	1D3F08h-1D3F0Bh
Name:	VDbox registers3
ShortName:	VDCGCTL3F08_VDBOX2
Address:	1D7F08h-1D7F0Bh
Name:	VDbox registers3
ShortName:	VDCGCTL3F08_VDBOX3
Address:	1E3F08h-1E3F0Bh
Name:	VDbox registers3
ShortName:	VDCGCTL3F08_VDBOX4
Address:	1E7F08h-1E7F0Bh
Name:	VDbox registers3
ShortName:	VDCGCTL3F08_VDBOX5
Address:	1F3F08h-1F3F0Bh
Name:	VDbox registers3
ShortName:	VDCGCTL3F08_VDBOX6
Address:	1F7F08h-1F7F0Bh
Name:	VDbox registers3
ShortName:	VDCGCTL3F08_VDBOX7
Unit Level Clock Gating Disable bits	

DWord	Bit	Description
0	31	**SPARE Clock Gating Disable8** Access: R/W SPARE Clock Gating Disable Control:

VDCGCTL3F08 - Vdbox unit Level Clock Gating Control 3F08

	'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
30	**SPARE Clock Gating Disable7** Access: R/W SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
29	**SPARE Clock Gating Disable6** Access: R/W SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
28	**spare Clock Gating Disable5** Access: R/W SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
27	**VClunit Clock Gating Disable** Access: R/W VClunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
26	**VCDunit Clock Gating Disable** Access: R/W VCDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
25	**vbspunit Clock Gating Disable** Access: R/W vbspunit Clock Gating Disable Control:

VDCGCTL3F08 - Vdbox unit Level Clock Gating Control 3F08

		'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	24	**VBPunits Clock Gating Disable** Access: R/W VBPunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	23	**VAMunit Clock Gating Disable** Access: R/W VAMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	22	**VADuit Clock Gating Disable** Access: R/W VADuit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	21	**VACunit Clock Gating Disable** Access: R/W VACunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	20	**USBunit Clock Gating Disable** Access: R/W USBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	19	**SECunit Clock Gating Disable** Access: R/W SECunit Clock Gating Disable Control:

VDCGCTL3F08 - Vdbox unit Level Clock Gating Control 3F08

		'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	18	**RDOFunit Clock Gating Disable** Access: R/W RDOFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	17	**RDOBunit Clock Gating Disable** Access: R/W RDOBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	16	**QRCunit Clock Gating Disable** Access: R/W QRCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	15	**MEDunit Clock Gating Disable** Access: R/W MEDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	14	**MPCunit Clock Gating Disable** Access: R/W MPCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	13	**MDCunit Clock Gating Disable** Access: R/W MDCunit Clock Gating Disable Control:

VDCGCTL3F08 - Vdbox unit Level Clock Gating Control 3F08

		'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	12	**jusbunit Clock Gating Disable** Access: R/W jusbunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	11	**JPGunit Clock Gating Disable** Access: R/W JPGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	10	**HWOPunit Clock Gating Disable** Access: R/W HWOPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	9	**HVDL1unit Clock Gating Disable** Access: R/W HVDL1unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	8	**HVDunit Clock Gating Disable** Access: R/W HVDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	7	**HTQunit Clock Gating Disable** Access: R/W

VDCGCTL3F08 - Vdbox unit Level Clock Gating Control 3F08

		HTQunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	6	**HSAOunit Clock Gating Disable** Access: R/W HSAOunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	5	**HRSunit Clock Gating Disable** Access: R/W HRSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	4	**HPOunit Clock Gating Disable** Access: R/W HPOunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	3	**HMDCunit Clock Gating Disable** Access: R/W HMDCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	2	**HLEunit Clock Gating Disable** Access: R/W HLEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	1	**HLCunit Clock Gating Disable** Access: R/W

VDCGCTL3F08 - Vdbox unit Level Clock Gating Control 3F08		
		HLCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	0	**HIMEunit Clock Gating Disable** Access: R/W HIMEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Vdbox unit Level Clock Gating Control 3F10

VDCGCTL3F10 - Vdbox unit Level Clock Gating Control 3F10	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	1C3F10h-1C3F13h
Name:	VDbox registers5
ShortName:	VDCGCTL3F10_VDBOX0
Address:	1C7F10h-1C7F13h
Name:	VDbox registers5
ShortName:	VDCGCTL3F10_VDBOX1
Address:	1D3F10h-1D3F13h
Name:	VDbox registers5
ShortName:	VDCGCTL3F10_VDBOX2
Address:	1D7F10h-1D7F13h
Name:	VDbox registers5
ShortName:	VDCGCTL3F10_VDBOX3
Address:	1E3F10h-1E3F13h
Name:	VDbox registers5
ShortName:	VDCGCTL3F10_VDBOX4
Address:	1E7F10h-1E7F13h
Name:	VDbox registers5
ShortName:	VDCGCTL3F10_VDBOX5
Address:	1F3F10h-1F3F13h
Name:	VDbox registers5
ShortName:	VDCGCTL3F10_VDBOX6
Address:	1F7F10h-1F7F13h
Name:	VDbox registers5
ShortName:	VDCGCTL3F10_VDBOX7

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31:11	**Reserved**

VDCGCTL3F10 - Vdbox unit Level Clock Gating Control 3F10

	Access:	R/W

10	**hmxbrouterunit Clock Gating Disable**
	Access: R/W
	hmxbrouterunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
9	**RAMDFTunit Clock Gating Disable**
	Access: R/W
	RAMDFTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
8	**VWOPunit Clock Gating Disable**
	Access: R/W
	VWOPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
7	**SWPunit Clock Gating Disable**
	Access: R/W
	SWPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
6	**VTQunit Clock Gating Disable**
	Access: R/W
	VTQunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
5	**VSLunit Clock Gating Disable**
	Access: R/W
	VSLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for

VDCGCTL3F10 - Vdbox unit Level Clock Gating Control 3F10

		functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	4	**VSECunit Clock Gating Disable** Access: R/W VSECunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	3	**VRTunit Clock Gating Disable** Access: R/W VRTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	2	**VPRunit Clock Gating Disable** Access: R/W VPRunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	1	**VOPunit Clock Gating Disable** Access: R/W VOPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	0	**VNEunit Clock Gating Disable** Access: R/W VNEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Vdbox unit Level Clock Gating Control 3F14

VDCGCTL3F14 - Vdbox unit Level Clock Gating Control 3F14	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	1C3F14h-1C3F17h
Name:	VDbox registers6
ShortName:	VDCGCTL3F14_VDBOX0
Address:	1C7F14h-1C7F17h
Name:	VDbox registers6
ShortName:	VDCGCTL3F14_VDBOX1
Address:	1D3F14h-1D3F17h
Name:	VDbox registers6
ShortName:	VDCGCTL3F14_VDBOX2
Address:	1D7F14h-1D7F17h
Name:	VDbox registers6
ShortName:	VDCGCTL3F14_VDBOX3
Address:	1E3F14h-1E3F17h
Name:	VDbox registers6
ShortName:	VDCGCTL3F14_VDBOX4
Address:	1E7F14h-1E7F17h
Name:	VDbox registers6
ShortName:	VDCGCTL3F14_VDBOX5
Address:	1F3F14h-1F3F17h
Name:	VDbox registers6
ShortName:	VDCGCTL3F14_VDBOX6
Address:	1F7F14h-1F7F17h
Name:	VDbox registers6
ShortName:	VDCGCTL3F14_VDBOX7

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31	**VDIunit Clock Gating Disable** Access: R/W VDIunit Clock Gating Disable Control:

VDCGCTL3F14 - Vdbox unit Level Clock Gating Control 3F14

		'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	30	**SFMunit Clock Gating Disable1** Access: R/W SFMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	29	**SFEunit Clock Gating Disable1** Access: R/W SFEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	28	**SFDunits Clock Gating Disable1** Access: R/W SFDunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	27	**SFAunit Clock Gating Disable1** Access: R/W SFAunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	26	**VEOunit Clock Gating Disable** Access: R/W VEOunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	25	**VNCunit Clock Gating Disable** Access: R/W VNCunit Clock Gating Disable Control:

VDCGCTL3F14 - Vdbox unit Level Clock Gating Control 3F14

		'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	24	**VMXunit Clock Gating Disable** Access: R/W VMXunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	23	**vmpcunit Clock Gating Disable** Access: R/W vmpcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	22	**vmmunit Clock Gating Disable** Access: R/W vmmunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	21	**VMCunit Clock Gating Disable** Access: R/W VMCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	20	**VLFunit Clock Gating Disable** Access: R/W VLFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	19	**VISunit Clock Gating Disable** Access: R/W VISunit Clock Gating Disable Control:

VDCGCTL3F14 - Vdbox unit Level Clock Gating Control 3F14

		'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	18	**vhmeunit Clock Gating Disable** Access: R/W vhmeunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	17	**vhlfunit Clock Gating Disable** Access: R/W vhlfunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	16	**VCWunit Clock Gating Disable** Access: R/W VCWunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	15	**vcreunit Clock Gating Disable** Access: R/W vcreunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	14	**USBunit Clock Gating Disable** Access: R/W USBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	13	**QRCunit Clock Gating Disable** Access: R/W QRCunit Clock Gating Disable Control:

VDCGCTL3F14 - Vdbox unit Level Clock Gating Control 3F14

		'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	12	**MPCunit Clock Gating Disable** Access: R/W MPCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	11	**mdcunit Clock Gating Disable** Access: R/W mdcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	10	**HWMunit Clock Gating Disable** Access: R/W HWMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	9	**IECPuit Clock Gating Disable** Access: R/W IECPuit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	8	**HVDunit Clock Gating Disable** Access: R/W HVDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	7	**Reserved**
	6	**Reserved**
	5	**HTQunit Clock Gating Disable**

VDCGCTL3F14 - Vdbox unit Level Clock Gating Control 3F14

		Access: R/W HTQunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	4	**HSAOunit Clock Gating Disable** Access: R/W HSAOunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	3	**HPRunit Clock Gating Disable** Access: R/W HPRunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	2	**HPPunit Clock Gating Disable** Access: R/W HPPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	1	**HHLFunit Clock Gating Disable** Access: R/W HHLFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	0	**HFCunit Clock Gating Disable** Access: R/W HFCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Vdbox unit Level Clock Gating Control 3F18

VDCGCTL3F18 - Vdbox unit Level Clock Gating Control 3F18	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	1C3F18h-1C3F1Bh
Name:	VDbox registers6
ShortName:	VDCGCTL3F18_VDBOX0
Address:	1C7F18h-1C7F1Bh
Name:	VDbox registers6
ShortName:	VDCGCTL3F18_VDBOX1
Address:	1D3F18h-1D3F1Bh
Name:	VDbox registers6
ShortName:	VDCGCTL3F18_VDBOX2
Address:	1D7F18h-1D7F1Bh
Name:	VDbox registers6
ShortName:	VDCGCTL3F18_VDBOX3
Address:	1E3F18h-1E3F1Bh
Name:	VDbox registers6
ShortName:	VDCGCTL3F18_VDBOX4
Address:	1E7F18h-1E7F1Bh
Name:	VDbox registers6
ShortName:	VDCGCTL3F18_VDBOX5
Address:	1F3F18h-1F3F1Bh
Name:	VDbox registers6
ShortName:	VDCGCTL3F18_VDBOX6
Address:	1F7F18h-1F7F1Bh
Name:	VDbox registers6
ShortName:	VDCGCTL3F18_VDBOX7

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31:27	**Reserved** Access: R/W Reserved

VDCGCTL3F18 - Vdbox unit Level Clock Gating Control 3F18

26	**VECS BE unit Clock Gating Disable** Access: R/W VECS BE unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
25	**VECS FE unit Clock Gating Disable** Access: R/W VECS FE unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
24	**VCS BE unit Clock Gating Disable** Access: R/W VCS BE unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
23	**VCS FE unit Clock Gating Disable** Access: R/W VCS FE unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
22	**amx router unit Clock Gating Disable** Access: R/W amxb router unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)

VDCGCTL3F18 - Vdbox unit Level Clock Gating Control 3F18

	21	**amx unit Clock Gating Disable** Access: R/W amx unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	20	**splt unit Clock Gating Disable** Access: R/W splt unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	19	**tbc unit Clock Gating Disable** Access: R/W tbc unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	18	**vdl1is unit Clock Gating Disable** Access: R/W vdl1is unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	17	**lbc unit Clock Gating Disable** Access: R/W lbc unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	16	**amxb unit Clock Gating Disable**

VDCGCTL3F18 - Vdbox unit Level Clock Gating Control 3F18

		Access: R/W
		amxb unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	15	**Reserved**
		Access: R/W
		Reserved
	14	**awm unit Clock Gating Disable**
		Access: R/W
		awm unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	13	**aln unit Clock Gating Disable**
		Access: R/W
		aln unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	12	**alf unit Clock Gating Disable**
		Access: R/W
		alf unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	11	**apr unit Clock Gating Disable**
		Access: R/W
		apr unit Clock Gating Disable Control:

VDCGCTL3F18 - Vdbox unit Level Clock Gating Control 3F18

		'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	10	**amc unit Clock Gating Disable** Access: R/W amc unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	9	**ait unit Clock Gating Disable** Access: R/W ait unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	8	**app unit Clock Gating Disable** Access: R/W app unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	7	**aed unit Clock Gating Disable** Access: R/W aed unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	6	**hfe unit Clock Gating Disable** Access: R/W hfe unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for

VDCGCTL3F18 - Vdbox unit Level Clock Gating Control 3F18

		functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	5	**scr unit Clock Gating Disable 2** Access: R/W scr unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	4	**scr unit Clock Gating Disable 1** Access: R/W scr unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	3	**scr unit Clock Gating Disable 0** Access: R/W scr unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	2	**scr unit Clock Gating Disable 3** Access: R/W scr unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	1	**Reserved** Access: R/W Reserved
	0	**kin unit Clock Gating Disable**

VDCGCTL3F18 - Vdbox unit Level Clock Gating Control 3F18			
		Access:	R/W
		kin unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)	

Vdbox unit Level Clock Gating override during rstflow

VDMISCCP3F20 - Vdbox unit Level Clock Gating override during rstflow

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31:0	**ECO Spare Bits** Access: R/W Reserved

vdcp Vdbox unit Level Clock Gating override during rstflow

VDMISCCP3F20 - vdcp Vdbox unit Level Clock Gating override during rstflow

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	03F20h

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31:1	**Reserved** Access: R/W Reserved
	0	**misccp Clock Gating Disable during rstflow** Default Value: 1b Access: R/W misccp Clock Gating Disable Control: '0' : Clock Gating Enabled during reset flows (i.e., clocks can be gated when they are not required to toggle for functionality, NOT Recommended) '1' : Clock Gating Disabled during reset flows. (i.e., clocks are toggling, always) Register bit defaults to value 1'b1, which is a requirement due to Synchronous reset flops Randomizing this bit will result in X flush not completing during the simulation

VEBOX1 MOCS Register

VEBX1_MOCS - VEBOX1 MOCS Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	10600h
Name:	VEBX1 MOCS 0
ShortName:	VEBX1_MOCS_0
Address:	10604h
Name:	VEBX1 MOCS 1
ShortName:	VEBX1_MOCS_1
Address:	10608h
Name:	VEBX1 MOCS 2
ShortName:	VEBX1_MOCS_2
Address:	1060Ch
Name:	VEBX1 MOCS 3
ShortName:	VEBX1_MOCS_3
Address:	10610h
Name:	VEBX1 MOCS 4
ShortName:	VEBX1_MOCS_4
Address:	10614h
Name:	VEBX1 MOCS 5
ShortName:	VEBX1_MOCS_5
Address:	10618h
Name:	VEBX1 MOCS 6
ShortName:	VEBX1_MOCS_6
Address:	1061Ch
Name:	VEBX1 MOCS 7
ShortName:	VEBX1_MOCS_7
Address:	10620h
Name:	VEBX1 MOCS 8
ShortName:	VEBX1_MOCS_8
Address:	10624h

VEBX1_MOCS - VEBOX1 MOCS Register	
Name:	VEBX1 MOCS 9
ShortName:	VEBX1_MOCS_9
Address:	10628h
Name:	VEBX1 MOCS 10
ShortName:	VEBX1_MOCS_10
Address:	1062Ch
Name:	VEBX1 MOCS 11
ShortName:	VEBX1_MOCS_11
Address:	10630h
Name:	VEBX1 MOCS 12
ShortName:	VEBX1_MOCS_12
Address:	10634h
Name:	VEBX1 MOCS 13
ShortName:	VEBX1_MOCS_13
Address:	10638h
Name:	VEBX1 MOCS 14
ShortName:	VEBX1_MOCS_14
Address:	1063Ch
Name:	VEBX1 MOCS 15
ShortName:	VEBX1_MOCS_15
Address:	10640h
Name:	VEBX1 MOCS 16
ShortName:	VEBX1_MOCS_16
Address:	10644h
Name:	VEBX1 MOCS 17
ShortName:	VEBX1_MOCS_17
Address:	10648h
Name:	VEBX1 MOCS 18
ShortName:	VEBX1_MOCS_18
Address:	1064Ch
Name:	VEBX1 MOCS 19
ShortName:	VEBX1_MOCS_19
Address:	10650h
Name:	VEBX1 MOCS 20
ShortName:	VEBX1_MOCS_20

VEBX1_MOCS - VEBOX1 MOCS Register	
Address:	10654h
Name:	VEBX1 MOCS 21
ShortName:	VEBX1_MOCS_21
Address:	10658h
Name:	VEBX1 MOCS 22
ShortName:	VEBX1_MOCS_22
Address:	1065Ch
Name:	VEBX1 MOCS 23
ShortName:	VEBX1_MOCS_23
Address:	10660h
Name:	VEBX1 MOCS 24
ShortName:	VEBX1_MOCS_24
Address:	10664h
Name:	VEBX1 MOCS 25
ShortName:	VEBX1_MOCS_25
Address:	10668h
Name:	VEBX1 MOCS 26
ShortName:	VEBX1_MOCS_26
Address:	1066Ch
Name:	VEBX1 MOCS 27
ShortName:	VEBX1_MOCS_27
Address:	10670h
Name:	VEBX1 MOCS 28
ShortName:	VEBX1_MOCS_28
Address:	10674h
Name:	VEBX1 MOCS 29
ShortName:	VEBX1_MOCS_29
Address:	10678h
Name:	VEBX1 MOCS 30
ShortName:	VEBX1_MOCS_30
Address:	1067Ch
Name:	VEBX1 MOCS 31
ShortName:	VEBX1_MOCS_31
Address:	10680h
Name:	VEBX1 MOCS 32

VEBX1_MOCS - VEBOX1 MOCS Register	
ShortName:	VEBX1_MOCS_32
Address:	10684h
Name:	VEBX1 MOCS 33
ShortName:	VEBX1_MOCS_33
Address:	10688h
Name:	VEBX1 MOCS 34
ShortName:	VEBX1_MOCS_34
Address:	1068Ch
Name:	VEBX1 MOCS 35
ShortName:	VEBX1_MOCS_35
Address:	10690h
Name:	VEBX1 MOCS 36
ShortName:	VEBX1_MOCS_36
Address:	10694h
Name:	VEBX1 MOCS 37
ShortName:	VEBX1_MOCS_37
Address:	10698h
Name:	VEBX1 MOCS 38
ShortName:	VEBX1_MOCS_38
Address:	1069Ch
Name:	VEBX1 MOCS 39
ShortName:	VEBX1_MOCS_39
Address:	106A0h
Name:	VEBX1 MOCS 40
ShortName:	VEBX1_MOCS_40
Address:	106A4h
Name:	VEBX1 MOCS 41
ShortName:	VEBX1_MOCS_41
Address:	106A8h
Name:	VEBX1 MOCS 42
ShortName:	VEBX1_MOCS_42
Address:	106ACh
Name:	VEBX1 MOCS 43
ShortName:	VEBX1_MOCS_43

VEBX1_MOCS - VEBOX1 MOCS Register	
Address:	106B0h
Name:	VEBX1 MOCS 44
ShortName:	VEBX1_MOCS_44
Address:	106B4h
Name:	VEBX1 MOCS 45
ShortName:	VEBX1_MOCS_45
Address:	106B8h
Name:	VEBX1 MOCS 46
ShortName:	VEBX1_MOCS_46
Address:	106BCh
Name:	VEBX1 MOCS 47
ShortName:	VEBX1_MOCS_47
Address:	106C0h
Name:	VEBX1 MOCS 48
ShortName:	VEBX1_MOCS_48
Address:	106C4h
Name:	VEBX1 MOCS 49
ShortName:	VEBX1_MOCS_49
Address:	106C8h
Name:	VEBX1 MOCS 50
ShortName:	VEBX1_MOCS_50
Address:	106CCh
Name:	VEBX1 MOCS 51
ShortName:	VEBX1_MOCS_51
Address:	106D0h
Name:	VEBX1 MOCS 52
ShortName:	VEBX1_MOCS_52
Address:	106D4h
Name:	VEBX1 MOCS 53
ShortName:	VEBX1_MOCS_53
Address:	106D8h
Name:	VEBX1 MOCS 54
ShortName:	VEBX1_MOCS_54
Address:	106DCh
Name:	VEBX1 MOCS 55

VEBX1_MOCS - VEBOX1 MOCS Register

ShortName:	VEBX1_MOCS_55

Address:	106E0h
Name:	VEBX1 MOCS 56
ShortName:	VEBX1_MOCS_56

Address:	106E4h
Name:	VEBX1 MOCS 57
ShortName:	VEBX1_MOCS_57

Address:	106E8h
Name:	VEBX1 MOCS 58
ShortName:	VEBX1_MOCS_58

Address:	106ECh
Name:	VEBX1 MOCS 59
ShortName:	VEBX1_MOCS_59

Address:	106F0h
Name:	VEBX1 MOCS 60
ShortName:	VEBX1_MOCS_60

Address:	106F4h
Name:	VEBX1 MOCS 61
ShortName:	VEBX1_MOCS_61

Address:	106F8h
Name:	VEBX1 MOCS 62
ShortName:	VEBX1_MOCS_62

Address:	106FCh
Name:	VEBX1 MOCS 63
ShortName:	VEBX1_MOCS_63

VEBX1 MOCS register.

DWord	Bit	Description
0	31:19	**Reserved** Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit

VEBX1_MOCS - VEBOX1 MOCS Register

		logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service** Default Value: 00b Access: R/W This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec. 00: Value from Private PAT Registers(40E0/40E4/40E8/40EC) 01: Class 1 10: Class 2 11: Class 3
	14	**Reserved**
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111:Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is do not care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled

VEBX1_MOCS - VEBOX1 MOCS Register

		1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT)

VEBX1_MOCS - VEBOX1 MOCS Register		
		11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

VEBOX2 MOCS Register

VEBX2_MOCS - VEBOX2 MOCS Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	10700h
Name:	VEBX2 MOCS 0
ShortName:	VEBX2_MOCS_0
Address:	10704h
Name:	VEBX2 MOCS 1
ShortName:	VEBX2_MOCS_1
Address:	10708h
Name:	VEBX2 MOCS 2
ShortName:	VEBX2_MOCS_2
Address:	1070Ch
Name:	VEBX2 MOCS 3
ShortName:	VEBX2_MOCS_3
Address:	10710h
Name:	VEBX2 MOCS 4
ShortName:	VEBX2_MOCS_4
Address:	10714h
Name:	VEBX2 MOCS 5
ShortName:	VEBX2_MOCS_5
Address:	10718h
Name:	VEBX2 MOCS 6
ShortName:	VEBX2_MOCS_6
Address:	1071Ch
Name:	VEBX2 MOCS 7
ShortName:	VEBX2_MOCS_7
Address:	10720h
Name:	VEBX2 MOCS 8
ShortName:	VEBX2_MOCS_8
Address:	10724h

VEBX2_MOCS - VEBOX2 MOCS Register	
Name:	VEBX2 MOCS 9
ShortName:	VEBX2_MOCS_9
Address:	10728h
Name:	VEBX2 MOCS 10
ShortName:	VEBX2_MOCS_10
Address:	1072Ch
Name:	VEBX2 MOCS 11
ShortName:	VEBX2_MOCS_11
Address:	10730h
Name:	VEBX2 MOCS 12
ShortName:	VEBX2_MOCS_12
Address:	10734h
Name:	VEBX2 MOCS 13
ShortName:	VEBX2_MOCS_13
Address:	10738h
Name:	VEBX2 MOCS 14
ShortName:	VEBX2_MOCS_14
Address:	1073Ch
Name:	VEBX2 MOCS 15
ShortName:	VEBX2_MOCS_15
Address:	10740h
Name:	VEBX2 MOCS 16
ShortName:	VEBX2_MOCS_16
Address:	10744h
Name:	VEBX2 MOCS 17
ShortName:	VEBX2_MOCS_17
Address:	10748h
Name:	VEBX2 MOCS 18
ShortName:	VEBX2_MOCS_18
Address:	1074Ch
Name:	VEBX2 MOCS 19
ShortName:	VEBX2_MOCS_19
Address:	10750h
Name:	VEBX2 MOCS 20
ShortName:	VEBX2_MOCS_20

VEBX2_MOCS - VEBOX2 MOCS Register	
Address:	10754h
Name:	VEBX2 MOCS 21
ShortName:	VEBX2_MOCS_21
Address:	10758h
Name:	VEBX2 MOCS 22
ShortName:	VEBX2_MOCS_22
Address:	1075Ch
Name:	VEBX2 MOCS 23
ShortName:	VEBX2_MOCS_23
Address:	10760h
Name:	VEBX2 MOCS 24
ShortName:	VEBX2_MOCS_24
Address:	10764h
Name:	VEBX2 MOCS 25
ShortName:	VEBX2_MOCS_25
Address:	10768h
Name:	VEBX2 MOCS 26
ShortName:	VEBX2_MOCS_26
Address:	1076Ch
Name:	VEBX2 MOCS 27
ShortName:	VEBX2_MOCS_27
Address:	10770h
Name:	VEBX2 MOCS 28
ShortName:	VEBX2_MOCS_28
Address:	10774h
Name:	VEBX2 MOCS 29
ShortName:	VEBX2_MOCS_29
Address:	10778h
Name:	VEBX2 MOCS 30
ShortName:	VEBX2_MOCS_30
Address:	1077Ch
Name:	VEBX2 MOCS 31
ShortName:	VEBX2_MOCS_31
Address:	10780h
Name:	VEBX2 MOCS 32

VEBX2_MOCS - VEBOX2 MOCS Register	
ShortName:	VEBX2_MOCS_32
Address:	10784h
Name:	VEBX2 MOCS 33
ShortName:	VEBX2_MOCS_33
Address:	10788h
Name:	VEBX2 MOCS 34
ShortName:	VEBX2_MOCS_34
Address:	1078Ch
Name:	VEBX2 MOCS 35
ShortName:	VEBX2_MOCS_35
Address:	10790h
Name:	VEBX2 MOCS 36
ShortName:	VEBX2_MOCS_36
Address:	10794h
Name:	VEBX2 MOCS 37
ShortName:	VEBX2_MOCS_37
Address:	10798h
Name:	VEBX2 MOCS 38
ShortName:	VEBX2_MOCS_38
Address:	1079Ch
Name:	VEBX2 MOCS 39
ShortName:	VEBX2_MOCS_39
Address:	107A0h
Name:	VEBX2 MOCS 40
ShortName:	VEBX2_MOCS_40
Address:	107A4h
Name:	VEBX2 MOCS 41
ShortName:	VEBX2_MOCS_41
Address:	107A8h
Name:	VEBX2 MOCS 42
ShortName:	VEBX2_MOCS_42
Address:	107ACh
Name:	VEBX2 MOCS 43
ShortName:	VEBX2_MOCS_43

VEBX2_MOCS - VEBOX2 MOCS Register	
Address:	107B0h
Name:	VEBX2 MOCS 44
ShortName:	VEBX2_MOCS_44
Address:	107B4h
Name:	VEBX2 MOCS 45
ShortName:	VEBX2_MOCS_45
Address:	107B8h
Name:	VEBX2 MOCS 46
ShortName:	VEBX2_MOCS_46
Address:	107BCh
Name:	VEBX2 MOCS 47
ShortName:	VEBX2_MOCS_47
Address:	107C0h
Name:	VEBX2 MOCS 48
ShortName:	VEBX2_MOCS_48
Address:	107C4h
Name:	VEBX2 MOCS 49
ShortName:	VEBX2_MOCS_49
Address:	107C8h
Name:	VEBX2 MOCS 50
ShortName:	VEBX2_MOCS_50
Address:	107CCh
Name:	VEBX2 MOCS 51
ShortName:	VEBX2_MOCS_51
Address:	107D0h
Name:	VEBX2 MOCS 52
ShortName:	VEBX2_MOCS_52
Address:	107D4h
Name:	VEBX2 MOCS 53
ShortName:	VEBX2_MOCS_53
Address:	107D8h
Name:	VEBX2 MOCS 54
ShortName:	VEBX2_MOCS_54
Address:	107DCh
Name:	VEBX2 MOCS 55

VEBX2_MOCS - VEBOX2 MOCS Register

ShortName:	VEBX2_MOCS_55

Address:	107E0h
Name:	VEBX2 MOCS 56
ShortName:	VEBX2_MOCS_56

Address:	107E4h
Name:	VEBX2 MOCS 57
ShortName:	VEBX2_MOCS_57

Address:	107E8h
Name:	VEBX2 MOCS 58
ShortName:	VEBX2_MOCS_58

Address:	107ECh
Name:	VEBX2 MOCS 59
ShortName:	VEBX2_MOCS_59

Address:	107F0h
Name:	VEBX2 MOCS 60
ShortName:	VEBX2_MOCS_60

Address:	107F4h
Name:	VEBX2 MOCS 61
ShortName:	VEBX2_MOCS_61

Address:	107F8h
Name:	VEBX2 MOCS 62
ShortName:	VEBX2_MOCS_62

Address:	107FCh
Name:	VEBX2 MOCS 63
ShortName:	VEBX2_MOCS_63

VEBX2 MOCS register.

DWord	Bit	Description
0	31:19	**Reserved** Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit

VEBX2_MOCS - VEBOX2 MOCS Register

		logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service** Default Value: 00b Access: R/W This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec. 00: Value from Private PAT Registers(40E0/40E4/40E8/40EC) 01: Class 1 10: Class 2 11: Class 3
	14	**Reserved**
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111:Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is do not care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled

		1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT)

VEBX2_MOCS - VEBOX2 MOCS Register		
		11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

VEBOX3 MOCS Register

VEBX3_MOCS - VEBOX3 MOCS Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	10800h
Name:	VEBX3 MOCS 0
ShortName:	VEBX3_MOCS_0
Address:	10804h
Name:	VEBX3 MOCS 1
ShortName:	VEBX3_MOCS_1
Address:	10808h
Name:	VEBX3 MOCS 2
ShortName:	VEBX3_MOCS_2
Address:	1080Ch
Name:	VEBX3 MOCS 3
ShortName:	VEBX3_MOCS_3
Address:	10810h
Name:	VEBX3 MOCS 4
ShortName:	VEBX3_MOCS_4
Address:	10814h
Name:	VEBX3 MOCS 5
ShortName:	VEBX3_MOCS_5
Address:	10818h
Name:	VEBX3 MOCS 6
ShortName:	VEBX3_MOCS_6
Address:	1081Ch
Name:	VEBX3 MOCS 7
ShortName:	VEBX3_MOCS_7
Address:	10820h
Name:	VEBX3 MOCS 8
ShortName:	VEBX3_MOCS_8
Address:	10824h

VEBX3_MOCS - VEBOX3 MOCS Register	
Name:	VEBX3 MOCS 9
ShortName:	VEBX3_MOCS_9
Address:	10828h
Name:	VEBX3 MOCS 10
ShortName:	VEBX3_MOCS_10
Address:	1082Ch
Name:	VEBX3 MOCS 11
ShortName:	VEBX3_MOCS_11
Address:	10830h
Name:	VEBX3 MOCS 12
ShortName:	VEBX3_MOCS_12
Address:	10834h
Name:	VEBX3 MOCS 13
ShortName:	VEBX3_MOCS_13
Address:	10838h
Name:	VEBX3 MOCS 14
ShortName:	VEBX3_MOCS_14
Address:	1083Ch
Name:	VEBX3 MOCS 15
ShortName:	VEBX3_MOCS_15
Address:	10840h
Name:	VEBX3 MOCS 16
ShortName:	VEBX3_MOCS_16
Address:	10844h
Name:	VEBX3 MOCS 17
ShortName:	VEBX3_MOCS_17
Address:	10848h
Name:	VEBX3 MOCS 18
ShortName:	VEBX3_MOCS_18
Address:	1084Ch
Name:	VEBX3 MOCS 19
ShortName:	VEBX3_MOCS_19
Address:	10850h
Name:	VEBX3 MOCS 20
ShortName:	VEBX3_MOCS_20

VEBX3_MOCS - VEBOX3 MOCS Register	
Address:	10854h
Name:	VEBX3 MOCS 21
ShortName:	VEBX3_MOCS_21
Address:	10858h
Name:	VEBX3 MOCS 22
ShortName:	VEBX3_MOCS_22
Address:	1085Ch
Name:	VEBX3 MOCS 23
ShortName:	VEBX3_MOCS_23
Address:	10860h
Name:	VEBX3 MOCS 24
ShortName:	VEBX3_MOCS_24
Address:	10864h
Name:	VEBX3 MOCS 25
ShortName:	VEBX3_MOCS_25
Address:	10868h
Name:	VEBX3 MOCS 26
ShortName:	VEBX3_MOCS_26
Address:	1086Ch
Name:	VEBX3 MOCS 27
ShortName:	VEBX3_MOCS_27
Address:	10870h
Name:	VEBX3 MOCS 28
ShortName:	VEBX3_MOCS_28
Address:	10874h
Name:	VEBX3 MOCS 29
ShortName:	VEBX3_MOCS_29
Address:	10878h
Name:	VEBX3 MOCS 30
ShortName:	VEBX3_MOCS_30
Address:	1087Ch
Name:	VEBX3 MOCS 31
ShortName:	VEBX3_MOCS_31
Address:	10880h
Name:	VEBX3 MOCS 32

VEBX3_MOCS - VEBOX3 MOCS Register	
ShortName:	VEBX3_MOCS_32
Address:	10884h
Name:	VEBX3 MOCS 33
ShortName:	VEBX3_MOCS_33
Address:	10888h
Name:	VEBX3 MOCS 34
ShortName:	VEBX3_MOCS_34
Address:	1088Ch
Name:	VEBX3 MOCS 35
ShortName:	VEBX3_MOCS_35
Address:	10890h
Name:	VEBX3 MOCS 36
ShortName:	VEBX3_MOCS_36
Address:	10894h
Name:	VEBX3 MOCS 37
ShortName:	VEBX3_MOCS_37
Address:	10898h
Name:	VEBX3 MOCS 38
ShortName:	VEBX3_MOCS_38
Address:	1089Ch
Name:	VEBX3 MOCS 39
ShortName:	VEBX3_MOCS_39
Address:	108A0h
Name:	VEBX3 MOCS 40
ShortName:	VEBX3_MOCS_40
Address:	108A4h
Name:	VEBX3 MOCS 41
ShortName:	VEBX3_MOCS_41
Address:	108A8h
Name:	VEBX3 MOCS 42
ShortName:	VEBX3_MOCS_42
Address:	108ACh
Name:	VEBX3 MOCS 43
ShortName:	VEBX3_MOCS_43

VEBX3_MOCS - VEBOX3 MOCS Register	
Address:	108B0h
Name:	VEBX3 MOCS 44
ShortName:	VEBX3_MOCS_44
Address:	108B4h
Name:	VEBX3 MOCS 45
ShortName:	VEBX3_MOCS_45
Address:	108B8h
Name:	VEBX3 MOCS 46
ShortName:	VEBX3_MOCS_46
Address:	108BCh
Name:	VEBX3 MOCS 47
ShortName:	VEBX3_MOCS_47
Address:	108C0h
Name:	VEBX3 MOCS 48
ShortName:	VEBX3_MOCS_48
Address:	108C4h
Name:	VEBX3 MOCS 49
ShortName:	VEBX3_MOCS_49
Address:	108C8h
Name:	VEBX3 MOCS 50
ShortName:	VEBX3_MOCS_50
Address:	108CCh
Name:	VEBX3 MOCS 51
ShortName:	VEBX3_MOCS_51
Address:	108D0h
Name:	VEBX3 MOCS 52
ShortName:	VEBX3_MOCS_52
Address:	108D4h
Name:	VEBX3 MOCS 53
ShortName:	VEBX3_MOCS_53
Address:	108D8h
Name:	VEBX3 MOCS 54
ShortName:	VEBX3_MOCS_54
Address:	108DCh
Name:	VEBX3 MOCS 55

VEBX3_MOCS - VEBOX3 MOCS Register

ShortName:	VEBX3_MOCS_55

Address:	108E0h
Name:	VEBX3 MOCS 56
ShortName:	VEBX3_MOCS_56

Address:	108E4h
Name:	VEBX3 MOCS 57
ShortName:	VEBX3_MOCS_57

Address:	108E8h
Name:	VEBX3 MOCS 58
ShortName:	VEBX3_MOCS_58

Address:	108ECh
Name:	VEBX3 MOCS 59
ShortName:	VEBX3_MOCS_59

Address:	108F0h
Name:	VEBX3 MOCS 60
ShortName:	VEBX3_MOCS_60

Address:	108F4h
Name:	VEBX3 MOCS 61
ShortName:	VEBX3_MOCS_61

Address:	108F8h
Name:	VEBX3 MOCS 62
ShortName:	VEBX3_MOCS_62

Address:	108FCh
Name:	VEBX3 MOCS 63
ShortName:	VEBX3_MOCS_63

VEBX3 MOCS register.

DWord	Bit	Description
0	31:19	**Reserved** Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit

VEBX3_MOCS - VEBOX3 MOCS Register

		logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service** Default Value: 00b Access: R/W This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec. 00: Value from Private PAT Registers(40E0/40E4/40E8/40EC) 01: Class 1 10: Class 2 11: Class 3
	14	**Reserved**
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111:Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is do not care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled

		1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT)

VEBX3_MOCS - VEBOX3 MOCS Register		
		11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

Vebox MOCS LECC 00 TC 00 Register

VEBOX_MOCS_LECC_00_TC_00 - Vebox MOCS LECC 00 TC 00 Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CB00h
Name:	Vebox MOCS 0
ShortName:	VEBOX_MOCS_0
Address:	0CB40h
Name:	Vebox MOCS 16
ShortName:	VEBOX_MOCS_16
Address:	0CB80h
Name:	Vebox MOCS 32
ShortName:	VEBOX_MOCS_32
Address:	0CBC0h
Name:	Vebox MOCS 48
ShortName:	VEBOX_MOCS_48

VEBOX MOCS register

DWord	Bit	Description
0	31:19	**Reserved** Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service**

VEBOX_MOCS_LECC_00_TC_00 - Vebox MOCS LECC 00 TC 00 Register

		Default Value: 00b Access: R/W This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec. 00: Value from Private PAT Registers(40E0/40E4/40E8/40EC) 01: Class 1 10: Class 2 11: Class 3
	14	**Reserved**
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is do not care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W

		Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

VEBOX MOCS LECC 00 TC 01 Register

VEBOX_MOCS_LECC_00_TC_01 - VEBOX MOCS LECC 00 TC 01 Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CB04h
Name:	VEBOX MOCS 1
ShortName:	VEBOX_MOCS_1
Address:	0CB44h
Name:	VEBOX MOCS 17
ShortName:	VEBOX_MOCS_17
Address:	0CB84h
Name:	VEBOX MOCS 33
ShortName:	VEBOX_MOCS_33
Address:	0CBC4h
Name:	VEBOX MOCS 49
ShortName:	VEBOX_MOCS_49

VEBOX MOCS register

DWord	Bit	Description
0	31:19	**Reserved** Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service**

VEBOX_MOCS_LECC_00_TC_01 - VEBOX MOCS LECC 00 TC 01 Register

		Default Value: 00b Access: R/W This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec. 00: Value from Private PAT Registers(40E0/40E4/40E8/40EC) 01: Class 1 10: Class 2 11: Class 3
	14	**Reserved**
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is do not care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W

VEBOX_MOCS_LECC_00_TC_01 - VEBOX MOCS LECC 00 TC 01 Register

		Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bi
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

VEBOX MOCS LECC 00 TC 10 Register

VEBOX_MOCS_LECC_00_TC_10 - VEBOX MOCS LECC 00 TC 10 Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CB08h
Name:	VEBOX MOCS 2
ShortName:	VEBOX_MOCS_2
Address:	0CB48h
Name:	VEBOX MOCS 18
ShortName:	VEBOX_MOCS_18
Address:	0CB88h
Name:	VEBOX MOCS 34
ShortName:	VEBOX_MOCS_34
Address:	0CBC8h
Name:	VEBOX MOCS 50
ShortName:	VEBOX_MOCS_50

VEBOX MOCS register

DWord	Bit	Description
0	31:19	**Reserved** Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service**

VEBOX_MOCS_LECC_00_TC_10 - VEBOX MOCS LECC 00 TC 10 Register

		Default Value: 00b Access: R/W This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec. 00: Value from Private PAT Registers(40E0/40E4/40E8/40EC) 01: Class 1 10: Class 2 11: Class 3
	14	**Reserved**
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is do not care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W

VEBOX_MOCS_LECC_00_TC_10 - VEBOX MOCS LECC 00 TC 10 Register

		Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

VEBOX MOCS LECC 01 TC 00 Register

VEBOX_MOCS_LECC_01_TC_00 - VEBOX MOCS LECC 01 TC 00 Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CB0Ch
Name:	VEBOX MOCS 3
ShortName:	VEBOX_MOCS_3
Address:	0CB4Ch
Name:	VEBOX MOCS 19
ShortName:	VEBOX_MOCS_19
Address:	0CB8Ch
Name:	VEBOX MOCS 35
ShortName:	VEBOX_MOCS_35
Address:	0CBCCh
Name:	VEBOX MOCS 51
ShortName:	VEBOX_MOCS_51

VEBOX MOCS register

DWord	Bit	Description
0	31:19	**Reserved** Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service**

VEBOX_MOCS_LECC_01_TC_00 - VEBOX MOCS LECC 01 TC 00 Register

		Default Value: 00b Access: R/W This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in.The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec. 00: Value from Private PAT Registers(40E0/40E4/40E8/40EC) 01: Class 1 10: Class 2 11: Class 3
	14	**Reserved**
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is do not care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the

VEBOX_MOCS_LECC_01_TC_00 - VEBOX MOCS LECC 01 TC 00 Register

		line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

VEBOX MOCS LECC 10 TC 00 Register

VEBOX_MOCS_LECC_10_TC_00 - VEBOX MOCS LECC 10 TC 00 Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CB10h
Name:	VEBOX MOCS 4
ShortName:	VEBOX_MOCS_4
Address:	0CB28h
Name:	VEBOX MOCS 10
ShortName:	VEBOX_MOCS_10
Address:	0CB50h
Name:	VEBOX MOCS 20
ShortName:	VEBOX_MOCS_20
Address:	0CB68h
Name:	VEBOX MOCS 26
ShortName:	VEBOX_MOCS_26
Address:	0CB90h
Name:	VEBOX MOCS 36
ShortName:	VEBOX_MOCS_36
Address:	0CBA8h
Name:	VEBOX MOCS 42
ShortName:	VEBOX_MOCS_42
Address:	0CBD0h
Name:	VEBOX MOCS 52
ShortName:	VEBOX_MOCS_52
Address:	0CBE8h
Name:	VEBOX MOCS 58
ShortName:	VEBOX_MOCS_58

VEBOX MOCS register

DWord	Bit	Description
0	31:19	**Reserved**

VEBOX_MOCS_LECC_10_TC_00 - VEBOX MOCS LECC 10 TC 00 Register

		Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service** Default Value: 00b Access: R/W This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec. 00: Value from Private PAT Registers(40E0/40E4/40E8/40EC) 01: Class 1 10: Class 2 11: Class 3
	14	**Reserved**
	13:11	**Page Faulting Mode** Default Value: 000b Access: R/W This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved
	10:8	**Skip Caching control** Default Value: 000b Access: R/W Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is do not care

VEBOX_MOCS_LECC_10_TC_00 - VEBOX MOCS LECC 10 TC 00 Register

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC)

VEBOX_MOCS_LECC_10_TC_00 - VEBOX MOCS LECC 10 TC 00 Register

		01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 10b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

VEBOX MOCS LECC 10 TC 01 Register

VEBOX_MOCS_LECC_10_TC_01 - VEBOX MOCS LECC 10 TC 01 Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CB14h
Name:	VEBOX MOCS 5
ShortName:	VEBOX_MOCS_5
Address:	0CB2Ch
Name:	VEBOX MOCS 11
ShortName:	VEBOX_MOCS_11
Address:	0CB54h
Name:	VEBOX MOCS 21
ShortName:	VEBOX_MOCS_21
Address:	0CB6Ch
Name:	VEBOX MOCS 27
ShortName:	VEBOX_MOCS_27
Address:	0CB94h
Name:	VEBOX MOCS 37
ShortName:	VEBOX_MOCS_37
Address:	0CBACh
Name:	VEBOX MOCS 43
ShortName:	VEBOX_MOCS_43
Address:	0CBD4h
Name:	VEBOX MOCS 53
ShortName:	VEBOX_MOCS_53
Address:	0CBECh
Name:	VEBOX MOCS 59
ShortName:	VEBOX_MOCS_59

VEBOX MOCS register

DWord	Bit	Description
0	31:19	**Reserved**

VEBOX_MOCS_LECC_10_TC_01 - VEBOX MOCS LECC 10 TC 01 Register

	Default Value:	0000000000000b
	Access:	RO

18:17 Self Snoop Enable

Default Value:	00b
Access:	R/W

00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic
01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface
11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface

16:15 Class of Service

Default Value:	00b
Access:	R/W

This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3

14 Reserved

13:11 Page Faulting Mode

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8 Skip Caching control

Default Value:	000b
Access:	R/W

Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface.
If "0" - than corresponding address bit value is do not care

VEBOX_MOCS_LECC_10_TC_01 - VEBOX MOCS LECC 10 TC 01 Register

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC)

<table>
<tr><th colspan="3">VEBOX_MOCS_LECC_10_TC_01 - VEBOX MOCS LECC 10 TC 01 Register</th></tr>
<tr><td></td><td></td><td>01: LLC Only
10: LLC/eLLC Allowed
11: LLC/eLLC Allowed</td></tr>
<tr><td></td><td>1:0</td><td>LLC/eDRAM cacheability control<table><tr><td>Default Value:</td><td>10b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>Memory type information used in LLC/eDRAM.
00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)
01: Uncacheable (UC) - non-cacheable
10: Writethrough (WT)
11: Writeback (WB)
Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used
Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index</td></tr>
</table>

VEBOX MOCS LECC 10 TC 10 Register

VEBOX_MOCS_LECC_10_TC_10 - VEBOX MOCS LECC 10 TC 10 Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CB18h
Name:	VEBOX MOCS 6
ShortName:	VEBOX_MOCS_6
Address:	0CB30h
Name:	VEBOX MOCS 12
ShortName:	VEBOX_MOCS_12
Address:	0CB58h
Name:	VEBOX MOCS 22
ShortName:	VEBOX_MOCS_22
Address:	0CB70h
Name:	VEBOX MOCS 28
ShortName:	VEBOX_MOCS_28
Address:	0CB98h
Name:	VEBOX MOCS 38
ShortName:	VEBOX_MOCS_38
Address:	0CBB0h
Name:	VEBOX MOCS 44
ShortName:	VEBOX_MOCS_44
Address:	0CBD8h
Name:	VEBOX MOCS 54
ShortName:	VEBOX_MOCS_54
Address:	0CBF0h
Name:	VEBOX MOCS 60
ShortName:	VEBOX_MOCS_60

VEBOX MOCS register

DWord	Bit	Description
0	31:19	**Reserved**

VEBOX_MOCS_LECC_10_TC_10 - VEBOX MOCS LECC 10 TC 10 Register

	Default Value:	0000000000000b
	Access:	RO

18:17 Self Snoop Enable

Default Value:	00b
Access:	R/W

00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic
01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface
11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface

16:15 Class of Service

Default Value:	00b
Access:	R/W

This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3

14 Reserved

13:11 Page Faulting Mode

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8 Skip Caching control

Default Value:	000b
Access:	R/W

Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface.
If "0" - than corresponding address bit value is do not care

VEBOX_MOCS_LECC_10_TC_10 - VEBOX MOCS LECC 10 TC 10 Register

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC)

<table>
<tr><th colspan="3">VEBOX_MOCS_LECC_10_TC_10 - VEBOX MOCS LECC 10 TC 10 Register</th></tr>
<tr><td></td><td></td><td>01: LLC Only
10: LLC/eLLC Allowed
11: LLC/eLLC Allowed</td></tr>
<tr><td></td><td>1:0</td><td>LLC/eDRAM cacheability control
<table><tr><td>Default Value:</td><td>10b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>Memory type information used in LLC/eDRAM.
00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)
01: Uncacheable (UC) - non-cacheable
10: Writethrough (WT)
11: Writeback (WB)
Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used
Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index</td></tr>
</table>

VEBOX MOCS LECC 11 TC 00 Register

VEBOX_MOCS_LECC_11_TC_00 - VEBOX MOCS LECC 11 TC 00 Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CB1Ch
Name:	VEBOX MOCS 7
ShortName:	VEBOX_MOCS_7
Address:	0CB34h
Name:	VEBOX MOCS 13
ShortName:	VEBOX_MOCS_13
Address:	0CB5Ch
Name:	VEBOX MOCS 23
ShortName:	VEBOX_MOCS_23
Address:	0CB74h
Name:	VEBOX MOCS 29
ShortName:	VEBOX_MOCS_29
Address:	0CB9Ch
Name:	VEBOX MOCS 39
ShortName:	VEBOX_MOCS_39
Address:	0CBB4h
Name:	VEBOX MOCS 45
ShortName:	VEBOX_MOCS_45
Address:	0CBDCh
Name:	VEBOX MOCS 55
ShortName:	VEBOX_MOCS_55
Address:	0CBF4h
Name:	VEBOX MOCS 61
ShortName:	VEBOX_MOCS_61

VEBOX MOCS register

DWord	Bit	Description
0	31:19	**Reserved**

VEBOX_MOCS_LECC_11_TC_00 - VEBOX MOCS LECC 11 TC 00 Register

	Default Value:	0000000000000b
	Access:	RO

18:17 Self Snoop Enable

Default Value:	00b
Access:	R/W

00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic
01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface
11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface

16:15 Class of Service

Default Value:	00b
Access:	R/W

This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3

14 Reserved

13:11 Page Faulting Mode

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8 Skip Caching control

Default Value:	000b
Access:	R/W

Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface.
If "0" - than corresponding address bit value is do not care

VEBOX_MOCS_LECC_11_TC_00 - VEBOX MOCS LECC 11 TC 00 Register

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC)

VEBOX_MOCS_LECC_11_TC_00 - VEBOX MOCS LECC 11 TC 00 Register

		01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

VEBOX MOCS LECC 11 TC 01 Register

VEBOX_MOCS_LECC_11_TC_01 - VEBOX MOCS LECC 11 TC 01 Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CB20h
Name:	VEBOX MOCS 8
ShortName:	VEBOX_MOCS_8
Address:	0CB38h
Name:	VEBOX MOCS 14
ShortName:	VEBOX_MOCS_14
Address:	0CB60h
Name:	VEBOX MOCS 24
ShortName:	VEBOX_MOCS_24
Address:	0CB78h
Name:	VEBOX MOCS 30
ShortName:	VEBOX_MOCS_30
Address:	0CBA0h
Name:	VEBOX MOCS 40
ShortName:	VEBOX_MOCS_40
Address:	0CBB8h
Name:	VEBOX MOCS 46
ShortName:	VEBOX_MOCS_46
Address:	0CBE0h
Name:	VEBOX MOCS 56
ShortName:	VEBOX_MOCS_56
Address:	0CBF8h
Name:	VEBOX MOCS 62
ShortName:	VEBOX_MOCS_62

VEBOX MOCS register

DWord	Bit	Description
0	31:19	**Reserved**

VEBOX_MOCS_LECC_11_TC_01 - VEBOX MOCS LECC 11 TC 01 Register

	Default Value:	0000000000000b
	Access:	RO

18:17 Self Snoop Enable

Default Value:	00b
Access:	R/W

00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic
01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface
11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface

16:15 Class of Service

Default Value:	00b
Access:	R/W

This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3

14 Reserved

13:11 Page Faulting Mode

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8 Skip Caching control

Default Value:	000b
Access:	R/W

Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface.
If "0" - than corresponding address bit value is do not care

VEBOX_MOCS_LECC_11_TC_01 - VEBOX MOCS LECC 11 TC 01 Register

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC)

<table>
<tr><th colspan="3">VEBOX_MOCS_LECC_11_TC_01 - VEBOX MOCS LECC 11 TC 01 Register</th></tr>
<tr><td></td><td></td><td>01: LLC Only
10: LLC/eLLC Allowed
11: LLC/eLLC Allowed</td></tr>
<tr><td></td><td>1:0</td><td>LLC/eDRAM cacheability control<table><tr><td>Default Value:</td><td>11b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>Memory type information used in LLC/eDRAM.
00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)
01: Uncacheable (UC) - non-cacheable
10: Writethrough (WT)
11: Writeback (WB)
Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used
Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index</td></tr>
</table>

VEBOX MOCS LECC 11 TC 10 Register

VEBOX_MOCS_LECC_11_TC_10 - VEBOX MOCS LECC 11 TC 10 Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CB24h
Name:	VEBOX MOCS 9
ShortName:	VEBOX_MOCS_9
Address:	0CB3Ch
Name:	VEBOX MOCS 15
ShortName:	VEBOX_MOCS_15
Address:	0CB64h
Name:	VEBOX MOCS 25
ShortName:	VEBOX_MOCS_25
Address:	0CB7Ch
Name:	VEBOX MOCS 31
ShortName:	VEBOX_MOCS_31
Address:	0CBA4h
Name:	VEBOX MOCS 41
ShortName:	VEBOX_MOCS_41
Address:	0CBBCh
Name:	VEBOX MOCS 47
ShortName:	VEBOX_MOCS_47
Address:	0CBE4h
Name:	VEBOX MOCS 57
ShortName:	VEBOX_MOCS_57
Address:	0CBFCh
Name:	VEBOX MOCS 63
ShortName:	VEBOX_MOCS_63

VEBOX MOCS register

DWord	Bit	Description
0	31:19	**Reserved**

VEBOX_MOCS_LECC_11_TC_10 - VEBOX MOCS LECC 11 TC 10 Register

	Default Value:	0000000000000b
	Access:	RO

18:17 Self Snoop Enable

Default Value:	00b
Access:	R/W

00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic
01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface
11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface

16:15 Class of Service

Default Value:	00b
Access:	R/W

This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3

14 Reserved

13:11 Page Faulting Mode

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8 Skip Caching control

Default Value:	000b
Access:	R/W

Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface.
If "0" - than corresponding address bit value is do not care

VEBOX_MOCS_LECC_11_TC_10 - VEBOX MOCS LECC 11 TC 10 Register

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC)

VEBOX_MOCS_LECC_11_TC_10 - VEBOX MOCS LECC 11 TC 10 Register

		01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 11b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

Vebox Power Context Save request

VECGCTL3F00 - Vebox Power Context Save request		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	1CBF00h-1CBF03h	
Name:	VEbox registers	
ShortName:	VECGCTL3F00_VEBOX0	
Address:	1DBF00h-1DBF03h	
Name:	VEbox registers	
ShortName:	VECGCTL3F00_VEBOX1	
Address:	1EBF00h-1EBF03h	
Name:	VEbox registers	
ShortName:	VECGCTL3F00_VEBOX2	
Address:	1FBF00h-1FBF03h	
Name:	VEbox registers	
ShortName:	VECGCTL3F00_VEBOX3	

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO Message Mask bots for lower 16 bits
	15:10	**Reserved** Access: RO Reserved
	9	**Power context save request** Access: R/W Set Power Context Save Request 1'b0 : Power context save is not being requested 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W QWord Credits for Power Context Save Request

VECGCTL3F00 - Vebox Power Context Save request		
		Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

Vebox unit Level Clock Gating Control 3F04

VECGCTL3F04 - Vebox unit Level Clock Gating Control 3F04		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	1CBF04h-1CBF07h	
Name:	VEbox registers	
ShortName:	VECGCTL3F04_VEBOX0	
Address:	1DBF04h-1DBF07h	
Name:	VEbox registers	
ShortName:	VECGCTL3F04_VEBOX1	
Address:	1EBF04h-1EBF07h	
Name:	VEbox registers	
ShortName:	VECGCTL3F04_VEBOX2	
Address:	1FBF04h-1FBF07h	
Name:	VEbox registers	
ShortName:	VECGCTL3F04_VEBOX3	
Unit Level Clock Gating Disable bits		

DWord	Bit	Description
0	31:24	**Reserved** Access: R/W Reserved
	23	**ramdftunit Clock Gating Disable** Access: R/W ramdftunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	22	**cg3ddis_spare2 Clock Gating Disable** Access: R/W cg3ddis_spare2 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

VECGCTL3F04 - Vebox unit Level Clock Gating Control 3F04

	21	**cg3ddis_spare1 Clock Gating Disable** Access: R/W cg3ddis_spare1 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	20	**MCRunit Clock Gating Disable** Default Value: 1b Access: R/W MCRunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	19	**VFWunit Clock Gating Disable** Access: R/W VFWunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	18	**VEOunit Clock Gating Disable** Access: R/W VEOunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	17	**ECSunit Clock Gating Disable** Access: R/W ECSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	16	**VDNunit Clock Gating Disable** Access: R/W VDNunit Clock Gating Disable Control:

VECGCTL3F04 - Vebox unit Level Clock Gating Control 3F04

		'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	15	**VDMunit Clock Gating Disable** Access: R/W VDMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	14	**VDIunit Clock Gating Disable** Access: R/W VDIunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	13	**VCWunit Clock Gating Disable** Access: R/W VCWunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	12	**VCUSunit Clock Gating Disable** Access: R/W VCUSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	11	**SFXunit Clock Gating Disable** Access: R/W SFXunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	10	**SFOunit Clock Gating Disable** Access: R/W SFOunit Clock Gating Disable Control:

VECGCTL3F04 - Vebox unit Level Clock Gating Control 3F04

		'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	9	**SFMunit Clock Gating Disable** Access: R/W SFMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	8	**SFIunit Clock Gating Disable** Access: R/W SFIunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	7	**SFEunit Clock Gating Disable** Access: R/W SFEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	6	**SFDunit Clock Gating Disable** Access: R/W SFDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	5	**SFAunit Clock Gating Disable** Access: R/W SFAunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	4	**Reserved**
	3	**IECPunit Clock Gating Disable** Access: R/W

VECGCTL3F04 - Vebox unit Level Clock Gating Control 3F04		
		IECPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	2	**GCPunit Clock Gating Disable** Access: R/W GCPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	1	**GAVARBunit Clock Gating Disable** Access: R/W GAVARBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	0	**GAVunit Clock Gating Disable** Access: R/W GAVunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Vebox unit Level Clock Gating Control 3F08

VECGCTL3F08 - Vebox unit Level Clock Gating Control 3F08			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Size (in bits):	32		
Address:	1CBF08h-1CBF0Bh		
Name:	VEbox registers		
ShortName:	VECGCTL3F08_VEBOX0		
Address:	1DBF08h-1DBF0Bh		
Name:	VEbox registers		
ShortName:	VECGCTL3F08_VEBOX1		
Address:	1EBF08h-1EBF0Bh		
Name:	VEbox registers		
ShortName:	VECGCTL3F08_VEBOX2		
Address:	1FBF08h-1FBF0Bh		
Name:	VEbox registers		
ShortName:	VECGCTL3F08_VEBOX3		
Unit Level Clock Gating Disable bits			
DWord	**Bit**	**Description**	
0	31:8	**Reserved**	
		Access:	R/W
		Reserved	
	7	**VEOunit Clock Gating Disable**	
		Access:	R/W
		VEOunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	6	**VDIunit Clock Gating Disable**	
		Access:	R/W
		VDIunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

VECGCTL3F08 - Vebox unit Level Clock Gating Control 3F08

	5	**VCWunit Clock Gating Disable** Access: R/W VCWunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	4	**SFMunit Clock Gating Disable** Access: R/W SFMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	3	**SFEunit Clock Gating Disable** Access: R/W SFEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	2	**SFDunits Clock Gating Disable** Access: R/W SFDunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	0	**IECPuit Clock Gating Disable** Access: R/W IECPuit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Vebox unit Level Clock Gating override during rstflow

VEMISCCP3F10 - Vebox unit Level Clock Gating override during rstflow

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	03F10h

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31:1	**Reserved** Access: R/W Reserved
	0	**misccp Clock Gating Disable during rstflow** Default Value: 1b Access: R/W misccp Clock Gating Disable Control: '0' : Clock Gating Enabled during reset flows (i.e., clocks can be gated when they are not required to toggle for functionality, NOT Recommended) '1' : Clock Gating Disabled during reset flows. (i.e., clocks are toggling, always) Register bit defaults to value 1'b1, which is a requirement for due to Synchronous reset flops Randomizing this bit will result in X flush not completing during the simulation

VEBX Fault Counter

VEBX_FAULT_CNTR - VEBX Fault Counter		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	0490Ch	

DWord	Bit	Description
0	31:0	**VEBX Flt Counter** Default Value: 00000000h Access: RO This counter only applies to advance context when fault and stream mode is selected.

VEBX Fixed Counter

VEBX_FIXED_CNTR - VEBX Fixed Counter		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	04910h	

DWord	Bit	Description
0	31:0	**VEBX Fixed Count** Default Value: 00000000h Access: RO This counter only applies to advance context when fault and stream mode is selected.

VEO Current Pipe 0 XY Register

VEO_CURRENT0_XY - VEO Current Pipe 0 XY Register

Register Space:	MMIO: 0/2/0
Source:	VideoEnhancementCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1CA054h
ShortName:	VEO_CURRENT0_XY_VECS0
Address:	1DA054h
ShortName:	VEO_CURRENT0_XY_VECS1
Address:	1EA054h
ShortName:	VEO_CURRENT0_XY_VECS2
Address:	1FA054h
ShortName:	VEO_CURRENT0_XY_VECS3

DWord	Bit	Description
0	31:30	**Reserved**
	29:16	**Current Input Pipe 0 X** Default Value: 0h
	15	**Reserved**
	14:0	**Current Input Pipe 0 Y** Default Value: 0h

VEO DN Pipe 0 XY Register

VEO_DN0_XY - VEO DN Pipe 0 XY Register

Register Space:	MMIO: 0/2/0
Source:	VideoEnhancementCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1CA04Ch
ShortName:	VEO_DN0_XY_VECS0
Address:	1DA04Ch
ShortName:	VEO_DN0_XY_VECS1
Address:	1EA04Ch
ShortName:	VEO_DN0_XY_VECS2
Address:	1FA04Ch
ShortName:	VEO_DN0_XY_VECS3

DWord	Bit	Description
0	31:30	**Reserved**
	29:16	**DN Pipe 0 X** Default Value: 0h dn_input_x[13:0]
	15	**Reserved**
	14:0	**DN Pipe 0 Y** Default Value: 0h dn_input_y[14:0]

VEO DN Pipe 1 XY Register

VEO_DN1_XY - VEO DN Pipe 1 XY Register	
Register Space:	MMIO: 0/2/0
Source:	VideoEnhancementCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1CA050h
ShortName:	VEO_DN1_XY_VECS0
Address:	1DA050h
ShortName:	VEO_DN1_XY_VECS1
Address:	1EA050h
ShortName:	VEO_DN1_XY_VECS2
Address:	1FA050h
ShortName:	VEO_DN1_XY_VECS3

DWord	Bit	Description
0	31:30	**Reserved**
	29:16	**DN Pipe 1 X** Default Value: 0h
	15	**Reserved**
	14:0	**DN Pipe 1 Y** Default Value: 0h

VEO DV Count Register

VEO_DV_COUNT - VEO DV Count Register	
Register Space:	MMIO: 0/2/0
Source:	VideoEnhancementCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1CA044h
ShortName:	VEO_DV_COUNT_VECS0
Address:	1DA044h
ShortName:	VEO_DV_COUNT_VECS1
Address:	1EA044h
ShortName:	VEO_DV_COUNT_VECS2
Address:	1FA044h
ShortName:	VEO_DV_COUNT_VECS3

DWord	Bit	Description
0	31:24	**Pipe1 Motion History DV/Hold Maxcount** Default Value: 0h
	23:16	**Pipe1 Pixel History DV/Hold Maxcount** Default Value: 0h
	15:8	**Pipe0 Motion History DV/Hold Maxcount** Default Value: 0h
	7:0	**Pipe0 Pixel History DV/Hold Maxcount** Default Value: 0h

VEO DV Hold Register

VEO_DVHOLD - VEO DV Hold Register

Register Space:	MMIO: 0/2/0
Source:	VideoEnhancementCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1CA05Ch
ShortName:	VEO_DVHOLD_VECS0
Address:	1DA05Ch
ShortName:	VEO_DVHOLD_VECS1
Address:	1EA05Ch
ShortName:	VEO_DVHOLD_VECS2
Address:	1FA05Ch
ShortName:	VEO_DVHOLD_VECS3

Datavalid/Hold signals for VEO interface

DWord	Bit	Description
0	31	**vdn_p0_veo_pixel_dv** Default Value: 0h
	30	**veo_vdn_p0_pixel_hold** Default Value: 0h
	29	**vdn_p0_veo_mh_dv** Default Value: 0h
	28	**veo_vdn_p0_mh_hold** Default Value: 0h
	27	**vdn_p0_veo_bne_luma_dv** Default Value: 0h
	26	**veo_vdn_p0_bne_luma_hold** Default Value: 0h
	25	**vdn_p0_veo_bne_chroma_dv**

VEO_DVHOLD - VEO DV Hold Register

		Default Value: 0h
	24	**veo_vdn_p0_bne_chroma_hold** Default Value: 0h
	23	**vdi_p0_veo_pixel_dv** Default Value: 0h
	22	**veo_vdi_p0_pixel_hold** Default Value: 0h
	21	**vdi_p0_veo_stmm_dv** Default Value: 0h
	20	**veo_vdi_p0_stmm_hold** Default Value: 0h
	19	**vdi_p0_veo_fmd_dv** Default Value: 0h
	18	**veo_vdi_p0_fmd_hold** Default Value: 0h
	17	**iecp_p0_veo_dv** Default Value: 0h
	16	**veo_iecp_p0_hold** Default Value: 0h
	15	**vdn_p1_veo_pixel_dv** Default Value: 0h
	14	**veo_vdn_p1_pixel_hold** Default Value: 0h
	13	**vdn_p1_veo_mh_dv** Default Value: 0h
	12	**veo_vdn_p1_mh_hold** Default Value: 0h
	11	**vdn_p1_veo_bne_luma_dv** Default Value: 0h
	10	**veo_vdn_p1_bne_luma_hold** Default Value: 0h
	9	**vdn_p1_veo_bne_chroma_dv** Default Value: 0h
	8	**veo_vdn_p1_bne_chroma_hold** Default Value: 0h

VEO_DVHOLD - VEO DV Hold Register		
	7	**vdi_p1_veo_pixel_dv** Default Value: 0h
	6	**veo_vdi_p1_pixel_hold** Default Value: 0h
	5	**vdi_p1_veo_stmm_dv** Default Value: 0h
	4	**veo_vdi_p1_stmm_hold** Default Value: 0h
	3	**vdi_p1_veo_fmd_dv** Default Value: 0h
	2	**veo_vdi_p1_fmd_hold** Default Value: 0h
	1	**iecp_p1_veo_dv** Default Value: 0h
	0	**veo_iecp_p1_hold** Default Value: 0h

VEO IECP DV Count Register

VEO_IECP_DV_COUNT - VEO IECP DV Count Register	
Register Space:	MMIO: 0/2/0
Source:	VideoEnhancementCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1CA048h
ShortName:	VEO_IECP_DV_COUNT_VECS0
Address:	1DA048h
ShortName:	VEO_IECP_DV_COUNT_VECS1
Address:	1EA048h
ShortName:	VEO_IECP_DV_COUNT_VECS2
Address:	1FA048h
ShortName:	VEO_IECP_DV_COUNT_VECS3

DWord	Bit	Description
0	31:24	**IECP DV/Hold Maxcount** Default Value: 0h
	23:16	**DI/FMD DV/Hold Maxcount** Default Value: 0h
	15:8	**DI/STMM DV/Hold Maxcount** Default Value: 0h
	7:0	**DI Pixel DV/Hold Maxcount** Default Value: 0h

VEO Previous Pipe 0 XY Register

VEO_PREVIOUS0_XY - VEO Previous Pipe 0 XY Register	
Register Space:	MMIO: 0/2/0
Source:	VideoEnhancementCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1CA058h
ShortName:	VEO_PREVIOUS0_XY_VECS0
Address:	1DA058h
ShortName:	VEO_PREVIOUS0_XY_VECS1
Address:	1EA058h
ShortName:	VEO_PREVIOUS0_XY_VECS2
Address:	1FA058h
ShortName:	VEO_PREVIOUS0_XY_VECS3

DWord	Bit	Description
0	31:30	**Reserved**
	29:16	**Previous Input Pipe 0 X** Default Value: 0h
	15	**Reserved**
	14:0	**Previous Input Pipe 0 Y** Default Value: 0h

VEO State Register

VEO_STATE - VEO State Register

Register Space:	MMIO: 0/2/0
Source:	VideoEnhancementCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1CA040h
ShortName:	VEO_STATE_VECS0
Address:	1DA040h
ShortName:	VEO_STATE_VECS1
Address:	1EA040h
ShortName:	VEO_STATE_VECS2
Address:	1FA040h
ShortName:	VEO_STATE_VECS3

Data valids and holds for the statistics interface

DWord	Bit	Description	
0	31	**iecp_p0_veo_his_dv**	
		Default Value:	0h
	30	**iecp_p0_veo_skin_dv**	
		Default Value:	0h
	29	**iecp_p0_veo_rgb_his_dv**	
		Default Value:	0h
	28	**iecp_p0_veo_out_dist_dv**	
		Default Value:	0h
	27	**iecp_p1_veo_his_dv**	
		Default Value:	0h
	26	**iecp_p1_veo_skin_dv**	
		Default Value:	0h
	25	**iecp_p1_veo_out_dist_dv**	

VEO_STATE - VEO State Register

	Default Value:	0h
24	**veo_iecp_p0_rgb_his_hold**	
	Default Value:	0h
23	**Reserved**	
22:19	**VSC_FSM_State**	
	Default Value:	0h
	State of the VEO_VSC_CNTRL state machine	
18:16	**GAV Command Credit Count**	
	Value	**Name**
	4h	**[Default]**
15:12	**GAV Data Credit Count**	
	Value	**Name**
	8h	**[Default]**
11:8	**Reserved**	
	Format:	MBZ
7:0	**GAV Stall Clk Cnt Max**	
	Default Value:	0h
	The longest stall from GAV since the beginning of the frame.	

VE SFC Forced Lock Acknowledgement Register

VE_SFC_FORCED_LOCK_ACK - VE SFC Forced Lock Acknowledgement Register

Register Space:	MMIO: 0/2/0
Source:	VideoEnhancementCS
Access:	RO
Size (in bits):	32
Address:	1CA018h
ShortName:	VE_SFC_FORCED_LOCK_ACK_VECS0
Address:	1DA018h
ShortName:	VE_SFC_FORCED_LOCK_ACK_VECS1
Address:	1EA018h
ShortName:	VE_SFC_FORCED_LOCK_ACK_VECS2
Address:	1FA018h
ShortName:	VE_SFC_FORCED_LOCK_ACK_VECS3

DWord	Bit	Description
0	31:1	**Reserved** Format: MBZ
	0	**VE_SFC_FORCED_LOCK_ACK** Format: U1 This bit can only be set by hardware and it has to be clear by hardware as well. This bit is going to be polled by driver. This bit indicates that VE has received MFX_SFC_Forced_Lock from driver and it has sent that signal to SFC. Once this bit is set, it indicates SFC status (lock or unlock) will not be changed anymore. Driver will be safe to start the reset process after this bit is set. Hardware has to de-assert this bit after driver de-assert VE_SFC_Forced_Lock as well.

VE SFC Forced Lock Register

VE_SFC_FORCED_LOCK - VE SFC Forced Lock Register		
Register Space:	MMIO: 0/2/0	
Source:	VideoEnhancementCS	
Access:	WO	
Size (in bits):	32	
Address:	1CA01Ch	
Address:	1DA01Ch	
Address:	1EA01Ch	
Address:	1FA01Ch	

DWord	Bit	Description
0	31:1	**Reserved** Format: MBZ
	0	**VE_SFC_FORCED_LOCK** Format: U1 This bit can only be set by driver and it has to be clear by driver as well. Driver should set this bit before issuing the software (watchdog timer) reset. It tells VEBox that a software reset is going to happen. VE then issues a forced lock to SFC. If SFC is currently locked to VE, SFC should not unlock itself from VE. If SFC is NOT currently locked to VE, SFC should not accept the lock request from VE. Driver needs to clear this bit after the software reset sequence is complete.

VE VFW SFC Usage Register

VE_SFC_USAGE - VE VFW SFC Usage Register

Register Space:	MMIO: 0/2/0
Source:	VideoEnhancementCS
Access:	RO
Size (in bits):	32
Address:	1CA014h
ShortName:	VE_SFC_USAGE_VECS0
Address:	1DA014h
ShortName:	VE_SFC_USAGE_VECS1
Address:	1EA014h
ShortName:	VE_SFC_USAGE_VECS2
Address:	1FA014h
ShortName:	VE_SFC_USAGE_VECS3

DWord	Bit	Description
0	31:1	**Reserved** Format: MBZ
	0	**VE_SFC_USAGE** Format: U1 This bit can only be set by hardware and it has to be clear by hardware as well. This bit indicates SFC is currently locked to VE. This bit should be set after SFC accepts the lock request from VE. This bit should be clear once SFC finishes the workload and unlocked from VEBox. In case a reset happens on MFX, this bit must be reset once a new workload is received

VF_FENCE_LSB

VF_FENCE_LSB	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	100000h
Name:	VF_FENCE0_LSB
ShortName:	VF_FENCE0_LSB
Address:	100008h
Name:	VF_FENCE1_LSB
ShortName:	VF_FENCE1_LSB
Address:	100010h
Name:	VF_FENCE2_LSB
ShortName:	VF_FENCE2_LSB
Address:	100018h
Name:	VF_FENCE3_LSB
ShortName:	VF_FENCE3_LSB

Virtual Function Fence Registers LSBs

DWord	Bit	Description
0	31:12	**FENCELO** Default Value: 000000h Access: R/W Bits 31:12 of the ending Graphics Address of the fence region. Fence regions must be aligned to a 4KB page. This address represents the last 4KB page of the fence region (Lower Bound is included in the fence region). Graphics Address is the offset within GMADR space.
	11:2	**RESERVED** Default Value: 000h Access: RO Reserved
	1	**TILE** Default Value: 0b

VF_FENCE_LSB

		Access: R/W This field specifies the spatial ordering of QW within tiles. 0b - Consecutive SWords (32B) sequenced in the X direction 1b - Consecutive OWords (16B) sequenced in the Y direction
	0	**FENCEVAL** Access: R/W This field specifies whether or not this fence register defines a fence region. Value / Name 0b: Fence Invalid **[Default]** 1b: Fence Valid

VF_FENCE_MSB

VF_FENCE_MSB	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	100004h
Name:	VF_FENCE0_MSB
ShortName:	VF_FENCE0_MSB
Address:	10000Ch
Name:	VF_FENCE1_MSB
ShortName:	VF_FENCE1_MSB
Address:	100014h
Name:	VF_FENCE2_MSB
ShortName:	VF_FENCE2_MSB
Address:	10001Ch
Name:	VF_FENCE3_MSB
ShortName:	VF_FENCE3_MSB

Virtual Fence Registers MSBs

DWord	Bit	Description
0	31:12	**FENCEUP** Default Value: 00000000h Access: R/W Bits 31:12 of the ending Graphics Address of the fence region. Fence regions must be aligned to a 4KB page. This address represents the last 4KB page of the fence region (Upper Bound is included in the fence region). Graphics Address is the offset within GMADR space.
	11	**Reserved** Default Value: 0b Access: RO Reserved
	10:0	**Pitch** Default Value: 000h

VF_FENCE_MSB		
		Access: R/W This field specifies the width (pitch) of the fence region in multiple of tile widths. For Tile X this field must be programmed to a multiple of 512B (003 is the minimum value) and for Tile Y this field must be programmed to a multiple of 128B (000 is the minimum value). 000h = 128B 001h = 256B 002h = 384B 003h = 512B 004h = 640B 005h = 768B 006h = 896B 007h = 1024B ... 3FFh = 128KB 4FFh = 160KB 5FFh = 192KB 6FFh = 224KB 7FFh = 256KB

VF_SW_FLAG

VF_SW_FLAG	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	190240h
Name:	VF_SW_FLAG_0
ShortName:	VF_SW_FLAG_0
Address:	190244h
Name:	VF_SW_FLAG_1
ShortName:	VF_SW_FLAG_1
Address:	190248h
Name:	VF_SW_FLAG_2
ShortName:	VF_SW_FLAG_2
Address:	19024Ch
Name:	VF_SW_FLAG_3
ShortName:	VF_SW_FLAG_3

Each Virtual Function has 4x32bit Software Flag registers, which can be used as scratch registers.

DWord	Bit	Description
0	31:0	**Data** Default Value: 00000000h Access: R/W The format of this register is defined by Software.

VF Scratch Pad

VFSKPD - VF Scratch Pad

Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	32

Address:	083A8h-083ABh
Name:	VF Scratch Pad
ShortName:	VFSKPD_VFUNIT

Address:	16EA8h-16EABh
Name:	VF Scratch Pad
ShortName:	VFSKPD_VFRUNIT

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask[15:0] Must be set to modify corresponding bit in Bits 15:0. (All bits implemented)
	15	**VFCACHE deadlock disable** Access: R/W Format: PBC Value / Name / Description: 0h **[Default]** The vfcache will stall elements on a vertex boundary to ensure elements will be synchronized on vertex boundaries. 1h The vfcache will allow elements on a vertex boundary to get one element out of order.
	14:13	**Reserved** Access: R/W Format: PBC
	12	**Reserved**

VFSKPD - VF Scratch Pad

Access:	R/W
Format:	PBC

11 POLYGON PrimitiveID Fix Disable

Access:	R/W
Format:	Disable

Value	Name	Description
0h	Enable **[Default]**	PrimitiveID is constant across all triangles of a POLYGON.
1h	Disable	PrimitiveID is incremented for each triangle of a POLYGON.

10 VF POSH Starvation Disable

Access:	R/W
Format:	Disable

Value	Name	Description
0h	Enable **[Default]**	The VF will inform OVR when it is starved for POSH token data.
1h	Disable	The VF will not inform OVR when it is starved for POSH token data.

9 Partial Autostrip Disable

Access:	R/W
Format:	Disable

Value	Name	Description
0h	Enable **[Default]**	The VF can generate "partial autostrip" primitives from TRILIST inputs (if/when possible).
1h	Disable	VF will not generate "partial autostrip" primitives

8 Reserved

Access:	R/W
Format:	PBC

7 Reserved

Access:	R/W
Format:	PBC

6 Autostrip Disable

VFSKPD - VF Scratch Pad

Access:	R/W
Format:	U1

Value	Name	Description
0h	Enable **[Default]**	The VF can generate "autostrip" primitives from TRILIST inputs (if/when possible).
1h	Disable	VF will not generate "autostrip" primitives.

5 **TLB Prefectch Enable**

Access:	R/W
Format:	U1

Value	Name	Description
0h	Disable **[Default]**	The VF will generate prefetch of TLB when it is fetching sequential vertex data and four or fewer vertex buffers are valid.
1h	Enable	VF will disable prefetch of TLB entries.

4 **4th Vertex Data Pipe Disable**

Access:	R/W
Format:	Disable

Value	Name	Description
0h	**[Default]**	The 4th Vertex Data Pipe is enabled.
1h		The 4th Vertex Data Pipe is disabled.

Programming Notes
This is only valid when there are 3 or more vertex data pipes.

3 **Nullprim early credit release disable**

Access:	R/W

Value	Name	Description
0h	**[Default]**	The nullprim credit release will be returned to csunit when the upper pipe of vfunit is empty.
1h		The nullprim credit release will be returned to csunit when the upper pipe and the lower pipe of vfunit are empty.

VFSKPD - VF Scratch Pad

2 **Vertex Cache Implicit Disable Inhibit**

Access:	R/W
Format:	U1

Value	Name	Description
0h	**[Default]**	Allow VF to disable VS0 when Sequential index or Prim ID is a valid Element.
1h		VF never implicitly disables the vertex cache. Software must disable the VS0 Cache when required.

1 **Disable Over Fetch Cache**

Access:	R/W

Value	Name	Description
0h	**[Default]**	Cache will check for data in cache before making a request to memory
1h		Always re-fetch new data from memory.

Programming Notes
Note that the Disable Multiple Miss Read squash bit must be cleared for Disable Over Fetch Cache to be set.

0 **Disable Multiple Miss Read squash**

Access:	R/W
Format:	Disable

Value	Name	Description
0h	**[Default]**	Allow VF to squash reads that are to the same cacheline for vertex buffer requests.
1h		Disallow VF from squashing reads that are to the same cacheline for vertex buffer requests.

VFW Credit Count Register

VFW_CREDIT_CNT - VFW Credit Count Register	
Register Space:	MMIO: 0/2/0
Source:	VideoEnhancementCS
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1CA010h
ShortName:	VFW_CREDIT_CNT_VECS0
Address:	1DA010h
ShortName:	VFW_CREDIT_CNT_VECS1
Address:	1EA010h
ShortName:	VFW_CREDIT_CNT_VECS2
Address:	1FA010h
ShortName:	VFW_CREDIT_CNT_VECS3

DWord	Bit	Description
0	31:8	**Reserved**
	7:0	**Credit Count** The number of outstanding credits between VFW and GAV. If zero VEBOX cannot proceed due to GAV not releasing credits.

Value	Name
4h	**[Default]**

VGA_CONTROL

VGA_CONTROL

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	41000h-41003h
Name:	VGA Control
ShortName:	VGA_CONTROL
Power:	PG0
Reset:	global

Restriction
VGA requires panel fitting to be enabled. VGA is always connected to pipe A. VGA can not be enabled while the display power well is powered down. VGA display should only be enabled if all display planes other than VGA are disabled.

DWord	Bit	Description
0	31	**VGA Display Disable** This bit will disable the VGA compatible display mode. It has no effect on VGA register or A0000-BFFFF memory aperture accesses which are controlled by the PCI configuration and VGA I/O register settings. **Value** / **Name** 0b – Enable 1b – Disable **[Default]** **Restriction** The VGA SR01 screen off bit must be programmed when enabling and disabling VGA. See the VGA Registers document.
	30:27	**Reserved**
	26	**VGA Border Enable** This bit determines if the VGA border areas are included in the active display area. The border will be scaled along with the pixel data. **Value** / **Name** 0b – Disable 1b – Enable
	25	**DBuf Clock Gate**

VGA_CONTROL

Access:	R/W

The bit controls the Display buffer clocking when VGA is used.
Software must set this bit to 0b before enabling VGA and set it to 1b after VGA gets disabled.

24 Pipe CSC Enable

Description
This bit enables pipe color space conversion and the pipe pre-CSC gamma for the VGA pixel data.

Value	Name
0b	Disable
1b	Enable

23:21 Reserved

20 Legacy 8Bit Palette En

This bit affects reads and writes to the palette through VGA I/O addresses. In the 6-bit mode, the 8-bits of data are shifted up two bits on the write (upper two bits are lost) and shifted two bits down on the read. This provides backward compatibility for original VGA programs as well as VESA VBE support for 8-bit palette. It does not affect palette accesses through the palette register MMIO path.

Value	Name
0b	6 bit DAC
1b	8 bit DAC

19 Reserved

18 Reserved

17:16 Reserved

15:12 Reserved

11:8 Reserved

7:6 Blink Duty Cycle

Controls the VGA text mode blink duty cycle relative to the VGA cursor blink duty cycle.

Value	Name	Description
00b	100%	100% Duty Cycle, Full Cursor Rate
01b	25%	25% Duty Cycle, 1/2 Cursor Rate
10b	50%	50% Duty Cycle, 1/2 Cursor Rate
11b	75%	75% Duty Cycle, 1/2 Cursor Rate

5:0 VSYNC Blink Rate

Controls the VGA blink rate in terms of the number of VSYNCs per on/off cycle.

Programming Notes
Program with (VSYNCs/cycle)/2-1

VIDEO_DIP_CTL

VIDEO_DIP_CTL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	60200h-60203h
Name:	Transcoder A Video Data Island Packet Control
ShortName:	VIDEO_DIP_CTL_A
Power:	PG2
Reset:	soft
Address:	61200h-61203h
Name:	Transcoder B Video Data Island Packet Control
ShortName:	VIDEO_DIP_CTL_B
Power:	PG2
Reset:	soft
Address:	62200h-62203h
Name:	Transcoder C Video Data Island Packet Control
ShortName:	VIDEO_DIP_CTL_C
Power:	PG2
Reset:	soft
Address:	6F200h-6F203h
Name:	Transcoder EDP Video Data Island Packet Control
ShortName:	VIDEO_DIP_CTL_EDP
Power:	PG1
Reset:	soft

Each type of Video DIP will be sent once each frame while it is enabled.

DWord	Bit	Description
0	31:30	**Reserved**
	29	**Reserved**

VIDEO_DIP_CTL

28	**DRM DIP enable**

This bit enables the output of the Dynamic Range and Mastering info frame DIP.

Value	Name
1b	DRM DIP enable
0b	DRM DIP disable

Programming Notes
This needs to be enabled with HDMI only.

27	**Reserved**
26:25	**Reserved**
24	**Reserved**
23	**Reserved**
22:21	**Reserved**

20	**VDIP Enable VSC**

This bit enables the output of the Video Stream Configuration DIP.

Value	Name
0b	Disable VSC DIP
1b	Enable VSC DIP

Restriction
VSC can only be enabled with DisplayPort. VSC should be enabled prior to enabling PSR or stereo 3D if VSC will be used to transmit stereo 3D related information.

19:17	**Reserved**

16	**VDIP Enable GCP**

This bit enables the output of the General Control Packet (GCP) DIP. GCP is different from other DIPs in that much of the payload is automatically reflected in the packet, and therefore there is a VIDEO_DIP_GCP register instead of DIP data buffers for GCP.

Value	Name
0b	Disable GCP DIP
1b	Enable GCP DIP

VIDEO_DIP_CTL

		Restriction GCP is only supported with HDMI when the bits per color is not equal to 8. GCP must be enabled prior to enabling TRANS_DDI_FUNC_CTL for HDMI with bits per color not equal to 8 and disabled after disabling TRANS_DDI_FUNC_CTL
	15:13	**Reserved**
	12	**VDIP Enable AVI** This bit enables the output of the Auxiliary Video Information DIP. **Value** / **Name** 0b – Disable AVI DIP 1b – Enable AVI DIP **Restriction** Only enable with HDMI.
	11:9	**Reserved**
	8	**VDIP Enable VS** This bit enables the output of the Vendor Specific (VS) DIP. **Value** / **Name** 0b – Disable VS DIP 1b – Enable VS DIP **Restriction** Only enable with HDMI.
	7:5	**Reserved**
	4	**VDIP Enable GMP** This bit enables the output of the Gamut Metadata Packet (GMP) DIP. GMP can be enabled with either DisplayPort or HDMI. **Value** / **Name** 0b – Disable GMP DIP 1b – Enable GMP DIP
	3:1	**Reserved**
	0	**VDIP Enable SPD** This bit enables the output of the Source Product Description (SPD) DIP. **Value** / **Name** 0b – Disable SPD DIP 1b – Enable SPD DIP **Restriction** Only enable with HDMI.

VIDEO_DIP_DATA

VIDEO_DIP_DATA	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	60220h-6023Fh
Name:	Transcoder A Video Data Island Packet AVI Data
ShortName:	VIDEO_DIP_AVI_DATA_A_*
Power:	PG2
Reset:	soft
Address:	60260h-6027Fh
Name:	Transcoder A Video Data Island Packet VS Data
ShortName:	VIDEO_DIP_VS_DATA_A_*
Power:	PG2
Reset:	soft
Address:	602A0h-602BFh
Name:	Transcoder A Video Data Island Packet SPD Data
ShortName:	VIDEO_DIP_SPD_DATA_A_*
Power:	PG2
Reset:	soft
Address:	6F2E0h-6F2FFh
Name:	Transcoder EDP Video Data Island Packet GMP Data
ShortName:	VIDEO_DIP_GMP_DATA_EDP_*
Power:	PG1
Reset:	soft
Address:	602E0h-602FFh
Name:	Transcoder A Video Data Island Packet GMP Data
ShortName:	VIDEO_DIP_GMP_DATA_A_*

VIDEO_DIP_DATA	
Power:	PG2
Reset:	soft
Address:	60320h-60343h
Name:	Transcoder A Video Data Island Packet VSC Data
ShortName:	VIDEO_DIP_VSC_DATA_A_*
Power:	PG2
Reset:	soft
Address:	61220h-6123Fh
Name:	Transcoder B Video Data Island Packet AVI Data
ShortName:	VIDEO_DIP_AVI_DATA_B_*
Power:	PG2
Reset:	soft
Address:	61260h-6127Fh
Name:	Transcoder B Video Data Island Packet VS Data
ShortName:	VIDEO_DIP_VS_DATA_B_*
Power:	PG2
Reset:	soft
Address:	612A0h-612BFh
Name:	Transcoder B Video Data Island Packet SPD Data
ShortName:	VIDEO_DIP_SPD_DATA_B_*
Power:	PG2
Reset:	soft
Address:	612E0h-612FFh
Name:	Transcoder B Video Data Island Packet GMP Data
ShortName:	VIDEO_DIP_GMP_DATA_B_*
Power:	PG2
Reset:	soft
Address:	61320h-61343h
Name:	Transcoder B Video Data Island Packet VSC Data
ShortName:	VIDEO_DIP_VSC_DATA_B_*

VIDEO_DIP_DATA

Power:	PG2
Reset:	soft
Address:	62220h-6223Fh
Name:	Transcoder C Video Data Island Packet AVI Data
ShortName:	VIDEO_DIP_AVI_DATA_C_*
Power:	PG2
Reset:	soft
Address:	62260h-6227Fh
Name:	Transcoder C Video Data Island Packet VS Data
ShortName:	VIDEO_DIP_VS_DATA_C_*
Power:	PG2
Reset:	soft
Address:	622A0h-622BFh
Name:	Transcoder C Video Data Island Packet SPD Data
ShortName:	VIDEO_DIP_SPD_DATA_C_*
Power:	PG2
Reset:	soft
Address:	622E0h-622FFh
Name:	Transcoder C Video Data Island Packet GMP Data
ShortName:	VIDEO_DIP_GMP_DATA_C_*
Power:	PG2
Reset:	soft
Address:	62320h-62343h
Name:	Transcoder C Video Data Island Packet VSC Data
ShortName:	VIDEO_DIP_VSC_DATA_C_*
Power:	PG2
Reset:	soft
Address:	6F320h-6F343h
Name:	Transcoder EDP Video Data Island Packet VSC Data
ShortName:	VIDEO_DIP_VSC_DATA_EDP_*

VIDEO_DIP_DATA

Power: PG1

Reset: soft

There are multiple instances of this register format per DIP type and per transcoder.

DWord	Bit	Description
0	31:0	**Video DIP DATA** This field contains the video DIP data to be transmitted. **Restriction** Data should be loaded before enabling the transmission through the DIP type enable bit.

VIDEO_DIP_DRM_DATA

VIDEO_DIP_DRM_DATA - VIDEO_DIP_DRM_DATA	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	60440h-6045Fh
Name:	Transcoder A Video Data Island Packet for DRM
ShortName:	VIDEO_DIP_DRM_DATA_A_*
Power:	PG2
Reset:	soft
Address:	61440h-6145Fh
Name:	Transcoder B Video Data Island Packet for DRM
ShortName:	VIDEO_DIP_DRM_DATA_B_*
Power:	PG2
Reset:	soft
Address:	62440h-6245Fh
Name:	Transcoder C Video Data Island Packet for DRM
ShortName:	VIDEO_DIP_DRM_DATA_C_*
Power:	PG2
Reset:	soft

HDMI 2.0 Dynamic Range Mastering Infoframe DIP data.

DWord	Bit	Description
0	31:0	**DRM DIP data**

VIDEO_DIP_DRM_ECC

VIDEO_DIP_DRM_ECC - VIDEO_DIP_DRM_ECC	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	60460h-60467h
Name:	Transcoder A Video Data Island Packet for DRM ECC
ShortName:	VIDEO_DIP_DRM_ECC_A_*
Power:	PG2
Reset:	soft
Address:	61460h-61467h
Name:	Transcoder B Video Data Island Packet for DRM ECC
ShortName:	VIDEO_DIP_DRM_ECC_B_*
Power:	PG2
Reset:	soft
Address:	62460h-62467h
Name:	Transcoder C Video Data Island Packet for DRM ECC
ShortName:	VIDEO_DIP_DRM_ECC_C_*
Power:	PG2
Reset:	soft

HDMI 2.0 Dynamic Range and Mastering Infoframe ECC data.

DWord	Bit	Description
0	31:0	**DRM ECC data**

VIDEO_DIP_ECC

VIDEO_DIP_ECC	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	60240h-60247h
Name:	Transcoder A Video Data Island Packet AVI ECC
ShortName:	VIDEO_DIP_AVI_ECC_A_*
Power:	PG2
Reset:	soft
Address:	60280h-60287h
Name:	Transcoder A Video Data Island Packet VS ECC
ShortName:	VIDEO_DIP_VS_ECC_A_*
Power:	PG2
Reset:	soft
Address:	602C0h-602C7h
Name:	Transcoder A Video Data Island Packet SPD ECC
ShortName:	VIDEO_DIP_SPD_ECC_A_*
Power:	PG2
Reset:	soft
Address:	60300h-60313h
Name:	Transcoder A Video Data Island Packet GMP ECC
ShortName:	VIDEO_DIP_GMP_ECC_A_*
Power:	PG2
Reset:	soft
Address:	60344h-6034Fh
Name:	Transcoder A Video Data Island Packet VSC ECC
ShortName:	VIDEO_DIP_VSC_ECC_A_*

VIDEO_DIP_ECC	
Power:	PG2
Reset:	soft
Address:	61240h-61247h
Name:	Transcoder B Video Data Island Packet AVI ECC
ShortName:	VIDEO_DIP_AVI_ECC_B_*
Power:	PG2
Reset:	soft
Address:	61280h-61287h
Name:	Transcoder B Video Data Island Packet VS ECC
ShortName:	VIDEO_DIP_VS_ECC_B_*
Power:	PG2
Reset:	soft
Address:	612C0h-612C7h
Name:	Transcoder B Video Data Island Packet SPD ECC
ShortName:	VIDEO_DIP_SPD_ECC_B_*
Power:	PG2
Reset:	soft
Address:	61300h-61313h
Name:	Transcoder B Video Data Island Packet GMP ECC
ShortName:	VIDEO_DIP_GMP_ECC_B_*
Power:	PG2
Reset:	soft
Address:	61344h-6134Fh
Name:	Transcoder B Video Data Island Packet VSC ECC
ShortName:	VIDEO_DIP_VSC_ECC_B_*
Power:	PG2
Reset:	soft
Address:	62240h-62247h
Name:	Transcoder C Video Data Island Packet AVI ECC
ShortName:	VIDEO_DIP_AVI_ECC_C_*

VIDEO_DIP_ECC

Power:	PG2
Reset:	soft
Address:	62280h-62287h
Name:	Transcoder C Video Data Island Packet VS ECC
ShortName:	VIDEO_DIP_VS_ECC_C_*
Power:	PG2
Reset:	soft
Address:	622C0h-622C7h
Name:	Transcoder C Video Data Island Packet SPD ECC
ShortName:	VIDEO_DIP_SPD_ECC_C_*
Power:	PG2
Reset:	soft
Address:	62300h-62313h
Name:	Transcoder C Video Data Island Packet GMP ECC
ShortName:	VIDEO_DIP_GMP_ECC_C_*
Power:	PG2
Reset:	soft
Address:	62344h-6234Fh
Name:	Transcoder C Video Data Island Packet VSC ECC
ShortName:	VIDEO_DIP_VSC_ECC_C_*
Power:	PG2
Reset:	soft
Address:	6F300h-6F313h
Name:	Transcoder EDP Video Data Island Packet GMP ECC
ShortName:	VIDEO_DIP_GMP_ECC_EDP_*
Power:	PG1
Reset:	soft
Address:	6F344h-6F34Fh
Name:	Transcoder EDP Video Data Island Packet VSC ECC
ShortName:	VIDEO_DIP_VSC_ECC_EDP_*

VIDEO_DIP_ECC

Power: PG1

Reset: soft

There are multiple instances of this register format per DIP type and per transcoder.

DWord	Bit	Description
0	31:0	**Video DIP ECC** This field contains the video DIP ECC value for read back.

VIDEO_DIP_GCP

VIDEO_DIP_GCP

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32

Address:	60210h-60213h
Name:	Transcoder A Video Data Island Packet GCP
ShortName:	VIDEO_DIP_GCP_A
Power:	PG2
Reset:	soft

Address:	61210h-61213h
Name:	Transcoder B Video Data Island Packet GCP
ShortName:	VIDEO_DIP_GCP_B
Power:	PG2
Reset:	soft

Address:	62210h-62213h
Name:	Transcoder C Video Data Island Packet GCP
ShortName:	VIDEO_DIP_GCP_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31:3	**Reserved** Format: MBZ
	2	**GCP color indication** Value / Name / Description: 0b / Don't Indicate / Don't indicate color depth. CD and PP bits in GCP set to zero. 1b / Indicate / Indicate color depth using CD bits in GCP. The color depth value comes from the TRANS_DDI_FUNC_CTL register. Restriction

VIDEO_DIP_GCP

		This bit must be set when in HDMI deep color (>8 BPC) mode.
	1	**GCP default phase enable** GCP default phase indicates that video timings meet alignment requirements such that the following conditions are met: 1. Htotal is a multiple of the value given in the table below 2. Hactive is an even number 3. Front and back porches for Hsync are even numbers 4. Vsync always starts on an even-numbered pixel within a line in interlaced modes (starting counting with 0)

BPC	Color Format	Htotal Multiple Requirement
8	RGB	2
8	YUV420	4
10	RGB	4
10	YUV420	8
12	RGB	2
12	YUV420	4

Value	Name	Description
0b	Clear	Default phase bit in GCP is cleared.
1b	Set	Default phase bit in GCP is set.

Restriction
Do not set this bit if these requirements are not met.

	0	**Reserved**

VS Invocation Counter

VS_INVOCATION_COUNT - VS Invocation Counter	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02320h-02327h
Name:	VS Invocation Counter
ShortName:	VS_INVOCATION_COUNT_RCSUNIT_BE_GEOMETRY
Address:	18320h-18327h
Name:	VS Invocation Counter
ShortName:	VS_INVOCATION_COUNT_POCSUNIT_BE_GEOMETRY
Address:	02320h-02327h
Name:	VS Invocation Counter
ShortName:	VS_INVOCATION_COUNT_RCSUNIT_BE
Address:	18320h-18327h
Name:	VS Invocation Counter
ShortName:	VS_INVOCATION_COUNT_POCSUNIT_BE
This register stores the value of the vertex count shaded by VS. This register is part of the context save and restore.	

DWord	Bit	Description
0..1	63:32	**VS Invocation Count Report UDW** Number of vertices that are dispatched as threads by the VS stage. Updated only when **Statistics Enable** is set in VS_STATE (see the Vertex Shader Chapter in the 3D Volume.)
	31:0	**VS Invocation Count Report LDW** Number of vertices that are dispatched as threads by the VS stage. Updated only when **Statistics Enable** is set in VS_STATE (see the Vertex Shader Chapter in the 3D Volume.)

VSR_PUSH_CONSTANT_BASE

VSR_PUSH_CONSTANT_BASE - VSR_PUSH_CONSTANT_BASE		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Size (in bits):	32	
Address:	0E518h	
Name:	VSR_PUSH_CONSTANT_BASE	
ShortName:	VSR_PUSH_CONSTANT_BASE	

DWord	Bit	Description
0	31:17	**Reserved** Default Value: 000000000000000b Access: RO Format: MBZ
	16:6	**VSR PUSH CONSTANT BASE** Default Value: 200h Access: R/W This is a 64 Byte aligned offset in to the URB indicating the base of the push constant allocation space for the push constant allocation space for VSR unit in POSH pipeline. The offset and size of the VSR allocation is relative to this base address.
	5:0	**Reserved** Access: RO Format: MBZ

Wait For Event and Display Flip Flags Register

SYNC_FLIP_STATUS - Wait For Event and Display Flip Flags Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	022D0h-022D3h
Name:	Wait For Event and Display Flip Flags Register
ShortName:	SYNC_FLIP_STATUS_RCSUNIT
Address:	182D0h-182D3h
Name:	Wait For Event and Display Flip Flags Register
ShortName:	SYNC_FLIP_STATUS_POCSUNIT
Address:	222D0h-222D3h
Name:	Wait For Event and Display Flip Flags Register
ShortName:	SYNC_FLIP_STATUS_BCSUNIT
Address:	1C02D0h-1C02D3h
Name:	Wait For Event and Display Flip Flags Register
ShortName:	SYNC_FLIP_STATUS_VCSUNIT0
Address:	1C42D0h-1C42D3h
Name:	Wait For Event and Display Flip Flags Register
ShortName:	SYNC_FLIP_STATUS_VCSUNIT1
Address:	1C82D0h-1C82D3h
Name:	Wait For Event and Display Flip Flags Register
ShortName:	SYNC_FLIP_STATUS_VECSUNIT0
Address:	1D02D0h-1D02D3h
Name:	Wait For Event and Display Flip Flags Register
ShortName:	SYNC_FLIP_STATUS_VCSUNIT2

SYNC_FLIP_STATUS - Wait For Event and Display Flip Flags Register

Address:	1D42D0h-1D42D3h
Name:	Wait For Event and Display Flip Flags Register
ShortName:	SYNC_FLIP_STATUS_VCSUNIT3

Address:	1D82D0h-1D82D3h
Name:	Wait For Event and Display Flip Flags Register
ShortName:	SYNC_FLIP_STATUS_VECSUNIT1

Address:	1E02D0h-1E02D3h
Name:	Wait For Event and Display Flip Flags Register
ShortName:	SYNC_FLIP_STATUS_VCSUNIT4

Address:	1E42D0h-1E42D3h
Name:	Wait For Event and Display Flip Flags Register
ShortName:	SYNC_FLIP_STATUS_VCSUNIT5

Address:	1E82D0h-1E82D3h
Name:	Wait For Event and Display Flip Flags Register
ShortName:	SYNC_FLIP_STATUS_VECSUNIT2

Address:	1F02D0h-1F02D3h
Name:	Wait For Event and Display Flip Flags Register
ShortName:	SYNC_FLIP_STATUS_VCSUNIT6

Address:	1F42D0h-1F42D3h
Name:	Wait For Event and Display Flip Flags Register
ShortName:	SYNC_FLIP_STATUS_VCSUNIT7

Address:	1F82D0h-1F82D3h
Name:	Wait For Event and Display Flip Flags Register
ShortName:	SYNC_FLIP_STATUS_VECSUNIT3

This register is the saved value of what wait for events are still valid. This register is part of context save and

SYNC_FLIP_STATUS - Wait For Event and Display Flip Flags Register

restore for RC6 feature.

Programming Notes	Source
Programming Restriction: This register should NEVER be programmed by SW, this is for HW internal use only.	
VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be exercised for reads or writes.	VideoCS, VideoCS2, VideoEnhancementCS

DWord	Bit	Description
0	31	**Reserved** Format: MBZ
	30	**Display Plane 1 Asynchronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 1 "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	29	**Display Plane 1 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 1 "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	28	**Display Plane 4 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 4 "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	27	**Reserved** Format: MBZ
	26	**Display Plane 2 Asynchronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 2 "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS - Wait For Event and Display Flip Flags Register

	25	**Display Plane 2 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	24	**Display Plane 5 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 5 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	23	**Reserved** Source: BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS Format: MBZ
	23	**Display Plane 1 Asynchronous Performance Flip Pending Wait Enable** Source: RenderCS Format: Enable This field enables a wait for the duration of a Display Plane 1 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	22	**Display Plane 1 Asynchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 1 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	21	**Display Plane 1 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 1 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	20	**Display Plane 4 Synchronous Flip Pending Wait Enable**

SYNC_FLIP_STATUS - Wait For Event and Display Flip Flags Register

		Format: Enable This field enables a wait for the duration of a Display Plane 4 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	19	**Reserved** Format: MBZ
	18	**Display Pipe A Scan Line Wait Enable** Format: Enable This field enables a wait while a Display Pipe A Scan Line condition exists. This condition is defined as the the start of the scan line specified in the Pipe A Display Scan Line Count Range Compare Register. See Scan Line Event in the Device Programming Interface chapter of MI Functions.
	17	**Display Pipe A Vertical Blank Wait Enable** Format: Enable This field enables a wait until the next Display Pipe A Vertical Blank event occurs. This event is defined as the start of the next Display Pipe A vertical blank period. Note that this can cause a wait for up to an entire refresh period. See Vertical Blank Event (See Programming Interface).
	16	**Reserved** Format: MBZ
	15	**Reserved** Source: BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS Format: MBZ
	15	**Display Plane 2 Asynchronous Performance Flip Pending Wait Enable** Source: RenderCS Format: Enable This field enables a wait for the duration of a Display Plane 2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	14	**Display Plane 2 Asynchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS - Wait For Event and Display Flip Flags Register

	13	**Display Plane 2 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	12	**Display Plane 5 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 5 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	11	**Reserved** Format: MBZ
	10	**Display Pipe B Scan Line Wait Enable** Format: Enable This field enables a wait while a Display Pipe B Scan Line condition exists. This condition is defined as the the start of the scan line specified in the Pipe B Display Scan Line Count Range Compare Register. See Scan Line Event in the Device Programming Interface chapter of MI Functions.
	9	**Display Pipe B Vertical Blank Wait Enable** Format: Enable This field enables a wait until the next Display Pipe B Vertical Blank event occurs. This event is defined as the start of the next Display Pipe B vertical blank period. Note that this can cause a wait for up to an entire refresh period. See Vertical Blank Event (See Programming Interface).
	8:0	**Reserved** Format: MBZ

Wait For Event and Display Flip Flags Register 1

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	022D4h-022D7h
Name:	Wait For Event and Display Flip Flags Register 1
ShortName:	SYNC_FLIP_STATUS_1_RCSUNIT
Address:	182D4h-182D7h
Name:	Wait For Event and Display Flip Flags Register 1
ShortName:	SYNC_FLIP_STATUS_1_POCSUNIT
Address:	222D4h-222D7h
Name:	Wait For Event and Display Flip Flags Register 1
ShortName:	SYNC_FLIP_STATUS_1_BCSUNIT
Address:	1C02D4h-1C02D7h
Name:	Wait For Event and Display Flip Flags Register 1
ShortName:	SYNC_FLIP_STATUS_1_VCSUNIT0
Address:	1C42D4h-1C42D7h
Name:	Wait For Event and Display Flip Flags Register 1
ShortName:	SYNC_FLIP_STATUS_1_VCSUNIT1
Address:	1C82D4h-1C82D7h
Name:	Wait For Event and Display Flip Flags Register 1
ShortName:	SYNC_FLIP_STATUS_1_VECSUNIT0
Address:	1D02D4h-1D02D7h
Name:	Wait For Event and Display Flip Flags Register 1
ShortName:	SYNC_FLIP_STATUS_1_VCSUNIT2

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

Address:	1D42D4h-1D42D7h
Name:	Wait For Event and Display Flip Flags Register 1
ShortName:	SYNC_FLIP_STATUS_1_VCSUNIT3
Address:	1D82D4h-1D82D7h
Name:	Wait For Event and Display Flip Flags Register 1
ShortName:	SYNC_FLIP_STATUS_1_VECSUNIT1
Address:	1E02D4h-1E02D7h
Name:	Wait For Event and Display Flip Flags Register 1
ShortName:	SYNC_FLIP_STATUS_1_VCSUNIT4
Address:	1E42D4h-1E42D7h
Name:	Wait For Event and Display Flip Flags Register 1
ShortName:	SYNC_FLIP_STATUS_1_VCSUNIT5
Address:	1E82D4h-1E82D7h
Name:	Wait For Event and Display Flip Flags Register 1
ShortName:	SYNC_FLIP_STATUS_1_VECSUNIT2
Address:	1F02D4h-1F02D7h
Name:	Wait For Event and Display Flip Flags Register 1
ShortName:	SYNC_FLIP_STATUS_1_VCSUNIT6
Address:	1F42D4h-1F42D7h
Name:	Wait For Event and Display Flip Flags Register 1
ShortName:	SYNC_FLIP_STATUS_1_VCSUNIT7
Address:	1F82D4h-1F82D7h
Name:	Wait For Event and Display Flip Flags Register 1
ShortName:	SYNC_FLIP_STATUS_1_VECSUNIT3

This register is the saved value of what wait for events are still valid. This register is part of context save and

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

restore for RC6 feature.

Programming Notes	Source
Programming Restriction: This register should NEVER be programmed by SW, this is for HW internal use only.	
VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be exercised for reads or writes.	VideoCS, VideoCS2, VideoEnhancementCS

DWord	Bit	Description
0	31:27	**Reserved** Format: MBZ
	26	**Display Plane 12 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 12 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	25	**Display Plane 12 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 12 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	24	**Display Plane 11 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 11 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	23	**Display Plane 11 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 11 Flip Pending condition. If a flip

		request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	22	**Display Plane 10 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 10 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	21	**Display Plane 10 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 10 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	20	**Display Plane 9 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 9 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	19	**Display Plane 9 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 9 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	18	**Display Plane 8 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 8 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

	17	**Display Plane 8 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 8 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	16	**Display Plane 7 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 7 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	15	**Display Plane 7 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 7 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	14	**Display Pipe C Scan Line Event Pending** Format: Enable This field indicates scan line event operation is pending from Display Pipe C. This field gets set when MI_SCANLINE_INCL/EXCL command is parsed for Display Plane-C and gets reset on scan line event completion for Display Plane-C.
	13	**Display Pipe B Scan Line Event Pending** Format: Enable This field indicates scan line event operation is pending from Display Pipe B. This field gets set when MI_SCANLINE_INCL/EXCL command is parsed for Display Plane-B and gets reset on scan line event completion for Display Plane 3.
	12	**Display Pipe A Scan Line Event Pending** Format: Enable This field indicates scan line event operation is pending from Display Pipe A. This field gets set when MI_SCANLINE_INCL/EXCL command is parsed for Display Plane-A and gets reset on scan line event completion for Display Plane 1.

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

	11	**Reserved** Format: MBZ
	10	**Display Plane 3 Asynchronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	9	**Display Plane 3 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	8	**Display Plane 6 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 6 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	7	**Reserved** Source: BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS Format: MBZ
	7	**Display Plane 3 Asynchronous Performance Flip Pending Wait Enable** Source: RenderCS Format: Enable This field enables a wait for the duration of a Display Plane 3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	6	**Display Plane 3 Asynchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 3 "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

		Pending Condition (in the Device Programming Interface chapter of MI Functions.
	5	**Display Plane 3 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	4	**Display Plane 6 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 6 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	3	**Reserved** Format: MBZ
	2	**Display Pipe C Scan Line Wait Enable** Format: Enable This field enables a wait while a Display Pipe C Scan Line condition exists. This condition is defined as the start of the scan line specified in the Pipe C Display Scan Line Count Range Compare Register. See Scan Line Event in the Device Programming Interface chapter of MI Functions.
	1	**Display Pipe C Vertical Blank Wait Enable** Format: Enable This field enables a wait until the next Display Pipe C Vertical Blank event occurs. This event is defined as the start of the next Display Pipe C vertical blank period. Note that this can cause a wait for up to an entire refresh period. See Vertical Blank Event (See Programming Interface).
	0	**Reserved** Format: MBZ

Wait For Event and Display Flip Flags Register 2

SYNC_FLIP_STATUS_2 - Wait For Event and Display Flip Flags Register 2	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	022ECh-022EFh
Name:	Wait For Event and Display Flip Flags Register 2
ShortName:	SYNC_FLIP_STATUS_2_RCSUNIT
Address:	182ECh-182EFh
Name:	Wait For Event and Display Flip Flags Register 2
ShortName:	SYNC_FLIP_STATUS_2_POCSUNIT
Address:	222ECh-222EFh
Name:	Wait For Event and Display Flip Flags Register 2
ShortName:	SYNC_FLIP_STATUS_2_BCSUNIT
Address:	1C02ECh-1C02EFh
Name:	Wait For Event and Display Flip Flags Register 2
ShortName:	SYNC_FLIP_STATUS_2_VCSUNIT0
Address:	1C42ECh-1C42EFh
Name:	Wait For Event and Display Flip Flags Register 2
ShortName:	SYNC_FLIP_STATUS_2_VCSUNIT1
Address:	1C82ECh-1C82EFh
Name:	Wait For Event and Display Flip Flags Register 2
ShortName:	SYNC_FLIP_STATUS_2_VECSUNIT0
Address:	1D02ECh-1D02EFh
Name:	Wait For Event and Display Flip Flags Register 2
ShortName:	SYNC_FLIP_STATUS_2_VCSUNIT2

SYNC_FLIP_STATUS_2 - Wait For Event and Display Flip Flags Register 2

Address:	1D42ECh-1D42EFh
Name:	Wait For Event and Display Flip Flags Register 2
ShortName:	SYNC_FLIP_STATUS_2_VCSUNIT3
Address:	1D82ECh-1D82EFh
Name:	Wait For Event and Display Flip Flags Register 2
ShortName:	SYNC_FLIP_STATUS_2_VECSUNIT1
Address:	1E02ECh-1E02EFh
Name:	Wait For Event and Display Flip Flags Register 2
ShortName:	SYNC_FLIP_STATUS_2_VCSUNIT4
Address:	1E42ECh-1E42EFh
Name:	Wait For Event and Display Flip Flags Register 2
ShortName:	SYNC_FLIP_STATUS_2_VCSUNIT5
Address:	1E82ECh-1E82EFh
Name:	Wait For Event and Display Flip Flags Register 2
ShortName:	SYNC_FLIP_STATUS_2_VECSUNIT2
Address:	1F02ECh-1F02EFh
Name:	Wait For Event and Display Flip Flags Register 2
ShortName:	SYNC_FLIP_STATUS_2_VCSUNIT6
Address:	1F42ECh-1F42EFh
Name:	Wait For Event and Display Flip Flags Register 2
ShortName:	SYNC_FLIP_STATUS_2_VCSUNIT7
Address:	1F82ECh-1F82EFh
Name:	Wait For Event and Display Flip Flags Register 2
ShortName:	SYNC_FLIP_STATUS_2_VECSUNIT3

This register is the saved value of what wait for events are still valid. This register is part of context save and

SYNC_FLIP_STATUS_2 - Wait For Event and Display Flip Flags Register 2

restore for RC6 feature.

Programming Notes	Source
Programming Restriction: This register should NEVER be programmed by SW, this is for HW internal use only.	
VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be exercised for reads or writes.	VideoCS, VideoCS2, VideoEnhancementCS

DWord	Bit	Description
0	31:27	**Reserved** Format: MBZ
	26	**Display Plane 12 Asynchronous Performance Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 12 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	25	**Display Plane 12 Asynchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 12 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	24	**Display Plane 12 Asynchronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 12 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	23	**Display Plane 11 Asynchronous Performance Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 11 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	22	**Display Plane 11 Asynchronous Flip Pending Wait Enable** Format: Enable

SYNC_FLIP_STATUS_2 - Wait For Event and Display Flip Flags Register 2

		This field enables a wait for the duration of a Display Plane 11 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	21	**Display Plane 11 Asynchronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 11 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	20	**Display Plane 10 Asynchronous Performance Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 10 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	19	**Display Plane 10 Asynchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 10 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	18	**Display Plane 10 Asynchronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 10 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	17	**Display Plane 9 Asynchronous Performance Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 9 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	16	**Display Plane 9 Asynchronous Flip Pending Wait Enable**

SYNC_FLIP_STATUS_2 - Wait For Event and Display Flip Flags Register 2

		Format: Enable This field enables a wait for the duration of a Display Plane 9 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	15	**Display Plane 9 Asynchronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 9 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	14	**Display Plane 8 Asynchronous Performance Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 8 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	13	**Display Plane 8 Asynchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 8 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	12	**Display Plane 8 Asynchronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 8 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	11	**Display Plane 7 Asynchronous Performance Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 7 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_2 - Wait For Event and Display Flip Flags Register 2

	10	**Display Plane 7 Asynchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 7 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	9	**Display Plane 7 Asynchronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 7 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	8	**Display Plane 6 Asynchronous Performance Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 6 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	7	**Display Plane 6 Asynchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 6 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	6	**Display Plane 6 Asynchronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 6 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	5	**Display Plane 5 Asynchronous Performance Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 5 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_2 - Wait For Event and Display Flip Flags Register 2

	4	**Display Plane 5 Asynchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 5 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	3	**Display Plane 5 Asynchronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 5 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	2	**Display Plane 4 Asynchronous Performance Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 4 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	1	**Display Plane 4 Asynchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 4 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	0	**Display Plane 4 Asynchronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 4 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

Wait For Event and Display Flip Flags Register 3

SYNC_FLIP_STATUS_3 - Wait For Event and Display Flip Flags Register 3	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	022B8h-022BBh
Name:	SYNC_FLIP_STATUS_3
ShortName:	SYNC_FLIP_STATUS_3_RCSUNIT
Address:	182B8h-182BBh
Name:	SYNC_FLIP_STATUS_3
ShortName:	SYNC_FLIP_STATUS_3_POCSUNIT
Address:	222B8h-222BBh
Name:	SYNC_FLIP_STATUS_3
ShortName:	SYNC_FLIP_STATUS_3_BCSUNIT
Address:	1C02B8h-1C02BBh
Name:	SYNC_FLIP_STATUS_3
ShortName:	SYNC_FLIP_STATUS_3_VCSUNIT0
Address:	1C42B8h-1C42BBh
Name:	SYNC_FLIP_STATUS_3
ShortName:	SYNC_FLIP_STATUS_3_VCSUNIT1
Address:	1C82B8h-1C82BBh
Name:	SYNC_FLIP_STATUS_3
ShortName:	SYNC_FLIP_STATUS_3_VECSUNIT0
Address:	1D02B8h-1D02BBh
Name:	SYNC_FLIP_STATUS_3
ShortName:	SYNC_FLIP_STATUS_3_VCSUNIT2

SYNC_FLIP_STATUS_3 - Wait For Event and Display Flip Flags Register 3

Address:	1D42B8h-1D42BBh
Name:	SYNC_FLIP_STATUS_3
ShortName:	SYNC_FLIP_STATUS_3_VCSUNIT3
Address:	1D82B8h-1D82BBh
Name:	SYNC_FLIP_STATUS_3
ShortName:	SYNC_FLIP_STATUS_3_VECSUNIT1
Address:	1E02B8h-1E02BBh
Name:	SYNC_FLIP_STATUS_3
ShortName:	SYNC_FLIP_STATUS_3_VCSUNIT4
Address:	1E42B8h-1E42BBh
Name:	SYNC_FLIP_STATUS_3
ShortName:	SYNC_FLIP_STATUS_3_VCSUNIT5
Address:	1E82B8h-1E82BBh
Name:	SYNC_FLIP_STATUS_3
ShortName:	SYNC_FLIP_STATUS_3_VECSUNIT2
Address:	1F02B8h-1F02BBh
Name:	SYNC_FLIP_STATUS_3
ShortName:	SYNC_FLIP_STATUS_3_VCSUNIT6
Address:	1F42B8h-1F42BBh
Name:	SYNC_FLIP_STATUS_3
ShortName:	SYNC_FLIP_STATUS_3_VCSUNIT7
Address:	1F82B8h-1F82BBh
Name:	SYNC_FLIP_STATUS_3
ShortName:	SYNC_FLIP_STATUS_3_VECSUNIT3

This register is the saved value of what wait for events are still valid. This register is part of context save and

SYNC_FLIP_STATUS_3 - Wait For Event and Display Flip Flags Register 3

restore for RC6 feature.

Programming Notes	Source
Programming Restriction: This register should NEVER be programmed by SW, this is for HW internal use only.	
VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be exercised for reads or writes.	VideoCS, VideoCS2, VideoEnhancementCS

DWord	Bit	Description
0	31:30	**Reserved** Format: MBZ
	29	**Display Plane 18 Asynchronous Performance Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 18 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	28	**Display Plane 18 Asynchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 18 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	27	**Display Plane 18 Asynchronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 18 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	26	**Display Plane 18 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 18 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	25	**Display Plane 18 Synchronous Flip Display Pending** Format: Enable

SYNC_FLIP_STATUS_3 - Wait For Event and Display Flip Flags Register 3

		This field enables a wait for the duration of a Display Plane 18 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	24	**Display Plane 17 Asynchronous Performance Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 17 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	23	**Display Plane 17 Asynchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 17 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	22	**Display Plane 17 Asynchronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 17 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	21	**Display Plane 17 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 17 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	20	**Display Plane 17 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 17 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	19	**Display Plane 16 Asynchronous Performance Flip Pending Wait Enable**

SYNC_FLIP_STATUS_3 - Wait For Event and Display Flip Flags Register 3

		Format: Enable This field enables a wait for the duration of a Display Plane 1616 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	18	**Display Plane 16 Asynchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	17	**Display Plane 16 Asynchronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 16 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	16	**Display Plane 16 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 16 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	15	**Display Plane 16 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 16 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	14	**Display Plane 15 Asynchronous Performance Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 15 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_3 - Wait For Event and Display Flip Flags Register 3

	13	**Display Plane 15 Asynchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 15 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	12	**Display Plane 15 Asynchronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 15 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	11	**Display Plane 15 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 15 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	10	**Display Plane 15 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 15 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	9	**Display Plane 14 Asynchronous Performance Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 4 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	8	**Display Plane 14 Asynchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 14 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_3 - Wait For Event and Display Flip Flags Register 3

	7	**Display Plane 14 Asynchronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 14 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	6	**Display Plane 14 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 14 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	5	**Display Plane 14 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 14 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	4	**Display Plane 13 Asynchronous Performance Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 13 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	3	**Display Plane 13 Asynchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 13 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	2	**Display Plane 13 Asynchronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 13 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front

SYNC_FLIP_STATUS_3 - Wait For Event and Display Flip Flags Register 3

		buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	1	**Display Plane 13 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 13 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	0	**Display Plane 13 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 13 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.

Wait For Event and Display Flip Flags Register 4

SYNC_FLIP_STATUS_4 - Wait For Event and Display Flip Flags Register 4	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	022C0h-022C3h
Name:	SYNC_FLIP_STATUS_4
ShortName:	SYNC_FLIP_STATUS_4_RCSUNIT
Address:	182C0h-182C3h
Name:	SYNC_FLIP_STATUS_4
ShortName:	SYNC_FLIP_STATUS_4_POCSUNIT
Address:	222C0h-222C3h
Name:	SYNC_FLIP_STATUS_4
ShortName:	SYNC_FLIP_STATUS_4_BCSUNIT
Address:	1C02C0h-1C02C3h
Name:	SYNC_FLIP_STATUS_4
ShortName:	SYNC_FLIP_STATUS_4_VCSUNIT0
Address:	1C42C0h-1C42C3h
Name:	SYNC_FLIP_STATUS_4
ShortName:	SYNC_FLIP_STATUS_4_VCSUNIT1
Address:	1C82C0h-1C82C3h
Name:	SYNC_FLIP_STATUS_4
ShortName:	SYNC_FLIP_STATUS_4_VECSUNIT0
Address:	1D02C0h-1D02C3h
Name:	SYNC_FLIP_STATUS_4
ShortName:	SYNC_FLIP_STATUS_4_VCSUNIT2

SYNC_FLIP_STATUS_4 - Wait For Event and Display Flip Flags Register 4

Address:	1D42C0h-1D42C3h
Name:	SYNC_FLIP_STATUS_4
ShortName:	SYNC_FLIP_STATUS_4_VCSUNIT3
Address:	1D82C0h-1D82C3h
Name:	SYNC_FLIP_STATUS_4
ShortName:	SYNC_FLIP_STATUS_4_VECSUNIT1
Address:	1E02C0h-1E02C3h
Name:	SYNC_FLIP_STATUS_4
ShortName:	SYNC_FLIP_STATUS_4_VCSUNIT4
Address:	1E42C0h-1E42C3h
Name:	SYNC_FLIP_STATUS_4
ShortName:	SYNC_FLIP_STATUS_4_VCSUNIT5
Address:	1E82C0h-1E82C3h
Name:	SYNC_FLIP_STATUS_4
ShortName:	SYNC_FLIP_STATUS_4_VECSUNIT2
Address:	1F02C0h-1F02C3h
Name:	SYNC_FLIP_STATUS_4
ShortName:	SYNC_FLIP_STATUS_4_VCSUNIT6
Address:	1F42C0h-1F42C3h
Name:	SYNC_FLIP_STATUS_4
ShortName:	SYNC_FLIP_STATUS_4_VCSUNIT7
Address:	1F82C0h-1F82C3h
Name:	SYNC_FLIP_STATUS_4
ShortName:	SYNC_FLIP_STATUS_4_VECSUNIT3

This register is the saved value of what wait for events are still valid. This register is part of context save and

SYNC_FLIP_STATUS_4 - Wait For Event and Display Flip Flags Register 4

restore for RC6 feature.

Programming Notes	Source
Programming Restriction: This register should NEVER be programmed by SW, this is for HW internal use only.	
VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be exercised for reads or writes.	VideoCS, VideoCS2, VideoEnhancementCS

DWord	Bit	Description
0	31:30	**Reserved** Format: MBZ
	29	**Display Plane 24 Asynchronous Performance Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 24 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	28	**Display Plane 24 Asynchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 24 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	27	**Display Plane 24 Asynchronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 24 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	26	**Display Plane 24 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 24 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	25	**Display Plane 24 Synchronous Flip Display Pending** Format: Enable

SYNC_FLIP_STATUS_4 - Wait For Event and Display Flip Flags Register 4

		This field enables a wait for the duration of a Display Plane 24 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	24	**Display Plane 23 Asynchronous Performance Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 23 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	23	**Display Plane 23 Asynchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 23 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	22	**Display Plane 23 Asynchronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 23 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	21	**Display Plane 23 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 23 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	20	**Display Plane 23 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 23 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	19	**Display Plane 22 Asynchronous Performance Flip Pending Wait Enable**

SYNC_FLIP_STATUS_4 - Wait For Event and Display Flip Flags Register 4

		Format: Enable This field enables a wait for the duration of a Display Plane 22 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	18	**Display Plane 22 Asynchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 22 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	17	**Display Plane 22 Asynchronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 22 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	16	**Display Plane 22 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 22 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	15	**Display Plane 22 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 22 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	14	**Display Plane 21 Asynchronous Performance Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 21 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_4 - Wait For Event and Display Flip Flags Register 4

	13	**Display Plane 21 Asynchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 21 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	12	**Display Plane 21 Asynchronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 21 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	11	**Display Plane 21 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 21 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	10	**Display Plane 21 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 21 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	9	**Display Plane 20 Asynchronous Performance Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 20 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	8	**Display Plane 20 Asynchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 20 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_4 - Wait For Event and Display Flip Flags Register 4

	7	**Display Plane 20 Asynchronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 20 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	6	**Display Plane 20 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 20 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	5	**Display Plane 20 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 20 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	4	**Display Plane 19 Asynchronous Performance Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 19 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	3	**Display Plane 19 Asynchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 19 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	2	**Display Plane 19 Asynchronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 19 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front

		buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	1	**Display Plane 19 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 19 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	0	**Display Plane 19 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 19 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.

Wait For Event and Display Flip Flags Register 5

SYNC_FLIP_STATUS_5 - Wait For Event and Display Flip Flags Register 5	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	022C4h-022C7h
Name:	SYNC_FLIP_STATUS_5
ShortName:	SYNC_FLIP_STATUS_5_RCSUNIT
Address:	182C4h-182C7h
Name:	SYNC_FLIP_STATUS_5
ShortName:	SYNC_FLIP_STATUS_5_POCSUNIT
Address:	222C4h-222C7h
Name:	SYNC_FLIP_STATUS_5
ShortName:	SYNC_FLIP_STATUS_5_BCSUNIT
Address:	1C02C4h-1C02C7h
Name:	SYNC_FLIP_STATUS_5
ShortName:	SYNC_FLIP_STATUS_5_VCSUNIT0
Address:	1C42C4h-1C42C7h
Name:	SYNC_FLIP_STATUS_5
ShortName:	SYNC_FLIP_STATUS_5_VCSUNIT1
Address:	1C82C4h-1C82C7h
Name:	SYNC_FLIP_STATUS_5
ShortName:	SYNC_FLIP_STATUS_5_VECSUNIT0
Address:	1D02C4h-1D02C7h
Name:	SYNC_FLIP_STATUS_5
ShortName:	SYNC_FLIP_STATUS_5_VCSUNIT2

SYNC_FLIP_STATUS_5 - Wait For Event and Display Flip Flags Register 5

Address:	1D42C4h-1D42C7h
Name:	SYNC_FLIP_STATUS_5
ShortName:	SYNC_FLIP_STATUS_5_VCSUNIT3
Address:	1D82C4h-1D82C7h
Name:	SYNC_FLIP_STATUS_5
ShortName:	SYNC_FLIP_STATUS_5_VECSUNIT1
Address:	1E02C4h-1E02C7h
Name:	SYNC_FLIP_STATUS_5
ShortName:	SYNC_FLIP_STATUS_5_VCSUNIT4
Address:	1E42C4h-1E42C7h
Name:	SYNC_FLIP_STATUS_5
ShortName:	SYNC_FLIP_STATUS_5_VCSUNIT5
Address:	1E82C4h-1E82C7h
Name:	SYNC_FLIP_STATUS_5
ShortName:	SYNC_FLIP_STATUS_5_VECSUNIT2
Address:	1F02C4h-1F02C7h
Name:	SYNC_FLIP_STATUS_5
ShortName:	SYNC_FLIP_STATUS_5_VCSUNIT6
Address:	1F42C4h-1F42C7h
Name:	SYNC_FLIP_STATUS_5
ShortName:	SYNC_FLIP_STATUS_5_VCSUNIT7
Address:	1F82C4h-1F82C7h
Name:	SYNC_FLIP_STATUS_5
ShortName:	SYNC_FLIP_STATUS_5_VECSUNIT3

This register is the saved value of what wait for events are still valid. This register is part of context save and

SYNC_FLIP_STATUS_5 - Wait For Event and Display Flip Flags Register 5

restore for RC6 feature.

Programming Notes	Source
Programming Restriction: This register should NEVER be programmed by SW, this is for HW internal use only.	
VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be exercised for reads or writes.	VideoCS, VideoCS2, VideoEnhancementCS

DWord	Bit	Description
0	31:30	**Reserved** Format: MBZ
	29	**Display Plane 30 Asynchronous Performance Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 30 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	28	**Display Plane 30 Asynchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 30 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	27	**Display Plane 30 Asynchronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 30 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	26	**Display Plane 30 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 30 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	25	**Display Plane 30 Synchronous Flip Display Pending** Format: Enable

SYNC_FLIP_STATUS_5 - Wait For Event and Display Flip Flags Register 5

		This field enables a wait for the duration of a Display Plane 30 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	24	**Display Plane 29 Asynchronous Performance Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 29 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	23	**Display Plane 29 Asynchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 29 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	22	**Display Plane 29 Asynchronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 29 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	21	**Display Plane 29 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 29 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	20	**Display Plane 29 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 29 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	19	**Display Plane 28 Asynchronous Performance Flip Pending Wait Enable**

SYNC_FLIP_STATUS_5 - Wait For Event and Display Flip Flags Register 5

		Format: Enable This field enables a wait for the duration of a Display Plane 28 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	18	**Display Plane 28 Asynchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 28 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	17	**Display Plane 28 Asynchronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 28 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	16	**Display Plane 28 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 28 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	15	**Display Plane 28 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 28 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	14	**Display Plane 27 Asynchronous Performance Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 27 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_5 - Wait For Event and Display Flip Flags Register 5

	13	**Display Plane 27 Asynchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 27 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	12	**Display Plane 27 Asynchronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 27 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	11	**Display Plane 27 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 27 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	10	**Display Plane 27 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 27 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	9	**Display Plane 26 Asynchronous Performance Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 26 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	8	**Display Plane 26 Asynchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 26 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_5 - Wait For Event and Display Flip Flags Register 5

	7	**Display Plane 26 Asynchronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 26 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	6	**Display Plane 26 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 26 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	5	**Display Plane 26 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 26 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	4	**Display Plane 25 Asynchronous Performance Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 25 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	3	**Display Plane 25 Asynchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 25 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	2	**Display Plane 25 Asynchronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 25 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front

SYNC_FLIP_STATUS_5 - Wait For Event and Display Flip Flags Register 5

		buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	1	**Display Plane 25 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 25 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	0	**Display Plane 25 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 25 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.

Wait For Event and Display Flip Flags Register 6

SYNC_FLIP_STATUS_6 - Wait For Event and Display Flip Flags Register 6	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	021F8h-021FBh
Name:	SYNC_FLIP_STATUS_6
ShortName:	SYNC_FLIP_STATUS_6_RCSUNIT
Address:	181F8h-181FBh
Name:	SYNC_FLIP_STATUS_6
ShortName:	SYNC_FLIP_STATUS_6_POCSUNIT
Address:	221F8h-221FBh
Name:	SYNC_FLIP_STATUS_6
ShortName:	SYNC_FLIP_STATUS_6_BCSUNIT
Address:	1C01F8h-1C01FBh
Name:	SYNC_FLIP_STATUS_6
ShortName:	SYNC_FLIP_STATUS_6_VCSUNIT0
Address:	1C41F8h-1C41FBh
Name:	SYNC_FLIP_STATUS_6
ShortName:	SYNC_FLIP_STATUS_6_VCSUNIT1
Address:	1C81F8h-1C81FBh
Name:	SYNC_FLIP_STATUS_6
ShortName:	SYNC_FLIP_STATUS_6_VECSUNIT0
Address:	1D01F8h-1D01FBh
Name:	SYNC_FLIP_STATUS_6
ShortName:	SYNC_FLIP_STATUS_6_VCSUNIT2

SYNC_FLIP_STATUS_6 - Wait For Event and Display Flip Flags Register 6

Address:	1D41F8h-1D41FBh
Name:	SYNC_FLIP_STATUS_6
ShortName:	SYNC_FLIP_STATUS_6_VCSUNIT3
Address:	1D81F8h-1D81FBh
Name:	SYNC_FLIP_STATUS_6
ShortName:	SYNC_FLIP_STATUS_6_VECSUNIT1
Address:	1E01F8h-1E01FBh
Name:	SYNC_FLIP_STATUS_6
ShortName:	SYNC_FLIP_STATUS_6_VCSUNIT4
Address:	1E41F8h-1E41FBh
Name:	SYNC_FLIP_STATUS_6
ShortName:	SYNC_FLIP_STATUS_6_VCSUNIT5
Address:	1E81F8h-1E81FBh
Name:	SYNC_FLIP_STATUS_6
ShortName:	SYNC_FLIP_STATUS_6_VECSUNIT2
Address:	1F01F8h-1F01FBh
Name:	SYNC_FLIP_STATUS_6
ShortName:	SYNC_FLIP_STATUS_6_VCSUNIT6
Address:	1F41F8h-1F41FBh
Name:	SYNC_FLIP_STATUS_6
ShortName:	SYNC_FLIP_STATUS_6_VCSUNIT7
Address:	1F81F8h-1F81FBh
Name:	SYNC_FLIP_STATUS_6
ShortName:	SYNC_FLIP_STATUS_6_VECSUNIT3

This register is the saved value of what wait for events are still valid. This register is part of context save and

SYNC_FLIP_STATUS_6 - Wait For Event and Display Flip Flags Register 6

restore for RC6 feature.

Programming Notes	Source
Programming Restriction: This register should NEVER be programmed by SW, this is for HW internal use only.	
VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be exercised for reads or writes.	VideoCS, VideoCS2, VideoEnhancementCS

DWord	Bit	Description
0	31:19	**Reserved** Format: MBZ
	18	**Display Pipe D Scan Line Event Pending** Format: Enable This field indicates scan line event operation is pending from Display Pipe D. This field gets set when MI_SCANLINE_INCL/EXCL command is parsed for Display Pipe D and gets reset on scan line event completion for Display Plane-C.
	17	**Display Pipe D Scan Line Wait Enable** Format: Enable This field enables a wait while a Display Pipe D Scan Line condition exists. This condition is defined as the the start of the scan line specified in the Pipe D Display Scan Line Count Range Compare Register. See Scan Line Event in the Device Programming Interface chapter of MI Functions.
	16	**Display Pipe D Vertical Blank Wait Enable** Format: Enable This field enables a wait until the next Display Pipe D Vertical Blank event occurs. This event is defined as the start of the next Display Pipe D vertical blank period. Note that this can cause a wait for up to an entire refresh period. See Vertical Blank Event (See Programming Interface).
	15:10	**Reserved** Format: MBZ
	9	**Display Plane 32 Asynchronous Performance Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 32 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	8	**Display Plane 32 Asynchronous Flip Pending Wait Enable**

SYNC_FLIP_STATUS_6 - Wait For Event and Display Flip Flags Register 6

		Format: Enable This field enables a wait for the duration of a Display Plane 32 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	7	**Display Plane 32 Asynchronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 32 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	6	**Display Plane 32 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 32 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	5	**Display Plane 32 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 32 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	4	**Display Plane 31 Asynchronous Performance Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 31 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	3	**Display Plane 31 Asynchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 31 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_6 - Wait For Event and Display Flip Flags Register 6

	2	**Display Plane 31 Asynchronous Display Flip Pending** Format: Enable This field enables a wait for the duration of a Display Plane 31 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	1	**Display Plane 31 Synchronous Flip Pending Wait Enable** Format: Enable This field enables a wait for the duration of a Display Plane 31 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	0	**Display Plane 31 Synchronous Flip Display Pending** Format: Enable This field enables a wait for the duration of a Display Plane 31 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.

Watchdog Counter

PR_CTR - Watchdog Counter	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	02190h-02193h
Name:	Watchdog Counter
ShortName:	PR_CTR_RCSUNIT
Address:	18190h-18193h
Name:	Watchdog Counter
ShortName:	PR_CTR_POCSUNIT
Address:	22190h-22193h
Name:	Watchdog Counter
ShortName:	PR_CTR_BCSUNIT
Address:	1C0190h-1C0193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VCSUNIT0
Address:	1C4190h-1C4193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VCSUNIT1
Address:	1C8190h-1C8193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VECSUNIT0
Address:	1D0190h-1D0193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VCSUNIT2
Address:	1D4190h-1D4193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VCSUNIT3
Address:	1D8190h-1D8193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VECSUNIT1

PR_CTR - Watchdog Counter

Address:	1E0190h-1E0193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VCSUNIT4

Address:	1E4190h-1E4193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VCSUNIT5

Address:	1E8190h-1E8193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VECSUNIT2

Address:	1F0190h-1F0193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VCSUNIT6

Address:	1F4190h-1F4193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VCSUNIT7

Address:	1F8190h-1F8193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VECSUNIT3

DWord	Bit	Description
0	31:0	**Counter Value** Format: U32 This register reflects the render watchdog counter value itself. It cannot be written to.

Watchdog Counter Control

PR_CTR_CTL - Watchdog Counter Control	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	02178h-0217Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_RCSUNIT
Address:	18178h-1817Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_POCSUNIT
Address:	22178h-2217Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_BCSUNIT
Address:	1C0178h-1C017Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_VCSUNIT0
Address:	1C4178h-1C417Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_VCSUNIT1
Address:	1C8178h-1C817Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_VECSUNIT0
Address:	1D0178h-1D017Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_VCSUNIT2
Address:	1D4178h-1D417Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_VCSUNIT3
Address:	1D8178h-1D817Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_VECSUNIT1

PR_CTR_CTL - Watchdog Counter Control

Address:	1E0178h-1E017Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_VCSUNIT4

Address:	1E4178h-1E417Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_VCSUNIT5

Address:	1E8178h-1E817Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_VECSUNIT2

Address:	1F0178h-1F017Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_VCSUNIT6

Address:	1F4178h-1F417Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_VCSUNIT7

Address:	1F8178h-1F817Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_VECSUNIT3

Programming Notes	Source
Ring Buffer Mode of scheduling SW must enable and disable watch dog counter inline to a command sequence of any given workload within the same command buffer dispatch. Watch Dog counter once enabled doesn't stop unless it is explicitly disabled. SW must explicitly reset the watch dog counter by disabling it before enabling the watch dog counter for a new command sequence. Preemption could happen in a command sequence prior to watch dog counter getting disabled resulting in watch dog counter enabled following preemption. SW must explicitly take care of disabling the watch dog counter as part of the preemption sequence. Execution List Mode of Scheduling: SW must enable and disable watch dog counter inline to a command sequence of any given workload within the same command buffer dispatch. On a context switch "Watch Dog Counter Control" and "Watch dog Threshold" are context save restored, whereas watch dog counter gets reset to 0x0 and remains disabled until it gets enabled by another context during context restore or due to explicit programming. Watch dog counter value doesn't get accumulated across multiple submissions of a given context.	
This register functionality is not supported and must not be programmed for Position command streamer.	PositionCS

DWord	Bit	Description
0	31	**Count Select** Format: U1

PR_CTR_CTL - Watchdog Counter Control

Value	Name	Description
0h	**[Default]**	Use eight times the time stamp base unit to increment the watch dog count. The granularity of the time stamp base unit is defined in the “Time Stamp Bases” subsection in Power Management chapter.
1h		Use the fixed function clock (csclk) to increment the watchdog count

30:0 **Counter Logic Op**

Default Value:	1h

This field specifies the action to be taken by the clock counter to generate interrupts. Writing a Zero value to this register starts the counting. Writing a Value of 0000_0001 to this counter stops the counter.

Watchdog Counter Threshold

PR_CTR_THRSH - Watchdog Counter Threshold	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	0217Ch-0217Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_RCSUNIT
Address:	1817Ch-1817Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_POCSUNIT
Address:	2217Ch-2217Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_BCSUNIT
Address:	1C017Ch-1C017Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VCSUNIT0
Address:	1C417Ch-1C417Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VCSUNIT1
Address:	1C817Ch-1C817Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VECSUNIT0
Address:	1D017Ch-1D017Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VCSUNIT2
Address:	1D417Ch-1D417Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VCSUNIT3
Address:	1D817Ch-1D817Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VECSUNIT1

PR_CTR_THRSH - Watchdog Counter Threshold

Address:	1E017Ch-1E017Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VCSUNIT4

Address:	1E417Ch-1E417Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VCSUNIT5

Address:	1E817Ch-1E817Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VECSUNIT2

Address:	1F017Ch-1F017Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VCSUNIT6

Address:	1F417Ch-1F417Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VCSUNIT7

Address:	1F817Ch-1F817Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VECSUNIT3

Programming Notes	Source
This register functionality is not supported and must not be programmed for Position command streamer.	PositionCS
This register must never be programmed with zero. This will cause the watchdog counter to exceed and not allow the engine to go into IDLE state.	

DWord	Bit	Description
0	31:0	**Counter Logic Threshold** Default Value: 00145855h Format: U32 This field specifies the threshold that the hardware checks against for the value of the render clock counter before generating an interrupt. The counter in hardware generates an interrupt when the threshold is reached, rolls over and starts counting again. The interrupt generated is the "Media Hang Notify" interrupt since this watchdog timer is intended primarily to remedy VLD hangs on the main pipeline.

WD_27_M

WD_27_M

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6E524h-6E527h
Name:	WD0 27 MHz M
ShortName:	WD_27_M_0
Power:	PG2
Reset:	soft
Address:	6ED24h-6ED27h
Name:	WD1 27 MHz M
ShortName:	WD_27_M_1
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31	**Counter Force** This field forces the 27 MHz counter to enabled even if the WD function is disabled. This may be necessary when WD audio is used while WD video is disabled. Value / Name: 1b – Force Enabled 0b – Do Not Force
	30:24	**Reserved** Format: MBZ
	23:0	**WD Link M** Description: This field specifies the M value for the 27 MHz clock. Link M / Link N = 27 MHz / CD clock frequency See the Sequences for Changing CD Clock Frequency for the values to use. Value / Name / Description: 000002h – 2 **[Default]** – M=2

WD_27_N

WD_27_N		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Access:	R/W	
Size (in bits):	32	
Address:	6E528h-6E52Bh	
Name:	WD0 27 MHz N	
ShortName:	WD_27_N_0	
Power:	PG2	
Reset:	soft	
Address:	6EC28h-6EC2Bh	
Name:	WD1 27 MHz N	
ShortName:	WD_27_N_1	
Power:	PG2	
Reset:	soft	

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:0	**WD Link N** Description: This field specifies the N value for the 27 MHz clock. Link M / Link N = 27 MHz / CD clock frequency See the Sequences for Changing CD Clock Frequency for the values to use.

Value	Name	Description
000019h	25 **[Default]**	N=25

WD_FRAME_STATUS

WD_FRAME_STATUS

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	6E568h-6E56Bh
Name:	WD0 Frame Status
ShortName:	WD_FRAME_STATUS_0
Power:	PG2
Reset:	soft
Address:	6ED68h-6ED6Bh
Name:	WD1 Frame Status
ShortName:	WD_FRAME_STATUS_1
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31	**Frame Complete** Access: R/WC This field is a sticky bit set when WD fully completes a frame. Clear by writing a 1 to it.
	30:27	**Reserved** Format: MBZ
	26:24	**WD State** Access: RO This field indicates the live state of WD capture. Value / Name / Description: 000b / IDLE / Reset state 001b / CAPSTART / Start timing generator for normal capture 010b / FRAME_START / Send framestart to display pipe 011b / CAPACTIVE / Capturing data 100b / TG_DONE / Completed writing pixels. Waiting for frame completion. 101b / WDX_DONE / Fully completed frame. Waiting to start next frame. 110b / QUICK_CAP / Quick capture entry
	23	**Reserved**

WD_FRAME_STATUS		
	22:21	**Reserved**
	20	**Reserved**
	19:0	**Reserved**

WD_IIR

WD_IIR	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/WC
Size (in bits):	32
Address:	6E564h-6E567h
Name:	WD0 Interrupt Identity
ShortName:	WD_IIR_0
Power:	PG2
Reset:	soft
Address:	6ED64h-6ED67h
Name:	WD1 Interrupt Identity
ShortName:	WD_IIR_1
Power:	PG2
Reset:	soft

See the WD interrupt bit definition to find the source event for each interrupt bit.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**Interrupt Identity Bits** This field holds the persistent values of the WD interrupt bits which are unmasked by the WD_IMR. Bits set in this register will propagate to the WD interrupt in the Display Engine Miscellaneous Interrupts. Bits set in this register will remain set (persist) until the interrupt condition is cleared by writing a '1' to the appropriate bits. 0b – Condition Not Detected 1b – Condition Detected

WD_IMR

WD_IMR	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	6E560h-6E563h
Name:	WD0 Interrupt Mask
ShortName:	WD_IMR_0
Power:	PG2
Reset:	soft
Address:	6ED60h-6ED63h
Name:	WD1 Interrupt Mask
ShortName:	WD_IMR_1
Power:	PG2
Reset:	soft

See the WD interrupt bit definition to find the source event for each interrupt bit.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**Interrupt Mask Bits** This field contains a bit mask which selects which WD events are reported in the WD_IIR. 0b – Not Masked 1b – Masked 0000FFFFh – All interrupts masked **[Default]**

WD_PERF_CNT

WD_PERF_CNT		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Access:	Write/Read Status	
Size (in bits):	32	
Address:	6E55Ch-6E55Fh	
Name:	WD0 Performance Counter	
ShortName:	WD_PERF_CNT_0	
Power:	PG2	
Reset:	soft	
Address:	6ED5Ch-6ED5Fh	
Name:	WD1 Performance Counter	
ShortName:	WD_PERF_CNT_1	
Power:	PG2	
Reset:	soft	

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:0	**WD Perf Cnt** This field increments every millisecond while capturing. It does not count the time after capture is completed and waiting for the next capsync. Writes to this register will set the count to the written value, then it will increment from that value onwards.

WD_STATUS

WD_STATUS	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	RO
Size (in bits):	32
Address:	6E558h-6E55Bh
Name:	WD0 Status
ShortName:	WD_STATUS_0
Power:	PG2
Reset:	soft
Address:	6ED58h-6ED5Bh
Name:	WD1 Status
ShortName:	WD_STATUS_1
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31:16	**WD Capsync Count** Access: RO The value in this register represents the live status of the capsync counter.
	15:8	**WD Laterun Frame Count** Access: RO The value in this register represents the number of frames WD has dropped due to late run. The count will increment at each capture sync when late run is detected. After reaching the maximum count value the counter will rollover and continue from 0.
	7:0	**Quickcap Frame Counter** Access: RO This field provides the live status of the quick capture frame counter.

WD_STRIDE

WD_STRIDE	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of capture sync or transcoder not enabled
Address:	6E510h-6E513h
Name:	WD0 Stride
ShortName:	WD_STRIDE_0
Power:	PG2
Reset:	soft
Address:	6ED10h-6ED13h
Name:	WD1 Stride
ShortName:	WD_STRIDE_1
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:6	**WD Stride** This field specifies the stride bits 15:6. This value is used to determine the line to line increment for the capture data writes. This field is programmed in units of 64 bytes. **Programming Notes** The stride has to be at least large enough to encompass all the pixels in a line, and rounded up to 64 byte alignment. Stride bytes >= CEILING[(Horizontal Active * WD Color Mode bytes per pixel) / 64] * 64 **Restriction** The stride is limited to a maximum of 32K bytes.
	5:0	**Reserved** Format: MBZ

WD_SURF

WD_SURF	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of capture sync or transcoder not enabled
Address:	6E514h-6E517h
Name:	WD0 Surface Base Address
ShortName:	WD_SURF_0
Power:	PG2
Reset:	soft
Address:	6ED14h-6ED17h
Name:	WD1 Surface Base Address
ShortName:	WD_SURF_1
Power:	PG2
Reset:	soft

Writes to this register arm WD registers.

DWord	Bit	Description
0	31:12	**WD Surface Base Address** Format: GraphicsAddress[31:12] This address specifies the surface base address bits 31:12. It is mapped to physical pages through the global GTT. **Programming Notes** The mapped pages must be located outside graphics data stolen memory. **Restriction** It must be at least 4KB aligned. It must use linear memory.
	11:0	**Reserved** Format: MBZ

WD_TAIL_CFG

WD_TAIL_CFG

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of capture sync or transcoder not enabled; after armed
Double Buffer Armed By:	Write to WD_SURF or WD not enabled

Address:	6E520h-6E523h
Name:	WD0 Tail Pointer Config
ShortName:	WD_TAIL_CFG_0
Power:	PG2
Reset:	soft

Address:	6ED20h-6ED23h
Name:	WD1 Tail Pointer Config
ShortName:	WD_TAIL_CFG_1
Power:	PG2
Reset:	soft

DWord	Bit	Description
0 If Delay < Period; first tail pointer is sent at the next multiple of Period, after the Delay. If Delay ≤ Period; first tail pointer is set at the Period. The tail pointer is also sent at the end of the frame. If Delay or Period are greater than the vertical size, only the tail pointer at the end of the frame is sent.	31:28	**Reserved** Format: MBZ
	27:16	**Tail Initial Update Delay** This field specifies the minimum number of scan lines that WD capture must wait for at the beginning of each frame before any tail pointer updates will be sent to media. This must be programmed smaller than the vertical active size.
	15:12	**Reserved** Format: MBZ
	11:4	**Tail Update Period** Default Value: 01h 16 lines This field specifies the number of scan lines that the WD

WD_TAIL_CFG		
		capture will write back to memory before sending each tail pointer message to media. This field is programmed in multiples of 16 scan lines. **Restriction** A value of 0 is not valid.
	3:0	**Reserved** Format: MBZ

WIDI MOCS LECC 00 TC 00 Register

WIDI_MOCS_LECC_00_TC_00 - WIDI MOCS LECC 00 TC 00 Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CE00h
Name:	WIDI MOCS 0
ShortName:	WIDI_MOCS_0
Address:	0CE40h
Name:	WIDI MOCS 16
ShortName:	WIDI_MOCS_16
Address:	0CE80h
Name:	WIDI MOCS 32
ShortName:	WIDI_MOCS_32
Address:	0CEC0h
Name:	WIDI MOCS 48
ShortName:	WIDI_MOCS_48

WIDI MOCS register

DWord	Bit	Description
0	31:19	**Reserved** Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service** Default Value: 00b

	Access:	R/W

This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3

14 **Reserved**

13:11 **Page Faulting Mode**

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8 **Skip Caching control**

Default Value:	000b
Access:	R/W

Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface.
If "0" - than corresponding address bit value is do not care
Bit[8]=1: address bit[9] needs to be "0" to cache in target
Bit[9]=1: address bit[10] needs to be "0" to cache in target
Bit[10]=1: address bit[11] needs to be "0" to cache in target

7 **Enable Reverse Skip Caching**

Default Value:	0b
Access:	R/W

Enable for the Skip cache mechanism
0: Not enabled
1: Enabled for LLC

6 **Dont allocate on miss**

Default Value:	0b
Access:	R/W

Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM).
0: Allocate on MISS (normal cache behavior)

WIDI_MOCS_LECC_00_TC_00 - WIDI MOCS LECC 00 TC 00 Register

		1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

WIDI MOCS LECC 00 TC 01 Register

WIDI_MOCS_LECC_00_TC_01 - WIDI MOCS LECC 00 TC 01 Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CE04h
Name:	WIDI MOCS 1
ShortName:	WIDI_MOCS_1
Address:	0CE44h
Name:	WIDI MOCS 17
ShortName:	WIDI_MOCS_17
Address:	0CE84h
Name:	WIDI MOCS 33
ShortName:	WIDI_MOCS_33
Address:	0CEC4h
Name:	WIDI MOCS 49
ShortName:	WIDI_MOCS_49

WIDI MOCS register

DWord	Bit	Description
0	31:19	**Reserved** Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service** Default Value: 00b

WIDI_MOCS_LECC_00_TC_01 - WIDI MOCS LECC 00 TC 01 Register

	Access:	R/W

This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3

14	**Reserved**
13:11	**Page Faulting Mode**

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8	**Skip Caching control**

Default Value:	000b
Access:	R/W

Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface.
If "0" - than corresponding address bit value is do not care
Bit[8]=1: address bit[9] needs to be "0" to cache in target
Bit[9]=1: address bit[10] needs to be "0" to cache in target
Bit[10]=1: address bit[11] needs to be "0" to cache in target

7	**Enable Reverse Skip Caching**

Default Value:	0b
Access:	R/W

Enable for the Skip cache mechanism
0: Not enabled
1: Enabled for LLC

6	**Dont allocate on miss**

Default Value:	0b
Access:	R/W

Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM).
0: Allocate on MISS (normal cache behavior)

WIDI_MOCS_LECC_00_TC_01 - WIDI MOCS LECC 00 TC 01 Register

		1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

WIDI MOCS LECC 00 TC 10 Register

WIDI_MOCS_LECC_00_TC_10 - WIDI MOCS LECC 00 TC 10 Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CE08h
Name:	WIDI MOCS 2
ShortName:	WIDI_MOCS_2
Address:	0CE48h
Name:	WIDI MOCS 18
ShortName:	WIDI_MOCS_18
Address:	0CE88h
Name:	WIDI MOCS 34
ShortName:	WIDI_MOCS_34
Address:	0CEC8h
Name:	WIDI MOCS 50
ShortName:	WIDI_MOCS_50

WIDI MOCS register

DWord	Bit	Description
0	31:19	**Reserved** Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service** Default Value: 00b

WIDI_MOCS_LECC_00_TC_10 - WIDI MOCS LECC 00 TC 10 Register

	Access:	R/W

This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3

14	**Reserved**
13:11	**Page Faulting Mode**

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8	**Skip Caching control**

Default Value:	000b
Access:	R/W

Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface.
If "0" - than corresponding address bit value is do not care
Bit[8]=1: address bit[9] needs to be "0" to cache in target
Bit[9]=1: address bit[10] needs to be "0" to cache in target
Bit[10]=1: address bit[11] needs to be "0" to cache in target

7	**Enable Reverse Skip Caching**

Default Value:	0b
Access:	R/W

Enable for the Skip cache mechanism
0: Not enabled
1: Enabled for LLC

6	**Dont allocate on miss**

Default Value:	0b
Access:	R/W

Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM).
0: Allocate on MISS (normal cache behavior)

		1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 00b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

WIDI MOCS LECC 01 TC 00 Register

WIDI_MOCS_LECC_01_TC_00 - WIDI MOCS LECC 01 TC 00 Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CE0Ch
Name:	WIDI MOCS 3
ShortName:	WIDI_MOCS_3
Address:	0CE4Ch
Name:	WIDI MOCS 19
ShortName:	WIDI_MOCS_19
Address:	0CE8Ch
Name:	WIDI MOCS 35
ShortName:	WIDI_MOCS_35
Address:	0CECCh
Name:	WIDI MOCS 51
ShortName:	WIDI_MOCS_51

WIDI MOCS register

DWord	Bit	Description
0	31:19	**Reserved** Default Value: 0000000000000b Access: RO
	18:17	**Self Snoop Enable** Default Value: 00b Access: R/W 00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic 01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface 11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface
	16:15	**Class of Service** Default Value: 00b

WIDI_MOCS_LECC_01_TC_00 - WIDI MOCS LECC 01 TC 00 Register

	Access:	R/W

This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3

14	**Reserved**
13:11	**Page Faulting Mode**

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8	**Skip Caching control**

Default Value:	000b
Access:	R/W

Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface.
If "0" - than corresponding address bit value is do not care
Bit[8]=1: address bit[9] needs to be "0" to cache in target
Bit[9]=1: address bit[10] needs to be "0" to cache in target
Bit[10]=1: address bit[11] needs to be "0" to cache in target

7	**Enable Reverse Skip Caching**

Default Value:	0b
Access:	R/W

Enable for the Skip cache mechanism
0: Not enabled
1: Enabled for LLC

6	**Dont allocate on miss**

Default Value:	0b
Access:	R/W

Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM).
0: Allocate on MISS (normal cache behavior)

WIDI_MOCS_LECC_01_TC_00 - WIDI MOCS LECC 01 TC 00 Register

		1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control** Default Value: 01b Access: R/W Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

WIDI MOCS LECC 10 TC 00 Register

WIDI_MOCS_LECC_10_TC_00 - WIDI MOCS LECC 10 TC 00 Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CE10h
Name:	WIDI MOCS 4
ShortName:	WIDI_MOCS_4
Address:	0CE28h
Name:	WIDI MOCS 10
ShortName:	WIDI_MOCS_10
Address:	0CE50h
Name:	WIDI MOCS 20
ShortName:	WIDI_MOCS_20
Address:	0CE68h
Name:	WIDI MOCS 26
ShortName:	WIDI_MOCS_26
Address:	0CE90h
Name:	WIDI MOCS 36
ShortName:	WIDI_MOCS_36
Address:	0CEA8h
Name:	WIDI MOCS 42
ShortName:	WIDI_MOCS_42
Address:	0CED0h
Name:	WIDI MOCS 52
ShortName:	WIDI_MOCS_52
Address:	0CEE8h
Name:	WIDI MOCS 58
ShortName:	WIDI_MOCS_58

WIDI MOCS register

DWord	Bit	Description	
0	31:19	**Reserved**	
		Default Value:	0000000000000b

WIDI_MOCS_LECC_10_TC_00 - WIDI MOCS LECC 10 TC 00 Register

	Access:	RO

18:17 Self Snoop Enable

Default Value:	00b
Access:	R/W

00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic
01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface
11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface

16:15 Class of Service

Default Value:	00b
Access:	R/W

This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in.The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3

14 Reserved

13:11 Page Faulting Mode

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8 Skip Caching control

Default Value:	000b
Access:	R/W

Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface.
If "0" - than corresponding address bit value is do not care
Bit[8]=1: address bit[9] needs to be "0" to cache in target
Bit[9]=1: address bit[10] needs to be "0" to cache in target
Bit[10]=1: address bit[11] needs to be "0" to cache in target

WIDI_MOCS_LECC_10_TC_00 - WIDI MOCS LECC 10 TC 00 Register

7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
1:0	**LLC/eDRAM cacheability control**

WIDI_MOCS_LECC_10_TC_00 - WIDI MOCS LECC 10 TC 00 Register

		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index	

WIDI MOCS LECC 10 TC 01 Register

WIDI_MOCS_LECC_10_TC_01 - WIDI MOCS LECC 10 TC 01 Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0F614h
Name:	WIDI MOCS 5
ShortName:	WIDI_MOCS_5
Address:	0F62Ch
Name:	WIDI MOCS 11
ShortName:	WIDI_MOCS_11
Address:	0F654h
Name:	WIDI MOCS 21
ShortName:	WIDI_MOCS_21
Address:	0F66Ch
Name:	WIDI MOCS 27
ShortName:	WIDI_MOCS_27
Address:	0F694h
Name:	WIDI MOCS 37
ShortName:	WIDI_MOCS_37
Address:	0F6ACh
Name:	WIDI MOCS 43
ShortName:	WIDI_MOCS_43
Address:	0F6D4h
Name:	WIDI MOCS 53
ShortName:	WIDI_MOCS_53
Address:	0F6ECh
Name:	WIDI MOCS 59
ShortName:	WIDI_MOCS_59

WIDI MOCS register

DWord	Bit	Description	
0	31:19	**Reserved**	
		Default Value:	0000000000000b

WIDI_MOCS_LECC_10_TC_01 - WIDI MOCS LECC 10 TC 01 Register

	Access:	RO

18:17 Self Snoop Enable

Default Value:	00b
Access:	R/W

00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic
01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface
11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface

16:15 Class of Service

Default Value:	00b
Access:	R/W

This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3

14 Reserved

13:11 Page Faulting Mode

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8 Skip Caching control

Default Value:	000b
Access:	R/W

Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface.
If "0" - than corresponding address bit value is do not care
Bit[8]=1: address bit[9] needs to be "0" to cache in target
Bit[9]=1: address bit[10] needs to be "0" to cache in target
Bit[10]=1: address bit[11] needs to be "0" to cache in target

WIDI_MOCS_LECC_10_TC_01 - WIDI MOCS LECC 10 TC 01 Register

7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
1:0	**LLC/eDRAM cacheability control**

WIDI_MOCS_LECC_10_TC_01 - WIDI MOCS LECC 10 TC 01 Register

		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index	

WIDI MOCS LECC 10 TC 10 Register

WIDI_MOCS_LECC_10_TC_10 - WIDI MOCS LECC 10 TC 10 Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CE18h
Name:	WIDI MOCS 6
ShortName:	WIDI_MOCS_6
Address:	0CE30h
Name:	WIDI MOCS 12
ShortName:	WIDI_MOCS_12
Address:	0CE58h
Name:	WIDI MOCS 22
ShortName:	WIDI_MOCS_22
Address:	0CE70h
Name:	WIDI MOCS 28
ShortName:	WIDI_MOCS_28
Address:	0CE98h
Name:	WIDI MOCS 38
ShortName:	WIDI_MOCS_38
Address:	0CEB0h
Name:	WIDI MOCS 44
ShortName:	WIDI_MOCS_44
Address:	0CED8h
Name:	WIDI MOCS 54
ShortName:	WIDI_MOCS_54
Address:	0CEF0h
Name:	WIDI MOCS 60
ShortName:	WIDI_MOCS_60

WIDI MOCS register

DWord	Bit	Description	
0	31:19	**Reserved**	
		Default Value:	0000000000000b

WIDI_MOCS_LECC_10_TC_10 - WIDI MOCS LECC 10 TC 10 Register

	Access:	RO

18:17 Self Snoop Enable

Default Value:	00b
Access:	R/W

00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic
01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface
11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface

16:15 Class of Service

Default Value:	00b
Access:	R/W

This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3

14 Reserved

13:11 Page Faulting Mode

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8 Skip Caching control

Default Value:	000b
Access:	R/W

Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface.
If "0" - than corresponding address bit value is do not care
Bit[8]=1: address bit[9] needs to be "0" to cache in target
Bit[9]=1: address bit[10] needs to be "0" to cache in target
Bit[10]=1: address bit[11] needs to be "0" to cache in target

WIDI_MOCS_LECC_10_TC_10 - WIDI MOCS LECC 10 TC 10 Register

	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control**

WIDI_MOCS_LECC_10_TC_10 - WIDI MOCS LECC 10 TC 10 Register

		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index	

WIDI MOCS LECC 11 TC 00 Register

WIDI_MOCS_LECC_11_TC_00 - WIDI MOCS LECC 11 TC 00 Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CE1Ch
Name:	WIDI MOCS 7
ShortName:	WIDI_MOCS_7
Address:	0CE34h
Name:	WIDI MOCS 13
ShortName:	WIDI_MOCS_13
Address:	0CE5Ch
Name:	WIDI MOCS 23
ShortName:	WIDI_MOCS_23
Address:	0CE74h
Name:	WIDI MOCS 29
ShortName:	WIDI_MOCS_29
Address:	0CE9Ch
Name:	WIDI MOCS 39
ShortName:	WIDI_MOCS_39
Address:	0CEB4h
Name:	WIDI MOCS 45
ShortName:	WIDI_MOCS_45
Address:	0CEDCh
Name:	WIDI MOCS 55
ShortName:	WIDI_MOCS_55
Address:	0CEF4h
Name:	WIDI MOCS 61
ShortName:	WIDI_MOCS_61

WIDI MOCS register

DWord	Bit	Description	
0	31:19	**Reserved**	
		Default Value:	0000000000000b

WIDI_MOCS_LECC_11_TC_00 - WIDI MOCS LECC 11 TC 00 Register

	Access:	RO

18:17 Self Snoop Enable

Default Value:	00b
Access:	R/W

00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic
01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface
11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface

16:15 Class of Service

Default Value:	00b
Access:	R/W

This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3

14 Reserved

13:11 Page Faulting Mode

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8 Skip Caching control

Default Value:	000b
Access:	R/W

Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface.
If "0" - than corresponding address bit value is do not care
Bit[8]=1: address bit[9] needs to be "0" to cache in target
Bit[9]=1: address bit[10] needs to be "0" to cache in target
Bit[10]=1: address bit[11] needs to be "0" to cache in target

WIDI_MOCS_LECC_11_TC_00 - WIDI MOCS LECC 11 TC 00 Register

7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
3:2	**Target Cache** Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
1:0	**LLC/eDRAM cacheability control**

WIDI_MOCS_LECC_11_TC_00 - WIDI MOCS LECC 11 TC 00 Register

Default Value:	11b
Access:	R/W

Memory type information used in LLC/eDRAM.
00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)
01: Uncacheable (UC) - non-cacheable
10: Writethrough (WT)
11: Writeback (WB)
Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used
Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

WIDI MOCS LECC 11 TC 01 Register

WIDI_MOCS_LECC_11_TC_01 - WIDI MOCS LECC 11 TC 01 Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CE20h
Name:	WIDI MOCS 8
ShortName:	WIDI_MOCS_8
Address:	0CE38h
Name:	WIDI MOCS 14
ShortName:	WIDI_MOCS_14
Address:	0CE60h
Name:	WIDI MOCS 24
ShortName:	WIDI_MOCS_24
Address:	0CE78h
Name:	WIDI MOCS 30
ShortName:	WIDI_MOCS_30
Address:	0CEA0h
Name:	WIDI MOCS 40
ShortName:	WIDI_MOCS_40
Address:	0CEB8h
Name:	WIDI MOCS 46
ShortName:	WIDI_MOCS_46
Address:	0CEE0h
Name:	WIDI MOCS 56
ShortName:	WIDI_MOCS_56
Address:	0CEF8h
Name:	WIDI MOCS 62
ShortName:	WIDI_MOCS_62

WIDI MOCS register

DWord	Bit	Description	
0	31:19	**Reserved**	
		Default Value:	0000000000000b

WIDI_MOCS_LECC_11_TC_01 - WIDI MOCS LECC 11 TC 01 Register

	Access:	RO

18:17 Self Snoop Enable

Default Value:	00b
Access:	R/W

00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic
01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface
11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface

16:15 Class of Service

Default Value:	00b
Access:	R/W

This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3

14 Reserved

13:11 Page Faulting Mode

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8 Skip Caching control

Default Value:	000b
Access:	R/W

Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface.
If "0" - than corresponding address bit value is do not care
Bit[8]=1: address bit[9] needs to be "0" to cache in target
Bit[9]=1: address bit[10] needs to be "0" to cache in target
Bit[10]=1: address bit[11] needs to be "0" to cache in target

WIDI_MOCS_LECC_11_TC_01 - WIDI MOCS LECC 11 TC 01 Register

	7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
	6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
	5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
	3:2	**Target Cache** Default Value: 01b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
	1:0	**LLC/eDRAM cacheability control**

WIDI_MOCS_LECC_11_TC_01 - WIDI MOCS LECC 11 TC 01 Register

		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB) Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index	

WIDI MOCS LECC 11 TC 10 Register

WIDI_MOCS_LECC_11_TC_10 - WIDI MOCS LECC 11 TC 10 Register

Register Space:	MMIO: 0/2/0
Source:	BSpec
Size (in bits):	32
Address:	0CE24h
Name:	WIDI MOCS 9
ShortName:	WIDI_MOCS_9
Address:	0CE3Ch
Name:	WIDI MOCS 15
ShortName:	WIDI_MOCS_15
Address:	0CE64h
Name:	WIDI MOCS 25
ShortName:	WIDI_MOCS_25
Address:	0CE7Ch
Name:	WIDI MOCS 31
ShortName:	WIDI_MOCS_31
Address:	0CEA4h
Name:	WIDI MOCS 41
ShortName:	WIDI_MOCS_41
Address:	0CEBCh
Name:	WIDI MOCS 47
ShortName:	WIDI_MOCS_47
Address:	0CEE4h
Name:	WIDI MOCS 57
ShortName:	WIDI_MOCS_57
Address:	0CEFCh
Name:	WIDI MOCS 63
ShortName:	WIDI_MOCS_63

WIDI MOCS register

DWord	Bit	Description	
0	31:19	**Reserved**	
		Default Value:	0000000000000b

WIDI_MOCS_LECC_11_TC_10 - WIDI MOCS LECC 11 TC 10 Register

	Access:	RO

18:17 Self Snoop Enable

Default Value:	00b
Access:	R/W

00: Default value. Self snoop attribute sent to the uncore is as today - determined by MIDI unit logic
01: Override the self snoop bit generated by MIDI with 0. No self snoops are sent to the uncore for any transactions from this surface
11: Override the self snoop bit generated by MIDI with 1. Self snoops are always sent to the uncore for any transactions from this surface

16:15 Class of Service

Default Value:	00b
Access:	R/W

This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec.
00: Value from Private PAT Registers(40E0/40E4/40E8/40EC)
01: Class 1
10: Class 2
11: Class 3

14 Reserved

13:11 Page Faulting Mode

Default Value:	000b
Access:	R/W

This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface:
000: Use the global page faulting mode from context descriptor (default)
001-111: Reserved

10:8 Skip Caching control

Default Value:	000b
Access:	R/W

Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface.
If "0" - than corresponding address bit value is do not care
Bit[8]=1: address bit[9] needs to be "0" to cache in target
Bit[9]=1: address bit[10] needs to be "0" to cache in target
Bit[10]=1: address bit[11] needs to be "0" to cache in target

WIDI_MOCS_LECC_11_TC_10 - WIDI MOCS LECC 11 TC 10 Register

7	**Enable Reverse Skip Caching** Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
6	**Dont allocate on miss** Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - do not bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS Received confirmation from Altug on 03/13/13 that nothing needs to be done on this bit
5:4	**LRU management** Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. When Target Cache(TC) == 00, LRU Age value will be from Private PAT registers(40E0/40E8/40EC) When Target Cache(TC) != 00, LRU Age value will be from MOCS as follows 11: Assign the age of "3" 10: do not change the age on a hit. 01: Assign the age of "0" 00: Take the age value from Uncore CRs
3:2	**Target Cache** Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: Value from Private PAT registers(40E0/40E4/40E8/40EC) 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed
1:0	**LLC/eDRAM cacheability control**

WIDI_MOCS_LECC_11_TC_10 - WIDI MOCS LECC 11 TC 10 Register

Default Value:	11b
Access:	R/W

Memory type information used in LLC/eDRAM.
00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)
01: Uncacheable (UC) - non-cacheable
10: Writethrough (WT)
11: Writeback (WB)
Note: Binding table index based memory typing cannot be used for LLC/eDRAM memory type. Instead page table based controls have to be used
Note: In case of SVM (advanced context), LLC/eDRAM memory type is used based on the page table controls and cannot be managed via MOCS index

Window Hardware Generated Clear Value

WMHWCLRVAL - Window Hardware Generated Clear Value	
Register Space:	MMIO: 0/2/0
Source:	RenderCS
Access:	RO
Size (in bits):	32
Address:	05524h

DWord	Bit	Description
0	31:0	**WM HW Generated Clear Value** Format: MBZ This register stores HW generated Z clear value.

WM_LINETIME

WM_LINETIME	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	45270h-45273h
Name:	Pipe Watermark Line Time
ShortName:	WM_LINETIME_A
Power:	PG1
Reset:	soft
Address:	45274h-45277h
Name:	Pipe Watermark Line Time
ShortName:	WM_LINETIME_B
Power:	PG2
Reset:	soft
Address:	45278h-4527Bh
Name:	Pipe Watermark Line Time
ShortName:	WM_LINETIME_C
Power:	PG2
Reset:	soft

DWord	Bit	Description
0	31:25	**Reserved**
	24:16	**Reserved**
	15:9	**Reserved**
	8:0	**Line Time** This field specifies the line time for the current screen resolution in units of 0.125us. **Programming Notes** Line time in microseconds = Pipe horizontal total number of pixels / pixel rate in MHz. Multiply by 8 to get units of 0.125us and round to nearest integer. Program the smallest line time when using multiple refresh rates. **Restriction** The line time value must be programmed before enabling any display low power watermark. Maximum supported line time is 63.875us (111111111b).

WM_MISC

WM_MISC

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Address:	45260h-45263h
Name:	Watermark Miscellaneous
ShortName:	WM_MISC
Power:	PG0
Reset:	soft

DWord	Bit	Description
0	31	**Reserved** Format: PBC
	30:28	**Reserved**
	27	**MIPI DBI Method** This field controls the behavior for the TTNF calculation for MIPI DBI. 0b – Calculated – TTNF calculated in active area and all 1s outside of active. TTVBI all 1s. 1b – Simple – TTNF all 0s in active area and all 1s outside of active. TTVBI all 1s.
	26:20	**Reserved** Format: PBC
	19:0	**Reserved**