Intel® OpenSource HD Graphics Programmer's Reference Manual (PRM)

Volume 1 Part 6: GT Interface Register (Ivy Bridge)

For the 2012 Intel® Core™ Processor Family

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1. GT Interface Registers

1.1 MBCunit Config Space

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
IDI Control Register	IDICR	9008h	900Bh	00000005h	RW
Snoop Control Register	SNPCR	900Ch	900Fh	00001B40h	RW, RO
IDI Cacheable Register	IDICA	9014h	9017h	00000000h	RW
IDI Self Snoop Register	IDISLFSNP	9018h	901Bh	00000000h	RW
Super Queue Internal Counters Register 1	SQCNT1	9024h	9027h	00000000h	RW, RO
Super Queue Internal Counters Register 2	SQCNT2	9028h	902Bh	00000F00h	RO, RW
Super Queue GFX Cycle Options Register	SQCFG	902Ch	902Fh	00000000h	RO, RW
Fence Control Register	MFCR	9070h	9073h	00000000h	RO, RW
MBC Control Register	MBCTL	907Ch	907Fh	00000000h	RW, RO
Mirror of TOLUD	TOLUD	9090h	9093h	00100000h	RO
Mirror of GMCH Graphics Control Register	MGGC	9094h	9097h	00000030h	RO
Mirror of TOUUD	TOUUD	9098h	909Fh	0000000000000000h	RO
Mirror of DSMBASE	DSMB	90A0h	90A3h	00000000h	RO
Mirror of GSMBASE	GSMB	90A4h	90A7h	00000000h	RO
Mirror of DPRBASE	DPRB	90A8h	90ABh	00000000h	RO
Mirror of Global Command Register	GCMD	90CCh	90CFh	00000000h	RO
Mirror of Graphics Translation Table and Memory Mapped Range Address	GTTMMADR	9124h	912Bh	0000000000000000h	RO
Mirror of PCICMD MAE/BME	PCICMD	912Ch	912Fh	00000000h	RW

Workaround: Accesses to the MMIO range from 0x9500-0x97ff can prevent GT from entering RC6 after the read or write. There are no registers in this range, thus no reason for software to read or write this range.

1.1.1 IDICR - IDI Control register

B/D/F/Type:	0/0/0/MBCunit_Config
Address Offset:	9008-900Bh
Default Value:	00000005h
Access:	RW
Size:	32 bits

Bits	Access	Default Value	RST/PWR	Description
31:15	RW	00000h	Core	**ECORSVD (ECORSVD):** ECO purposes and Reserved.
6:4	RW	000b	Core	**LRUHint (LRU):** 000b: No LRUHint command sent to uncore. It's reserved. 001b: If LRUHint is asserted from SQ with a read or write command, IDI dispatcher chooses to send an **LlcPrefData**. 101b: If LRUHint is asserted from SQ with a read or write command, IDI dispatcher chooses to send an **LLCPrefCode** command on the C2U request channel. 010b: If LRUHint is asserted from SQ with a read/write command, IDI dispatcher chooses to send an **LlcPrefRFO** command on the C2U request channel. 011b: If LRUHint is asserted from SQ with a read, IDI dispatcher chooses to send an **LlcPrefData** command on the C2U request channel. If LRUHint is asserted from SQ with a write, IDI dispatcher chooses to send **LlcPrefRFO** command on the C2U request channel. 111b: If LRUHint is asserted from SQ with a read, IDI dispatcher chooses to send an **LLCPrefCode** command on the C2U request channel. If LRUHint is asserted from SQ with a write, IDI dispatcher chooses to send **LlcPrefRFO** command on the C2U request channel.
3	RO	0b	Core	**Reserved**.
2	RW	0b	Core	**Rsp Port1 Disable:** 0 - Default value - Both the Response ports on the BGF side are enabled. 1 - Rsp Port1 Disable - Response Port1 is disable on the BGF Side
1:0	RW	01b	Core	**SQ Grant Counter (SQGNT):** SQ grant counter - 2-bit grant counter for SQ requests: 00b - 1 grant 01b - 2 grants 10b - 4 grants 11b - 8 grants

1.1.2 SNPCR - Snoop control register

B/D/F/Type: 0/0/0/MBCunit_Config
Address Offset: 900C-900Fh
Default Value: 00001B40h
Access: RW, RO
Size: 32 bits

Snoop control register

<table>
<tr><th>Bits</th><th>Access</th><th>Default Value</th><th>RST/PWR</th><th>Description</th></tr>
<tr><td>31:23</td><td>RO</td><td>000000000b</td><td>Core</td><td>Reserved (RSVD):
RSVD</td></tr>
<tr><td>22:21</td><td>RW</td><td>00b</td><td>Core</td><td>IDICOS (IDICOS):
00 => MAX uncore resources (default)
01 => Medium uncore resources
10 => LOW uncore resources
11 => MIN uncore resources
<table>
<tr><th colspan="5">SNPCR - Snoop control register, IDICOS values explanation</th></tr>
<tr><th>Bits</th><th>COS Value</th><th>Description (from BSpec)</th><th>GT</th><th>GT</th></tr>
<tr><td colspan="5">Mobile 8MB Total Cache Size CPUs (4+2, ie 3820QM)</td></tr>
<tr><td>22:21</td><td>00</td><td></td><td>6</td><td>3MB</td></tr>
<tr><td></td><td>01</td><td></td><td>16</td><td>8MB</td></tr>
<tr><td></td><td>10</td><td></td><td>12</td><td>6MB</td></tr>
<tr><td></td><td>11</td><td></td><td>1</td><td>512KB</td></tr>
<tr><td colspan="5">Mobile 6MB Cache Size CPUs (4+2, ie 3615QM)</td></tr>
<tr><td>22:21</td><td>00</td><td></td><td>5</td><td>2.5MB</td></tr>
<tr><td></td><td>01</td><td></td><td>12</td><td>6MB</td></tr>
<tr><td></td><td>10</td><td></td><td>9</td><td>4.5MB</td></tr>
<tr><td></td><td>11</td><td></td><td>1</td><td>512KB</td></tr>
<tr><td colspan="5">IVB Mobile 4MB Cache Size CPUs (2+?, like 3520M)</td></tr>
<tr><td>22:21</td><td>00</td><td></td><td>6</td><td>1.5MB</td></tr>
<tr><td></td><td>01</td><td></td><td>16</td><td>4MB</td></tr>
<tr><td></td><td>10</td><td></td><td>12</td><td>3MB</td></tr>
<tr><td></td><td>11</td><td></td><td>1</td><td>256KB</td></tr>
<tr><td colspan="5">Mobile 3MB Cache Size CPUs (2+?, like 3320M)</td></tr>
<tr><td>22:21</td><td>00</td><td></td><td>5</td><td>1.25MB</td></tr>
<tr><td></td><td>01</td><td></td><td>12</td><td>6MB</td></tr>
<tr><td></td><td>10</td><td></td><td>9</td><td>2.25MB</td></tr>
<tr><td></td><td>11</td><td></td><td>1</td><td>256KB</td></tr>
</table>
</td></tr>
<tr><td>20</td><td>RW</td><td>0b</td><td>Core</td><td>Non Temporal (NONTMP):
Indication to uncore that - Request is of the type that should get minimal cache resources in the uncore</td></tr>
<tr><td>19:16</td><td>RO</td><td>0000b</td><td>Core</td><td>RSVD (RSVD):
Reserved</td></tr>
<tr><td>15</td><td>RW</td><td>0b</td><td>Core</td><td>Thread ID (THDID):
1 bit Thread ID for GT</td></tr>
<tr><td>14</td><td>RW</td><td>0b</td><td>Core</td><td>Force Invalidate (FINV):
Force Invalidate - Forces the invalidate flag to be set with snoop lookups all the time.
0 - normal invalidation (based on req) - Default</td></tr>
</table>

Bits	Access	Default Value	RST/PWR	Description
				1 - Forced invalidation
13:11	RW	011b	Core	**IDI Pend Timer (IDITIMER):** IDIpend timer - Time to wait before monitoring the sq_snpc_idipend signal. 000=> 0 clocks 001 => 1 clock 010 => 2 clocks 011 => 4 clocks (default) 100 => 8 101 => 16 110 => 32 111 => 64
10:8	RW	011b	Core	**Retry Limi (RTRYLMT):** Retry Limit - Number of times to retry before switching to the freeze mechanism 000=> Always freeze (first shot) 001=> 1 retry 010 => 2 retry 011 => 4 retry (default) 100 => 8 retry 101 => 16 retry 110 => 32 retry 111 => infinite (no freeze)
7:3	RW	01000b	Core	**Retry Timer (RTRYTIMER):** Retry Timer - Time between receiving a reject from SQ and repeating the monitor sequence. 00000=> 0 clocks 00001 => 1 clock 00010 => 2 clocks 00011 => 3 clocks 00111 => 7 clocks 01000 => 8 clocks (Default) . . . 11111 => 32 clocks

Bits	Access	Default Value	RST/PWR	Description
2:0	RW	000b	Core	**MLCSQ Timer (MSTIMER):** MLC-SQ Timer - Time between doing an MLC lookup and SQ lookup 000=> 0 clocks (default) 001 => 1 clock 010 => 2 clocks 011 => 4 clocks 100 => 8 101 => 16 110 => 32 111 => 64

1.1.3 IDICA - IDI Cacheable Register

B/D/F/Type: 0/0/0/MBCunit_Config
Address Offset: 9014-9017h
Default Value: 00000000h
Access: RW
Size: 32 bits

Cacheable:

Bits	Access	Default Value	RST/PWR	Description
31:30	RW	00b	Core	**LLCWBCA (LLCWBCA):** NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO “00”.
29:28	RW	00b	Core	**LLCPRFOCA (LLCPRFOCA):** NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO “00”.
27:26	RW	00b	Core	**LLCPCCA (LLCPCCA):** NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO “00”.
25:24	RW	00b	Core	**LLCPDCA (LLCPDCA):** NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO “00”.
23:22	RW	00b	Core	**CLFCA (CLFCA):** NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO “00”.
21:20	RW	00b	Core	**POCA (POCA):** NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO “00”.
19:18	RW	00b	Core	**ITMCA (ITMCA):** NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO “00”.

Bits	Access	Default Value	RST/PWR	Description
17:16	RW	00b	Core	**WCILFCA (WCILFCA):** NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO “00”.
15:14	RW	00b	Core	**WILCA (WILCA):** NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO “00”. CANNOT BE FLEXED.
13:12	RW	00b	Core	**WCILCA (WCILCA):** NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO “00”. CANNOT BE FLEXED.
11:10	RW	00b	Core	**WBMCA (WBMCA):** NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO “00”.
9:8	RW	00b	Core	**RFOCA (RFOCA):** NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO “00”.
7:6	RW	00b	Core	**PORINCA (PORINCA):** NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO “00”.
5:4	RW	00b	Core	**PRDCA (PRDCA):** NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO “00”.
3:2	RW	00b	Core	**DRDCA (DRDCA):** 00b: What ever the logic decides (so force feature is disabled) - Default. 01b: Always drive “0”. 10b: Always drive “1”. 11b: Reserved.
1:0	RW	00b	Core	**CRDCA (CRDCA):** 00b: What ever the logic decides (so force feature is disabled) - Default. 01b: Always drive “0”. 10b: Always drive “1”. 11b: Reserved.

1.1.4 IDISLFSNP - IDI Self Snoop Register

B/D/F/Type: 0/0/0/MBCunit_Config
Address Offset:9018-901Bh
Default Value: 00000000h
Access: RW
Size: 32 bits

IDI Self Snoop Register:

Bits	Access	Default Value	RST/PWR	Description
31:30	RW	00b	Core	**LLCWBSNP (LLCWBSNP):** 00b: Whatever the logic decides (so force feature is disabled) - Default. 01b: Always drive “0”. 10b: Always drive “1”. 11b: Reserved.
29:28	RW	00b	Core	**LLCPRFOSNP (LLCPRFOSNP):** NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO “00”. CANNOT BE FLEXED.
27:26	RW	00b	Core	**LLCPCSNP (LLCPCSNP):** NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO “00”. CANNOT BE FLEXED.
25:24	RW	00b	Core	**LLCPDSNP (LLCPDSNP):** NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO “00”. CANNOT BE FLEXED.
23:22	RW	00b	Core	**CLFCA (CLFCA):** NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO “00”. CANNOT BE FLEXED.
21:20	RW	00b	Core	**POCA (POCA):** NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO “00”. CANNOT BE FLEXED.
19:18	RW	00b	Core	**ITMSNP (ITMSNP):** 00b: Whatever the logic decides (so force feature is disabled) - Default. 01b: Always drive “0”. 10b: Always drive “1”. 11b: Reserved.
17:16	RW	00b	Core	**WCILFSNP (WCILFSNP):** NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO “00”. CANNOT BE FLEXED.

Bits	Access	Default Value	RST/PWR	Description
15:14	RW	00b	Core	**WILSNP (WILSNP):** NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO “00”. CANNOT BE FLEXED.
13:12	RW	00b	Core	**WCILSNP (WCILSNP):** NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO “00”. CANNOT BE FLEXED.
11:10	RW	00b	Core	**WBMSNP (WBMSNP):** NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO “00”. CANNOT BE FLEXED.
9:8	RW	00b	Core	**RFOSNP (RFOSNP):** 00b: What ever the logic decides (so force feature is disabled) - Default. 01b: Always drive “0”. 10b: Always drive “1”. 11b: Reserved.
7:6	RW	00b	Core	**PORINSNP (PORINSNP):** NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO “00”. CANNOT BE FLEXED.
5:4	RW	00b	Core	**PRDSNP (PRDSNP):** NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO “00”. CANNOT BE FLEXED.
3:2	RW	00b	Core	**DRDSNP (DRDSNP):** 00b: Whatever the logic decides (so force feature is disabled) - Default. 01b: Always drive “0”. 10b: Always drive “1”. 11b: Reserved.
1:0	RW	00b	Core	**CRDSP (CRDSP):** 00b: Whatever the logic decides (so force feature is disabled) - Default. 01b: Always drive “0”. 10b: Always drive “1”. 11b: Reserved.

1.1.5 SQCNT1 - Super Queue Internal Cnt Register I

B/D/F/Type: 0/0/0/MBCunit_Config
Address Offset: 9024-9027h
Default Value: 00000000h
Access: RW, RO
Size: 32 bits

SQ Internal Counter Register

Bits	Access	Default Value	RST/PWR	Description
31:24	RO	00000000b	Core	**RSVD (RSVD):** RSVD
23:20	RW	0000b	Core	**SQRWCQD (SQRWCQD):** Read-Write Request Queue Command Get Delay: This indicates the number of clocks that are inserted between each GFX cycle being accepted on the GFX Read or GFX Write ports. By default, this is disabled, which means that the RWRQ is able to accept one cycle per clock. By any other value, the RWRQ will insert the number of idle clocks listed in this register before accepting another cycle from GFX, essentially throttling the bandwidth. During each idle clock, RWRQ is guaranteed not to assert its command get to either read or write port. 0000 = disabled (no additional clocks added) 0001 = one idle clock inserted between command gets 0010 = two idle clocks inserted between command gets ... 1111 = fifteen idle clocks inserted between command gets
19:16	RW	0000b	Core	**SQCQD (SQCQD):** Read-Only Request Queue Command Get Delay: This indicates the number of clocks that are inserted between each GFX cycle being accepted on the GFX Read-Only port. By default, this is disabled, which means that the RORQ is able to accept one cycle per clock. By any other value, the RORQ will insert the number of idle clocks listed in this register before accepting another cycle from GFX, essentially throttling the bandwidth. During each idle clock, RORQ is guaranteed not to assert its command get. 0000 = disabled (no additional clocks added) 0001 = one idle clock inserted between command gets 0010 = two idle clocks inserted between command gets ... 1111 = fifteen idle clocks inserted between command gets

Bits	Access	Default Value	RST/PWR	Description
15:13	RW	000b	Core	**SQDPTH (SQDPTH):** Super Queue Depth: This indicates the maximum number of cycles that are supported at any given time by Super Queue. By default, this is 48, which is the maximum size of the Super Queue, but can be throttled back to support fewer GFX cycles. Note: By limiting the depth of the super queue, effectively the recycle queue limits the SQIDs that are allowed to be used. 000 = disabled (48 deep) 001 = Rsvd. 010 = 2 deep 011 = 4 deep 100 = 8 deep 101 = 16 deep 110 = 24 deep 111 = 32 deep
12:9	RW	0000b	Core	**SQMQCNT (SQMQCNT):** Outstanding MQ IDI Cycle Counter: Note: This register Bits (SQMQCNT) should not be programmed. The default value "0" (16 entries) is the POR. This indicates the maximum number of outstanding cycles that are presented to IDI/uncore at any given time by Maintenance Queue. By default, this is 16, but can be throttled back to support fewer IDI cycles. 0 = disabled (16) 1-15 = max number of outstanding IDI cycles
8:6	RW	000b	Core	**SQVTDCNT (SQVTDCNT):** Outstanding VTD read Counter: This indicates the maximum number of outstanding VTD read cycles that are presented to IDI/uncore at any given time by Super Queue. By default, this is 4, but can be throttled back to support fewer VTD read cycles. 000 = 1 max outstanding VTD read cycle 001 = 2 max outstanding VTD read cycles 010 = 3 max outstanding VTD read cycles 011 = 4 max outstanding VTD read cycles (Default value) 100 = 5 max outstanding VTD read cycles 101 = 6 max outstanding VTD read cycles

Bits	Access	Default Value	RST/PWR	Description
				110 = 7 max outstanding VTD read cycles 111 = 8 max outstanding VTD read cycles
5:0	RW	000000b	Core	**SQIDICNT (SQIDICNT):** Outstanding SQ IDI Cycle Counter: This indicates the maximum number of outstanding cycles that are presented to IDI/uncore at any given time by Super Queue. By default, this is 48, but can be throttled back to support fewer IDI cycles. 0 = disabled (48) 1-47 = max number of outstanding IDI cycles 48+ = reserved

1.1.6 SQCNT2 - Super Queue Internal Counters Register II

B/D/F/Type: 0/0/0/MBCunit_Config
Address Offset: 9028-902Bh
Default Value: 00000F00h
Access: RO, RW
Size: 32 bits

Super Queue Internal Counter register

Bits	Access	Default Value	RST/PWR	Description
31:30	RO	00b	Core	**Reserved (RSVD):** Reserved
29	RW	0b	Core	**Enable Promotion on Read (ENPROM):** **Enable Promotion on Read Match:** Enable the promotion of write request if matched with a Read request.
28	RW	0b	Core	**Priority 3 Pool Count Disable (PRIO3PCDIS):** **Priority3 Pool Count Disable:** When set, priority3 pool becomes unlimited. And priority3 pool count value should not be used in reset of the remaining counters.
27:25	RW	000b	Core	**Priority3 Pool Count: (PRIO3PC):** Priority3 Pool Count: The count of cycles is selected from priority3 pool before switching to lower priority pools. Count is used as the power of 2. 000: 1 request 001: 2 requests 010: 4 requests 011: 8 requests

Bits	Access	Default Value	RST/PWR	Description
				….. 111: 128 requests
24	RW	0b	Core	**Priority2 Pool Count Disable (PRIO2PCDIS):** **Priority2 Pool Count Disable:** When set, priority2 pool becomes unlimited. And priority2 pool count value should not be used in reset of the remaining counters.
23:21	RW	000b	Core	**Priority2 Pool count (PRIO2PC):** Priority2 Pool Count: The count of cycles is selected from priority2 pool before switching to lower priority pools. Count is used as the power of 2. 000: 1 request 001: 2 requests 010: 4 requests 011: 8 requests ….. 111: 128 requests
20	RW	0b	Core	**Priority1 Pool Count Disable (PRIO1PCDIS):** **Priority1 Pool Count Disable:** When set, priority1 pool becomes unlimited. And priority1 pool count value should not be used in reset of the remaining counters.
19:17	RW	000b	Core	**Priority1 Pool Count (PRIO1PC):** Priority1 Pool Count: The count of cycles is selected from priority1 pool before switching to lower priority pools. Count is used as the power of 2. 000: 1 request 001: 2 requests 010: 4 requests 011: 8 requests ….. 111: 128 requests
16	RW	0b	Core	**Priority0 Pool Count Disable (PRIO0PCDIS):** **Priority0 Pool Count Disable:** When set, priority0 pool becomes unlimited. And priority0 pool count value should not be used in reset of the remaining counters.
15:13	RW	000b	Core	**Priority0 Pool Count (PRIO0PC):** Priority0 Pool Count: The count of cycles is selected from priority0 pool before switching to lower priority pools. Count is used as the power of 2.

Bits	Access	Default Value	RST/PWR	Description
				000: 1 request 001: 2 requests 010: 4 requests 011: 8 requests ….. 111: 128 requests
12	RW	0b	Core	**Enable Priority Selection (PRIOEN):** Enable Priority Selection: Enables the use of priority bits coming from GFX core. If disabled, all slots in SQ is treated as same peiority 0 (default) : Disabled 1: Enable
11:8	RW	1111b	Core	**Super Queue Internal Register count (VTD):** SQ Mas VTD Cycles This is the binary value of the maximum number of VTd cycles that GTI Super Queue will accept from graphics before new VTd requests are throttled. In essence, this determines the depth of the VTd queue within the Super Queue. 0000 = 1 VTd cycle 0001 = 2 VTd cycles 0010 = 3 VTd cycles ... 1110 = 15 VTd cycles 1111 = 16 VTd cycles
7:0	RO	00h	Core	**LRU Hint counter (LRU):** Reserved

1.1.7 SQCFG - Super Queue GFX cycle Options register

B/D/F/Type: 0/0/0/MBCunit_Config
Address Offset: 902C-902Fh
Default Value: 00000000h
Access: RO, RW
Size: 32 bits

Super Queue GFX Cycle Options register.

Bits	Access	Default Value	RST/PWR	Description
31:3	RO	00000000h	Core	**Reserved (RSVD):** Reserved
2	RW	0b	Core	**SQ Read-Only Port Reject Disable (SQRORD):** SQ Read-Only Port Reject Disable This indicates whether rejections can be issued from the Super Queue to GFX for read cycles on the Read Only port. Rejected cycles are retried at a later time by GFX. By default, read cycles that have a matching address elsewhere in the Super Queue are rejected, and GFX is notified of the rejection. If this bit is set, no rejections will ever occur on the SQ-GFX interface. SQ will accept all requests, but in the case of a matching address, the SQ will stall the Read-Only port until the address match disappears (matching entry is retired by SQ). 1 = Rejections are disabled, SQ will stall if needed 0 = Rejections are enabled
1	RW	0b	Core	**SQ ReadPort GFX Read Ownership (SQRWO):** SQ Read Port GFX Read Ownership (SQRWO): SQ Read-Only Port GFX Read Ownership Indication This indicates the type of request that is issued to uncore for each read cycle from the GFX Read-Only port which produces a miss in the MLC. By default, read cycles that have no matching MLC entry will produce a regular read request from uncore through the IDI. If this bit is set, the request is changed from a regular read to a request for ownership (RFO) of the cacheline. This applies for all read requests from the GFX Read-Only port ONLY. 1 = All GFX reads from RO port require ownership of the cacheline 0 = GFX reads from RO port do
0	RW	0b	Core	**SQ Read-Only Port GFX Read (SQROO):** SQ Read-Only Port GFX Read (SQROO): SQ Read-Only Port GFX Read Ownership Indication This indicates the type of request that is issued to uncore for each read cycle from the GFX Read-Only port which produces a miss in the MLC. By default, read cycles that have no matching MLC entry will produce a regular read request from uncore through the IDI. If this bit is set, the request is changed from a regular read to a request for ownership (RFO) of the cacheline. This applies for all read requests from the GFX Read-Only port ONLY. 1 = All GFX reads from RO port require ownership of the cacheline 0 = GFX reads from RO port do

1.1.8 SQERR - SQ Error Status

B/D/F/Type: 0/2/0/MMADR_MBCunit_Config
Address Offset: 9034-9037h
Default Value: 00000000h
Access: RWC, RO
Size: 32 bits

SQ Error Status register

Bits	Access	Default Value	RST/PWR	Description
31:1	RO	00000000h	Core	**RSVD (RSVD):** RSVD
0	RWC	0b	Core	**SQ Address Decode Error (SQADDRERR):** SQ Address Decode Error

1.1.9 MFCR - Fence Control Register

B/D/F/Type: 0/2/0/MMADR_MBCunit_Config
Address Offset: 9070-9073h
Default Value: 00000000h
Access: RW, RO
Size: 32 bits

Fence Control Register:

Bits	Access	Default Value	RST/PWR	Description
31:16	RW	0000h	Core	**ECO RSVD (ECORSVD):** ECO purposes Reserved.
15:5	RO	00000000000b	Core	**RSVD (RSVD):** Reserved.
2	RW	0b	Core	**Write/Read Port Block (MFCBLK):** 0: Dont Block the R/W port when Query is started. 1: Block the R/W port until the Memory Fence is completed This is applicable for only Memory Fence.
1	RW	0b	Core	**LLC Query Enable (MFCLLC):** 0: Query for 16 Ways. 1: Query for 32 Ways. No Flexing.
0	RW	0b	Core	**Fence Controller GFDT Mode (MFCGFDT):** Fence Controller GFDT Mode: 0: Single bit GFDT mode. 1: Two bit GFDT mode.

1.1.10 MBCTL - MBC Control Register

B/D/F/Type: 0/0/0/MBCunit_Config
Address Offset:907C-907Fh
Default Value: 00000000h
Access: RW, RO
Size: 32 bits

MBC Control Register:

Bits	Access	Default Value	RST/PWR	Description
31:16	RW	0000000000000000b	Core	**ECORSVD (ECORSVD):** ECO purposes Reserved.
18:17	R/W	00	Core	**Multicast slice Read Return Select:** This field is provided to MCHGunit. End point based on this value selects one of the registers from multicast destinations. 00b means upper left half slice. 01b means upper right half slice. 10b means lower left half slice. 11b means lower right half slice.
16	R/W	0	Core	**VCR fuse R/W as posted.** 0: Not posted. 1: Posted.
15:6	RO	0000000000b	Core	**RSVD (RSVD):** RSVD.
5	RO	0h		**Reserved (RSVD).**
4	RW	0		**Enable Boot Fetch:** Config bit for driver managed boot kick off. 1 - Enable Boot Fetch without any PM interaction. 0 - Default (no action). The driver must set this bit in the following scenarios: • To reload the HW boot context every time it gets loaded through the OS. • After an FLR clears the register (the BIOS won't run afterwards).
3	RW	0b	Core	**Context Fetch Needed (CTXTFETCH):** Context Fetch Needed for Power Exits. 0 - Context Fetch Not Needed. 1 - Context Fetch Needed for Power Exits (CPD Entry).
2	RW	0b	Core	**BME Update Enable (BMEUE):**

Bits	Access	Default Value	RST/PWR	Description
				BME Update Enable: 0: Default. BME Update is not Enabled. MBC ignores all BME updates from SA. 1: BME update is Enabled.
1	RW	0b	Core	**MAE Update Enable (MBEUE):** MAE Update Enable - 0: Default. Mae Update is not Enabled. MBC ignores all MAE updates from SA. 1: MAE update is Enabled. MBC responds to MAE updates.
0	RW	0b	Core	**Boot Fetch Mechanism (BOOTF):** Choose between 2 different boot context fetch mechanisms: 0: Use MBC to GAM path with 8B reads (default). 1: Use MBC to Config Agent register interface with 4B reads.

1.1.11 TOLUD - Mirror of TOLUD

B/D/F/Type: 0/0/0/MBCunit_Config
Address Offset: 9090-9093h
Default Value: 00100000h
Access: RO
Size: 32 bits

Top of Low usable Dram.

Bits	Access	Default Value	RST/PWR	Description
31:20	RO	001h	Core	**TOLUD (TOLUD):** This register contains bits 31 to 20 of an address one byte above the maximum DRAM memory below 4G that is usable by the operating system. Address bits 31 down to 20 programmed to 01h implies a minimum memory size of 1MB. Configuration software must set this value to the smaller of the following 2 choices: maximum amount memory in the system minus ME stolen memory plus one byte or the minimum address allocated for PCI memory. Address bits 19:0 are assumed to be 0_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register. The Top of Low Usable DRAM is the lowest address above both Graphics Stolen memory and Tseg. BIOS determines the base of Graphics Stolen Memory by subtracting the Graphics Stolen Memory Size from TOLUD and further decrements by Tseg size to determine base of Tseg. This register must be 1MB aligned when reclaim is enabled.
19:0	RO	00000h	Core	**RSVD (RSVD):** Reserved

1.1.12 MGGC - Mirror of GMCH Graphics Control Register

B/D/F/Type: 0/0/0/MBCunit_Config
Address Offset:9094-9097h
Default Value: 00000030h
Access: RO
Size: 32 bits

Mirror of GMCH Graphics Control Register:

Bits	Access	Default Value	RST/PWR	Description
31:16	RO	0000h	Core	**RSVD (RSVD):** Reserved.
15	RO	0b	Core	**FLR Capability Structure Select (FLRCSSEL):** 1: The Vendor Specific Capability Structure is selected for FLR. 0: FLR uses the Standard Capability Structure with unique Capability ID assigned by PCISIG.
14	RO	0b	Core	**Versatile Acceleration Mode Enable (VAMEN):** Enables the use of the iGFX engines for Versatile Acceleration. 1 - iGFX engines are in Versatile Acceleration Mode. Device 2 Class Code is 048000h. 0 - iGFX engines are in iGFX Mode. Device 2 Class Code is 030000h.
13:10	RO	0000b	Core	**RSVD (RSVD):** Reserved.
9:8	RO	0h	Core	**GTT Graphics Memory Size (GGMS):** This field selects the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. GSM is assumed to be a contiguous physical DRAM space with DSM, and the BIOS needs to allocate a contiguous memory chunk. Hardware derives the base of GSM from DSM only using the GSM size programmed in the register. 0h: No memory pre-allocated. GTT cycles (Mem and I/O) are not claimed. 1h: 1 MB of memory pre-allocated for GTT. 2h: 2 MB of memory pre-allocated for GTT. 3h: Reserved. Hardware functionality in case of programming this value to Reserved is not guaranteed. This register is locked and becomes Read Only when the D_LCK bit in the SMRAMC register is set.
7:4	RO	3h	Core	**Graphics Mode Select (GMS):** This field selects the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS

<table>
<tr><th>Bits</th><th>Access</th><th>Default Value</th><th>RST/PWR</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td></td><td>ensures that memory is pre-allocated only when Internal graphics is enabled.

0h: No memory pre-allocated. Device 2 (IGD) does not claim VGA cycles (Mem and I/O), and the Sub-Class Code field within Device 2 function 0 Class Code register is 80.

1h-4h: Reserved.

5h-Dh: DVMT (UMA) mode, memory pre-allocated for frame buffer, in quantities as shown in the Encoding table.

Eh-Fh: Reserved.

NOTE: This register is locked and becomes Read Only when the D_LCK bit in the SMRAMC register is set. This register is also LT lockable.

Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled.

BIOS Requirement: BIOS must not set this field to 0h if IVD (bit 1 of this register) is 0.

<table>
<tr><th>Encoding</th><th>Description</th></tr>
<tr><td>0h</td><td>No memory preallocated</td></tr>
<tr><td>5h</td><td>32 MB</td></tr>
<tr><td>6h</td><td>48 MB</td></tr>
<tr><td>7h</td><td>64 MB</td></tr>
<tr><td>8h</td><td>128 MB</td></tr>
<tr><td>9h</td><td>256 MB</td></tr>
<tr><td>Ah</td><td>96 MB</td></tr>
<tr><td>Bh</td><td>160 MB</td></tr>
<tr><td>Ch</td><td>224 MB</td></tr>
<tr><td>Dh</td><td>352 MB</td></tr>
</table>
</td></tr>
<tr><td>3:2</td><td>RO</td><td>00b</td><td>Core</td><td>RSVD (RSVD):

Reserved.</td></tr>
<tr><td>1</td><td>RO</td><td>0b</td><td>Core</td><td>IGD VGA Disable (IVD):

0: Enable. Device 2 (IGD) claims VGA memory and I/O cycles, and the Sub-Class Code field within Device 2 Class Code register is 00.

1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and I/O), and the Sub-Class Code field within Device 2 function 0 Class Code register is 80.

BIOS Requirement: BIOS must not set this bit to 0 if the GMS field (bits 6:4 of this register) pre-allocates no memory.

This bit MUST be set to 1 if Device 2 is disabled either via a fuse or fuse override (CAPID0[46] == 1) or via a register (DEVEN[3] == 0).

This register is locked by LT lock.</td></tr>
<tr><td>0</td><td>RO</td><td>0b</td><td>Core</td><td>RSVD (RSVD):

Reserved.</td></tr>
</table>

1.1.13 TOUUD - Mirror of TOUUD

B/D/F/Type:	0/0/0/MBCunit_Config
Address Offset:	9098-909Fh
Default Value:	0000000000000000h
Access:	RO
Size:	64 bits

TOUUD

Bits	Access	Default Value	RST/PWR	Description
63:39	RO	0000000h	Core	**RSVD (RSVD):** Reserved
38:20	RO	00000000000000000000b	Core	**TOUUD LOW (TOUUD):** This register contains bits 38 to 20 of an address one byte above the maximum DRAM memory above 4G that is usable by the operating system. Configuration software must set this value to TOM minus all EP stolen memory if reclaim is disabled. If reclaim is enabled, this value must be set to reclaim limit 1MB aligned since reclaim limit + 1byte is 1MB aligned. Address bits 19:0 are assumed to be 000_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than 4GB.
19:0	RO	00000000000000000000b	Core	**RSVD (RSVD):** Reserved

1.1.14 DSMB - Mirror of DSMBASE

B/D/F/Type:	0/0/0/MBCunit_Config
Address Offset:	90A0-90A3h
Default Value:	00000000h
Access:	RO
Size:	32 bits

DSM Base:

Bits	Access	Default Value	RST/PWR	Description
31:20	RO	000h	Core	**DSM Base Lower 32 Bits (DSMBL):** This register contains bits 31 to 20 of the base address of stolen DRAM memory. The BIOS determines the base of graphics stolen memory by subtracting the graphics stolen memory size (PCI Device 0 offset 52 bits 6:4) from TOLUD (PCI Device 0 offset BC bits 31:20).

Bits	Access	Default Value	RST/PWR	Description
19:0	RO	00000h	Core	**RSVD (RSVD):** Reserved

1.1.15 GSMB - Mirror of GSMBASE

B/D/F/Type: 0/0/0/MBCunit_Config

Address Offset: 90A4-90A7h

Default Value: 00000000h

Access: RO

Size: 32 bits

This register contains the base address of stolen DRAM memory for the GTT. The BIOS determines the base of GTT stolen memory by subtracting the GTT graphics stolen memory size (PCI Device 0 offset 52 bits 11:8) from the Graphics Base of Data Stolen Memory (PCI Device 0 offset B0 bits 31:20).

Bits	Access	Default Value	RST/PWR	Description
31:20	RO	000h	Core	**GSM Base (GSMB):** This register contains the base address of stolen DRAM memory for the GTT. The BIOS determines the base of GTT stolen memory by subtracting the GTT graphics stolen memory size (PCI Device 0 offset 52 bits 11:8) from the Graphics Base of Data Stolen Memory (PCI Device 0 offset B0 bits 31:20).
19:0	RO	00000h	Core	**RSVD (RSVD):** Reserved

1.1.16 GCMD - Mirror of Global Command Register

B/D/F/Type: 0/0/0/MBCunit_Config

Address Offset: 90CC-90CFh

Default Value: 00000000h

Access: RO

Size: 32 bits

Bits	Access	Default Value	RST/PWR	Description
31	RO	0b	Core	**Translation Enable (TE):** Software writes to this field to request hardware to enable/disable DMA-remapping hardware. 0: Disable DMA-remapping hardware. 1: Enable DMA-remapping hardware. Hardware reports the status of the translation enable operation

				through the TES field in the Global Status register. Before enabling (or re-enabling) DMA-remapping hardware through this field, software must: 1. Setup the DMA-remapping structures in memory. 2. Flush the write buffers (through the WBF field), if write buffer flushing is reported as required. 3. Set the root-entry table pointer in hardware (through the SRTP field). 4. Perform global invalidation of the context cache and global invalidation of the IOTLB. 5. If advanced fault logging is supported, setup the fault log pointer (through the SFL field) and enable advanced fault logging (through the EAFL field). Refer to Section 9 for detailed software requirements. There may be active DMA requests in the platform when software updates this field. Hardware must enable or disable remapping logic only at deterministic transaction boundaries, so that any in-flight transaction is either subject to remapping or not at all. Hardware implementations supporting DMA draining must drain any in-flight translated DMA read/write requests queued within the root complex before completing the translation enable command and reflecting the status of the command through the TES field in the GSTS_REG. Reading this bit returns an undefined value.
30	RO	0b	Core	**Set Root Table Pointer (SRTP):** Software sets this field to set/update the root-entry table pointer used by hardware. The root-entry table pointer is specified through the Root-entry Table Address register. Hardware reports the status of the "root table pointer set" operation through the RTPS field in the Global Status register. The root table pointer set operation must be performed before enabling or re-enabling (after disabling) DMA remapping through the TE field. After a "root table pointer set" operation, software must globally invalidate the context cache and then globally invalidate the IOTLB. This is required to ensure hardware uses only the remapping structures referenced by the new root table pointer, and not any stale cached entries. While DMA remapping is active, software may update the root table pointer through this field. However, to ensure valid in-flight DMA requests are deterministically remapped, software must ensure that the structures referenced by the new root table pointer are programmed to provide the same remapping results as the structures referenced by the previous root-table pointer. Clearing this bit has no effect. Reading this bit returns an undefined value.
29	RO	0b	Core	**Set Fault Log (SFL):**

				This field is valid only for implementations supporting advanced fault logging. Software sets this field to request hardware to set/update the fault-log pointer used by hardware. The fault-log pointer is specified through the Advanced Fault Log register. Hardware reports the status of the fault log set operation through the FLS field in the Global Status register. The fault log pointer must be set before enabling advanced fault logging (through the EAFL field). Once advanced fault logging is enabled, the fault log pointer may be updated through this field while DMA remapping is active. Clearing this bit has no effect. Reading this bit returns an undefined value.
28	RO	0b	Core	**Enable Fault Logging (EAFL):** This field is valid only for implementations supporting advanced fault logging. Software writes to this field to request hardware to enable or disable advanced fault logging. 0: Disable advanced fault logging. In this case, translation faults are reported through the Fault Recording registers. 1: Enable use of memory-resident fault log. When enabled, translation faults are recorded in the memory-resident log. The fault log pointer must be set in hardware (through the SFL field) before enabling advanced fault logging. Hardware reports the status of the advanced fault logging enable operation through the AFLS field in the Global Status register. Reading this bit returns an undefined value.
27	RO	0b	Core	**Write Buffer Flush (WBF):** This bit is valid only for implementations requiring write buffer flushing. Software sets this field to request hardware to flush the root-complex internal write buffers. This is done to ensure any updates to the memory-resident remapping structures are not held in any internal write posting buffers. Refer to Section 11.1 for details on write-buffer flushing requirements. Hardware reports the status of the write buffer flushing operation through the WBFS field in the Global Status register. Clearing this bit has no effect. Reading this bit returns an undefined value.
26	RO	0b	Core	**Queued Invalidation Enable (QIE):** This field is valid only for implementations supporting queued invalidations.

				Software writes to this field to enable or disable queued invalidations. 0: Disable queued invalidations. 1: Enable queued invalidations. Hardware reports the status of queued invalidation enable operations through the QIES field in the Global Status register. Refer to Section 6.2.2 for software requirements for enabling/disabling queued invalidations. Reading this bit returns an undefined value.
25	RO	0b	Core	**Interrupt Remapping Enable (IRE):** This field is valid only for implementations supporting interrupt remapping. 0: Disable interrupt-remapping hardware 1: Enable interrupt-remapping hardware Hardware reports the status of the interrupt remapping enable operation through the IRES field in the Global Status register. There may be active interrupt requests in the platform when software updates this field. Hardware must enable or disable interrupt-remapping logic only at deterministic transaction boundaries, so that any in-flight interrupts are either subject to remapping or not at all. Hardware implementations must drain any in-flight interrupts requests queued in the Root-Complex before completing the interrupt-remapping enable command and reflecting the status of the command through the IRES field in the Global Status register. Reading this bit returns an undefined value.
24	RO	0b	Core	**Set Interrupt Remap Table Pointer (SIRTP):** This field is valid only for implementations supporting interrupt-remapping. Software sets this field to set/update the interrupt remapping table pointer used by hardware. The interrupt remapping table pointer is specified through the Interrupt Remapping Table Address register. Hardware reports the status of the interrupt remapping table pointer set operation through the IRTPS field in the Global Status register. The interrupt remap table pointer set operation must be performed before enabling or re-enabling (after disabling) interrupt-remapping hardware through the IRE field. After an interrupt remap table pointer set operation, software must globally invalidate the interrupt entry cache. This is required to ensure hardware uses only the interrupt-remapping entries referenced by the new interrupt remap table pointer, and not any stale cached entries. While interrupt remapping is active, software may update the

				interrupt remapping table pointer through this field. However, to ensure valid in-flight interrupt requests are deterministically remapped, software must ensure that the structures referenced by the new interrupt remap table pointer are programmed to provide the same remapping results as the structures referenced by the previous interrupt remap table pointer. Clearing this bit has no effect. Reading this bit returns an undefined value.
23	RO	0b	Core	**Compatibility Format Interrupt (CFI):** This field is valid only for Intel(R)64 implementations supporting interrupt-remapping. Software writes to this field to enable or disable Compatibility Format interrupts on Intel(R)64 platforms. The value in this field is effective only when interrupt-remapping is enabled and Legacy Interrupt Mode is active. 0: Block Compatibility format interrupts. 1: Process Compatibility format interrupts as pass-throughs (bypass interrupt remapping). Hardware reports the status of updating this field through the CFIS field in the Global Status register. Refer to Section 5.4.1 for details on Compatibility Format interrupt requests. The value returned on a read of this field is undefined. This field is not implemented on Itanium(TM) implementations.
22:0	RO	000000h	Core	**RSVD (RSVD):** Reserved

1.1.17 GTTMMADR - Mirror of Graphics Translation Table and Memory Mapped Range Address

B/D/F/Type: 0/0/0/MBCunit_Config

Address Offset: 9124-912Bh

Default Value: 0000000000000000h

Access: RO

Size: 64 bits

This register requests allocation for the combined Graphics Translation Table Modification Range and Memory Mapped Range. The range requires 4 MB combined for MMIO and Global GTT aperture, with 2MB of that used by MMIO and 2MB used by GTT. GTTADR begins at (GTTMMADR + 2 MB) while the MMIO base address is the same as GTTMMADR.

For the Global GTT, this range is defined as a memory BAR in graphics device config space. It is an alias into which software is required to write Page Table Entry values (PTEs). Software may read PTE values from the global Graphics Translation Table (GTT). PTEs cannot be written directly into the global GTT memory area.

The device snoops writes to this region to invalidate any cached translations within the various TLBs implemented on-chip. There are some exceptions to this - see GTT-TLB in the Programming Interface chapter.

The allocation is for 4MB and the base address is defined by bits [38:22].

Bits	Access	Default Value	RST/PWR	Description
63:39	RO	0000000h	Core	**RSVD (RSVD):** Reserved
38:22	RO	00000000000000000b	Core	**Memory Base Address (MMADR):** Set by the OS, these bits correspond to address signals [38:22]. 4MB combined for MMIO and Global GTT table aperture (2MB for MMIO and 2 MB for GTT).
21:4	RO	000000000000000000b	Core	**RSVD (RSVD):** Reserved
3	RO	0b	Core	**Prefetchable Memory (PREFMEM):** Hardwired to 0 to prevent prefetching.
2:1	RO	00b	Core	**Memory Type (MEMTYP):** 00b: To indicate 32 bit base address 01b: Reserved 10b: To indicate 64 bit base address 11b: Reserved
0	RO	0b	Core	**Memory I/O Space (MIOS):** Hardwired to 0 to indicate memory space.

1.1.18 PCICMD - Mirror of PCICMD MAE/BME

B/D/F/Type: 0/0/0/MBCunit_Config

Address Offset: 912C-912Fh

Default Value: 00000000h

Access: RW

Size: 32 bits

Mirror of PCICMD MAE/BME:

Bits	Access	Default Value	RST/PWR	Description
31:11	RW	000000h	Core	**RSVD (RSVD):** Reserved.
10	RW	0b	Core	**Interrupt Disable (INTDIS):**

Bits	Access	Default Value	RST/PWR	Description
				This bit disables the device from asserting INTx#. 0: Enable the assertion of this device's INTx# signal. 1: Disable the assertion of this device's INTx# signal. DO_INTx messages are not sent to DMI. GSA Implementation: When 1, blocks the sending of a MSI interrupt and blocks the sending of a Line interrupt. (The interrupt status is not blocked from being reflected in the INTSTS bit.) When 0, permits the sending of a MSI interrupt or Line interrupt.
9	RW	0b	Core	**Fast Back to Back (FB2B):** Not Implemented. Hardwired to 0.
8	RW	0b	Core	**SERR Enable (SERRE):** Not Implemented. Hardwired to 0.
7	RW	0b	Core	**Address/Data Stepping Enable (ADSPTEP):** Not Implemented. Hardwired to 0.
6	RW	0b	Core	**Parity Error Enable (PERRE):** Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.
5	RW	0b	Core	**Video Pallete Snooping (VPS):** This bit is hardwired to 0 to disable snooping.
4	RW	0b	Core	**Memory Write and Invalidate Enable (MWIE):** Hardwired to 0. The IGD does not support memory write and invalidate commands.
3	RW	0b	Core	**Special Cycle Enable (SCE):** This bit is hardwired to 0. The IGD ignores Special cycles.
2	RW	0b	Core	**Bus Master Enable (BME):** 0: Disable IGD bus mastering. 1: Enable the IGD to function as a PCI compliant master. GSA Implementation: 0: Disable sending MSI interrupts. 1: Enable sending MSI interrupts. (Note: See descriptions of INTDIS, MSE, and INTSTS bits.)
1	RW	0b	Core	**Memory Access Enable (MAE):**

Bits	Access	Default Value	RST/PWR	Description
				This bit controls the IGD's response to memory space accesses. 0: Disable. 1: Enable.
0	RW	0b	Core	**I/O Access Enable (IOAE):** This bit controls the IGD's response to I/O space accesses. 0: Disable. 1: Enable.

1.1.19 PERFCNT1 - Performance Counter 1

B/D/F/Type: 0/2/0/MMADR_MBCunit_Config

Address Offset: 91B8-91BFh

Default Value: 0000000000000000h

Access: RO, RW

Size: 64 bits

GT implements two general purpose counters each with 44 bits. Each counter can be programmed to count one main event out of set of events (see the event list). Some events are simple duration events and some are edge detects (0=>1 transition is counted). The nature of the event is also programmed to the register that allocates the counter value.

Bits	Access	Default Value	RST/PWR	Description
63	RW	0b	Core	**Counter 1 Enable (CNT1EN):** Counter#1 Enable 0: Counter is disabled, the count value is not deterministic. 1: Counter is enabled. Once enabled, the counter is activated if the global enable (from NCU is also asserted).
62	RW	0b	Core	**Overflow Enable (OVFEN):** Overflow Enable 0: Overflow reporting is enabled. 1: Overflow reporting is disabled.
61	RW	0b	Core	**Edge Detect (EDGEDET):** Edge Detect: 0: Edge detect is enabled. 1: Edge detect is disabled.
60	RW	0b	Core	**Counter Clear (CNTCLR):** Counter Clear.

Bits	Access	Default Value	RST/PWR	Description
59:52	RW	00000000b	Core	**Event Selection (EVENTSEL):** Event Selection: The event list (see attached). Used as a MUX control to select the event to Counter.
51:44	RO	00000000b	Core	**RSVD (RSVD):** Reserved.
43:0	RO	00000000000h	Core	**Counter Value (CNTVALUE):** The Counter Value: This is the field where the counter value can be observed via a simple read from the register.

1.1.20 PERFCNT2 - Performance Counter 2

B/D/F/Type: 0/2/0/MMADR_MBCunit_Config

Address Offset: 91C0-91C7h

Default Value: 0000000000000000h

Access: RO, RW

Size: 64 bits

GT implements two general purpose counters each with 44 bits. Each counter can be programmed to count one main event out of the set of events (see the event list). Some events are simple duration events and some are edge detects (0=>1 transition is counted). The nature of the event is also programmed to the register that allocates the counter value.

Bits	Access	Default Value	RST/PWR	Description
63	RW	0b	Core	**Counter 2 Enable (CNT2EN):** Counter#2 Enable 0: Counter is disabled, the count value is not deterministic. 1: Counter is enabled. Once enabled, the counter is activated if the global enable (from NCU is also asserted).
62	RW	0b	Core	**Overflow Enable (OVFEN):** Overflow Enable 0: Overflow reporting is enabled. 1: Overflow reporting is disabled.
61	RW	0b	Core	**Edge Detect (EDGEDET):** Edge Detect: 0: Edge detect is enabled. 1: Edge detect is disabled.
60	RW	0b	Core	**Counter Clear (CNTCLR):** Counter Clear.

Bits	Access	Default Value	RST/PWR	Description
59:52	RW	00000000b	Core	**Event Selection (EVENTSEL):** Event Selection: The event list (see attached). Used as a MUX control to select the event to Counter.
51:44	RO	00000000b	Core	**RSVD (RSVD):** Reserved.
43:0	RO	00000000000h	Core	**Counter Value (CNTVALUE):** The Counter Value: This is the field where the counter value can be observed via a simple read from the register.

1.1.21 PERFMATRIX - Performance Matrix Events

B/D/F/Type: 0/2/0/MMADR_MBCunit_Config

Address Offset: 91C8-91CFh

Default Value: 0000000000000000h

Access: RW, RO

Size: 64 bits

Performance Matrix Events:

Bits	Access	Default Value	RST/PWR	Description
63:38	RO	0000000h	Core	**RSVD (RSVD):** Reserved.
37	RW	0b	Core	**NON Dram (NONDRAM):** Non DRAM - Target was non-DRAM system address.
36	RW	0b	Core	**Hit Modified (HITM):** A snoop was needed and it HitMed in local or remote cache. HitM denotes a cache-line was modified before snoop effect. This includes: -Snoop HitM w/ Invalidation and WB (LLC miss, CRD/DRD) -Snoop Forward Modified w/ Invalidation (LLC Hit/Miss, RFO) -Snoop MtoS (LLC Hit, CRD/DRD)
35	RW	0b	Core	**Hit with Forward (HITFWD):** A snoop was needed and data was Forwarded from a remote socket. -Snoop Forward Clean, Left Shared (LLC Miss, CRD/DRD)
34	RW	0b	Core	**Hit No Forward (HITNOFWD):** A snoop was needed and it Hits in at least one snooped cache. Hit denotes a cache-line was valid before snoop effect. This includes:

Bits	Access	Default Value	RST/PWR	Description
				-Snoop Hit w/ Invalidation (LLC Hit, RFO) -Snoop Hit, Left Shared (LLC Hit/Miss, CRD/DRD) -Snoop Forward Clean w/ Invalidation (LLC Miss, RFO)
33	RW	0b	Core	**SNOOP Miss (SMISS):** A snoop was need and it missed all snooped caches: -For LLC Hit, RespIHitI was returned by all cores -For LLC Miss, RspI was returned by all sockets
32	RW	0b	Core	**NO Snoop Was needed (NOSNP):** No snoop was neeeded to satisfy the request.
31	RW	0b	Core	**NONE - No Details as to Snoop related infor (NONE):** NONE - No Details as to Snoop related information.
30	RW	0b	Core	**NID7 (NID 7):** NID 7
29	RW	0b	Core	**NID6 (NID 6):** NID 6
28	RW	0b	Core	**NID5 (NID 5):** NID 5
27	RW	0b	Core	**NID4 (NID 4):** NID 4
26	RW	0b	Core	**NID3 (NID 3):** NID 3
25	RW	0b	Core	**NID2 (NID 2):** NID 2
24	RW	0b	Core	**NID1 (NID 1):** NID 1
23	RW	0b	Core	**NID0 (NID0):** NID 0
22	RW	0b	Core	**Local Node (LOCALNODE):** Local Node.
21	RW	0b	Core	**F-STATE (FSTATE):**

Bits	Access	Default Value	RST/PWR	Description
				F-STATE
20	RW	0b	Core	**S-State (SSTATE):** S-State
19	RW	0b	Core	**E-STATE (ESTATE):** E-STATE
18	RW	0b	Core	**M-STATE (MSTATE):** M-state
17	RW	0b	Core	**No Supplier Details (NONE):** No Supplier Details.
16	RW	0b	Core	**Snoop Response from Uncore (SNPRSP):** Account for any snoop response from Uncore.
15	RW	0b	Core	**IDI requests (ANYIDIREQ):** Any - any requests that crosses IDI.
14:12	RO	000b	Core	**RSVD (RSVD):** Reserved.
11	RW	0b	Core	**WCIL AND WCILF (WCIL):** Write Combining.
10	RW	0b	Core	**LOCK (LCKSPLIT):** Locks – count locks and split lock requests.
9	RW	0b	Core	**MLC Prefetch to LLC (LLCPREFCODE):** MLC prefetch to LLC - Code.
8	RW	0b	Core	**LLCRFO (LLCPREFRFO):** MLC prefetch to LLC - RFO.
7	RW	0b	Core	**MLC Prefetch to LLC (LLCPREFDATA):** MLC prefetch to LLC - Load (exclude LRUhints).
6	RW	0b	Core	**MPL RFOs (PFRFO):** PF Ifetch = MPL Fetches.
5	RW	0b	Core	**PF Ifetch (PFFETCH):** PF Ifetch = MPL Fetches.
4	RW	0b	Core	**MPL Reads (PFDATARD):**

Bits	Access	Default Value	RST/PWR	Description
				PF Data Rd = MPL Reads.
3	RW	0b	Core	**Write Back (DCUWB):** Writeback = MLC_EVICT/DCUWB.
2	RW	0b	Core	**Demand Ifetch (IFUFETCH):** Demand Ifetch = IFU Fetches.
1	RW	0b	Core	**Demand RFO (DCURFO):** Demand RFO = DCU RFOs.
0	RW	0b	Core	**Demand Data Rd (DATARD):** Demand Data Rd = DCU reads (exclude partials).

1.2 MBCunit Message

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
IDI MESSAGES	IDIMSG	8500h	8503h	00000000h	RO, RW
BOOT VECTOR	BOOTMSG	8504h	8507h	00000000h	RO, RW
GFX / DPR Update Message Bits	GFXPMRDPR	8508h	850Bh	00000000h	RO, RW
IDI Lookup Register 1	IDILK1	8510h	8513h	00000000h	RW, RO
IDI Lookup Register 2	IDILK2	8514h	8517h	00000000h	RW, RO

1.2.1 IDIMSG - IDI MESSAGES

B/D/F/Type: 0/0/0/MBCunit_Message

Address Offset: 8500-8503h

Default Value: 00000000h

Access: RO, RW

Size: 32 bits

BIOS Optimal Default 00h

IDI Message:

Bits	Access	Default Value	RST/PWR	Description
31:16	RO	0000h	Core	**Mask Bits (MASKB):** Reserved
15:11	RO	0h		**Reserved (RSVD)**
10	RW	0b	Core	**MBC Busy ACK (BUSYACK):** 1 - Busy ACK from GPMunit(Non-Idle). 0 - Non Busy ACK from Gpmunit (Idle).

Bits	Access	Default Value	RST/PWR	Description
				This bit is valid only if bit 26 of this register is set.
9	RW	0b	Core	**VTD Invalidation (VTDINV):** VTD invalidation from SA. This bit is valid only if bit 25 of this register is set.
8	RW	0b	Core	**VTD Enable and Disable (VTDED):** VTD Enable and Disable message from SA. This bit is valid only if bit 24 of this register is set.
7	RO	0b	Core	**RSVD (RSVD):** RSVD.
6	RW	0b	Core	**CPD Entry and Exits (CPD):** CPD Entry and Exit indication. This bit is valid only if bit 22 of this register is set. CPD Entry = 1. CPD Exit = 0.
5	RW	0b	Core	**Unblock MMIO ack (UNBLKACK):** Unblock MMIO ACK coming from SA. This bit is valid only if bit 21 of this register is set.
4	RW	0b	Core	**Mbcunit Arbitration request/Release ACK (ARBREQRELACK):** Arbitration request is sent during the MAE update. The ack is received from GPMunit. This bit is valid only if bit 20 of this register is set. Arb req ack = 1. Arb release ack = 0.
3	RW	0b	Core	**IDI Shutdown request (IDISD):** IDI Shutdown Request from GPM to MBCunit. This bit is valid only if bit 19 of this register is set.
2	RW	0b	Core	**IDI Wakeup Message (IDIWK):** IDI wakeup message from PM to MBCunit. This bit is valid only if bit 18 of this register is set.
1	RW	0b	Core	**Credit Active De-assertreq ACK (CDA):** Credit Active De-assertreq ACK - GPMunit sends to the MBCunit. This bit is valid only if bit 17 of this register is set.
0	RO	0b	Core	**RSVD (RSVD):** Reserved

1.2.2 BOOTMSG - BOOT VECTOR

B/D/F/Type: 0/0/0/MBCunit_Message

Address Offset: 8504-8507h

Default Value: 00000000h

Access: RO, RW

Size: 32 bits

Bits	Access	Default Value	RST/PWR	Description
31:30	RO	00b	Core	**Reserved (RSVD)**
29:26	RW	0000b	Core	**APICID (APICID):** Place holder for APIC ID
25:21	RW	00000b	Core	**Way Number for C6 (WC6):** Way Marker for C6 Save area
20:17	RW	0000b	Core	**Slice Marker for C6 save area (SLC6):** Slice Marker for C6 Save area
16	RO	0b	Core	**Reserved (RSVD)**
15:9	RW	0000000b	Core	**C6 Area Pointer (C6PTR):** C6 Area Pointer
8	RW	0b	Core	**Patch Restore (PR)**
7	RW	0b	Core	**APIC RESTORE (APR)**
6	RW	0b	Core	**Core Content Restore (CCR)**
5:4	RW	00b	Core	**Reset Type Register (RTYP)**
3:0	RW	0000b	Core	**Ring Stop ID (RID)**

1.2.3 GFXPMRDPR - GFX/DPR Update Message Bits

B/D/F/Type: 0/0/0/MBCunit_Message

Address Offset: 8508-850Bh

Default Value: 00000000h

Access: RO, RW

Size: 32 bits

This is the GFX, and DPR update Message from SA. The MBCunit does the needed operation whenever there is an Update.

Bits	Access	Default Value	RST/PWR	Description
31:16	RO	0000h	Core	**Mask Bits (MB):**
15:8	RO	00000000b	Core	**RSVD (RSVD):** Reserved

Bits	Access	Default Value	RST/PWR	Description
7	RW	0b	Core	**VCSFLUSH ACK (VCSFLSHACK):** VCS to MBC Flush ACK message.
6	RW	0b	Core	**BCS2MBCFLSH ACK (BCSFLSHACK):** BCS2MBC Flush ACK message.
5	RW	0b	Core	**CS2MBC Flush ACK (CSFLSHACK):** CS 2 MBC Flush ACK Message Bit.
4	RW	0b	Core	**VCS to MBC stop execution ACK (VCSSTOPEXACK):** BCS to MBC stop execution ACK message.
3	RW	0b	Core	**BCS to MBC Stop Execution ACK (BCSSTOPEXACK):** BCS to MBC stop execution ACK.
2	RW	0b	Core	**CS MBC VTD Stop Ex ACK (CSSTOPACK):** CS to MBC ACK message for stopping the Execution of CS.
1	RW	0b	Core	**DPR Update (DPRED):** DPR Update - Valid with Mask bit 17th.

1.2.4 IDILK1 - IDI Lookup Register 1

B/D/F/Type: 0/0/0/MBCunit_Message

Address Offset: 8510-8513h

Default Value: 00000000h

Access: RW, RO

Size: 32 bits

IDI Lookup Register 1:

Bits	Access	Default Value	RST/PWR	Description
31:17	RO	0000h	Core	**Reserved (RSVD):** Reserved.
16:13	RW	0000b	Core	**GT Logical ID (LOGID):** Logical ID for GT.
12	RO	0b	Core	**RSVD for SA (RSVD):** Reserved for SA slice.
11	RW	0b	Core	**Colloc bit for SA Slice (CBSA):**

Bits	Access	Default Value	RST/PWR	Description
				Co-located indicates that the Collocated Cbo should receive this request.
10	RW	0b	Core	**Direction Bit for SA (DBSA):** In Half ring uncore topologies this bit indicates if the request needs to be driven on the Up going (1) or the Down going (0) ring direction. For Full ring it indicates clockwise (1) or counterclockwise (0) directions. 1: Going Up. 0: Going Down.
9	RW	0b	Core	**Polarity bit for SA Slice (PBSA):** Polarity based on the current core Slice ID and the Destination Cbo ID - should this request be sent to the rings in Even or Odd cycles (this is basically the Distance between the source and destination). 1 - Even. 0 - Odd.
8	RW	0b	Core	**For Me bit for SA (FMSA):** The next slice the Target of this request (MyNeighborId == DestCboId).
7:4	RW	0000b	Core	**Number of LLC SA Slices (LLCNUMSLICE):** Number of Slice information in the system. This register contains the number of LLC cache slices on the RING. Default: 0000b
3:0	RW	0000b	Core	**Colocated Slice ID for GT (CLSID):** This register contains the ID of the slice that is servicing GT's co-located cycles. The default is for slice0 to service GT.

1.2.5 IDILK2 - IDI Lookup Register 2

B/D/F/Type: 0/0/0/MBCunit_Message

Address Offset: 8514-8517h

Default Value: 00000000h

Access: RW, RO

Size: 32 bits

IDI Lookup Register 2:

Bits	Access	Default Value	RST/PWR	Description
31:30	RO	00b	Core	**RSVD (RSVD):** Reserved.

Bits	Access	Default Value	RST/PWR	Description
29	RO	0b	Core	**Reserved for Slice 5 (RSVD):** Reserved for Slice 5.
28	RW	0b	Core	**Colloc bit for Slice 5 (CBS5):** Co-located indicates that the Collocated Cbo should receive this request.
27	RW	0b	Core	**Direction bit for Slice 5 (DBS5):** In Half ring uncore topologies this indicates: 1: Going Up. 0: Going Down.
26	RW	0b	Core	**Polarity bit for Slice 5 (PBS5):** Polarity based on the current core Slice ID and the Destination Cbo ID - should this request be sent to the rings in Even or Odd cycles (this is basically the Distance between the source and destination). 1 - Even. 0 - Odd.
25	RW	0b	Core	**For Me for Slice 5 (FMS5):** The next slice the Target of this request (MyNeighborId == DestCboId)
24	RO	0b	Core	**Reserved for Slice 4 (RSVD):** Reserved.
23	RW	0b	Core	**Colloc bit for Slice 4 (CBS4):** Co-located indicates that the Collocated Cbo should receive this request.
22	RW	0b	Core	**Direction bit for Slice 4 (DBS4):** In Half ring uncore topologies this indicates: 1: Going Up. 0: Going Down.
21	RW	0b	Core	**Polarity Bit for Slice 4 (PBS4):** Polarity based on the current core Slice ID and the Destination Cbo ID - should this request be sent to the rings in Even or Odd cycles (this is basically the Distance between the source and destination). 1 - Even. 0 - Odd.
20	RW	0b	Core	**For Me bit for Slice 4 (FMS4):** The next slice the Target of this request (MyNeighborId == DestCboId).
19	RW	0b	Core	**Reserved for Slice 3 (RSVD):**

Bits	Access	Default Value	RST/PWR	Description
				Reserved for Slice 3.
18	RW	0b	Core	**Colloc bit for Slice 3 (CBS3):** Co-located indicates that the Collocated Cbo should receive this request.
17	RW	0b	Core	**Direction bit for S3 (DBS3):** In Half ring uncore topologies this indicates: 1: Going Up. 0: Going Down.
16	RW	0b	Core	**Polarity Bit for Slice 3 (PBS3):** Polarity based on the current core Slice ID and the Destination Cbo ID - should this request be sent to the rings in Even or Odd cycles (this is basically the Distance between the source and destination). 1 - Even. 0 - Odd.
15	RW	0b	Core	**For Me Bit for Slice 3 (FMS3):** The next slice the Target of this request (MyNeighborId == DestCboId).
14	RO	0b	Core	**Reserved for Slice 2 (RSVD):** Reserved for Slice2.
13	RW	0b	Core	**Colloc bit for Slice 2 (CBS2):** Co-located indicates that the Collocated Cbo should receive this request.
12	RW	0b	Core	**Direction Bit for Slice 2 (DBS2):** In Half ring uncore topologies this indicates: 1: Going Up. 0: Going Down.
11	RW	0b	Core	**Polarity Bit for Slice 2 (PBS2):** Polarity based on the current core Slice ID and the Destination Cbo ID - should this request be sent to the rings in Even or Odd cycles (this is basically the Distance between the source and destination). 1 - Even. 0 - Odd.
10	RW	0b	Core	**For me Bit for Slice 2 (FMS2):** The next slice the Target of this request (MyNeighborId == DestCboId).
9	RO	0b	Core	**Reserved bit for Slice 1 (RSVD):** Reserved for Slice1.

Bits	Access	Default Value	RST/PWR	Description
8	RW	0b	Core	**Colloc Bit for Slice 1 (CBS1):** Co-located indicates that the Collocated Cbo should receive this request.
7	RW	0b	Core	**Direction Bit for Slice 1 (DBS1):** In Half ring uncore topologies this indicates: 1: Going Up. 0: Going Down.
6	RW	0b	Core	**Polarity Bit for Slice 1 (PBS1):** Polarity based on the current core Slice ID and the Destination Cbo ID - should this request be sent to the rings in Even or Odd cycles (this is basically the Distance between the source and destination). 1 - Even. 0 - Odd.
5	RW	0b	Core	**For Me Bit for Slice 1 (FMS1):** The next slice the Target of this request (MyNeighborId == DestCboId).
4	RO	0b	Core	**Reserved for Slice 0 (RSVD):** Reserved for Slice 0.
3	RW	0b	Core	**Colloc Bit for Slice 0 (CBS0):** Co-located indicates that the Collocated Cbo should receive this request.
2	RW	0b	Core	**Direction Bit in Slice0 (DBS0):** Direction bit for Slice0: In Half ring uncore topologies this indicates if the reqeust needs to be driven on the Up going (1) or the Down going (0) ring direction. For Full ring it indicates clockwise (1) or counterclockwise (0) directions. 1: Going Up. 0: Going Down.
1	RW	0b	Core	**Polarity Bit for Slice 0 (PBS0):** Polarity based on the current core Slice ID and the Destination Cbo ID - should this request be sent to the rings in Even or Odd cycles (this is basically the Distance between the source and destination). 1 - Even. 0 - Odd.
0	RW	0b	Core	**For Me bit for Slice0 (FMS0):** The next slice the Target of this request (MyNeighborId == DestCboId).

1.3 GDTunit Config Space

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
PSMI Base Register	PSMIBase	9870	9873	00000000h	RW
PSMI Control	PSMICtrl	9874	9877	00000000h	RO, RW/L
PSMI Status	PSMIStatus	9878	987C	0000000000h	RO

1.3.1 PSMIBase - PSMI Base Register

B/D/F/Type: 0/2/0/MMADR_GDTunit_Config

Address Offset: 9870-9873h

Default Value: 00000000h

Access: RW

Size: 32 bits

Host Physical Address of the PSMI Base of GT:

Bits	Access	Default Value	RST/PWR	Description
31:0	RW	00000000h	Core	**PSMI Base of GT (ADDR).**

1.3.2 PSMICtrl - PSMI Control

B/D/F/Type: 0/2/0/MMADR_GDTunit_Config

Address Offset: 9874-9877h

Default Value: 00000000h

Access: RO, RW/L

Size: 32 bits

PSMI Control:

Bits	Access	Default Value	RST/PWR	Description
31:4	RO	0000000h	Core	**Reserved (RSVD).**
3	RW/L	0b	Core	**Status of GT Sync (PSMISYNC):** Handler checks whether there is a need to sync the GT content.
2	RW/L	0b	Core	**Start PSMI Context Restore (PSMICON):** Before sending the PSMI restore request, poll until 12050h[4] == 1 AND 22050h[4] == 1.
1	RW/L	0b	Core	**Start PSMI Context Save (PSMIRES).**
0	RW/L	0b	Core	**AS1/AS2 Mode PSMI (Sync Mode) (PSMISEL):** 0: AS1 Mode PSMI - Sync Mode. 1: AS2 Mode PSMI - Scan Chain Based Approach.

1.3.3 PSMIStatus - PSMI Status

B/D/F/Type:	0/2/0/MMADR_GDTunit_Config
Address Offset:	9878-987Ch
Default Value:	0000000000h
Access:	RO
Size:	40 bits
BIOS Optimal Default:	0h

PSMI Status:

Bits	Access	Default Value	RST/PWR	Description
39:32	RO	0h		**Reserved (RSVD)**
31:2	RO	00000000000000000000000000000000b	Core	**Reserved (RSVD):** Reserved.
1	RO	0b	Core	**Context Restore Done Status (PSMICNT):** 1: Context Restore Is Done. 0: Context Restore is Not Done.
0	RO	0b	Core	**Reserved (RSVD):** Reserved.

1.4 GCPunit Config Register Space

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Unit Level Clock Gating Control 1	UCGCTL1	9400	9403	02F00000h	RW
Unit Level Clock Gating Control 2	UCGCTL2	9404	9407	00000000h	RW
Unit Level Clock Gating Control 3	UCGCTL3	9408	940B	04000000h	RW
Unit Level Clock Gating Control 4	UCGCTL4	940C	940F	00000003h	RO, RW
RAM Clock Gating Control 1	RCGCTL1	9410	9413	00000180h	RW, RO
RAM Clock Gating Control 2	RCGCTL2	9414	9417	00000000h	RW, RO
Integrated Power Supply Frequency Domain Impedance Meter Controls	IFDIMCTL	9418	941B	00000000h	RO, RW
Graphics Device Reset Control	GDRST	941C	941F	00000000h	RWHC, RO
Misc. Reset Control Register	RSTCTL	9420	9423	00000000h	RW, RO
Misc. Clocking/Reset Control Registers	MISCCPCTL	9424	9427	00000000h	RW

1.4.1 UCGCTL1 - Unit Level Clock Gating Control 1

B/D/F/Type: 0/2/0/MMADR_GCPunit_Config

Address Offset: 9400-9403h

Default Value: 02F00000h

Access: RW

Size: 32 bits

Unit Level Clock Gating Control Registers.

Bits	Access	Default Value	RST/PWR	Description
31	RW	0b	Core	**ISCunit Clock Gating Disable (cg3ddisisc):** ISCunit Clock Gating Disable Control:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
30	RW	0b	Core	**IEFunit Clock Gating Disable (cg3ddisief):** IEFunit Clock Gating Disable Control:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
29	RW	0b	Core	**IECPunit Clock Gating Disable (cg3ddisiecp):** IECPunit Clock Gating Disable Control:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
28	RW	0b	Core	**ICunit Clock Gating Disable (cg3ddisic):** ICunit Clock Gating Disable Control:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
27	RW	0b	Core	**HIZunit Clock Gating Disable (cg3ddishiz):** HIZunit Clock Gating Disable Control:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
26	RW	0b	Core	**GWunit Clock Gating Disable (cg3ddisgw):** GWunit Clock Gating Disable Control:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
25	RW	1b	Core	**GTIunit Clock Gating Disable (cg3ddisgti):** GTI Units Clock Gating Disable Control:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)

Bits	Access	Default Value	RST/PWR	Description
24	RW	0b	Core	**GSunit Clock Gating Disable (cg3ddisgs):** GSunit Clock Gating Disable Control:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
23	RW	1b	Core	**GPMunit Clock Gating Disable (cg3ddisgpm):** GPMunit Clock Gating Disable Control:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
22	RW	1b	Core	**GAMunit Clock Gating Disable (cg3ddisgam):** GAMunit Clock Gating Disable Control:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
21	RW	1b	Core	**GACunit Clock Gating Disable (cg3ddisgac):** GACunit Clock Gating Disable Control:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
20	RW	1b	Core	**GABunit Clock Gating Disable (cg3ddisgab):** GABunit Clock Gating Disable Control:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
19	RW	0b	Core	**FTunit Clock Gating Disable (cg3ddisft):** FTunit Clock Gating Disable Control:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
18	RW	0b	Core	**FLunit Clock Gating Disable (cg3ddisfl):** FLunit Clock Gating Disable Control:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
17	RW	0b	Core	**EU_MSunit Clock Gating Disable (cg3ddiseu_ms):** EU_MSunit Clock Gating Disable Control:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
16	RW	0b	Core	**EU_MDunit Clock Gating Disable (cg3ddiseu_md):** EU_MDunit Clock Gating Disable Control:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
15	RW	0b	Core	**EU_IFunit Clock Gating Disable (cg3ddiseu_if):** EU_IFunit Clock Gating Disable Control:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating

Bits	Access	Default Value	RST/PWR	Description
				Disabled. (i.e., clocks are toggling, always)
14	RW	0b	Core	**EU_GAunit Clock Gating Disable (cg3ddiseu_ga):** EU_GAunit Clock Gating Disable Control:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
13	RW	0b	Core	**EUunit Clock Gating Disable (cg3ddiseu):** EUunit Clock Gating Disable Control:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
12	RW	0b	Core	**EMunit Clock Gating Disable (cg3ddisem):** EMunit Clock Gating Disable Control:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always) This bit must be 1.
11	RW	0b	Core	**DTunit Clock Gating Disable (cg3ddisdt):** DTunit Clock Gating Disable Control:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
10	RW	0b	Core	**DMunit Clock Gating Disable (cg3ddisdm):** DMunit Clock Gating Disable Control:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
9	RW	0b	Core	**DGunit Clock Gating Disable (cg3ddisdg):** DGunit Clock Gating Disable Control:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always) {W/A}]: This bit must be 1.
8	RW	0b	Core	**DAPunit Clock Gating Disable (cg3ddisdap):** DAPunit Clock Gating Disable Control:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
7	RW	0b	Core	**CSunit Clock Gating Disable (cg3ddiscs):** CSunit Clock Gating Disable Control:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
6	RW	0b	Core	**CLunit Clock Gating Disable (cg3ddiscl):** CLunit Clock Gating Disable Control:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating

Bits	Access	Default Value	RST/PWR	Description
				Disabled. (i.e., clocks are toggling, always)
5	RW	1b	Core	**BLBunit Clock Gating Disable (cg3ddisblb):** BLBunit Clock Gating Disable Control:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
4	RW	0b	Core	**BFunit Clock Gating Disable (cg3ddisbf):** BFunit Clock Gating Disable Control:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
3	RW	0b	Core	**BDunit Clock Gating Disable (cg3ddisbd):** BDunit Clock Gating Disable Control:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
2	RW	0b	Core	**BCSunit Clock Gating Disable (cg3ddisbcs):** BCSunit Clock Gating Disable Control:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
1	RW	0b	Core	**AVSunit Clock Gating Disable (cg3ddisavs):** AVSunit Clock Gating Disable Control:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
0	RW	0b	Core	**AVDunit Clock Gating Disable (cg3ddisavd):** AVDunit Clock Gating Disable Control:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)

1.4.2 UCGCTL2 - Unit Level Clock Gating Control 2

B/D/F/Type: 0/2/0/MMADR_GCPunit_Config

Address Offset: 9404-9407h

Default Value: 00000000h

Access: RW

Size: 32 bits

Unit Level Clock Gating Control Registers.

IVB:GT2:A0: 0x9404 Bit 22 must be high (TDLunit clock gating)

IVB: 0x9404 Bit 13 must be high (RCZunit clock-gating)

Bits	Access	Default Value	RST/PWR	Description
31	RW	0b	Core	**VFunit Clock Gating Disable (cg3ddisvf):** VFunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
30	RW	0b	Core	**VDSunit Clock Gating Disable (cg3ddisvds):** VDSunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
29	RW	0b	Core	**VDIunit Clock Gating Disable (cg3ddisvdi):** VDIunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
28	RW	0b	Core	**VCSunit Clock Gating Disable (cg3ddisvcs):** VCSunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
27	RW	0b	Core	**DTOunit Clock Gating Disable (cg3ddisdto):** DTOunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
26	RW	0b	Core	**VCPunit Clock Gating Disable (cg3ddisvcp):** VCPunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
25	RW	0b	Core	**VCDunit Clock Gating Disable (cg3ddisvcd):** VCDunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)

Bits	Access	Default Value	RST/PWR	Description
24	RW	0b	Core	**URBunit Clock Gating Disable (cg3ddisurb):** URBunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
23	RW	0b	Core	**TSunit Clock Gating Disable (cg3ddists):** TSunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
22	RW	0b	Core	**TDunit Clock Gating Disable (cg3ddistd):** TDunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
21	RW	0b	Core	**SVTSunit Clock Gating Disable (cg3ddissvts):** SVTSunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
20	RW	0b	Core	**SVSMunit Clock Gating Disable (cg3ddissvsm):** SVSMunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
19	RW	0b	Core	**SVGunit Clock Gating Disable (cg3ddissvg):** SVGunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
18	RW	0b	Core	**SOunit Clock Gating Disable (cg3ddisso):** SOunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)

Bits	Access	Default Value	RST/PWR	Description
17	RW	0b	Core	**SIunit Clock Gating Disable (cg3ddissi):** SIunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
16	RW	0b	Core	**SFunit Clock Gating Disable (cg3ddissf):** SFunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
15	RW	0b	Core	**SECunit Clock Gating Disable (cg3ddissec):** SECunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
14	RW	0b	Core	**SCunit Clock Gating Disable (cg3ddissc):** SCunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
13	RW	0b	Core	**RCZunit Clock Gating Disable (cg3ddisrcz):** RCZunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
12	RW	0b	Core	**RCPBunit Clock Gating Disable (cg3ddisrcpb):** RCPBunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
11	RW	0b	Core	**RCCunit Clock Gating Disable (cg3ddisrcc):** RCCunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)

Bits	Access	Default Value	RST/PWR	Description
10	RW	0b	Core	**QCunit Clock Gating Disable (cg3ddisqc):** QCunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
9	RW	0b	Core	**PSDunit Clock Gating Disable (cg3ddispsd):** PSDunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
8	RW	0b	Core	**PLunit Clock Gating Disable (cg3ddispl):** PLunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
7	RW	0b	Core	**MTunit Clock Gating Disable (cg3ddismt):** MTunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
6	RW	0b	Core	**MPCunit Clock Gating Disable (cg3ddismpc):** MPCunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
5	RW	0b	Core	**MLC Tag Logic and Tag / State / LRU Arrays Clock Gating Disable (cg3ddismlctag):** MLC Tag Logic and Tag / State / LRU Arrays Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
4	RW	0b	Core	**MLC ECC and Error Detection / Correction Logic Clock Gating Disable (cg3ddismlcecc):** MLC ECC and Error Detection / Correction Logic Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)

Bits	Access	Default Value	RST/PWR	Description
				1: Clock Gating Disabled. (i.e., clocks are toggling, always)
3	RW	0b	Core	**MLC Data Array Clock Gating Disable (cg3ddismlcdbank):** MLC Data Array Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
2	RW	0b	Core	**MLC Data Pipeline and Scheduler Logic Clock Gating Disable (cg3ddismlcdata):** MLC Data Pipeline and Scheduler Logic Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
1	RW	0b	Core	**MAunit Clock Gating Disable (cg3ddisma):** MAunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
0	RW	0b	Core	**IZunit Clock Gating Disable (cg3ddisiz):** IZunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)

1.4.3 UCGCTL3 - Unit Level Clock Gating Control 3

B/D/F/Type: 0/2/0/MMADR_GCPunit_Config

Address Offset: 9408-940Bh

Default Value: 04000000h

Access: RW

Size: 32 bits

Unit Level Clock Gating Control Registers.

Bits	Access	Default Value	RST/PWR	Description
31	RW	0b	Core	**VXCunit Clock Gating Disable (cg3ddisvxc):** VXCunits' Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
30	RW	0b	Core	**SVRRunit Clock Gating Disable (cg3ddissvrr):** SVRRunits' Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
29	RW	0b	Core	**VCRunit Clock Gating Disable (cg3ddisvcr):** VCRunits' Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
28	RW	0b	Core	**EDTunit Clock Gating Disable (cg3ddisedt):** EDTunits' Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
27	RW	0b	Core	**VCIunit Clock Gating Disable (cg3ddisvci):** VCIunits' Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
26	RW	1b	Core	**CCRunit Clock Gating Disable (cg3ddisccr):**

Bits	Access	Default Value	RST/PWR	Description
				CCRunits' Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
25	RW	0b	Core	**MLCunit Clock Gating Disable (cg3ddismlc):** MLCunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
24	RW	0b	Core	**CTCunit Clock Gating Disable (cg3ddisctc):** CTCunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
23	RW	0b	Core	**QRCunit Clock Gating Disable (cg3ddisqrc):** QRCunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
22	RW	0b	Core	**MSPBISTunit Clock Gating Disable (cg3ddismspbist):** MSPBISTunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
21	RW	0b	Core	**BSPunit Clock Gating Disable (cg3ddisbsp):** BSPunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
20	RW	0b	Core	**OACSunit Clock Gating Disable (cg3ddisoacs):** OACSunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
19	RW	0b	Core	**OACRMunit Clock Gating Disable (cg3ddisoacrm):**

Bits	Access	Default Value	RST/PWR	Description
				OACRMunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
18	RW	0b	Core	**OACRROWunit Clock Gating Disable (cg3ddisoacrrow):** OACRROWunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
17	RW	0b	Core	**WMBE Clock Gating Disable (cg3ddiswmbe):** WMBEunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
16	RW	0b	Core	**WMFEunit Clock Gating Disable (cg3ddiswmfe):** WMFEunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
15	RW	0b	Core	**VSCunit Clock Gating Disable (cg3ddisvsc):** VSCunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
14	RW	0b	Core	
13	RW	0b	Core	**USBunit Clock Gating Disable (cg3ddisusb):** USBunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
12	RW	0b	Core	**STCunit Clock Gating Disable (cg3ddisstc):** STCunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
11	RW	0b	Core	**VS0unit Clock Gating Disable (cg3ddisvs0):**

Bits	Access	Default Value	RST/PWR	Description
				VS0unit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
10	RW	0b	Core	**VOPunit Clock Gating Disable (cg3ddisvop):** VOPunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
9	RW	0b	Core	**VMXunit Clock Gating Disable (cg3ddisvmx):** VMXunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
8	RW	0b	Core	**VMEunit Clock Gating Disable (cg3ddisvme):** VMEunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
7	RW	0b	Core	**VMDunit Clock Gating Disable (cg3ddisvmd):** VMDunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
6	RW	0b	Core	**VMCunit Clock Gating Disable (cg3ddisvmc):** VMCunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
5	RW	0b	Core	**VLFunit Clock Gating Disable (cg3ddisvlf):** VLFunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
4	RW	0b	Core	**VITunit Clock Gating Disable (cg3ddisvit):**

Bits	Access	Default Value	RST/PWR	Description
				VITunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
3	RW	0b	Core	**VIPunit Clock Gating Disable (cg3ddisvip):** VIPunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
2	RW	0b	Core	**VINunit Clock Gating Disable (cg3ddisvin):** VINunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
1	RW	0b	Core	**VFTunit Clock Gating Disable (cg3ddisvft):** VFTunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
0	RW	0b	Core	**VFEunit Clock Gating Disable (cg3ddisvfe):** VFEunit Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)

1.4.4 UCGCTL4 - Unit Level Clock Gating Control 4

B/D/F/Type: 0/2/0/MMADR_GCPunit_Config

Address Offset: 940C-940Fh

Default Value: 00000003h

Access: RO, RW

Size: 32 bits

Unit Level Clock Gating Control Registers.

Bits	Access	Default Value	RST/PWR	Description
31:26	RO	00000000000000000000000000000000b	Core	**Reserved (RSVD):** Reserved.
25	RW	0	Core	**L3 Bank 2x Clock Disable**: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always) For IVBA/B-steppings, this bit needs to be "1"
24:3	RO	0	Core	**Reserved (RSVD):** Reserved.
2	RW	0b	Core	**VID2 VINunit Clock Gating Disable (cg3ddisvin_vid2):** VID2 VINunits' Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
1:0	RW	11b	Core	**MSQCunit Clock Gating Disable (cg3ddismsqc):** MSQCunits' Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)

1.4.5 RCGCTL1 - RAM Clock Gating Control 1

B/D/F/Type: 0/2/0/MMADR_GCPunit_Config

Address Offset: 9410-9413h

Default Value: 00000180h

Access: RW, RO

Size: 32 bits

RAM Clock Gating Control Registers.

Bits	Access	Default Value	RST/PWR	Description
31	RW	0b	Core	**USBunit RAM Clock Gating Disable (ramcgdis_usb):** USBunit RAM Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to

Bits	Access	Default Value	RST/PWR	Description
				toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
30	RW	0b	Core	**VLFunit RAM Clock Gating Disable (ramcgdis_vlf):** VLFunit RAM Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
29	RW	0b	Core	**VDSunit RAM Clock Gating Disable (ramcgdis_vds):** VDSunit RAM Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
28	RW	0b	Core	**STCunit RAM Clock Gating Disable (ramcgdis_stc):** STCunit RAM Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
27	RW	0b	Core	**AVDunit RAM Clock Gating Disable (ramcgdis_avd):** AVDunit RAM Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
26	RW	0b	Core	**VMCunit RAM Clock Gating Disable (ramcgdis_vmc):** VMCunit RAM Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
25	RW	0b	Core	**QRCunit RAM Clock Gating Disable (ramcgdis_qrc):** QRCunit RAM Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
24	RW	0b	Core	**SCunit RAM Clock Gating Disable (ramcgdis_sc):** SCunit RAM Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to

Bits	Access	Default Value	RST/PWR	Description
				toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
23	RW	0b	Core	**WMBEunit RAM Clock Gating Disable (ramcgdis_wmbe):** WMBEunit RAM Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
22	RW	0b	Core	**VFunit RAM Clock Gating Disable (ramcgdis_vfm):** VFunit RAM Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
21	RW	0b	Core	**URBunit RAM Clock Gating Disable (ramcgdis_urb):** URBunit RAM Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
20	RW	0b	Core	**SVSMunit RAM Clock Gating Disable (ramcgdis_svsm):** SVSMunit RAM Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
19	RO	0b	Core	**Reserved (Rsvd3):** Reserved
18	RW	0b	Core	**RCZunit RAM Clock Gating Disable (ramcgdis_rcz):** RCZunit RAM Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
17	RW	0b	Core	**RCPBEunit RAM Clock Gating Disable (ramcgdis_rcpbe):** RCPBEunit RAM Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
16	RW	0b	Core	**RCCunit RAM Clock Gating Disable (ramcgdis_rcc):**

Bits	Access	Default Value	RST/PWR	Description
				RCCunit RAM Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
15	RW	0b	Core	**PSDunit RAM Clock Gating Disable (ramcgdis_psd):** PSDunit RAM Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
14	RW	0b	Core	**MTunit RAM Clock Gating Disable (ramcgdis_mt):** MTunit RAM Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
13	RO	0b	Core	**Reserved (Rsvd1):** Reserved
12	RW	0b	Core	**IZunit RAM Clock Gating Disable (ramcgdis_iz):** IZunit RAM Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
11	RW	0b	Core	**ISCunit RAM Clock Gating Disable (ramcgdis_isc):** ISCunit RAM Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
10	RW	0b	Core	**ICunit RAM Clock Gating Disable (ramcgdis_ic):** ICunit RAM Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
9	RW	0b	Core	**HIZunit RAM Clock Gating Disable (ramcgdis_hiz):** HIZunit RAM Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)

Bits	Access	Default Value	RST/PWR	Description
				1: Clock Gating Disabled. (i.e., clocks are toggling, always)
8	RW	1b	Core	**GAMunit RAM Clock Gating Disable (ramcgdis_gam):** GAMunit RAM Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always
7	RW	1b	Core	**GACunit RAM Clock Gating Disable (ramcgdis_gac):** GACunit RAM Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
6	RO	0b	Core	**Reserved (RSVD):** Reserved.
5	RW	0b	Core	**DMunit RAM Clock Gating Disable (ramcgdis_dm):** DMunit RAM Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
4	RW	0b	Core	**DAPunit RAM Clock Gating Disable (ramcgdis_dap):** DAPunit RAM Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
3	RW	0b	Core	**CSunit RAM Clock Gating Disable (ramcgdis_cs):** CSunit RAM Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
2	RW	0b	Core	**BLBunit RAM Clock Gating Disable (ramcgdis_blb):** BLBunit RAM Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
1	RW	0b	Core	**MPCunit RAM Clock Gating Disable (ramcgdis_mpc):** MPCunit RAM Clock Gating Disable Control:

Bits	Access	Default Value	RST/PWR	Description
				0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)
0	RW	0b	Core	**BFunit RAM Clock Gating Disable (ramcgdis_bf):** BFunit RAM Clock Gating Disable Control: 0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) 1: Clock Gating Disabled. (i.e., clocks are toggling, always)

1.4.6 RCGCTL2 - RAM Clock Gating Control 2

B/D/F/Type: 0/2/0/MMADR_GCPunit_Config

Address Offset: 9414-9417h

Default Value: 00000000h

Access: RW, RO

Size: 32 bits

RAM Clock Gating Control Registers.

Bits	Access	Default Value	RST/PWR	Description
31:27	RO	00000b	Core	**Reserved (RSVD):** Reserved.
26	RW	0b	Core	**VMXunit RAM Clock GatingDisable (ramcgdis_vmx):** VMXunit RAM Clock Gating Disable Control:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
25	RW	0b	Core	**MSunit RAM Clock Gating Disable in EU2 ROW3 (ramcgdis_ms_eu2_row3):** MSunit RAM Clock Gating Disable Control in EU2 ROW3:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
24	RW	0b	Core	**MSunit RAM Clock Gating Disable in EU1 ROW3 (ramcgdis_ms_eu1_row3):** MSunit RAM Clock Gating Disable Control in EU1 ROW3:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
23	RW	0b	Core	**MSunit RAM Clock Gating Disable in EU0 ROW3 (ramcgdis_ms_eu0_row3):** MSunit RAM Clock Gating Disable Control in EU0 ROW3:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)

Bits	Access	Default Value	RST/PWR	Description
22	RW	0b	Core	**MSunit RAM Clock Gating Disable in EU2 ROW2 (ramcgdis_ms_eu2_row2):** MSunit RAM Clock Gating Disable Control in EU2 ROW2:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
21	RW	0b	Core	**MSunit RAM Clock Gating Disable in EU1 ROW2 (ramcgdis_ms_eu1_row2):** MSunit RAM Clock Gating Disable Control in EU1 ROW2:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
20	RW	0b	Core	**MSunit RAM Clock Gating Disable in EU0 ROW2 (ramcgdis_ms_eu0_row2):** MSunit RAM Clock Gating Disable Control in EU0 ROW2:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
19	RW	0b	Core	**MSunit RAM Clock Gating Disable in EU2 ROW1 (ramcgdis_ms_eu2_row1):** MSunit RAM Clock Gating Disable Control in EU2 ROW1:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
18	RW	0b	Core	**MSunit RAM Clock Gating Disable in EU1 ROW1 (ramcgdis_ms_eu1_row1):** MSunit RAM Clock Gating Disable Control in EU1 ROW1:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
17	RW	0b	Core	**MSunit RAM Clock Gating Disable in EU0 ROW1 (ramcgdis_ms_eu0_row1):** MSunit RAM Clock Gating Disable Control in EU0 ROW1:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
16	RW	0b	Core	**MSunit RAM Clock Gating Disable in EU2 ROW0 (ramcgdis_ms_eu2_row0):** MSunit RAM Clock Gating Disable Control in EU2 ROW0:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
15	RW	0b	Core	**MSunit RAM Clock Gating Disable in EU1 ROW0 (ramcgdis_ms_eu1_row0):** MSunit RAM Clock Gating Disable Control in EU1 ROW0:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
14	RW	0b	Core	**MSunit RAM Clock Gating Disable in EU0 ROW0 (ramcgdis_ms_eu0_row0):** MSunit RAM Clock Gating Disable Control in EU0 ROW0:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
13	RW	0b	Core	**GAunit RAM Clock Gating Disable in EU2 ROW3 (ramcgdis_ga_eu2_row3):** GAunit RAM Clock Gating Disable Control in EU2 ROW3:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for

Bits	Access	Default Value	RST/PWR	Description
				functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
12	RW	0b	Core	**GAunit RAM Clock Gating Disable in EU1 ROW3 (ramcgdis_ga_eu1_row3):** GAunit RAM Clock Gating Disable Control in EU1 ROW3:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
11	RW	0b	Core	**GAunit RAM Clock Gating Disable in EU0 ROW3 (ramcgdis_ga_eu0_row3):** GAunit RAM Clock Gating Disable Control in EU0 ROW3:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
10	RW	0b	Core	**GAunit RAM Clock Gating Disable in EU2 ROW2 (ramcgdis_ga_eu2_row2):** GAunit RAM Clock Gating Disable Control in EU2 ROW2:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
9	RW	0b	Core	**GAunit RAM Clock Gating Disable in EU1 ROW2 (ramcgdis_ga_eu1_row2):** GAunit RAM Clock Gating Disable Control in EU1 ROW2:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
8	RW	0b	Core	**GAunit RAM Clock Gating Disable in EU0 ROW2 (ramcgdis_ga_eu0_row2):** GAunit RAM Clock Gating Disable Control in EU0 ROW2:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
7	RW	0b	Core	**GAunit RAM Clock Gating Disable in EU2 ROW1 (ramcgdis_ga_eu2_row1):** GAunit RAM Clock Gating Disable Control in EU2 ROW1:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
6	RW	0b	Core	**GAunit RAM Clock Gating Disable in EU1 ROW1 (ramcgdis_ga_eu1_row1):** GAunit RAM Clock Gating Disable Control in EU1 ROW1:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
5	RW	0b	Core	**GAunit RAM Clock Gating Disable in EU0 ROW1 (ramcgdis_ga_eu0_row1):** GAunit RAM Clock Gating Disable Control in EU0 ROW1:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
4	RW	0b	Core	**GAunit RAM Clock Gating Disable in EU2 ROW0 (ramcgdis_ga_eu2_row0):** GAunit RAM Clock Gating Disable Control in EU2 ROW0:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
3	RW	0b	Core	**GAunit RAM Clock Gating Disable in EU1 ROW0 (ramcgdis_ga_eu1_row0):**

Bits	Access	Default Value	RST/PWR	Description
				GAunit RAM Clock Gating Disable Control in EU1 ROW0:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
2	RW	0b	Core	**GAunit RAM Clock Gating Disable in EU0 ROW0 (ramcgdis_ga_eu0_row0):** GAunit RAM Clock Gating Disable Control in EU0 ROW0:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
1	RW	0b	Core	**GSunit RAM Clock Gating Disable (ramcgdis_gs):** GSunit RAM Clock Gating Disable Control:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)
0	RW	0b	Core	**CTCunit RAM Clock Gating Disable (ramcgdis_ctc):** CTCunit RAM Clock Gating Disable Control:0: Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)1: Clock Gating Disabled. (i.e., clocks are toggling, always)

1.4.7 IFDIMCTL - Integrated Power Supply Frequency Domain Impedance Meter Controls

B/D/F/Type: 0/2/0/MMADR_GCPunit_Config

Address Offset: 9418-941Bh

Default Value: 00000000h

Access: RO, RW

Size: 32 bits

Integrated Power Supply Frequency Domain Impedance Meter (IFDIM) Controls:

Bits	Access	Default Value	RST/PWR	Description
31	RO	0b	Core	**Reserved (RSVD):** Reserved.
30:4	RW	00000000000000000000000000b	Core	**IFDIM Modulation Counter Delay Value (IFDIMCNTVAL):** The IFDIM Modulation Counter Delay Value. Note that this 27-bit count value is not exact. The counter sits in csclk domain, and the modulation gating/un-gating is done on clock beat alignments.
3	RW	0b	Core	**CSCLK Moudlation Enable (CSMODEN):** csclk Modulation Enable: 1 - Enable csclk domain clock modulation. 0 - Disable csclk domain clock modulation; csclk domain

Bits	Access	Default Value	RST/PWR	Description
				is gated.
2	RW	0b	Core	**MLCCLK Modulation Enable (MLCMODEN):** mlcclk Modulation Enable: 1 - Enable mlcclk domain clock modulation. 0 - Disable mlcclk domain clock modulation; mlcclk domain is gated.
1	RW	0b	Core	**CRCLK Modulation Enable (CRMODEN):** crclk Modulation Enable: 1 - Enable crclk domain clock modulation. 0 - Disable crclk domain clock modulation; crclk domain is gated.
0	RW	0b	Core	**Enable IFDIM (IFDIMEN):** Enable IFDIM Operation: 1 - IFDIM operation enabled; Selected clocks (see bits #1, #2, #3) are modulated. 0 - IFDIM operation disabled.

1.4.8 GDRST - Graphics Device Reset Control

B/D/F/Type: 0/2/0/MMADR_GCPunit_Config

Address Offset: 941C-941Fh

Default Value: 00000000h

Access: RWHC, RO

Size: 32 bits

Graphics Device Reset Control Registers:

Bits	Access	Default Value	RST/PWR	Description
31:4	RO	0000000h	Core	**Reserved (RSVD):** Reserved
3	RWHC	0b	Core	**Initiate Graphics Blitter Soft Reset (INIT_BLIT_SR):** Graphics Blitter Soft-Reset Control: 1: Initiate a graphics blitter domain reset. - Cleared by CP once the reset is complete. 0: N/A - Once set, clearing this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.
2	RWHC	0b	Core	**Initiate Graphics Media Soft Reset (INIT_MEDIA_SR):**

Bits	Access	Default Value	RST/PWR	Description
				Graphics Media Soft-Reset Control: 1: Initiate a graphics media domain reset. - Cleared by CP once the reset is complete. 0: N/A - Once set, clearing this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.
1	RWHC	0b	Core	**Initiate Graphics Render Soft Reset (INIT_RENDER_SR):** Graphics Render Soft-Reset Control: 1: Initiate a graphics render domain reset. - Cleared by CP once the reset is complete. 0: N/A - Once set, clearing this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.
0	RWHC	0b	Core	**Initiate Graphics Full Soft Reset (INIT_GFXFULL_SR):** Graphics Full Soft-Reset Control: 1: Initiate a full graphics reset (i.e., graphics render, media, and blitter reset). - Cleared by CP once the reset is complete. 0: N/A - Once set, clearing this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.

1.4.9 RSTCTL - Misc. Reset Control Register

B/D/F/Type: 0/2/0/MMADR_GCPunit_Config

Address Offset: 9420-9423h

Default Value: 00000000h

Access: RW, RO

Size: 32 bits

Miscellaneous reset control registers.

Bits	Access	Default Value	RST/PWR	Description
31:4	RO	0000000h	Core	**Reserved (Rsvd.):** Reserved
3:2	RW	00b	Core	**Reset Staggering Period Control (RSTSTGRT):** Reset assertion staggering period between reset domains: "00" : no reset assertion staggering "01" : 16 cs clocks "10" : 32 cs clocks "11" : 64 cs clocks
1:0	RW	00b	Core	**Reset Residency Control (RSTRSDNCY):** Reset assertion residency period for FLR and soft-resets. "00" : 8 cs clocks "01" : 16 cs clocks "10" : 32 cs clocks "11" : 64 cs clocks

1.4.10 MISCCPCTL - Misc. Clocking/Reset Control Register

B/D/F/Type: 0/2/0/MMADR_GCPunit_Config

Address Offset: 9424-9427h

Default Value: 00000000h

Access: RW

Size: 32 bits

Miscellaneous Clocking/Reset Control Register:

Bits	Access	Default Value	RST/PWR	Description
31:2	RW	00000000000000000000000000000000b	Core	**Bonus (BONUS):** Reserved.
1	RW	0b	Core	**L1 Clock Ungate Enabling Control During Reset (L1UGTEN4RST):** Control to enable/disable L1 clock gating during soft resets and FLR reset processing. 1: Disable L1 clock gating during soft resets and FLR. 0: Enable L1 clock gating during soft resets and FLR (default op).
0	RW	0b	Core	**DOP Clock Gating Enable for Row and Media Clocks (DOPCGEN):** Controls the Enabling of the DOP-level Row and Media Clock Gating via PM event messages: 1: Clock gating is enabled. 0: Clock gating is disabled.

1.5 GCPunit Message Register Space

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
GT Function Level Reset Control Message	FLRCTLMSG	8100	8103	00000000h	RO, RWHC
Glock Gating Messages	CGMSG	8104	8107	00000000h	RO, RW
Reset Flow Control Messages	RSTFCTLMSG	8108	810B	00000000h	RO, RW

1.5.1 FLRCTLMSG - GT Function Level Reset Control Message

B/D/F/Type: 0/2/0/MMADR_GCPunit_Message

Address Offset: 8100-8103h

Default Value: 00000000h

Access: RO, RWHC

Size: 32 bits

GT FLR Control Register:

Bits	Access	Default Value	RST/PWR	Description
31:16	RO	0000h	Core	**Message Mask (MSGMSK):** Message Mask To write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1: 40004000h.
15:1	RO	000000000000000b	Core	**Reserved (RSVD):** Reserved.
0	RWHC	0b	Core	**Initiate GT Function Level Reset Message (INIT_FLR):** GT Function Level Reset (FLR) 1: Initiate GT FLR - This is a Non-Posted message to reset Render, Media, Blitter, and GTI-Device domains. This bit is cleared by the CPunit on completion of the reset.

1.5.2 CGMSG - Glock Gating Messages

B/D/F/Type: 0/2/0/MMADR_GCPunit_Message

Address Offset: 8104-8107h

Default Value: 00000000h

Access: RO, RW

Size: 32 bits

Clock Gating Messages Register:

Bits	Access	Default Value	RST/PWR	Description
31:16	RO	0000h	Core	**Message Mask (MSGMSK):** Message Mask To write to bits 15:0, the corresponding message mask bits must be written.

Bits	Access	Default Value	RST/PWR	Description
				For example, for bit 14 to be set, bit 30 needs to be 1: 40004000h.
15:2	RO	00000000000000b	Core	**Reserved (RSVD):** Reserved.
1	RW	0b	Core	**Media Clock Gating Control Message (MCGCTL):** Gate Media Clock Message: 0: Media Clock Un-gate Request (un-gates the crmclk clock). 1: Media Clock Gate Request (gates the crmclk clock).
0	RW	0b	Core	**Row Clock Gating Control Message (RCGCTL):** Gate Row Clocks Message : 0: Row Clock Un-gate Request (un-gates the csrowclk and crrowclk clocks). 1: Row Clock Gate Request (gates the csrowclk and crrowclk clocks).

1.5.3 RSTFCTLMSG - Reset Flow Control Messages

B/D/F/Type: 0/2/0/MMADR_GCPunit_Message

Address Offset: 8108-810Bh

Default Value: 00000000h

Access: RO, RW

Size: 32 bits

Soft-Reset and FLR Flow Control Message Registers

Bits	Access	Default Value	RST/PWR	Description
31:16	RO	0000h	Core	**Message Mask (MSGMAK):** Message Mask To write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1: 40004000
15:8	RO	00h	Core	**Reserved (RSVD):** Reserved.
7	RW	0b	Core	**Blitter Reset Flow Acknowledgement Messages (BLITRSTACK):** PM Acknowledgement Messages for Blitter reset: 1: PREP_RST_BLIT_ACK - Acknowledgement that graphics blitter is prepared for reset assertion. 0: DONE_BLIT_RST_ACK - Acknowledgement that graphics blitter reset is de-asserted

Bits	Access	Default Value	RST/PWR	Description
6	RW	0b	Core	**Media Reset Flow Acknowledgement Messages (MEDIARSTACK):** PM Acknowledgement Messages for Media reset: 1: PREP_RST_MEDIA_ACK - Acknowledgement that graphics media block is prepared for reset assertion. 0: DONE_MEDIA_RST_ACK - Acknowledgement that the graphics media reset is de-asserted
5	RW	0b	Core	**Render Reset Flow Acknowledgement Messages (RENDERRSTACK):** PM Acknowledgement Messages for Render reset: 1: PREP_RST_RENDER_ACK - Acknowledgement that the graphics render block is prepared for reset assertion. 0: DONE_RENDER_RST_ACK - Acknowledgement that the graphics render reset is de-asserted
4	RW	0b	Core	**GTI-Device Reset Flow Acknowledgement Messages (GTIDEVRSTACK):** PM Acknowledgement Messages for GTI-Device reset: 1: PREP_RST_GTIDEV_ACK - Acknowledgement that the GTI device is prepared for reset assertion. 0: DONE_GTIDEV_RST_ACK - Acknowledgement that the GTI device reset is de-asserted
3:2	RO	00b	Core	**Reserved (Rsvd.):** Reserved
1	RW	0b	Core	**Global Resource Arbitration Acknowledgement Messages (GRARBACK):** Global Resource Arbitration Acknowledgement Message from PM: 1: CP_ARB_REQ_ACK - Acknowledgement for CPunit's global resource arbitration request 0: CP_ARB_RELEASE_ACK - Acknowledgement to CPunit's release of global resources
0	RW	0b	Core	**CP Busy / Idle Status Acknowledgement Messages (CPBUSYSTATACK):** CP Busy / Idle Status Acknowledgement Message from PM: 0: CP_NOT_BUSY_ACK - Acknowledgement that the CPunit is idle. 1: CP_BUSY_ACK - Acknowledgement that the CPunit is busy.

Revision History

Revision Number	Description	Revision Date
1.0	First 2012 OpenSource edition	May 2012

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