Intel® OpenSource HD Graphics Programmer's Reference Manual (PRM)
Volume 3 Part 4: South Display Engine Registers
(Ivy Bridge)

For the 2012 Intel® Core™ Processor Family

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1. Introduction

This chapter contains the register descriptions for the display portion of a family of graphics devices.

These registers vary by devices within the family of devices, so special attention needs to be paid to which devices use which registers and register fields.

Different devices within the family may add, modify, or delete registers or register fields relative to another device in the same family based on the supported functions of that device.

This chapter applies to both Cougarpoint (CPT) and Pantherpoint (PPT) display. Unless specifically indicated, all references to Cougarpoint (CPT) will apply to both Cougarpoint (CPT) and Pantherpoint (PPT).

1.1 Display Mode Set Sequence

See the North Display Engine Registers document.

1.1.1 Simultaneous Display Capabilities on a Single Display Pipe/Transcoder

	Embedded DisplayPort (on CPU)	Integrated LVDS	HDMI/DVI	DisplayPort	CRT
Embedded DisplayPort (on CPU)	No (4)	No (7)	No (7)	No (7)	No (7)
Integrated LVDS		No (4)	No (2, 3, 8)	No (2, 8, 9)	Some (3, 8)
HDMI/DVI			No (6, 8,10)	No (6, 8, 9)	Some (5, 8)
DisplayPort				No (3, 6, 8, 9)	No (5, 8, 9)
CRT					No (4)

Shading: Rose = Does not work, White = Some cases work, Green = Works, Gray = Redundant (see other half of table)

2) No internal LVDS HDMI/DVI, or DisplayPort on same pipe/transcoder.

3) No SSC on CRT or HDMI/DVI. DisplayPort optionally has SSC.

4) Only 1 integrated LVDS, and 1 CRT on PCH. Only 1 embedded DisplayPort on CPU.

5) Only works if DisplayPort/HDMI/DVI is in 24bpp mode.

6) DisplayPort/HDMI/DVI ports are multiplexed on the same pins, only works if ports are on different pins.

7) Embedded DisplayPort is on the CPU; can not share the link.

8) Dithering, range correction, and gamma are done in the CPU; the display with lower bpp can truncate or the display with higher bpp can lose bits. One of the displays dictates range and gamma.

9) No DisplayPort allowed with other port on the same pipe/transcoder.

10) No HDMI allowed with another HDMI on the same transcoder.

1.1.2 Terminology

Description	Software Use	Should be implemented as
Read/Write, R/W	This bit can be read or written.	
Reserved	Don't assume a value for these bits. Writes have no effect.	Writes are ignored. Reads return zero.
Reserved: must be zero, MBZ	Software must always write a zero to these bits. This allows new features to be added using these bits that will be disabled when using old software and as the default case.	Writes are ignored. Reads return zero. Maybe be connected as Read/Write in future projects.
Reserved: PBC, software must preserve contents	Software must write the original value back to this bit. This allows new features to be added using these bits.	
Read Only	This bit is read only. The read value is determined by hardware. Writes to this bit have no effect.	According to each specific bit. The bit value is determined by hardware and not affected by register writes to the actual bit.
Read/Clear, Read/Write Clear	This bit can be read. Writes to it with a one cause the bit to clear.	Hardware events cause the bit to be set and the bit will be cleared on a write operation where the corresponding bit has a one for a value.
Double Buffered	Write when desired. Read gives the unbuffered value (written value) unless specified otherwise. Written values will update to take effect after a certain point. Some have a specific arming sequence where a write to another register is required before the update can take place. This is used to ensure atomic updates of several registers.	Two stages of registers used. First stage is written into and used for readback (unless specified otherwise). First stage value is transferred into second stage at the update point. Second stage value is used to control hardware. Arm/disarm flag for specific arming sequences.

2. South Display Engine Shared Functions

2.1 South Display Engine Interrupts

2.1.1 South Display Engine Interrupt Bit Definition

South Display Engine Interrupt Bit Definition	
Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Size (in bits):	32

South Display Engine (SDE) interrupt bits come from events within the south display engine.
The SDE_IIR bits are ORed together to generate the South/PCH Display Interrupt Event which will appear in the North Display Engine Interrupt Control Registers.
The South Display Engine Interrupt Control Registers all share the same bit definitions from this table.

Programming Notes

Only the rising edge of the PCH Display interrupt will cause the North Display IIR (DEIIR) PCH Display Interrupt event bit to be set, so all PCH Display Interrupts, including back to back interrupts, must be cleared in the SDEIIR before a new PCH Display Interrupt can cause the DEIIR to be set.

DWord	Bit	Description
0	31	**Audio Power State change Port D** This is an active high pulse when there is a power state change for audio for port D.
	30	**Audio Power State change Port C** This is an active high pulse when there is a power state change for audio for port C.
	29	**Audio Power State change Port B** This is an active high pulse when there is a power state change for audio for port B.
	28	**Reserved**
	27	**AUX Channel D** This is an active high pulse on the AUX D done event
	26	**AUX Channel C** This is an active high pulse on the AUX C done event
	25	**AUX Channel B** This is an active high pulse on the AUX B done event
	24	**Reserved**
	23	**DisplayPort/HDMI/DVI D Hotplug** The ISR is an active high level representing the Digital Port D hotplug line when the Digital Port D hotplug detect input is enabled. The unmasked IIR is set on either a short or long pulse detection status in the Digital Port Hot Plug Control Register.
	22	**DisplayPort/HDMI/DVI C Hotplug** The ISR is an active high level representing the Digital Port C hotplug line when the Digital Port C hotplug detect input is enabled.

South Display Engine Interrupt Bit Definition		
		The unmasked IIR is set on either a short or long pulse detection status in the Digital Port Hot Plug Control Register.
	21	**DisplayPort/HDMI/DVI B Hotplug** The ISR is an active high level representing the Digital Port B hotplug line when the Digital Port B hotplug detect input is enabled. The unmasked IIR is set on either a short or long pulse detection status in the Digital Port Hot Plug Control Register.
	20	**Reserved**
	19	**CRT Hotplug** The ISR is an active high level representing the ORed together blue and green channel detection status as of the last detection cycle. The unmasked IIR is set on the rising or falling edges of the blue or green channel detection status in the Analog Port CRT DAC Control Register.
	17	**Gmbus** This is an active high pulse when any of the events unmasked events in GMBUS4 Interrupt Mask register occur.
	16	**South Error Interrupts Combined** This is an active high level while any of the South Error Interrupt bits are set.
	15:11	**Reserved**
	9	**Audio CP Change Transcoder C** This is an active high pulse when there is a change in the protection request from audio azalia verb programming for transcoder C.
	8	**FDI RX Interrupts Combined C** This is an active high level while any of the FDI_RX_ISR bits are set for transcoder C
	7	**Reserved**
	5	**Audio CP Change Transcoder B** This is an active high pulse when there is a change in the protection request from audio azalia verb programming for transcoder B.
	4	**FDI RX Interrupts Combined B** This is an active high level while any of the FDI_RX_ISR bits are set for transcoder B
	3	**Reserved**
	1	**Audio CP Change Transcoder A** This is an active high pulse when there is a change in the protection request from audio azalia verb programming for transcoder A.
	0	**FDI RX Interrupts Combined A** This is an active high level while any of the FDI_RX_ISR bits are set for transcoder A

2.1.2 ISR — Interrupt Status

ISR		
Register Space:		MMIO: 0/2/0
Default Value:		0x00000000
Access:		RO
Size (in bits):		32
Address:	C4000h-C4003h	
Name:	South DE Interrupt Status	
ShortName:	SDE_ISR	

See the interrupt bit definition table to find the source event for each interrupt bit.

DWord	Bit	Description
0	31:0	**Interrupt Status Bits** This field contains the non-persistent values of all interrupt status bits. The IMR register selects which of these interrupt conditions are reported in the persistent IIR.

Value	Name	Description
0b	Condition Doesn't exist	Interrupt Condition currently does not exist
1b	Condition Exists	Interrupt Condition currently exists

Programming Notes
Some inputs to this register are short pulses; therefore software should not expect to use this register to sample these conditions.

2.1.3 IMR — Interrupt Mask

IMR		
Register Space:		MMIO: 0/2/0
Default Value:		0x00000000
Access:		R/W
Size (in bits):		32
Address:	C4004h-C4007h	
Name:	South DE Interrupt Mask	
ShortName:	SDE_IMR	

See the interrupt bit definition table to find the source event for each interrupt bit.

DWord	Bit	Description
0	31:0	**Interrupt Mask Bits** This field contains a bit mask which selects which interrupt bits from the ISR are reported in the IIR.

Value	Name	Description
0b	Not Masked	Not Masked – will be reported in the IIR
1b	Masked	Masked – will not be reported in the IIR

2.1.4 IIR — Interrupt Identity

IIR		
Register Space:		MMIO: 0/2/0
Default Value:		0x00000000
Access:		R/WC
Size (in bits):		32
Address:	C4008h-C400Bh	
Name:	South DE Interrupt Identity	
ShortName:	SDE_IIR	

See the interrupt bit definition table to find the source event for each interrupt bit.

DWord	Bit	Description
0	31:0	**Interrupt Identity Bits** This field holds the persistent values of the interrupt bits from the ISR which are unmasked by the IMR. If enabled by the IER, bits set in this register will generate a PCH display interrupt. Bits set in this register will remain set (persist) until the interrupt condition is cleared by writing a '1' to the appropriate bits. For each bit, the IIR can store a second pending interrupt if two or more of the same interrupt conditions occur before the first condition is cleared, then upon clearing the first interrupt, the IIR bit and PCH display interrupt will momentarily go low, then return high to indicate there is another interrupt pending.

Value	Name	Description
0b	Condition Not Detected	Interrupt Condition Not Detected
1b	Condition Detected	Interrupt Condition Detected (may or may not have generated a PCH display interrupt)

Programming Notes
Only the rising edge of the PCH Display interrupt will cause the North Display IIR (DEIIR) PCH Display Interrupt event bit to be set, so all PCH Display Interrupts, including back to back interrupts, must be cleared here before a new PCH Display Interrupt can cause the DEIIR to be set.

2.1.5 IER — Interrupt Enable

IER		
Register Space:		MMIO: 0/2/0
Default Value:		0x00000000
Access:		R/W
Size (in bits):		32
Address:	C400Ch-C400Fh	
Name:	South DE Interrupt Enable	
ShortName:	SDE_IER	

See the interrupt bit definition table to find the source event for each interrupt bit.

DWord	Bit	Description
0	31:0	**Interrupt Enable Bits** The bits in this register enable a PCH display interrupt to be generated whenever the corresponding bit in the IIR becomes set. A disabled interrupt will still appear in the IIR register to allow polling of interrupt sources.

Value	Name	Description
0b	Disable	Disable
1b	Enable	Enable

2.1.6 SHOTPLUG_CTL — South Hot Plug Control

SHOTPLUG_CTL		
Register Space:		MMIO: 0/2/0
Default Value:		0x00000000
Access:		R/W
Size (in bits):		32
Address:	C4030h-C4033h	
Name:	South Hot Plug control	
ShortName:	SHOTPLUG_CTL	

DWord	Bit	Description
0	31:21	**Reserved**
	20	**DP D HPD Input Enable** Controls the state of the HPD buffer for the digital port D. The buffer state is independent of whether the port is enabled or not.

Value	Name	Description
0b	Disable	Buffer disabled
1b	Enable	Buffer enabled. Hot plugs bit reflect the electrical state of the HPD pin

	19:18	**DP D HPD Short Pulse Duration** These bits define the duration of the pulse defined as a short pulse for the digital port D.

Value	Name	Description

SHOTPLUG_CTL

00b	2ms	2mS
01b	4.5ms	4.5mS
10b	6ms	6mS
11b	100ms	100mS

17:16 **DP D HPD Status**
This reflects hot plug detect status on the digital port D.
Write a one to these bits to clear the status.
These bits are used for either monitor hotplug/unplug or for notification of a sink event.
When either a long or short pulse is detected, one of these bits will set.
These bits are ORed together to go to the main ISR hotplug register bit.

Value	Name	Description
00b	No Detect **[Default]**	Digital port hot plug event not detected
X1b	Short Detect	Digital port short pulse hot plug event detected
1Xb	Long Detect	Digital port long pulse hot plug event detected

15:13 **Reserved**

12 **DP C HPD Input Enable**
Controls the state of the HPD buffer for the digital port C. The buffer state is independent of whether the port is enabled or not.

Value	Name	Description
0b	Disable	Buffer disabled
1b	Enable	Buffer enabled. Hot plugs bit reflect the electrical state of the HPD pin

11:10 **DP C HPD Short Pulse Duration**
These bits define the duration of the pulse defined as a short pulse for the digital port C.

Value	Name	Description
00b	2ms	2mS
01b	4.5ms	4.5mS
10b	6ms	6mS
11b	100ms	100mS

9:8 **DP C HPD Status**
This reflects hot plug detect status on the digital port C.
Write a one to these bits to clear the status.
These bits are used for either monitor hotplug/unplug or for notification of a sink event.
When either a long or short pulse is detected, one of these bits will set.
These bits are ORed together to go to the main ISR hotplug register bit.

Value	Name	Description
00b	No Detect **[Default]**	Digital port hot plug event not detected
X1b	Short Detect	Digital port short pulse hot plug event detected
1Xb	Long Detect	Digital port long pulse hot plug event detected

7:5 **Reserved**

4 **DP B HPD Input Enable**
Controls the state of the HPD buffer for the digital port B. The buffer state is independent of whether the port is enabled or not.

Value	Name	Description
0b	Disable	Buffer disabled
1b	Enable	Buffer enabled. Hot plugs bit reflect the electrical state of the HPD pin

3:2 **DP B HPD Short Pulse Duration**
These bits define the duration of the pulse defined as a short pulse for the digital port B.

Value	Name	Description

SHOTPLUG_CTL				
		00b	2ms	2mS
		01b	4.5ms	4.5mS
		10b	6ms	6mS
		11b	100ms	100mS
	1:0	**DP B HPD Status** This reflects hot plug detect status on the digital port B. Write a one to these bits to clear the status. These bits are used for either monitor hotplug/unplug or for notification of a sink event. When either a long or short pulse is detected, one of these bits will set. These bits are ORed together to go to the main ISR hotplug register bit.		
		Value	**Name**	**Description**
		00b	No Detect **[Default]**	Digital port hot plug event not detected
		X1b	Short Detect	Digital port short pulse hot plug event detected
		1Xb	Long Detect	Digital port long pulse hot plug event detected

2.1.7 SERR_INT—South Error Interrupts

SERR_INT		
Register Space:		MMIO: 0/2/0
Default Value:		0x00000000
Access:		R/WC
Size (in bits):		32
Address:	C4040h-C4043h	
Name:	South Error Interrupts	
ShortName:	SERR_INT	

These are sticky bits, cleared by writing 1 to them.
All the South Error Interrupt bits are ORed together to go to the South Display Engine ISR Error Interrupts Combined bit.

DWord	Bit	Description
0	31	**South Poison Status** This bit is set upon receiving the poison message.
		Value / **Name** / **Description** 0b / Not Detected / Event not detected 1b / Detected / Event detected
	30:7	**Reserved**
	6	**Transcoder FIFO Underrun C** This bit is set when the transcoder FIFO underrun signal is high.
		Value / **Name** / **Description** 0b / Not Detected / Event not detected 1b / Detected / Event detected
	5:4	**Reserved**
	3	**Transcoder FIFO Underrun B** This bit is set when the transcoder FIFO underrun signal is high.

SERR_INT				
		Value	**Name**	**Description**
		0b	Not Detected	Event not detected
		1b	Detected	Event detected
	2:1	**Reserved**		
	0	**Transcoder FIFO Underrun A** This bit is set when the transcoder FIFO underrun signal is high.		
		Value	**Name**	**Description**
		0b	Not Detected	Event not detected
		1b	Detected	Event detected

2.2 GMBUS and GPIO

2.2.1 GPIO Pin Usage (By Functions)

GPIO pins allow the support of simple query and control functions such as DDC and I^2C interface protocols. GPIO pins exist in pairs (for the most part) and provide a mechanism to control external devices through a register programming interface. GPIO pins can be set to a level or the value of the pin can be read. This allows for a "bit banging" version of an I2C interface to be implemented. An additional function of using the GMBUS engine to run the I2C protocols is also allowed. Refer to the *Philips I2C-BUS SPECIFICATION version 2.1* for a description of the I2C bus and protocol.

Some of the GPIO pins will be muxed with other functions and are only available when the other function is not being used. The following subsections describe the GPIO pin to register mapping. OEMs have the ability to remap these functions onto other pins as long as the hardware limitations are observed.

Port	Pin Use (Name)	GMBUS Use		Internal Pullup	I^2C	Device	Description
5	HDMI/DPD CTLDATA	Yes	No	No (weak pulldown on reset)	Yes	All	DDC for HDMI connection via the integrated HDMI port D
	HDMI/DPD CTLCLK			No	Yes		
4							
3	HDMI/DPC CTLDATA	Yes	No	No (weak pulldown on reset)	Yes	All	DDC for HDMI connection via the integrated HDMI port C.
	HDMI/DPC CTLCLK			No	Yes		
2	LVDS DDC Data (DDCLDATA)	Yes	No	No	Yes	All	DDC for Digital Display connection via the integrated LVDS
	LVDS DDC Clock (DDCLCLK)				Yes		
1	I2C Data (LCLKCTRLB)	Yes	No	No	Yes	All	For control of SSC clock generator devices on motherboard. Support can be optionally I2C or

Port	Pin Use (Name)	GMBUS Use		Internal Pullup	I²C	Device	Description
							control level.
	I2C Clock (LCLKCTRLA)				Yes		
0	DAC DDC Data (DDCADATA)	Yes	No	No	Yes	All	DDC for Analog monitor (VGA) connection. This cannot be shared with other DDC or I2C pairs due to legacy monitor issues.
	DAC DDC Clock (DDCACLK)				Yes		

2.2.2 GPIO_CTL— GPIO Control

GPIO Control Register Format

Default Value: 0x00000808

DWord	Bit	Description
0	31:13	**Reserved** Format: MBZ
	12	**GPIO Data In** Default Value: Ub Undefined (read only depends on I/O pin) Access: RO This is the value that is sampled on the GPIO_Data pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset.
	11	**GPIO Data Value** Default Value: 1b One Access: R/W This is the value that should be place on the GPIO Data pin as an output. This value is only written into the register if GPIO DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Data DIRECTION VALUE contains a value that will configure the pin as an output. TThe hardware drives a default of '1' since the I2C interface defaults to a '1'(this mimics the I2C external pull-ups on the bus).
	10	**GPIO Data Mask** Access: WO This is a mask bit to determine whether the GPIO DATA VALUE bit should be written into the register. This value is not stored and when read returns 0.

Value	Name	Description
0b	No Write	Do NOT write GPIO Data Value bit
1b	Write	Write GPIO Data Value bit.

	9	**GPIO Data Direction Value** Access: R/W

GPIO Control Register Format

This is the value that should be used to define the output enable of the GPIO Data pin.
This value is only written into the register if GPIO Data DIRECTION MASK is also asserted.
The value that will appear on the pin is defined by what is in the register for the GPIO DATA VALUE bit.

Value	Name	Description
0b	Input	Pin is configured as an input
1b	Output	Pin is configured as an output

8 GPIO Data Direction Mask

Access:	WO

This is a mask bit to determine whether the GPIO DIRECTION VALUE bit should be written into the register.
This value is not stored and when read always returns 0.

Value	Name	Description
0b	No Write	Do NOT write GPIO Data Direction Value bit
1b	Write	Write GPIO Data Direction Value bit

7:5 Reserved

Format:	MBZ

4 GPIO Clock Data In

Default Value:	Ub Undefined (read only depends on I/O pin)
Access:	RO

This is the value that is sampled on the GPIO Clock pin as an input.
This input is synchronized to the Core Clock domain.
Because the default setting is this buffer is an input, this bit is undefined at reset.

3 GPIO Clock Data Value

Default Value:	1b One
Access:	R/W

This is the value that should be place on the GPIO Clk pin as an output.
This value is only written into the register if GPIO Clock DATA MASK is also asserted.
The value will appear on the pin if this data value is actually written to this register and the GPIO Clock DIRECTION VALUE contains a value that will configure the pin as an output.
The hardware drives a default of '1' since the I2C interface defaults to a '1' (this mimics the I2C external pull-ups on the bus).

2 GPIO Clock Data Mask

Access:	WO

This is a mask bit to determine whether the GPIO Clock DATA VALUE bit should be written into the register.
This value is not stored and when read always returns 0.

Value	Name	Description
0b	No Write	Do NOT write GPIO Clock Data Value bit
1b	Write	Write GPIO Clock Data Value bit

1 GPIO Clock Direction Value

Access:	R/W

This is the value that should be used to define the output enable of the GPIO Clock pin.
This value is only written into the register if GPIO Clock DIRECTION MASK is also asserted.
The value that will appear on the pin is defined by what is in the register for the GPIO Clock DATA VALUE bit.

Value	Name	Description

GPIO Control Register Format

		0b	Input	Pin is configured as an input and the output driver is set to tri-state
		1b	Output	Pin is configured as an output
	0	**GPIO Clock Direction Mask**		
		Access:		WO
		This is a mask bit to determine whether the GPIO Clock DIRECTION VALUE bit should be written into the register. This value is not stored and when read returns 0.		
		Value	**Name**	**Description**
		0b	No Update	Do NOT update the GPIO Clock Direction Value bit on a write
		1b	Update	Update the GPIO Clock Direction Value bit. on a write operation to this register

GPIO_CTL

Register Space:	MMIO: 0/2/0
Default Value:	0x00000808, 0x00000808, 0x00000808, 0x00000808, 0x00000808, 0x00000808
Access:	R/W
Size (in bits):	6x32

Address:	C5010h-C5027h
Name:	GPIO Control
ShortName:	GPIO_CTL_[0-5]

These registers define the control of sets of the “general purpose” I/O pins.
Each register controls a pair of pins that can be used for general purpose control, but most are designated for specific functions according to the requirements of the device and the system that the device is in.

Each pin of the two pin pair is designated as a clock or data for descriptive purposes.

See the table at the beginning of this section to determine which pins/registers are supported and their intended functions.
Board design variations are possible and would affect the usage of these pins.

The registers that control digital display (HDMI/DVI and DisplayPort) pins should only be utilized if the Port Detected bit in the related control register is set to 1.

DWord	Bit	Description	
0	31:0	**GPIOCTL 0**	
		Format:	GPIO Control Register Format
1	31:0	**GPIOCTL 1**	
		Format:	GPIO Control Register Format
2	31:0	**GPIOCTL 2**	
		Format:	GPIO Control Register Format
3	31:0	**GPIOCTL 3**	
		Format:	GPIO Control Register Format
4	31:0	**GPIOCTL 4**	
		Format:	GPIO Control Register Format
5	31:0	**GPIOCTL 5**	
		Format:	GPIO Control Register Format

2.2.3 GMBUS Controller Programming Interface

The GMBUS (Graphic Management Bus) can be used to indirectly access/control devices connected to a GMBUS bus as an alternate to bit-wise programming via software.

The GMBUS interface is I^2C compatible. The basic features are listed as follow:

1. Works as the master of a single master bus.
2. The bus clock frequency is selectable by software to be 50KHz, 100KHz, 400KHz , and 1MHz
3. The GMBUS controller can be attached to the selected GPIO pin pairs.
4. 7 or 10-Bit Slave Address and 8- or 16-bit index.
5. Hardware byte counter to track the data transmissions/reception
6. Timing source from core display clock.
7. There is a double buffered data register and a 9 bit counter to support 0 byte to 256 byte transfers.
8. The slave device can cause a stall by pulling down the clock line (Slave Stall), or delay the slave acknowledge response.
9. The master controller detects and reports time out conditions for a stall from a slave device or delayed or missing slave acknowledge.
10. Interrupt may optionally be generated.
11. The GMBUS is controlled by a set of memory mapped IO registers. Status is reported through the GMBUS status register.
12. The GMBUS controller does not directly support segment pointer addressing as defined by the Enhanced Display Data Channel standard. Segment pointer addressing for EDDC shall be supported as follows:
    a. Use bit bashing (manual GPIO programming) to complete segment pointer write over ther target I2C port **without terminating in a stop or wait cycle**.
    b. Terminate bit bashing phase with both I2C lines pulled high by tri-stating the data line before the clock line. Follow EDDC requirement for response received from slave device.
    c. Initiate GMBUS cycle as required to transfer EDID following normal procedure.

The byte counter register is a read/write register, and in receiving mode, is used to track the data bytes received. There is a status register to indicate the error condition, data buffer busy, time out, and data complete acknowledgement.

2.2.4 GMBUS0—GMBUS Clock/Port Select

GMBUS0		
Register Space:		MMIO: 0/2/0
Default Value:		0x00000000
Access:		R/W
Size (in bits):		32
Address:	C5100h-C5103h	
Name:	GMBUS0 Clock/Port Select	
ShortName:	GMBUS0	

The GMBUS0 register will set the clock rate of the serial bus and the device the controller is connected to.
This register should be set before the first data valid bit is set, because it will be read only at the very first data valid bit, and not read during the period of the transmission until stop is issued and next first data valid bit is set.

DWord	Bit	Description
0	31:12	**Reserved**
	10:8	**GMBUS Rate Select** These two bits select the rate that the GMBUS will run at. It also defines the AC timing parameters used. It should only be changed when between transfers when the GMBUS is idle.

Value	Name	Description
000b	100KHz **[Default]**	100 KHz
001b	50KHz	50 KHz
010b	400KHz	400 KHz
011b	1MHz	1 MHz
Others	Reserved	Reserved

	7:3	**Reserved**
		Format: MBZ
	2:0	**Pin Pair Select** This field selects a GMBUS pin pair for use in the GMBUS communication. Use the table above to determine which pin pairs are available for a particular device and the intended function of that pin pair. It is not a straight forward mapping of port numbers to pair select numbers.

Value	Name	Description
000b	None **[Default]**	None (disabled)
001b	LCTRCLK	LCTRCLKA, LCTRLCLKB
010b	Analog Mon	Dedicated Analog Monitor DDC Pins (DDC1DATA, DDC1CLK)
011b	LVDS	Integrated Digital Panel DDC Pins, LVDS
100b	Port C	Port C
101b	Port B	Port B
110b	Port D	Port D
111b	Reserved	Reserved

2.2.5 GMBUS1—GMBUS Command/Status

GMBUS1

Register Space:	MMIO: 0/2/0
Default Value:	0x00000000
Access:	R/W Protect
Size (in bits):	32

Address:	C5104h-C5107h
Name:	GMBUS1 Command/Status
ShortName:	GMBUS1

This register lets the software indicate to the GMBUS controller the slave device address, register index, and indicate when the data write is complete.
When the SW_CLR_INT bit is asserted, all writes to the GMBUS2, GMBUS3, and GMBUS4 registers are discarded. The GMBUS1 register writes to any other bit except the SW_CLR_INT are also lost.
Reads to these registers always work normally regardless of the state of the SW_CLR_INT bit.

DWord	Bit	Description
0	31	**Software Clear Interrupt** Access: R/W (SW_CLR_INT) This bit must be clear for normal operation. Setting the bit then clearing it acts as local reset to the GMBUS controller. This bit is commonly used by software to clear a BUS_ERROR when a slave device delivers a NACK. **Value / Name / Description** 0b / Clear HW_RDY / If this bit is written as a zero when its current state is a one, will clear the HW_RDY bit and allows register writes to be accepted to the GMBUS registers (Write Protect Off). This bit is cleared to zero when an event causes the HW_RDY bit transition to occur. 1b / Assert HW_RDY / Asserted by software after servicing the GMBUS interrupt. Setting this bit causes the INT status bit to be cleared. Setting (1) this bit also asserts the HW_RDY bit (until this bit is written with a 0). When this bit is set, no writes to GMBUS registers will cause the contents to change with the exception of this bit which can be written.
	30	**Software Ready** (SW_RDY) Data handshake bit used in conjunction with HW_RDY bit. **Value / Name / Description** 0b / De-Assert / De-asserted via the assertion event for HW_RDY bit 1b / SW Assert / When asserted by software, results in de-assertion of HW_RDY bit
	29	**Enable Timeout** (ENT) Enables timeout for slave response. When this bit is enabled and the slave device response has exceeded the timeout period, the GMBUS Slave Stall Timeout Error interrupt bit is set. **Value / Name / Description** 0b / Disable / Disable timeout counter 1b / Enable / Enable timeout counter
	28	**Reserved**
	27:25	**Bus Cycle Select** GMBUS cycle will always consist of a START followed by Slave Address, followed by an optional read or write data phase.

GMBUS1

A read cycle with an index will consist of a START followed by a Slave Address a WRITE indication and the INDEX and then a RESTART with a Slave Address and an optional read data phase.
The GMBUS cycle will terminate either with a STOP or by entering a wait state.
The WAIT state is exited by generating a STOP or by starting another GMBUS cycle.
This can only cause a STOP to be generated if a GMBUS cycle is generated, the GMBUS is currently in a data phase, or it is in a WAIT phase
Note that the three bits can be decoded as follows: 27 = STOP generated, 26 = INDEX used, 25 = Cycle ends in a WAIT

Value	Name	Description
000b	No cycle	No GMBUS cycle is generated
001b	No Index, No Stop, Wait	GMBUS cycle is generated without an INDEX, with no STOP, and ends with a WAIT
010b	Reserved	Reserved
011b	Index, No Stop, Wait	GMBUS cycle is generated with an INDEX, with no STOP, and ends with a WAIT
100b	Gen Stop	Generates a STOP if currently in a WAIT or after the completion of the current byte if active
101b	No Index, Stop	GMBUS cycle is generated without an INDEX and with a STOP
110b	Reserved	Reserved
111b	Index, Stop	GMBUS cycle is generated with an INDEX and with a STOP

24:16 **Total Byte Count**
This determines the total number of bytes to be transferred during the DATA phase of a GMBUS cycle.
The DATA phase can be prematurely terminated by generating a STOP while in the DATA phase (see Bus Cycle Select).
Do not change the value of this field during GMBUS cycles transactions.

15:8 **8 bit Slave Register Index**
(INDEX) This field specifies the 8-bits of index to be used for the generated bus write transaction or the index used for the WRITE portion of the WRITE/READ pair.
It only has an effect if the enable Index bit is set.
Do not change this field during a GMBUS transaction.

7:0 **Slave Address And Direction**
Bits 7:1 = 7-bit GMBUS Slave Address (SADDR): When a GMBUS cycle is to be generated using the Bus Cycle Select field, this field specifies the value of the slave address that is to be sent out.
For use with 10-bit slave address devices, set this value to 11110XXb (where the last two bits (XX) are the two MSBs of the 10-bit address) and the slave direction bit to a write.
This is followed by the first data byte being the 8 LSBs of the 10-bit slave address.

Bit 0 = Slave Direction Bit: When a GMBUS cycle is to be generated based on the Bus Cycle Select, this bit determines if the operation will be a read or a write.
A read operation with the index enabled will perform a write with just the index followed by a re-start and a read.
A 1 indicates that a Read from the slave device operation is to be performed.
A 0 indicates that a Write to the slave device operation is to be performed.

Value	Name	Description
00000001b	General	General Call Address
00000000b	Start	Start Bye
0000001Xb	CBUS	CBUS Address
11110XXXb	10-bit	10-Bit addressing
Others	Reserved	Reserved

2.2.6 GMBUS2—GMBUS Status

GMBUS2

Register Space:	MMIO: 0/2/0
Default Value:	0x00000800
Access:	R/W Protect
Size (in bits):	32
Address:	C5108h-C510Bh
Name:	GMBUS2 Status
ShortName:	GMBUS2

DWord	Bit	Description
0	31:16	**Reserved**
	15	**INUSE** Software wishing to arbitrate for the GMBUS resource can poll this bit until it reads a zero and will then own usage of the GMBUS controller. This bit has no effect on the hardware, and is only used as semaphore among various independent software threads that don't know how to synchronize their use of this resource that may need to use the GMBUS logic. Writing a one to this bit is software's indication that the software use of this resource is now terminated and it is available for other clients.

Value	Name	Description
0b	GMBUS is Acquired	Read operation that contains a zero in this bit position indicates that the GMBUS engine is now acquired and the subsequent reads of this register will now have this bit set. Writing a 0 to this bit has no effect.
1b	GMBUS in Use	Read operation that contains a one for this bit indicates that the GMBUS is currently allocated to someone else and "In use". Once set, a write of a 1 to this bit indicates that the software has relinquished the GMBUS resource and will reset the value of this bit to a 0.

	14	**Hardware Wait Phase**

Access:	RO

(HW_WAIT_PHASE) Once in a WAIT_PHASE, the software can now choose to generate a STOP cycle or a repeated start (RESTART) cycle followed by another GMBUS transaction on the GMBUS.

Value	Name	Description
0b	No Wait	The GMBUS engine is not in a wait phase.
1b	Wait	Set when GMBUS engine is in wait phase. Wait phase is entered at the end of the current transaction when that transaction is selected not to terminate with a STOP.

	13	**Slave Stall Timeout Error**

Access:	RO

This bit indicates that a slave stall timeout has occurred.
It is tied to the Enable Timeout (ENT) bit.

Value	Name	Description
0b	No Slave Timeout	No slave timeout has occurred
1b	Slave Timeout	A slave acknowledge timeout has occurred

	12	**GMBUS Interrupt Status**

Access:	RO

GMBUS2

This bit indicates that an event that causes a GMBUS interrupt has occurred.

Value	Name	Description
0b	No Interrupt	The conditions that could cause a GMBUS interrupt have not occurred or this bit has been cleared by software assertion of the SW_CLR_INT bit.
1b	Interrupt	GMBUS interrupt event occurred. This interrupt must have been one of the types enabled in the GMBUS4 register

11 **Hardware Ready**

Access:	RO

(HW_RDY) This provides a method of detecting when the current software client routine can proceed with the next step in a sequence of GMBUS operations.
This data handshake bit is used in conjunction with the SW_RDY bit.
When this bit is asserted by the GMBUS controller, it results in the de-assertion of the SW_RDY bit.
This bit resumes to normal operation when the SW_CLR_INT bit is written to a 0.

Value	Name	Description
0b	Ready 0	Condition required for assertion has not occurred or when this bit is a one and SW_RDY bit has been asserted During a GMBUS read transaction, after the each read of the data register During a GMBUS write transaction, after each write of the data register SW_CLR_INT bit has been cleared
1b	Ready 1 **[Default]**	This bit is asserted under the following conditions: After a reset or when the transaction is aborted by the setting of the SW_CLR_INT bit When an active GMBUS cycle has terminated with a STOP When during a GMBUS write transaction, the data register needs and can accept another four bytes of data During a GMBUS read transaction, this bit is asserted when the data register has four bytes of new data or the read transaction DATA phase is complete and the data register contains the last few bytes of the read data

10 **NAK Indicator**

Access:	RO

Value	Name	Description
0b	No bus error	No bus error has been detected or SW_CLR_INT has been written as a zero since the last bus error
1b	No Ack	Set by hardware if any expected device acknowledge is not received from the slave within the timeout

9 **GMBUS Active**

Access:	RO

(GA) This is a status bit that indicates whether the GMBUS controller is in an IDLE state or not.

Value	Name	Description
0b	Idle	The GMBUS controller is currently IDLE
1b	Active	This indicates that the bus is in START, ADDRESS, INDEX, DATA, WAIT, or STOP Phase. Set when GMBUS hardware is not IDLE.

8:0 **Current Byte Count**

Access:	RO

Can be used to determine the number of bytes currently transmitted/received by the GMBUS controller hardware.
Set to zero at the start of a GMBUS transaction data transfer and incremented after the completion of each byte of the data phase.
Note that because reads have internal storage, the byte count on a read operation may be ahead of

GMBUS2		
		the data that has been accepted from the data register.

2.2.7 GMBUS3—GMBUS Data Buffer

GMBUS3		
Register Space:		MMIO: 0/2/0
Default Value:		0x00000000
Access:		R/W Protect
Size (in bits):		32
Double Buffer Update Point:		Start of next Vblank
Double Buffer Armed By:		HW_RDY
Address:	C510Ch-C510Fh	
Name:	GMBUS3 Data Buffer	
ShortName:	GMBUS3	

This is data read/write register. This register is double buffered.
Bit 0 is the first bit sent or read, bit 7 is the 8th bit sent or read, all the way through bit 31 being the 32nd bit sent or read.
For GMBUS write operations with a non-zero byte count, this register should be written with the data before the GMBUS cycle is initiated.
For byte counts that are greater than four bytes, this register will be written with subsequent data only after the HW_RDY status bit is set indicating that the register is now ready for additional data.
For GMBUS read operations, software should wait until the HW_RDY bit indicates that the register contains the next set of valid read data before reading this register.

DWord	Bit	Description
0	31:24	**Data Byte 3**
	23:16	**Data Byte 2**
	15:8	**Data Byte 1**
	7:0	**Data Byte 0**

2.2.8 GMBUS4—GMBUS Interrupt Mask

GMBUS4		
Register Space:		MMIO: 0/2/0
Project:		
Default Value:		0x00000000
Access:		R/W
Size (in bits):		32
Address:	C5110h-C5113h	
Name:	GMBUS4 Interrupt Mask	
ShortName:	GMBUS4	

DWord	Bit	Description
0	31:5	**Reserved**
	4:0	**Interrupt Mask** This field specifies which GMBUS interrupts events may contribute to the setting of GMBUS interrupt status bit in second level interrupt status register. For gmbus writes, the HW Ready (HWRDY) interrupt indicates that software can write the next DWORD. It does NOT mean that the transfer of data to the slave device has completed. The IDLE or HW wait interrupt may be used to detect the end of writing data to the slave device. The HWRDY interrupt may be used for gmbus write cycles only to detect when to write the next DWORD after the first two DWORDs have been written to GMBUS3. For gmbus reads, the HWRDY interrupt indicates the arrival of the next dword.

Value	Name	Description
0XXXXb	GMBUS Slave stall TO Disable	Disable GMBUS Slave stall timeout interrupt
1XXXXb	GMBUS Slave stall TO Enable	Enable GMBUS Slave stall timeout interrupt
X0XXXb	GMBUS NAK Disable	Disable GMBUS NAK interrupt
X1XXXb	GMBUS NAK Enable	Enable GMBUS NAK interrupt
XX0XXb	GMBUS Idle Disable	Disable GMBUS Idle interrupt
XX1XXb	GMBUS Idle Enable	Enable GMBUS Idle interrupt
XXX0Xb	HW Wait Disable	Disable Hardware wait (GMBUS cycle without a stop has completed) Interrupt
XXX1Xb	HW Wait Enable	Enable Hardware wait (GMBUS cycle without a stop has completed) Interrupt
XXXX0b	HW Ready Disable	Disable Hardware ready (Data has been transferred) interrupt
XXXX1b	HW Ready Enable	Enable Hardware ready (Data has been transferred) interrupt

2.2.9 GMBUS5—GMBUS 2 Byte Index

GMBUS5		
Register Space:		MMIO: 0/2/0
Project:		
Default Value:		0x00000000
Access:		R/W
Size (in bits):		32
Address:	C5120h-C5123h	
Name:	GMBUS5 2 Byte Index	
ShortName:	GMBUS5	

This register provides a method for the software indicate to the GMBUS controller the 2 byte device index.

DWord	Bit	Description
0	31	**2 Byte Index Enable** When this bit is asserted (1), then bits 15:0 are used as the index. Bits 15:8 are used in the first byte which is the most significant index bits. The slave index in the GMBUS1<15:8> are ignored. Bits 7:0 are used in the second byte which is the least significant index bits.
	30:16	**Reserved**
	15:0	**2 Byte Slave Index** This is the 2 byte index used in all GMBUS accesses when bit 31 is asserted (1).

2.3 Display Clock Control

Pixel Data Rate	Dot Clock	Dual Channel?	External Clock	Data Clock Rate	Multiplier
	100-200MHz	NO	100-200MHz	1.0-2.0GHz	4x
	100-200MHz	NO	100-200MHz	1.0-2.0GHz	2x
	100-225MHz	NO	100-225MHz	1.0-2.25GHz	1x
LVDS 25-112MHz	25-112MHz	NO	25-112MHz	175-784MHz	1x
LVDS 80-224MHz	80-224MHz	YES	80-224MHz	280-784MHz	1x

Display Modes	Display Clock Frequency Range (MHz)
CRT DAC	25-350
HDMI/DVI	25-225 (pixel rate can differ from clock frequency)
	100-225 (pixel rate can differ from clock frequency)
LVDS (Single Channel)	25-112

Display Modes	Display Clock Frequency Range (MHz)
LVDS (Dual Channel)	80-224
	100-200
DisplayPort	162, 270 (pixel rate can differ from clock frequency)

The PLL frequency selection must be done such that the internal VCO frequency is within its limits.

The PLL Frequency is based on the selected register and the following formula.

DotClk_Frequency = (ReferenceFrequency * (5* (M1+2)+(M2+2)) / (N+2))/ (P1* P2)

Reference Frequency: 120 MHz for CRT, HDMI, LVDS, 100MHz for the FDI.

Item	Units	Range	Notes
Dot Clock	Frequency	20-350	MHz (Combining ALL modes)
VCO	Frequency	1760-3510	MHz
N – Counter	Value	3-8	
M – Counter	Value	79-127	M=5*(M1+2)+(M2+2)
M1 and M2		M1 > M2	
M1	Value	12-22	
M2	Value	5-9	
P-Div	Value	5-80	
P-Div	Value	28-112	Combined P1 and P2 for LVDS mode
P1-Div	Value	1-8	All modes

Note: For HDMI 12bpc usage model, the PCH display pixel clock should be programmed at 1.5x the effective pixel clock of the CPU display. This needs to be taken into account when setting the post divisors.

2.3.1 DPLL_CTL—DPLL Control

DPLL_CTL	
Register Space:	MMIO: 0/2/0
Project:	
Default Value:	0x04800080
Access:	R/W Protect
Size (in bits):	32
Double Buffer Update Point:	Transcoder vertical blank, except as stated
Address:	C6014h-C6017h
Name:	DPLLA Control
ShortName:	DPLL_CTL_A
Address:	C6018h-C601Bh
Name:	DPLLB Control

DPLL_CTL

ShortName: DPLL_CTL_B

Write Protect by Panel Power Sequencer when panel is connected to this transcoder.

DWord	Bit	Description
0	31	**DPLL VCO Enable** Access: R/W This bit will enable or disable the PLL VCO. Disabling the PLL will cause the display pixel clock to stop. Value / Name / Description: 0b / Disable / DPLL is disabled in its lowest power state 1b / Enable / DPLL is enabled and operational
	30	**DPLL High Speed IO clock En** Value / Name / Description: 0b / Disable / High Speed IO Clock Disabled 1b / Enable / High Speed IO Clock Enabled (must be set in HDMI/DVI and DisplayPort modes).
	29:28	**Reserved** Format: MBZ
	27:26	**DPLL Mode Select** Configure the DPLL for various supported Display Modes. Value / Name / Description: 00b / Reserved / Reserved 01b / Non-LVDS **[Default]** / DPLL in DAC/HDMI/DisplayPort mode. 10b / LVDS / DPLL in LVDS mode 11b / Reserved / Reserved
	25:24	**FP0 FP1 P2 Clock Divide** Value / Name / Description: 00b / Div 14 or 10 / Divide by 14 for Single-Channel LVDS. Divide by 10 for DisplayPort. Also used for DAC and HDMI modes with Dot Clock <= 225MHz. 01b / Div 7 or 5 / Divide by 7 for Dual-Channel LVDS Divide by 5 for DAC and HDMI modes with Dot Clock > 225MHz. Others / Reserved / Reserved
	23:16	**FP0 P1 Post Divisor** Writes to this byte finalize the write of m, n and p values into the PLL when the PLL is disabled. Writing to FP1 when FP0 is in use (or vice versa) is also allowed. Writes to this register take effect immediately. Value / Name / Description: 00000001b / 1 / Divide by one 00000010b / 2 / Divide by two 00000100b / 3 / Divide by three 00001000b / 4 / Divide by four 00010000b / 5 / Divide by five 00100000b / 6 / Divide by six 01000000b / 7 / Divide by seven 10000000b / 8 **[Default]** / Divide by eight Others / Reserved / Reserved
	15:13	**PLL Reference Input Select** (Not Double Buffered) The PLL reference should be selected based on the display device that is being driven. The standard reference clock is used for CRT modes using the analog port CRT DAC or LCD panels or for the integrated LVDS.

DPLL_CTL

Value	Name	Description
000b	DREFCLK	DREFCLK (default is 120 MHz) for DAC/HDMI/DVI/DisplayPort.
001b	Super SSC	120MHz super-spread clock
011b	SSC	Spread spectrum input clock (120MHz default) for LVDS/DisplayPort.
Others	Reserved	Reserved

12 **Reserved**

11:9 **DPLL HDMI multiplier**

This field determines the data multiplier for HDMI and is also applied to CRT.
In order to keep the clock rate to a more narrow range of rates, the multiplier is set and the Display PLL programmed to a multiple of the display mode's actual clock rate.
The value is = multiplication factor - 1

Value	Name
000b	1X
001b	2X
010b	3X
011b	4X

Programming Notes
Restriction : The DPLL must be enabled and stable before setting these bits. These bits must be programmed after DPLL_SEL is programmed.

8 **Reserved**

Format:	MBZ

7:0 **FP1 P1 Post Divisor**

Writes to this byte finalize the write of m, n and p values into the PLL when the PLL is disabled.
Writing to FP1 when FP0 is in use (or vice versa) is also allowed.
Writes to this register take effect immediately.

Value	Name	Description
00000001b	1	Divide by one
00000010b	2	Divide by two
00000100b	3	Divide by three
00001000b	4	Divide by four
00010000b	5	Divide by five
00100000b	6	Divide by six
01000000b	7	Divide by seven
10000000b	8 **[Default]**	Divide by eight
Others	Reserved	Reserved

2.3.2 DPLL_FP0—DPLL Divisor 0

DPLL_FP0	
Register Space:	MMIO: 0/2/0
Project:	
Default Value:	0x00000000
Access:	R/W Protect
Size (in bits):	32
Double Buffer Update Point:	Transcoder vertical blank
Address:	C6040h-C6043h
Name:	DPLLA Divisor 0
ShortName:	DPLL_FP0_A
Address:	C6048h-C604Bh
Name:	DPLLB Divisor 0
ShortName:	DPLL_FP0_B

Write Protect by Panel Power Sequencer when panel is connected to this transcoder.

DWord	Bit	Description
0	31:28	**Reserved** Format: MBZ
	27	**Frequency doubler clock enable** This bit enables/disables the frequency doubler clock. When the VCO clock to the doubler is disabled, the circuit does not dissipate power and its output clock is not available Value / Name / Description: 0b / Disable / Disables clock of frequency doubler 1b / Enable / Enables clock of frequency doubler
	26:25	**Reserved** Format: MBZ
	24:22	**CB Tuning** These bits are used for CB tuning the Display PLL Analog core on PCH. These bits are required to improve the jitter performance and VCO headroom of the Display PLL across Process, Voltage and Temperature variations. The CB tune should be turned on when the M/N ratio is less than a certain value given in the table below. The bits should be programmed to 0x011 to turn the complete CB cap on. Display Mode / If M/N Ratio is less than / Bits [24:22]: DAC / 21.00 / 011 HDMI / 21.00 / 011 LVDS 1ch (120mhz input clock) / 21.00 / 011 LVDS 2ch (120mhz input clock) / 21.00 / 011 LVDS 1ch (100mhz input clock) / 25.00 / 011 LVDS 2ch (100mhz input clock) / 25.00 / 011 **Example 1** In DAC mode, for pixel clock = 31MHz, N=4; M=83; P=80; Therefore M/N ratio = 20.75 which is < 21.00 mentioned in the table above. Hence the CB tune bits [24:22] need to be programmed to 011.

DPLL_FP0		
		Example 2 In DAC mode, for pixel clock = 31.5MHz, N=4; M=84; P=80; Therefore M/N ratio = 21 which equal to the value of M/N ration mentioned in the table above. Hence the CB tune bits [24:22] need to be programmed to 000.

Value	Name	Description
000b	Off	CB Tune Off
011b	100%	CB Tune 100% On

21:16	**FP0 N Divisor** N-Divisor value calculated for the desired output frequency. The register value is programmed two less than the actual divisor.
15:14	**Reserved** Format: MBZ
13:8	**FP0 M1 Divisor** M-Divisor value calculated for the desired output frequency. The register value is programmed to two less than the actual divisor.
7:6	**Reserved** Format: MBZ
5:0	**FP0 M2 Divisor** M-Divisor value calculated for the desired output frequency. The register value is programmed two less than the actual divisor.

2.3.3 DPLL_FP1—DPLL Divisor 1

DPLL_FP1	
Register Space:	MMIO: 0/2/0
Project:	
Default Value:	0x00000000
Access:	R/W Protect
Size (in bits):	32
Double Buffer Update Point:	Transcoder vertical blank
Address:	C6044h-C6047h
Name:	DPLLA Divisor 1
ShortName:	DPLL_FP1_A
Address:	C604Ch-C604Fh
Name:	DPLLB Divisor 1
ShortName:	DPLL_FP1_B

Write Protect by Panel Power Sequencer when panel is connected to this transcoder.

DWord	Bit	Description
0	31:25	**Reserved** Format: MBZ

DPLL_FP1		
	24:22	**CB Tuning** See FP0 CB_Tuning description **Value** / **Name** / **Description** 000b / Off / CB Tune Off 011b / 100% / CB Tune 100% On
	21:16	**FP1 N Divisor** N-Divisor value calculated for the desired output frequency. The register value is programmed two less than the actual divisor.
	15:14	**Reserved** Format: MBZ
	13:8	**FP1 M1 Divisor** M-Divisor value calculated for the desired output frequency. The register value is programmed to two less than the actual divisor.
	7:6	**Reserved** Format: MBZ
	5:0	**FP1 M2 Divisor** M-Divisor value calculated for the desired output frequency. The register value is programmed two less than the actual divisor.

2.3.4 DREF_CTL — Display Reference Clock Control

DREF_CTL		
Register Space:		MMIO: 0/2/0
Project:		
Default Value:		0x00000000
Access:		R/W
Size (in bits):		32
Address:	C6200h-C6203h	
Name:	Display Reference Clock Control	
ShortName:	DREF_CTL	

DWord	Bit	Description
0	31:15	**Reserved** Format: MBZ
	14:13	**120MHz CPU source output en** **Value** / **Name** / **Description** 00b / Disabled / Source output to CPU disabled 01b / Reserved / Rerserved 10b / Downspread / -0.5% SSC downspread source output to CPU enabled. Both the 120MHz SSC source (bits 12:11) and the SSC1 modulator (bit1) must be enabled prior to enabling this output 11b / Non-spread / Non-spread source output to CPU enabled. The 120MHz non-SSC source (bit 10:9) must be enabled prior to enabling this output
	12:11	**120MHz SSC source en** This bit enables the 120MHz SSC source used as a reference for DisplayPort or CPU

DREF_CTL

Value	Name	Description
00b	Disabled	Source disabled
01b	Reserved	Reserved for CK505 buffered source enabled
10b	Enabled	Integrated source enabled
11b	Reserved	Reserved

10:9 **120MHz nonspread source en**

This field enables the 120MHz non-SSC source for display

Value	Name	Description
00b	Disabled	Source disabled
01b	CK505	CK505 buffered source enabled.
10b	Integrated	Integrated source enabled
11b	Reserved	Reserved

8:7 **120MHz superspread source en**

This field enables the 120MHz super-SSC source for display

Value	Name	Description
00b	Disabled	Source disabled
01b	Reserved	Reserved
10b	Enabled	Integrated source enabled
11b	Reserved	Reserved

6 **SSC4 Spread Mode**

This is the reference clock used for super-spread on LVDS.
This bit must not be changed after bit 0 is set. It may be updated simultaneously with the update of bit 0.

Value	Name	Description
0b	Downspread	Center vs downspread: this bit sets down spread on the SSC4 modulator used for superspread.
1b	Centerspread	Center vs downspread: this bit sets center spread on the SSC4 modulator used for superspread.

Programming Notes
Restriction : This reference is shared with SATA. If it is used for SATA it must not be used for LVDS.

5:2 **Reserved**

Format:	MBZ

1 **120MHz SSC1 modulation en**

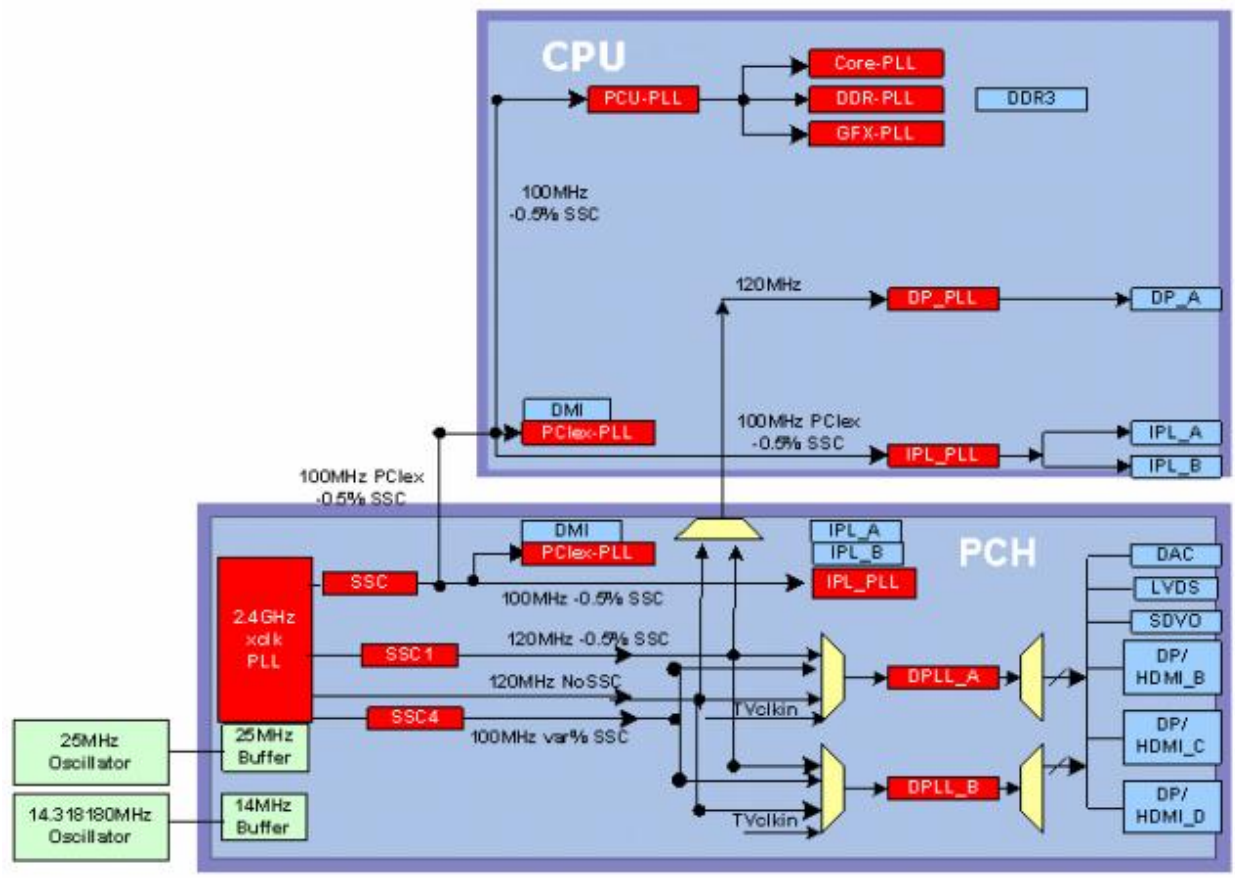
This bit enables the -0.5% modulator used for the 120MHz SSC source used for the CPU DisplayPort or as the -0.5% input to the DPLL in the PCH.
It must be set 0uS or more after the 120MHz SSC output is enabled (this bit and bits 12:11 can be written to enable at the same time).
PLL's using this clock as an input must be enabled 1uS or more after this bit is enabled to ensure a stable input.

Value	Name	Description
0b	Disabled	SSC1 disabled
1b	Enabled	SSC1 enabled

0 **120MHz SSC4 modulation en**

This bit enables the variable % modulator used for the 120MHz SSC source used for LVDS.
It must be set 0uS or more after the 120MHz super-spread source is enabled (this bit and bits 8:7 can be written to enable at the same time).
PLL's using this clock as an input must be enabled 1uS or more after this bit is enabled to ensure a stable input.

DREF_CTL				
		Value	Name	Description
		0b	Disabled	SSC4 disabled
		1b	Enabled	SSC4 enabled



2.3.5 RAWCLK_FREQ—Rawclk Frequency

RAWCLK_FREQ		
Register Space:		MMIO: 0/2/0
Project:		
Default Value:		0x00000000
Access:		R/W
Size (in bits):		32
Address:	C6204h-C6207h	
Name:	Rawclk Frequency	
ShortName:	RAWCLK_FREQ	

DWord	Bit	Description
0	31:10	**Reserved**
	9:0	**Rawclk frequency** Program this field to match the rawclk frequency of 125 MHz. This is used to generate a divided down clock for miscellaneous timers in display.

2.3.6 SSC4_PARMS – SSC4 Parameters

SSC4_PARMS		
Register Space:		MMIO: 0/2/0
Project:		
Default Value:		0x01204860
Access:		R/W
Size (in bits):		32
Address:	C6210h-C6213h	
Name:	SSC4 Parameters	
ShortName:	SSC4_PARMS	

Notes:

- This register must not be changed after bit 0 of register DREF_CTL is set.
- Default values of this register are meaningless.
- 0% spread option for SSC4 should be configured by clearing bit 0 of DREF_CTL to disable SSC4 module. In this case, registers SSC4PARMS and SSC4AuxPARMS settings have no effect and are don't care to the hardware. Bits 8:7 of DREF_CTL still need to be configured to enable the divisor DIV4, i.e. the source of the clock.
- This register needs to be configured by the display driver for desired spread percentages. Recommended settings for 0.5% down spread and 0.5%, 1.0%, 1.5%, 2.0%, and 2.5% center spread are listed in the following look-up table. Recommended settings for half-step clock bending usage is also listed.

Register fields	Half-step clock bend	0.5% down spread	0.5% center spread	1.0% center spread	1.5% center spread	2.0% center spread	2.5% center spread
6/5/4Ni_1NjRpt, [29:28]	00b	01b	01b	01b	01b	01b	01b
3Ni_1NjRpt,	000b	010b	010b	010b	010b	010b	010b

SSC4_PARMS

[26:24]							
2Ni1NjRpt, [22:20]	000b	111b	111b	111b	111b	111b	111b
1Ni1NjRpt, [18:10]	0_0000_0000b	0_0010_1001b	0_0010_1001b	0_0000_0010b	0_0000_1010b	0_0000_0010b	0_0000_1010b
MxPhsStp, [9:3]	000_0000b	000_0101b	000_0010b	000_0101b	000_0100b	000_0101b	000_0100b
PhsIncVal, [2:0]	000b	000b	000b	000b	001b	001b	010b

DWord	Bit	Description
0	31:30	**Reserved** Format: MBZ
	29:28	**SSC4 6 5 4Ni 1Nj Repeat Count** Select the number of repeats for the portion of 4, or 5, or 6 clocks of Ni and 1 clock of Nj within a dithering pattern of a step. See 1Ni_1Nj Repeat Count for more information. Value is zero based. Value: 00b — Name: 1 times
	27	**Reserved** Format: MBZ
	26:24	**SSC4 3Ni 1Nj Repeat Count** Default Value: 001b 2 times Select the number of repeats for the portion of 3 clocks of Ni and 1 clock of Nj within a dithering pattern of a step. See 1Ni_1Nj Repeat Count for more information. Value is zero based.
	23	**Reserved** Format: MBZ
	22:20	**SSC4 2Ni 1Nj Repeat Count** Default Value: 010b 3 times Select the number of repeats for the portion of 2 clocks of Ni and 1 clock of Nj within a dithering pattern of a step. See 1Ni_1Nj Repeat Count for more information. Value is zero based.
	19	**Reserved** Format: MBZ
	18:10	**SSC4 1Ni 1Nj Repeat Count** Default Value: 000010010b 19 times Select the number of repeats for the portion of 1 clock of Ni and 1 clock of Nj within a dithering pattern of a step. Together, 1Ni_1Nj Repeat Count, 2Ni_1Nj Repeat Count, 3Ni_1Nj Repeat Count, and 6/5/4Ni_1Nj Repeat Count tune the width of the target 32Khz modulated period. For down spread, the target these fields are to be tuned to is one half of the modulated period. For center spread, the target is one quarter of the modulated period. Value is zero based.
	9:3	**SSC4 Max Phase Step** Default Value: 0001100b 13 steps Select the number of steps to reach peak of modulated phase adjustment value. Together, Max Phase Step field and Phase Increment Value field control the magnitude of the spread. Value is zero based.
	2:0	**SSC4 Phase Increment Value**

SSC4_PARMS		
		Select the granularity of each phase step. Together, Max Phase Step field and Phase Increment Value field control the magnitude of the spread. Value is zero based.
		Value / **Name** 000b / 1 PI change per step

2.3.7 DPLL_SEL— DPLL Select

DPLL_SEL		
Register Space:		MMIO: 0/2/0
Project:		
Default Value:		0x00000000
Access:		R/W
Size (in bits):		32
Address:	C7000h-C7003h	
Name:	DPLL Select	
ShortName:	DPLL_SEL	

Individual bits are write protected by panel power sequencing when the panel is connected to the transcoder associated with that bit.

DWord	Bit	Description
0	31:12	**Reserved**
	11	**Transcoder C DPLL Enable** Value / Name / Description 0b / Disable / Disable DPLL to this transcoder 1b / Enable / Enable DPLL to this transcoder
	10:9	**Reserved**
	8	**Transcoder C DPLL Select** Value / Name / Description 0b / DPLLA / Select DPLLA for this transcoder 1b / DPLLB / Select DPLLB for this transcoder
	7	**Transcoder B DPLL Enable** Value / Name / Description 0b / Disable / Disable DPLL to this transcoder 1b / Enable / Enable DPLL to this transcoder
	6:5	**Reserved**
	4	**Transcoder B DPLL Select** Value / Name / Description 0b / DPLLA / Select DPLLA for this transcoder 1b / DPLLB / Select DPLLB for this transcoder
	3	**Transcoder A DPLL Enable** Value / Name / Description 0b / Disable / Disable DPLL to this transcoder 1b / Enable / Enable DPLL to this transcoder
	2:1	**Reserved**

DPLL_SEL		
	0	**Transcoder A DPLL Select** **Value** / **Name** / **Description** 0b / DPLLA / Select DPLLA for this transcoder 1b / DPLLB / Select DPLLB for this transcoder

2.4 Panel Power Sequencing

2.4.1 PP_STATUS—Panel Power Status

PP_STATUS		
Register Space:		MMIO: 0/2/0
Project:		
Default Value:		0x08000000
Access:		RO
Size (in bits):		32
Address:	C7200h-C7203h	
Name:	Panel Power Status	
ShortName:	PP_STATUS	

DWord	Bit	Description
0	31	**Panel Power On Status** This field gives the current panel power status **Value** / **Name** / **Description** 0b / Off / Indicates that the panel power down sequencing has completed. A power cycle delay may be currently active. It is safe and allowed to program timing, port, and DPLL registers. 1b / On / Indicates that the panel is currently powered up or is currently in the power down sequence and it is unsafe to change the timing, port, and DPLL registers for the pipe or transcoder that is assigned to the panel output. Register write protect is active and writes to protected registers will be ignored unless the write protect key value is set in the panel sequencing control register.
	30	**Require Asset Status** This bit indicates the status of programming of the DPLL and the selected port. A power on cycle will not be allowed unless this status indicates that the required assets are programmed and ready for use or the PP_CONTROL Write Protect Key is programmed to 0xABCD. The following conditions determine that the assets are ready: 1) PCH DPLL is enabled and frequency locked. 2) Port selected in PP_ON_DELAYS Panel control port select is enabled or is DisplayPort A. **Value** / **Name** / **Description** 0b / Not Ready / All required assets are not properly programmed 1b / Ready / All required assets are ready for the driving of a panel **Programming Notes** This bit should be ignored when using DisplayPort A.

PP_STATUS		
	29:28	**Power Sequence Progress** **Value** / **Name** / **Description** 00b / None / Indicates that the panel is not in a power sequence 01b / Power Up / Indicates that the panel is in a power up sequence (may include power cycle delay) 10b / Power Down / Indicates that the panel is in a power down sequence 11b / Reserved / Reserved
	27	**Power Cycle Delay Active** Power cycle delays occur after a panel power down sequence or after a hardware reset. On reset, a power cycle delay will occur using the default value for the timing. **Value** / **Name** / **Description** 0b / Not Active / A power cycle delay is not currently active 1b / Active **[Default]** / A power cycle delay (T4) is currently active
	26:4	**Reserved**

2.4.2 PP_CONTROL—Panel Power Control

PP_CONTROL		
Register Space:		MMIO: 0/2/0
Project:		
Default Value:		0x00000000
Access:		R/W
Size (in bits):		32
Address:	C7204h-C7207h	
Name:	Panel Power Control	
ShortName:	PP_CONTROL	

When the panel is either powered up or in the process of a power up sequence, registers involved in generation of panel timing or control become write protected.
Any write cycles to those write protected registers, while they will complete as normal, will not change the value of the register when write protected.
In situations where the embedded panel port is unused, the port should remain powered down and the write protect will be inactive.

List of write protected registers:
- LVDS Port Control (entire register)
- DisplayPort Control (port enable and port to transcoder select bits)
- Panel power on sequencing delays
- Panel power off sequencing delays
- Panel power cycle delay and Reference Divisor
- DPLL Control DPLL Divisors
- HTOTAL—Horizontal Total Register
- HBLANK—Horizontal Blank Register
- HSYNC—Horizontal Sync Register
- VTOTAL—Vertical Total Register
- VBLANK—Vertical Blank Register
- VSYNC—Vertical Sync Register

DWord	Bit	Description

PP_CONTROL

0 — 31:16 — Write Protect Key

This field in normal operation should be kept at the default value of 0000h. This field can be programmed with the key value "ABCD" to uncoditionally disable write protect.

Value	Name
0000h	Enable Write Protect **[Default]**
ABCDh	Disable Write Protect
Others	Enable Write Protect

Programming Notes

Workaround : Write Protect Key must be programmed to 0xABCD when using panel power sequencing on DisplayPort A (PP_ON_DELAYS bits 31:30 Panel Control port select is set to 01b DisplayPort A).

15:4 — Reserved

3 — eDP VDD Override for AUX

This bit is used to force on VDD for the embedded DisplayPort panel so AUX transactions can occur without enabling the panel power sequence.
This is intended for panels that require VDD to be asserted before accessing AUX port on the receiver.

Value	Name	Description
0b	Not Force	Panel VDD controlled by Panel Power Sequence state machine
1b	Force	Force panel VDD on to allow AUX transaction. Panel power sequence flow should be used regardless of the state of this bit when it is desired to enable the embedded DisplayPort main link.

Programming Notes

Restriction : When software clears this bit from ‘1’ to ‘0’ (disable VDD override) it must ensure that T4 power cycle delay is met before setting this bit to ‘1’ again.

2 — Backlight Enable

Enabling this bit enables the panel backlight when hardware is in the correct panel power sequence state and the port is a DisplayPort, as indicated in PP_ON_DELAYS Panel_control_port_select.

Value	Name	Description
0b	Disable	Backlight disabled
1b	Enable	Backlight enabled

1 — Power Down on Reset

Enabling this bit causes the panel to power down on reset warning.
When system reset is initiated, the panel power down sequence begins automatically.
If the panel is not on during a reset event, this bit is ignored.

Value	Name	Description
0b	Do not Run	Do not run panel power down sequence when reset is detected
1b	Run	Run panel power down sequence when system is reset

0 — Power State Target

This bit sets the panel power state target. It can be written at any time and takes effect at the completion of any current power cycle.

Value	Name	Description
0b	Off	The panel power state target is off. If the panel is either on or in a power on sequence, a power off sequence is started as soon as the panel reaches the power on state. This may include a power cycle delay. If the panel is currently off, there is no change of the power state or sequencing done.
1b	On	The panel power state target is on. If the panel is in either the off state or a power off sequence, and all pre-conditions are

PP_CONTROL				
				met, a power on sequence is started as soon as the panel reaches the power off state. This may include a power cycle delay. If the panel is currently on, there is no change of the power state or sequencing done.

2.4.3 PP_ON_DELAYS—Panel Power On Sequencing Delays

PP_ON_DELAYS			
Register Space:			MMIO: 0/2/0
Project:			
Default Value:			0x00000000
Access:			R/W Protect
Size (in bits):			32
Address:	C7208h-C720Bh		
Name:	Panel Power On Sequencing Delays		
ShortName:	PP_ON_DELAYS		
Write Protect by Panel Power Sequencer			

DWord	Bit	Description
0	31:30	**Panel control port select** These bits define to which port the embedded panel is connected. This is used for automatic control of the panel power. If the selected port is disabled, the power sequence will not allow a panel power up.

Value	Name	Description
00b	LVDS	Panel is connected to the LVDS port
01b	DisplayPort A	Panel is connected to the DisplayPort A
10b	DisplayPort C	Panel is connected to the DisplayPort C
11b	DisplayPort D	Panel is connected to the DisplayPort D

Programming Notes
Workaround : PP_CONTROL bits 31:16 Write_Protect_Key must be programmed to 0xABCD when using panel power sequencing on DisplayPort A.

DWord	Bit	Description
	29	**Reserved**
	28:16	**Power up delay** Programmable value of panel power sequencing delay during panel power up. The time unit used is the 100us timer. LVDS: This provides the time delay for the T1+T2 time sequence. DisplayPort: Software programs this field with the time delay for the eDP T3 time value; the time from the source enabling panel power to when the sink HPD and AUX channel are ready.
	15:13	**Reserved**
	12:0	**Power on to backlight on** Power on to backlight enable delay. Programmable value of panel power sequencing delay during panel power up. The time unit used is the 100us timer.

PP_ON_DELAYS		
		LVDS: This provides the time delay for the T5 time sequence. DisplayPort: Software programs this field with a value of 1b to get the minimum delay from hardware. Software controls the source valid video data output and backlight enable after this delay has been met. Hardware will not allow the backlight to enable until after this delay and the power up delay (eDP T3) have passed.

2.4.4 PP_OFF_DELAYS—Panel Power Off Sequencing Delays

PP_OFF_DELAYS		
Register Space:		MMIO: 0/2/0
Project:		
Default Value:		0x00000000
Access:		R/W Protect
Size (in bits):		32
Address:	C720Ch-C720Fh	
Name:	Panel Power Off Sequencing Delays	
ShortName:	PP_OFF_DELAYS	
Write Protect by Panel Power Sequencer		

DWord	Bit	Description
0	31:29	**Reserved**
	28:16	**Power Down delay** Programmable value of panel power sequencing delay during power up. The time unit used is the 100us timer. LVDS: This provides the time delay for the T3 time sequence. DisplayPort: Software programs this field with the time delay for the eDP T10 time value; the time from source ending valid video data to source disabling panel power. Software controls the source valid video data output, so this together with T9 is only used as a step towards the final power down delay.
	15:13	**Reserved**
	12:0	**Backlight off to power down** Power backlight off to power down delay. The time unit used is the 100us timer. LVDS: Programmable value of panel power sequencing delay during power down. This provides the time delay for the Tx time sequence. DisplayPort: Software programs this field with the time delay for the eDP T9 time value; the time from backlight disable to source ending valid video data. Software controls the backlight disable and source valid video data output, so this together with T10 is only used as a step towards the final power down delay.

2.4.5 PP_DIVISOR—Panel Power Cycle Delay and Reference Divisor

PP_DIVISOR	
Register Space:	MMIO: 0/2/0
Project:	
Default Value:	0x00186904
Access:	R/W Protect
Size (in bits):	32
Address:	C7210h-C7213h
Name:	Panel Power Cycle Delay and Reference Divisor
ShortName:	PP_DIVISOR

DWord	Bit	Description
0	31:8	**Reference divider** Default Value: 001869h 125MHz This field provides the value of the divider used for the creation of the panel timer reference clock. The value of zero should not be used. When it is desired to divide by N, the actual value to be programmed is (N/2)-1. The value should be (100 * Ref clock frequency in MHz / 2) - 1. Reference Clock: 125MHz — Frequency Value of Field: 1869h
	7:5	**Reserved**
	4:0	**Power Cycle Delay** Default Value: 4h 300 mS Programmable value of time panel must remain in a powered down state after powering down. If the panel power on sequence is attempted during this delay, the power on sequence will commence once the power cycle delay is complete. The time unit used is the 100 ms timer. This register needs to be programmed to a “+1” value. For instance to achieve 400 ms, program a value of 5. Writing a value of 0 selects no delay or is used to abort the delay if it is active. For devices coming out of reset, the timer will be set to the default value and the count down will begin after the de-assertion of reset. Even if the panel is not enabled, the count happens after reset. LVDS: This corresponds to the T4 of the SPWG specification. DisplayPort: This provides the time delay for the eDP T12 time value; the shortest time from panel power disable to power enable. If a panel power on sequence is attempted during this delay, the power on sequence will not commence until the delay is complete.

2.5 Backlight Control

2.5.1 SBLC_BLM_CTL1—South BLM PWM Control 1

SBLC_PWM_CTL1		
Register Space:		MMIO: 0/2/0
Project:		
Default Value:		0x00000000
Access:		R/W
Size (in bits):		32
Address:	C8250h-C8253h	
Name:	South BLM Control 1	
ShortName:	SBLC_PWM_CTL1	

DWord	Bit	Description
0	31	**PWM PCH Enable** This bit enables the PWM counter logic in the PCH.

Value	Name	Description
0b	Disable	PCH PWM disabled
1b	Enable	PCH PWM enabled

DWord	Bit	Description
	29	**Backlight Polarity** This field controls the polarity of the PWM signal.

Value	Name	Description
0b	High	Active High
1b	Low	Active Low

DWord	Bit	Description
	28:0	**Reserved**

2.5.2 SBLC_BLM_CTL2—South BLM PWM Control 2

SBLC_PWM_CTL2		
Register Space:		MMIO: 0/2/0
Project:		
Default Value:		0x00000000
Access:		R/W
Size (in bits):		32
Address:	C8254h-C8257h	
Name:	South BLM Control 2	
ShortName:	SBLC_PWM_CTL2	

DWord	Bit	Description
0	31:16	**Backlight Modulation Frequency** This field determines the number of time base events in total for a complete cycle of modulated backlight control. This field is normally set once during initialization based on the frequency of the clock that is being used and the desired PWM frequency. This value represents the period of the PWM stream in PCH display raw clocks multiplied by 128.
	15:0	**Backlight Duty Cycle Override** This value overrides the CPU control of PWM duty cycle when the PWM PCH Override Enable bit is set. This field determines the number of time base events for the active portion of the PWM backlight control. This should never be larger than the frequency field. A value of zero will turn the backlight off. A value equal to the backlight modulation frequency field will be full on. This field gets updated when it is desired to change the intensity of the backlight, it will take affect at the end of the current PWM cycle. This value represents the active time of the PWM stream in PCH display raw clock periods multiplied by 128.

3. South Display Engine Transcoder and Port Controls

3.1 Transcoder Timing

3.1.1 HTOTAL—Horizontal Total

HTOTAL		
Register Space:		MMIO: 0/2/0
Project:		
Default Value:		0x00000000
Access:		R/W
Size (in bits):		32
Address:	E0000h-E0003h	
Name:	Transcoder A Horizontal Total	
ShortName:	TRANS_HTOTAL_A	
Address:	E1000h-E1003h	
Name:	Transcoder B Horizontal Total	
ShortName:	TRANS_HTOTAL_B	
Address:	E2000h-E2003h	
Name:	Transcoder C Horizontal Total	
ShortName:	TRANS_HTOTAL_C	

Write Protect by Panel Power Sequencer when panel is connected to this transcoder.

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28:16	**Horizontal Total** This field specifies Horizontal Total size. This should be equal to the sum of the horizontal active and the horizontal blank sizes. This field is programmed to the number of pixels desired minus one. **Programming Notes** Restriction : The number of pixels (before the minus one) needs to be a multiple of two when driving the LVDS port in two channel mode. This register must always be programmed to the same value as the Horizontal Blank End.
	15:12	**Reserved** Format: MBZ
	11:0	**Horizontal Active** This field specifies Horizontal Active Display size. The first horizontal active display pixel is considered pixel number 0. This field is programmed to the number of pixels desired minus one. **Programming Notes**

HTOTAL		
		Restriction : The number of pixels (before the minus one) needs to be a multiple of two when driving the LVDS port in two channel mode. The minimum horizontal active display size is 64 pixels. This register must always be programmed to the same value as the Horizontal Blank Start.

3.1.2 HBLANK—Horizontal Blank

HBLANK		
Register Space:		MMIO: 0/2/0
Project:		
Default Value:		0x00000000
Access:		R/W
Size (in bits):		32
Address:	E0004h-E0007h	
Name:	Transcoder A Horizontal Blank	
ShortName:	TRANS_HBLANK_A	
Address:	E1004h-E1007h	
Name:	Transcoder B Horizontal Blank	
ShortName:	TRANS_HBLANK_B	
Address:	E2004h-E2007h	
Name:	Transcoder C Horizontal Blank	
ShortName:	TRANS_HBLANK_C	
Write Protect by Panel Power Sequencer when panel is connected to this transcoder.		

DWord	Bit	Description
0	31:29	**Reserved**
	28:16	**Horizontal Blank End** This field specifies Horizontal Blank End position relative to the horizontal active display start. **Programming Notes** Restriction : The number of pixels within horizontal blank needs to be a multiple of two when driving the LVDS port in two channel mode. The minimum horizontal blank size is 32 pixels This register must always be programmed to the same value as the Horizontal Total.
	15:13	**Reserved**
	12:0	**Horizontal Blank Start** This field specifies the Horizontal Blank Start position relative to the horizontal active display start. **Programming Notes** Restriction : This register must always be programmed to the same value as the Horizontal Active.

3.1.3 HSYNC—Horizontal Sync

HSYNC		
Register Space:		MMIO: 0/2/0
Project:		
Default Value:		0x00000000
Access:		R/W
Size (in bits):		32
Address:	E0008h-E000Bh	
Name:	Transcoder A Horizontal Sync	
ShortName:	TRANS_HSYNC_A	
Address:	E1008h-E100Bh	
Name:	Transcoder B Horizontal Sync	
ShortName:	TRANS_HSYNC_B	
Address:	E2008h-E200Bh	
Name:	Transcoder C Horizontal Sync	
ShortName:	TRANS_HSYNC_C	

Write Protect by Panel Power Sequencer when panel is connected to this transcoder.

DWord	Bit	Description
0	31:29	**Reserved** Format: MBZ
	28:16	**Horizontal Sync End** This field specifies the Horizontal Sync End position relative to the horizontal active display start. It is programmed with HorizontalActive+FrontPorch+Sync-1. **Programming Notes** Restriction : The number of pixels within horizontal sync needs to be a multiple of two when driving the LVDS port in two channel mode. This value must be greater than the horizontal sync start and less than Horizontal Total. Restriction : HDMI and DVI with audio are not supported when HSYNC Start is programmed equal to HBLANK Start.
	15:13	**Reserved** Format: MBZ
	12:0	**Horizontal Sync Start** This field specifies the Horizontal Sync Start position relative to the horizontal active display start. It is programmed with HorizontalActive+FrontPorch-1. **Programming Notes** Restriction : The number of pixels from active to horizontal sync needs to be a multiple of two when driving the LVDS port in two channel mode. This value must be greater than Horizontal Active.

3.1.4 VTOTAL—Vertical Total

VTOTAL		
Register Space:		MMIO: 0/2/0
Project:		
Default Value:		0x00000000
Access:		R/W
Size (in bits):		32
Address:	E000Ch-E000Fh	
Name:	Transcoder A Vertical Total	
ShortName:	TRANS_VTOTAL_A	
Address:	E100Ch-E100Fh	
Name:	Transcoder B Vertical Total	
ShortName:	TRANS_VTOTAL_B	
Address:	E200Ch-E200Fh	
Name:	Transcoder C Vertical Total	
ShortName:	TRANS_VTOTAL_C	

Write Protect by Panel Power Sequencer when panel is connected to this transcoder.

DWord	Bit	Description
0	31:29	**Reserved**
	28:16	**Vertical Total** This field specifies Vertical Total size. This should be equal to the sum of the vertical active and the vertical blank sizes. For progressive display modes, this field is programmed to the number of lines desired minus one. For interlaced display modes, this field is programmed with the number of lines desired minus two. The vertical counter is incremented on the leading edge of the horizontal sync. For interlaced display, hardware uses this value to calculate the vertical total in each field. Both even and odd vertical totals are supported. **Programming Notes** Restriction : This register must always be programmed to the same value as the Vertical Blank End.
	15:12	**Reserved**
	11:0	**Vertical Active** This field specifies Vertical Active Display size. The first vertical active display line is considered pixel number 0. This field is programmed to the number of lines desired minus one. For interlaced display, hardware uses this value to calculate the vertical active in each field. **Programming Notes** Restriction : When using the internal panel fitting logic, the minimum vertical active area must be seven lines. This register must always be programmed to the same value as the Vertical Blank Start.

3.1.5 VBLANK—Vertical Blank

VBLANK		
Register Space:		MMIO: 0/2/0
Project:		
Default Value:		0x00000000
Access:		R/W
Size (in bits):		32
Address:	E0010h-E0013h	
Name:	Transcoder A Vertical Blank	
ShortName:	TRANS_VBLANK_A	
Address:	E1010h-E1013h	
Name:	Transcoder B Vertical Blank	
ShortName:	TRANS_VBLANK_B	
Address:	E2010h-E2013h	
Name:	Transcoder C Vertical Blank	
ShortName:	TRANS_VBLANK_C	

Write Protect by Panel Power Sequencer when panel is connected to this transcoder.

DWord	Bit	Description
0	31:29	**Reserved**
	28:16	**Vertical Blank End** This field specifies Vertical Blank End position relative to the vertical active display start. For interlaced display, hardware uses this value to calculate the vertical blank end in each field. **Programming Notes** Restriction : This register must always be programmed to the same value as the Vertical Total. The minimum vertical blank size is 5 lines.
	15:13	**Reserved**
	12:0	**Vertical Blank Start** This field specifies the Vertical Blank Start position relative to the vertical active display start. For interlaced display, hardware uses this value to calculate the vertical blank start in each field. **Programming Notes** Restriction : This register must always be programmed to the same value as the Vertical Active

3.1.6 VSYNC—Vertical Sync

VSYNC		
Register Space:		MMIO: 0/2/0
Project:		
Default Value:		0x00000000
Access:		R/W
Size (in bits):		32
Address:	E0014h-E0017h	
Name:	Transcoder A Vertical Sync	
ShortName:	TRANS_VSYNC_A	
Address:	E1014h-E1017h	
Name:	Transcoder B Vertical Sync	
ShortName:	TRANS_VSYNC_B	
Address:	E2014h-E2017h	
Name:	Transcoder C Vertical Sync	
ShortName:	TRANS_VSYNC_C	

Write Protect by Panel Power Sequencer when panel is connected to this transcoder.

DWord	Bit	Description
0	31:29	**Reserved**
	28:16	**Vertical Sync End** This field specifies the Vertical Sync End position relative to the vertical active display start. It is programmed with VerticalActive+FrontPorch+Sync-1. For interlaced display, hardware uses this value to calculate the vertical sync start in each field. **Programming Notes** Restriction : This value must be greater than the vertical sync start and less than Vertical Total.
	15:13	**Reserved**
	12:0	**Vertical Sync Start** This field specifies the Vertical Sync Start position relative to the vertical active display start. It is programmed with VerticalActive+FrontPorch-1. For interlaced display, hardware uses this value to calculate the vertical sync end in each field. **Programming Notes** Restriction : This value must be greater than Vertical Active.

3.1.7 VSYNCSHIFT— Vertical Sync Shift

VSYNCSHIFT		
Register Space:		MMIO: 0/2/0
Project:		
Default Value:		0x00000000
Access:		R/W
Size (in bits):		32
Address:	E0028h-E002Bh	
Name:	Transcoder A Vertical Sync Shift	
ShortName:	TRANS_VSYNCSHIFT_A	
Address:	E1028h-E102Bh	
Name:	Transcoder B Vertical Sync Shift	
ShortName:	TRANS_VSYNCSHIFT_B	
Address:	E2028h-E202Bh	
Name:	Transcoder C Vertical Sync Shift	
ShortName:	TRANS_VSYNCSHIFT_C	
Write Protect by Panel Power Sequencer when panel is connected to this transcoder.		

DWord	Bit	Description
0	31:13	**Reserved**
	12:0	**Second Field VSync Shift** This value specifies the vertical sync alignment for the start of the interlaced second field, expressed in terms of the absolute pixel number relative to the horizontal active display start. This value will only be used if the transcoder is in an interlaced mode. Typically, the interlaced second field vertical sync should start one pixel after the point halfway between successive horizontal syncs, so the value of this register should be programmed to: horizontal sync start - floor[horizontal total / 2] (use the actual horizontal sync start and horizontal total values and not the minus one values programmed into the registers) This vertical sync shift only occurs during the interlaced second field. In all other cases the vertical sync start position is aligned with horizontal sync start.

3.2 Transcoder M/N Values

These values are used for DisplayPort.

When switching between two refresh rates, both the M1/N1 data and link values and the M2/N2 link values must be programmed. For dynamic refresh rate control, M1/N1 values are the primary values and are used for the normal M/N value setting, and M2/N2 values are the secondary values and are used for the lower power M/N value setting. Selection of M1/N1 or M2/N2 is indicated via MSA from the CPU display.

Example calculation of TU, Data M, and Data N: (See DisplayPort specification for exact calculation)

For modes that divide into the link frequency evenly,

Active/TU = Payload/Capacity = Data M/N = dot clock * bytes per pixel / ls_clk * number of lanes

Default value to program TU size is "111111" for TU size of 64.

Calculation of Link M and Link N:

Link M/N = dot clock / ls_clk

Restriction on clocks and number of lanes:

Number of lanes >= INT(dot clock * bytes per pixel / ls_clk)

Pcdclk * number of lanes >= dot clock * bytes per pixel

Please note that in the DisplayPort specification, dot clock is referred to as strm_clk.

3.2.1 DATAM— Data M Value

DATAM		
Register Space:		MMIO: 0/2/0
Project:		
Default Value:		0x00000000
Access:		R/W
Size (in bits):		32
Double Buffer Update Point:		Start of vertical blank
Double Buffer Armed By:		Writing the LINKN
Address:	E0030h-E0033h	
Name:	Transcoder A Data M value 1	
ShortName:	TRANS_DATAM1_A	
Address:	E0038h-E003Bh	
Name:	Transcoder A Data M value 2	
ShortName:	TRANS_DATAM2_A	
Address:	E1030h-E1033h	
Name:	Transcoder B Data M value 1	
ShortName:	TRANS_DATAM1_B	
Address:	E1038h-E103Bh	
Name:	Transcoder B Data M value 2	
ShortName:	TRANS_DATAM2_B	
Address:	E2030h-E2033h	
Name:	Transcoder C Data M value 1	
ShortName:	TRANS_DATAM1_C	
Address:	E2038h-E203Bh	
Name:	Transcoder C Data M value 2	

DATAM		
ShortName:	TRANS_DATAM2_C	
DWord	**Bit**	**Description**
0	31	**Reserved** Format: MBZ
	30:25	**TU Size** This field is the size of the transfer unit, minus one.
	24	**Reserved** Format: MBZ
	23:0	**Data M value** This field is the m value for internal use of the DDA.

3.2.2 DATAN— Data N Value

DATAN	
Register Space:	MMIO: 0/2/0
Project:	
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank
Double Buffer Armed By:	Writing the LINKN
Address:	E0034h-E0037h
Name:	Transcoder A Data N value 1
ShortName:	TRANS_DATAN1_A
Address:	E003Ch-E003Fh
Name:	Transcoder A Data N value 2
ShortName:	TRANS_DATAN2_A
Address:	E1034h-E1037h
Name:	Transcoder B Data N value 1
ShortName:	TRANS_DATAN1_B
Address:	E103Ch-E103Fh
Name:	Transcoder B Data N value 2
ShortName:	TRANS_DATAN2_B
Address:	E2034h-E2037h
Name:	Transcoder C Data N value 1
ShortName:	TRANS_DATAN1_C
Address:	E203Ch-E203Fh
Name:	Transcoder C Data N value 2
ShortName:	TRANS_DATAN2_C

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:0	**Data N value** This field is the n value for internal use of the DDA.

3.2.3 LINKM— Link M Value

LINKM		
Register Space:		MMIO: 0/2/0
Project:		
Default Value:		0x00000000
Access:		R/W
Size (in bits):		32
Double Buffer Update Point:		Start of vertical blank
Double Buffer Armed By:		Writing the LINKN
Address:	E0040h-E0043h	
Name:	Transcoder A Link M value 1	
ShortName:	TRANS_LINKM1_A	
Address:	E0048h-E004Bh	
Name:	Transcoder A Link M value 2	
ShortName:	TRANS_LINKM2_A	
Address:	E1040h-E1043h	
Name:	Transcoder B Link M value 1	
ShortName:	TRANS_LINKM1_B	
Address:	E1048h-E104Bh	
Name:	Transcoder B Link M value 2	
ShortName:	TRANS_LINKM2_B	
Address:	E2040h-E2043h	
Name:	Transcoder C Link M value 1	
ShortName:	TRANS_LINKM1_C	
Address:	E2048h-E204Bh	
Name:	Transcoder C Link M value 2	
ShortName:	TRANS_LINKM2_C	

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:0	**Link M value** This field is the m value for external transmission in the Main Stream Attributes.

3.2.4 LINKN— Link N Value

LINKN		
Register Space:		MMIO: 0/2/0
Project:		
Default Value:		0x00000000
Access:		R/W
Size (in bits):		32
Double Buffer Update Point:		Start of vertical blank
Address:	E0044h-E0047h	
Name:	Transcoder A Link N value 1	
ShortName:	TRANS_LINKN1_A	
Address:	E004Ch-E004Fh	
Name:	Transcoder A Link N value 2	
ShortName:	TRANS_LINKN2_A	
Address:	E1044h-E1047h	
Name:	Transcoder B Link N value 1	
ShortName:	TRANS_LINKN1_B	
Address:	E104Ch-E104Fh	
Name:	Transcoder B Link N value 2	
ShortName:	TRANS_LINKN2_B	
Address:	E2044h-E2047h	
Name:	Transcoder C Link N value 1	
ShortName:	TRANS_LINKN1_C	
Address:	E204Ch-E204Fh	
Name:	Transcoder C Link N value 2	
ShortName:	TRANS_LINKN2_C	

Writes to this register arm M/N registers for this transcoder.

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:0	**Link N value** This field is the n value for external transmission in the Main Stream Attributes and VB-ID.

3.3 Transcoder Video DIP

3.3.1 VIDEO_DIP_CTL—Video DIP Control

VIDEO_DIP_CTL	
Register Space:	MMIO: 0/2/0
Project:	
Default Value:	0x00200900
Access:	R/W
Size (in bits):	32
Address:	E0200h-E0203h
Name:	Transcoder A Video Data Island Packet Control
ShortName:	VIDEO_DIP_CTL_A
Address:	E1200h-E1203h
Name:	Transcoder B Video Data Island Packet Control
ShortName:	VIDEO_DIP_CTL_B
Address:	E2200h-E2203h
Name:	Transcoder C Video Data Island Packet Control
ShortName:	VIDEO_DIP_CTL_C

Please note that writes to this register take effect immediately. Therefore, it is critical for software to follow the write and read sequences as described in the bit 31 text.

DWord	Bit	Description
0	31	**Enable Graphics DIP** Data Island Packet (DIP) is a mechanism that allows up to 36 bytes to be sent over digital port during VBLANK, according to the HDMI and DisplayPort specifications. This includes header, payload, checksum and ECC information. Each type of DIP can be sent once per vsync, once every other vsync, or once. This data can be transmitted on either transcoder, through any digital port (digital port B, C or D), but not two simultaneously on one transcoder. Please note that the audio subsystem is also capable of sending Data Island Packets. These packets are programmed by the audio driver and can be read by in MMIO space via the audio control state and audio HDMI widget data island registers. Write sequence: Wait for 1 VSync to ensure completion of any pending DIP transmissions. Disable the Video_DIP_type_enable and set the Video_DIP_buffer_index for the DIP being written.

Set the Video_DIP_access_address to the desired DWORD to be written.

Write DIP data 1 DWORD at a time. The DIP access address auto-increments with each DWORD write, wrapping around to address 0 when the max buffer address size has been reached. Please note that software must write an entire DWORD at a time.

Enable the DIP type and transmission frequency.

Read sequence:

Set the Video_DIP_buffer_index for the DIP being read.

Set the Video_DIP_access_address to the desired DWORD to be read.

Read DIP data 1 DWORD at a time. The DIP access address auto-increments with each DWORD read, wrapping around to address 0 when the max buffer address size has been reached.

Value	Name	Description
0b	Disable	Video DIP is disabled
1b	Enable	Video DIP is enabled

Programming Notes
Partial DIPs are never sent out while the port is enabled. Disabling the DIP at the same time it is being transferred will result in the DIP being completed before the function is disabled. Shutting off the port on which DIP is being transmitted will result in partial transfer of DIP data. There is no need to switch off the DIP enable bit if the port transmitting DIP is disabled. Enabling a DIP function at the same time that the DIP would have been sent out (had it already been enabled) will result in the DIP being sent on the following frame. Enabling should only be done after the buffer contents have been written. If DIP is enabled but DIP types are all disabled, no DIP is sent. However, a single Null DIP will be sent at the same point in the stream that DIP packets would have been sent. This is done to keep the port in HDMI mode, otherwise it would revert to DVI mode. HDMI_CTL HDMI or DVI Select overrides this behavior.
Restriction : When disabling both the DIP port and DIP transmission, first disable the port and then disable DIP.
Workaround : Enable_Graphics_DIP (bit 31) and Data_Island_Packet_type_enable for AVI (bit 23) must be set or cleared in the same write if the HDMI port is already enabled.

30:26 **Reserved**

25 **GCP DIP enable**

This bit enables the output of the General Control Packet.
GCP is different from other DIPs in that much of the payload is automatically reflected in the packet, and therefore a DIP buffer for GCP is not needed.
Writes to this bit take effect immediately.

Value	Name	Description
0b	Disable	GCP DIP disabled
1b	Enable	GCP DIP enabled

VIDEO_DIP_CTL

Programming Notes
Workaround : Enable this bit before enabling the port when GCP is required, and disable this bit after disabling the port.

24:21 **Video DIP type enable**

These bits enable the output of a given data island packet type.
It can be updated while the port is enabled and is immediately updated (not double-buffered).
Within 2 vblank periods, the DIP is guaranteed to have been transmitted.

Value	Name	Description
0001b	Enable AVI DIP **[Default]**	
XXX1b	Enable AVI	Enable AVI DIP
XX1Xb	Enable Vendor	Enable Vendor-specific DIP
X1XXb	Enable Gamut	Enable Gamut Metadata Packet
1XXXb	Enable Source	Enable Source Product Description DIP

Programming Notes
Workaround : Software must enable VS DIP type (initialized to zero or programmed with valid VS payload) in addition when it is desired to enable AVI + SPD + GMP. AVI enable (bit 23) and Enable_Graphics_DIP (bit 31) must be set or cleared in the same write if the HDMI port is already enabled. AVI should be updated dynamically (without clearing the enable bit) by waiting for vertical blank and then updating the AVI buffer.

20:19 **Video DIP buffer index**

This field is used during programming of different DIPs.
These bits are used as an index to their respective DIP buffers.
The transmission frequency must also be written when programming the buffer.

Value	Name	Description
00b	AVI	AVI DIP (31 bytes of space available)
01b	Vendor-specific	Vendor-specific DIP
10b	Gamut Metadata	Gamut Metadata Packet
11b	Source Product	Source Product Description DIP

18 **Reserved**

17:16 **Video DIP frequency**

These bits dictate the frequency of Video DIP transmission for the DIP buffer index designated in bits 20:19.
When writing Video DIP data, this value is also latched when the first DW of the Video DIP is written.
When read, this value reflects the Video DIP transmission frequency for the Video DIP buffer designated in bits 20:19.
This field is ignored for Gamut Metadata Packet transmission.

Value	Name	Description
00b	Send Once	Send Once
01b	Every VSync	Send Every VSync (Default for AVI)
10b	Every Other Vsync	Send at least every other VSync
11b	Reserved	Reserved

Programming Notes
Restriction : Always program AVI to "Send Every Vsync" when enabling AVI.

VIDEO_DIP_CTL		
	15:12	**Reserved** Format: MBZ
	11:8	**Video DIP buffer size** Default Value: 1001b 9 dwords Access: RO This reflects the buffer size in dwords available for the type of Video DIP being indexed by bits 20:19 of this register, including the header. It is hardwired to the maximum size of a Video DIP, 36 bytes. Please note that this count includes ECC bytes, which are not writable by software. These bits are immediately valid after write of the DIP index.
	7:4	**Reserved** Format: MBZ
	3:0	**Video DIP access address** Selects the DWORD address for access to the Video DIP buffers. This value is automatically incremented after each read or write of the Video DIP Data Register. The value wraps back to zero when it autoincrements past the max address value of 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.

3.3.2 VIDEO_DIP_DATA–Video Data Island Packet Data

VIDEO_DIP_DATA		
Register Space:	MMIO: 0/2/0	
Project:		
Default Value:	0x00000000	
Access:	R/W (DWORD access only, no byte access)	
Size (in bits):	32	
Address:	E0208h-E020Bh	
Name:	Transcoder A Video Data Island Packet Data	
ShortName:	VIDEO_DIP_DATA_A	
Address:	E1208h-E120Bh	
Name:	Transcoder B Video Data Island Packet Data	
ShortName:	VIDEO_DIP_DATA_B	
Address:	E2208h-E220Bh	
Name:	Transcoder C Video Data Island Packet Data	
ShortName:	VIDEO_DIP_DATA_C	
Programming Notes		
Restriction : Writes must be full 32 bit DWORDs only. Byte enables are ignored.		

DWord	Bit	Description
0	31:0	**Video DIP DATA** When read, this returns the current value at the location specified in the Video DIP buffer index select and Video DIP access address fields. The address index is incremented after each read or write of this register. DIP data can be read at any time.

VIDEO_DIP_DATA		
		Data should be loaded before enabling the transmission through the DIP type enable bit.

Construction of DIP Data:

Dword	Byte3	Byte2	Byte1	Byte0
0	DP : HB3 HDMI: ECC (RO)	HB2	HB1	HB0
1	DB3	DB2	DB1	DB0
2	DB7	DB6	DB5	DB4
3	DB11	DB10	DB9	DB8
4	DB15	DB14	DB13	D12
5	DB19	DB18	DB17	DB16
6	DB23	DB22	DB21	DB20
7	DB27	DB26	DB25	DB24
8	ECC byte3 (RO)	ECC byte2 (RO)	ECC byte1 (RO)	ECC byte0 (RO)
9	DP: ECC byte7 (RO) HDMI : Reserved	DP: ECC byte6 (RO) HDMI : Reserved	DP: ECC byte5 (RO) HDMI : Reserved	DP: ECC byte4 (RO) HDMI : Reserved
10	DP: ECC byte11 (RO) HDMI : Reserved	DP: ECC byte10 (RO) HDMI : Reserved	DP: ECC byte9 (RO) HDMI : Reserved	DP: ECC byte8 (RO) HDMI : Reserved
11	Reserved	Reserved	Reserved	Reserved
12	Reserved	Reserved	Reserved	Reserved
13	Reserved	Reserved	Reserved	Reserved
14	Reserved	Reserved	Reserved	Reserved
15	Reserved	Reserved	Reserved	Reserved

HB = Header Byte

DB = Data Byte

DP = DisplayPort

3.3.3 VIDEO_DIP_GCP–Video Data Island Payload GCP

VIDEO_DIP_GCP	
Register Space:	MMIO: 0/2/0
Project:	
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	E0210h-E0213h
Name:	Transcoder A Video Data Island Payload
ShortName:	VIDEO_DIP_GCP_A
Address:	E1210h-E1213h
Name:	Transcoder B Video Data Island Payload
ShortName:	VIDEO_DIP_GCP_B
Address:	E2210h-E2213h
Name:	Transcoder C Video Data Island Payload
ShortName:	VIDEO_DIP_GCP_C

DWord	Bit	Description
0	31:3	**Reserved** Format: MBZ
	2	**GCP color indication** This bit must be set when in deep color mode. It may optionally be set for 24-bit mode. It must be set if the sink attached to the transcoder can receive GCP data. Value / Name / Description: 0b / Don't Indicate / Don't indicate color depth. CD and PP bits in GCP set to zero 1b / Indicate / Indicate color depth using CD bits in GCP. It will be set depending on programmed pixel depth in port control register
	1	**GCP default phase enable** Indicates the video timings meet alignment requirements such that the following conditions are met: Htotal is an even number Hactive is an even number Hsync is an even number Front and back porches for Hsync are even numbers Vsync always starts on an even-numbered pixel within a line in interlaced modes (starting counting with 0) Value / Name / Description: 0b / Clear / Default phase bit in GCP is cleared 1b / Require Met / Default phase bit in GCP is set.

VIDEO_DIP_GCP				
				All requirements must be met before setting this bit

3.4 Transcoder DisplayPort Control

3.4.1 TRANS_DP_CTL—Transcoder DisplayPort Control

TRANS_DP_CTL	
Register Space:	MMIO: 0/2/0
Project:	
Default Value:	0x60000018
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Depends on bit
Address:	E0300h-E0303h
Name:	Transcoder A DisplayPort Control
ShortName:	TRANS_DP_CTL_A
Address:	E1300h-E1303h
Name:	Transcoder B DisplayPort Control
ShortName:	TRANS_DP_CTL_B
Address:	E2300h-E2303h
Name:	Transcoder C DisplayPort Control
ShortName:	TRANS_DP_CTL_C

This register configures transcoder based DisplayPort logic. This register must be used in conjunction with the DisplayPort Control registers.

DWord	Bit	Description
0	31	**Transcoder DP Output Enable** This bit determines if this transcoder will output to a DisplayPort. Value / Name / Description: 0b / Disable / Disable the transcoder output to DisplayPort 1b / Enable / Enable the transcoder to output to DisplayPort **Programming Notes** Restriction : Transcoder DP Port Select needs to be set to 11b (None) when writing a 0b to this bit to disable transcoder output to DisplayPort.
	30:29	**Transcoder DP Port Select** This bit determines which DisplayPort port block will be driven by the DisplayPort output of this transcoder. Port selection takes place on the Vblank after being written. Value / Name / Description: 00b / Port B / DisplayPort Port B 01b / Port C / DisplayPort Port C 10b / Port D / DisplayPort Port D

TRANS_DP_CTL

	11b	None **[Default]**	No port selected

Programming Notes

Restriction : This field needs to be set to 11b (None) when writing a 0b to Transcoder_DP_Output_Enable to disable transcoder output to DisplayPort.

28:27	**Reserved**	
	Format:	MBZ
25:19	**Reserved**	
	Format:	MBZ
17:12	**Reserved**	
	Format:	MBZ

11:9 **Transcoder DP Bits Per Color**

This field selects the number of bits per color output on DisplayPorts connected to this transcoder. Software should enable dithering in the pipe if selecting a pixel color depth higher or lower than the pixel color depth of the frame buffer.

Value	Name	Description
000b	8 bpc	8 bits per color
001b	10 bpc	10 bits per color
010b	6 bpc	6 bits per color
011b	12 bpc	12 bits per color
Others	Reserved	Reserved

8:5	**Reserved**	
	Format:	MBZ

4:3 **Transcoder DP Sync Polarity**

Indicates the polarity of Hsync and Vsync to be transmitted in MSA on this transcoder DisplayPort output.

Value	Name	Description
00b	Low	VS and HS are active low (inverted)
01b	VS Low, HS High	VS is active low (inverted), HS is active high
10b	VS High, HS Low	VS is active high, HS is active low (inverted)
11b	High **[Default]**	VS and HS are active high

2:0	**Reserved**	
	Format:	MBZ

3.5 Analog Port CRT DAC

3.5.1 DAC_CTL—Analog Port CRT DAC Control

DAC_CTL

Register Space:	MMIO: 0/2/0
Project:	
Default Value:	0x00040000
Access:	R/W
Size (in bits):	32

Address:	E1100h-E1103h
Name:	Analog Port CRT DAC Control
ShortName:	DAC_CTL

DWord	Bit	Description
0	31	**Port Enable** This bit enables or disables the analog port CRT DAC and syncs outputs. The CRT DAC disable fuse can block this from enabling.

Value	Name	Description
0b	Disable	Disable the analog port DAC and disable output of syncs
1b	Enable	Enable the analog port DAC and enable output of syncs

Bit	Description
30:29	**Transcoder Select** Determines which transcoder will feed this DAC port.

Value	Name	Description
00b	Transcoder A	Transcoder A
01b	Transcoder B	Transcoder B
10b	Transcoder C	Transcoder C
11b	Reserved	Reserved

Bit	Description
28:26	**Reserved**
25:24	**CRT HPD Channel Status**

Access:	RO

These bits are set when a CRT hot plug or unplug event has been detected and indicate which color channels were attached.
Write a one to these bits to clear the status.
The rising or falling edges of these bits are ORed together to go to the SDE_ISR CRT hot plug register bit.

Value	Name	Description
00b	None	No channels attached
01b	Blue	Blue channel only is attached
10b	Green	Green channel only is attached
11b	Both	Both blue and green channel attached

Bit	Description
23	**CRT HPD Enable** Hot plug detection is used to set status bits or an interrupt on the connection or disconnection of a CRT to the analog port CRT DAC.

Value	Name	Description
0b	Disable	CRT hot plug detection is disabled
1b	Enable	CRT hot plug detection is enabled

Bit	Description
22	**CRT HPD Activation Period**

DAC_CTL

This bit sets the activation period for the CRT hot plug circuit.

Value	Name	Description
0b	64 rawclk	64 rawclk periods
1b	128 rawclk	128 rawclk periods

21 **CRT HPD Warmup Time**

This bit sets the warmup time for the CRT hot plug circuit.

Value	Name	Description
0b	4ms	Approximately 4ms
1b	8ms	Approximately 8ms

20 **CRT HPD Sampling Period**

This bit determines the length of time between sampling periods when the transcoder is disabled.

Value	Name	Description
0b	2 seconds	Approximately 2 seconds
1b	4 seconds	Approximately 4 seconds

19:18 **CRT HPD Voltage Value**

Compare value for Vref to determine whether the analog port is connected to a CRT.

Value	Name	Description
00b	40	40
01b	50 **[Default]**	50
10b	60	60
11b	70	70 (bit 17 must be = 1)

17 **CRT HPD Reference Voltage**

Value	Name	Description
0b	325mv	325mv
1b	475mv	475mv (bits 19:18 must be = 11)

16 **Force CRT HPD Trigger**

Triggers a CRT hotplug/unplug detection cycle independent of the hot plug detection enable bit.
This bit is automatically cleared after the detection is completed.
The result of this trigger is reflected in the CRT Hot Plug Detection Status. Software must reset status after a force CRT detect trigger.

Value	Name	Description
0b	No Trigger	No Trigger
1b	Force Trigger	Force Trigger

15:5 **Reserved**

4 **VSYNC Polarity Control**

The output VSYNC polarity is controlled by this bit.
This is used to implement display modes that require inverted polarity syncs and to set the disabled state of the VSYNC signal.

Value	Name	Description
0b	Low	Active Low
1b	High	Active High

3 **HSYNC Polarity Control**

The output HSYNC polarity is controlled by this bit.
This is used to implement display modes that require inverted polarity syncs and to set the disabled state of the HSYNC signal.

Value	Name	Description
0b	Low	Active Low
1b	High	Active High

DAC_CTL		
	2:0	**Reserved**

3.6 HDMI Port

3.6.1 HDMI_CTL—HDMI Port Control

HDMI_CTL		
Register Space:		MMIO: 0/2/0
Project:		
Default Value:		0x00000018
Access:		R/W
Size (in bits):		32
Double Buffer Update Point:		Depends on bit
Address:	E1140h-E1143h	
Name:	HDMI Port B Control	
ShortName:	HDMI_CTL_B	
Address:	E1150h-E1153h	
Name:	HDMI Port C Control	
ShortName:	HDMI_CTL_C	
Address:	E1160h-E1163h	
Name:	HDMI Port D Control	
ShortName:	HDMI_CTL_D	

DisplayPort B uses the same physical pins as HDMI/DVI B. Therefore HDMI/DVI B and DisplayPort B cannot be enabled simultaneously. The same applies for ports C and D.

DWord	Bit	Description
0	31	**Port Enable** Disabling this port will put it in its lowest power state. Port enable takes place on the Vblank after being written. Both this bit and the audio output bit of this register must be enabled to send audio over this port.

Value	Name	Description
0b	Disable	Disable and tristates the port interface
1b	Enable	Enables the port interface

Programming Notes
Workaround : During modeset, for inverted vertical sync mode turn on Port_Enable during the vertical active region.

DWord	Bit	Description
	30:29	**Transcoder Select** This bit determines from which display transcoder the source data will originate. Transcoder selection takes place on the Vblank after being written.

Value	Name	Description
00b	Transcoder A	Transcoder A

HDMI_CTL

01b	Transcoder B	Transcoder B
10b	Transcoder C	Transcoder C
11b	Reserved	Reserved

28:26 **Color Format**

This field selects the number of bits per color sent to a receiver device connected to this port.
Color format takes place on the Vblank after being written.
Color format change must be done as a part of mode set since different color depths require different pixel clock settings.
Software should enable dithering in the pipe/transcoder if selecting a pixel color depth higher or lower than the pixel color depth of the frame buffer.

Value	Name	Description
000b	8 BPC	8 bits per color
011b	12 BPC	12 bits per color
Others	Reserved	Reserved

Programming Notes

Workaround (WaEnableHDMI8bpcBefore12bpc) : When enabling HDMI with the 12 BPC mode, disable HDMI clock gating, enable HDMI with Color Format in 8 BPC mode, switch Color Format to 12 BPC mode, then restore HDMI clock gating.

Suggested sequence:
0. Driver notified that HDMI must be enabled with the 12 bits per color format
1. Disable HDMI clock gating (see clock gate disable locations below)
2. Write to HDMI control register with Port Enable = Enable, Color Format = 8 BPC, and other fields set as needed
3. Write to HDMI control register with Port Enable = Enable, Color Format = 12 BPC, and other fields set as needed
4. Restore HDMI clock gating

HDMI clock gating for transcoder A is disabled by setting 0xF0060 bit 10 = 1.
HDMI clock gating for transcoder B is disabled by setting 0xF1060 bit 10 = 1.
HDMI clock gating for transcoder C is disabled by setting 0xF2060 bit 10 = 1.

24 **Reserved**

22:19 **Reserved**

17:16 **Reserved**

15 **Port Lane Reversal**

This bit reverses the order of the 4 lanes within the port.
Locked once port is enabled. Updates when the port is disabled then re-enabled

Value	Name	Description
0b	Not reversed	Not reversed
1b	Reversed	Reversed

14:12 **Reserved**

11:10 **Encoding**

These bits select among encoding types.

Value	Name	Description
10b	TMDS	TMDS encoding for HDMI/DVI. In this mode, the external HPD pin is used to generate hotplug.
Others	Reserved	Reserved

HDMI_CTL

9 — HDMI or DVI Select

This bit selects between HDMI and DVI modes of operation.
HDMI mode enables a null packet (32 bytes of a value of 0) to be sent when Vsync=1 on this port, required for HDMI operation. It also enables preambles and guardbands prior to the null packets, in accordance with the HDMI specification.

Value	Name	Description
0b	DVI	Port will function in DVI mode if no DIP packets are enabled and no audio is present.
1b	HDMI	Port will function in HDMI mode.

8 — Reserved

Format:	MBZ

6 — Audio Output Enable

This bit directs audio to this port.
When enabled and audio data is available, the audio data will be combined with the video data and sent over this port.
The status of this bit is used to indicate presence of the HDMI output to the audio driver.

Value	Name	Description
0b	Disable	No audio output on this port
1b	Enable	Enable audio on this port

4:3 — Sync Polarity

Indicates the polarity of Hsync and Vsync.
Inverted polarity is transmitted as SYNC-BLANK-SYNC and standard polarity is transmitted as BLANK-SYNC-BLANK.
For example, if Vsync is not inverted and Hsync is inverted, an Hsync period transmitted during Vsync would be transmitted as BLANK+VS+HS – BLANK+VS – BLANK+VS+HS.

Value	Name	Description
00b	VS Low, HS Low	VS and HS are active low (inverted)
01b	VS Low, HS High	VS is active low (inverted), HS is active high
10b	VS High, HS Low	VS is active high, HS is active low (inverted)
11b	VS High, HS High **[Default]**	VS and HS are active high

2 — Port Detected

Access:	RO

Read-only bit indicating whether a digital display was detected during initialization.
It signifies the level of the GMBUS port (port 4 for B, port 3 for C, port 5 for D) data line at boot.
This bit is valid regardless of whether the port is enabled.

Value	Name	Description
0b	Not Detected	Port not detected during initialization
1b	Detected	Port detected during initialization

1:0 — Reserved

Format:	MBZ

3.6.2 HDMI_BUF_CTL—HDMI Buffer Control

HDMI_BUF_CTL	
Register Space:	MMIO: 0/2/0
Project:	
Default Value:	0x01773F30
Access:	R/W
Size (in bits):	32
Address:	FC810h-FC813h
Name:	HDMI Buffer Control Lane 0
ShortName:	HDMI_BUF_CTL_0
Address:	FC81Ch-FC81Fh
Name:	HDMI Buffer Control Lane 1
ShortName:	HDMI_BUF_CTL_1
Address:	FC828h-FC82Bh
Name:	HDMI Buffer Control Lane 2
ShortName:	HDMI_BUF_CTL_2
Address:	FC834h-FC837h
Name:	HDMI Buffer Control Lane 3
ShortName:	HDMI_BUF_CTL_3
Address:	FCC00h-FCC03h
Name:	HDMI Buffer Control Lane 4
ShortName:	HDMI_BUF_CTL_4
Address:	FCC0Ch-FCC0Fh
Name:	HDMI Buffer Control Lane 5
ShortName:	HDMI_BUF_CTL_5
Address:	FCC18h-FCC1Bh
Name:	HDMI Buffer Control Lane 6
ShortName:	HDMI_BUF_CTL_6
Address:	FCC24h-FCC27h
Name:	HDMI Buffer Control Lane 7
ShortName:	HDMI_BUF_CTL_7
Address:	FD000h-FD003h
Name:	HDMI Buffer Control Lane 8
ShortName:	HDMI_BUF_CTL_8
Address:	FD00Ch-FD00Fh
Name:	HDMI Buffer Control Lane 9
ShortName:	HDMI_BUF_CTL_9
Address:	FD018h-FD01Bh
Name:	HDMI Buffer Control Lane 10

HDMI_BUF_CTL

ShortName:	HDMI_BUF_CTL_10
Address:	FD024h-FD027h
Name:	HDMI Buffer Control Lane 11
ShortName:	HDMI_BUF_CTL_11

Lanes 0-3 are used by port B.
Lanes 4-7 are used by port C.
Lanes 8-11 are used by port D.

Programming Notes

The default values are not the optimal values.
Correct values should be programmed prior to enabling HDMI.
See the HDMI Buffer Control Register Settings table for the correct values to use.

DWord	Bit	Description
0	31:25	**Reserved** Format: MBZ
	24:17	**Driver Swing Control** This field modulates the output swing while maintaining the pre-emphasis level.

Value	Name
01100110b	0.90x
01110111b	0.95x
10001000b	1.00x
10011001b	1.05x
10101010b	1.10x
10111011b	1.15x **[Default]**
11001100b	1.20x
11011101b	1.25x
11101110b	1.30x
11111111b	1.35x

	16:3	**Driver Enable and Pre-Emphasis Control** Default Value: 10011111100110b This field sets the Driver Enable/Pre-emphasis Settings.

Programming Notes

Refer to the HDMI Buffer Control Register Settings table for valid settings.

	2:0	**Reserved** Format: MBZ

HDMI Buffer Control Register Settings:

Approximate Swing	Approximate Preemp	Register Value	Notes
800mV	4.0dB	0x01773F30	Register default
800mV	0.0dB	0x01986F00	HDMI Active Level Shifter Optimized Setting
800mV	3.0dB	0x01FFFF28	HDMI Cost Reduced Level Shifter Optimized Setting
1000mV	0.0dB	0x01993F00	Alternate HDMI Setting
900mV	0.0dB	0x01987D00	Alternate HDMI Setting
775mV	0.0dB	0x01987300	Alternate HDMI Setting
750mV	0.0dB	0x01986D00	Alternate HDMI Setting
725mV	0.0dB	0x01986B00	Alternate HDMI Setting
700mV	0.0dB	0x01986700	Alternate HDMI Setting
400mV	0.0dB	0x01982000	Level 0 Preemp 0
400mV	3.5dB	0x01981710	Level 0 Preemp 1

Approximate Swing	Approximate Preemp	Register Value	Notes
400mV	6.0dB	0x0198DF48	Level 0 Preemp 2
400mV	9.5dB	0x01DCBF70	Level 0 Preemp 3
600mV	0.0dB	0x01981700	Level 1 Preemp 0
600mV	3.5dB	0x01996F40	Level 1 Preemp 1
600mV	6.0dB	0x01FF3F68	Level 1 Preemp 2
800mV	0.0dB	0x01983D00	Level 2 Preemp 0
800mV	3.5dB	0x01FF3F30	Level 3 Preemp 1
1200mV	0.0dB	0x01FFFF00	Level 4 Preemp 0

3.7 LVDS Port

3.7.1 LVDS_CTL—LVDS Port Control

LVDS_CTL

Register Space:	MMIO: 0/2/0
Project:	
Default Value:	0x00000000
Access:	R/W Protect
Size (in bits):	32

Address:	E1180h-E1183h
Name:	LVDS Port Control
ShortName:	LVDS_CTL

Write Protect by Panel Power Sequencer

DWord	Bit	Description
0	31	**LVDS Port Enable** When disabled the LVDS port is inactive and in it's low power state. Enabling the LVDS port changes the way that the PLL for this transcoder is programmed. This bit must be set before the display PLL is enabled and the port is power sequenced on using the panel power sequencing logic.

Value	Name	Description
0b	Disable	The port is disabled and all LVDS pairs are powered down.
1b	Enable	The port is enabled. The LVDS disable fuse can block this port from enabing.

Programming Notes
Workaround : LVDS clock gating must be disabled (South Display Unit Clock Gating Disable bits #30 and #14 in 0xC2020 set to '1') at boot and remained disabled before enabling dual channel LDVS mode.

DWord	Bit	Description
	30:29	**LVDS Port Transcoder Select** This field selects which transcoder LVDS is attached to.

Value	Name	Description
00b	Transcoder A	The port gets data from Transcoder A
01b	Transcoder B	The port gets data from Transcoder B
10b	Transcoder C	The port gets data from Transcoder C
11b	Reserved	Reserved

LVDS_CTL

Programming Notes
Workaround : The transcoder select state must be preserved when disabling the port. The transcoder select may be updated after the port has been disabled.

28:25 **Reserved**

24 **Data Format Select**
Combined with the other control bits it selects the LVDS data format. Other control bits in this register determine if two channel is enabled and 18 or 24 bit color is enabled.

Value	Name	Description
0b	1x18.0, 2x18.0, 1x24.0 or 2x24.0	1x18.0, 2x18.0, 1x24.0 or 2x24.0
1b	1x24.1 or 2x24.1	1x24.1 or 2x24.1

23 **LE Control Enable**
This bit is used when the second channel control signal field indicates that we are using the LE instead of HS and the two channel mode is enabled. In single channel mode, this bit has no effect.

Value	Name	Description
0b	Send 0	Send 0 on second channel HS (B2<2>)
1b	Send 1	Send 1 on second channel HS

22 **LF Control Enable**
This bit is used when the second channel control signal field indicates that we are using the LF instead of VS and two channel mode is enabled. In single channel mode, this bit has no effect.

Value	Name	Description
0b	Send 0	Send 0 on second channel VS (B2<3>)
1b	Send 1	Send 1 on second channel VS

21 **VSYNC Polarity**
This controls the polarity of the VSYNC indicator that is sent over the LVDS connection. Panels may require one or the other polarity or work with either polarity.

Value	Name	Description
0b	No Invert	No inversion (1=active)
1b	Invert	Invert the sense (0=active)

20 **HSYNC Polarity**
(LP_Invert) This controls the polarity of the HSYNC indicator that is sent over the LVDS connection. Panels may require one or the other polarity or work with either polarity.

Value	Name	Description
0b	No Invert	No inversion (1=active)
1b	Invert	Invert the sense (0=active)

19 **DE Invert**
This controls the polarity of the DE indicator that is sent over the LVDS connection.

Value	Name	Description
0b	No Invert	No inversion of DE (1=active)
1b	Invert	Invert the sense of DE (0=active)

18:17 **Second Channel Control Signals**
This bit only applies to the two channel modes of operation it has no effect in single channel modes.

Value	Name	Description
00b	Send	Send DE, HS, VS on second channel if enabled
01b	Reserved	
10b	Do not send	Do not send DE, HS, VS on second channel use zero instead
11b	DE 0	Use DE=0, HS=LE, VS=LF on second channel

LVDS_CTL

16 — Channel Reserved Bits

Value	Name	Description
0b	Send 0	Send 0 for the channel reserved bits
1b	Send Duplicate	Send duplicate data bit for reserved bits

15:11 — Reserved

10 — Buffer Power Down State

This bit selects the state of the LVDS buffers during a powered down state caused by the power sequence logic power down.
This selection will be made based on the connected panel requirements.

Value	Name	Description
0b	Zero	Zero Volts (Driven on both lines of the pairs)
1b	Tri-State	Tri-State (High impedance state)

9:8 — ClkA0 A2 Control

This field controls the A0-A2 data pairs and CLKA.
It sets the highest level of activity that is allowed on these lines when the panel is powered on.
Power sequencing for LVDS connected panels overrides the control. When the power sequencer is in the power down mode all signals are in the power down state.

Value	Name	Description
00b	Power Down	Power Down all A channel signals including A3 (0V)
01b	Power Up Data 0	Power up – A0, A1, A2 Data bits forced to 0,Timing active, Clock Active
10b	Reserved	
11b	Power Up All Active	Power up – Data lines and clock active

7:6 — Eight bit ch A3 B3 Control

This field can control both the A3 and B3 data pairs.
Enabling those pairs indicates the selection of 8-bit per color channel mode.
It sets the highest level of activity that is allowed on these lines when the panel is powered on.
The A3 pair will only be powered up if both this field and the A0, A1, A2, CLKA field indicates that the pair should be powered up and will only be active if both indicate that it should be active.
The B3 pair will only be powered up if both this field and the B0, B1, B2, (B3) field indicates that the pair should be powered up and will only be active if both indicate that it should be active.
Power sequencing for LVDS connected panels overrides the control. When the power sequencer is in the power down mode all signals are in the power down state.

Value	Name	Description
00b	Power Down	Power Down all signals A3, B3 (common mode)
01b	Power Up Data 0	Power up – A3, (B3) Data (pixel data not control) lines forced to 0 output
10b	Reserved	
11b	Power Up Data Active	Power up – A3, (B3) Data lines active

5:4 — Two channel mode ClkB Control

When in two channel mode, this field controls the CLKB pair.
It sets the highest level of activity that is allowed on these lines when the panel is powered on.
The CLKB pair should only be powered up if the B0, B1, B2, (B3) field indicates that the second channel should be powered up and will only be active if both indicate that it should be active.
Power sequencing for LVDS connected panels overrides the control.

Value	Name	Description
00b	Power Down	Power Down CLKB (common mode)
01b	Power Up CLKB 0	Power up – CLKB Forced to 0
10b	Reserved	
11b	Power Up CLKB Active	Power up – Clock B active

3:2 — Two channel mode B0 B2 Control

This field controls both the set B0-B2 data pairs.

LVDS_CTL		
		It sets the highest level of activity that is allowed on these lines when the panel is powered on. Power sequencing for LVDS connected panels overrides the control. During single channel operation (1x18.0), these bits need to be both zero. Two channel operation is selected by setting them to ones. The second clock can be optionally enabled or disabled by the two channel mode ClkB control field.

Value	Name	Description
00b	Power Down	Power Down all signals including B3 and CLKB
01b	Power Up Data 0	Power up – B0, B1, B2, Data lines forced to 0, timing is active
10b	Reserved	
11b	Power Up Data Active	Power up – Data lines active (color and timing)

	1	**Port Detected**

Access:	RO

Read-only bit indicating whether LVDS was detected during initialization. It signifies the level of the GMBUS port 2 (LVDS) data line at boot. This bit is valid regardless of whether the port is enabled.

Value	Name	Description
0b	Not Detected	LVDS not detected during initialization
1b	Detected	LVDS detected during initialization

	0	**Reserved**

3.8 DisplayPort

3.8.1 DP_CTL—DisplayPort Control

DP_CTL	
Register Space:	MMIO: 0/2/0
Project:	
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Depends on bit
Address:	E4100h-E4103h
Name:	DisplayPort B Control
ShortName:	DP_CTL_B
Address:	E4200h-E4203h
Name:	DisplayPort C Control
ShortName:	DP_CTL_C
Address:	E4300h-E4303h
Name:	DisplayPort D Control
ShortName:	DP_CTL_D

Port enable is write protected by Panel Power Sequencer when panel is connected to this port.
DisplayPort B uses the same physical pins as HDMI/DVI B. Therefore HDMI/DVI B and DisplayPort B cannot be

DP_CTL

enabled simultaneously. The same applies for ports C and D.

DWord	Bit	Description
0	31	**DisplayPort Enable** Disabling this port will put it in its lowest power state. Port enable takes place on the Vblank after being written.

Value	Name	Description
0b	Disable	Disable and tristate the DisplayPort interface
1b	Enable	Enable the DisplayPort interface

Programming Notes	Project
Workaround : When panel power sequencing is selected for DisplayPort D, the clock gating disable register SCLKGATE_DIS 0xC2020 bit 14 must be set to 1b prior to enabling DisplayPort D, then cleared to 0b after disabling DisplayPort D.	

	30:28	**Reserved**

Format:	MBZ

	27:25	**Voltage swing level set** These bits are used for setting the voltage swing for pattern 1, defined as Vdiff_pp in the DisplayPort specification.

Value	Name	Description
000b	0.4V	0.4V
001b	0.6V	0.6V
010b	0.8V	0.8V
011b	1.2V	1.2V
Others	Reserved	Reserved

	24:22	**Preemphasis level set** These bits are used for setting link pre-emphasis for pattern 2, as defined in the DisplayPort specification.

Value	Name	Description
000b	0dB	No pre-emphasis
001b	3.5dB	3.5dB pre-emphasis (1.5x)
010b	6dB	6dB pre-emphasis (2x)
011b	9.5dB	9.5dB pre-emphasis (3x)
Others	Reserved	Reserved

	21:19	**Port Width Selection** This bit selects the number of lanes to be enabled on the DisplayPort link. Port width change must be done as a part of mode set. Locked once port is enabled. Updates when the port is disabled then re-enabled.

Value	Name	Description
000b	x1	x1 Mode
001b	x2	x2 Mode
011b	x4	x4 Mode
Others	Reserved	Reserved

	18:16	**Reserved**

Format:	MBZ

	15	**Port reversal** Enables lane reversal within the port: lane 0 mapped to lane 3, lane 1 mapped to lane 2, etc. Port reversal does not affect AUX channel lane mapping. Locked once port is enabled. Updates when the port is disabled then re-enabled

Value	Name	Description

DP_CTL

	0b	Not Reversed	Port not reversed
	1b	Reversed	Port reversed

14:11 Reserved

Format:	MBZ

10:8 Link training pattern enable

These bits are used for link initialization as defined in the DisplayPort specification.
The link must first be configured prior to sending training patterns.

Value	Name	Description
000b	Pattern 1	Pattern 1 enabled
001b	Pattern 2	Pattern 2 enabled
010b	Idle	Idle Pattern enabled
011b	Normal	Link not in training: Send normal pixels
Others	Reserved	Reserved

Programming Notes

Restriction : When enabling the port, it must be turned on with pattern 1 enabled. When retraining, the port must be disabled, then re-enabled with pattern 1 enabled.

6 Audio Output Enable

This bit enables audio output on this port.
It may be enabled or disabled only when the link training is complete and set to "Normal".

Value	Name	Description
0b	Disable	Audio output disabled
1b	Enable	Audio output enabled

4:3 Reserved

Format:	MBZ

2 Port Detected

Access:	RO

Read-only bit indicating whether a digital display was detected during initialization.
It signifies the level of the detect pin (GMBUS port 4 for port B, GMBUS port 3 for port C, GMBUS port 5 for port D) at boot.
This bit is valid regardless of whether the port is enabled.

Value	Name	Description
0b	Not Detected	Digital display not detected during initialization
1b	Detected	Digital display detected during initialization

1:0 Reserved

Format:	MBZ

3.8.2 DP_AUX_CTL—DisplayPort AUX Channel Control

DP_AUX_CTL	
Register Space:	MMIO: 0/2/0
Project:	
Default Value:	0x00050000
Access:	R/W Special
Size (in bits):	32
Address:	E4110h-E4113h
Name:	DisplayPort B AUX Channel Control
ShortName:	DP_AUX_CTL_B
Address:	E4210h-E4213h
Name:	DisplayPort C AUX Channel Control
ShortName:	DP_AUX_CTL_C
Address:	E4310h-E4313h
Name:	DisplayPort D AUX Channel Control
ShortName:	DP_AUX_CTL_D

DWord	Bit	Description
0	31	**Send Busy** Setting this bit to a one initiates the transaction, when read this bit will be a 1 until the transmission completes. The transaction is completed when the response is received or when a timeout occurs. Do not write a 1 again until transaction completes. Writes of 0 will be ignored. **Value** / **Name** 0b – Not Busy 1b – Send or Busy **Programming Notes** Do not change any fields while Send/Busy bit 31 is asserted.
	30	**Done** Access: R/WC A sticky bit that indicates the transaction has completed. Write a 1 to this bit to clear the event. **Value** / **Name** 0b – Not done 1b – Done
	29	**Interrupt on Done** Enable an interrupt in the hotplug status register when the transaction completes or times out. **Value** / **Name** 0b – Enable 1b – Disable
	28	**Time out error** Access: R/WC A sticky bit that indicates the transaction has timed out. Write a 1 to this bit to clear the event. **Value** / **Name**

DP_AUX_CTL

0b	Not error
1b	Error

27:26 Time out timer value

Used to determine how long to wait for receiver response before timing out.

Value	Name	Description
00b	400us	400us
01b	600us	600us
10b	800us	800us
11b	1600us	1600us

25 Receive error

Access:	R/WC

A sticky bit that indicates that the data received was corrupted, not in multiples of a full byte, or more than 20 bytes.
Write a 1 to this bit to clear the event.

Value	Name
0b	Not error
1b	Error

24:20 Message Size

This field is used to indicate the total number bytes to transmit (including the header). It also indicates the number of bytes received in a transaction (including the header).
This field is valid only when the done bit is set, and if timeout or receive error has not occurred.
Sync/Stop are not part of the message or the message size.
Reads of this field will give the response message size. The read value will not be valid while Send/Busy bit 31 is asserted.
Message sizes of 0 or >20 are not allowed.

19:16 Precharge Time

Default Value:	0101b 10us

This field determines the precharge time for the Aux Channel drivers. During this time the Aux Channel will drive the SYNC pattern.
Every microsecond gives one additional SYNC pulse beyond the hard coded 26 SYNC pulses.
The value is the number of microseconds times 2.
Default is 5 decimal which gives 10us of precharge which is 10 extra SYNC pulses for a total of 36.
Example: For 10us precharge, program 5 (10us/2us).

10:0 2X Bit Clock divider

Used to determine the 2X bit clock the Aux Channel logic runs on.
This value divides the input clock frequency down to 2X bit clock rate.
For the 125 MHz input clock and desired 2MHz 2X bit clock, program 63 (125MHz/2MHz).

3.8.3 DP_AUX_DATA—DisplayPort AUX Channel Data

DP Aux Channel Data Format		
Project:		
Size (in bits):		32
Default Value:		0x00000000
DWord	**Bit**	**Description**
0	31:0	**AUX CH DATA** A DWord of the message. Writes give the data to transmit during the transaction. The MSbyte is transmitted first. Reads will give the response data after transaction complete.

DP_AUX_DATA		
Register Space:	MMIO: 0/2/0	
Project:		
Default Value:	0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	5x32	
Address:	E4114h-E4127h	
Name:	DisplayPort B AUX Channel Data	
ShortName:	DP_AUX_DATA_[1-5]_B	
Address:	E4214h-E4227h	
Name:	DisplayPort C AUX Channel Data	
ShortName:	DP_AUX_DATA_[1-5]_C	
Address:	E4314h-E4327h	
Name:	DisplayPort D AUX Channel Data	
ShortName:	DP_AUX_DATA_[1-5]_D	
The read value will not be valid while the DisplayPort Aux Channel Control Register Send/Busy bit is asserted.		

DWord	Bit	Description
0	31:0	**AUX CH DATA1** Format: DP Aux Channel Data Format
1	31:0	**AUX CH DATA2** Format: DP Aux Channel Data Format
2	31:0	**AUX CH DATA3** Format: DP Aux Channel Data Format
3	31:0	**AUX CH DATA4** Format: DP Aux Channel Data Format
4	31:0	**AUX CH DATA5** Format: DP Aux Channel Data Format

3.8.4 DP_BUFTRANS—DisplayPort Buffer Translation

DisplayPort Buffer Translation Format		
Project:		
Size (in bits):	32	
Default Value:	0x00000000	

DWord	Bit	Description
0	31:28	**Reserved** Format: MBZ
	27:19	**OE** These bits select the OE vswing level Value: [0,511] — Name:
	18:17	**Reserved** Format: MBZ
	16:12	**Pre Emphasis** These bits select the pre-emphasis level Value: [0,31] — Name:
	11:10	**Reserved** Format: MBZ
	9:6	**P current drive** These bits select the P current drive value Value: [0,15] — Name:
	5:4	**Reserved** Format: MBZ
	3:0	**N current drive** These bits select the N current drive value Value: [0,15] — Name:

Programming Requirements:

DP mode		Offset	Value
L1	0dB	0xE4F00	**0x0100030C**
L1	3.5dB	0xE4F04	**0x00B8230C**
L1	6dB	0xE4F08	**0x06F8930C**
L1	9.5dB	0xE4F0C	**0x05F8E38E**
L2	0dB	0xE4F10	**0x00B8030C**
L2	3.5dB	0xE4F14	**0x0B78830C**

DP mode		Offset	Value
L2	6dB	0xE4F18	**0x09F8D3CF**
L3	0dB	0xE4F1C	**0x01E8030C**
L3	3.5dB	0xE4F20	**0x09F863CF**
L4	0 dB	0xE4F24	**0x0FF803CF**

Vswing	0dB pre-emphasis	3.5dB pre-emphasis	6dB pre-emphasis	9.5dB pre-emphasis
400mV	DWord 0	DWord 1	DWord 2	DWord 3
600mV	DWord 4	DWord 5	Dword 6	Not supported
800mV	Dword 7	Dword 8	Not supported	Not supported
1200mV	Dword 9	Not supported	Not supported	Not supported

DP_BUFTRANS

Register Space:	MMIO: 0/2/0
Project:	
Default Value:	0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000
Access:	R/W
Size (in bits):	10x32

Address:	E4F00h-E4F27h
Name:	DP Buffer Translation
ShortName:	DP_BUFTRANS_[0-9]

These registers define current drive, pre-emphasis and voltage swing buffer programming required for the different voltage swing and pre-emphasis settings in the DisplayPort Control.
The default values are not the optimal values. See the programming notes for the correct values to use.

DWord	Bit	Description
0	31:0	**Vswing400mV Pre0.0dB** Default Value: 0100038Eh Format: DisplayPort Buffer Translation Format **Programming Notes** Recommended programming is 0100_030Ch
1	31:0	**Vswing400mV Pre3.5dB** Default Value: 00B8338Eh

DP_BUFTRANS			
		Format:	DisplayPort Buffer Translation Format
		Programming Notes	
		Recommended programming is 00B8_230Ch	
2	31:0	**Vswing400mV Pre6.0dB**	
		Default Value:	0178838Eh
		Format:	DisplayPort Buffer Translation Format
		Programming Notes	
		Recommended programming is 06F8_930Ch	
3	31:0	**Vswing400mV Pre9.5dB**	
		Default Value:	09F8E38Eh
		Format:	DisplayPort Buffer Translation Format
		Programming Notes	
		Recommended programming is 05F8_E38Eh	
4	31:0	**Vswing600mV Pre0.0dB**	
		Default Value:	00B8038Eh
		Format:	DisplayPort Buffer Translation Format
		Programming Notes	
		Recommended programming is 00B8_030Ch	
5	31:0	**Vswing600mV Pre3.5dB**	
		Default Value:	0978838Eh
		Format:	DisplayPort Buffer Translation Format
		Programming Notes	
		Recommended programming is 0B78_830Ch	
6	31:0	**Vswing600mV Pre6.0dB**	
		Default Value:	09F8B38Eh
		Format:	DisplayPort Buffer Translation Format
		Programming Notes	
		Recommended programming is 09F8_D3CFh	
7	31:0	**Vswing800mV Pre0.0dB**	
		Default Value:	0178038Eh
		Format:	DisplayPort Buffer Translation Format
		Programming Notes	
		Recommended programming is 01E8_030Ch	
8	31:0	**Vswing800mV Pre3.5dB**	
		Default Value:	09F8638Eh
		Format:	DisplayPort Buffer Translation Format

<table>
<tr><th colspan="3">DP_BUFTRANS</th></tr>
<tr><td></td><td></td><td><table><tr><th>Programming Notes</th></tr><tr><td>Recommended programming is 09F8_63CFh</td></tr></table></td></tr>
<tr><td>9</td><td>31:0</td><td>Vswing1200mV Pre0.0dB<table><tr><td>Default Value:</td><td>09F8038Eh</td></tr><tr><td>Format:</td><td>DisplayPort Buffer Translation Format</td></tr></table><table><tr><th>Programming Notes</th></tr><tr><td>Recommended programming is 0FF8_03CFh</td></tr></table></td></tr>
</table>

4. South Display Engine Audio

4.1 Audio Programming Sequence

The following HDMI and DisplayPort audio programming sequences are for use when enabling or disabling audio or temporarily disabling audio during a display mode set.

The audio codec and audio controller disable sequences must be followed prior to disabling the transcoder or port in a display mode set.

The audio codec and controller enable sequences can be followed after the transcoder is enabled and the port is enabled and completed link training (not sending TP1, TP2, or Idle).

The audio controller and audio codec sequences may be done in parallel or serial. In general, the change in ELDV/PD in the codec sequence will generate an unsolicited response to the audio controller driver to indicate that the controller sequence should start, but other mechanisms may be used.

Audio codec disable sequence:

Disable sample fabrication

- Set AUD_MISC_CTRL Sample_Fabrication_EN (bit 2) to “0”.
- Disable timestamps
- Set AUD_CONFIG N_value_index (bit 29) to "0" for HDMI or "1" for DisplayPort.
- Set N_programming_enable (bit 28) to "1"
- Set Upper_N_value and Lower_N_value (bits 28:20, 15:4) to all "0"s.

Disable ELDV and ELD buffer

- Set AUD_CNTRL_ST2 ELD_valid (bit 0, 4, or 8 based on which port is used) to "0"
- Wait for 2 vertical blanks

Optional: Disable audio PD (Presence Detect)

- Software may choose to skip this in order to keep PD enabled during a resolution switch.
- Set the port control register (HDMI_CTL or DP_CTL) Audio_Output_Enable (bit 6) to "0".

Audio controller disable sequence:

Program Stream ID to 0 – Verb ID 706

Disable audio info frames transmission – Verb ID 732

Disable Digen – Verb ID 70D

Program the codec to D3 state if needed.

Audio driver may stop the audio controller DMA engine at this point if needed, but not required.

Audio codec enable sequence:

- Enable audio Presence Detect
- Set the port control register (HDMI_CTL or DP_CTL) Audio_Output_Enable (bit 6) to "1".
- Wait for 1 vertical blank
- Load ELD buffer and Enable ELDV
- Set AUD_CNTRL_ST2 ELD_valid (bit 0, 4, or 8 based on which port is used) to "1".
- Enable timestamps
- Set AUD_CONFIG N_value_index (bit 29) to "0" for HDMI or "1" for DisplayPort.
- Set N_programming_enable (bit 28) to "0".
    - Program Upper_N_value and Lower_N_value (bits 28:20, 15:4) if a non-default N value is needed.
- Enable sample fabrication if this feature is needed
- Set AUD_MISC_CTRL Sample_Fabrication_EN (bit 2) to “1”.

Audio controller enable sequence:

Program the codec to D0 state if in D3 state.

Program Stream ID to non zero – Verb ID 706

Enable audio info frames transmission – Verb ID 732

Enable Digen – Verb ID 70D

If audio controller DMA engine is stopped, audio driver can start the DMA engine at this point.

4.2 Audio Configuration

4.2.1 AUD_CONFIG—Audio Configuration

AUD_CONFIG		
Register Space:		MMIO: 0/2/0
Project:		
Default Value:		0x00000000
Access:		R/W
Size (in bits):		32
Address:	E5000h-E5003h	
Name:	Audio Configuration Transcoder A	
ShortName:	AUD_CONFIG_A	
Address:	E5100h-E5103h	
Name:	Audio Configuration Transcoder B	
ShortName:	AUD_CONFIG_B	
Address:	E5200h-E5203h	
Name:	Audio Configuration Transcoder C	
ShortName:	AUD_CONFIG_C	

This register configures the audio output.

DWord	Bit	Description
0	31:30	**Reserved**
	29	**N value Index** Value / Name / Description 0b / HDMI / N value read on bits 27:20 and 15:4 reflects HDMI N value. Bits 27:20 and 15:4 are programmable to any N value – default h7FA6. 1b / DisplayPort / N value read on bits 27:20 and 15:4 reflects DisplayPort N value. Set this bit to 1 before programming N value register. When this bit is set to 1, 27:20 and 15:4 will reflect the current N value – default h8000.
	28	**N programming enable** This bit enables programming of N values for non-CEA modes. Please note that the Transcoder to which audio is attached must be disabled when changing this field.
	27:20	**Upper N value** These are bits [19:12] of programmable N values for non-CEA modes. Bit 29 of this register must also be written in order to enable programming. Please note that the Transcoder to which audio is attached must be disabled when changing this field. This register can also be used to program N value for DisplayPort for a specific Port. Default value for N when bit 29 is set to 0 is h7FA6
	19:16	**Pixel Clock HDMI** This is the target frequency of the CEA/HDMI video mode to which the audio stream is added. This value is used for generating N_CTS packets. This refers to only HDMI Pixel clock and does not refer to DisplayPort Link clock. DisplayPort Link clock does not require this programming. Note: The Transcoder on which audio is attached must be disabled when changing this field. Value / Name / Description

AUD_CONFIG				
		0000b	25.2 / 1.001 MHz	25.2 / 1.001 MHz
		0001b	25.2 MHz	25.2 MHz (Program this value for pixel clocks not listed in this field)
		0010b	27 MHz	27 MHz
		0011b	27 * 1.001 MHz	27 * 1.001 MHz
		0100b	54 MHz	54 MHz
		0101b	54 * 1.001 MHz	54 * 1.001 MHz
		0110b	74.25 / 1.001 MHz	74.25 / 1.001 MHz
		0111b	74.25 MHz	74.25 MHz
		1000b	148.5 / 1.001 MHz	148.5 / 1.001 MHz
		1001b	148.5 MHz	148.5 MHz
		Others	Reserved	Reserved
	15:4	**Lower N value** These are bits [11:0] of programmable N values for non-CEA modes. Bit 29 of this register must also be written in order to enable programming. Please note that the Transcoder to which audio is attached must be disabled when changing this field. This register can also be used to program N value for DisplayPort for a specific Port. Default value for N when bit 29 is set to 0 is h7FA6		
	2:0	**Reserved**		

4.2.2 AUD_CTS_ENABLE – Audio CTS Programming Enable

AUD_CTS_ENABLE				
Register Space:			MMIO: 0/2/0	
Project:				
Default Value:			0x00000000	
Access:			RO	
Size (in bits):			32	
Address:	E5028h-E502Bh			
Name:	Audio CTS Programming Enable Transcoder A			
ShortName:	AUD_CTS_ENABLE_A			
Address:	E5128h-E512Bh			
Name:	Audio CTS Programming Enable Transcoder B			
ShortName:	AUD_CTS_ENABLE_B			
Address:	E5228h-E522Bh			
Name:	Audio CTS Programming Enable Transcoder C			
ShortName:	AUD_CTS_ENABLE_C			
These values are returned from the device as the Subordinate Node Count response to a Get Root Node command.				
DWord	**Bit**	**Description**		
0	31:22	**Reserved**		
	21	**CTS M value Index**		
		Value	**Name**	**Description**
		0b	CTS	CTS value read on bits 23:4 reflects CTS value. Bit 23:4 is programmable to any CTS

AUD_CTS_ENABLE				
				value. default is 0
		1b	M	M value read on bits 21:4 reflects DisplayPort M value. Set this bit to 1 before programming M value register. When this is set to 1 23:4 will reflect the current N value
	20	**Enable CTS or M programming** When set will enable CTS or M programming.		
	19:0	**CTS programming** These are bits [19:0] of programmable CTS values for non-CEA modes. Bit 21 of this register must also be written in order to enable programming. Please note that the Transcoder to which audio is attached must be disabled when changing this field.		

4.2.3 AUD_MISC_CTRL—Audio MISC Control

AUD_MISC_CTRL		
Register Space:		MMIO: 0/2/0
Project:		
Default Value:		0x00000040
Access:		RO
Size (in bits):		32
Address:	E5010h-E5013h	
Name:	Audio Misc Control Converter A	
ShortName:	AUD_MISC_CTRL_A	
Address:	E5110h-E5113h	
Name:	Audio Misc Control Converter B	
ShortName:	AUD_MISC_CTRL_B	
Address:	E5210h-E5213h	
Name:	Audio Misc Control Converter C	
ShortName:	AUD_MISC_CTRL_C	

DWord	Bit	Description
0	31:9	**Reserved** Format: MBZ
	7:4	**Output Delay** Default Value: 0100b 4 samples The number of samples between when the sample is received and when it appears as an analog signal at the pin.
	3	**Reserved** Format: MBZ
	2	**Sample Fabrication EN bit** Access: R/W This bit indicates whether internal fabrication of audio samples is enabled during a link underrun.

Value	Name	Description
0b	Disable	Audio fabrication disabled

AUD_MISC_CTRL				
		1b	Enable	Audio fabrication enabled
	0	**Reserved**		
		Format:		MBZ

4.2.4 AUD_VID_DID—Audio Vendor ID / Device ID

AUD_VID_DID				
Register Space:				MMIO: 0/2/0
Project:				
Default Value:				0x80862805
Access:				RO
Size (in bits):				32
Address:		E5020h-E5023h		
Name:		Audio Vendor ID / Device ID		
ShortName:		AUD_VID_DID		
These values are returned from the device as the Vendor ID/ Device ID response to a Get Root Node command.				
DWord	**Bit**	**Description**		
0	31:16	**Vendor ID**		
		Default Value:		8086h
		Used to identify the codec within the PnP system. This field is hardwired within the device.		
	15:0	**Device ID**		
		Constant used to identify the codec within the PnP system. This field is set by the device hardware.		
		Value	**Name**	**Description** / **Project**
		2805h	**[Default]**	Cougarpoint
		2806h	**[Default]**	Pantherpoint

4.2.5 AUD_RID—Audio Revision ID

AUD_RID		
Register Space:		MMIO: 0/2/0
Project:		
Default Value:		0x00000000
Access:		RO
Size (in bits):		32
Address:	E5024h-E5027h	
Name:	Audio Revision ID	
ShortName:	AUD_RID	

AUD_RID

These values are returned from the device as the Revision ID response to a Get Root Node command.

DWord	Bit	Description
0	31:24	**Reserved**
	15:8	**Revision ID** The vendor's revision number for this given Device ID. This field is hardwired within the device. Value: 00000000b Name:
	7:0	**Stepping ID** An optional vendor stepping number within the given Revision ID. This field is hardwired within the device. Value: 00000000b Name:

4.2.6 AUD_PWRST—Audio Power State

Audio Power State Format

Project:

Size (in bits): 2

Default Value: 0x00000003

DWord	Bit	Description		
0	1:0	**Power State**		
		Value	**Name**	**Description**
		00b	D0	D0
		01b,10b	Unsupported	Unsupported
		11b	D3 **[Default]**	D3

AUD_PWRST

Register Space: MMIO: 0/2/0

Project:

Default Value: 0x0FFFFFFF

Access: RO

Size (in bits): 32

Address: E504Ch-E504Fh

Name: Audio Power State

ShortName: AUD_PWRST

These values are returned from the device as the Power State response to a Get Audio Function Group command.

DWord	Bit	Description
0	31:28	**Reserved**
	27:26	**Func Grp Dev PwrSt Curr** Format: Audio Power State Format

AUD_PWRST

		Function Group Device current power state
	25:24	**Func Grp Dev PwrSt Set** Format: Audio Power State Format Function Group Device power state that was set
	23:22	**ConvC Widget PwrSt Curr** Format: Audio Power State Format ConverorC Widget current power state
	21:20	**ConvC Widget PwrSt Req** Format: Audio Power State Format ConverorC Widget power state that was requested by audio software
	19:18	**ConvertorB Widget PwrSt Curr** Format: Audio Power State Format ConverorB Widget current power state
	17:16	**ConvertorB Widget PwrSt Req** Format: Audio Power State Format ConverorB Widget power state that was requested by audio software
	15:14	**ConvertorA Widget PwrSt Curr** Format: Audio Power State Format ConverorA Widget current power state
	13:12	**ConvertorA Widget PwrSt Req** Format: Audio Power State Format ConverorA Widget power state that was requested by audio software
	11:10	**PinD Widget PwrSt Curr** Format: Audio Power State Format PinD Widget current power state
	9:8	**PinD Widget PwrSt Set** Format: Audio Power State Format PinD Widget power state that was set
	7:6	**PinC Widget PwrSt Curr** Format: Audio Power State Format PinC Widget current power state
	5:4	**PinC Widget PwrSt Set** Format: Audio Power State Format PinC Widget power state that was set
	3:2	**PinB Widget PwrSt Curr** Format: Audio Power State Format

AUD_PWRST		
		PinB Widget current power state
	1:0	**PinB Widget PwrSt Set** Format: Audio Power State Format PinB Widget power state that was set

4.2.7 AUD_PINW_CONNLNG_LIST—Audio Connection List

AUD_PINW_CONNLNG_LIST		
Register Space:		MMIO: 0/2/0
Project:		
Default Value:		0x00000302
Access:		RO
Size (in bits):		32
Address:	E50A8h-E50ABh	
Name:	Audio Connection List	
ShortName:	AUD_PINW_CONNLNG_LIST	

These values are returned from the device as the Connection List Length response to a Get Pin Widget command.

DWord	Bit	Description
0	31:16	**Reserved**
	15:8	**Connection List Entry** Default Value: 03h 0x03 Connection to Convertor Widget Node 0x03
	7	**Long Form** This bit indicates whether the items in the connection list are ‘long form’ or ‘short form’. This bit is hardwired to 0 (items in connection list are short form)
	6:0	**Connection List Length** Default Value: 02h 0x02 This field indicates the number of items in the connection list. If this field is 2, there is only one hardwired input possible, which is read from the Connection List, and there is no Connection Select Control.

4.2.8 AUD_PINW_CONNLNG_SEL—Audio Connection Select

AUD_PINW_CONNLNG_SEL		
Register Space:		MMIO: 0/2/0
Project:		
Default Value:		0x00000000
Access:		RO
Size (in bits):		32
Address:	E50ACh-E50AFh	
Name:	Audio Connection Select	
ShortName:	AUD_PINW_CONNLNG_SEL	

These values are returned from the device as the Connection List Length response to a Get Pin Widget command.

DWord	Bit	Description
0	31:24	**Reserved**
	23:16	**Connection select Control D** Connection Index Currently Set [Default 0x00], Port D Widget is set to 0x00
	15:8	**Connection select Control C** Connection Index Currently Set [Default 0x00], Port C Widget is set to 0x00
	7:0	**Connection select Control B** Connection Index Currently Set [Default 0x00], Port B Widget is set to 0x00

4.2.9 AUD_CNTL_ST—Audio Control State

AUD_CNTL_ST		
Register Space:		MMIO: 0/2/0
Project:		
Default Value:		0x00005400
Access:		R/W
Size (in bits):		32
Address:	E50B4h-E50B7h	
Name:	Audio Control State Transcoder A	
ShortName:	AUD_CNTL_ST_A	
Address:	E51B4h-E51B7h	
Name:	Audio Control State Transcoder B	
ShortName:	AUD_CNTL_ST_B	
Address:	E52B4h-E52B7h	
Name:	Audio Control State Transcoder C	
ShortName:	AUD_CNTL_ST_C	

DWord	Bit	Description	
0	31	**Reserved**	
		Format:	MBZ

AUD_CNTL_ST

30:29 DIP Port Select

Access:	RO

This read-only bit reflects which port is used to transmit the DIP data. This can only change when DIP is disabled. If one or more audio-related DIP packets is enabled and audio is enabled on a digital port, these bits will reflect the digital port to which audio is directed.

Value	Name	Description
00b	Reserved	Reserved
01b	Digital Port B	Digital Port B
10b	Digital Port C	Digital Port C
11b	Digital Port D	Digital Port D

28:25 Reserved

Format:	MBZ

24:21 DIP type enable status

Access:	RO

These bits reflect the DIP types enabled. It can be updated while the port is enabled. Within 2 vblank periods, the DIP is guaranteed to have been transmitted. Disabling a DIP type results in setting the contents of that DIP buffer to zero. A reserved setting reflects a disabled DIP.

Value	Name	Description
XXX0b	Disable	Audio DIP disabled
XXX1b	Enable	Audio DIP enabled
XX0Xb	Disable	Generic 1 (ACP) DIP disabled
XX1Xb	Enable	Generic 1 (ACP) DIP enabled
X0XXb	Disable	Generic 2 DIP disabled
X1XXb	Enable	Generic 2 DIP enabled, can be used by ISRC1 or ISRC2
1XXXb	Reserved	Reserved

20:18 DIP buffer index

This field is used during read of different DIPs, and during read or write of ELD data. These bits are used as an index to their respective DIP or ELD buffers. When the index is not valid, the contents of the DIP will return all 0's.

Value	Name	Description
000b	Audio	Audio DIP (31 bytes of address space, 31 bytes of data)
001b	Gen 1	Generic 1 (ACP) Data Island Packet (31 bytes of address space, 31 bytes of data)
010b	Gen 2	Generic 2 (ISRC1) Data Island Packet (31 bytes of address space, 31 bytes of data)
011b	Gen 3	Generic 3 (ISRC2) Data Island Packet (31 bytes of address space, 31 bytes of data)
Others	Reserved	Reserved

17:16 DIP transmission frequency

Access:	RO

These bits reflect the frequency of DIP transmission for the DIP buffer type designated in bits 20:18. When writing DIP data, this value is also latched when the first DW of the DIP is written.
When read, this value reflects the DIP transmission frequency for the DIP buffer designated in bits 20:18.

Value	Name	Description
00b	Disable	Disabled
01b	Reserved	Reserved
10b	Send Once	Send Once
11b	Best Effort	Best effort (Send at least every other vsync)

15 Reserved

Format:	MBZ

14:10 ELD buffer size

AUD_CNTL_ST		
	Default Value:	10101b 84 Bytes of ELD
	Access:	RO
	This field reflects the size of the ELD buffer in DWORDs	
9:5	**ELD access address** Selects the DWORD address for access to the ELD buffer (84 bytes). The value wraps back to zero when incremented past the max addressing value 0x1F. This field change takes effect immediately after being written. The read value indicates the current access address.	
4	**ELD ACK** Acknowledgement from the audio driver that ELD read has been completed	
3:0	**DIP access address** Selects the DWORD address for access to the DIP buffers. The value wraps back to zero when it incremented past the max addressing value of 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.	

4.2.10 AUD_CNTRL_ST2— Audio Control State 2

AUD_CNTRL_ST2		
Register Space:		MMIO: 0/2/0
Project:		
Default Value:		0x00000000
Access:		R/W
Size (in bits):		32
Address:	E50C0h-E50C3h	
Name:	Audio Control State 2	
ShortName:	AUD_CNTRL_ST2	

This register is used for handshaking between the audio and video drivers for interrupt management.
Display software sets these bits as part of enabling the respective audio-enabled digital port.
For each port, ELD readiness is sent by the display software to the audio software via an unsolicited response when the ELD ready bit is set.

DWord	Bit	Description
0	31:10	**Reserved**
	8	**ELD validD** This R/W bit reflects the state of the ELD data written to the ELD RAM. After writing the ELD data, the video software must set this bit to 1 to indicate that the ELD data is valid. At audio codec initialization, or on a hotplug event, this bit is set to 0 by the video software. This bit is reflected in the audio pin complex widget as the ELD valid status bit.
		Value / **Name** / **Description** 0b / Invalid / ELD data invalid (default, when writing ELD data, set 0 by software) 1b / Valid / ELD data valid (Set by video software only)
	7:6	**Reserved**
	4	**ELD validC** See ELD_validD descripion.
		Value / **Name** / **Description**

AUD_CNTRL_ST2				
		0b	Invalid	ELD data invalid (default, when writing ELD data, set 0 by software)
		1b	Valid	ELD data valid (Set by video software only)
	3:2	**Reserved**		
	0	**ELD validB** See ELD_validD descripion.		
		Value	**Name**	**Description**
		0b	Invalid	ELD data invalid (default, when writing ELD data, set 0 by software)
		1b	Valid	ELD data valid (Set by video software only)

4.2.11 AUD_HDMIW_HDMIEDID—Audio HDMI Data EDID Block

AUD_HDMIW_HDMIEDID	
Register Space:	MMIO: 0/2/0
Project:	
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	E5050h-E5053h
Name:	Audio HDMI Data EDID Block Transcoder A
ShortName:	AUD_HDMIW_HDMIEDID_A
Address:	E5150h-E5153h
Name:	Audio HDMI Data EDID Block Transcoder B
ShortName:	AUD_HDMIW_HDMIEDID_B
Address:	E5250h-E5253h
Name:	Audio HDMI Data EDID Block Transcoder C
ShortName:	AUD_HDMIW_HDMIEDID_C

These registers contain the HDMI data block from the EDID. The graphics driver reads the EDID and writes the structure to these registers. The vendor specific data block may be longer than 8 bytes, but the driver must not write more than 48 bytes to the buffer. The EDID format is Version 3 within the CEA-861B specification. The HDMI Vendor Specific Data Block is described in version 1.1 of the HDMI specification.

These values are returned from the device as the HDMI Vendor Specific Data Block response to a Get HDMI Widget command.

Writing sequence:

- Video software sets ELD invalid, and sets the ELD access address to 0, or to the desired DWORD to be written.
- Video software writes ELD data 1 DWORD at a time. The ELD access address autoincrements with each DWORD write, wrapping around to address 0 when the max buffer address size of 0xF has been reached. Please note that software must write an entire DWORD at a time.
- Please note that the audio driver checks the valid bit with each byte read of the ELD. This means that the video driver can unilaterally write ELD irrespective of audio driver ELD read status.

Reading sequence:

- Video software sets the ELD access address to 0, or to the desired DWORD to be read.
- Video software reads ELD data 1 DWORD at a time. The ELD access address autoincrements with each DWORD

AUD_HDMIW_HDMIEDID		
read, wrapping around to address 0 when the max buffer address size of 0xF has been reached.		
DWord	**Bit**	**Description**
0	31:0	**EDID HDMI Data Block** Please note that the contents of this buffer are not cleared when ELD is disabled. The contents of this buffer are cleared during gfx reset

4.2.12 AUD_HDMIW_INFOFR—Audio Widget Data Island Packet

AUD_HDMIW_INFOFR	
Register Space:	MMIO: 0/2/0
Project:	
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	E5054h-E5057h
Name:	Audio Widget Data Island Packet Transcoder A
ShortName:	AUD_HDMIW_INFOFR_A
Address:	E5154h-E5157h
Name:	Audio Widget Data Island Packet Transcoder B
ShortName:	AUD_HDMIW_INFOFR_B
Address:	E5254h-E5257h
Name:	Audio Widget Data Island Packet Transcoder C
ShortName:	AUD_HDMIW_INFOFR_C

When the IF type or dword index is not valid, the contents of the DIP will return all 0's.
These values are programmed by the audio driver in an HDMI Widget Set command.
To fetch a specific byte, the audio driver should send an HDMI Widget HDMI DIP Index Pointer Set command to set the index, then fetch the indexed byte using the HDMI DIP get.
Video software reads DIP data 1 DWORD at a time.
The DIP access address auto increments with each DWORD write, wrapping around to address 0 when the max buffer address size of 0xF has been reached.

DWord	Bit	Description
0	31:0	**Data Island Packet Data** This reflects the contents of the DIP indexed by the DIP access address. The contents of this buffer are cleared during function reset.

5. South Display Engine Transcoder and FDI Control

5.1 Transcoder Control

5.1.1 TRANS_CONF—Transcoder Configuration

TRANS_CONF	
Register Space:	MMIO: 0/2/0
Project:	
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank OR transcoder disabled
Address:	F0008h-F000Bh
Name:	Transcoder A Config
ShortName:	TRANS_CONF_A
Address:	F1008h-F100Bh
Name:	Transcoder B Config
ShortName:	TRANS_CONF_B
Address:	F2008h-F200Bh
Name:	Transcoder C Config
ShortName:	TRANS_CONF_C

DWord	Bit	Description
0	31	**Transcoder Enable** Setting this bit to the value of one, turns on the transcoder. Turning the transcoder off disables the timing generator and synchronization pulses to the display will not be maintained. Transcoder timing registers must contain valid values before this bit is enabled.

Value	Name	Description
0b	Disable	Disabled
1b	Enable	Enabled

Programming Notes
Workaround : Set timing override (transcoder A 0xF0064, transcoder B 0xF1064, transcoder C 0xF2064) bit 31 = 1 prior to enabling the transcoder. Clear timing override (transcoder A 0xF0064, transcoder B 0xF1064, transcoder C 0xF2064) bit 31 = 0 after disabling the transcoder.

DWord	Bit	Description
	30	**Transcoder State** This read only bit indicates the actual state of the transcoder.

Value	Name	Description
0b	Disabled	Transcoder is disabled

TRANS_CONF				
		1b	Enabled	Transcoder is enabled
	29:24	**Reserved**		
	23:21	**Interlaced Mode** These bits are used for control of the transcoder interlaced mode.		
		Value	**Name**	**Description**
		000b	Progressive	Progressive
		011b	Interlaced	Interlaced (north display must also be set to interlaced)
		Others	Reserved	
	20:11	**Reserved**		
	10	**xvYCC Color Range Limit** This bit is used to limit the color range of the port outputs from 1 to 254 for 8-bit components, 4 to 109 for 10-bit components, or 16 to 4079 for 12-bit components. Values outside of the range will be clamped to fit within the range. There is no need to set this bit if the equivalent bit is set in the north display pipe configuration register.		
		Value	**Name**	**Description**
		0b	Full	Do not limit the range
		1b	Limit	Limit range
	9:0	**Reserved**		

5.2 FDI Receiver

5.2.1 FDI_RX_CTL— FDI Rx Control

FDI_RX_CTL		
Register Space:		MMIO: 0/2/0
Project:		
Default Value:		0x00000040
Access:		R/W
Size (in bits):		32
Double Buffer Update Point:		Depends on bit
Address:	F000Ch-F000Fh	
Name:	FDI A RX Control	
ShortName:	FDI_RX_CTL_A	
Address:	F100Ch-F100Fh	
Name:	FDI B RX Control	
ShortName:	FDI_RX_CTL_B	
Address:	F200Ch-F200Fh	
Name:	FDI C RX Control	
ShortName:	FDI_RX_CTL_C	

DWord	Bit	Description

FDI_RX_CTL

0 — 31 — FDI Rx Enable

Disabling this port will put it in its lowest power state.

Value	Name	Description
0b	Disable	Disable the FDI Rx interface
1b	Enable	Enable the FDI Rx interface

Programming Notes	Project
Restriction : IF FDI polarity is reversed, set FDI Polarity Reversal (transcoder A 0xF0064, transcoder B 0xF1064, transcoder C 0xF2064) bit 29 = 1 prior to enabling FDI Rx.	
Restriction : FDIC can only be enabled if FDIB is never used.	
Workaround : 0xC2000 bit #12 must be programmed correctly prior to enabling FDIB or FDIC and cannot be changed after enabling either FDIB or FDIC. If 0xC2000 bit #12 = 0: Only FDIB can be used. FDIC cannot be used. FDIB can use up to 4 lanes. If 0xC2000 bit #12 = 1: Both FDIB and FDIC can be used. FDIB can use up to 2 lanes and FDIC can use up to 2 lanes. It is recommended to select this when using FDIB in 1 or 2 lane modes, even if FDIC will not be used at that time, so that if FDIC is later enabled it will not be necessary to disable FDIB and change the 0xC2000 setting.	

30:28 — Reserved

Format:	MBZ

27 — FS error correction enable

This bit enables the Fill Start error correction over FDI.
Once the FS code is incorrectly received, the receiver will recover the FS code.
The FDI Rx TU size register must be set correctly and the following condition must be met in order to set this bit: (Active+2)/TU >= 1

Value	Name	Description
0b	Disable	Disable FS Error Correction
1b	Enable	Enable FS Error Correction

26 — FE error correction enable

This bit enables the Fill End error correction over FDI.

Value	Name	Description
0b	Disable	Disable FE Error Correction
1b	Enable	Enable FE Error Correction

25 — FS error reporting enable

This bit enables the FS error reporting over FDI.

Value	Name	Description
0b	Disable	Disable FS Error Reporting
1b	Enable	Enable FS Error Reporting

24 — FE error reporting enable

This bit enables the FE error reporting over FDI.

Value	Name	Description
0b	Disable	Disable FE Error Reporting
1b	Enable	Enable FE Error Reporting

23:22 — Reserved

21:19 — Port Width Selection

These bits select the number of lanes to be enabled on the link.
Port width change must be done as a part of mode set.

FDI_RX_CTL

Locked once port is enabled. Updates when the port is disabled then re-enabled

Value	Name	Description
000b	x1 Mode	x1 Mode
001b	x2 Mode	x2 Mode
010b	x3 Mode	x3 Mode
011b	x4 Mode	x4 Mode
Others	Reserved	

Programming Notes

Restriction : FDI B and FDI C share lanes.
FDI C maximum port width is 2 lanes.
FDI B maximum port width is 4 lanes when FDI C is disabled, 2 lanes when FDI C is enabled.

18:16 **Bits Per Color**

This field selects the number of bits per color sent over the link.
Color format takes place on the Vblank after being written.

Value	Name	Description
000b	8 bpc	8 bits per color
001b	10 bpc	10 bits per color
010b	6 bpc	6 bits per color
011b	12 bpc	12 bits per color
Others	Reserved	Reserved

15 **Link reversal strap override**

By default, link is reversed if DMI is reversed according to the DMI reversal strap. This bit can be set to override FDI to use the reverse of what is strapped for DMI.
All FDI links must be off in order for this bit to take effect.
This bit is ORed with the link reversal strap overrides from any other FDI Rx Control registers.

Value	Name	Description
0b	Not Overwritten	Link reversal strap not overwritten
1b	Overwritten	Link reversal strap overwritten.

14 **DMI Link reversal status**

Access:	RO

This bit reflects the DMI link reversal strap.

Value	Name	Description
0b	Not Reversed	Link not reversed
1b	Reversed	Link reversed.

13 **FDI PLL enable**

Format:	Enable

This bit enables the FDI PLL.
This bit is ORed with the FDI PLL enables from any other FDI Rx Control registers.

Programming Notes

Restriction : After enabling the FDI PLL, software must wait for a warmup period before enabling the link.

12 **Reserved**

11 **Composite Sync Select**

This bit selects between composite Sync and separate Fsync/Lsync on this port.
This bit is ORed with the composite sync select from any other FDI Rx Control registers.

Value	Name	Description
0b	Separate	Separate Fsync/Lsync

1b	Composite	Composite Sync

Programming Notes

Restriction : Composite sync can only be used if the CPU display supports it.

FDI A can use either separate sync or composite sync. FDI A must use composite sync when FDI C is enabled.
FDI B can use either separate sync or composite sync. FDI B must use composite sync when FDI C is enabled.
FDI C can only use composite sync.

It is recommended to always use composite sync when the CPU display supports it, even when just using FDI A or FDI B, so that FDI C can be enabled later without needing to temporarily disable FDI A and FDI B in order to change them to composite.

10 **FDI Auto Train**

This bit enables FDI auto-training on this port.
Locked once port is enabled. Updates when port is disabled.

Value	Name	Description
0b	Disable	Disable FDI auto-training
1b	Enable	Enable FDI auto-training

9:8 **Link training pattern enable**

These bits are used for link initialization.

Value	Name	Description
00b	Pattern 1	Pattern 1 enabled
01b	Pattern 2	Pattern 2 enabled
10b	Idle	Idle Pattern enabled
11b	Normal	Link not in training: Send normal pixels

Programming Notes

Restriction : When enabling the port, it must be turned on with pattern 1 enabled. When retraining, the port must be disabled, then re-enabled with pattern 1 enabled.

6 **Enhanced Framing Enable**

This bit selects enhanced framing.
Locked once port is enabled. Updates when the port is disabled then re-enabled

Value	Name	Description
0b	Disable	Enhanced framing disabled
1b	Enable **[Default]**	Enhanced framing enabled

4 **Rawclk to PCDCLK selection**

This bit switches PCH display clocking between the raw oscillator clock and PCDCLK.
It must be programmed as part of enabling and disabling the link.
This bit is ORed with the selection bit from any other FDI Rx Control registers.

Value	Name	Description
0b	Rawclk	Rawclk used
1b	PCDCLK	PCDCLK used

Programming Notes

Restriction : The FDI PLL must be enabled and warmed up before switching to PCDCLK.

FDI_RX_CTL		
	3:0	**Reserved** Format: MBZ

5.2.2 FDI_RX_MISC— FDI Rx Miscellaneous

FDI_RX_MISC	
Register Space:	MMIO: 0/2/0
Project:	
Default Value:	0x00000080
Access:	R/W
Size (in bits):	32
Address:	F0010h-F0013h
Name:	FDI A RX Miscellaneous
ShortName:	FDI_RX_MISC_A
Address:	F1010h-F1013h
Name:	FDI B RX Miscellaneous
ShortName:	FDI_RX_MISC_B
Address:	F2010h-F2013h
Name:	FDI C RX Miscellaneous
ShortName:	FDI_RX_MISC_C

DWord	Bit	Description
0	31:22	**Reserved** Format: MBZ
	21:20	**TP1 to TP2 Time** These bits select the number of link clocks to count before transitioning from TP1 to TP2 during auto training. Value / Name / Description: 10b / 48 / 48 clocks - required programming 11b / 64 / 64 clocks **Programming Notes** Restriction : Program to 48 clocks before enabling FDI with auto-training.
	19	**Reserved** Format: MBZ
	18:16	**Bit Lock Timeout Time** These bits select the number of link clocks to count before timing out on bit lock during auto training. Value / Name / Description: 000b / 128 / 128 clocks 001b / 256 / 256 clocks 010b / 384 / 384 clocks 011b / 512 / 512 clocks 100b / 640 / 640 clocks

FDI_RX_MISC				
		101b	768	768 clocks
		110b	896	896 clocks
		111b	1024	1024 clocks
	15:13	**Reserved**		
		Format:		MBZ
	12:0	**FDI Delay** This field specifies latency as relative delay with respect to the dot clock required for active data over the FDI interface to reach the timing generator FIFO in the transcoder.		

Value	Name	Description
80h	80h **[Default]**	Default
90h	90h	Required for all FDI configurations

Programming Notes
Workaround : Program 90h when FDI is used.

5.2.3 FDI_RX_IMR — FDI Rx Interrupt Mask

FDI Receiver Interrupt Bit Definition	
Register Space:	MMIO: 0/2/0
Project:	
Default Value:	0x00000000
Size (in bits):	32

FDI Receiver (FDI Rx) interrupt bits come from FDI Receiver events.
The FDI_RX_IIR bits are ORed together to generate the FDI_RX Combined Interrupt which will appear in the South Display Engine Interrupt Control Registers.
The FDI Receiver Interrupt Control Registers all share the same bit definitions from this table.

DWord	Bit	Description
0	31:12	**Reserved**
	11	**FDI RX Bit Lock Timeout** This indicates that bit lock timeout occured.
	10	**FDI RX Interlane Alignment** This indicates all the lanes are properly inter-lane aligned.
	9	**FDI RX Symbol Lock** This indicates training pattern 2 was consecutively received successfully on all the enabled lanes.
	8	**FDI RX Bit Lock** This indicates training pattern 1 was consecutively received successfully on all the enabled lanes.
	7	**FDI RX Training Pattern 2 Fail** This indicates that the training pattern 2 has failed.
	6	**FS Code Error** This reports the Fill Start code missing condition.
	5	**FE Code Error** This reports the Fill End code missing condition.
	4	**FDI RX High Symbol Error Rate**

FDI Receiver Interrupt Bit Definition

		This indicates the received symbol error rate is more than 10^-10.
	2	**FDI RX Pixel FIFO Overflow** This indicates the Pixel FIFO overflowed.
	1	**FDI RX Cross Clock FIFO Overflow** This indicates the cross clock symbol clock to display clock FIFO overflowed.
	0	**FDI RX Symbol Queue overflow** This indicates the symbol queue overflowed.

FDI_RX_IMR

Register Space:	MMIO: 0/2/0
Project:	
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32

Address:	F0018h-F001Bh
Name:	FDI A RX Interrupt Mask
ShortName:	FDI_RX_IMR_A

Address:	F1018h-F101Bh
Name:	FDI B RX Interrupt Mask
ShortName:	FDI_RX_IMR_B

Address:	F2018h-F201Bh
Name:	FDI C RX Interrupt Mask
ShortName:	FDI_RX_IMR_C

See the interrupt bit definition table to find the source event for each interrupt bit.

DWord	Bit	Description
0	31:0	**Interrupt Mask Bits** This field contains a bit mask which selects which FDI_RX events are reported int the FDI_RX_IIR.

Value	Name	Description
0b	Not Masked	Not Masked – will be reported in the FDI_RX_IIR
1b	Masked	Masked – will not be reported in the FDI_RX_IIR

5.2.4 FDI_RX_IIR — FDI Rx Interrupt Identity

FDI_RX_IIR		
Register Space:		MMIO: 0/2/0
Project:		
Default Value:		0x00000000
Access:		R/WC
Size (in bits):		32
Address:	F0014h-F0017h	
Name:	FDI A RX Interrupt Identity	
ShortName:	FDI_RX_IIR_A	
Address:	F1014h-F1017h	
Name:	FDI B RX Interrupt Identity	
ShortName:	FDI_RX_IIR_B	
Address:	F2014h-F2017h	
Name:	FDI C RX Interrupt Identity	
ShortName:	FDI_RX_IIR_C	

See the interrupt bit definition table to find the source event for each interrupt bit.

DWord	Bit	Description
0	31:0	**Interrupt Identity Bits** This field holds the persistent values of the FDI_RX interrupt bits which are unmasked by the FDI_RX_IMR. Bits set in this register will propagate to the combined FDI_RX interrupt in the SDE_ISR. Bits set in this register will remain set (persist) until the interrupt condition is cleared by writing a '1' to the appropriate bits.

Value	Name	Description
0b	Condition Not Detected	Interrupt Condition Not Detected
1b	Condition Detected	Interrupt Condition Detected

5.2.5 FDI_RX_TUSIZE— FDI Rx Transfer Unit Size

FDI_RX_TUSIZE	
Register Space:	MMIO: 0/2/0
Project:	
Default Value:	0x7E000000
Access:	R/W
Size (in bits):	32
Address:	F0030h-F0033h
Name:	FDI A RX TU Size 1
ShortName:	FDI_RX_TUSIZE_1_A
Address:	F0038h-F003Bh
Name:	FDI A RX TU Size 2
ShortName:	FDI_RX_TUSIZE_2_A
Address:	F1030h-F1033h
Name:	FDI B RX TU Size 1
ShortName:	FDI_RX_TUSIZE_1_B
Address:	F1038h-F103Bh
Name:	FDI B RX TU Size 2
ShortName:	FDI_RX_TUSIZE_2_B
Address:	F2030h-F2033h
Name:	FDI C RX TU Size 1
ShortName:	FDI_RX_TUSIZE_1_C
Address:	F2038h-F203Bh
Name:	FDI C RX TU Size 2
ShortName:	FDI_RX_TUSIZE_2_C

Programming Notes

Restriction : The FDI Receiver TU1 and TU2 sizes must be programmed to match the TU sizes used by the FDI Transmitter.
When switching between two refresh rates, both the TU1 and TU2 values must be programmed.
For dynamic refresh rate control, TU1 values are the primary values and are used for the normal setting, and TU2 values are the secondary values and are used for the lower power setting.

DWord	Bit	Description
0	31	**Reserved** Format: MBZ
	30:25	**TU Size** This field is the size of the transfer unit for FDI, minus one. Value: 111111b — Name: 63 **[Default]** Value: [1,63] — Name:
	24:0	**Reserved** Format: MBZ

Revision History

Revision Number	Description	Revision Date
1.0	First 2012 OpenSource edition	May 2012

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