Intel® UHD Graphics Open Source

Programmer's Reference Manual

For the 2020 Intel Core™ Processors with Intel Hybrid Technology based on the "Lakefield" Platform

Volume 4: Configurations

May 2021, Revision 1.0

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Configurations Overview

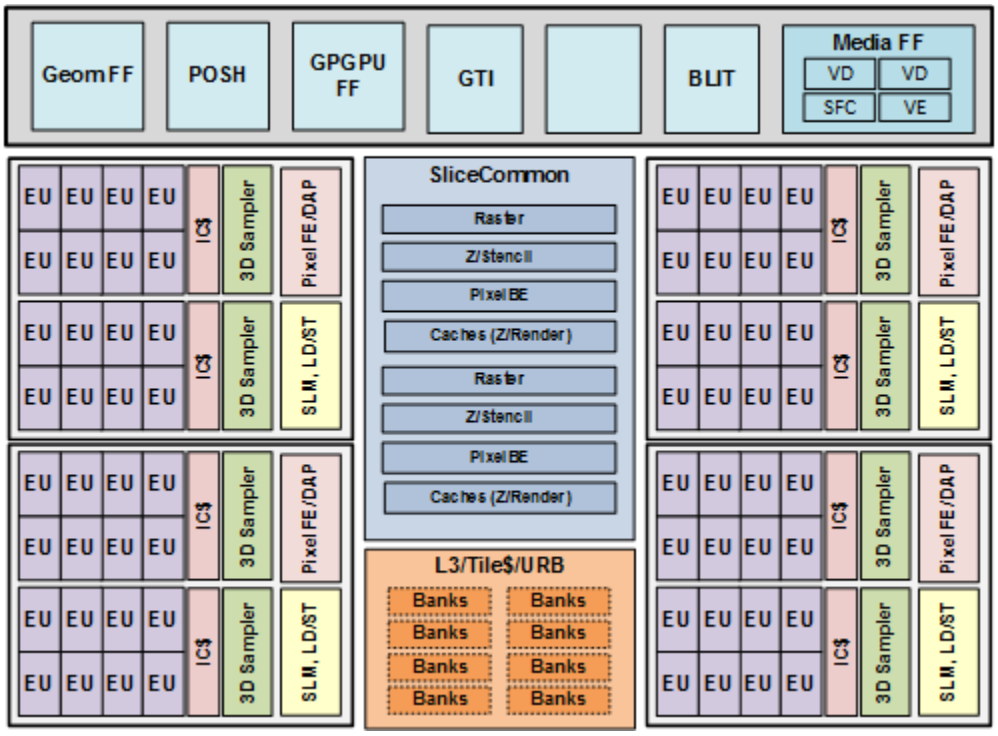
The Intel Graphics Architecture was first introduced to the market in 2004. Since that time, the architecture and implementation have evolved to add many new features, increase performance, and improve power efficiency.

Each product generation has its own configurations chapter. Each chapter has a section for each project, and each project contains the following subsections:

- Top Level Block Diagrams - Shows basic feature blocks of the project's graphics architecture, for GT configurations.
- Device Attributes - Lists details of the graphics configuration options for each project.
- Steppings and Device IDs - Lists all the current unique GT Die / Packages for a specific project.

Top Level Block Diagram

The diagram below shows basic feature blocks of the Lakefield graphics architecture.



Device Attributes

The following table lists detailed GT device attributes for proposed SKUs.

NOTE: This information is preliminary, and subject to change.

Product Configuration Attribute Table	
Architectural Name *	**1x8x8**
SKU Name	**LKF**
Global Attributes	
Slice count	1
Subslice Count	8
EU/Subslice	8
EU count (total)	64
Thread Count	7
Thread Count (Total)	448
FLOPs/Clk - Half Precision, MAD (peak)	2048
FLOPs/Clk - Single Precision, MAD (peak)	1024
FLOPs/Clk - Double Precision, MAD (peak)	N/A
Unslice clocking (coupled/decoupled from Cr slice)	Coupled
GTI / Ring Interfaces	
GTI bandwidth (bytes/unslice-clk)	64R
	64W
eDRAM Support	N/A
Graphics Virtual Address Range	36 bit
Graphics Physical Address Range	39 bit
Caches & Dedicated Memories	
L3 Cache, total size (bytes)(1)	2560KB
L3 Cache, bank count(1)	8
L3 Cache, bandwidth (bytes/clk)	16x64: R|W
L3 Cache, D$ Size (Kbytes)(1)	1536KB
URB Size (kbytes)(1)	512KB-1024KB
L3 Cache, Tile Cache (Kbytes)	1024KB
SLM Size (kbytes)	4x64KB
LLC/L4 size (bytes)	2x2MB
Instruction Cache (instances, bytes ea.)	8x48KB
Color Cache (RCC, bytes)	2x32k
MSC Cache (MSC, bytes)	2x16k
HiZ Cache (HZC, bytes)	2x12k

Product Configuration Attribute Table	
Architectural Name *	**1x8x8**
SKU Name	**LKF**
	48 ways x 4 x 64
Z Cache (RCZ, bytes)	2x32k 32 ways x 16 x 64
Stencil Cache (STC, bytes)	2x8k 32 ways x 4 x 64
Instruction Issue Rates	
FMAD, SP (ops/EU/clk)	8
FMUL, SP (ops/EU/clk)	8
FADD, SP (ops/EU/clk)	8
MIN,MAX, SP (ops/EU/clk)	8
CMP, SP (ops/EU/clk)	8
INV, SP (ops/EU/clk)	2
SQRT, SP (ops/EU/clk)	2
RSQRT, SP (ops/EU/clk)	2
LOG, SP (ops/EU/clk)	2
EXP, SP (ops/EU/clk)	2
POW, SP (ops/EU/clk)	1
IDIV, SP (ops/EU/clk)	1-6
TRIG, SP (ops/EU/clk)	2
FDIV, SP (ops/EU/clk)	1
Load/Store	
Data Ports (HDC)	2x2
L3 Load/Store - same addresses within msg (dwords/clk)	256 B/c (2*2*64)
L3 Load/Store - unique addresses within msg (dwords/clk)	256 B/c (2*2*64)
SLM Load//Store - same addresses within msg (dwords/clk)	512 B/c (4*2*64)
SLM Load//Store - unique addresses within msg (dwords/clk)	512 B/c (4*2*64)
Atomic, Local 32b - same addresses within msg (dwords/clk)	64 dw/c (4*2*8)
Atomic, Global 32b - unique addresses within msg (dwords/clk)	64 dw/c (2*2*16)
3D Attributes	

Product Configuration Attribute Table	
Architectural Name *	**1x8x8**
SKU Name	**LKF**
Geometry pipes	1
Samplers (3D)	8
2D Texel Rate, point, 32b (tex/clk)	32
2D Texel Rate, point, 64b (tex/clk)	32
2D Texel Rate, point, 128b (tex/clk)	32
2D Texel Rate, bilinear, 32b (tex/clk)	32
2D Texel Rate, bilinear, 64b (tex/clk)	32
2D Texel Rate, bilinear, 128b (tex/clk)	8
2D Texel Rate, trilinear, 32b (tex/clk)	16
2D Texel Rate, trilinear, 64b (tex/clk)	8
2D Texel Rate, trilinear, 128b (tex/clk)	8
2D Texel Sample Rate, aniso 2x (MIP nearest), 32b (tex/clk)	32
2D Texel Sample Rate, aniso 4x (MIP nearest), 32b (tex/clk)	16
2D Texel Sample Rate, aniso 8x (MIP nearest), 32b (tex/clk)	8
2D Texel Sample Rate, aniso 16x (MIP nearest), 32b (tex/clk)	4
3D Texel Sample Rate, point, 32b (tex/clk)	32
3D Texel Sample Rate, point, 64b (tex/clk)	32
3D Texel Sample Rate, point, 128b (tex/clk)	16
3D Texel Sample Rate, bilinear, 32b (tex/clk)	16
3D Texel Sample Rate, bilinear, 64b (tex/clk)	16
3D Texel Sample Rate, bilinear, 128b (tex/clk)	4
HiZ Rate, (ppc)	2x64
IZ Rate, (ppc)	2x16
Stencil Rate (ppc)	2x64
(500 MHz, DDR-2400 or eDRAM; Range depends on dynamic compression ratio)	
Pixel Rate, fill, 32bpp (pix/clk, RCC hit)	16
Pixel Rate, fill, 32bpp (pix/clk, LLC hit @ 1.0x unslice clk)	16
Pixel Rate, fill, 32bpp (pix/clk, LLC hit, @ 1.5x unslice clk)	16
Pixel Rate, fill, 32bpp (pix/clk, memory, @ 1.0x unslice clk)	16
Pixel Rate, fill, 32bpp (pix/clk, memory, @ 1.5x unslice clk)	16
(500 MHz, DDR-2400 or eDRAM; Range depends on dynamic compression ratio)	
Pixel Rate, blend, 32bpp (p/clk, RCC hit)	16
Pixel Rate, blend, 32bpp (p/clk, RCC miss, @ 1.0x unslice clk)	16
Pixel Rate, blend, 32bpp (p/clk, RCC miss, @ 1.5x unslice clk)	16
Pixel Rate, blend, 32bpp (pix/clk, memory, @ 1.0x unslice clk)	16

Product Configuration Attribute Table	
Architectural Name *	**1x8x8**
SKU Name	**LKF**
Pixel Rate, blend, 32bpp (pix/clk, memory, @ 1.5x unslice clk)	16
Media Attributes	
Samplers (media)	0
VDBox Instances (See)	2
VEBox Instances(2)	1
SFC Instances	1
WGBox Instances	0

Notes:

* Architectural Name = Slice Count x Subslice Count x EUs per Subslice

(1) Programmable range; Data and URB portioning of L3 cache.

(2) Pass-through only, no VEbox processing logic.

Steppings and Device IDs

SKUs and Device IDs

Index	CPU SKU*	Config	EUs	TDP	Dev2 ID	Comments
1	LKF	1x8x8	64	7W	0x9840	Production
3	LKF	1x6x8	48	7W	0x9841	Production