Intel® Open Source HD Graphics, Intel Iris™ Graphics, and Intel Iris™ Pro Graphics

Programmer's Reference Manual

For the 2015 - 2016 Intel Core™ Processors, Celeron™ Processors, and Pentium™ Processors based on the "Skylake" Platform

Volume 16: Workarounds

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Workarounds

This table lists all SKL workarounds. Note that the functional area for each item is listed below, and you can search on this value or other content on this page using search (e.g. Ctrl-F).

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
0210	3D		WaDisableMidObjectPreemptionForGSLineStripAdj	This is a bug in GS. GS expected vertex count doesn't decode linestrip_adj_cont nor polygon_cont. Only linestrip_adj_cont since polygon is not pre-empted. WA: Disable mid-draw preemption when draw-call is a linestrip_adj and GS is enabled.	SIWA_FOREVER (all SKUs/ steppings for applicable projects - no HW workaround planned)
0233	3D		WaForceMinMaxGSThreadCount	GS being stalled can cause the fftid to go over max threads causing undefined scratch space to be used. WA: Limit the number of handles to the number of threads, with some GS performance loss. Set min/max threads to 8 for GS. Should be handled in USC/IGC.	SIWA_FOREVER (Means this applies to all SKUs/steppings for SKL- no HW fix is planned)
0234	3D		WaGrfScoreboardClearInGpgpuContextSave	Need to use stop_done pulse to clear grf scoreboard on save. Logic exists to restore grf scoreboard based on MDE data being restored to MEU. WA: Software workaround in SIP: State register special handling against page fault issue; change is requested by EU team. In Context save sr0.1 register is stored in temporary register, temporary register is masked and sent to csr buffer, next sr0.1 is cleared. In context restore sr0.1 is restored as one	SKL SIWA_FOREVER (all SKUs/ steppings for applicable projects - no HW workaround planned)

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
				of the last registers (just before r0 restore and exception clear).	
0236	3D		WaAdditionalMovWhenSrc1ModOnMulMach	A source modifier must not be used on src1 for the mul/mach macro operations. WA: Use extra move instead of src modifier for src1.	All
0237	3D		WaRestoreFC4RegisterDW0fromDW1	GfxSV - [MDT] - GPGPU Pre-emption - Execution Mask not being saved/restored correctly (memdiff). WA: SIP routine has to correct the address while restoring. Flow control register FC4 has to be restored from DW1.	SIWA_FOREVER (all SKUs/ steppings for applicable projects - no HW workaround planned)
0238	3D		WaScalarAtomic	This is a performance improvement implemented as a W/A. Improves append counter updates from 1/6 clks (L3 limit) to 16/6 clks.	SIWA_FOREVER
0240	3D	Media State and Primitive Commands		Two MEDIA_STATE_FLUSH commands need to be used to ensure that the flush is complete.	All
0241	3D	Extended Math Function		When both srcs are NAN, FDIV produces denorminator NAN as output.	All
0242	3D		WaThreadSwitchAfterCall	[MDT}GfxSV - GPGPU Pre-emption - CALL Inst ruction Hang. WA: Follow every call by a dummy non-JEU and non-send instruction with a SWITCH for both cases whether a subroutine is taken or not.	SIWA_FOREVER (all SKUs/ steppings for applicable projects - no HW workaround planned)

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
0243	3D	MEDIA_STATE_FLUSH		A MEDIA_STATE_FLUSH with no options must be added after a GPGPU_WALKER command which doesn't use either SLM or barriers.	All

0244	3D		WaNearestFilterLODClamp	DX10.1 LOD clamping VS Max LOD DX case.
				Workarounds:
				DX:
				`If ( mipfilter_nearest )`
				`MaxLOD = floor(MaxLOD)`
				`MinLOD = floor(MinLOD)`
				OGL:
				`If ( mipfilter_nearest )`
				`lodbiad = lodbiad - 0.000001b`
				Dx9 - (Not Required for Dx9. Max always set to to 14.0)
				Mac - Should not be needed - but needs follow up.
					SIWA_FOREVER (Means this applies to all SKUs/steppings for SKL-no HW fix is planned)

0245	3D	GPGPU Context Switch Workarounds		After either a MI_SET_CONTEXT or a PIPE_CONTROL with Generic Media State Clear, there must be a MEDIA_VFE_STATE command before any pre-emptable command. The parameter of this MEDIA_VFE_STATE command can be set to default values.	All

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
0248	3D	3D Sampler Message Types		If Surface Format is R10G10B10_SNORM_A2_UNORM and Gather4 Source Channel Select is alpha channel, the returned value may be incorrect.	SKL
0249	3D	Programming Media Pipeline - Command Sequence		A MEDIA_STATE_FLUSH needs to be placed right before the MI_BATCH_BUFFER_END of any batch buffer that uses MEDIA_OBJECT.	SKL
0257	3D		WaCallForcesThreadSwitch	RTL TC: (Tracking) Dependency is not set for call instruction. WA: Call instructions must have Thread switch bit set.	All
0261	3D		WaClearFlowControlGpgpuContextSave	Stack entry valid will no t be reset during ctxsave. WA: Set the value to 0 through restore SIP.	All
0262	3D		WaClearArfDependenciesBeforeEot	GFXDRV [B0] - BattleForge3 hang - flag register dependency not cleared after EOT. WA: Source ARF registers before EOT.	All
0263	3D		WaClearCr0SpfInGpgpuContextRestore	GfxSV - GPGPU Pre-emption - Corruption on context restore. WA: To reset SPF bit through SIP during restore.	All
0265	3D		WaDisableNoSrcDepSetBeforeEOTSend	GFXDRV: [MDT] WGF11Compute UAV hang. WA: The send or sends before the EOT should not have the NoSrcDepSet bit set.	All

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
0266	3D		WaClearNotificationRegInGpgpuContextSave	GFXSV GPGPU: GPG PU Pre-emption test hang 4. WA: In SIP, move zeroes into notify count registers.	All
0268	3D		WaL3UseSamplerForVectorLoadScatter	WA: Use sampler for vector load.	All
0270	3D		WaIntegerDivisionSourceModifierNotSupported	Both Fulsim and RTL do not apply src mod for integer divide - BSPEC needs update. WA: Src mods cannot be used for integer divide math ints.	All
0272	3D		WaDoNotPushConstantsForAllPulledGSTopologies	SKL GFXDRV: GS Patchlist_14 and above in PULL Model - Cannot push constants. When Include Vertex Handles is set for non-instanced SIMD8 dispatch of PATCHLIST_14..32 objects, pushed vertex data and/or pushed constants cannot be used as they would need to start in the payload beyond the range of this field (that is, beyond R15).	All
0275	3D	Addressing 1D, 2D, 3D, CUBE Surfaces		If the surface state indicates the Number of Multisamples > 1, then the LOD parameter is not optional: the R and LOD parameters must be specified along with the MSAA sample number parameter.	All
0278	3D		WaZeroOneClearValuesMSAA	Precision issue with non 0/1 clears for MSAA. WA: For SKL, disable non 0/1 clears for any MSAA surface.	All

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
0279	3D		WaZeroOneClearValuesAtSampler	Precision match fix for Non-0/1 Clear color [S/W H/W Bypass codesign] WA: SKL clear values other than 0/1 need resolve pass before being sampled. This is a BSPEC Restriction.	SIWA_FROM_B0 (all SKUs/steppings starting with B0)
0280	3D	MSAA Typed Surface ReadWrite Messages [SKL]		The SIMD4x2 MSAA Read message may not correctly handle out-of-range sample numbers on the second slot. Software workaround is use the SIMD8 version of the message.	All
0282	3D		WaOCLEnableFMaxFMinPlusZero	FMIN/FMAX behavior dependent on denormal bit.	All
0283	3D		WaVFComponentPackingRequiresEnabledComponent	GFXDRV: StreamOut hangs with VF, VS, and CS not done.	All
0284	3D	QWord Untyped Atomic Integer Messages		AOP CMPWR_2W is not supported in A64 SIMD4x2 DWord operations. Use the A64 SIMD8 DWord operation as a workaround.	All
0285	3D	OWord Untyped Atomic Integer Messages		AOP_CMPWR_2W is not supported on A64 Qword SIMD4x2 or SIMD8.	All
0286	3D		WaSetTriLinearFilterForLODPreclamp	FPF: OGL LOD rounding when LOD calculated is 0.5. WA: S/W w/a in place; no BSpec update is required.	All

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
0287	3D			GS issue with inputvtxramout read ptr in trail mode Issue is in Trail mode - RD pointers getting corrupted. SW WA exists; need confirmation if it is acceptable for SKL C0. WA: Reorder mode bit in 3DSTATE_GS should be always leading. Dx10 does this by default and is only API with GS.	All
0289	3D		WaDisable1DDepthStencil	Common tiler: Linear tiling Support for STC Decision made to not support Linear STC for A0 SKLGFX WA: Fix is to change 1D depth/stencil to 2D with height of 1. B0 Candidate: [64KB Tiling] 1d Surfaces illegal for depth and stencil buffers on SKL A0 WA: WA on SKL to disable 1D Depth Stencil buffers and use 2D with ht of 1 instead.	All
0290	3D	GPGPU Context Switch Workarounds		HW does not support pre-empting implicit flushes triggered by Render CS on parsing non-pipeline state commands. When a pending execlist gets submitted during an ongoing implicit flush on parsing a non-pipeline state command, HW will wait for the completion of implicit flush and to encounter a pre-emptable command before accepting the new pending execlist. This leads to increased pre-emption latencies compared to when pending execlist is submitted when a pre-emptable command is being executed. This issue	All

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
				is unique to GPGPU workloads where mid thread pre-emption is supported and does not apply for 3D workloads. Note: To circumvent this issue SW must always program PIPE_CONTROL with "CS Stall" and "Render Target Cache Flush Enable" set prior to programming the following commands for GPGPU workloads (that is, when pipeline select is GPGPU via PIPELINE_SELECT command). STATE_BASE_ADDRESS, GPGPU_CSR_BASE_ADDRESS, PIPELINE_SELECT	
0292	3D	Notification Registers		Write operation is allowed in normal operation and is not restricted to context restore.	All
0294	3D	3D Sampler Messages - Message Format		When 16-bit return format is used, SIMD16 messages should always be used with a header.	SKL,
0301	3D	State Register		WA: These bits will have undefined value if a previously saved GPGPU context is restored for execution. All new contexts will have these bits initialized to zero. Bits Definition [6:5] Reserved 4 Inexact Exception 3 Overflow 2 Underflow 1 Divide by Zero	All

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
				0 Invalid Operation	
0308	Blitter			No Blitter workarounds have been submitted for SKL.	ALL
0342	Display	DisplayPort		DP MST output incorrect for certain M and N and VC payload size values. WA: VC payload must be multiple of 4 in x1 lane config, 2 in x2, 1 in x4. See M/N Values.	All
0347	Display	DisplayPort		Aux channel transactions get intermittent NAK errors with some receivers. WA: Increase DDI_AUX_CTL bits 27:26 Time out timer value to 600us 01b when doing DDI aux transactions.	All
0371	Display	Panel fitter	WaPanelFitterDownscale	Not a bug, but good to know. When using panel fitter downscaling (pipe source size is larger than panel fitter window size) the maximum supported pixel rate will be reduced by the downscale amount, and watermarks must be adjusted. Use panel fitter scale amount when calculating maximum pixel rate and watermarks.	All
0373	Display	Panel power sequencing	WaVDDOverrideT4Power	When software clears the panel power sequencing VDD override bit from 1 to 0 (disable VDD override) it must ensure that T4 power cycle delay is met before setting the bit to 1 again, else panel ma y be damaged. WA: Use software timers to ensure T4 delay is met or use full panel power enable and not the VDD override.	All

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
0386	Display	PSR		PSR single frame update - When single frame update is enabled, the PSR CRC must be disabled for panel compatibility. See North Display Engine Registers SRD_CTL register for details.	All
0387	Display	PSR		PSR single frame update - Mask register write events when using single frame update. See North Display Engine Registers SRD_CTL register for details.	All
0388	Display	PSR		PSR power saving - Mask PSR max timeout when PSR CRC is enabled. See North Display Engine Registers, SRD_CTL register for details.	All
0456	Memory Views	Planar Memory Organization		The offset for the start of the U and V plane must be a multiple of 4 cache-lines except YUV_PLANAR_* surface formats.	All
0457	Memory Views	Planar Memory Organization		When using Planar formats for YUV with half-pitch chroma planes (for example, YV12), fenced tiling is not supported.	All
0517	3D	Depth Buffer	DepthBufferR2T8x	WA: Depth surface aligned to 128 bytes and pitch a multiple of 256 byteswhen samples == 16	SKL All
0527	Display	Power		MMIO accesses to 0x8Fxxx registers are not allowed when DC5/DC6 power states are enabled. Disable DC5/DC6 during mode set and re-enable them after the mode set programming is completed.	All

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
				For optimal performance, disable DC5/DC6 when programming a set of registers and re-enable them after the programming is completed. MMIO accesses have more latency when DC5/DC6 is enabled.	
0529	Display	FBC		Corruption in some cases when FBC is enabled and the plane surface format is in linear, tile Y legacy or tile Yf WA: Display register 4208Ch bit 13 must be set to 1b and bits 12:0 must be programmed with the compressed buffer stride value. The compressed buffer stride must be calculated using the following equation: Compressed buffer stride = ceiling [(at least plane width in pixels) / (32 * compression limit factor)] * 8 At least plane width = a value greater than or equal to the width of the plane. Software may choose to use a greater value in order to handle cases where the plane width is changing from frame to frame. Compression limit factor is either 1, 2 or 4 based on the Compression Limit field. If the limit is 2:1, the compression limit factor to be used is 2. Ceiling function rounds up any non-integer value to next greater number. Example ceiling [0.3] = 1, ceiling[2.1] = 3, ceiling[4.8] = 5, ceiling[4] = 4.	ALL

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
0530	Display	Render Compression, Async Flips		When render decompression is enabled, hardware internally converts the Async flips to Sync flips WA: Do not enable render decompression when Async flips are enabled.	All
0531	Display	Render Compression		Render decompression is broken when plane widths greater than 3840 are used with horizontal panning. WA: When the render compression is enabled with plane width greater than 3840 and horizontal panning (Start X Position in the PLANE_OFFSET register is not 0), the stride programmed in the PLANE_STRIDE register must be multiple of 4.	All
0540	KMD		WaForceContextSaveRestoreNonCoherent	To avoid a potential hang condition with TLB invalidation driver should enable masked bit 5 of MMIO 0x7300 at boot.	SIWA_FOREVER
0551	KMD		WaDisableMidThreadPreempt	Disable GPGPU thread-level (a.k.a. mid-thread) preemption on parts (until B0) since validation was minimal on those parts.	SKL: SIWA_FOREVER
0556	KMD		Wa4x4STCOptimizationDisable	HIZ/STC hang in hawx frames. W/A: Disable 4x4 RCPFE-STC optimization and therefore only send one valid 4x4 to STC on 4x4 interface. This will require setting bit 6 of reg. 0x7004. Must be done at boot and all save/restore paths.	SIWA_FOREVER

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
0562	Power	FBC		FBC sometimes causes screen corruption. WA: 'FBC Watermark Disable' bit in ARB_CTL register must be set to 1b.	SKL:ALL
0572	KMD	RTL	WaFlushCoherentL3CacheLinesAtContextSwitch	Coherent L3 cache lines are not getting flushed during context switch which is causing issues like corruption. Need to set bit 21 of MMIO b118, then send PC with DC flush and then reset bit 21 of b118. This programming sequence needs to be part of the indirect context WA BB	SIWA_FOREVER
0590	KMD		WaSkipInvalidSubmitsFromOS	For Invalid submits from OS - simply report fence completion without submitting the DMA buffer to GPU.	SIWA_FOREVER
0594	3D			Tristrip- wrong provoking vertex If there is an odd number of TRs in the clipper, we have an issue in picking the correct provoking vertex in SF. We swap the vertices to right winding order in clipper, and in SF we pick the provoking vertex. If there is odd TRs in clipper, these two go out of sync and SF picks vtx1 instead of vtx2 and vice versa. WA: Using flip logic from clipper instead of local flip logic to set the provoking vertex for tristrip.	SKL:SIWA_UNTIL_H0

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
0596	GT			While CS deciding to do sync ctx switch on semaphore wait lite restore happens. As a result CS does lite restore and skips the semaphore wait. This happens only on a particular clock if lite restore occurs during semaphore wait.	SKL:SIWA_UNTIL_H0
0598	GTI			An invalidation request comes from GAMT to GAMD after an RCP request for which an RCP$ miss request was already sent to memory. After this there is another RCP request to RCP$ which occupies the same cacheline. WA: RCP Invalidation pulse will be sent from GAMT only when the corresponding atomic fence advances from the TLB. Fix in one of the TLBs is given below: always_comb ctrl_rcp_mfx0_inv_nxt = (reg_rcpinvalidate_atfncadv & ctrl_wcp_flush_mfx0) | (~reg_rcpinvalidate_atfncadv & ctrl_rcp_mfx0_inv_i); 'GT_ASYNC_RSTB_MSFF(ctrl_rcp_mfx0_inv, ctrl_rcp_mfx0_inv_nxt, cuclk, cdevrst_b)	SKL:SIWA_UNTIL_H0
0599	GTI			GA MMCD: in RCP cahce even if fine miss resposne is not present , new miss cycle evicts out this entry	SKL:SIWA_UNTIL_H0

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
0601	3D			When there is a sequence of non-media message followed by media MMCD message in back to back clock inside HDC pipeline, the non-media message incorrectly gets the MMCD values of the next message in pipeline. This leads to memory corruption in GAM. WA: Muxed the mmcd values to 0 when the msg is a non-media.	SKL:SIWA_UNTIL_H0
0603	GTI			Media: Decoder DN test hang with MMCD bug Fix emulation model WA: The test has virtual64 enabled and the test passes without virtual64.	SKL:SIWA_UNTIL_I0

0622	Blitter	Blitter FBC		Incorrect MUX select in BLB to select between Fast Copy and Legacy FBC requests.
				WA: Blitter FBC front buffer modification tracking must not be enabled (BCS_ECOSKPD bit[3] must always be 0).
				• If using Front buffer rendering via BLT & Display FBC compression feature is enabled, SW must follow the BLT commands that target the front buffer with:
				  ○ Flush
				  ○ LRI to 0x50380 with data 0x0000_0004 (This causes FBC to
					SKL:SIWA_FOREVER

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
				recompress the entire buffer after BLT operation)	
0642	3D		WaClearCCStatePriorPipelineSelect	Architecture hole; on GPGPU context restore, at the end of the context when CS sends a null prim, SVG and SARB does a state prefetch; by the time the data returns from memory, CS gates the FF clock. WA: In GPGPU mode, color cal state should not have valid bits. Before switching pipelines, send null CC state pointers.	SKL:SIWA_FOREVER
0671	3D			DF --> f format conversion for align16 has wrong emask calculation when the source is immediate. WA: In Align16 mode, format conversion from double-float to floats is not allowed when source is immediate data.	SIWA_FOREVER
0673	3D		WaStallBeforePostSyncOpOnGPGPU	Preemption mid-thread focused test failures. WA: PIPECONTROL command with “Command Streamer Stall Enable”must be programmed prior to programming MI_SEMAPHORE_SIGNAL command with Post-Sync Operation set in GPGPU mode of operation (i.e when PIPELINE_SELECT command is set to	SIWA_FOREVER

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
				GPGPU mode of operation). PIPECONTROL command with "Command Streamer Stall Enable"must be programmed prior to programming MI_ATOMIC command with Post-Sync Operation set in GPGPU mode of operation (i.e when PIPELINE_SELECT command is set to GPGPU mode of operation). PIPECONTROL command with "Command Streamer Stall Enable"must be programmed prior to programming a PIPECONTROL command with Post Sync Op in GPGPU mode of operation (i.e when PIPELINE_SELECT command is set to GPGPU mode of operation).	
0675	3D		WaFlushBefore3DSTATEGS	GS_SIMD8_OTHANDLE_RELAX test hanging due to an issue in gs_trg clock gating logic. WA: Add state_osb_statedv into trg_cg equation.	SIWA_FOREVER
0677	3D		WaDisableLosslessCompressionForSampleL	Sampler Throughput drop with lossless enabled for 0% & 50%, compression tests with 100%bypass. WA: Disabe double-fetch.	SIWA_FOREVER
0678	3D		WaDisableStencilBufferTestOnStencilBufferDisable	MSAA test hangs with RCZ, IZ, WMFE and SVL not done. WA: Force the 3DSTATE_WM_DEPTH_STENCIL :: Stencil Buffer Test Enable to 0 when 3DSTATE_STENCIL_BUFFER	SIWA_FOREVER

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
				::STENCIL_BUFFER_ENABLE = 0	
0680	3D		WaDisableSamplerL2BypassForTextureCompressedFormats	RTL DM producing Xs for SC output. WA: Disable Bypass on some of the compressed formats.	SIWA_FOREVER
0684	3D		WaDisableKillLogic	System hang while using RC6 and HW TRTT. WA: Platform work stable with RC6 disabled or after switching to SW TRTT.	SIWA_FOREVER
0689	3D		WaPipeControlBeforeVFCacheInvalidationEnable	Vf randomly decodes nullprim packets as state packets causing illegal internal states in it. WA: B2B control packets to be sent when VS_cache_enable is programmed to be enabled. First control packet with bit11 as '0' and the next control packet with bit11 as '1'.	SIWA_FOREVER
0692	3D		WaKVMNotificationOnConfigChange	DPR currently sends a "decreg" signal to DPCEUNIT for TRANS_CONF_EDP. The signal is expected only to pulse when a write on TRANS_CONF_EDP has occurred, but the signal is actually assigned to logic directly out of the automated register code which is read and write accesses. This is resulting in repeated KVM config changes being sent to ME in silicon when using an EDP panel and ultimately results in poor performance and notable lag in mouse movements when using EDP. WA: Current workaround is to set	SIWA_FOREVER

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
				DPCE to be less aggressive with its config change checks.	
0696	3D		WaBindlessSurfaceStateModifyEnable	Missing "Size Modify Enable" Bit For Bindless Sizes in STATE_BASE_ADDRESS. WA: The suggested WA is that when NOT setting the modify enable bit for Bindless Surface State Base Address, program the dword length to "Eh"instead of "11h"and zero out the last 3 DW or not send them.	SIWA_FOREVER
0703	GTI	L3	WaDisableL3ErrorDetectionHangOnError	Model hang in wgf11shader5x store_raw tests. WA: Connected ~SVL[9] to LNCFUNIT lncf_csr_bank_hang_override which is then routed to LBCFUNIT. • On SKL A0, Bit(9) must be set to zero (no hang on error) due to hw bug. • On SKL B0 this bit can be set to either 0 or 1,setting the bit to one will ensure error data does not get propagated. • For SKL A0, no driver programming is required. That means no hang on uncorrectable error. For SKLB0 onwards, set BIT(9) of L3CNTLREG (0x7034h) for GPGPU context.	SKL:SIWA_FROM_A0

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
0707	3D			MMIO address for preemption save/restore, barrier prog. need to be fixed for GW, GWC and TDL. WA: Fixed MMIO addresses for slice1 and slice2 signals.	SKL:SIWA_FROM_C0
0708	3D			Eutc generates wrong dst length for simd16 call with source register offset 0.4 WA: Use SIMD16 and SIMD32 call instruction with offset .0.	SKL:SIWA_FROM_B0
0709	3D	Surface State used by RT		Failing to implement the following WA, can cause Gfx device to hang WA : Option 1 (exhaustive conditions to limit performance impact of WA. requires SW to check both surface state and per draw call state parameters) When all the following conditions are true for any render target: [(SURFACE_STATE.SurfaceType == SURFTYPE_2D) & (SURFACE_STATE.SurfaceMinLOD < 2 or SURFACE_STATE.LOD < 2) & (SURFACE_STATE.NumberOfMultisamples != MULTISAMPLECOUNT_16) & (3DSTATE_PS_EXTRA.PixelShaderIsPerSample != 1) & (SURFACE_STATE.SurfaceFormat != 64 bits/pixel) & (SURFACE_STATE.SurfaceFormat != 128 bits/pixel) &	SKL:GT2:ALL SKL:GT3:SIWA_UNTIL_K0

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
				(SURFACE_STATE.TileMode == XMAJOR or YMAJOR) & ((BLEND_STATE_ENTRY.LogicOpEnable == 1) or (BLEND_STATE_ENTRY.ColorBufferBlendEnable == 1) or ((SURFACE_STATE.SurfaceFormat has non byte aligned channels & (BLEND_STATE.WriteDisableAlpha == 1) or (BLEND_STATE.WriteDisableRed == 1) or (BLEND_STATE.WriteDisableBlue == 1) or (BLEND_STATE.WriteDisableGreen == 1)))) & (SURFACE_STATE.renderTargetRotation == 0DEG) & (SURFACE_STATE.XOffset == 0)], SW must set render targets' SURFACE_STATE.AuxiliarySurfaceMode to AUX_CCS or AUX_MCS. SW may set CACHE_MODE_1.MCSCacheDisable if all render targets do not support MCS Option 2 : The following simplified version of the WA removes all per draw call state from the list of conditions and keeps only the surface state parameters. This makes the WA coarser and will likely have bigger performance impact than option 1 When all the following conditions are true for any render target: [(SURFACE_STATE.SurfaceType ==	

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
				SURFTYPE_2D) & (SURFACE_STATE.SurfaceMinLOD < 2 or SURFACE_STATE.LOD < 2) & (SURFACE_STATE.NumberOfMultisamples != MULTISAMPLECOUNT_16) & (SURFACE_STATE.SurfaceFormat != 64 bits/pixel) & (SURFACE_STATE.SurfaceFormat != 128 bits/pixel) & (SURFACE_STATE.TileMode == XMAJOR or YMAJOR) & (SURFACE_STATE.renderTargetRotation == 0DEG) & (SURFACE_STATE.XOffset == 0)], SW must set SURFACE_STATE.AuxiliarySurfaceMode to AUX_CCS or AUX_MCS. SW needs to set CACHE_MODE_1.MCSCacheDisable if render target does not support MCS	
0711	3D			While executing MI_SEMAPHORE_SIGNAL command from per ctx WA batch buffer after a context switch - CS will not release credits and can stall and hang in WA batch execution. WA: Not to put semaphore signal command for per context WA batch buffer.	SIWA_FOREVER

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
0712	3D			Byte Mask Media write have issue with byte enable when block width is less then 32. WA: Restriction for A0 and B0 : byte mask media message cannot be used.	SKL:SIWA_FROM_A0
0715	3D			Dst dependency is getting cleared on commit. It should be cleared on writeback data. WA: During HDC page fault mode, destination and source overlap cannot happen for send instruction.	SKL: SIWA_FROM_A0
0716	Blitter			When subblt is off: Ty->Ty single CL in the y-direction When subblt is on: Ty-Ty copy where a subblt is created that is a single CL in the y-direction Under this case, Two CLs with the same address will be created. Sine the signal one_cl doesn't assert causing the walker to have it's "run" bit set. "run" should not be set under this case. WA: Restriction on memory surface.	SKL:SIWA_FROM_B0
0717	GTI			With the current implimentation, the mask is applied on the allocated entries in TLB, but not on the look up address. This will cause issues becasue we would not be invalidating the entries properly. WA: In Mask based TLB Shoot down ,	SKL:SIWA_FROM_B0

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
				Mask should be applied on Look up address before sending it to GAMT.	
0719	3D			When accumulator destination and offset is odd with the stride of 2 then there is mismatch. 3D driver does not use this kind of instruction but need feedback from media driver team. WA: Do not use the odd offset with the stride of 2.	SKL:SIWA_FROM_B0
0726	3D			Free running grant in flunit is causing clock ratio determinism issue in SBFT mode. WA: Permanent (for dft mode) is to use unit level clock gating for grant logic still steady state.	SKL:ALL
0729	3D			OA can't be functional for media-only perf analysis when render is powerdown. WA: Keep render engine powered ON when OA is enabled for media only perf analysis.	SKL:SIWA_FROM_A0
0731	Display		WaDisableRCWithAsyncFlip	Display corruption with Async flips when render decompression is enabled. WA: Render Compression is not supported with ASync flips. Disable render compression when ASync flips are used.	SKL:SIWA_FROM_A0

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
0732	3D			When src1 has indirect addressing with sends instruction there is a miscompare at the output of EU. 3D and media compiler are not using this instruction with indirect addressing. WA: Indirect addressing not to be used for src1 of sends instruction.	SKL:SIWA_FROM_A0
0736	3D			RTCompression test miscomapres in the MCS buffer. WA: Disable RTR for 1x case (i.e, non-MSAA).	SKL:SIWA_FROM_C0
0737	3D		WaDisableDither	OptHizClear test with partial clear miscomparing. WA: Dither to be disabled.	SKL:SWIA_FROM_A0
0738	GTI		WaSetMDRBunitClckGatingDisable	Clkgating bugs in mdrbunit. WA: Disable clkgating on mdrbunit.	SKL:SWIA_FROM_A0
0740	3D			Groupd id select is not resettiing for media walker during context switch from media to GPGPU mode. WA: Need to disable media walker with groups.	SKL:SWIA_FROM_A0
0742	3D			In certain cases in 3D workload if CS is preempted in window of MI_RS_CONTROL(OFF) to MI_RS_CONTROL(ON), then CS may start RS for the instruction which are in RS disable window bracketed by MI_RS_CONTROL(OFF) to MI_RS_CONTROL(ON) after resubmission. WA: Whenever programming MI_RS_CONTROL(OFF), disable all the	SKL:SWIA_FROM_A0

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
				pools so that RS will not generate any produce after execution instruction from this MI_RS_CONTROL(OFF) to MI_RS_CONTROL(ON) zone.	
0743	3D		WaDisableIndirectDataAndFlushGPGPUWalker	VFE counter overflow due to missing pending_cntr signal for cntr3. WA: Limit urb entries to 63 and MI_ATOMIC_FLUSH need to be inserted after media curbe load command.	SKL:SWIA_UNTIL_G0
0750	3D			Mid Thread Preemption enabling causes VFE TSG hang in Media Context. WA: MEDIA_STATE_FLUSH need to programmed before MI_BATCH_BUFFER_END of the batch buffer with Media_Object or media object walker command.	SKL:SIWA_FOREVER
0752	3D		WaSamplerResponseLengthMustBeGreaterThan1	Dcs_pwc_rc signal is not set when notify clear comes out of phase WA: disable MMIO reads from GW & all sampler sends in GPGPU workloads with response length of 1.	SKL:SIWA_UNTIL_G0
0754	3D			Select_global_ts_vld typo need to be fixed in GT3 and GT4 mode. WA: Slice and subslice need to be changed it to slice[1:0], subslice[1:0].	SKL:SIWA_FROM_E0
0755	3D			Not able to preempt IDLE flush (rdop) when inhibit sync ctx sw is set. WA: SW must always program PIPE_CONTROL with "CS Stall" and "Render Target Cache Flush Enable"	SKL:SIWA_FROM_C0

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
				set prior to programming MI_WAIT_FOR_EVENT command for GPGPU workloads i.e when pipeline select is GPGPU via PIPELINE_SELECT command. This is required to achieve better GPGPU preemption latencies for certain programming sequences. If programming PIPE_CONTROL has performance implications then preemption latencies can be trade off against performance by not implementing this programming note.	
0760	3D			Pooled EU EUStressWorkload barrier hang. WA: Need to use bigger thread group workloads.	SKL:SIWA_UNTIL_G0
0762	GTI		WaSendExtraRSGatherConstantAndRSStoreImmCmds	RS sends Write and later L3 sends same Read. If GAFM gets GFX fence and do RS flush and stall RS, if RS WR comes, it will stay in FIFO due to STALL after fence, L3 read comes when RS is present in GAFM, L3 gets blocked due to same Address WR present. And gets hang as GAFM cannot respond flush due to this dead lock. WA: Inserting 5 STDW after RS cycle and once it is out then only send L3 RD cycle.	SKL:SIWA_FROM_A0

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
0763	GT			DOP Clock gating not supported when context switching due to preemption is disabled and a streamer wait condition is encountered. WA: Set inhibit_sync_contextswitch bit in this sceanrio. It will enable clock gating.	SKL:SIWA_FOREVER
0765	3D		WaDisableMidObjectPreemptionForTrifanOrPolygon	TriFan miscompare in Execlist Preemption test. Cut index that is on a previous context. End the previous, the resume another context with a tri-fan or polygon, and the vertex count is corrupted. If we prempt again we will cause corruption. WA: Disable mid-draw preemption when draw-call has a tri-fan.	SKL:SIWA_FOREVER
0771	3D			Issue in Trail mode - rd pointers getting corrupted. WA: Reoder mode bit in 3DSTATE_GS should be always leading.	SKL:SIWA_FROM_A0
0775	3D		WaLodRequiredOnTypedMsaaUav	Color buffer corruption in PS UAV test with typed MSAA reads enabled. WA: MSAA registers are not used in SKL (see HSD 2134364)	SKL: SIWA_FROM_C0
0776	3D		WaBarrierPerformanceFixDisable	Gw clearing N0 incorrectly without complete barrier hit. WA: Disable Barrier Performance DCN by programming MMIO register 7300, bit 14 to 1.	SKL:SIWA_FROM_E0

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
0778	3D			gpgpu_walker_valid need to be reset when start>=dim to avoid corruption in context image. WA: gpgpu_walker_valid need to be reset when dim=0 or start>= dim to avoid corruption in context image	SKL:SIWA_FROM_E0
0780	3D			Test hangs as stall_for_barrier_pre value held from 3d workload is affecting gpgpu workload which is submitted later. WA: Disable ACK removal DCN when using both 3d and GPGPU workloads together.	SKL:SIWA_FROM_E0
0794	3D	Media GPGPU		Address corruption from TSG to MCR when VFE state and global release message during 1-2 clock window: WA (SKL): An MI_FLUSH is required before MEDIA_VFE_STATE unless the only bits that are changed are scoreboard related: Scoreboard Enable, Scoreboard Type, Scoreboard Mask, Scoreboard * Delta. For these scoreboard related states, a MEDIA_STATE_FLUSH is sufficient if the last command is not media walker/media object group id with global barrier. WA: An MI_FLUSH is required before MEDIA_VFE_STATE unless the only bits that are changed are scoreboard related: Scoreboard Enable, Scoreboard Type, Scoreboard Mask, Scoreboard * Delta. For these	SKL:SIWA_FROM_F0

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
				scoreboard related states, a MEDIA_STATE_FLUSH is sufficient if the last command is not media walker/media object group id with local/global barrier.	
0796	3D			Preemption protocol of csr_dispatch_done followed by tsg_tdg_preemption is broken on Msflush with flushtogo. WA: MSFLUSH without watermark and flush-to-go need to be inserted before MSFLUSH with flush to go command.	SKL:SIWA_FROM_E0
0798	3D			VF is corrupting GAFS data when preempted on an instance boundary and replayed with instancing enabled. WA: Disable preemption when using instanceing.	SKL:SIWA_FROM_C0
0800	GTI	GA		Atomic fence is overtaking WCP eviction cycles on the GAM egress. WA: Add a backup 4AAC flush.	SKL:SIWA_FROM_B0
0803	GTI			F&H Faults pending with GFX reset GO0 seq is not getting completed. WA: Do a full reset if hit a gam fault.	SKL:SIWA_FROM_C0
0808	GTI			Atomic fence is overtaking WCP eviction cycles on the GAM egress. WA (SKL): Add a backup 4AAC flush.	SKL:SIWA_FROM_B0
0812	3D	Tiled resources		RCC cacheline is composed of X-adjacent 64B fragments instead of memory adjacent. This causes a single 128B cacheline to straddle multiple LODs inside the TYF MIPtail for 3D surfaces (beyond a certain slot	ALL

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
				number) , leading to corruption when CCS is enabled for these LODs and RT is later bound as texture. WA: If RENDER_SURFACE_STATE.Surface Type = 3D and RENDER_SURFACE_STATE.Auxiliary Surface Mode != AUX_NONE and RENDER_SURFACE_STATE.Tiled ResourceMode is TYF or TYS, Set the value of RENDER_SURFACE_STATE.Mip Tail Start LOD to a mip that larger than those present in the surface (i.e. 15)	
0816	3D			Vertex is dropped when the preempted on first vertex of a lineloop. This will cause corruption. WA: Disable mid-draw preemption when the draw uses a lineloop topology.	SKL:SIWA_FROM_C0
0825	3D		WaRTReadsOOBBehavior	The HW implementation returns zero in all components if the RTread pixel or sample is outside the primitive. WA: The DirectX spec requires that if the alpha component is not specified in the format, the alpha return value must be the default value of 0x1 for uint and sint number types and 1.0f for all other number types. The SW WA detects this case in the pixel shader and corrects it to match the DirectX spec required behavior.	SKL:ALL

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
0828	Display	PSR2		PSR2 screen corruptions when multiple regions are updated in a single frame. WA: Set 0x42080 bit 3 = 1 before enabling PSR2. The register can safely remain set when PSR2 is disabled.	SKL:ALL
0831	KMD		WaDisableSamplerPowerBypassForSOPingPong	SI can get stuck ping ponging rows in a 2-2-2 fashion instead of 1-1-1 leading to a ~3% performance reduction. WA: Disable sampler power bypass to avoid negatively impacting SO 'ping-pong' performance.	SKL: SIWA_FOREVER
0836	Display	Clocks		Increase timeout to 1ms for gt-driver pcode mailbox programming for CDCLK frequency changes. Pcode can take this long in extreme cases. Typical time is less than 200us.	SKL:ALL
0837	GAM		WaSpuriousIOMMUFaults	GT GAM HW prefetches context (or extended context) entry when a context is loaded, root pointer is updated or when there is a context cache flush. This prefetch happens without a memory transaction from the context. On this prefetch, if the context entry is a NULL (P=0), HW will generate a fault – invalid context entry. However, it is legal to have a NULL context entry, as long as no memory references are done via that context	SKL:ALL

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
				entry. WA: To avoid these spurious DMA faults, SW should mark the context entry as present (not a NULL entry), and mark the page tables as not present.	
0838	GTI			MGSR hang when MsgCh cycle arrives a couple clocks after IOSF SB shadow request. This is being brought up into the SW WA section for completeness. 0xD00[3:1] already indicate that bits should be set by SW. WA: Enable 0x0D00[3:1] fixes in SW for all Gen9 products.	SKL:ALL
0840	Display	Watermarks SAGV		Programming needed for SAGV to prevent underflows in multi-display scenarios. See Display Watermark Programming - Watermark Calculations section.	SKL:ALL
0851	Display	FBC		To prevent missed invalidations around the time FBC is being enabled, FBC render tracking must use the "Render Tracking With Nuke" method. See Frame Buffer Compression page.	SKL:ALL
0856	Display	Memory Bandwidth		Display underflow with high resolutions and multiple displays. WA: Restrict display configurations to fit within system memory bandwidth	SKL:ALL

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
				threshold. Increase watermarks at some system memory bandwidth thresholds. See Display Watermark Calculations and Display Mode Set Gen9 Display Resolution Support.	
0857	Display	Planes		Display underrun issues with Y & Yf Tiling. WA: Set the bit 13 of MMIO register 0x46430 to 1b.	SKL:ALL
0859	Display	FBC		This workaround helps to acheive better idle power savings when FBC is enabled. WA: set bit 31 of MMIO register 0x45000 to 1'b1.	SKL:ALL
0869	Display/Power	SRD		Workaround sequence for SRD/SFU Mode: Scenario: Display is in MBO mode and flip occurs other frame. Repeat: Frame Without Flip: Set PIPE_MISC[21] = '0'. Optionally driver can send flip to display. Unmask bit takes effect at next Vblank. Frame With Flip: Send Flip to display. Set PIPE_MISC[21] = '1'.	SKL:ALL

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
				Mask bit takes effect at next Vblank. In any scenario, PIPE_MISC[21] must not be set for more than 2 frames. Ex: If no flip is detected for several frames, driver must unmask PIPE_MISC[21].	
0872	3D	CS		Global Workaround Batch Buffer will not execute when enabled and Execution List mode is enabled. WA: Do not enable Global WABB when in Execution List mode.	SKL:ALL
0873	Display	FBC		Screen corruption observed with FBC when the front buffer is updated by host modify. WA: To prevent missed host invalidations around the time FBC is being enabled, enable Nuke on modify. Set bit 23 of MMIO register 0x43224 to 1'b1.	SKL:ALL
0874	GTI	MMIO	GAMGo0BeforeCPD	When the BGF receives these read-return packets towards the slice when the slice is in reset, it loses synchronization between the valid and the data parts of the transaction. Post this, any actual data returns will be sent with data that is not associated with that transaction, hence causing various problems like corrupted	SKL:ALL

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
				instructions, corrupted state etc. Also, since the valid signals and data signals are out of sync, the last data return can also get indefinitely held leading to L3 hangs waiting for data returns. WA: Initiate a GAM Go=0 sequence prior to all CPD enter flows to block all memory traffic.	
0876	GTI	CS	WaForceCsStallOnTimestampQueryOrDepthCount	Due to known HW issue specific to GT4; on a specific incident (few HW events must happens on the same clock under certain programming conditions) address, data and control fields corresponding to a PIPECONTROL command will get registered wrongly in hardware. Following this incident Fence Reports, Depth Statistic Report (Occlusion Query) and time_stamp reports will get corrupted leading to OS/KMD/UMD hangs. **Workaround (option-1):** PIEPCONTROL command programmed with “Post Sync Operation” set to “Write Timestamp” or “Write Depth Query” must also set “Command Streamer stall Enable” to ‘1’. **Workaround (option-2):** Software must memorize the event of programming “Post Sync Operation”	SKL:GT4 (all GT4 SKU's)

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
				set to “Write Timestamp” or “Write Depth Query” and must set “Pipecontrol Flush Enable” on next PIPECONTROL programmed. Note: Since the passing on the memorized event between UMD and KMD (ring buffer and batch buffer) is difficult, one way it could be addressed in following way. KMD must always program the first PIPECONTROL being programmed in the ringbuffer following the MI_BATCH_BUFFER_START with “Pipecontrol Flush Enable” set. KMD must always program PIPECONTROL with “Pipecontrol Flush Enable” set prior to programming MI_BATCH_BUFFER_START in the ring buffer. **OR** UMD must always program the first PIPECONTROL in the batch buffer with “Pipecontrol Flush Enable” set and must always program the last command in every dispatch of the batch buffer to a PIPECONTROL with “Pipecontrol Flush Enable” set.	

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
0877	3D	Pixel Shader		Hang possible when pixel shader dispatched with only header phases (R0-R2) WA: Enable a non-header phase (e.g. push constant) when dispatch would have been header-only.	SKL:ALL
0878	3D	Pixel Shader		Push constant buffer corruption possible. WA: Insert 2 zero-length PushConst_PS before every intended PushConst_PS update, issue a NULLPRIM after each of the zero len PC update to make sure CS commits them.	SKL:ALL
0880	Display	Clocks		Timeout for display cdclk mailbox programming increased from 1ms to 3ms to account for some corner cases that can exceed 1ms.	SKL:ALL
0883	Display	FBC		When FBC is enabled sometimes screen corruptions/system hangs obeserved under high memory bandwidth conditions. WA: Set the bit 8 of MMIO register 0x43224 to 1b. Set the bit 31 of MMIO register 0x45000 to 1b.	SKL:ALL

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
0884	Display	FBC+PSR		When FBC is enabled in DisplayPort PSR mode the CPU host modify writes may not get updated on the Display as expected. WA: Write 0x00000000 to MMIO register 0x700AC with every CPU host modify write.	SKL:ALL
0887	3D	URB SIMD8 Channel Mask		URB SIMD8 messages do not support some combinations of with mixed settings of EU execution masks with mixed settings of per-vertex Channel Masks. If an unsupported combination is selected, the EU can hang waiting on a read data completion. Workaround is either: • set all EU execution masks when Channel Masks are used, or • when EU execution masks have some cleared entries, either don't use Channel Masks data phase or set all Channel Masks to 0FFh.	SKL:ALL
0888	3D	URB SIMD8 Channel Mask		An address corruption can occur on writes, or a data hang can occur on reads, if a SIMD slot address is the most significant OWORD in a cache line and the length of the data is > 4 DWORDs and the per-vertex Channel	SKL:ALL

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
				Mask has mixed settings. The workaround is either • restrict all Slot0 - Slot7 offsets to be aligned on a cache line, so that accesses do not span a cache line, or • either don't use Channel Masks data phase or set all Channel Masks to 0FFh.	
0893	Display	Memory Bandwidth		Display underflow with high resolutions and multiple displays when using dual channel single rank memory. WA: Increase watermarks at some system memory bandwidth thresholds. See Display Watermark Calculations.	SKL:ALL