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Offices:
VIA Technologies Incorporated
Taiwan Office:
1st Floor, No. 531 Chung-Cheng Road, Hsin-Tien
Taipei, Taiwan ROC
Tel: 886-2-2218-5452
FAX: 886-2-2218-5453
Home page: http://www.via.com.tw

VIA Technologies Incorporated
USA Office:
940 Mission Court
Fremont, CA 94539
USA
Tel: 510-683-3300
FAX: 510-683-3301 or 510-687-4654
Home Page: http://www.viatech.com
## REVISION HISTORY

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<th>Revision</th>
<th>Initials</th>
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<td>LW</td>
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<thead>
<tr>
<th>Sub-Address (Bits [31:24]): 00-51h</th>
<th>...</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>HPARATYPE 02H: ATTRIBUTE OF TEXTURE STAGE N (HPARASUBTYPE: FEH)</strong></td>
<td>128</td>
</tr>
<tr>
<td>Sub-Address (Bits [31:24]): 00-13h</td>
<td>...</td>
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<tr>
<td><strong>HPARATYPE 03H: PALETTE (HPARASUBTYPE: 00-22H)</strong></td>
<td>138</td>
</tr>
<tr>
<td><strong>HPARATYPE 04H: VERTEX AND PRIMITIVE SETTING</strong></td>
<td>148</td>
</tr>
<tr>
<td>Sub-Address (Bits [31:24]): 00-AAh</td>
<td>...</td>
</tr>
<tr>
<td><strong>HPARATYPE 10H: COMMANDS FOR COMMAND REGULATOR</strong></td>
<td>166</td>
</tr>
<tr>
<td><strong>HPARATYPE 11H: COMMANDS FOR FRAME BUFFER SWAPPING AND CR’S MISCELLANEOUS SETTING</strong></td>
<td>166</td>
</tr>
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INTRODUCTION

This document contains detailed graphics registers descriptions and other general information for the Chrome9 HCM graphic engine. The graphics registers for the Chrome9 HCM main features and its underlying subsystems are described explicitly in the following chapters.

About This Programming Guide

The programming manual is organized into 2 volumes (Part I & Part II). A brief description of each chapter is given below:

Part I:

Introduction.
An overview of the Chrome9 HCM design features is given in this chapter, along with block diagram and reference list.

Register Overview
Register specifications for register addressing and I/O space division are shown in this chapter.

PCI Interface Register Descriptions
PCI interface summary table and detailed register descriptions are presented in this chapter.

VGA I/O Register Descriptions
This chapter provides detailed VGA-related register summary and descriptions. The various video modes support by the Chrome9 HCM controller are also included in the configuration section.

2D Engine Register Descriptions
In this chapter provides detailed 2D Engine register summary and descriptions.

DMA Register Descriptions
This chapter provides detailed DMA register summary and descriptions.

CBU Rotation Register Descriptions
This chapter provides detailed CBU rotation register summary and descriptions.

LVDS Register Descriptions
This chapter provides detailed LVDS register summary and descriptions.

Part II:

Video Display Engine Register Descriptions
This chapter provides detailed video display engine register summary and descriptions.

Video Capture Engine Register Descriptions
This chapter provides detailed video capture engine register summary and descriptions.
HQV Register Descriptions
This chapter provides detailed HQV register summary and descriptions.

Command Regulator (CR) Register Descriptions
This chapter provides detailed CR register summary and descriptions.

3D Engine Register Descriptions
This chapter provides detailed 3D Engine register summary and descriptions.
Supporting Products and Features

This document includes all the GFX registers for VIA VX855 and VX875. Please refer to Table 1 for the specification differences of VX855 and VX875 products.

This chip integrates functional modules of the traditional North Bridge and South Bridge chips, plus 3D/2D and Video Processors, Video Decoding Accelerator and controller for external display interface. The register set is partitioned into three blocks: North Module, South Module and Graphics and Video Module; of which, North Module and South Module registers are described in this System Programming Manual while graphics and video registers are described in the Graphics Programming Guide.

Table 1. VX855 / VX875 Series Comparison Table

<table>
<thead>
<tr>
<th>Product Model</th>
<th>VX855</th>
<th>VX875</th>
</tr>
</thead>
<tbody>
<tr>
<td>FSB Speed (MHz)</td>
<td>400-800</td>
<td>400-533</td>
</tr>
<tr>
<td>Memory Type</td>
<td>DDR2-800</td>
<td>DDR2-667</td>
</tr>
<tr>
<td></td>
<td>1.5V / 1.8V</td>
<td>1.5V / 1.8V</td>
</tr>
<tr>
<td>Snapshot Memory</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Core Voltage</td>
<td>1.2V</td>
<td>1.0V</td>
</tr>
<tr>
<td>Package Dimension</td>
<td>27x27mm FCBGA, 906 balls</td>
<td>21x21mm FCBGA, 945 balls</td>
</tr>
</tbody>
</table>
System Block Diagram

The block diagram for the Chrome9 HCM is shown Figure 1.

![Chrome9 HCM Block Diagram](image)

Figure 1. The Chrome9 HCM Block Diagram
VIDEO DISPLAY REGISTERS

This document provides detailed video display engine register summary table. Register descriptions on video playback / blending engine are followed in the sequent sections.

Video Display Registers

The Chrome9 HCM Graphic Engine has an integrated video playback and blending engine. The video playback engine can simultaneously support up to three live video windows, and each video window can be independently scaled. Two blending engines support the graphics-to-video blending, followed by video-to-video blending effect. The blending factor is from constant, alpha stream or is combined with graphics data. Table 2 summarizes the video playback and blending engine registers. Detail register description follows.

Table 2. Video Display Engine Registers

<table>
<thead>
<tr>
<th>Offset (Hex)</th>
<th>Register Name</th>
<th>Attribute</th>
</tr>
</thead>
<tbody>
<tr>
<td>203-200</td>
<td>Interrupt Flags &amp; Masks Control</td>
<td>RW</td>
</tr>
<tr>
<td>207-204</td>
<td>Address Flip Status</td>
<td>RO</td>
</tr>
<tr>
<td>20B-208</td>
<td>Alpha Window / HI (For Second Display) Horizontal and Vertical Location Start</td>
<td>RW</td>
</tr>
<tr>
<td>20F-20C</td>
<td>Alpha Window Horizontal and Vertical End &amp; HI (For Second Display) Center Offset</td>
<td>RW</td>
</tr>
<tr>
<td>213-210</td>
<td>Alpha Window Control</td>
<td>RW</td>
</tr>
<tr>
<td>217-214</td>
<td>CRT Starting Address</td>
<td>RW</td>
</tr>
<tr>
<td>21B-218</td>
<td>The Second Display Starting Address</td>
<td>RW</td>
</tr>
<tr>
<td>21F-21C</td>
<td>Alpha Stream Frame Buffer Stride</td>
<td>RW</td>
</tr>
<tr>
<td>223-220</td>
<td>Primary Display Color Key</td>
<td>RW</td>
</tr>
<tr>
<td>227-224</td>
<td>Alpha Window &amp; HI (For Second Display) Frame Buffer Starting Address</td>
<td>RW</td>
</tr>
<tr>
<td>22B-228</td>
<td>Chroma Key Lower Bound</td>
<td>RW</td>
</tr>
<tr>
<td>22F-22C</td>
<td>Chroma Key Upper Bound</td>
<td>RW</td>
</tr>
<tr>
<td>233-230</td>
<td>Video Stream 1 Control</td>
<td>RW</td>
</tr>
<tr>
<td>237-234</td>
<td>Video Window 1 Fetch Count</td>
<td>RW</td>
</tr>
<tr>
<td>23B-238</td>
<td>Video Window 1 Frame Buffer Y Starting Address 1</td>
<td>RW</td>
</tr>
<tr>
<td>23F-23C</td>
<td>Video Window 1 Frame Buffer Stride</td>
<td>RW</td>
</tr>
<tr>
<td>243-240</td>
<td>Video Window 1 Horizontal and Vertical Start Location</td>
<td>RW</td>
</tr>
<tr>
<td>247-244</td>
<td>Video Window 1 Horizontal and Vertical Ending Location</td>
<td>RW</td>
</tr>
<tr>
<td>24B-248</td>
<td>Video Window 1 Frame Buffer Y Starting Address 2</td>
<td>RW</td>
</tr>
<tr>
<td>24F-24C</td>
<td>Video Window 1 Display Zoom Control</td>
<td>RW</td>
</tr>
<tr>
<td>253-250</td>
<td>Video Window 1 Minify and Interpolation Control</td>
<td>RW</td>
</tr>
<tr>
<td>257-254</td>
<td>Video Window 1 Frame Buffer Y Starting Address 0</td>
<td>RW</td>
</tr>
<tr>
<td>25B-258</td>
<td>Video 1 FIFO Depth and Threshold Control</td>
<td>RW</td>
</tr>
<tr>
<td>25F-25C</td>
<td>Video Window 1 Horizontal and Vertical Starting Location Offset</td>
<td>RW</td>
</tr>
<tr>
<td>263-260</td>
<td>HI Control For Second Display</td>
<td>RW</td>
</tr>
<tr>
<td>267-264</td>
<td>The Second Display Color Key</td>
<td>RW</td>
</tr>
<tr>
<td>26B-268</td>
<td>V3 and Alpha Window FIFO Pre-threshold Control</td>
<td>RW</td>
</tr>
<tr>
<td>26F-26C</td>
<td>Video Window 1 Display Count On Screen Control</td>
<td>RW</td>
</tr>
<tr>
<td>273-270</td>
<td>HI Transparent Color For Second Display</td>
<td>RW</td>
</tr>
<tr>
<td>277-274</td>
<td>HI Inverse Color For Second Display</td>
<td>RW</td>
</tr>
<tr>
<td>27B-278</td>
<td>V3 and Alpha Window FIFO Depth and Threshold Control</td>
<td>RW</td>
</tr>
<tr>
<td>27F-27C</td>
<td>V3 Display Count On Screen Control</td>
<td>RW</td>
</tr>
<tr>
<td>283-280</td>
<td>Primary Display Second Color Key</td>
<td>RW</td>
</tr>
<tr>
<td>287-284</td>
<td>V1 Color Space Conversion &amp; Enhancement Control 1</td>
<td>RW</td>
</tr>
</tbody>
</table>
### Video Display Registers

<table>
<thead>
<tr>
<th>Offset (Hex)</th>
<th>Register Name</th>
<th>Attribute</th>
</tr>
</thead>
<tbody>
<tr>
<td>28B-288</td>
<td>V1 Color Space Conversion &amp; Enhancement Control 2</td>
<td>RW</td>
</tr>
<tr>
<td>28F-28C</td>
<td>Reserved</td>
<td>RO</td>
</tr>
<tr>
<td>293-290</td>
<td>Alpha Window/HI (For Primary Display) Ending Position</td>
<td>RW</td>
</tr>
<tr>
<td>297-294</td>
<td>3D AGP Pause Address MMIO Port</td>
<td>WO</td>
</tr>
<tr>
<td>29B-298</td>
<td>Compose Output Modes Select</td>
<td>RW</td>
</tr>
<tr>
<td>29F-29C</td>
<td>V3 Frame Buffer Starting Address 2</td>
<td>RW</td>
</tr>
<tr>
<td>2A3-2A0</td>
<td>V3 Control</td>
<td>RW</td>
</tr>
<tr>
<td>2A7-2A4</td>
<td>V3 Frame Buffer Starting Address 0</td>
<td>RW</td>
</tr>
<tr>
<td>2AB-2A8</td>
<td>V3 Frame Buffer Starting Address 1</td>
<td>RW</td>
</tr>
<tr>
<td>2AF-2AC</td>
<td>V3 Frame Buffer Stride</td>
<td>RW</td>
</tr>
<tr>
<td>2B3-2B0</td>
<td>V3 Horizontal and Vertical Start</td>
<td>RW</td>
</tr>
<tr>
<td>2B7-2B4</td>
<td>V3 Horizontal and Vertical End</td>
<td>RW</td>
</tr>
<tr>
<td>2BB-2B8</td>
<td>V3 and Alpha Window Fetch Count</td>
<td>RW</td>
</tr>
<tr>
<td>2BF-2BC</td>
<td>V3 Display Zoom Control</td>
<td>RW</td>
</tr>
<tr>
<td>2C3-2C0</td>
<td>V3 Minify &amp; Interpolation Control</td>
<td>RW</td>
</tr>
<tr>
<td>2C7-2C4</td>
<td>V3 Color Space Conversion &amp; Enhancement Control 1</td>
<td>RW</td>
</tr>
<tr>
<td>2CB-2C8</td>
<td>V3 Color Space Conversion &amp; Enhancement Control 2</td>
<td>RW</td>
</tr>
<tr>
<td>2CF-2CC</td>
<td>Reserved</td>
<td>RO</td>
</tr>
<tr>
<td>2D3-2D0</td>
<td>Graphics Hardware Cursor Mode Control</td>
<td>RW</td>
</tr>
<tr>
<td>2D7-2D4</td>
<td>Graphics Hardware Cursor Position</td>
<td>RW</td>
</tr>
<tr>
<td>2DB-2D8</td>
<td>Graphics Hardware Cursor Origin</td>
<td>RW</td>
</tr>
<tr>
<td>2DF-2DC</td>
<td>Graphics Hardware Cursor Background Color</td>
<td>RW</td>
</tr>
<tr>
<td>2E3-2E0</td>
<td>Graphics Hardware Cursor Foreground Color</td>
<td>RW</td>
</tr>
<tr>
<td>2E7-2E4</td>
<td>Reserved</td>
<td>RO</td>
</tr>
<tr>
<td>2EB-2E8</td>
<td>HI for Primary Display FIFO Control Signal</td>
<td>RW</td>
</tr>
<tr>
<td>2EF-2EC</td>
<td>HI for Primary Display Transparent color</td>
<td>RW</td>
</tr>
<tr>
<td>2F3-2F0</td>
<td>HI for Primary Display Control Signal</td>
<td>RW</td>
</tr>
<tr>
<td>2F7-2F4</td>
<td>HI for Primary Display Frame Buffer Starting Address</td>
<td>RW</td>
</tr>
<tr>
<td>2FB-2F8</td>
<td>HI for Primary Display Horizontal and Vertical Start</td>
<td>RW</td>
</tr>
<tr>
<td>2FF-2FC</td>
<td>HI for Primary Display Center Offset</td>
<td>RW</td>
</tr>
</tbody>
</table>

### Video Related Engines Register Space 2 (0x00001200 ~ 0x000013FF)

<table>
<thead>
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<th>Offset (Hex)</th>
<th>Register Name</th>
<th>Attribute</th>
</tr>
</thead>
<tbody>
<tr>
<td>1203-1200</td>
<td>Video 1 Gamma R Correction Control</td>
<td>RW</td>
</tr>
<tr>
<td>1207-1204</td>
<td>Video 1 Gamma G Correction Control</td>
<td>RW</td>
</tr>
<tr>
<td>120B-1208</td>
<td>Video 1 Gamma B Correction Control</td>
<td>RW</td>
</tr>
<tr>
<td>120F-120C</td>
<td>HI (For Primary Display) Inverse Color</td>
<td>RW</td>
</tr>
<tr>
<td>1223-1220</td>
<td>Video 3 Gamma R Correction Control</td>
<td>RW</td>
</tr>
<tr>
<td>1227-1224</td>
<td>Video 3 Gamma G Correction Control</td>
<td>RW</td>
</tr>
<tr>
<td>122B-1228</td>
<td>Video 3 Gamma B Correction Control</td>
<td>RW</td>
</tr>
<tr>
<td>122F-122C</td>
<td>Video 3 Horizontal and Vertical Starting Location Offset</td>
<td>RW</td>
</tr>
<tr>
<td>127F-1230</td>
<td>Reserved</td>
<td>RO</td>
</tr>
<tr>
<td>1283-1280</td>
<td>Interrupt Flags and Masks Control</td>
<td>RW</td>
</tr>
<tr>
<td>1287-1284</td>
<td>Logic Signature Setting</td>
<td>RW</td>
</tr>
<tr>
<td>128B-1288</td>
<td>Reserved</td>
<td>RO</td>
</tr>
<tr>
<td>128F-128C</td>
<td>Logic Signature Address Result 0</td>
<td>RW</td>
</tr>
<tr>
<td>1293-1290</td>
<td>IGA1 Display Position Counter 0</td>
<td>RO</td>
</tr>
<tr>
<td>1297-1294</td>
<td>IGA1 Display Position Counter 1</td>
<td>RO</td>
</tr>
<tr>
<td>129B-1298</td>
<td>IGA1 Display Position Counter 2</td>
<td>RW</td>
</tr>
<tr>
<td>129F-129C</td>
<td>Logic Signature Data Result 0</td>
<td>RW</td>
</tr>
<tr>
<td>12A3-12A0</td>
<td>IGA2 Display Position Counter 0</td>
<td>RO</td>
</tr>
<tr>
<td>12A7-12A4</td>
<td>IGA2 Display Position Counter 1</td>
<td>RO</td>
</tr>
<tr>
<td>12AB-12A8</td>
<td>IGA2 Display Position Counter 2</td>
<td>RW</td>
</tr>
</tbody>
</table>
### Video Display Registers

<table>
<thead>
<tr>
<th>Offset (Hex)</th>
<th>Register Name</th>
<th>Attribute</th>
</tr>
</thead>
<tbody>
<tr>
<td>12B3-12B0</td>
<td>Primary Display Data Color Space Conversion and Enhancement Control 1</td>
<td>RW</td>
</tr>
<tr>
<td>12B7-12B4</td>
<td>Primary Display Data Color Space Conversion and Enhancement Control 2</td>
<td>RW</td>
</tr>
<tr>
<td>12BB-12B8</td>
<td>Primary Display Data Color Space Conversion and Enhancement Control 3</td>
<td>RW</td>
</tr>
<tr>
<td>12BF-12BC</td>
<td>Primary Display Data Color Space Conversion and Enhancement Control 4</td>
<td>RW</td>
</tr>
<tr>
<td>12FF-12C0</td>
<td>Reserved</td>
<td>RO</td>
</tr>
</tbody>
</table>

#### Extended Video Engines Register Space 2 (0x00003200 ~ 0x000033FF)

<table>
<thead>
<tr>
<th>Offset (Hex)</th>
<th>Register Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>3260</td>
<td>DVD / Video ID Control</td>
</tr>
<tr>
<td>326C</td>
<td>DVD / Video Wait Control Register</td>
</tr>
</tbody>
</table>

Note:
1) Port Address: MB1 + Offset Address
   MB1 is declared in the register with offset address 17h-14h in the PCI configuration space.

2) There is additional register space to match the above register definition. When write a register to this space, it will be sent to “command regulator” first and then pass to video display engine. However, register read will be same as the original action. The relationship between the additional register space and original register space is:
   \( \text{(The additional register address)} = \text{(The original register address)} + 16'h2000. \)
### Video Display Engine Register Descriptions (200-12F0h)

**Offset Address:** 203-200h  
**Interrupt Flags and Masks Control**  
**Default Value:** 0000 0000h

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31  | RW 0      | Interrupt Enable  
0: Disable  
1: Enable |
| 30  | RW 0      | LVDS Sense Interrupt Enable  
0: Disable  
1: Enable |
| 29  | RW 0      | Capture 0 VBI Capture End Interrupt Enable  
0: Disable  
1: Enable |
| 28  | RW 0      | Capture 0 Active Video Data Capture End Enable  
0: Disable  
1: Enable |
| 27  | RW1C 0    | LVDS Sense Interrupt Status |
| 26  | RW 0      | Capture 1 VBI Capture End Interrupt Enable  
0: Disable  
1: Enable |
| 25  | RW 0      | First HQV Engine Interrupt Enable  
0: Disable  
1: Enable (Refer to 03D0h) |
| 24  | RW 0      | Capture 1 Active Video Data Capture End Enable  
0: Disable  
1: Enable |
| 23  | RW 0      | DMA1 Transfer Done Interrupt Enable  
0: Disable  
1: Enable |
| 22  | RW 0      | DMA1 Descriptor Done Interrupt Enable  
0: Disable  
1: Enable |
| 21  | RW 0      | DMA0 Transfer Done Interrupt Enable  
0: Disable  
1: Enable |
| 20  | RW 0      | DMA0 Descriptor Done Interrupt Enable  
0: Disable  
1: Enable |
| 19  | RW 0      | VGA VSYNC Interrupt Mask Enable  
0: Disable  
1: Enable |
| 18  | RW 0      | MC Complete Frame Interrupt Mask Enable  
0: Disable  
1: Enable |
| 17  | RW 0      | Secondary Display VSYNC Interrupt Enable  
0: Disable  
1: Enable |
| 16  | RW 0      | DVI Sense Interrupt Enable  
0: Disable  
1: Enable |
| 15  | RW1C 0    | Secondary Display VSYNC Interrupts Status |
| 14  | RW1C 0    | Capture 1 VBI Capture End Interrupt Status |
| 13  | RW1C 0    | Capture 0 VBI Capture End Interrupt Status |
| 12  | RW1C 0    | Capture 0 Active Video Data Capture End Interrupt Status |
| 11  | RW 0      | Second HQV Engine Interrupt Enable  
0: Disable  
1: Enable (Refer to 13D0h for more detail.) |
| 10  | RW 0      | Second HQV Engine Interrupt Status  
(Refer to 13D0h for more detail.) |
| 9   | RW1C 0    | First HQV Engine Interrupt Status  
(Refer to 03D0h for more detail.) |
| 8   | RW1C 0    | Capture 1 Active Video Data Capture End Interrupt Status |
| 7   | RW1C 0    | DMA 1 Transfer Done Interrupt Status |
| 6   | RW1C 0    | DMA 1 Descriptor Done Interrupt Status |
| 5   | RW1C 0    | DMA 0 Transfer Done Interrupt Status |
| 4   | RW1C 0    | DMA 0 Descriptor Done Interrupt Status |
| 3   | RW1C 0    | VGA VSYNC Interrupt Status |
| 2   | RW1C 0    | MC Complete Frame Interrupt Status |
| 1   | RO 0      | Vertical Blanking Status |
| 0   | RW1C 0    | DVI Sense Interrupt Status |
### Offset Address: 207-204h

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:12</td>
<td>RO</td>
<td>0</td>
<td><strong>Reserved</strong></td>
</tr>
</tbody>
</table>
| 11 | RO | 0 | Video Window 1 SW Flip Status (R)  
Write B0+254'h port to clear this bit. |
| 10 | RO | 0 | Video Window 3 SW Flip Status (R)  
Write B0+2A4'h port to clear this bit. |
| 9:6 | RO | 0 | **Reserved** |
| 5 | RW1C | 0 | CR Interrupt Status |
| 4 | RO | 0 | Alpha Window Starting Address Update Status  
0: Updated  
1: Not yet updated  
It will be set as writes Rx224, and be cleared as starting address is updated. |
| 3 | RO | 0 | Video Window 3 Starting Address Update Status  
0: Updated  
1: Not yet updated  
It will be set as writes Rx2A4, and be cleared as starting address is updated. |
| 2 | RO | 0 | IGA2 Vertical Blanking Status |
| 1 | RO | 0 | Graphics Starting Address Update Status  
0: Updated  
1: Not yet updated  
It will be set as writes Rx214, and be cleared as starting address is updated. |
| 0 | RO | 0 | Video Window 1 Starting Address Update Status  
0: Updated  
1: Not yet updated  
It will be set as writes Rx254, and be cleared as starting address is updated. |

### Offset Address: 20B-208h

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:27</td>
<td>RO</td>
<td>0</td>
<td><strong>Reserved</strong></td>
</tr>
</tbody>
</table>
| 26:16 | WO | 0 | Depend on Hardware Icon Enable (Rx260[0])  
*When Rx260[0]=0:*  
Alpha window horizontal (X) starting location  
*When Rx260[0]=1:*  
Hardware icon horizontal (X) starting location  
Unit: Pixel |
| 15:11 | RO | 0 | **Reserved** |
| 10:0 | WO | 0 | Depend on Hardware Icon Enable (Rx260[0])  
*When Write:*  
Alpha window vertical (Y) starting location  
*When Rx260[0]=0:*  
*When Rx260[0]=1:*  
Hardware icon vertical (Y) starting location  
Unit: Line  
*When Read:*  
Graphic Display Vertical Line Number  
Unit: Line |

### Offset Address: 20F-20Ch

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:27</td>
<td>RW</td>
<td>0</td>
<td><strong>Reserved</strong></td>
</tr>
</tbody>
</table>
| 26:16 | RW | 0 | Depend on Hardware Icon Enable (Rx260[0])  
*When Rx260[0]=0:*  
Alpha window horizontal (X) ending location  
*When Rx260[0]=1:*  
Hardware icon horizontal (X) center offset  
Unit: Pixel |
| 15:11 | RO | 0 | **Reserved** |
| 10:0 | RW | 0 | Depend on Hardware Icon Enable (Rx260[0])  
*When Rx260[0]=0:*  
bits[10:0] = Alpha window vertical (Y) ending location  
*When Rx260[0]=1:*  
bits[6:0] = Hardware icon vertical (Y) enter offset  
Unit: Line |
### Offset Address: 213-210h
#### Alpha Window Control

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:21</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 20:16 | RW | 0 | Alpha Stream Request Expire Number  
| | | | Unit: 4 Requests |
| 15:8 | RW | FFh | Constant Alpha Factor Setting For Graphics Blending |
| 7:2 | RO | 0 | Reserved |
| 1:0 | RW | 00b | Graphics Blending Alpha Select (Alpha*VID+(1-Alpha)*GRA)  
| | | | 00: Blending using constant alpha factor [15:8]  
| | | | 01: Alpha is from alpha stream  
| | | | 10: Alpha is from graphics stream  
| | | | 11: Reserved |

### Offset Address: 217-214h
#### CRT Starting Address Shadow

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31 | RW | 0 | IGA1 Down Scaling Flip  
| | | | Address equivalent to 3X5.EC[1] |
| 30 | RW | 0 | IGA1 Down Scaling Line Flip Enable |
| 29 | RO | 0 | Reserved |
| 28:0 | RW | 0 | Primary Display Starting Address or  
| | | | IGA1 Down Scaling Source Starting Address (Valid when 3X5.EC[0] = 1)  
| | | | Address equivalent to:  
| | | | 3X5.48 [4:0]  
| | | | 3X5.34 [7:0]  
| | | | 3X5.0C [7:0]  
| | | | 3X5.0D [7:0] |

Note: In monochrome mode, the “X” in the above table stands for “B”. In color mode, the “X” in the above table stands for “D”.

### Offset Address: 21B-218h
#### The Second Display Starting Address

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31:29 | RO | 0 | Display Address Selection  
| | | | 00: S.L.  
| | | | Others are not supported |
| 28:3 | RW | 0 | The Second Display Starting Address or  
| | | | IGA2 Down Scaling Source Starting Address (Valid when 3X5.E8[4] = 1)  
| | | | Unit: 8 bytes |
| 2 | RO | 0 | Reserved |
| 1 | RW | 0 | IGA2 Down Scaling Line Flip Enable |
| 0 | RW | 0 | IGA2 Down Scaling Flip  
| | | | Address equivalent to 3X5.E8[5]. |

Note: This register should be the same with 3X5.5E, 5D and 5C registers.

### Offset Address: 21F-21Ch
#### Alpha Stream Frame Buffer Stride

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:13</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 12:4 | RW | 0 | Alpha Stream Frame Buffer Stride  
| | | | Unit: 16 bytes |
| 3:0 | RO | 0 | Reserved |
### Video Display Registers

#### Offset Address: 223-220h

**Primary Display Color Key**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RW</td>
<td>0</td>
<td>CRT Color Key</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>For RGB10 color mode [29]</td>
</tr>
<tr>
<td>30</td>
<td>RW</td>
<td>0</td>
<td>CRT Color Key Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td>29</td>
<td>RW</td>
<td>0</td>
<td>CRT Color Key Inverse Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Display video if color key matches</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Display video if color key does not match</td>
</tr>
<tr>
<td>28:0</td>
<td>RW</td>
<td>0</td>
<td>CRT Color Key</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Bits [28:0]: For RGB10 color mode [28:0]</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Bits [23:0]: For 32-bit true color mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Bits [15:0]: For 565 high color mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Bits [14:0]: For 555 high color mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Bits [7:0]: For 256 color mode</td>
</tr>
</tbody>
</table>

#### Offset Address: 227-224h

**Alpha Window / Hardware Icon Frame Buffer Starting Address**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>30:29</td>
<td>RW</td>
<td>00b</td>
<td>Target of Frame Buffer Starting Address</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: S.L.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: S.F.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: L.L.</td>
</tr>
<tr>
<td>28:4</td>
<td>RW</td>
<td>0</td>
<td>Depend On Hardware Icon Enable (Rx260[0])</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Frame buffer starting address for alpha window</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Frame buffer starting address for hardware icon</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Unit: 16 bytes</td>
</tr>
<tr>
<td>3:0</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

#### Offset Address: 22B-228h

**Chroma Key Lower Bound**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RW</td>
<td>0</td>
<td>Chroma Key Lower for Y/G Bit [1]</td>
</tr>
<tr>
<td>30</td>
<td>RW</td>
<td>0</td>
<td>Chroma Key Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td>29</td>
<td>RW</td>
<td>0</td>
<td>Chroma Key Inverse Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Display video if chroma key does not match</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Display video if chroma key matches</td>
</tr>
<tr>
<td>28:0</td>
<td>RW</td>
<td>0</td>
<td>Chroma Key Lower</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>{[23:16], [31], [28]}: Y/G</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>{[15:8], [27:26]}: U/R</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>{[7:0], [25:24]}: V/B</td>
</tr>
</tbody>
</table>

#### Offset Address: 22F-22Ch

**Chroma Key Upper Bound**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>30</td>
<td>RW</td>
<td>0</td>
<td>Chroma Key Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Select video 3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Select video 1</td>
</tr>
<tr>
<td>29:0</td>
<td>RO</td>
<td>0</td>
<td>Chroma Key Upper</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>{[23:16], [29:28]}: Y/G</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>{[15:8], [27:26]}: U/R</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>{[7:0], [25:24]}: V/B</td>
</tr>
</tbody>
</table>
### Offset Address: 233-230h

**Video Stream 1 Control**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31  | RW        | 0       | V1 Display to CRT or the Second Display  
0: CRT  
1: Second display |
| 30  | RW        | 0       | V1 Window Pre-fetch Enable |
| 29  | RW        | 0       | V1 Window Gamma Function Enable |
| 28  | RW        | 0       | V1 Window De-Gamma Function Enable |
| 27  | RW        | 0       | V1 Window Adder Tile Mode Enable |
| 26:25 | RW      | 00b     | V1 Flip Control  
00: SW flip  
01: HW flip and triggered by the HQV engine.  
10: HW flip and triggered by the Capture Port 0.  
11: HW flip and triggered by the Capture Port 1. |
| 24  | RW        | 0       | V1 Frame to Field Enable  
0: Disable  
1: Enable  
If enabled, the stride will be 2 times of original values.  
This bit is valid at  
1. Software flip.  
2. HQV flip.  
3. Capture frame mode flip.  
4. MC frame mode flip. |
| 23  | RO        | 0       | Reserved |
| 22  | RW        | 0       | V1 De-interface Mode  
If enabled, hardware will add one line to the top of odd (bottom) field.  
0: Disable  
1: Enable |
| 21  | RW        | 0       | V1 Line Flip Only in Non Video Active Period Enable  
0: Disable  
1: Enable |
| 20:16 | RW      | 0       | V1 Request Expire Number (Unit: 4 requests) |
| 15:10 | RO      | 0       | Reserved |
| 9   | RW        | 0       | Divided V1 Flip for HQV Engine VSYNC Number to Half Enable  
0: Disable  
1: Enable |
| 8   | RW        | 0       | V1 Color Space Conversion Disable  
0: Enable  
1: Disable |
| 7   | RW        | 0       | V1 Color Space Conversion Chroma Sign Bits Conversion |
| 6:5 | RO        | 0       | Reserved |
| 4:2 | RW        | 000b    | V1 Stream Data Format  
000: YUV422  
001: RGB32  
010: RGB15  
011: RGB16  
100: YUV411  
101: RGB10  
Other : reserved |
| 1   | RO        | 0       | Reserved |
| 0   | RW        | 0       | V1 Enable  
0: Disable  
1: Enable |

---

### Offset Address: 237-234h

**Video Window 1 Fetch Count**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:30</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 29:20 | RW      | 0       | V1 Per Line Fetch Count  
It is equal to no-sizing line fetch count / minify times. (Unit: 16 bytes) |
| 19:0  | RO       | 0       | Reserved |
### Offset Address: 23B-238h
#### Video Window 1 Fetch Buffer Y Starting Address 1

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>30:29</td>
<td>RW 00b</td>
<td>0</td>
<td>Target of The Second Frame Buffer Starting Address</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: S.L.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: S.F.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: L.L.</td>
</tr>
<tr>
<td>28:3</td>
<td>RW 0</td>
<td>0</td>
<td>V1 Packed Mode</td>
</tr>
<tr>
<td>2:0</td>
<td>RO 0</td>
<td>0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

### Offset Address: 23F-23Ch
#### Video Window 1 Frame Buffer Stride

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:14</td>
<td>RO 0</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>13:4</td>
<td>RW 0</td>
<td>0</td>
<td>V1 Packed Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Frame buffer stride (Unit: 16 bytes)</td>
</tr>
<tr>
<td>3:0</td>
<td>RO 0</td>
<td>0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

### Offset Address: 243-240h
#### Video Window 1 Horizontal and Vertical Starting Location

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:27</td>
<td>RO 0</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>26:16</td>
<td>RW 0</td>
<td>0</td>
<td>Video Window 1 Horizontal (X) Starting Location</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(1). (Unit: pixel)</td>
</tr>
<tr>
<td>15:11</td>
<td>RO 0</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>10:0</td>
<td>RW 0</td>
<td>0</td>
<td>Video Window 1 Vertical (Y) Starting Location</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(1). (Unit: Line)</td>
</tr>
</tbody>
</table>

### Offset Address: 247-244h
#### Video Window 1 Horizontal and Vertical Ending Location

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:27</td>
<td>RO 0</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>26:16</td>
<td>RW 0</td>
<td>0</td>
<td>Video Window 1 Horizontal (X) Ending Location</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(1). (Unit: pixel)</td>
</tr>
<tr>
<td>15:11</td>
<td>RO 0</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>10:0</td>
<td>RW 0</td>
<td>0</td>
<td>Video Window 1 Vertical (Y) Ending Location</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(1). (Unit: Line)</td>
</tr>
</tbody>
</table>

### Offset Address: 24B-248h
#### Video Window 1 Frame Buffer Y Starting Address 2

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RO 0</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>30:29</td>
<td>RW 00b</td>
<td>0</td>
<td>Target of The Third Frame Buffer Starting Address</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: S.L.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: S.F.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: L.L.</td>
</tr>
<tr>
<td>28:3</td>
<td>RW 0</td>
<td>0</td>
<td>V1 Packed Mode</td>
</tr>
<tr>
<td>2:0</td>
<td>RO 0</td>
<td>0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
### Offset Address: 24F-24Ch

**Video Window 1 Display Zoom Control**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RW</td>
<td>0</td>
<td>Video Window 1 Horizontal (X) Zoom Enable</td>
</tr>
<tr>
<td>30:27</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>26:16</td>
<td>RW</td>
<td>0</td>
<td>Video Window 1 Vertical (Y) Zoom Enable</td>
</tr>
<tr>
<td>15</td>
<td>RW</td>
<td>0</td>
<td>Video Window 1 Vertical (Y) Zoom Factor</td>
</tr>
<tr>
<td>14:10</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>9:0</td>
<td>RW</td>
<td>0</td>
<td>Video Window 1 Vertical (Y) Zoom Factor</td>
</tr>
</tbody>
</table>

### Offset Address: 253-250h

**Video Window 1 Minify & Interpolation Control**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:27</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>26:24</td>
<td>RW</td>
<td>000b</td>
<td>Video Window 1 Horizontal (X) Minify Control</td>
</tr>
<tr>
<td>23:19</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>18:16</td>
<td>RW</td>
<td>000b</td>
<td>Video Window 1 Vertical (Y) Minify Control</td>
</tr>
<tr>
<td>15:3</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>2</td>
<td>RW</td>
<td>0</td>
<td>Video Luma-only Interpolation When the Vertical Interpolation Is Enabled</td>
</tr>
<tr>
<td>1</td>
<td>RW</td>
<td>0</td>
<td>Video Horizontal (X) Interpolation Mode Select</td>
</tr>
<tr>
<td>0</td>
<td>RW</td>
<td>0</td>
<td>Video Vertical (Y) Interpolation Mode Select</td>
</tr>
</tbody>
</table>
Offset Address: 257-254h

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31  | RO        | 0       | V1 Play Odd / Even Field Control  
This bit is valid when SW Playback and Field Base Picture are selected.
0: Play even field  
1: Play odd field |
| 30:29 | RO       | 00b     | Target of The First Frame Buffer Starting Address  
00: S.L.  
01: S.F.  
10: Reserved  
11: L.L. |
| 28:2 | RO        | 0       | V1 Packed Mode  
The first frame buffer starting address. (Unit : 4 bytes) |
| 1:0  | RO        | 0       | Reserved |

Note: In packed mode, we could use Rx254[3:2] to get  
1. No minify: 4 bytes alignment. Rx254[3:2] are valid  

Offset Address: 25B-258h

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31:24 | RW       | 0       | V1 FIFO Pre-threshold  
Let V1 issue request early. Normally, this value is greater than or equal to V1 FIFO threshold (Rx258[15:8]). (Unit : level) |
| 23:26 | RO       | 0       | Reserved |
| 15:8   | RW       | 0       | V1 FIFO Threshold  
Let V1 request priority from low to high. (Unit: level) |
| 7:0    | RW       | 0       | V1 FIFO Depth (-1)  
(Unit: level) |

Note: One level is equal to 16 bytes.

Offset Address: 25F-25Ch

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:27</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>26:16</td>
<td>RW</td>
<td>0</td>
<td>Video Window 1 Horizontal (X) Starting Location Offset (Unit: 16 bytes)</td>
</tr>
<tr>
<td>15:11</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>10:0</td>
<td>RW</td>
<td>0</td>
<td>Video Window 1 Vertical (Y) Starting Location Offset (Unit: Line)</td>
</tr>
</tbody>
</table>
### Offset Address: 263-260h

#### Hardware Icon (HI) Control (Only for Second Display)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31    | RW        | 0       | V4 Display Target Select  
0: Display to CRT  
1: Display to secondary display |
| 30    | RW        | 0       | V4 Window Pre-fetch Enable  
0: Disable  
1: Enable |
| 29    | RW        | 0       | HI + (1-aplha)*Graphics Mode  
0: Disable  
1: Enable |
| 28    | RW        | 0       | Alpha Value Source Select  (Only for the true color Hardware icon)  
0: From bits [23:16]  
1: From the bits [31:24] of hardware icon |
| 27:26 | RW        | 00b     | HI Window Size  
00: 32x32  
01: 64x64  
1x: 128x128  
Unit: Pixel * line |
| 25:24 | RW        | 00b     | HI Data Stream Format  
00: RGB555  
01: RGB565  
10: RGB32  
11: RGB10 |
| 23:20 | RO        | 0       | Reserved |
| 19:16 | RW        | Fh      | HI Constant Alpha [3:0] (HIAPA) |
| 15:12 | RW        | 0       | Alpha Changed Value (HICV) Per Frame As HI Fan In/Out Turn on (When Rx260[8]=1)  
ALPHAn[7:0] = ALPHAn-1[7:0] +/- HICV[3:0], where just ALPHAn[7:4] is valid alpha value and ALPHA0 = {HIAPA}. |
| 11:10 | RW        | 0       | DMA1 Descriptor Done Interrupt Enable  
0: Disable  
1: Enable |
| 9     | RW        | 0       | HI Fan In / Out Selector  
0: Default  
1: Fan in (+) |
| 8     | RW        | 0       | HI Fan In / Out Enable  
0: Disable  
1: Enable |
| 7:4   | RW        | Fh      | HI Constant Alpha[7:4] (HIAPA)  
The rest bits are put on [19:16]. |
| 3     | RO        | 0       | Reserved |
| 2     | RW        | 0       | HI Blending Enable  
0: Disable  
1: Enable |
| 1     | RO        | 0       | Reserved |
| 0     | RW        | 0       | HI Enable  
0: Disable  
1: Enable |
### Offset Address: 267-264h

#### The Second Display Color Key

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31  | RW        | 0       | The Second Display Color Key Bit [29] For RGB10 True Color Mode  

See also bits [28:0] for detail. |
| 30  | RW        | 0       | Second Display Color Key Enable  

0: Disable  
1: Enable |
| 29  | RW        | 0       | Second Display Color Key Inverse Control  

0: Display video if color key matches  
1: Display video if color key does not match |
| 28:0 | RW | 0 | The Second Display Color Key  

Bits [31,28:0]: For RGB10 true color mode  
Bits [23:0]: For 32-bit true color mode  
Bits [15:0]: For 565 high color mode  
Bits [14:0]: For 555 high color mode  
Bits [7:0]: For 256 color mode |

---

### Offset Address: 26B-268h

#### V3 and Alpha Window FIFO Pre-Threshold Control

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:23</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 22:16 | RW | 0 | Alpha Window FIFO Pre-threshold  

Let alpha engine issue request early.  This value is normally greater than or equal to the alpha engine FIFO threshold (Rx278[30:24]).  
Unit: Level |
| 15:8 | RO | 0 | Reserved |
| 7:0 | RW | 0 | V3 FIFO Pre-threshold  

Let V3 issue request early. This value is normally greater than or equal to V3 FIFO threshold (Rx278[15:8]).  
Unit: Level |

---

### Offset Address: 26F-26Ch

#### Video Window 1 Display Count On Screen Control

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:28</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>27:26</td>
<td>RW</td>
<td>0</td>
<td>V1 Vertical Line Count That Shows On Screen (Unit: Line)</td>
</tr>
<tr>
<td>25:12</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>11:0</td>
<td>RW</td>
<td>0</td>
<td>V1 Horizontal Pixel Count That Shows On Screen (-1) (Unit: Pixel)</td>
</tr>
</tbody>
</table>

---

### Offset Address: 273-270h

#### Hardware Icon (HI) Transparent Color (Only For Second Display)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:30</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 29:0 | RW | 0 | HI Transparent Color  

Bits [29:0]: For RGB10  
Bits [23:0]: For RGB32  
Bits [15:0]: For RGB565  
Bits [14:0]: For RGB555 |
### Offset Address: 277-274h
**Hardware Icon (HI) Inverse Color (Only For Second Display)**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:30</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 29:0 | RW | 0 | HI Inverse Color  
Bits [29:0]: For RGB10  
Bits [23:0]: For RGB32  
Bits [15:0]: For RGB565  
Bits [14:0]: For RGB555 |

### Offset Address: 27B-278h
**V3 and Alpha Window FIFO Depth and Threshold Control**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 30:24 | RW | 0 | Alpha Window FIFO Threshold  
Unit: Level |
| 23 | RO | 0 | Reserved |
| 22:16 | RW | 0 | Alpha Window FIFO Depth (-1)  
Unit: Level |
| 15:8 | RW | 0 | Video Window 3 FIFO Threshold  
Unit: Level |
| 7:0 | RW | 0 | Video Window 3 FIFO Depth (-1)  
Unit: Level |

Note: One level is equal to 16 bytes.

### Offset Address: 27F-27Ch
**Video Window 3 Display Count On Screen Control**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:28</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>27:26</td>
<td>RW</td>
<td>0</td>
<td>V3 Vertical Line Count That Shows On Screen (Unit: Line)</td>
</tr>
<tr>
<td>15:12</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>11:0</td>
<td>RW</td>
<td>0</td>
<td>V1 Horizontal Pixel Count That Shows On Screen (-1) (Unit: Pixel)</td>
</tr>
</tbody>
</table>

### Offset Address: 283-280h
**Primary Display Second Color Key**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 30 | RW | 0 | CRT Color Key Enable  
0: Disable  
1: Enable |
| 29 | RW | 0 | CRT Color Key Inverse Control  
0: Display video if color key matches  
1: Display video if color key does not match |
| 28:24 | RO | 0 | Reserved |
| 23:0 | RW | 0 | Primary Display Color Key  
Bits [23:0]: For 32-bit true color mode  
Bits [15:0]: For 565 high color mode  
Bits [14:0]: For 555 high color mode  
Bits [7:0]: For 256 color mode |
### Offset Address: 287-284h

**Video Window 1 Color Space Conversion and Enhancement Control 1**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31  | RW        | 0       | SDTV (BT601) Coefficient Enable  
0: Disable  
1: Enable |
| 30  | RW        | 0       | HDTV (BT709) Coefficient Enable  
0: Disable  
1: Enable |
| 29  | RO        | 0       | Reserved |
| 28:24| RW       | 0       | Coefficient A  
X.XXXX  From 0 to 1.9375 |
| 23:22| RO        | 0       | Reserved |
| 21:16| RW       | 0       | Coefficient B1  
SXX.XXX  S=1: negative, S=0: positive; from −2.125 to 2.125. |
| 15:14| RO        | 0       | Reserved |
| 13:8 | RW        | 0       | Coefficient C1  
SXX.XXX  S=1: negative, S=0: positive; from −2.125 to 2.125. |
| 7:0  | RW        | 0       | Coefficient D  
2’s complement integer; from -128 to 127. |

Note: R = AY+B1Cb+C1Cr+D

### Offset Address: 28B-288h

**Video Window 1 Color Space Conversion and Enhancement Control 2**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:29</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 28:24| RW        | 0       | Coefficient B2  
SXX.XXX  S=1: negative, S=0: positive; from −1.875 to 1.875. |
| 23:21| RO        | 0       | Reserved |
| 20:16| RW        | 0       | Coefficient C2  
SXX.XXX  S=1: negative, S=0: positive; from −1.875 to 1.875. |
| 15:14| RO        | 0       | Reserved |
| 13:8 | RW        | 0       | Coefficient B3  
SXX.XXX  S=1: negative, S=0: positive; from −3.875 to 3.875. |
| 7:6  | RO        | 0       | Reserved |
| 5:0  | RW        | 0       | Coefficient C3  
SXX.XXX  S=1: negative, S=0: positive; from −3.875 to 3.875. |

Note: G = AY+B2Cb+C2Cr+D  
B = AY+B3Cb+C3Cr+D

### Offset Address: 28F-28Ch – Reserved

### Offset Address: 293-290h

**Alpha Window / Hardware Icon (For Primary Display) Ending Position**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:28</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>27:16</td>
<td>RW</td>
<td>0</td>
<td>Hardware Icon Horizontal (X) Ending Position</td>
</tr>
<tr>
<td>15:11</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 10:0 | RW        | 0       | Hardware Icon Vertical (Y) Ending Position  
Unit: Line |

### Offset Address: 297-294h

**3D AGP Pause Address MMIO Port**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>RW</td>
<td>0</td>
<td>3D AGP Pause Address MMIO Port</td>
</tr>
</tbody>
</table>
### Offset Address: 29B-298h

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31  | RW        | 0       | Video 1 Command End, V1 Load New Register Setting  
|     |           |         | 1: Fire  
|     |           |         | If registers are updated to engine, this bit will be cleared to 0 and the default is set at 0. |
| 30  | RW        | 0       | Video 3 Command End, V3 Load New Register Setting  
|     |           |         | 1: Fire  
|     |           |         | If registers are updated to engine, this bit will be cleared to 0 and the default is set at 0. |
| 29  | RW        | 0       | Video Register Always Loaded  
|     |           |         | For hardware simulation and the default is set at 0. |
| 28  | RW        | 0       | Video Register Loaded at Vertical Blanking Without Waiting Source Flip  
|     |           |         | Need to write bit[31] or bit[30] and default is set at 0. |
| 27  | RW        | 0       | Video 3 Register Always Loaded  
|     |           |         | For hardware simulation and the default is set at 0. |
| 26  | RW        | 0       | Video 3 Register Loaded at Vertical Blanking Without Waiting Source Flip  
|     |           |         | Need to write bit[31] or bit[30] and default is set at 0. |
| 25:24| RW | 11b | Interpolation FIFO Clock Select  
|      |       |       | 00: Not in use  
|      |       |       | 01: V1 HDTV  
|      |       |       | 10: V3 HDTV  
|      |       |       | 11: V1 SDTV and V3 SDTV |
| 23:21| RO | 0     | Reserved |
| 20  | RW        | 0       | Video Output Overlap Control  
|     |           |         | 0: V1 is on top  
|     |           |         | 1: V3 is on top |
| 19:8| RO        | 0       | Reserved |
| 7   | RW        | 0       | MCK Bypass Enable  
|     |           |         | 0: Disable  
|     |           |         | 1: Enable |
| 6   | RO        | 0       | Reserved |
| 5   | RW        | 0       | Bypass LCD Horizontal Magnify Function |
| 4   | RW        | 0       | Bypass LCD Vertical Magnify Function |
| 3   | RW        | 0       | Video 3 Line Flip Enable  
|     |           |         | 0: Disable  
|     |           |         | 1: Enable |
| 2   | RW        | 0       | Video 1 Line Flip Enable  
|     |           |         | 0: Disable  
|     |           |         | 1: Enable |
| 1   | RO        | 0       | Reserved |
| 0   | RW        | 0       | Video 1 Round Control Enable  
|     |           |         | 0: Disable  
|     |           |         | 1: Enable |

### Offset Address: 29F-29Ch

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 30:29| RW | 00b | Target of The Third Frame Buffer Starting Address  
|      |       |         | 00: S.L.  
|      |       |         | 01: S.F.  
|      |       |         | 10: Reserved  
|      |       |         | 11: L.L. |
| 28:3| RW        | 0       | The Third Frame Buffer Starting Address of V3  
|     |           |         | Unit: 16 bytes |
| 2:0 | RO        | 0       | Reserved |
### Offset Address: 2A3-2A0h
#### Video Stream 3 Control

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 30    | RW        | 0       | V3 Window Pre-fetch Enable  
0: Disable  
1: Enable |
| 29    | RW        | 0       | V3 Window Gamma Function Enable  
0: Disable  
1: Enable |
| 28:27 | RO        | 0       | Reserved                                                                    |
| 26:25 | RW        | 00b     | V3 Flip Control  
00: SW flip  
01: HW flip and triggered by the HQV engine  
10: Reserved  
11: HW flip and triggered by the Capture Port 0  
11: HW flip and triggered by the Capture Port 1 |
| 24    | RW        | 0       | V3 Frame to Field Enable  
0: Disable  
1: Enable  
If enabled, the stride will be 2 times of original values.  
This bit is valid when software flip or HQV flip. |
| 23    | RO        | 0       | Reserved                                                                    |
| 22    | RW        | 0       | V3 De-interlace Mode  
0: Disable  
1: Enable |
| 21    | RW        | 0       | V3 Line Flip Only in Non Video Active Period Enable  
0: Disable  
1: Enable |
| 20:16 | RW        | 0       | V3 Request Expire Number  
Unit: 4 requests |
| 15:10 | RO        | 0       | Reserved                                                                    |
| 9     | RW        | 0       | Divided V3 Flip for HQV Engine VSYNC Number to Half  
0: Disable  
1: Enable |
| 8     | RW        | 0       | V3 Color Space Conversion  
0: Enable  
1: Disable |
| 7     | RW        | 0       | V3 Color Space Conversion Chroma Sign Bits Conversion  
0: Normal  
1: Inverse |
| 6:5   | RO        | 0       | Reserved                                                                    |
| 4:2   | RW        | 00b     | V3 Stream Data Format  
x00: YUV422  
x01: RGB32  
x10: RGB15  
x11: RGB16  
Others: Reserved |
| 1     | RO        | 0       | Reserved                                                                    |
| 0     | RW        | 0       | V3 Enable  
0: Disable  
1: Enable |

### Offset Address: 2A7-2A4h
#### Video Window 3 Frame Buffer Starting Address 0

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31    | RW        | 0       | V3 Play Odd / Even Field Control  
This bit is valid when SW Playback and Field Base Picture are selected.  
0: Play even field  
1: Play odd field |
| 30:29 | RO        | 00b     | Target of The First Frame Buffer Starting Address  
00: S.L.  
01: S.F.  
10: Reserved  
11: L.L. |
| 28:2  | RW        | 0       | The First Frame Buffer Starting Address of V3  
Unit: 4 bytes |
| 1:0   | RO        | 0       | Reserved                                                                    |
### Offset Address: 2AB-2A8h
**Video Window 3 Frame Buffer Starting Address 1**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>30:29</td>
<td>RW</td>
<td>00b</td>
<td>Target of The Second Frame Buffer Starting Address</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: S.L.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: S.F.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: L.L.</td>
</tr>
<tr>
<td>28:3</td>
<td>RW</td>
<td>0</td>
<td>The Second Frame Buffer Starting Address of V3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Unit: 16 bytes</td>
</tr>
<tr>
<td>2:0</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

### Offset Address: 2AF-2ACb
**Video Window 3 Frame Buffer Stride**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:14</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>13:4</td>
<td>RW</td>
<td>0</td>
<td>V3 Frame Buffer Stride</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Unit: 16 bytes</td>
</tr>
<tr>
<td>3:0</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

### Offset Address: 2B3-2B0h
**Video Window 3 Horizontal and Vertical Start**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:27</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>26:16</td>
<td>RW</td>
<td>0</td>
<td>V3 Horizontal (X) Starting Location</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Unit: Pixel</td>
</tr>
<tr>
<td>15:11</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>10:0</td>
<td>RW</td>
<td>0</td>
<td>V3 Vertical (Y) Starting Location</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Unit: Line</td>
</tr>
</tbody>
</table>

### Offset Address: 2B7-2B4h
**Video Window 3 Horizontal and Vertical End**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:27</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>26:16</td>
<td>RW</td>
<td>0</td>
<td>V3 Horizontal (X) Ending Location</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Unit: Pixel</td>
</tr>
<tr>
<td>15:11</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>10:0</td>
<td>RW</td>
<td>0</td>
<td>V3 Vertical (Y) Ending Location</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Unit: Line</td>
</tr>
</tbody>
</table>

### Offset Address: 2BB-2B8h
**Video Window 3 and Alpha Window Fetch Count**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:30</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>29:20</td>
<td>RW</td>
<td>0</td>
<td>V3 Per Line Fetch Count</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Unit: Pixel</td>
</tr>
<tr>
<td>19:10</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>9:0</td>
<td>RW</td>
<td>0</td>
<td>Alpha Window Per Line Fetch Count</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Unit: Line</td>
</tr>
</tbody>
</table>
### Offset Address: 2BF-2BCh

#### Video Window 3 Display Zoom Control

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RW</td>
<td>0</td>
<td>V3 Horizontal (X) Zoom Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td>30:27</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>26:16</td>
<td>RW</td>
<td>0</td>
<td>V3 Horizontal (X) Zoom Factor</td>
</tr>
<tr>
<td>15</td>
<td>RW</td>
<td>0</td>
<td>V3 Vertical (Y) Zoom Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td>14:10</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>9:0</td>
<td>RW</td>
<td>0</td>
<td>V3 Vertical (Y) Zoom Factor</td>
</tr>
</tbody>
</table>

### Offset Address: 2C3-2C0h

#### Video Window 3 Minify and Interpolation Control

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:27</td>
<td>RW</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>26:24</td>
<td>RW</td>
<td>000b</td>
<td>V3 Horizontal (X) Minify Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>000: No minify</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>001: Minify by a factor of 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>010: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>011: Minify by a factor of 4</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>101: Minify by a factor of 8</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>111: Minify by a factor of 16</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Others: Reserved.</td>
</tr>
<tr>
<td>23:19</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>18:16</td>
<td>RW</td>
<td>000b</td>
<td>V3 Vertical (Y) Minify Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>000: No minify</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>001: Minify by a factor of 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>010: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>011: Minify by a factor of 4</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>101: Minify by a factor of 8</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>111: Minify by a factor of 16</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Others: Reserved.</td>
</tr>
<tr>
<td>15:3</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>2</td>
<td>RW</td>
<td>0</td>
<td>V3 Luma-only Interpolation When The Vertical Interpolation Is Enabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Only luma values interpolated</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: All YUV/YcbCr values interpolated</td>
</tr>
<tr>
<td>1</td>
<td>RW</td>
<td>0</td>
<td>V3 Horizontal (X) Interpolation Mode Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Pixel is replicated</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable interpolation</td>
</tr>
<tr>
<td>0</td>
<td>RW</td>
<td>0</td>
<td>V3 Vertical (Y) Interpolation Mode Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 Pixel is replicated</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 Enable interpolation</td>
</tr>
</tbody>
</table>

Note: V1 and V3 can support interpolation simultaneously when both video source resolutions are lower than 800x600. If anyone exceeds the 800x600 resolution, only one of them can support interpolation. The control bit is defined at 0x298[25:24].
### Offset Address: 2C7-2C4h
**Video Window 3 Color Space Conversion and Enhancement Control 1**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31   | RW        | 0       | SDTV (BT601) Coefficient Enable  
0: Disable  
1: Enable |
| 30   | RW        | 0       | HDTV (BT709) Coefficient Enable  
0: Disable  
1: Enable |
| 29   | RO        | 0       | Reserved |
| 28:24| RW        | 0       | Coefficient A  
X.XXXX from 0 to 1.9375 |
| 23:22| RO        | 0       | Reserved |
| 21:16| RW        | 0       | Coefficient B1  
SXX.XXX  
S=1: negative, S=0: positive; from –2.125 to 2.125. |
| 15:14| RO        | 0       | Reserved |
| 13:8 | RW        | 0       | Coefficient C1  
SXX.XXX  
S=1: negative, S=0: positive; from –2.125 to 2.125. |
| 7:0  | RW        | 0       | Coefficient D[10:3]  
2’s complement integer; from -128 to 127. |

Note: R = AY + B1Cb + C1Cr + D

### Offset Address: 2CB-2C8h
**Video Window 3 Color Space Conversion and Enhancement Control 2**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31:29| RW        | 0       | Coefficient D[2:0]  
2’s complement integer; from -128 to 127. |
| 28:24| RW        | 0       | Coefficient B2  
SX.XXX  
S=1: negative, S=0: positive; from –1.875 to 1.875. |
| 23:21| RO        | 0       | Reserved |
| 20:16| RW        | 0       | Coefficient C2  
SX.XXX  
S=1: negative, S=0: positive; from –1.875 to 1.875. |
| 15:14| RO        | 0       | Reserved |
| 13:8 | RW        | 0       | Coefficient B3  
SXX.XX  
S=1: negative, S=0: positive; from 0 to 3.75. |
| 7:6  | RO        | 0       | Reserved |
| 5:0  | RW        | 0       | Coefficient C3  
SX.XX  
S=1: negative, S=0: positive; from –3.875 to 3.875. |

Note: G = AY + B2Cb + C2Cr + D, B = AY + B3Cb + C3Cr + D

### Offset Address: 2CF-2CCh
**Reserved**
### Offset Address: 2D3-2D0h

#### Graphic Hardware Cursor Mode Control

Default Value: 0000 0000h

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RW</td>
<td>0</td>
<td>Mono Cursor Display Path</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Primary</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Secondary</td>
</tr>
<tr>
<td>30:29</td>
<td>RW</td>
<td>00b</td>
<td>Target of The Hardware Cursor Buffer Starting Address</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: S.L.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: S.F.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: L.L.</td>
</tr>
<tr>
<td>28:26</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>25:8</td>
<td>RW</td>
<td>0</td>
<td>Hardware Cursor Base Address</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Up to 64M bytes</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>For 32x32x2 pattern: Bits [25:8] define the base address</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>For 64x64x2 pattern: Bits [25:10] define the base address</td>
</tr>
<tr>
<td>7:2</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>1</td>
<td>RW</td>
<td>0</td>
<td>Hardware Cursor Size</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: 64x64x2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: 32x32x2</td>
</tr>
<tr>
<td>0</td>
<td>RW</td>
<td>0</td>
<td>Hardware Cursor Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable</td>
</tr>
</tbody>
</table>

### Offset Address: 2D7-2D4h

#### Graphic Hardware Cursor Position

Default Value: 0000 0000h

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:27</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>26:16</td>
<td>RW</td>
<td>0</td>
<td>Hardware Cursor Position in the X-coordinate</td>
</tr>
<tr>
<td>15:11</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>10:0</td>
<td>RW</td>
<td>0</td>
<td>Hardware Cursor Position in the Y-coordinate</td>
</tr>
</tbody>
</table>

### Offset Address: 2DB-2D8h

#### Graphic Hardware Cursor Origin

Default Value: 0000 0000h

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:27</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>26:16</td>
<td>RW</td>
<td>0</td>
<td>Hardware Cursor Origin in the X-coordinate</td>
</tr>
<tr>
<td>15:11</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>10:0</td>
<td>RW</td>
<td>0</td>
<td>Hardware Cursor Origin in the Y-coordinate</td>
</tr>
</tbody>
</table>

### Offset Address: 2DF-2DCh

#### Graphic Hardware Cursor Background

Default Value: 0000 0000h

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:24</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>23:0</td>
<td>RW</td>
<td>0</td>
<td>For 256 Color Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Bits [7:0] specify hardware cursor background color</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>For 555 High Color Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Bits [14:0] specify hardware cursor background color</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>For 565 High Color Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Bits [15:0] specify hardware cursor background color</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>For 32-bits True Color Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Bits [23:0] specify hardware cursor background color</td>
</tr>
</tbody>
</table>
Offset Address: 2E3-2E0h
Graphic Hardware Cursor Foreground

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:24</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 23:0 | RW | 0 | For 256 Color Mode  
Bits [7:0] specify hardware cursor foreground color.  
For 555 High Color Mode  
Bits [14:0] specify hardware cursor foreground color.  
For 565 High Color Mode  
Bits [15:0] specify hardware cursor foreground color.  
For 32-bits True Color Mode  
Bits [23:0] specify hardware cursor foreground color. |

Table 3 below shows the hardware color cursor operation. Please be noted this table is only applicable to the graphics modes. For the text modes, the VGA registers control the hardware color cursor.

Table 3. Graphics Hardware Color Cursor Operation

<table>
<thead>
<tr>
<th>Pixel Operation</th>
<th>AND Plane</th>
<th>XOR Plane</th>
</tr>
</thead>
<tbody>
<tr>
<td>Choose graphics hardware color cursor background color</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Choose graphics hardware color cursor foreground color</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Transparent</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>VGA data is inverted</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Offset Address: 2E7-2E4h – Reserved

Offset Address: 2EB-2E8h
HI FIFO Depth and Threshold Control (Only For Primary Display)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31:24 | RW | 0 | HI FIFO Pre-threshold  
Let HI issue request early. Normally, this value is greater than or equal to HI FIFO threshold (Rx2E8[14:8]). (Unit: Level) |
| 23:16 | RO | 0 | Reserved |
| 15:8 | RW | 0 | HI FIFO Threshold  
Let HI request priority from low to high. (Unit: Level) |
| 7:0 | RO | 0 | HI FIFO Depth (-1)  
Unit: Level |

Offset Address: 2EF-2ECh
Hardware Icon (HI) Transparent Color (Only For Primary Display)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:30</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 29:0 | RW | 0 | HI Transparent Color  
Bits [29:0]: For RGB10  
Bits [23:0]: For RGB32  
Bits [15:0]: For RGB565  
Bits [14:0]: For RGB555 |
### Video Display Registers

#### Offset Address: 2F3-2F0h

**Hardware Icon (HI) Control (Only for Primary Display)**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>30</td>
<td>RW</td>
<td>0</td>
<td>HI Window Pre-fetch Enable</td>
</tr>
<tr>
<td>29</td>
<td>RW</td>
<td>0</td>
<td>HWI + (1-aplha) * Graphics Mode</td>
</tr>
</tbody>
</table>

- **0**: Disable
- **1**: Enable

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>28</td>
<td>RW</td>
<td>0</td>
<td>Alpha Value Come From Where</td>
</tr>
</tbody>
</table>

- **0**: From bits [7:4] and bits[19:16] (HIAPA) = 0
- **1**: From bits [31:24] of hardware icon

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>27:26</td>
<td>RW</td>
<td>00b</td>
<td>HI Window Size</td>
</tr>
</tbody>
</table>

- **00**: 32 x 32
- **01**: 64 x 64
- **1x**: 128 x 128 Unit: Pixel x line

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>25:24</td>
<td>RW</td>
<td>00b</td>
<td>HI Data Stream Format</td>
</tr>
</tbody>
</table>

- **00**: RGB555
- **01**: RGB565
- **10**: RGB32
- **11**: RGB10

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:20</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>19:16</td>
<td>RW</td>
<td>Fh</td>
<td>HI Constant Alpha [3:0] (HIAPA)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:12</td>
<td>RW</td>
<td>0</td>
<td>Alpha Changed Value (HICV) Per Frame as HI Fan In / Out Turn On (When Rx260[8] = 1)</td>
</tr>
</tbody>
</table>

ALPHA[7:0] = ALPHAn-1[7:0] +/- HICV[3:0], where just ALPHAn[7:4] is valid alpha value and ALPHA0 = (HIAPA)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>11:10</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>9</td>
<td>RW</td>
<td>0</td>
<td>HI Fan In / Out Selector</td>
</tr>
</tbody>
</table>

- **0**: Default
- **1**: Fan in (+)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>RW</td>
<td>0</td>
<td>HI Fan In / Out Enable</td>
</tr>
</tbody>
</table>

- **0**: Disable
- **1**: Enable

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:4</td>
<td>RW</td>
<td>Fh</td>
<td>HI Constant Alpha [7:4] (HIAPA)</td>
</tr>
</tbody>
</table>

The rest bits are put on bits [19:16].

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>2</td>
<td>RW</td>
<td>0</td>
<td>HI Blending Enable</td>
</tr>
</tbody>
</table>

- **0**: Default
- **1**: Enable

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>0</td>
<td>RW</td>
<td>0</td>
<td>HI Enable</td>
</tr>
</tbody>
</table>

- **0**: Default
- **1**: Enable

#### Offset Address: 2F7-2F4h

**Hardware Icon Frame Buffer Starting Address (Only For Primary Display)**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>30:29</td>
<td>RW</td>
<td>00b</td>
<td>Target of The Frame Buffer Starting Address</td>
</tr>
</tbody>
</table>

- **00**: S.L.
- **01**: S.F.
- **10**: Reserved
- **11**: L.L.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>28:4</td>
<td>RW</td>
<td>0</td>
<td>Frame Buffer Starting Address for Hardware Icon</td>
</tr>
</tbody>
</table>

Unit: 16 bytes

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3:0</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
### Offset Address: 2FB-2F8h
**Hardware Icon (HI) Horizontal and Vertical Location Start (Only For Primary Display)**  Default Value: 0000 0000h

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:27</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>26:16</td>
<td>RW</td>
<td>0</td>
<td>Hardware Icon Horizontal (X) Starting Location Unit: Pixel</td>
</tr>
<tr>
<td>15:11</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>10:0</td>
<td>RW</td>
<td>0</td>
<td>Hardware Icon Vertical (Y) Starting Location Unit: Line</td>
</tr>
</tbody>
</table>

### Offset Address: 2FF-2FCh
**Hardware Icon (HI) Center Offset (Only For Primary Display)**  Default Value: 0000 0000h

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:23</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>22:16</td>
<td>RW</td>
<td>0</td>
<td>Hardware Icon Horizontal (X) Center Offset Unit: Pixel</td>
</tr>
<tr>
<td>15:7</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>6:0</td>
<td>RW</td>
<td>0</td>
<td>Hardware Icon Vertical (Y) Center Offset Unit: Line</td>
</tr>
</tbody>
</table>

### Offset Address: 1203-1200h
**Video Gamma Color R Register for Video 1**  Default Value: 0000 0000h

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:26</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>25:16</td>
<td>RW</td>
<td>0</td>
<td>Color Value After Gamma Function</td>
</tr>
<tr>
<td>15:5</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>4:0</td>
<td>RW</td>
<td>0</td>
<td>Color Index Number for Gamma Function Division</td>
</tr>
</tbody>
</table>

### Offset Address: 1207-1204h
**Video Gamma Color G Register for Video 1**  Default Value: 0000 0000h

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:26</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>25:16</td>
<td>RW</td>
<td>0</td>
<td>Color Value After Gamma Function</td>
</tr>
<tr>
<td>15:5</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>4:0</td>
<td>RW</td>
<td>0</td>
<td>Color Index Number for Gamma Function Division</td>
</tr>
</tbody>
</table>

### Offset Address: 120B-1208h
**Video Gamma Color B Register for Video 1**  Default Value: 0000 0000h

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:26</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>25:16</td>
<td>RW</td>
<td>0</td>
<td>Color Value After Gamma Function</td>
</tr>
<tr>
<td>15:5</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>4:0</td>
<td>RW</td>
<td>0</td>
<td>Color Index Number for Gamma Function Division</td>
</tr>
</tbody>
</table>

### Offset Address: 120F-120Ch
**Hardware Icon (HI) Inverse Color (Only For Primary Display)**  Default Value: 0000 0000h

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:30</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>29:0</td>
<td>RW</td>
<td>0</td>
<td>HI Inverse Color</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Bits [29:0]: For RGB10</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Bits [23:0]: For RGB32</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Bits [15:0]: For RGB565</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Bits [14:0]: For RGB555</td>
</tr>
</tbody>
</table>
### Video Display Registers

#### Offset Address: 1223-1220h

**Video Gamma Color R Register for Video 3**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:26</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>25:16</td>
<td>RW</td>
<td>0</td>
<td>Color Value After Gamma Function</td>
</tr>
<tr>
<td>15:5</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>4:0</td>
<td>RW</td>
<td>0</td>
<td>Color Index Number for Gamma Function Division</td>
</tr>
</tbody>
</table>

#### Offset Address: 1227-1224h

**Video Gamma Color G Register for Video 3**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:26</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>25:16</td>
<td>RW</td>
<td>0</td>
<td>Color Value After Gamma Function</td>
</tr>
<tr>
<td>15:5</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>4:0</td>
<td>RW</td>
<td>0</td>
<td>Color Index Number for Gamma Function Division</td>
</tr>
</tbody>
</table>

#### Offset Address: 122B-1228h

**Video Gamma Color B Register for Video 3**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:26</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>25:16</td>
<td>RW</td>
<td>0</td>
<td>Color Value After Gamma Function</td>
</tr>
<tr>
<td>15:5</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>4:0</td>
<td>RW</td>
<td>0</td>
<td>Color Index Number for Gamma Function Division</td>
</tr>
</tbody>
</table>

#### Offset Address: 122F-122Ch

**Video Window 3 Horizontal and Vertical Starting Location Offset**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:27</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>26:16</td>
<td>RW</td>
<td>0</td>
<td>Video Window 3 Horizontal (X) Starting Location Offset (Unit: 16 bytes)</td>
</tr>
<tr>
<td>15:11</td>
<td>RO</td>
<td>0</td>
<td>Video Window 3 Vertical (Y) Starting Location Offset (Unit: Line)</td>
</tr>
</tbody>
</table>

#### Offset Address: 1283-1280h

**Interrupt Flags and Masks Control**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RW1C</td>
<td>0</td>
<td>MSI Pending Interrupt Re-trigger Bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When SW wants to exit interrupt service, please clear the bit. HW may send out interrupt again if pending interrupt exists. The function is enabled when MSI Enable = 1'b1.</td>
</tr>
<tr>
<td>30:20</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>19</td>
<td>RW</td>
<td>0</td>
<td>DMA3 Transfer Done Interrupt Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td>18</td>
<td>RW</td>
<td>0</td>
<td>DMA3 Descriptor Done Interrupt Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td>17</td>
<td>RW</td>
<td>0</td>
<td>DMA2 Transfer Done Interrupt Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td>16</td>
<td>RW</td>
<td>0</td>
<td>DMA2 Descriptor Done Interrupt Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td>15:5</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>4</td>
<td>RW1C</td>
<td>0</td>
<td>CRT Sense Interrupt Status</td>
</tr>
<tr>
<td>3</td>
<td>RW1C</td>
<td>0</td>
<td>DMA3 Transfer Done Interrupt Status</td>
</tr>
<tr>
<td>2</td>
<td>RW1C</td>
<td>0</td>
<td>DMA3 Descriptor Done Interrupt Status</td>
</tr>
<tr>
<td>1</td>
<td>RW1C</td>
<td>0</td>
<td>DMA2 Transfer Done Interrupt Status</td>
</tr>
<tr>
<td>0</td>
<td>RW1C</td>
<td>0</td>
<td>DMA2 Descriptor Done Interrupt Status</td>
</tr>
</tbody>
</table>
### Video Display Registers

**Offset Address: 1287-1284h**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:4</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>3</td>
<td>RW</td>
<td>0</td>
<td>Signature RD Disable Channel 0</td>
</tr>
<tr>
<td>2</td>
<td>RW</td>
<td>0</td>
<td>VSYNC Select Signal Channel 0</td>
</tr>
<tr>
<td>1</td>
<td>RW</td>
<td>0</td>
<td>Signature Enable Channel 0 from T-Arbiter</td>
</tr>
<tr>
<td>0</td>
<td>RW</td>
<td>0</td>
<td>Signature Enable Channel 0 from P-Arbiter</td>
</tr>
</tbody>
</table>

**Offset Address: 128B-1288h – Reserved**

**Offset Address: 128F-128Ch**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>RW</td>
<td>0</td>
<td>Logic Signature Adder Result 0</td>
</tr>
</tbody>
</table>

**Offset Address: 1293-1290h**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>RO</td>
<td>0</td>
<td>IGA1 Display Line Counter</td>
</tr>
<tr>
<td>15:0</td>
<td>RO</td>
<td>0</td>
<td>IGA1 Display Frame Counter</td>
</tr>
</tbody>
</table>

**Offset Address: 1297-1294h**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>15:0</td>
<td>RO</td>
<td>0</td>
<td>IGA1 Display Frame Counter</td>
</tr>
</tbody>
</table>

**Offset Address: 129B-1298h**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>15:0</td>
<td>RW</td>
<td>0</td>
<td>IGA1 Display Frame Counter Enable</td>
</tr>
</tbody>
</table>

When this bit is disabled, frame counter always gets 16'h0.

**Offset Address: 129F-129Ch**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>RW</td>
<td>0</td>
<td>Logic Signature Data Result 0</td>
</tr>
</tbody>
</table>

**Offset Address: 12A3-12A0h**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>RO</td>
<td>0</td>
<td>IGA2 Display Line Counter</td>
</tr>
<tr>
<td>15:0</td>
<td>RO</td>
<td>0</td>
<td>IGA2 Display Frame Counter</td>
</tr>
</tbody>
</table>
### Offset Address: 12A7-12A4h

**IGA2 Display Position Counter 1**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>15:0</td>
<td>RO</td>
<td>0</td>
<td>IGA2 Display Frame Counter</td>
</tr>
</tbody>
</table>

### Offset Address: 12AB-12A8h

**IGA2 Display Position Counter 2**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>15:0</td>
<td>RW</td>
<td>0</td>
<td>IGA2 Display Frame Counter Enable</td>
</tr>
</tbody>
</table>

0: Disable
1: Enable
When this bit is disabled, frame counter always gets 16’h0.

### Offset Address: 12B3-12B0h

**Primary Display Data Color Space Conversion and Enhancement Control 1**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:30</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>29:20</td>
<td>RW</td>
<td>0</td>
<td>A1 &lt;= XXXXXXXXXX</td>
</tr>
<tr>
<td>19:10</td>
<td>RW</td>
<td>0</td>
<td>B1 &lt;= XXXXXXXXXX</td>
</tr>
<tr>
<td>9:0</td>
<td>RW</td>
<td>0</td>
<td>C1 &lt;= XXXXXXXXXX</td>
</tr>
</tbody>
</table>

Note: Y = A1R + B1G + C1B + D
Coefficient A1, B1, C1: 10 bits, 0.XXXXXXXX from 0 to 0.99903  Coefficient D: 8 bit positive integer from 16 to 255

### Offset Address: 12B7-12B4h

**Primary Display Data Color Space Conversion and Enhancement Control 2**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:30</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>29:20</td>
<td>RW</td>
<td>0</td>
<td>A2[9:0] &lt;= XXXXXXXXXX</td>
</tr>
<tr>
<td>19:10</td>
<td>RW</td>
<td>0</td>
<td>B2[9:0] &lt;= XXXXXXXXXX</td>
</tr>
<tr>
<td>9:0</td>
<td>RW</td>
<td>0</td>
<td>C2[9:0] &lt;= XXXXXXXXXX</td>
</tr>
</tbody>
</table>

Note: Cr = A2R + B2G + C2B +128
Coefficient A2, B2, C2: 11 bits S.XXXXXXXX  2’s complement from -0.99903 to 0.99903

### Offset Address: 12BB-12B8h

**Primary Display Data Color Space Conversion and Enhancement Control 3**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:30</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>29:20</td>
<td>RW</td>
<td>0</td>
<td>A3[9:0] &lt;= XXXXXXXXXX</td>
</tr>
<tr>
<td>19:10</td>
<td>RW</td>
<td>0</td>
<td>B3[9:0] &lt;= XXXXXXXXXX</td>
</tr>
<tr>
<td>9:0</td>
<td>RW</td>
<td>0</td>
<td>C3[9:0] &lt;= XXXXXXXXXX</td>
</tr>
</tbody>
</table>

Note: Cr = A3R + B3G + C3B +128
Coefficient A3, B3, C3: 11 bits S.XXXXXXXX  2’s complement from -0.99903 to 0.99903

### Offset Address: 12BF-12BCh

**Primary Display Data Color Space Conversion and Enhancement Control 4**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:14</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>13</td>
<td>RW</td>
<td>0</td>
<td>A2[10] &lt;= S</td>
</tr>
<tr>
<td>12</td>
<td>RW</td>
<td>0</td>
<td>B2[10] &lt;= S</td>
</tr>
<tr>
<td>11</td>
<td>RW</td>
<td>0</td>
<td>C2[10] &lt;= S</td>
</tr>
<tr>
<td>10</td>
<td>RW</td>
<td>0</td>
<td>A3[10] &lt;= S</td>
</tr>
<tr>
<td>9</td>
<td>RW</td>
<td>0</td>
<td>B3[10] &lt;= S</td>
</tr>
<tr>
<td>8</td>
<td>RW</td>
<td>0</td>
<td>C3[10] &lt;= S</td>
</tr>
<tr>
<td>7:0</td>
<td>RW</td>
<td>0</td>
<td>D</td>
</tr>
</tbody>
</table>
DVD / Video Control Register (3260-326Ch)

Offset Address: 3260h
DVD / Video ID Control - Refer to CR Chapter’s “CR Registers in Video Control Register Space” for more details

Offset Address: 326Ch
DVD / Video Wait Control - Refer to CR Chapter’s “CR Registers in Video Control Register Space” for more details
VIDEO CAPTURE ENGINE REGISTERS

This document provides detailed video capture engine register summary table. Register descriptions on video capture engine registers are followed in the sequent sections.

Video Capture Engine Registers

These video capture engine register tables document the address offset, register name and register attribute for each register.

Table 4. Video Capture Engine

<table>
<thead>
<tr>
<th>Offset (Hex)</th>
<th>Register Name</th>
<th>Attribute</th>
</tr>
</thead>
<tbody>
<tr>
<td>303-300</td>
<td>Capture Interrupt Control and Flags</td>
<td>RW</td>
</tr>
<tr>
<td>307-304</td>
<td>Reserved</td>
<td>RO</td>
</tr>
<tr>
<td>30B-308</td>
<td>Transport Stream Control</td>
<td>RW</td>
</tr>
<tr>
<td>30F-30C</td>
<td>Reserved</td>
<td>RO</td>
</tr>
<tr>
<td>313-310</td>
<td>Capture Interface Control</td>
<td>RW</td>
</tr>
<tr>
<td>317-314</td>
<td>Active Video Horizontal Range (CCIR601 only)</td>
<td>RW</td>
</tr>
<tr>
<td>31B-318</td>
<td>Active Video Vertical Range (CCIR601 only)</td>
<td>RW</td>
</tr>
<tr>
<td>31F-31C</td>
<td>Active Video Scaling Control</td>
<td>RW</td>
</tr>
<tr>
<td>323-320</td>
<td>VBI Data Horizontal Range</td>
<td>RW</td>
</tr>
<tr>
<td>327-324</td>
<td>VBI Data Vertical Range</td>
<td>RW</td>
</tr>
<tr>
<td>32B-328</td>
<td>First VBI Buffer Starting Address</td>
<td>RW</td>
</tr>
<tr>
<td>32F-32C</td>
<td>VBI Buffer Stride</td>
<td>RW</td>
</tr>
<tr>
<td>333-330</td>
<td>Ancillary Data Count Setting</td>
<td>RW</td>
</tr>
<tr>
<td>337-334</td>
<td>Maximum Data Count of Active Video</td>
<td>RW</td>
</tr>
<tr>
<td>33B-338</td>
<td>Maximum Data Count of VBI or ANC</td>
<td>RW</td>
</tr>
<tr>
<td>33F-33C</td>
<td>Capture Data Count</td>
<td>RO</td>
</tr>
<tr>
<td>343-340</td>
<td>First Active Video Frame Buffer Starting Address</td>
<td>RW</td>
</tr>
<tr>
<td>347-344</td>
<td>Second Active Video Frame Buffer Starting Address</td>
<td>RW</td>
</tr>
<tr>
<td>34B-348</td>
<td>Third Active Video Frame Buffer Starting Address</td>
<td>RW</td>
</tr>
<tr>
<td>34F-34C</td>
<td>Second VBI Buffer Starting Address</td>
<td>RW</td>
</tr>
<tr>
<td>353-350</td>
<td>Stride of Active Video Buffer and Coring Function Control</td>
<td>RW</td>
</tr>
<tr>
<td>357-354</td>
<td>TS Buffer 0 Error Packet Indicator</td>
<td>RO</td>
</tr>
<tr>
<td>35B-358</td>
<td>TS Buffer 1 Error Packet Indicator</td>
<td>RO</td>
</tr>
<tr>
<td>35F-35C</td>
<td>TS Buffer 2 Error Packet Indicator</td>
<td>RO</td>
</tr>
</tbody>
</table>

Second Video Capture Engine Registers (Refer to Rx300-35C register descriptions for detail.)

<table>
<thead>
<tr>
<th>Offset (Hex)</th>
<th>Register Name</th>
<th>Attribute</th>
</tr>
</thead>
<tbody>
<tr>
<td>1303-1300</td>
<td>Capture Interrupt Control and Flags</td>
<td>RW</td>
</tr>
<tr>
<td>1307-1304</td>
<td>Reserved</td>
<td>RO</td>
</tr>
<tr>
<td>130B-1308</td>
<td>Transport Stream Control</td>
<td>RW</td>
</tr>
<tr>
<td>130F-130C</td>
<td>Reserved</td>
<td>RO</td>
</tr>
<tr>
<td>1313-1310</td>
<td>Capture Interface Control</td>
<td>RW</td>
</tr>
<tr>
<td>1317-1314</td>
<td>Active Video Horizontal Range (CCIR601 only)</td>
<td>RW</td>
</tr>
<tr>
<td>131B-1318</td>
<td>Active Video Vertical Range (CCIR601 only)</td>
<td>RW</td>
</tr>
<tr>
<td>131F-131C</td>
<td>Active Video Scaling Control</td>
<td>RW</td>
</tr>
<tr>
<td>1323-1320</td>
<td>VBI Data Horizontal Range</td>
<td>RW</td>
</tr>
<tr>
<td>1327-1324</td>
<td>VBI Data Vertical Range</td>
<td>RW</td>
</tr>
<tr>
<td>132B-1328</td>
<td>First VBI Buffer Starting Address</td>
<td>RW</td>
</tr>
<tr>
<td>132F-132C</td>
<td>VBI Buffer Stride</td>
<td>RW</td>
</tr>
<tr>
<td>1333-1330</td>
<td>Ancillary Data Count Setting</td>
<td>RW</td>
</tr>
<tr>
<td>1337-1334</td>
<td>Maximum Data Count of Active Video</td>
<td>RW</td>
</tr>
<tr>
<td>133B-1338</td>
<td>Maximum Data Count of VBI or ANC</td>
<td>RW</td>
</tr>
<tr>
<td>133F-133C</td>
<td>Capture Data Count</td>
<td>RO</td>
</tr>
<tr>
<td>Offset (Hex)</td>
<td>Register Name</td>
<td>Attribute</td>
</tr>
<tr>
<td>-------------</td>
<td>---------------------------------------------------------</td>
<td>-----------</td>
</tr>
<tr>
<td>1343-1340</td>
<td>First Active Video Frame Buffer Starting Address</td>
<td>RW</td>
</tr>
<tr>
<td>1347-1344</td>
<td>Second Active Video Frame Buffer Starting Address</td>
<td>RW</td>
</tr>
<tr>
<td>134B-1348</td>
<td>Third Active Video Frame Buffer Starting Address</td>
<td>RW</td>
</tr>
<tr>
<td>134F-134C</td>
<td>Second VBI Buffer Starting Address</td>
<td>RW</td>
</tr>
<tr>
<td>1353-1350</td>
<td>Stride of Active Video Buffer and Coring Function Control</td>
<td>RW</td>
</tr>
<tr>
<td>1357-1354</td>
<td>TS Buffer0 Error Packet Indicator</td>
<td>RO</td>
</tr>
<tr>
<td>135B-1358</td>
<td>TS Buffer1 Error Packet Indicator</td>
<td>RO</td>
</tr>
<tr>
<td>135F-135C</td>
<td>TS Buffer2 Error Packet Indicator</td>
<td>RO</td>
</tr>
<tr>
<td>1360-137C</td>
<td>Reserved</td>
<td>RO</td>
</tr>
</tbody>
</table>

Note:
1) Port Address: MB1 + Offset Address
   MB1 is declared in the register with offset address 17h-14h in the PCI configuration space.

2) There is additional register space to match the above register definition. When a command is written to that space, it will be sent to "command regulator" first and then pass to video display engine. However, register read will be the same as the original action. The relationship between the additional register space and original register space is:
   (The additional register address) = (The original register address) + 16'h2000
### Video Capture Engine Register Descriptions (300-35Fh)

**Offset Address: 303-300h**

Capture Interrupt Control and Flags

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:11</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>10</td>
<td>RW</td>
<td>0</td>
<td>Current Writing VBI Buffer ID</td>
</tr>
<tr>
<td>9</td>
<td>RW</td>
<td>0</td>
<td>End of VBI Interrupt Enable</td>
</tr>
<tr>
<td>8</td>
<td>RW</td>
<td>0</td>
<td>End of Active Video Interrupt Enable</td>
</tr>
<tr>
<td>7</td>
<td>RW</td>
<td>0</td>
<td>Video Capture Port Internal FIFO Full Status</td>
</tr>
<tr>
<td>6</td>
<td>RO</td>
<td>0</td>
<td>Current Active Video Input Field Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Top field</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Bottom field</td>
</tr>
<tr>
<td>5</td>
<td>RO</td>
<td>0</td>
<td>Current Input Vsync Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Vertical blanking</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Active video</td>
</tr>
<tr>
<td>4:3</td>
<td>RO</td>
<td>0</td>
<td>Current Writing Active Video (or TS Data) Frame Buffer ID</td>
</tr>
<tr>
<td>2</td>
<td>RO</td>
<td>0</td>
<td>Flipping Active Video Field Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Top field</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Bottom field</td>
</tr>
<tr>
<td>1</td>
<td>RW</td>
<td>0</td>
<td>Video Capture End-of-VBI Status</td>
</tr>
<tr>
<td>0</td>
<td>RW</td>
<td>0</td>
<td>Video Capture End-of-Active Video Status</td>
</tr>
</tbody>
</table>

**Offset Address: 30B-308h**

Transport Stream Control

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:23</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>22</td>
<td>RW</td>
<td>0</td>
<td>Serial Input Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Enable parallel TS input</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable serial TS input</td>
</tr>
<tr>
<td>21</td>
<td>RW</td>
<td>0</td>
<td>Bit Alignment</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Serial input mode only</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: LSB first</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: MSB first</td>
</tr>
<tr>
<td>20</td>
<td>RW</td>
<td>0</td>
<td>Packet Starting Signal Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Disable</td>
</tr>
<tr>
<td>19</td>
<td>RW</td>
<td>0</td>
<td>Change Buffer Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: According to count packet number</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: According to byte count</td>
</tr>
<tr>
<td>18:4</td>
<td>RW</td>
<td>0</td>
<td>When bit 19 = 0 Packet_Number_Minus_One</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>There are (Packet_Number_Minus_One + 1) packets per buffer.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When bit 19 = 1 KBytes_Count</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>There are KBytes_Count Kbytes per buffer.</td>
</tr>
<tr>
<td>3:2</td>
<td>RW</td>
<td>00b</td>
<td>Method to Move Received TS Data</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x: Capture engine writes data to FB (Frame Buffer). After filled a buffer, it will trigger an interrupt to driver.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: Capture engine writes data to FB. After filled a buffer, it will trigger an interrupt to DMA.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: Capture engine controls DMA to move data. (not via frame buffer) (In mode = 2'b11, set FIFO Threshold Rx310[27:24] to 1)</td>
</tr>
<tr>
<td>1</td>
<td>RW</td>
<td>0</td>
<td>Drop Error Packet</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This bit is valid only when TS_DERR pin is available</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Write all received data out</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Drop the data of error packet</td>
</tr>
<tr>
<td>0</td>
<td>RW</td>
<td>0</td>
<td>Transport Stream Input Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Turn on this bit before enabling capture engine Rx310[0].</td>
</tr>
</tbody>
</table>
## Offset Address: 313-310h

### Capture Interface Control

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31  | RW        | 0       | **Capture CLK Enable**  
|     |           |         | 0: Disable  
|     |           |         | 1: Enable  
|     |           |         | This bit should be turned on before setting Rx310[0]. |
| 30  | RW        | 0       | **Capture FIELD Signal Output Inverted Select**  
|     |           |         | 0: Normal  
|     |           |         | 1: Inverted |
| 29  | RW        | 0       | **Vertical Count Starting Reference**  
|     |           |         | 0: Negative edge of VREF  
|     |           |         | 1: Positive edge of VREF |
| 28  | RW        | 0       | **Horizontal Count Starting Reference**  
|     |           |         | 0: Negative edge of HREF  
|     |           |         | 1: Positive edge of HREF |
| 27:24 | RW | 0 | **Capture FIFO Threshold** (Unit: level)  
|      |           |         | Once the queuing captured data is more than the threshold, it starts to write data out. Unit of the 1st capture engine is 4-level, the FIFO size is 64-level x 64-bit. Unit of the 2nd capture engine is 2-level, the FIFO size is 32-level x 64-bit. |
| 23  | RW        | 0       | **Switch Capture Clock Source**  
|     |           |         | Since there are two capture clock sources, use this bit to switch it.  
|     |           |         | In VIP2.0 while using task bit to differentiate video stream, it needs to switch the clock source as the same one.  
|     |           |         | For 1st Capture Engine:  
|     |           |         | 0: Clock from 1st capture CLK pin  
|     |           |         | 1: Clock from 2nd capture CLK pin  
|     |           |         | For 2nd Capture Engine:  
|     |           |         | 0: Clock from 2nd capture CLK pin  
|     |           |         | 1: Clock from 1st capture CLK pin |
| 22  | RW        | 0       | **Capture FIELD Input Inverted Select**  
|     |           |         | 0: Normal  
|     |           |         | 1: Inverted |
| 21  | RW        | 0       | **Capture HREF Input Inverted Select**  
|     |           |         | 0: Normal  
|     |           |         | 1: Inverted |
| 20  | RW        | 0       | **Capture VREF Input Inverted Select**  
|     |           |         | 0: Normal  
|     |           |         | 1: Inverted |
| 19  | RW        | 0       | **Capture CLK Input Inverted Select**  
|     |           |         | 0: Normal  
|     |           |         | 1: Inverted |
| 18:16 | RW | 000b | **Capture Horizontal Filter Mode Select (2P)**  
|      |           |         | 000: No filtering  
|      |           |         | 001: 2 tap (1,1)/2  
|      |           |         | 010: 3 tap (1,2,1)/4  
|      |           |         | 011: 4 tap (1,3,3,1)/8  
|      |           |         | 100: 5 tap (1,2.2,2,1)/8  
|      |           |         | 101~111:Reserved |
| 15  | RW        | 0       | **Capture Flipping Control When Rx310[13:12] Is Set to 2'b11**  
|     |           |         | 0: Capture engine flips to HQV or video engine after captured a frame.  
|     |           |         | 1: Capture engine flips to HQV or video engine after captured a field (HQV or Video should set to frame to field). |
| 14  | RW        | 0       | **4:2:2 to 4:4:4 Cb, Cr Type Select**  
|     |           |         | 0: Duplication  
|     |           |         | 1: Interpolation |
| 13:12 | RW | 00b | **Capture De-interlace Mode Select**  
|      |           |         | 00: Capture odd field only, 30fps  
|      |           |         | 01: Capture even field only, 30fps  
|      |           |         | 10: Capture odd / even field, 60fps; place on the same location  
|      |           |         | 11: Capture odd / even field, 30fps; place in interlace fashion doubling the storage space |
| 11  | RW        | 0       | **Input FIELD Signal Enable**  
|     |           |         | If TS is enabled, it defines as TS_DERR signal enable.  
|     |           |         | 0: Disable  
|     |           |         | 1: Enable |
| 10  | RW        | 0       | **VIP Type**  
|     |           |         | 0: VIP1.1. VBI data region is specified by task bit.  
|     |           |         | 1: VIP2. VBI data region is specified by SAV / EAV during vertical blanking period. |
### Video Display Registers (Continued for Rx310h)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9:8</td>
<td>RW</td>
<td>00b</td>
<td><strong>Byte Swapping Control</strong>&lt;br&gt;00: 0123 (no swap: UYVY)&lt;br&gt;01: 1032 (C, Y swap: UYVY)&lt;br&gt;10: 0521 (C, Cr swap: YYVU)&lt;br&gt;11: 3012 (C, Cr swap and Y swap: VYUY)</td>
</tr>
<tr>
<td>7</td>
<td>RW</td>
<td>0</td>
<td><strong>16 Bit Input Low/High Swap</strong>&lt;br&gt;0: Not inverted&lt;br&gt;1: Low/high byte inverted</td>
</tr>
<tr>
<td>6</td>
<td>RW</td>
<td>0</td>
<td><strong>CCIR656-16 Bit Header Decode Mode</strong>&lt;br&gt;0: Low 8 bits&lt;br&gt;1: 16 bits all</td>
</tr>
<tr>
<td>5:4</td>
<td>RW</td>
<td>00b</td>
<td><strong>Input Stream Type</strong>&lt;br&gt;00: CCIR601, 8-bit&lt;br&gt;01: CCIR656, 8-bit&lt;br&gt;10: CCIR601, 16-bit&lt;br&gt;11: CCIR656, 16-bit</td>
</tr>
<tr>
<td>3</td>
<td>RW</td>
<td>0</td>
<td><strong>VIP Enable</strong>&lt;br&gt;0: Disable&lt;br&gt;1: Enable</td>
</tr>
<tr>
<td>2</td>
<td>RW</td>
<td>0</td>
<td><strong>Buffer Mode</strong>&lt;br&gt;0: Double buffers, use starting address 1 and 2&lt;br&gt;1: Triple buffers, use starting address 1, 2 and 3</td>
</tr>
<tr>
<td>1</td>
<td>RW</td>
<td>0</td>
<td><strong>Bit Stream Selection of VIP2.0</strong>&lt;br&gt;In VIP2.0, task bit to differentiate video stream.&lt;br&gt;For the 1st capture engine:&lt;br&gt;0: Capture the data of task bit is 0&lt;br&gt;1: Capture the data of task bit is 1&lt;br&gt;For the 2nd capture engine:&lt;br&gt;0: Capture the data of task bit is 1&lt;br&gt;1: Capture the data of task bit is 0</td>
</tr>
<tr>
<td>0</td>
<td>RW</td>
<td>0</td>
<td><strong>Capture Enable</strong>&lt;br&gt;0: Disable&lt;br&gt;1: Enable</td>
</tr>
</tbody>
</table>

**Offset Address: 317-314h**

**Active Video Horizontal Range**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:28</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>27:16</td>
<td>RW</td>
<td>0</td>
<td><strong>Horizontal Ending Cycle (CCIR601 only)</strong> (Unit: Cycle)</td>
</tr>
<tr>
<td>15:12</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>11:0</td>
<td>RW</td>
<td>0</td>
<td><strong>Horizontal Starting Cycle (CCIR601 only)</strong> (Unit: Cycle)</td>
</tr>
</tbody>
</table>

**Offset Address: 31B-318h**

**Active Video Vertical Range**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:27</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>26:16</td>
<td>RW</td>
<td>0</td>
<td><strong>Vertical Ending Line (CCIR601 only)</strong> (Unit: Line)</td>
</tr>
<tr>
<td>15:11</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>10:0</td>
<td>RW</td>
<td>0</td>
<td><strong>Vertical Starting Line (CCIR601 only)</strong> (Unit: Line)</td>
</tr>
</tbody>
</table>
### Offset Address: 31F-31Ch
#### Active Video Scaling Control

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:28</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>26</td>
<td>RW</td>
<td>0</td>
<td>Vertical Minify Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td>25:16</td>
<td>RW</td>
<td>0</td>
<td>Vertical Minify Factor</td>
</tr>
<tr>
<td>15:12</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>11</td>
<td>RW</td>
<td>0</td>
<td>Horizontal Minify Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td>10:0</td>
<td>RW</td>
<td>0</td>
<td>Horizontal Minify Factor</td>
</tr>
</tbody>
</table>

### Offset Address: 323-320h
#### VBI Data Horizontal Range

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:28</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>27:16</td>
<td>RW</td>
<td>0</td>
<td>Horizontal Ending Cycle (Unit: Cycle)</td>
</tr>
<tr>
<td>15:12</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>11:0</td>
<td>RW</td>
<td>0</td>
<td>Horizontal Starting Cycle (Unit: Cycle)</td>
</tr>
</tbody>
</table>

### Offset Address: 327-324h
#### VBI Data Vertical Range

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:27</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>26:16</td>
<td>RW</td>
<td>0</td>
<td>Vertical Ending Line (Unit: Line)</td>
</tr>
<tr>
<td>15:11</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>10:0</td>
<td>RW</td>
<td>0</td>
<td>Vertical Starting Line (Unit: Line)</td>
</tr>
</tbody>
</table>

### Offset Address: 32B-328h
#### First VBI Buffer Starting Address

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RW</td>
<td>0</td>
<td>VBI Data Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td>30</td>
<td>RW</td>
<td>0</td>
<td>VBI Mode Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Range depends on SAV/EAV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Capture by specific range (defined by register 320h, 324h)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When VIP is enabled (Rx310[3]=1), this bit setting would be ignored, capture VBI data is defined as VIP spec.</td>
</tr>
<tr>
<td>29</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>28:4</td>
<td>RW</td>
<td>0</td>
<td>VBI or ANC Buffer 0 Starting Address (Unit: 16 bytes)</td>
</tr>
<tr>
<td>3:2</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>1:0</td>
<td>RW</td>
<td>00b</td>
<td>Buffer Selection</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: S.L.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: S.F.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: S.M.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: L.L.</td>
</tr>
</tbody>
</table>

### Offset Address: 32F-32Ch
#### VBI Buffer Stride

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:14</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>13</td>
<td>RW</td>
<td>0</td>
<td>VBI Data Placement Method</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Linear, no stride needed</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: With stride</td>
</tr>
<tr>
<td>12:4</td>
<td>RW</td>
<td>0</td>
<td>VBI Buffer Stride (Unit: 16 bytes)</td>
</tr>
<tr>
<td>3:0</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
### Offset Address: 333-330h

**Ancillary Data Count Setting**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:15</td>
<td>RO</td>
<td>0</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>14</td>
<td>RW</td>
<td>0</td>
<td><strong>Ancillary Data Type</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Type2 – 00-FF-FF-DID-DDID-NN-…-…-CheckSumByte-FillBytes. Total captured data are (8Bytes + NN*4Bytes).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Type1 – 00-FF-FF-DDID-DDBN-NN-…-…-CheckSumByte-FillBytes. Total captured data are (8Bytes + (DBN+NN)*4Bytes).</td>
</tr>
<tr>
<td>13</td>
<td>RW</td>
<td>0</td>
<td><strong>Ancillary Data Enable</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td>12</td>
<td>RW</td>
<td>0</td>
<td><strong>Ancillary Data Count Reference Select</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: By header decoder</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: By register (define by Rx330[11:0])</td>
</tr>
<tr>
<td>11:0</td>
<td>RW</td>
<td>0</td>
<td><strong>Ancillary Data Should Be Capture Length</strong> (Unit: Double-word)</td>
</tr>
</tbody>
</table>

### Offset Address: 337-334h

**Maximum Data Count of Active Video**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:26</td>
<td>RO</td>
<td>0</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>26:16</td>
<td>RW</td>
<td>0</td>
<td><strong>Maximum Active Video Line Count In A Field</strong> (Unit: Line)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>If TS is enabled, it defines as the maximum TS data count of a packet (Unit: Byte).</td>
</tr>
<tr>
<td>15:9</td>
<td>RO</td>
<td>0</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>8:0</td>
<td>RW</td>
<td>0</td>
<td><strong>Maximum Active Video QW Count In A Line</strong> (Unit: 8 bytes)</td>
</tr>
</tbody>
</table>

### Offset Address: 33B-338h

**Maximum Data Count of VBI or ANC**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:26</td>
<td>RO</td>
<td>0</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>26:16</td>
<td>RW</td>
<td>0</td>
<td><strong>Maximum VBI or ANC Line Count In A Field</strong> (Unit: Line)</td>
</tr>
<tr>
<td>15:9</td>
<td>RO</td>
<td>0</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>8:0</td>
<td>RW</td>
<td>0</td>
<td><strong>Maximum VBI or ANC QW Count In A Line</strong> (Unit: 8 bytes)</td>
</tr>
</tbody>
</table>

### Offset Address: 33F-33Ch

**Capture Data Count**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:27</td>
<td>RO</td>
<td>0</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>26:16</td>
<td>RW</td>
<td>0</td>
<td><strong>Current Active Video Line Counter</strong> (Unit: Line)</td>
</tr>
<tr>
<td>15:13</td>
<td>RO</td>
<td>0</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>12:0</td>
<td>RW</td>
<td>0</td>
<td><strong>VBI or ANC Data Length That Has Been Captured</strong> (Unit: 8 bytes)</td>
</tr>
</tbody>
</table>

### Offset Address: 343-340h

**First Active Video Frame Buffer Starting Address**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:29</td>
<td>RO</td>
<td>0</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>28:4</td>
<td>RW</td>
<td>0</td>
<td><strong>Active Video Frame Buffer 0 Starting Address</strong> (Unit: 16 bytes)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>If TS is enabled, it defines as frame buffer 0 starting address for TS data.</td>
</tr>
<tr>
<td>3:2</td>
<td>RO</td>
<td>0</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>1:0</td>
<td>RW</td>
<td>00b</td>
<td><strong>Buffer Selection</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: S.L.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: S.F.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: S.M.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: L.L.</td>
</tr>
</tbody>
</table>
### Offset Address: 347-344h
**Second Active Video Frame Buffer Starting Address**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:29</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>28:4</td>
<td>RW</td>
<td>0</td>
<td>Active Video Frame Buffer 1 Starting Address (Unit: 16 bytes)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>If TS is enabled, it defines as frame buffer 1 starting address for TS data.</td>
</tr>
<tr>
<td>3:2</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>1:0</td>
<td>RW</td>
<td>00b</td>
<td>Buffer Selection</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: S.L.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: S.F.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: S.M.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: L.L.</td>
</tr>
</tbody>
</table>

### Offset Address: 34B-348h
**Third Active Video Frame Buffer Starting Address**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:29</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>28:4</td>
<td>RW</td>
<td>0</td>
<td>Active Video Frame Buffer 2 Starting Address (Unit: 16 bytes)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>If TS is enabled, it defines as frame buffer 2 starting address for TS data.</td>
</tr>
<tr>
<td>3:2</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>1:0</td>
<td>RW</td>
<td>00b</td>
<td>Buffer Selection</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: S.L.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: S.F.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: S.M.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: L.L.</td>
</tr>
</tbody>
</table>

### Offset Address: 34F-34Ch
**Second VBI Buffer Starting Address**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:29</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>28:4</td>
<td>RW</td>
<td>0</td>
<td>VBI or ANC Buffer 1 Starting Address (Unit: 16 bytes)</td>
</tr>
<tr>
<td>3:2</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>1:0</td>
<td>RW</td>
<td>00b</td>
<td>Buffer Selection</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: S.L.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: S.F.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: S.M.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: L.L.</td>
</tr>
</tbody>
</table>

### Offset Address: 353-350h
**Stride of Active Video Buffer & Coring Function Control**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:24</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>23</td>
<td>RW</td>
<td>0</td>
<td>Coring Function Enable</td>
</tr>
<tr>
<td>22:16</td>
<td>RW</td>
<td>0</td>
<td>Coring Function Compare Data (CCD)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>If coring function is enabled (Rx350[23]) and (-CCD+1) &lt;= U, V &lt;= CCD, all of these U and V will be truncated to zero.</td>
</tr>
<tr>
<td>15:13</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>12:4</td>
<td>RW</td>
<td>0</td>
<td>Stride of Active Video Buffer (Unit: 8 bytes)</td>
</tr>
<tr>
<td>3:0</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
### Offset Address: 357-354h
#### TS Buffer 0 Error Packet Indicator
<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RO</td>
<td>0</td>
<td><strong>Last Error Packet Indicator</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Less than one error packet in this buffer, defined at bits [15:0]</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: More than two error packets, the last error packet ID defined at bits [30:16]</td>
</tr>
<tr>
<td>30:16</td>
<td>RO</td>
<td>0</td>
<td><strong>Last Error Packet ID</strong></td>
</tr>
<tr>
<td>15</td>
<td>RO</td>
<td>0</td>
<td><strong>First Error Packet Indicator</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: No error packet in this buffer</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: More than one error packet, the first error packet ID defined at bits [14:0]</td>
</tr>
<tr>
<td>14:0</td>
<td>RO</td>
<td>0</td>
<td><strong>First Error Packet ID</strong></td>
</tr>
</tbody>
</table>

### Offset Address: 35B-358h
#### TS Buffer 1 Error Packet Indicator
<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RO</td>
<td>0</td>
<td><strong>Last Error Packet Indicator</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Less than one error packet in this buffer, defined at bits [15:0]</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: More than two error packets, the last error packet ID defined at bits [30:16]</td>
</tr>
<tr>
<td>30:16</td>
<td>RO</td>
<td>0</td>
<td><strong>Last Error Packet ID</strong></td>
</tr>
<tr>
<td>15</td>
<td>RO</td>
<td>0</td>
<td><strong>First Error Packet Indicator</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: No error packet in this buffer</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: More than one error packet, the first error packet ID defined at bits [14:0]</td>
</tr>
<tr>
<td>14:0</td>
<td>RO</td>
<td>0</td>
<td><strong>First Error Packet ID</strong></td>
</tr>
</tbody>
</table>

### Offset Address: 35F-35Ch
#### TS Buffer 2 Error Packet Indicator
<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RO</td>
<td>0</td>
<td><strong>Last Error Packet Indicator</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Less than one error packet in this buffer, defined at bits [15:0]</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: More than two error packets, the last error packet ID defined at bits [30:16]</td>
</tr>
<tr>
<td>30:16</td>
<td>RO</td>
<td>0</td>
<td><strong>Last Error Packet ID</strong></td>
</tr>
<tr>
<td>15</td>
<td>RO</td>
<td>0</td>
<td><strong>First Error Packet Indicator</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: No error packet in this buffer</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: More than one error packet, the first error packet ID defined at bits [14:0]</td>
</tr>
<tr>
<td>14:0</td>
<td>RO</td>
<td>0</td>
<td><strong>First Error Packet ID</strong></td>
</tr>
</tbody>
</table>

Note:
Capture supports 2 input interfaces; therefore, an additional register space is provided to match the above registers definition.

A write to this additional register space will send the data to the second Capture Engine.
The relationship between the additional register space and original register space is
(The additional register address) = (The original register address) + 16'h1000.
## HQV Registers

This section provides detailed HQV register summary table. Register descriptions on high quality video registers are followed in the sequent sections.

### HQV Registers

These HQV register tables document the I/O port, I/O index and attribute (“Attribute”) for each register.

#### Table 5. High Quality Video Registers

<table>
<thead>
<tr>
<th>Offset (Hex)</th>
<th>Register Name</th>
<th>Attribute</th>
</tr>
</thead>
<tbody>
<tr>
<td>363-360</td>
<td>HQV Color Adjustment Control 1</td>
<td>RW</td>
</tr>
<tr>
<td>367-364</td>
<td>HQV Color Adjustment Control 2</td>
<td>RW</td>
</tr>
<tr>
<td>36B-368</td>
<td>HQV Color Adjustment Control 3</td>
<td>RW</td>
</tr>
<tr>
<td>36F-36C</td>
<td>HQV Color Adjustment Control 4</td>
<td>RW</td>
</tr>
<tr>
<td>373-370</td>
<td>HQV Video Start Point Offset Control in Source</td>
<td>RW</td>
</tr>
<tr>
<td>377-374</td>
<td>HQV Sub-picture Start Point Offset Control in Source</td>
<td>RW</td>
</tr>
<tr>
<td>37B-378</td>
<td>HQV Video End Point Offset Control in Source</td>
<td>RW</td>
</tr>
<tr>
<td>37F-37C</td>
<td>HQV Sub-picture End Point Offset Control in Source</td>
<td>RW</td>
</tr>
<tr>
<td>383-380</td>
<td>HQV Video Start point Offset Control in Destination</td>
<td>RW</td>
</tr>
<tr>
<td>387-384</td>
<td>HQV Sub-picture Start Point Offset Control in Destination</td>
<td>RW</td>
</tr>
<tr>
<td>38B-388</td>
<td>HQV Video End Point Offset Control in Destination</td>
<td>RW</td>
</tr>
<tr>
<td>38F-38C</td>
<td>HQV Sub-picture End Point Offset Control in Destination</td>
<td>RW</td>
</tr>
<tr>
<td>393-390</td>
<td>HQV Parameters of Hardware Tuning Performance/Quality</td>
<td>RW</td>
</tr>
<tr>
<td>397-394</td>
<td>HQV Extended Control</td>
<td>RW</td>
</tr>
<tr>
<td>39B-398</td>
<td>HQV Static Record Frame Buffer Starting Address</td>
<td>RW</td>
</tr>
<tr>
<td>39F-39C</td>
<td>HQV Static Record Frame Buffer Stride</td>
<td>RW</td>
</tr>
<tr>
<td>3A3-3A0</td>
<td>HQV Color Adjustment Control 5</td>
<td>RW</td>
</tr>
<tr>
<td>3A7-3A4</td>
<td>HQV Color Adjustment Control 6</td>
<td>RW</td>
</tr>
<tr>
<td>3AB-3A8</td>
<td>HQV Color Adjustment Control 7</td>
<td>RW</td>
</tr>
<tr>
<td>3AF-3AC</td>
<td>HQV Color Adjustment Control 8</td>
<td>RW</td>
</tr>
<tr>
<td>3B3-3B0</td>
<td>HQV Video Horizontal Scale Control</td>
<td>RW</td>
</tr>
<tr>
<td>3B7-3B4</td>
<td>HQV Video Vertical Scale Control</td>
<td>RW</td>
</tr>
<tr>
<td>3BB-3B8</td>
<td>HQV Background Color</td>
<td>RW</td>
</tr>
<tr>
<td>3BF-3BC</td>
<td>HQV Segment Residue Pixel Frame Buffer Starting Address</td>
<td>RW</td>
</tr>
<tr>
<td>3C3-3C0</td>
<td>HQV Sub-picture Frame Buffer Stride and Control</td>
<td>RW</td>
</tr>
<tr>
<td>3C7-3C4</td>
<td>HQV Sub-picture Frame Buffer Starting Address</td>
<td>RW</td>
</tr>
<tr>
<td>3CB-3C8</td>
<td>HQV Sub-picture 4 x 16 RAM Table Write Control</td>
<td>RW</td>
</tr>
<tr>
<td>3CF-3CC</td>
<td>HQV Background Offset</td>
<td>RW</td>
</tr>
<tr>
<td>3D3-3D0</td>
<td>HQV Stream Control and Status</td>
<td>RW</td>
</tr>
<tr>
<td>3D7-3D4</td>
<td>HQV SW Source Buffer – Luma or Packed Starting Address</td>
<td>RW</td>
</tr>
<tr>
<td>3DB-3D8</td>
<td>HQV SW Source Buffer – Chroma Starting Address</td>
<td>RW</td>
</tr>
<tr>
<td>3DF-3DC</td>
<td>HQV Linear/Tile Address Mode, Color Space Conversion, Gamma and De-blocking Control</td>
<td>RW</td>
</tr>
<tr>
<td>3E3-3E0</td>
<td>HQV Sub-picture Horizontal Scale Control</td>
<td>RW</td>
</tr>
<tr>
<td>3E7-3E4</td>
<td>HQV Motion Adaptive De-interlace Control &amp; Threshold</td>
<td>RW</td>
</tr>
<tr>
<td>3EB-3E8</td>
<td>HQV Sub-picture Vertical Scale Control</td>
<td>RW</td>
</tr>
<tr>
<td>3EF-3EC</td>
<td>HQV Destination Frame Buffer Starting Address 0</td>
<td>RW</td>
</tr>
<tr>
<td>3F3-3F0</td>
<td>HQV Destination Frame Buffer Starting Address 1</td>
<td>RW</td>
</tr>
<tr>
<td>3F7-3F4</td>
<td>HQV Destination Frame Buffer Stride</td>
<td>RW</td>
</tr>
<tr>
<td>3FB-3F8</td>
<td>HQV Source Frame Buffer Stride</td>
<td>RW</td>
</tr>
<tr>
<td>3FF-3FC</td>
<td>HQV Destination Frame Buffer Starting Address 2</td>
<td>RW</td>
</tr>
</tbody>
</table>
### HQV Registers

<table>
<thead>
<tr>
<th>Offset (Hex)</th>
<th>Register Name</th>
<th>Attribute</th>
</tr>
</thead>
<tbody>
<tr>
<td>1363-1360</td>
<td>HQV Color Adjustment Control 1</td>
<td>RW</td>
</tr>
<tr>
<td>1367-1364</td>
<td>HQV Color Adjustment Control 2</td>
<td>RW</td>
</tr>
<tr>
<td>136B-1368</td>
<td>HQV Color Adjustment Control 3</td>
<td>RW</td>
</tr>
<tr>
<td>136F-136C</td>
<td>HQV Color Adjustment Control 4</td>
<td>RW</td>
</tr>
<tr>
<td>1373-1370</td>
<td>HQV Video Start Point Offset Control in Source</td>
<td>RW</td>
</tr>
<tr>
<td>1377-1374</td>
<td>HQV Sub-picture Start Point Offset Control in Source</td>
<td>RW</td>
</tr>
<tr>
<td>137B-1378</td>
<td>HQV Video End Point Offset Control in Source</td>
<td>RW</td>
</tr>
<tr>
<td>137F-137C</td>
<td>HQV Sub-picture End Point Offset Control in Source</td>
<td>RW</td>
</tr>
<tr>
<td>1383-1380</td>
<td>HQV Video Start Point Offset Control in Destination</td>
<td>RW</td>
</tr>
<tr>
<td>1387-1384</td>
<td>HQV Sub-picture Start Point Offset Control in Destination</td>
<td>RW</td>
</tr>
<tr>
<td>138B-1388</td>
<td>HQV Video End Point Offset Control in Destination</td>
<td>RW</td>
</tr>
<tr>
<td>138F-138C</td>
<td>HQV Sub-picture End Point Offset Control in Destination</td>
<td>RW</td>
</tr>
<tr>
<td>1393-1390</td>
<td>HQV Parameters of Hardware Tuning Performance/Quality</td>
<td>RW</td>
</tr>
<tr>
<td>1397-1394</td>
<td>HQV Extended Control</td>
<td>RW</td>
</tr>
<tr>
<td>139B-1398</td>
<td>HQV Static Record Frame Buffer Starting Address</td>
<td>RW</td>
</tr>
<tr>
<td>139F-139C</td>
<td>HQV Static Record Frame Buffer Stride</td>
<td>RW</td>
</tr>
<tr>
<td>13A3-13A0</td>
<td>HQV Color Adjustment Control 5</td>
<td>RW</td>
</tr>
<tr>
<td>13A7-13A4</td>
<td>HQV Color Adjustment Control 6</td>
<td>RW</td>
</tr>
<tr>
<td>13AB-13A8</td>
<td>HQV Color Adjustment Control 7</td>
<td>RW</td>
</tr>
<tr>
<td>13AF-13AC</td>
<td>HQV Color Adjustment Control 8</td>
<td>RW</td>
</tr>
<tr>
<td>13B3-13B0</td>
<td>HQV Video Horizontal Scale Control</td>
<td>RW</td>
</tr>
<tr>
<td>13B7-13B4</td>
<td>HQV Video Vertical Scale Control</td>
<td>RW</td>
</tr>
<tr>
<td>13BB-13B8</td>
<td>HQV Background Color</td>
<td>RW</td>
</tr>
<tr>
<td>13BF-13BC</td>
<td>HQV Segment Residue Pixel Frame Buffer Starting Address</td>
<td>RW</td>
</tr>
<tr>
<td>13C3-13C0</td>
<td>HQV Sub-picture Frame Buffer Stride and Control</td>
<td>RW</td>
</tr>
<tr>
<td>13C7-13C4</td>
<td>HQV Sub-picture Frame Buffer Starting Address</td>
<td>RW</td>
</tr>
<tr>
<td>13CB-13C8</td>
<td>HQV Sub-picture 4 x 16 RAM Table Write Control</td>
<td>RW</td>
</tr>
<tr>
<td>13CF-13CC</td>
<td>HQV Background Offset</td>
<td>RW</td>
</tr>
<tr>
<td>13D3-13D0</td>
<td>HQV Stream Control and Status</td>
<td>RW</td>
</tr>
<tr>
<td>13D7-13D4</td>
<td>HQV SW Source Buffer – Luma or Packed Starting Address</td>
<td>RW</td>
</tr>
<tr>
<td>13DB-13D8</td>
<td>HQV SW Source Buffer – Chroma Starting Address</td>
<td>RW</td>
</tr>
<tr>
<td>13DF-13DC</td>
<td>HQV Linear/Tile Address Mode, Color Space Conversion, Gamma and De-blocking Control</td>
<td>RW</td>
</tr>
<tr>
<td>13E3-13E0</td>
<td>HQV Sub-picture Horizontal Scale Control</td>
<td>RW</td>
</tr>
<tr>
<td>13E7-13E4</td>
<td>HQV Motion Adaptive De-interlace Control &amp; Threshold</td>
<td>RW</td>
</tr>
<tr>
<td>13EB-13E8</td>
<td>HQV Sub-picture Vertical Scale Control</td>
<td>RW</td>
</tr>
<tr>
<td>13EF-13EC</td>
<td>HQV Destination Frame Buffer Starting Address 0</td>
<td>RW</td>
</tr>
<tr>
<td>13F3-13F0</td>
<td>HQV Destination Frame Buffer Starting Address 1</td>
<td>RW</td>
</tr>
<tr>
<td>13F7-13F4</td>
<td>HQV Destination Frame Buffer Stride</td>
<td>RW</td>
</tr>
<tr>
<td>13FB-13F8</td>
<td>HQV Source Frame Buffer Stride</td>
<td>RW</td>
</tr>
<tr>
<td>13FF-13FC</td>
<td>HQV Destination Frame Buffer Starting Address 2</td>
<td>RW</td>
</tr>
</tbody>
</table>

**Note:**

1) Port Address: MB1 + Offset Address

MB1 is declared in the register with offset address 17h-14h in the PCI configuration space.

2) There is an additional register space to match the above register definition. When write a register to this space, it will be sent to "command regulator" first and then pass to video display engine. However, register read will be the same as the original action. The relationship between the additional register space and original register space is:

\[
\text{The additional register address} = \text{(The original register address)} + 16\times2000
\]

Preliminary Revision 1.0, July 29, 2009
## HQV Engine Register Descriptions (360-3FFh)

### Offset Address: 363-360h
#### HQV Color Adjustment Control 1

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:28</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>27:17</td>
<td>RW</td>
<td>0</td>
<td>Coefficient D1(s[26:18],[17])</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(2P)</td>
</tr>
<tr>
<td>16:0</td>
<td>RW</td>
<td>0</td>
<td>Coefficient C1(s[15:8],[7:0])</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(2P)</td>
</tr>
</tbody>
</table>

### Offset Address: 367-364h
#### HQV Color Adjustment Control 2

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:28</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>27:17</td>
<td>RW</td>
<td>0</td>
<td>Coefficient D2(s[26:18],[17])</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(2P)</td>
</tr>
<tr>
<td>16:0</td>
<td>RW</td>
<td>0</td>
<td>Coefficient C2(s[15:8],[7:0])</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(2P)</td>
</tr>
</tbody>
</table>

### Offset Address: 36B-368h
#### HQV Color Adjustment Control 3

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:28</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>27:17</td>
<td>RW</td>
<td>0</td>
<td>Coefficient D3(s[26:18],[17])</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(2P)</td>
</tr>
<tr>
<td>16:0</td>
<td>RW</td>
<td>0</td>
<td>Coefficient C3(s[15:8],[7:0])</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(2P)</td>
</tr>
</tbody>
</table>

### Offset Address: 36F-36Ch
#### HQV Color Adjustment Control 4

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:17</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>16:0</td>
<td>RW</td>
<td>0</td>
<td>Coefficient B1(s[15:8],[7:0])</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(2P)</td>
</tr>
</tbody>
</table>

### Offset Address: 373-370h
#### HQV Video Start Point Offset Control in Source

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:27</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>26:16</td>
<td>RW</td>
<td>0</td>
<td>Horizontal Offset of Start Point for Video Location in Source Picture</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Unit: Pixel (2P)</td>
</tr>
<tr>
<td>15:11</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>10:0</td>
<td>RW</td>
<td>0</td>
<td>Vertical Offset of Start Point for Video Location in Source Picture</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Unit: Pixel (2P)</td>
</tr>
</tbody>
</table>

### Offset Address: 377-374h
#### HQV Sub-picture Start Point Offset Control in Source

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:27</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>26:16</td>
<td>RW</td>
<td>0</td>
<td>Horizontal Offset of Start Point for Sub-picture Location in Source Picture</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Unit: Pixel (2P)</td>
</tr>
<tr>
<td>15:11</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>10:0</td>
<td>RW</td>
<td>0</td>
<td>Vertical Offset of Start Point for Sub-picture Location in Source Picture</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Unit: Pixel (2P)</td>
</tr>
</tbody>
</table>
### Offset Address: 37B-378h
**HQV Video End Point Offset Control in Source**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:27</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>26:16</td>
<td>RW</td>
<td>0</td>
<td>Horizontal Offset of End Point for Video Location in Source Picture</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Unit: Pixel (2P)</td>
</tr>
<tr>
<td>15:11</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>10:0</td>
<td>RW</td>
<td>0</td>
<td>Vertical Offset of End Point for Video Location in Source Picture</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Unit: Pixel (2P)</td>
</tr>
</tbody>
</table>

### Offset Address: 37F-37Ch
**HQV Sub-picture End Point Offset Control in Source**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:27</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>26:16</td>
<td>RW</td>
<td>0</td>
<td>Horizontal Offset of End Point for Sub-picture Location in Source Picture</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Unit: Pixel (2P)</td>
</tr>
<tr>
<td>15:11</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>10:0</td>
<td>RW</td>
<td>0</td>
<td>Vertical Offset of End Point for Sub-picture Location in Source Picture</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Unit: Pixel (2P)</td>
</tr>
</tbody>
</table>

### Offset Address: 383-380h
**HQV Video Start Point Offset Control in Destination**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:27</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>26:16</td>
<td>RW</td>
<td>0</td>
<td>Horizontal Offset of Start Point for Video Location in Destination Picture</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Unit: Pixel (2P)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Either video or sub-picture destination data horizontal offset of start point should be set to zero.</td>
</tr>
<tr>
<td>15:11</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>10:0</td>
<td>RW</td>
<td>0</td>
<td>Vertical Offset of Start Point for Video Location in Destination Picture</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Unit: Line (2P)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Either video or sub-picture destination data vertical offset of start point should be set to zero.</td>
</tr>
</tbody>
</table>

### Offset Address: 387-384h
**HQV Sub-picture Start Point Offset Control in Destination**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:27</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>26:16</td>
<td>RW</td>
<td>0</td>
<td>Horizontal Offset of Start Point for Sub-picture Location in Destination Picture</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Unit: Pixel (2P)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Either video or sub-picture destination data horizontal offset of start point should be set to zero.</td>
</tr>
<tr>
<td>15:11</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>10:0</td>
<td>RW</td>
<td>0</td>
<td>Vertical Offset of Start Point for Sub-picture Location in Destination Picture</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Unit: Line (2P)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Either video or sub-picture destination data vertical offset of start point should be set to zero.</td>
</tr>
</tbody>
</table>

### Offset Address: 38B-388h
**HQV Video End Point Offset Control in Destination**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:27</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>26:16</td>
<td>RW</td>
<td>0</td>
<td>Horizontal Offset of End Point for Video Location in Destination Picture</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Unit: Pixel (2P)</td>
</tr>
<tr>
<td>15:11</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>10:0</td>
<td>RW</td>
<td>0</td>
<td>Vertical Offset of End Point for Video Location in Destination Picture</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Unit: Line (2P)</td>
</tr>
</tbody>
</table>
### HQV Sub-picture End Point Offset Control in Destination

**Offset Address:** 38F-38Ch  
**Default Value:** 0000 0000h

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:27</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 26:16 | RW | 0 | Horizontal Offset of End Point for Sub-picture Location In Destination Picture  
Unit: Byte (2P) |
| 15:11 | RO | 0 | Reserved |
| 10:0 | RW | 0 | Vertical Offset of End Point for Sub-picture Location In Destination Picture  
Unit: Line (2P) |

### HQV Parameters of Hardware Tuning Performance / Quality

**Offset Address:** 393-390h  
**Default Value:** 4664 8688h

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 30:28 | RW | 100b | Threshold of Inter-Field Complexity for Pull Down Detection (x4)  
Calculate the difference between current & previous field. |
| 27 | RO | 0 | Reserved |
| 26:25 | RW | 11b | Factor of Calculating Threshold of Intra-Field Complexity  
00: Threshold = 390[30:28]*4 + 390[30:28]*1  
| 24:23 | RO | 0 | Reserved |
| 22:21 | RW | 11b | Static Judgment Number (SJN)  
As static record number is equal to SJN, then static flag is asserted |
| 20 | RW | 0 | The Field Number for The Increment of Static Record  
0: 1 field / (static record)  
1: 2 fields / (static record) |
| 19:18 | RW | 01b | Pull-down Factor 1  
Apply this factor while pull-down not yet detected.  
00: 2/8  
01: 3/8  
10: 4/8  
11: 5/8 |
| 17:16 | RW | 00b | Pull-down Factor 2  
Apply this factor while pull-down detected  
00: 3/8  
01: 4/8  
10: 5/8  
11: 6/8 |
| 15:14 | RW | 10b | Threshold for Pull Down Detection  
(R390[15:14]*R3DC[10:0]) as the minimum threshold for valid pull-down detection |
| 13:12 | RO | 0 | Reserved |
| 11:8 | RW | 6h | Threshold for Motion Detection (x2)  
Edge Detection Threshold- for Degree 90 (x2) |
| 7:4 | RW | 8h | Maximum Difference between Block Boundary (x4)  
Apply de-blocking with sin(x) function while the difference between block boundary is greater than this setting. |
| 3:0 | RW | 8h | |
### HQV Registers

#### HQV Extended Control

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:11</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>10:8</td>
<td>RW</td>
<td>0</td>
<td>Constriction Enable&lt;br&gt;000: Constriction disable&lt;br&gt;001–111: Rounding LSB1–LSB7</td>
</tr>
<tr>
<td>7</td>
<td>RW</td>
<td>0</td>
<td>Color Adjustment Enable&lt;br&gt;0: Disable&lt;br&gt;1: Enable</td>
</tr>
<tr>
<td>6</td>
<td>RW</td>
<td>0</td>
<td>Bob de-interlacing method&lt;br&gt;0: Line average&lt;br&gt;1: Line duplication (for TV output)</td>
</tr>
<tr>
<td>5</td>
<td>RW</td>
<td>0</td>
<td>YUV Output Format Control (2P)&lt;br&gt;0: YUV422 out&lt;br&gt;1: YUV444 out&lt;br&gt;This bit is effective when (H or V scaling size) &lt; (1/2 H or V original) size. For the other cases, it just uses YUV422 out.</td>
</tr>
<tr>
<td>4</td>
<td>RW</td>
<td>0</td>
<td>Color Space Conversion Method&lt;br&gt;0: BT601&lt;br&gt;1: BT709</td>
</tr>
<tr>
<td>3</td>
<td>RW</td>
<td>0</td>
<td>Color Format Convert Method (from YUV420 → YUV422)&lt;br&gt;0: 4-tap interpolation&lt;br&gt;1: Method 1 (−1 9 9 −1).</td>
</tr>
<tr>
<td>2:1</td>
<td>RW</td>
<td>00b</td>
<td>Color Format Convert Method (from YUV422 → YUV444)&lt;br&gt;00: Method 1 (WMV9 and H.264)&lt;br&gt;01: Reserved&lt;br&gt;1x: Method 3 (−1 9 9 −1).</td>
</tr>
<tr>
<td>0</td>
<td>RW</td>
<td>0</td>
<td>Color Format Convert Method (from YUV444 → YUV422)&lt;br&gt;0: Method 1 (1 1)&lt;br&gt;1: Method 2 (Drop)&lt;br&gt;This bit is effective as (no scaling) or (scaling size) &gt; (1/2 original size). For the other cases, it just uses method 2.</td>
</tr>
</tbody>
</table>

#### HQV Static Record Frame Buffer Starting Address

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:29</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>28:4</td>
<td>RW</td>
<td>0</td>
<td>Static Record Frame Buffer Starting Address&lt;br&gt;Unit: 16 bytes</td>
</tr>
<tr>
<td>3:2</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>1:0</td>
<td>RW</td>
<td>0</td>
<td>Memory Location</td>
</tr>
</tbody>
</table>

#### HQV Static Record Frame Buffer Stride

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>14:10</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>9:4</td>
<td>RW</td>
<td>0</td>
<td>Static Record Frame Buffer Stride&lt;br&gt;Unit: 16 bytes</td>
</tr>
<tr>
<td>3:0</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

#### HQV Color Adjustment Control 5

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:17</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>16:0</td>
<td>RW</td>
<td>0</td>
<td>Coefficient B3s[15:8] [7:0] (2P)&lt;br&gt;Note: Ŷ'(R') = A1<em>Ŷ(R) + B1</em>Cb(G) + C1*Cr(B) + D1</td>
</tr>
</tbody>
</table>

---

Preliminary Revision 1.0, July 29, 2009

47  HQV Registers
### Offset Address: 3A7-3A4h
**HQV Color Adjustment Control 6**
Default Value: 0000 0000h

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:17</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>16:0</td>
<td>RW</td>
<td>0</td>
<td>Coefficient A1(s[15:8],[7:0]) (2P)</td>
</tr>
</tbody>
</table>

Note: \( Cb'(G') = A2*Y(R) + B2*Cb(G) + C2*Cr(B) + D2 \)

### Offset Address: 3AB-3A8h
**HQV Color Adjustment Control 7**
Default Value: 0000 0000h

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:17</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>16:0</td>
<td>RW</td>
<td>0</td>
<td>Coefficient A2(s[15:8],[7:0]) (2P)</td>
</tr>
</tbody>
</table>

Note: \( Cr'(B') = A3*Y(R) + B3*Cb(G) + C3*Cr(B) + D3 \)

### Offset Address: 3AF-3ACh
**HQV Color Adjustment Control 8**
Default Value: 0000 0000h

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:17</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>16:0</td>
<td>RW</td>
<td>0</td>
<td>Coefficient A3(s[15:8],[7:0]) (2P)</td>
</tr>
</tbody>
</table>

### Offset Address: 3B3-3B0h
**HQV Video Horizontal Scale Control**
Default Value: 0000 0000h

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RW</td>
<td>0</td>
<td>Horizontal Scale Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable (2P)</td>
</tr>
<tr>
<td>30</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>29:28</td>
<td>RW</td>
<td>00b</td>
<td>Horizontal Scale Function (2P)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: Scale up.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: 1~1/4</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: 1/4~1/8</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: &lt;1/8</td>
</tr>
<tr>
<td>27:15</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>14:0</td>
<td>RW</td>
<td>0</td>
<td>Horizontal Scale Factor [14:12],[11:0] (2P)</td>
</tr>
</tbody>
</table>

Note: Scale factor:
1. Scale up: source/destination
2. 1~1/4: source/(destination+0.5)
3. 1/4~1/8: source/destination
4. <1/8: destination/source

### Offset Address: 3B7-3B4h
**HQV Video Vertical Scale Control**
Default Value: 0000 0000h

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RW</td>
<td>0</td>
<td>Vertical Scale Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable (2P)</td>
</tr>
<tr>
<td>30:29</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>28</td>
<td>RW</td>
<td>0</td>
<td>Vertical Scale Function (2P)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Scale up.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Scale down</td>
</tr>
<tr>
<td>27:17</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>16:0</td>
<td>RW</td>
<td>0</td>
<td>Vertical Scale Factor [16:12],[11:0] (2P)</td>
</tr>
</tbody>
</table>

Note: Scale factor:
1. Scale up: source/destination;
2. Scale down: source/(destination+0.5)

PS:
For all scaling calculation, the final results should be rounded to the nearest integer.
For bi-linear factor, please use 6 binary fraction of factor (need be rounded to the nearest 6th fraction) to do the calculation.
### HQV Background Color

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:30</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>29:20</td>
<td>RW</td>
<td>0</td>
<td>Luma(Y) or Red Color Value</td>
</tr>
<tr>
<td>19:10</td>
<td>RW</td>
<td>0</td>
<td>Chroma(Cb) or Green Color Value</td>
</tr>
<tr>
<td>9:0</td>
<td>RW</td>
<td>0</td>
<td>Chroma(Cr) or Blue Color Value</td>
</tr>
</tbody>
</table>

**Default Value:** 0000 0000h

### HQV Segment Residue Pixel Frame Buffer Starting Address

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RO</td>
<td>0</td>
<td>HQV Output Field</td>
</tr>
<tr>
<td>30</td>
<td>RO</td>
<td>0</td>
<td>HQV Current Process Field</td>
</tr>
<tr>
<td>29</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>28:4</td>
<td>RW</td>
<td>0</td>
<td>Segment Residue Pixel Frame Buffer Starting Address</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Unit : 16 bytes</td>
</tr>
<tr>
<td>3:2</td>
<td>RO</td>
<td>0</td>
<td>HQV Current Process Destination Buffer ID</td>
</tr>
<tr>
<td>1:0</td>
<td>RW</td>
<td>0</td>
<td>Memory Location</td>
</tr>
</tbody>
</table>

**Default Value:** 0000 0000h

### HQV Sub-picture Frame Buffer Stride and Control

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:24</td>
<td>RW</td>
<td>0</td>
<td>MC Flipping Count</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><em>For MC flip to HQV path:</em> Read only</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><em>For SW flip path:</em> R/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>HQV update read out register data at the beginning of HQV processing a frame.</td>
</tr>
<tr>
<td>23:21</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>20</td>
<td>RW</td>
<td>0</td>
<td>Sub-picture Blending Option</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Blending before scaling</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Scaling before blending</td>
</tr>
<tr>
<td>19</td>
<td>RW</td>
<td>0</td>
<td>Sub-picture Format</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: AI44 or IA44</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: AYUV (MSB A(8)-Y(8)-U(8)-V(8) LSB)</td>
</tr>
<tr>
<td>18</td>
<td>RW</td>
<td>0</td>
<td>Inverse Alpha Value in AI44 Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Inverse (One’s Complement)</td>
</tr>
<tr>
<td>17</td>
<td>RW</td>
<td>0</td>
<td>Alpha, Index Exchange in AI44 Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: AI44</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: IA44</td>
</tr>
<tr>
<td>16</td>
<td>RW</td>
<td>0</td>
<td>HQV Sub-picture Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Only active at HQV source format is YUV.</td>
</tr>
<tr>
<td>15:14</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>13:4</td>
<td>RW</td>
<td>0</td>
<td>Subpicture Frame Buffer Stride</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Unit: 16 bytes</td>
</tr>
<tr>
<td>3:0</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

**Default Value:** 0000 0000h

### HQV Sub-picture Frame Buffer Starting Address

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:29</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>28:4</td>
<td>RW</td>
<td>0</td>
<td>Sub-picture Frame Buffer Starting Address (Unit: 16 bytes)</td>
</tr>
<tr>
<td>3:2</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>1:0</td>
<td>RW</td>
<td>0</td>
<td>Memory Location</td>
</tr>
</tbody>
</table>

**Default Value:** 0000 0000h
### Offset Address: 3CB-3C8h
#### HQV Sub-picture 4x16 RAM Table Write Control

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>RW</td>
<td>0</td>
<td>RAM Table Write Data</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>V: Bits[31:24]</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>U: Bits[23:16]</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Y: Bits[15:8]</td>
</tr>
<tr>
<td>7:4</td>
<td>RW</td>
<td>0</td>
<td>RAM Table Read / Write Address</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Indicate which entry of palette table will be written or read. Palette table contains 16 entries of palette data. (HQV3C8[7:4] = 0x0000 ~ HQV3C8[7:4] = 0x1111)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Need to program HQV3C8[31:8] and HQV3C8[7:4] 16 times to fill the subpicture palette table.</td>
</tr>
<tr>
<td>3</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>2</td>
<td>RW</td>
<td>0</td>
<td>V Write Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td>1</td>
<td>RW</td>
<td>0</td>
<td>U Write Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td>0</td>
<td>RW</td>
<td>0</td>
<td>Y Write Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable</td>
</tr>
</tbody>
</table>

### Offset Address: 3CF-3CCh
#### HQV Background Offset

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:27</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>26:16</td>
<td>RW</td>
<td>0</td>
<td>Background Horizontal Offset (-1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(Unit: Pixel)</td>
</tr>
<tr>
<td>15:11</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>10:0</td>
<td>RW</td>
<td>0</td>
<td>Background Vertical Offset (-1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(Unit: Pixel)</td>
</tr>
</tbody>
</table>

### Offset Address: 3D3-3D0h
#### HQV Stream Control and Status

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:28</td>
<td>RW</td>
<td>0</td>
<td>Video Data Stream Format [3:0]</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0000: RGB32 – (X8R8G8B8)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0001: RGB32 – (X2R10G10B10)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0010: RGB16 – (R5G6B5)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0011: RGB15 – (X1R5G5B5)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0100: YUV444 – (X8Y8U8V8)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0101: V410 – (V10Y10U10X2)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1000: YUV422 – (V8Y8U8Y8)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1001: UYVV – (Y8V8Y8U8)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1100: YUV420 – (NV12; planar mode)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1101: YUV411 – (NV11; planar mode : Y8Y8Y8Y8Y8V8U8)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1110: P208 – (YUV422 planar mode)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Others: Reserved</td>
</tr>
<tr>
<td>27</td>
<td>RW</td>
<td>0</td>
<td>High Quality Video Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td>26</td>
<td>RW</td>
<td>0</td>
<td>Buffer Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Double destination buffers</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Triple destination buffers</td>
</tr>
<tr>
<td>25:24</td>
<td>RW</td>
<td>00b</td>
<td>Video Stream Source [1:0]</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: SW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: Capture 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: Capture 1</td>
</tr>
<tr>
<td>23</td>
<td>RW</td>
<td>0</td>
<td>Advanced De-interlace Mode Enable (reference more than one field)</td>
</tr>
<tr>
<td>22</td>
<td>RW</td>
<td>0</td>
<td>Vertical Low Pass Filter Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td>21</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>Bit</td>
<td>Attribute</td>
<td>Default</td>
<td>Description</td>
</tr>
<tr>
<td>-----</td>
<td>-----------</td>
<td>---------</td>
<td>-------------</td>
</tr>
</tbody>
</table>
| 20  | RW        | 0       | Planar Mode Chrominance Source Data Format  
|     |           |         | 0: Source Chrominance is saved by frame picture  
|     |           |         | 1: Source Chrominance is saved by field picture  |
| 19  | RW        | 0       | Inverse Input Field  
|     |           |         | 0: Non-inversed  
|     |           |         | 1: Inversed  |
| 18  | RW        | 0       | Frame To Field  
|     |           |         | 0: No action  
|     |           |         | 1: Frame base source, extract a field from a frame  |
| 17  | RW        | 0       | Field To Frame  
|     |           |         | 0: No action  
|     |           |         | 1: Field source, de-interlace to progressive frame  |
| 16  | RO        | 0       | Reserved  |
| 15  | RW        | 0       | Sub-Picture Flip  
|     |           |         | Software writes 1 to this bit indicates a new sub-picture need to blend.  
|     |           |         | After blending completes, hardware clears it to 0. Software can read this bit to check the status if hardware completes blending.  |
| 14:13 | RO   | 0       | Reserved  |
| 12  | RO        | 0       | HQV Flip FIFO Full Status  
|     |           |         | The FIFO depth defined in Rx3F8 [17:16]  |
| 11  | RO        | 0       | Reserved  |
| 10:8| RO        | 0       | State Machine Status of HQV Flip Module  |
| 7   | RW        | 0       | HQV Interrupt Enable  
|     |           |         | 0: Disable HQV interrupt.  
|     |           |         | 1: HQV send interrupt signal after done a frame  
|     |           |         | Relative setting: Rx3D0[0]  |
| 6   | RW        | 0       | Single Destination Buffer  
|     |           |         | 0: Not used  
|     |           |         | 1: Single buffer used  
|     |           |         | Rx3D0[26] would be ignored.  |
| 5   | RW        | 0       | Field of Software Source Input  
|     |           |         | 0: Top  
|     |           |         | 1: Bottom  |
| 4   | RW        | 0       | Software Source Flip  
|     |           |         | Software writes 1 to flip a image to HQV. (Rx3D0[25:24] should be 00h)  
|     |           |         | After processing completes, hardware clears it to 0. Software reads this bit to check flip status.  |
| 3   | RO        | 0       | HQV Engine Idle State  
|     |           |         | 0: Busy  
|     |           |         | 1: Idle  |
| 2:1 | RO        | 0       | HQV Output Buffer ID  
|     |           |         | HQV destination buffer ID  |
| 0   | RW1C      | 0       | HQV End of Frame Status  
|     |           |         | 0: Frame not ready  
|     |           |         | 1: HQV has been output an image. (Software writes 1 to clear this bit)  
|     |           |         | After HQV done an image, this bit will be pulled high, and it will be pulled down only when software writes 1b to it  |

**Offset Address: 3D7-3D4h**  
HQV SW Source Buffer – Luma or Packed Starting Address  
Default Value: 0000 0000h

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:29</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>28:4</td>
<td>RW</td>
<td>0</td>
<td>SW Source Buffer Y or Packed Mode Starting Address (Unit: 16 bytes)</td>
</tr>
<tr>
<td>3:2</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>1:0</td>
<td>RW</td>
<td>0</td>
<td>Memory Location</td>
</tr>
</tbody>
</table>

**Offset Address: 3DB-3D8h**  
HQV SW Source Buffer – Chroma Starting Address  
Default Value: 0000 0000h

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:29</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>28:4</td>
<td>RW</td>
<td>0</td>
<td>SW Source Buffer U, V Starting Addresses (Unit: 16 bytes)</td>
</tr>
<tr>
<td>3:2</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>1:0</td>
<td>RW</td>
<td>0</td>
<td>Memory Location</td>
</tr>
</tbody>
</table>
### HQV Linear / Tile Address Mode, Color Space Conversion, Gamma, De-blocking Control

**Default Value:** 0000 0000h

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:30</td>
<td>RW</td>
<td>00b</td>
<td><strong>Linear / Tile Address Mode Control</strong>&lt;br&gt;(Tile address is valid only at source data from MC, 3D0[25:24]=01)&lt;br&gt;00: Linear&lt;br&gt;01: 256 bits x 8 tile mode (Addr = SA + (Y[10:3]<em>PTh</em>8) + {X[7:1],Y[2:0],X[0]}&lt;br&gt;10: 256 bits tile mode (Addr = SA + (Y[10:4]<em>PTh</em>16) + {X[6:1],Y[3:0],X[0]}&lt;br&gt;11: 512 bits tile mode (Addr = SA + (Y[10:4]<em>PTh</em>16) + {X[6:2], Y[3:0],X[1:0]})&lt;br&gt;Where unit of X is 128-bit; unit of Y is line.</td>
</tr>
<tr>
<td>29</td>
<td>RW</td>
<td>0</td>
<td><strong>HQV Output Data Pack In 32-bits Mode.</strong>&lt;br&gt;0: 16 bits (RGB565)&lt;br&gt;1: 32 bits (RGB888)&lt;br&gt;Only valid when the source is YUV and color space conversion is enabled.</td>
</tr>
<tr>
<td>28</td>
<td>RW</td>
<td>0</td>
<td><strong>Color Space Conversion Enable</strong>&lt;br&gt;0: Disable&lt;br&gt;1: Enable</td>
</tr>
<tr>
<td>27</td>
<td>RW</td>
<td>0</td>
<td><strong>De-blocking Enable</strong></td>
</tr>
<tr>
<td>26-25</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>24:20</td>
<td>RW</td>
<td>0</td>
<td><strong>HQV Output FIFO Threshold for Write Request Control</strong> (Unit: level)&lt;br&gt;HQV output FIFO has 64 levels, once the data in output FIFO touch the threshold (32+3DC.[24:20]), the write request would be triggered.</td>
</tr>
<tr>
<td>19:16</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>15</td>
<td>RW</td>
<td>0</td>
<td><strong>Constant Alpha of RGB32 Format</strong>&lt;br&gt;0: Alpha = 00&lt;br&gt;1: Alpha = FF</td>
</tr>
<tr>
<td>14</td>
<td>RW</td>
<td>0</td>
<td><strong>Enable Synchronization Flipping Field with Interlaced IGA</strong>&lt;br&gt;0: Disable&lt;br&gt;1: Enable</td>
</tr>
<tr>
<td>13</td>
<td>RW</td>
<td>0</td>
<td><strong>IGA Field Inverse</strong>&lt;br&gt;0: Not inversed&lt;br&gt;1: Inverse</td>
</tr>
<tr>
<td>12:11</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>10:0</td>
<td>RW</td>
<td>0</td>
<td><strong>Image Size / 1024</strong>&lt;br&gt;Used for pull-down detection.</td>
</tr>
</tbody>
</table>

---

### HQV Sub-picture Horizontal Scale Control

**Default Value:** 0000 0000h

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RW</td>
<td>0</td>
<td><strong>Horizontal Scale Enable</strong>&lt;br&gt;0: Disable&lt;br&gt;1: Enable</td>
</tr>
<tr>
<td>30</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>29:28</td>
<td>RW</td>
<td>0</td>
<td><strong>Horizontal Scale Function; (2P)</strong>&lt;br&gt;00: Scale up&lt;br&gt;01: 1–1/4&lt;br&gt;10: 1/4–1/8&lt;br&gt;11: &lt;1/8</td>
</tr>
<tr>
<td>27:15</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 14:0  | RW        | 0        | **Horizontal Scale Factor [14:12],[11] (2P)**<br>Scale up : source/destination<br>1–1/4 : source(destination + 0.5)<br>1/4–1/8 : source/destination<br><1/8 : destination/source
### HQV Registers

#### Offset Address: 3E7-3E4h

**HQV Motion Adaptive De-interlace Control & Threshold**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RW</td>
<td>0</td>
<td>2:2 Pull Down Sequence Detection Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Relative setting: Rx3DC[10:0]</td>
</tr>
<tr>
<td>30:28</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>27</td>
<td>RW</td>
<td>0</td>
<td>3:2 Pull Down Sequence Detection Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Relative setting: Rx3DC[10:0]</td>
</tr>
<tr>
<td>26:25</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>24</td>
<td>RW</td>
<td>0</td>
<td>2:3:3:2 Pull Down Sequence Detection Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Relative setting: Rx3DC[10:0]</td>
</tr>
<tr>
<td>23:13</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>12:8</td>
<td>RW</td>
<td>0</td>
<td>Motion Detection Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td>7</td>
<td>RO</td>
<td>0</td>
<td>2:2 Pull Down Detection Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Not detected</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Detected</td>
</tr>
<tr>
<td>6</td>
<td>RO</td>
<td>0</td>
<td>3:2 Pull Down Detection Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Not detected</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Detected</td>
</tr>
<tr>
<td>5</td>
<td>RO</td>
<td>0</td>
<td>2:3:3:2 Pull Down Detection Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Not detected</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Detected</td>
</tr>
<tr>
<td>4:1</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>1</td>
<td>RW</td>
<td>0</td>
<td>Edge Detection Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable</td>
</tr>
</tbody>
</table>

#### Offset Address: 3EB-3E8h

**HQV Sub-picture Vertical Scale Control**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RW</td>
<td>0</td>
<td>Vertical Scale Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td>30:29</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>28</td>
<td>RW</td>
<td>0</td>
<td>Vertical Scale Function; (2P)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Scale up</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Scale down</td>
</tr>
<tr>
<td>27:17</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>16:0</td>
<td>RW</td>
<td>0</td>
<td>Vertical Scale Factor [14:12],[11] (2P)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Scale up : source/destination</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Scale down : source/(destination + 0.5)</td>
</tr>
</tbody>
</table>

#### Offset Address: 3EF-3ECh

**HQV Destination Frame Buffer Starting Address 0**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RW</td>
<td>0</td>
<td>HQV Output Data Pack In 32 Bits xRGB2-10-10-10 Format After HQV’s Color Space Conversion</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Note: Only one of [Rx3EC[31], Rx3DC[29]] can be set to 1.</td>
</tr>
<tr>
<td>30</td>
<td>RW</td>
<td>0</td>
<td>Enable Output In Tile Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Addr = ST_ADDR[28:4] + Y[10:3]*{PITCH[10:0], 3'b0} + {X[10:1], Y[2:0], X[0]}</td>
</tr>
<tr>
<td>29</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>28:4</td>
<td>RW</td>
<td>0</td>
<td>Destination Frame Buffer Starting Address 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Unit: 16 bytes</td>
</tr>
<tr>
<td>3:2</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>1:0</td>
<td>RW</td>
<td>0</td>
<td>Memory Location</td>
</tr>
</tbody>
</table>
### HQV Destination Frame Buffer Starting Address 1

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:29</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>28:4</td>
<td>RW</td>
<td>0</td>
<td>Destination Frame Buffer Starting Address 1 Unit: 16 bytes</td>
</tr>
<tr>
<td>3:2</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>1:0</td>
<td>RW</td>
<td>0</td>
<td>Memory Location</td>
</tr>
</tbody>
</table>

### HQV Destination Frame Buffer Stride

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:14</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>13:4</td>
<td>RW</td>
<td>0</td>
<td>Destination Frame Buffer Stride (2P) Unit: 16 bytes</td>
</tr>
<tr>
<td>3:0</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

### HQV Source Frame Buffer Stride

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RW</td>
<td>0</td>
<td>Load Starting Address Rx3D4[25:4], Rx3D8[25:4] for Advanced De-interlacing 0: Not used. Hardware keeps the starting address. 1: Load starting address to current field</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Note: Command sequence</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Step1: Write Rx3D4, Rx3D8</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Step2: Write Rx3F8; new address to PN</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Step3: Write Rx3D4, Rx3D8</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Step4: Write Rx3F8; PN to PC; new address to PN</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Step5: Write Rx3D4, Rx3D8</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Step6: Write Rx3F8; PC to PP; PN to PC; new address to PN</td>
</tr>
<tr>
<td>30</td>
<td>RW</td>
<td>0</td>
<td>SJN Reset Write 1 to reset static judgment number</td>
</tr>
<tr>
<td>29</td>
<td>RW</td>
<td>0</td>
<td>Pull Down Detection Low-Threshold Value</td>
</tr>
<tr>
<td>28</td>
<td>RW</td>
<td>0</td>
<td>Pull Down Detection Error Sequence Check One Time 0: Disable 1: Enable</td>
</tr>
<tr>
<td>27:26</td>
<td>RW</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>25</td>
<td>RW</td>
<td>0</td>
<td>Not Check Size 0: Check size 1: Not check size</td>
</tr>
<tr>
<td>24:21</td>
<td>RW</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>20</td>
<td>RW</td>
<td>0</td>
<td>Software Flip Queue Enable 0: Pull Rx3D0[4] low at frame done. 1: Pull Rx3D0[4] low at beginning of processing frame</td>
</tr>
<tr>
<td>19</td>
<td>RW</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>18</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>17:16</td>
<td>RW</td>
<td>00b</td>
<td>FIFO Depth of HQV Flip Control Engine For hardware flip only. (Rx3D0[25:24] ! = 00b) Only supports 2 stages FIFO queuing hardware flipping. 00: Pull “FIFO full status Rx3D0[12]” high, while both two stage are queuing. Drop current processing frame while both two stage are queuing. 01: Pull “FIFO full status Rx3D0[12]” high, while one stage is queuing. Drop current processing frame while both two stage are queuing. 10: Pull “FIFO full status Rx3D0[12]” high, while both two stage are queuing. Never drop current processing frame. 11: Pull “FIFO full status Rx3D0[12]” high, while one stage is queuing. Never drop current processing frame.</td>
</tr>
<tr>
<td>15:14</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>13:4</td>
<td>RW</td>
<td>0</td>
<td>Source Frame Buffer Stride (Unit: 16 bytes)</td>
</tr>
<tr>
<td>3:0</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
### HQV Destination Frame Buffer Starting Address 2

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:29</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>28:4</td>
<td>RW</td>
<td>0</td>
<td>Destination Frame Buffer Starting Address 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Unit: 16 bytes</td>
</tr>
<tr>
<td>3:2</td>
<td>RO</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>1:0</td>
<td>RW</td>
<td>0</td>
<td>Memory Location</td>
</tr>
</tbody>
</table>

Note: HQV supports 2 Video Streams; therefore, an additional register space is provided to match the above registers definition. Writing a register to this space, it will write to the second HQV, which output to V3 and source is from the second MC engine.

The relationship between the additional register space and the original register space is

(Additional register address) = (Original register address) + 16'h1000.
COMMAND REGULATOR (CR) REGISTERS

This chapter provides detailed Command Regulator register descriptions.

Memory Mapped I/O Register Address Spaces

The following MMIO space is fed into and processed by CR, and then dispatch to related engine.

<table>
<thead>
<tr>
<th>Memory Range (Note)</th>
<th>Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 ~ 2M-1:</td>
<td></td>
</tr>
<tr>
<td>0x00000000 ~ 0x000001FF</td>
<td>2D Engine Register Space</td>
</tr>
<tr>
<td>0x00000200 ~ 0x000003FF</td>
<td>Video Related Engines Register Space 1 (bypass)</td>
</tr>
<tr>
<td>0x00000400 ~ 0x000007FF</td>
<td>3D Engine Register Space</td>
</tr>
<tr>
<td>0x00000800 ~ 0x00000BFF</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x00000C00 ~ 0x00000DFF</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x00001200 ~ 0x000013FF</td>
<td>Video Related Engines Register Space 2 (bypass)</td>
</tr>
<tr>
<td>0x00002200 ~ 0x000023FF</td>
<td>Extended Video Engines Register Space 1</td>
</tr>
<tr>
<td>0x00002E00 ~ 0x00002FFF</td>
<td>DMA(AGP) Register Space 2</td>
</tr>
<tr>
<td>0x00003200 ~ 0x000033FF</td>
<td>Extended Video Engines Register Space 2</td>
</tr>
</tbody>
</table>

2M ~ 4M-1: 2D Host BitBLT Space

Note: These addresses are offset address from PCI Memory Base 1 (MB1).
### Definition of I/O Registers

The I/O Register Base Address for 3D/CR is 400h. Offsets Rx1Ch to Rx3Bh are used to set CR registers. These registers are allowed to be set through the starting address Rx1Ch or Rx3Ch with the same HParaType 10h and HparaType 11h. Settings through Rx1Ch would not enable the 3D Engine clock, while settings through Rx3Ch would enable the 3D Engine clock.

### For Write Mode

#### Setting of Command Regulator

<table>
<thead>
<tr>
<th>Scope</th>
<th>Offset</th>
<th>Description</th>
<th>Mnemonic</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transmission Setting</td>
<td>1Ch</td>
<td>The Beginning of Internal Address for Parameter Programming</td>
<td>HParaAdr</td>
</tr>
<tr>
<td></td>
<td>1Dh</td>
<td>Offset Setting for Some Special Parameter Types</td>
<td>HParaOS</td>
</tr>
<tr>
<td></td>
<td>1Eh</td>
<td>Parameter Type</td>
<td>HParaType</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>HParaType</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000 0000b ~ 0000 1111b</td>
<td>Reserved</td>
</tr>
<tr>
<td>0001 0000b</td>
<td>Command Decoded in front of Command Regulator</td>
</tr>
<tr>
<td>0001 0001b</td>
<td>Command for Frame Buffer AutoSwapping and CR’s Miscellaneous Setting</td>
</tr>
<tr>
<td>0001 0010b ~ 1111 1111b</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

For more details for the parameters, please refer to Definition of Parameter section.

<table>
<thead>
<tr>
<th>Scope</th>
<th>Offset</th>
<th>Parameter Type Sub-code</th>
<th>Mnemonic</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transmission Space</td>
<td>1Fh</td>
<td>Parameter Type Sub-code</td>
<td>HParaSubType</td>
</tr>
<tr>
<td></td>
<td>23h-20h</td>
<td>Parameter 0</td>
<td>Hpara0</td>
</tr>
<tr>
<td></td>
<td>27h-24h</td>
<td>Parameter 1</td>
<td>Hpara1</td>
</tr>
<tr>
<td></td>
<td>2Bh-28h</td>
<td>Parameter 2</td>
<td>Hpara2</td>
</tr>
<tr>
<td></td>
<td>.......</td>
<td>.......</td>
<td>.......</td>
</tr>
<tr>
<td></td>
<td>3Bh-38h</td>
<td>Parameter 6</td>
<td>Hpara6</td>
</tr>
</tbody>
</table>
Setting of 3D Engine

<table>
<thead>
<tr>
<th>Scope</th>
<th>Offset</th>
<th>Description</th>
<th>Mnemonic</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transmission Setting</td>
<td>3Ch</td>
<td>The Beginning of Internal Address for Parameter Programming</td>
<td>HParaAdr</td>
</tr>
<tr>
<td></td>
<td>3Dh</td>
<td>Offset Setting for Some Special Parameter Types</td>
<td>HParaOS</td>
</tr>
<tr>
<td>Scope</td>
<td>Offset</td>
<td>Parameter Type</td>
<td>Description</td>
</tr>
<tr>
<td>-------</td>
<td>--------</td>
<td>----------------</td>
<td>-------------</td>
</tr>
<tr>
<td>3Eh</td>
<td>0000 0000b</td>
<td>Primitive Vertex Data or Vertex Index</td>
<td></td>
</tr>
<tr>
<td>0000 0001b</td>
<td>Attribute Other Than Texture</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0000 0010b</td>
<td>Attribute of Texture n</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>The setting for texture is divided into 2 kinds of stages: One is defined as Texture Stage with HParaSubType 0nh.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>n is the number stored in HParaSubType (Rx3Fh):</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0000 0000 = Texture 0</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0000 0001 = Texture 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0000 0010 = Texture 2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0000 0011 = Texture 3</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0000 0100 = Texture 4</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0000 0101 = Texture 5</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0000 0110 = Texture 6</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0000 0111 = Texture 7</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0000 1000 = Texture 8</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0000 1001 = Texture 9</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0000 1010 = Texture A</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0000 1011 = Texture B</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0000 1100 = Texture C</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0000 1101 = Texture D</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0000 1110 = Texture E</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0000 1111 = Texture F</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Another type is Texture Sample Stage with HParaSubType 02nh. n is the number stored in HParaSubType (Rx3Fh):</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0010 0000 = Texture sample 0</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0010 0001 = Texture sample 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0010 0010 = Texture sample 2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0010 0011 = Texture sample 3</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0010 0100 = Texture sample 4</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0010 0101 = Texture sample 5</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0010 0110 = Texture sample 6</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0010 0111 = Texture sample 7</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0010 1000 = Texture sample 8</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0010 1001 = Texture sample 9</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0010 1010 = Texture sample A</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0010 1011 = Texture sample B</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0010 1100 = Texture sample C</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0010 1101 = Texture sample D</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0010 1110 = Texture sample E</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0010 1111 = Texture sample F</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1111 1110 = General Texture Setting</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>The use of 1111 1111 is prohibited.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Others = Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0000 0011b</td>
<td>Palette</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>HParaSubType (Rx3Fh) shows the palette type:</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0000 0000 = Texture Palette 0 (Only for AI44 and IA44 Video Texture)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0000 1xxx = Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0001 0000 = Base Address Offset of Each Texture</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0001 0001 = Texture 4X4 Filter Coefficient Table</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0001 0011 = Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0001 0100 = Stipple Palette</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0001 0101 = De-Gamma Table for Reading Texture</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0001 0110 = Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0001 0111 = Gamma-de-Gamma Table for Writing Destination Color</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0010 0000 = Pixel Shader ALU Instruction</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0010 0001 = Pixel Shader TAU Instruction</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0010 0010 = Pixel Shader Constant Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Vertex and Primitive Setting</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0001 0000b</td>
<td>Command Decoded in front of Command Regulator</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0001 0001b</td>
<td>Command for Frame Buffer AutoSwapping and CR’s Miscellaneous Setting</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1111 1101b</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

For details of the parameters, please refer to Definition of Parameter section.
<table>
<thead>
<tr>
<th>Scope</th>
<th>Offset</th>
<th>Description</th>
<th>Mnemonic</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transmission Space</td>
<td>3Fh</td>
<td>Parameter Type Sub-code</td>
<td>HParaSubType</td>
</tr>
<tr>
<td></td>
<td>43h-40h</td>
<td>Parameter 0</td>
<td>Hpara0</td>
</tr>
<tr>
<td></td>
<td>47h-44h</td>
<td>Parameter 1</td>
<td>Hpara1</td>
</tr>
<tr>
<td></td>
<td>4Bh-48h</td>
<td>Parameter 2</td>
<td>Hpara2</td>
</tr>
<tr>
<td></td>
<td>......</td>
<td>......</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1F7h-1F4h</td>
<td>Parameter 109</td>
<td>Hpara6D</td>
</tr>
<tr>
<td></td>
<td>1FBh-1F8h</td>
<td>Parameter 110</td>
<td>Hpara6E</td>
</tr>
<tr>
<td></td>
<td>1FFh-1FCh</td>
<td>Parameter 111</td>
<td>Hpara6F</td>
</tr>
<tr>
<td></td>
<td>......</td>
<td>......</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2FFh-2FCh</td>
<td>Parameter 175</td>
<td>HparaAF</td>
</tr>
</tbody>
</table>
HParaType 00h: Primitive Vertex Data or Vertex Index

HParaType 00h is used for Primitive Vertex Data (for Vertex Command Mode) or Vertex Index (for Vertex Buffer Index Mode). There is no sub-address in this ParaType. The steps to fire 3D Engine are as follows:

Step 1: Set the correct value to all the related 3D globe registers through ParaType 01h, 02h, 03h, 04h, 10h, 11h and FEh.
Step 2: Sent Vertex Data or Vertex Index (according to HVertexMode) through ParaType 00h. CR would configure the vertex (according HVFVLEN and HnFVF) and generate fire signal automatically whenever all the vertices of a primitive are ready (according to HVCycle, H2and1VT and HPMType). CR would also generate the PLEND (Primitive List End) signal whenever the entire listed vertexes are finished (according to HVTXnum), or receive a “Stop Command”.

For next primitive list, repeat the two steps above.
HParaType 10h: Commands for Command Regulator

Sub-Address (Bits [31:24]): 00-7Ch

HParaType = 10h, Sub-Address = 00h
PCI Command Setting

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:9</td>
<td>WO xxh</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>WO xxh</td>
<td></td>
<td>Enable of Packaging the PCI Command in front of CR</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable 1: Enable</td>
</tr>
<tr>
<td>7:0</td>
<td>WO xxh</td>
<td></td>
<td>Number of ECLK Cycle for PCI Command Packaging Time Out</td>
</tr>
</tbody>
</table>

HParaType = 10h, Sub-Address = 02h
Read Register Back Command Setting

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:21</td>
<td>WO xxh</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>20:12</td>
<td>WO xxh</td>
<td></td>
<td>Reading-Back Register to Debug Port</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Address [10:2] for Reading-Back Register to Debug port; will be multiplexed with HJ2CR_RADR[8:2].</td>
</tr>
<tr>
<td>11</td>
<td>WO xxh</td>
<td></td>
<td>Enable Reading-Back Register to Debug Port</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable 1: Enable</td>
</tr>
<tr>
<td>10:8</td>
<td>WO xxh</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>7:0</td>
<td>WO xxh</td>
<td></td>
<td>ID for Reading-Back Register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0000 0000: Reading the RB registers from CR</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0000 0001: Reading the RB registers from FE (including VP, CL and SE)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0000 0010: Reading the RB registers from PE (including RZ and CZ)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0000 0011: Reading the RB registers from RC</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0000 0100: Reading the RB registers from PS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0000 0101: Reading the RB registers from XE</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0000 0110: Reading the RB registers from BE (including GEMI)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0000 0111: Reading the RB registers for Performance Profile Counters</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Others: Reserved</td>
</tr>
</tbody>
</table>

HParaType = 10h, Sub-Address = 03h
Address for Reading-Back Register

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:0</td>
<td>WO xxh</td>
<td></td>
<td>Address for Reading-Back Register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This address setting will read back E32CR WBREG[127:0].</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Bits[23:16]: HParaSubType</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Bits[15:8]: HParaType</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Bits[ 7: 0]: Sub-Address</td>
</tr>
</tbody>
</table>

HParaType = 10h, Sub-Address = 04h
Interrupt State Buffer Control 1

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:4</td>
<td>WO xxh</td>
<td></td>
<td>Lower 24-bit of Interrupt State Buffer Base Address &lt;HIRSBBAs Lower Bits&gt;</td>
</tr>
<tr>
<td>3:2</td>
<td>WO xxh</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>1:0</td>
<td>WO xxh</td>
<td></td>
<td>Interrupt State Buffer Location</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: System Local Frame Buffer (S.L.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: System Dynamic Frame Buffer (S.F.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: System Memory (S..M.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: Reserved</td>
</tr>
</tbody>
</table>
**HParaType = 10h, Sub-Address = 05h**

**Interrupt State Buffer Control 2**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:9</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 8           | WO        | xxh     | Store 3D Engine’s Register Setting in State Buffer <HIRSB4E3>  
0: Disable. It is not necessary to store 3D’s register setting (default).  
1: Enable. Store 3D’s register setting into the State Buffer. |
| 7:0         | WO        | xxh     | Higher 8-bit of Interrupt State Buffer Base Address <HIRSBBas Higher Byte>  
It is A[31:24]. |

**HParaType = 10h, Sub-Address = 06h**

**Left Vertex Data Threshold**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 23:0        | WO        | xxh     | Threshold Value of the Left Vertex Data within One DIP in CR <HIRFthStop>  
When the left vertex data in CR are more than HIRFthStop and HIRStop (see Sub-Address 07: bit [0] below) is set, CR would stop 3D immediately. Otherwise, CR would stop 3D at the end of DIP.  
Unit: Dword. |

**HParaType = 10h, Sub-Address = 07h**

**Interrupt Command**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:2</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 1           | WO        | xxh     | Interrupt Request for Pause <HIRPause>  
Force CR into “Pause State” until this bit is cleared.  
When in “Pause State”, CR just holds and not sends any command or data to the Video engine, 2D engine or 3D engine |
| 0           | WO        | xxh     | Interrupt Request for Stop <HIRStop>  
When this register is set, CR would interrupt the GPU and wait new Command triggered. |

Note: HIRPause and HIRStop can not be set at the same time.

**HParaType = 10h, Sub-Address = 10h**

**VMR Control**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:1</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>0</td>
<td>WO</td>
<td>xxh</td>
<td>VMR ID Buffer Status Reset</td>
</tr>
</tbody>
</table>

**HParaType = 10h, Sub-Address = 60h**

**AGP Command Setting 1**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 23:4        | WO        | xxh     | Lower 3 Bytes of AGP Buffer Start Address <HAGPBst Low Bytes>  
| 3:2         | WO        | xxh     | Reserved    |
| 1:0         | WO        | xxh     | AGP Buffer Location  
00: System Local Frame Buffer (S.L.)  
01: System Dynamic Frame Buffer (S.F.)  
10: System Memory (S.M.)  
11: Reserved |
### HParaType = 10h, Sub-Address = 61h
#### AGP Command Setting 2

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:8</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 7:0         | WO        | xxh     | Higher Byte of AGP Buffer Start Address  
*<HAGPBst High Byte>*  
It is A[31:24]. |

### HParaType = 10h, Sub-Address = 62h
#### AGP Command Setting 3

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 23:0        | WO        | xxh     | Lower 3 bytes of AGP Buffer End Address  

### HParaType = 10h, Sub-Address = 63h
#### AGP Command Setting 4

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:8</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 7:0         | WO        | xxh     | Higher Byte of AGP Buffer End Address  
It is A[31:24]. |

### HParaType = 10h, Sub-Address = 64h
#### AGP Command Setting 5

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 23:0        | WO        | xxh     | Lower 3 Bytes of AGP Buffer Pause Address  

### HParaType = 10h, Sub-Address = 65h
#### AGP Command Setting 6

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:10</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 9:8         | WO        | xxh     | AGP Buffer Pause Address ID  
00: HAGPBp (see bits 7:0) is the Pause Address of AGP Command Fetch. If AGP Command Fetcher wants to continuously fetch AGP Command again, it will start on the next address after HAGPBp.  
01: HAGPBp is the End Address of a portion of AGP Command Block. When AGP Command Fetcher reaches this address, it will start to fetch next AGP Command addressed by HAGPBst without waiting.  
10: HAGPBp is the AGP Command Stop Address. Whenever, AGP Command Fetcher reach this address, the AGP Command Fetching is finished. If we want to do another AGP Command Fetching, we have to set HAGPBTrig as 1.  
11: Reserved |
| 7:0         | WO        | xxh     | Higher Byte of AGP Buffer Pause Address  
*<HAGPBp High Byte>*  
It is A[31:24]. |

### HParaType = 10h, Sub-Address = 66h
#### AGP Command Setting 7

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 23:0        | WO        | xxh     | Lower 3 bytes of AGP Buffer Jump Address  
### HParaType = 10h, Sub-Address = 67h
**AGP Command Setting 8**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:8</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 7:0         | WO        | xxh     | Higher Byte of AGP Buffer Jump Address  
It is A[31:24]. |

### HParaType = 10h, Sub-Address = 68h
**AGP Command Setting 9**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:22</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 21:16       | WO        | xxh     | Threshold Value of Read AGP Command  
Default value is 8. |
| 15:5        | WO        | xxh     | Reserved    |
| 4           | WO        | xxh     | Clear Fence Queue |
| 3           | WO        | xxh     | Clear AGP Cycle |
| 2           | WO        | xxh     | Trigger Restore AGP Command Cycle  
Hardware will only restore AGP command. |
| 1           | WO        | xxh     | Trigger Restore 3D Register Cycle |
| 0           | WO        | xxh     | Trigger AGP Cycle  
The Trig signal of AGP command. |

### HParaType = 10h, Sub-Address = 69h
**Branch Command Setting**

<table>
<thead>
<tr>
<th>Bit [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:1</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 0          | WO        | xxh     | Default is On  
0: Disable AGP Branch.  Branched AGP Header (FE8x) is forbidden.  
1: Enable AGP Branch |

### HParaType = 10h, Sub-Address 6Ch
**Restore Command Setting 1**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 23:4        | WO        | xxh     | Lower 3 Bytes of Interrupt State Buffer Restore Start Address  
| 3:2         | WO        | xxh     | Reserved    |
| 1:0         | WO        | xxh     | Interrupt State Buffer Restore Location  
00: System Local Frame Buffer (S.L.)  
01: System Dynamic Frame Buffer (S.F.)  
10: System Memory (S.M.)  
11: Reserved |

### HParaType = 10h, Sub-Address 6Dh
**Restore Command Setting 2**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:8</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 7:0         | WO        | xxh     | Higher Byte of Interrupt State Buffer Restore Start Address  
**HPara Type = 10h, Sub-Address 6Eh**

**Restore Command Setting 3**

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:4</td>
<td>WO</td>
<td>xxh</td>
<td>Lower 3 bytes of AGP Buffer Restore Start Address</td>
</tr>
<tr>
<td>3:0</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

**HPara Type = 10h, Sub-Address 6Fh**

**Restore Command Setting 4**

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:8</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>7:0</td>
<td>WO</td>
<td>xxh</td>
<td>Higher Byte of AGP Buffer Restore Start Address</td>
</tr>
</tbody>
</table>

**HPara Type = 10h, Sub-Address 70h**

**CMDQ Setting 1**

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:4</td>
<td>WO</td>
<td>xxh</td>
<td>Lower 3 Bytes of Command Queue Start Address</td>
</tr>
<tr>
<td>3:2</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>1:0</td>
<td>WO</td>
<td>xxh</td>
<td>Command Queue Location</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: System Local Frame Buffer (S.L.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: System Dynamic Frame Buffer (S.F.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: System Memory (S.M.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: Reserved</td>
</tr>
</tbody>
</table>

**HPara Type = 10h, Sub-Address 71h**

**CMDQ Setting 2**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:0</td>
<td>WO</td>
<td>xxh</td>
<td>Lower 3 Bytes of Command Queue End Address</td>
</tr>
</tbody>
</table>

**HPara Type = 10h, Sub-Address 72h**

**CMDQ Setting 3**

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:16</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>15:8</td>
<td>WO</td>
<td>xxh</td>
<td>Higher Byte of Command Queue End Address</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>128-bit alignment.</td>
</tr>
<tr>
<td>7:0</td>
<td>WO</td>
<td>xxh</td>
<td>Higher Byte of Command Queue Start Address</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>128-bit alignment.</td>
</tr>
</tbody>
</table>

**HPara Type = 10h, Sub-Address 73h**

**CMDQ Setting 4**

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:0</td>
<td>WO</td>
<td>xxh</td>
<td>Length of Command Queue</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The minimum value is 24'h800 in unit of 128 bits.</td>
</tr>
</tbody>
</table>
### HParaType = 10h, Sub-Address = 74h

**CMDQ Setting 5**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:22</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>21:16</td>
<td>WO</td>
<td>xxh</td>
<td>Threshold Value of Write Command Queue FIFO</td>
</tr>
<tr>
<td>15:14</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>13:8</td>
<td>WO</td>
<td>xxh</td>
<td>Threshold Value of Read Command Queue FIFO</td>
</tr>
<tr>
<td>7:4</td>
<td>WO</td>
<td>xxh</td>
<td>Control Setting for CMDQ Read Request Interrupting Write Request</td>
</tr>
<tr>
<td>&amp;           &amp;         &amp; 0000: Never interrupt. CMDQ handles Read request only after CMDQ Write finished.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>&amp;           &amp;         &amp; 0001: Interrupt CMDQ Write request whenever CMDQ Read request arrived</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>&amp;           &amp;         &amp; 1000: Interrupt whenever 16 CMDQ Write requests accepted</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>&amp;           &amp;         &amp; 1001: Interrupt whenever 32 CMDQ Write requests accepted</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>&amp;           &amp;         &amp; 1100: Interrupt whenever 32 CMDQ Write request cycles completed</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>&amp;           &amp;         &amp; 1101: Interrupt whenever 64 CMDQ Write request cycles completed</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>&amp;           &amp;         &amp; Others: Reserved</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>2</td>
<td>WO</td>
<td>xxh</td>
<td>CMDQ Is Used for Command from AGP or PCI</td>
</tr>
<tr>
<td>&amp;           &amp;         &amp; 0: Store Command from PCI</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>&amp;           &amp;         &amp; 1: Store Command from AGP</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>WO</td>
<td>xxh</td>
<td>Enable Request Length for CMDQ of Command Regulator</td>
</tr>
<tr>
<td>&amp;           &amp;         &amp; 0: Disable. Always use 1 128-bit command in one request.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>&amp;           &amp;         &amp; 1: Enable. Allow having 1, 2, or 4 128-bit commands within one request.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>WO</td>
<td>xxh</td>
<td>Enable Command Queue</td>
</tr>
<tr>
<td>&amp;           &amp;         &amp; 0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>&amp;           &amp;         &amp; 1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### HParaType = 10h, Sub-Address = 78h

**CMDQ Setting 6**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:4</td>
<td>WO</td>
<td>xxh</td>
<td>Lower 3 Bytes of Command Queue Start Address for 2D/3D Command</td>
</tr>
<tr>
<td>3:2</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>1:0</td>
<td>WO</td>
<td>xxh</td>
<td>Command Queue Location for 2D/3D Command</td>
</tr>
<tr>
<td>&amp;           &amp;</td>
<td>00: System Local Frame Buffer (S.L.)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>&amp;           &amp;</td>
<td>01: System Dynamic Frame Buffer (S.F.)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>&amp;           &amp;</td>
<td>10: System Memory (S.M.)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>&amp;           &amp;</td>
<td>11: Reserved</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### HParaType = 10h, Sub-Address = 79h

**CMDQ Setting 7**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:0</td>
<td>WO</td>
<td>xxh</td>
<td>Lower 3 Bytes of Command Queue End Address for 2D/3D Command</td>
</tr>
</tbody>
</table>

### HParaType = 10h, Sub-Address = 7Ah

**CMDQ Setting 8**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:16</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>15:8</td>
<td>WO</td>
<td>xxh</td>
<td>Higher Byte of Command Queue End Address for 2D/3D Command</td>
</tr>
<tr>
<td>7:0</td>
<td>WO</td>
<td>xxh</td>
<td>Higher Byte of Command Queue Start Address for 2D/3D Command.</td>
</tr>
</tbody>
</table>
### HParaType = 10h, Sub-Address = 7Bh

#### CMDQ Setting 9

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 23:0        | WO        | xxh     | **Length of Command Queue for 2D/3D Command**  
The minimum value is 24'h800 in unit of 128 bits. |

### HParaType = 10h, Sub-Address = 7Ch

#### CMDQ Setting 10

<table>
<thead>
<tr>
<th>Bits [23:14]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:14</td>
<td>WO</td>
<td>xxh</td>
<td><strong>Reserved</strong></td>
</tr>
</tbody>
</table>
| 13:8         | WO        | xxh     | **Threshold Value of Read Command Queue FIFO for 2D/3D Command**  
0000: Never interrupt. CMDQ handles Read request only after CMDQ Write finished.  
0001: Interrupt CMDQ Write request whenever CMDQ Read request arrived.  
0010: Interrupt whenever 16 CMDQ Write requests accepted  
0011: Interrupt whenever 32 CMDQ Write requests accepted  
0100: Interrupt whenever 32 CMDQ Write request cycles completed  
1000: Interrupt whenever 64 CMDQ Write request cycles completed  
Others: Reserved |
| 7:4          | WO        | xxh     | **Control Setting for CMDQ Read Request Interrupting Write Request for 2D/3D Command**  
0000: Never interrupt. CMDQ handles Read request only after CMDQ Write finished.  
0001: Interrupt CMDQ Write request whenever CMDQ Read request arrived.  
0010: Interrupt whenever 16 CMDQ Write requests accepted  
0011: Interrupt whenever 32 CMDQ Write requests accepted  
0100: Interrupt whenever 32 CMDQ Write request cycles completed  
1000: Interrupt whenever 64 CMDQ Write request cycles completed  
1001: Interrupt whenever 32 CMDQ Write request cycles completed  
1100: Interrupt whenever 32 CMDQ Write request cycles completed  
1101: Interrupt whenever 64 CMDQ Write request cycles completed  
Others: Reserved |
| 3            | WO        | xxh     | **Reserved**                                      |
| 2            | WO        | xxh     | **CMDQ Is Used for Command from AGP or PCI for 2D/3D Command**  
0: Store command from PCI  
1: Store command from AGP |
| 1            | WO        | xxh     | **Enable Request Length for CMDQ of Command Regulator for 2D/3D Command**  
0: Disable. Always use 1 128-bit command in one request.  
1: Enable. Allow having 1, 2, or 4 128-bit commands within one request. |
| 0            | WO        | xxh     | **Enable Command Queue for 2D/3D Command**  
0: Disable  
1: Enable |
HParaType 11h: Commands for Frame Buffer Swapping and CR’s Miscellaneous Setting

Sub-Address (Bits [31:24]): 00-ABh

HParaType = 11h, Sub-Address = 00h
CR’s Miscellaneous Setting

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:17</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 16          | WO        | xxh     | Enable 2D/3D Request Lock Control  
0: Disable. When one of 3D/2D engines is busy, CR will not send commands to another engine.  
1: Enable. When one of 3D/2D engines is busy, CR sent commands to another engine but another engine does not access memory. Only one of the 2D and 3D engine is working in one time. However, E3FIRE can be sent to 3D engine when 2D engine is busy. Also, E2FIRE can be sent to 2D engine when 3D engine is busy. In the first case, Command Regulator will set CRLock3D before issuing E3FIRE and reset CRLock3D after 3D engine is idle. Similarly, CRLock2D is working in the same way. |
| 15:11       | WO        | xxh     | Reserved    |
| 10:8        | WO        | 010b    | The Depth N of FIFO 1 in CR  
000: n = 16  
001: n = 24  
010: n = 32 (default)  
011: n = 48  
100: n = 64  
Others: Reserved |
| 7:5         | WO        | 010b    | The Depth N of FIFO 2 in CR  
000: n = 16  
001: n = 24  
010: n = 32 (default)  
011: n = 48  
100: n = 64  
Others: Reserved |
| 4:2         | WO        | 010b    | The Depth N of FIFO 3 in CR  
000: n = 16  
001: n = 24  
010: n = 32 (default)  
011: n = 48  
100: n = 64  
Others: Reserved |
| 1           | WO        | xxh     | Reserved    |
| 0           | WO        | xxh     | Enable to Treat Followed CMDs as “Critical” (Not Breakable)  
0: The Command Queue can be broken by an “Interrupt command”  
1: The Command Queue can not be broken. The “STOP” procedure is executed only after this bit is cleared. |

HParaType = 11h, Sub-Address = 04h
Fence Command 1

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:20</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 19:0        | WO        | xxh     | Higher Bits of Fence Command Base Address  
If HFCMode[2]=1 (see Sub-Address:07 [19:16] below), it is the higher 20-bit Fence Command Base address for PCI Master Write (A[43:24]).  
If HFCMode[2]=0, it is the higher 12-bit Fence Type (FenceType[31:20]). |

HParaType = 11h, Sub-Address = 05h
Fence Command 2

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 23:4        | WO        | xxh     | Lower Bits of Fence Command Base Address  
If HFCMode[2]=1, it is the lower 24-bit Fence Command Base address for PCI Master Write (A[23:4]).  
If HFCMode[2]=0, it is the lower 24-bit Fence Type (FenceType[19:0]). |
| 3:0         | WO        | xxh     | Reserved    |
HParaType = 11h, Sub-Address = 06h
Fence Command 3

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:0</td>
<td>WO</td>
<td>xxh</td>
<td>Lower 24-bit Fence Command ID &lt;HFCID – Lower Bytes&gt;</td>
</tr>
</tbody>
</table>

HParaType = 11h, Sub-Address = 07h
Fence Command 4

<table>
<thead>
<tr>
<th>Bits [23:9]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23</td>
<td>WO</td>
<td>xxh</td>
<td>Fence Command Queue Full Skip</td>
</tr>
<tr>
<td>22</td>
<td>WO</td>
<td>xxh</td>
<td>Fence Command Interrupt Wait</td>
</tr>
<tr>
<td>21</td>
<td>WO</td>
<td>xxh</td>
<td>Fence Command Trigger</td>
</tr>
<tr>
<td>19:16</td>
<td>WO</td>
<td>xxh</td>
<td>Fence Command Mode &lt;HFCMode&gt;</td>
</tr>
</tbody>
</table>

Save Command 1

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:4</td>
<td>WO</td>
<td>xxh</td>
<td>Lower 24-bit of Save Buffer Start Base Address &lt;HSvBSt Lower Bits&gt;</td>
</tr>
<tr>
<td>3:2</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>1:0</td>
<td>WO</td>
<td>xxh</td>
<td>Save Buffer Location</td>
</tr>
</tbody>
</table>

Save Command 2

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:9</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>8</td>
<td>WO</td>
<td>xxh</td>
<td>Store 3D Engine’s Register Write Enable &lt;HSvWTEn&gt;</td>
</tr>
<tr>
<td>7:0</td>
<td>WO</td>
<td>xxh</td>
<td>Higher 8-bit of Save Buffer Start Base Address &lt;HSvBSt Higher Byte&gt;</td>
</tr>
</tbody>
</table>
**HParaType = 11h, Sub-Address = 0Bh**

**Save Command 3**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:1</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>0</td>
<td>WO</td>
<td>xxh</td>
<td>Save Trig for Save 3D Write Back Registers&lt;br&gt;When this register is set, CR saves 3D write back registers and then keep running.</td>
</tr>
</tbody>
</table>

**Note:**
Priority HIRSB4E3 > HSvWTEn, if HIRSB4E3=1, all 3D save register will save to HIRSBBAs not HSvBSst.

**HIRSB4E3:** HparaType 10h, Sub-Address 05h, bit [8]
**HSvWTEn:** HparaType 11h, Sub-Address 05h, bit [8]
**HIRSBBAs:** HparaType 10h, Sub-Address 05h, bits [7:0] and HparaType 10h, Sub-Address 04h, bits [23:4]
**HIRSBBAs:** HparaType 11h, Sub-Address 09h, bits [7:0] and HparaType 11h, Sub-Address 08h, bits [23:4]

**HParaType = 11h, Sub-Address = 10h**

**Frame Buffer Automatic Swapping 1**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:3</td>
<td>WO</td>
<td>xxh</td>
<td>Lower 3 Bytes of Display Frame Buffer Base Address of IGA1</td>
</tr>
<tr>
<td>2</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>1:0</td>
<td>WO</td>
<td>xxh</td>
<td>Display Frame Buffer Location&lt;br&gt;00: System Local Frame Buffer (S.L.)&lt;br&gt;01: System Dynamic Frame Buffer (S.F.)&lt;br&gt;10: System Memory (S.M.)&lt;br&gt;11: Reserved</td>
</tr>
</tbody>
</table>

**HParaType = 11h, Sub-Address = 11h**

**Frame Buffer Automatic Swapping 2**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:8</td>
<td>WO</td>
<td>xxh</td>
<td>Frame Flip Count of IGA1</td>
</tr>
<tr>
<td>7:0</td>
<td>WO</td>
<td>xxh</td>
<td>Higher Byte of Display Frame Buffer Base Address of IGA1</td>
</tr>
</tbody>
</table>

**HParaType = 11h, Sub-Address = 12h**

**Frame Buffer Automatic Swapping 3**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:4</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>3</td>
<td>WO</td>
<td>xxh</td>
<td>Enable Frame Buffer Automatic Swapping for IGA1</td>
</tr>
<tr>
<td>2</td>
<td>WO</td>
<td>0</td>
<td>Skip to Wait Blank When Automatic Swapping for IGA1 (default=0)</td>
</tr>
<tr>
<td>1:0</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

**HParaType = 11h, Sub-Address = 13-17h: Reserved** (for Frame Buffer Automatic Swapping)

**HParaType = 11h, Sub-Address = 18h**

**Frame Buffer Automatic Swapping 4**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:3</td>
<td>WO</td>
<td>xxh</td>
<td>Lower 3 Bytes of Display Frame Buffer Base Address of IGA2</td>
</tr>
<tr>
<td>2</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>1:0</td>
<td>WO</td>
<td>xxh</td>
<td>Display Frame Buffer Location of IGA2&lt;br&gt;00: System Local Frame Buffer (S.L.)&lt;br&gt;01: System Dynamic Frame Buffer (S.F.)&lt;br&gt;10: System Memory (S.M.)&lt;br&gt;11: Reserved</td>
</tr>
</tbody>
</table>
### HParaType = 11h, Sub-Address = 19h
**Frame Buffer Automatic Swapping 5**

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[23:0]</td>
<td>WO</td>
<td>xxh</td>
<td>Frame Flip Count of IGA2</td>
</tr>
<tr>
<td>7:0</td>
<td>WO</td>
<td>xxh</td>
<td>Higher Byte of Display Frame Buffer Base Address of IGA2</td>
</tr>
</tbody>
</table>

### HParaType = 11h, Sub-Address = 1Ah
**Frame Buffer Automatic Swapping 6**

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[23:0]</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>3</td>
<td>WO</td>
<td>xxh</td>
<td>Enable Frame Buffer Automatic Swapping for IGA2</td>
</tr>
<tr>
<td>2</td>
<td>WO</td>
<td>0</td>
<td>Skip to Wait Blank When Automatic Swapping for IGA2, (default=0)</td>
</tr>
<tr>
<td>1:0</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

### HParaType = 11h, Sub-Address = 1B-2Fh: Reserved
(for Frame Buffer Automatic Swapping)

### HParaType = 11h, Sub-Address = 30h
**Frame Buffer Automatic Swapping 7**

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[23:0]</td>
<td>WO</td>
<td>xxh</td>
<td>Lower 3 Bytes of Display Frame Buffer Base Address of IGA Duo-view Control</td>
</tr>
<tr>
<td>2</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>1:0</td>
<td>WO</td>
<td>xxh</td>
<td>Display Frame Buffer location of IGA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: System Local Frame Buffer (S.L.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: System Dynamic Frame Buffer (S.F.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: System Memory (S.M.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: Reserved</td>
</tr>
</tbody>
</table>

### HParaType = 11h, Sub-Address = 31h
**Frame Buffer Automatic Swapping 8**

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[23:0]</td>
<td>WO</td>
<td>xxh</td>
<td>Frame Flip Count of IGA</td>
</tr>
<tr>
<td>7:0</td>
<td>WO</td>
<td>xxh</td>
<td>Higher Byte of Display Frame Buffer Base Address of IGA</td>
</tr>
</tbody>
</table>

### HParaType = 11h, Sub-Address = 32h
**Frame Buffer Automatic Swapping 9**

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[23:0]</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>3</td>
<td>WO</td>
<td>xxh</td>
<td>Enable Frame Buffer Automatic Swapping for IGA</td>
</tr>
<tr>
<td>2</td>
<td>WO</td>
<td>0</td>
<td>Skip to Wait blank When Automatic Swapping for IGA, (default=0)</td>
</tr>
<tr>
<td>1:0</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

### HParaType = 11h, Sub-Address = 33-34h: Reserved
(for Frame Buffer Automatic Swapping)
### HParaType = 11h, Sub-Address = 68h
First Branch Command Setting 1

HParaType 11, Sub-Address 68-6Bh are active only in “AGP format” command.

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:1</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>0</td>
<td>WO</td>
<td>xxh</td>
<td>Branch Type</td>
</tr>
</tbody>
</table>

- **Branch Type**
  - 0: Branch for Normal (default). Branch commands are independent on previous command. Insert Branch commands in CR command queue.
  - 1: Branch for Restore. Wait the completion of all previous commands before Branch header (FE8x), and then activate Branch request.

### HParaType = 11h, Sub-Address = 69h
First Branch Command Setting 2

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:1</td>
<td>WO</td>
<td>xxh</td>
<td>Lower 3 Bytes of Branch Buffer Start Address</td>
</tr>
</tbody>
</table>

- It is A[23:1] where A[0] is useless. (Unit: Word, 16-bit alignment)

Note to Driver and hardware:
1. The branch buffer address is modified to be alignment with 16 bits because of this address points to the vertex index in vertex buffer.
2. Branch for 3D vertex index in vertex buffer (16bits aligned) is only from Header3 (Do not set in Header 2).
3. DWcount of header = valid vertex data DWcount + invalid vertex data DWcount before valid vertex data (ex: HAGPBranchL[3:1]=2, i.e. invalid vertex data(16-bit alignment) DWcount before valid vertex data = 1)

| 0           | WO        | xxh     | Reserved    |

### HParaType = 11h, Sub-Address = 6Ah
First Branch Command Setting 3

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:22</td>
<td>WO</td>
<td>xxh</td>
<td>Branch Buffer Location</td>
</tr>
</tbody>
</table>

- 00: System Local Frame Buffer (S.L.)
- 01: System Dynamic Frame Buffer (S.F.)
- 10: System Memory (S.M.)
- 11: Reserved

| 21:8        | WO        | xxh     | Reserved    |
| 7:0         | WO        | xxh     | Higher Byte of Branch Buffer Start Address |

It is A[31:24].

Note: For Sub-Address 6Ah, branch command trigger is hidden in AGP header (FE8x). “NESTED” branch buffer is forbidden.

### HParaType = 11h, Sub-Address = 6Bh
First Branch Command Setting 4

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:0</td>
<td>WO</td>
<td>xxh</td>
<td>Size of Branch Buffer</td>
</tr>
</tbody>
</table>

In unit of 16 bytes (128 bits).

### HParaType = 11h, Sub-Address 6Ch: Reserved
(for Second Branch Command Setting)
**HParaType = 11h, Sub-Address 6Dh**

Second Branch Command Setting 1

T11A6C-6F (HparaType 11, Sub-Address 6C-6Fh) are active only in “AGP format” command.

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 23:1        | WO        | xxh     | **Lower 3 Bytes of Branch Buffer Start Address**  
It is A[23:1] where A[0] is useless. (Unit: Word, 16-bit alignment)  
Note to Driver and hardware:  
1. The branch buffer address is modified to be alignment with 16 bits because of this address points to the vertex index in  
   vertex buffer.  
2. Branch for 3D vertex index in vertex buffer (16bits aligned) is only from Header3 (Do not set in Header 2). |
| 0           | WO        | xxh     | Reserved    |

**HParaType = 11h, Sub-Address 6Eh**

Second Branch Command Setting 2

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 23:22       | WO        | xxh     | **Branch Buffer Location**  
00: System Local Frame Buffer (S.L.)  
01: System Dynamic Frame Buffer (S.F.)  
10: System Memory (S.M.)  
11: Reserved |
| 21:8        | WO        | xxh     | Reserved    |
| 7:0         | WO        | xxh     | **Higher Byte of Branch Buffer Start Address**  
It is A[31:24]. |

Note: For Sub-Address 6Eh, branch command trigger is hidden in AGP header (FE8x). “NESTED” branch buffer is forbidden.

**HParaType = 11h, Sub-Address 6Fh**

Second Branch Command Setting 3

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 23:0        | WO        | xxh     | **Size of Branch Buffer**  
In unit of 16 bytes (128 bits). |

**HParaType = 11h, Sub-Address AAh**

SW Inspection (R/W) 1

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:0</td>
<td>RW</td>
<td>xxh</td>
<td><strong>Software Event TAG for Software Inspection</strong></td>
</tr>
</tbody>
</table>

**HParaType = 11h, Sub-Address ABh**

SW Inspection (R/W) 2

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:0</td>
<td>RW</td>
<td>xxh</td>
<td><strong>Software Event TAG for Software Inspection</strong></td>
</tr>
</tbody>
</table>
CR Registers in 2D Register Space (60-6Ch)

For detailed 2D register descriptions, please refer to 2D chapter.

### Offset Address: 60h

#### 3D / 2D 1D Control

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td></td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td></td>
<td>xxh</td>
<td>3D / 2D Command Force Start (Software Must Fill Zero)</td>
</tr>
<tr>
<td>29:28</td>
<td></td>
<td>xxh</td>
<td>3D / 2D Command Status&lt;br&gt;00: 3D / 2D command start&lt;br&gt;01: 3D / 2D command end&lt;br&gt;10: 3D / 2D command end and wait 3D idle&lt;br&gt;11: 3D / 2D command end and wait 2D idle</td>
</tr>
<tr>
<td>27</td>
<td></td>
<td>xxh</td>
<td>3D / 2D Command Stream Kinds</td>
</tr>
<tr>
<td>26:24</td>
<td></td>
<td>xxh</td>
<td>3D / 2D Working Buffer Number</td>
</tr>
<tr>
<td>23:16</td>
<td></td>
<td>xxh</td>
<td>Reserved for Hardware Use</td>
</tr>
<tr>
<td>15:0</td>
<td></td>
<td>xxh</td>
<td>3D / 2D Working ID</td>
</tr>
</tbody>
</table>

### Offset Address: 6Ch

#### 3D / 2D Wait Control

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td></td>
<td>xxh</td>
<td>Wait HQV0 Idle</td>
</tr>
<tr>
<td>30</td>
<td></td>
<td>xxh</td>
<td>Wait HQV1 Idle</td>
</tr>
<tr>
<td>29</td>
<td></td>
<td>xxh</td>
<td>Wait MC Idle</td>
</tr>
<tr>
<td>28:24</td>
<td></td>
<td>xxh</td>
<td>Wait Idle Count</td>
</tr>
<tr>
<td>23</td>
<td></td>
<td>xxh</td>
<td>Wait 3D Idle – for 3D / 2D Command Path</td>
</tr>
<tr>
<td>22</td>
<td></td>
<td>xxh</td>
<td>Wait 2D Idle – for 3D / 2D Command Path</td>
</tr>
<tr>
<td>21</td>
<td></td>
<td>xxh</td>
<td>Wait DMA Channel 3 Idle</td>
</tr>
<tr>
<td>20</td>
<td></td>
<td>xxh</td>
<td>Wait DMA Channel 2 Idle</td>
</tr>
<tr>
<td>19</td>
<td></td>
<td>xxh</td>
<td>Wait DMA Channel 1 Idle</td>
</tr>
<tr>
<td>18</td>
<td></td>
<td>xxh</td>
<td>Wait DMA Channel 0 Idle</td>
</tr>
<tr>
<td>17</td>
<td></td>
<td>xxh</td>
<td>Wait LCD DN Idle</td>
</tr>
<tr>
<td>16:14</td>
<td></td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>13</td>
<td></td>
<td>xxh</td>
<td>Command Wait Later IGA VBLK Interval to Start to Work</td>
</tr>
<tr>
<td>12</td>
<td></td>
<td>xxh</td>
<td>Command Wait Former IGA VBLK Interval to Start to Work</td>
</tr>
<tr>
<td>11</td>
<td></td>
<td>xxh</td>
<td>Command Wait Later IGA VBLK End Pulse to Start to Work</td>
</tr>
<tr>
<td>10</td>
<td></td>
<td>xxh</td>
<td>Command Wait Former IGA VBLK End Pulse to Start to Work</td>
</tr>
<tr>
<td>9</td>
<td></td>
<td>xxh</td>
<td>Command Wait Later IGA VBLK Start Pulse to Start to Work</td>
</tr>
<tr>
<td>8</td>
<td></td>
<td>xxh</td>
<td>Command Wait Former IGA VBLK Start Pulse to Start to Work</td>
</tr>
<tr>
<td>7:6</td>
<td></td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>5</td>
<td></td>
<td>xxh</td>
<td>Command Wait IGA2 VBLK Interval to Start to Work</td>
</tr>
<tr>
<td>4</td>
<td></td>
<td>xxh</td>
<td>Command Wait IGA1 VBLK Interval to Start to Work</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td>xxh</td>
<td>Command Wait IGA2 VBLK End Pulse to Start to Work</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>xxh</td>
<td>Command Wait IGA1 VBLK End Pulse to Start to Work</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>xxh</td>
<td>Command Wait IGA2 VBLK Start Pulse to Start to Work</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td>xxh</td>
<td>Command Wait IGA1 VBLK Start Pulse to Start to Work</td>
</tr>
</tbody>
</table>
CR Registers in Video Control Register Space (3260-326Ch)

For detailed video register descriptions, please refer to Video Overlay Engine chapter.

**Offset Address: 3260h**

**DVD / Video ID Control**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>30</td>
<td>WO</td>
<td>xxh</td>
<td>DVD / Video Command Force Start (Software Must Fill Zero)</td>
</tr>
<tr>
<td>29:28</td>
<td>WO</td>
<td>xxh</td>
<td>DVD / Video Command Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: DVD / Video command start</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: DVD / Video command end</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: DVD / Video command end and wait DVD idle</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: DVD / Video command end and wait Video idle</td>
</tr>
<tr>
<td>27</td>
<td>WO</td>
<td>xxh</td>
<td>DVD / Video Command Stream Kinds</td>
</tr>
<tr>
<td>26:25</td>
<td>WO</td>
<td>xxh</td>
<td>DVD / Video Working Buffer Number</td>
</tr>
<tr>
<td>24:22</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved for Hardware Use</td>
</tr>
<tr>
<td>21</td>
<td>WO</td>
<td>xxh</td>
<td>DVD / Video Working ID</td>
</tr>
</tbody>
</table>

**Offset Address: 326Ch**

**DVD / Video Wait Control**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>WO</td>
<td>xxh</td>
<td>Wait 3D Idle – for Video Command Path</td>
</tr>
<tr>
<td>30</td>
<td>WO</td>
<td>xxh</td>
<td>Wait 2D Idle – for Video Command Path</td>
</tr>
<tr>
<td>29:25</td>
<td>WO</td>
<td>xxh</td>
<td>Wait Idle Count</td>
</tr>
<tr>
<td>24:22</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>21</td>
<td>WO</td>
<td>xxh</td>
<td>Wait HQV1 Starting Address Load</td>
</tr>
<tr>
<td>20</td>
<td>WO</td>
<td>xxh</td>
<td>Wait HQV1 Fire Bit</td>
</tr>
<tr>
<td>19</td>
<td>WO</td>
<td>xxh</td>
<td>Wait HQV1 HW Flip FIFO Full</td>
</tr>
<tr>
<td>18</td>
<td>WO</td>
<td>xxh</td>
<td>Wait HQV1 Subpicture / Updateoverlay Flip</td>
</tr>
<tr>
<td>17</td>
<td>WO</td>
<td>xxh</td>
<td>Wait HQV1 SW Flip</td>
</tr>
<tr>
<td>16</td>
<td>WO</td>
<td>xxh</td>
<td>Wait HQV1 Finish a Frame</td>
</tr>
<tr>
<td>15</td>
<td>WO</td>
<td>xxh</td>
<td>Wait DMA Channel 3 Idle</td>
</tr>
<tr>
<td>14</td>
<td>WO</td>
<td>xxh</td>
<td>Wait DMA Channel 2 Idle</td>
</tr>
<tr>
<td>13</td>
<td>WO</td>
<td>xxh</td>
<td>Wait DMA Channel 1 Idle</td>
</tr>
<tr>
<td>12</td>
<td>WO</td>
<td>xxh</td>
<td>Wait DMA Channel 0 Idle</td>
</tr>
<tr>
<td>11:6</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>5</td>
<td>WO</td>
<td>xxh</td>
<td>Wait HQV0 Starting Address Load</td>
</tr>
<tr>
<td>4</td>
<td>WO</td>
<td>xxh</td>
<td>Wait HQV0 Fire Bit</td>
</tr>
<tr>
<td>3</td>
<td>WO</td>
<td>xxh</td>
<td>Wait HQV0 Hardware Flip FIFO Full</td>
</tr>
<tr>
<td>2</td>
<td>WO</td>
<td>xxh</td>
<td>Wait HQV0 Subpicture / Updateoverlay Flip</td>
</tr>
<tr>
<td>1</td>
<td>WO</td>
<td>xxh</td>
<td>Wait HQV0 Software Flip</td>
</tr>
<tr>
<td>0</td>
<td>WO</td>
<td>xxh</td>
<td>Wait HQV0 Finish a Frame</td>
</tr>
</tbody>
</table>
3D REGISTERS

This chapter provides detailed 3D register descriptions. Please also refer to Chapter “Command Regulator”, Section “Definition of I/O Register” for basic introduction on 3D/CR operations and 3D/CR register summary table.

HParaType 00h: Primitive Vertex Data or Vertex Index

HParaType 00h is used for Primitive Vertex Data (for Vertex Command Mode) or Vertex Index (for Vertex Buffer Index Mode). There is no sub-address in this ParaType. The steps of how to fire 3D Engine are as follows:

   Step 1: Set the correct value to all the related 3D globe registers through ParaType 01h, 02h, 03h, 04h, 10h, 11h and FEh.
   Step 2: Sent Vertex Data or Vertex Index (according to HVertexMode) through ParaType 00h. CR would configure the vertex (according HVFVLEN and HnFVF) and generate fire signal automatically whenever all the vertices of a primitive are ready (according to HVCycle, H2and1VT and HPMTYPE). CR would also generate the PLEND (Primitive List End) signal whenever the entire listed vertexes are finished (according to HVTXnum), or receive a “Stop Command”.

For next primitive list, repeat the two steps above.
### HParaType 01h: Attribute Other Than Texture

**Sub-Address (Bits [31:24]): 00-AAh**

#### HParaType = 01h, Sub-Address = 00-0Fh

**Enable Setting 1**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23</td>
<td>WO xxh</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>WO xxh</td>
<td>Inverse Enable (Disable) BE’s 32-byte (Adjacent 128-bit) Packing</td>
<td>0: Enable 1: Disable</td>
</tr>
<tr>
<td>21</td>
<td>WO xxh</td>
<td>Inverse Enable (Disable) BE’s Smart Packing</td>
<td>0: Enable 1: Disable</td>
</tr>
<tr>
<td>20</td>
<td>WO xxh</td>
<td>Enable Alpha Test Result of RT0 for All Render Targets (RTn)</td>
<td>0: The success or failure of alpha test for RTn depends on its own alpha test result and HenATMRTn, where n = 0 .. 3. 1: Execution of the alpha test for RT0 and all render targets depend on the result to be killed or not. HenATMRT0, HenATMRT1, HenATMRT2 &amp; HenATMRT3 are ignored</td>
</tr>
<tr>
<td>19</td>
<td>WO xxh</td>
<td>Enable Alpha Test for Render Target 3 &lt;HenATMRT3&gt;</td>
<td>0: Disable 1: Enable</td>
</tr>
<tr>
<td>18</td>
<td>WO xxh</td>
<td>Enable Alpha Test for Render Target 2 &lt;HenATMRT2&gt;</td>
<td>0: Disable 1: Enable</td>
</tr>
<tr>
<td>17</td>
<td>WO xxh</td>
<td>Enable Alpha Test for Render Target 1 &lt;HenATMRT1&gt;</td>
<td>0: Disable 1: Enable</td>
</tr>
<tr>
<td>16</td>
<td>WO xxh</td>
<td>Enable Alpha Test for Render Target 0 &lt;HenATMRT0&gt;</td>
<td>0: Disable 1: Enable</td>
</tr>
<tr>
<td>15</td>
<td>WO xxh</td>
<td>Enable Specula Color for Render Target 3</td>
<td>0: Disable 1: Enable</td>
</tr>
<tr>
<td>14</td>
<td>WO xxh</td>
<td>Enable Specula Color for Render Target 2</td>
<td>0: Disable 1: Enable</td>
</tr>
<tr>
<td>13</td>
<td>WO xxh</td>
<td>Enable Specula Color for Render Target 1</td>
<td>0: Disable 1: Enable</td>
</tr>
<tr>
<td>12</td>
<td>WO xxh</td>
<td>Enable Specula Color for Render Target 0</td>
<td>0: Disable 1: Enable</td>
</tr>
<tr>
<td>11</td>
<td>WO xxh</td>
<td>Enable Fog for Render Target 3</td>
<td>0: Disable 1: Enable</td>
</tr>
<tr>
<td>10</td>
<td>WO xxh</td>
<td>Enable Fog for Render Target 2</td>
<td>0: Disable 1: Enable</td>
</tr>
<tr>
<td>9</td>
<td>WO xxh</td>
<td>Enable Fog for Render Target 1</td>
<td>0: Disable 1: Enable</td>
</tr>
<tr>
<td>8</td>
<td>WO xxh</td>
<td>Enable Fog for Render Target 0</td>
<td>0: Disable 1: Enable</td>
</tr>
<tr>
<td>7</td>
<td>WO xxh</td>
<td>Enable Alpha Blending for Render Target 3</td>
<td>0: Disable 1: Enable</td>
</tr>
<tr>
<td>6</td>
<td>WO xxh</td>
<td>Enable Alpha Blending for Render Target 2</td>
<td>0: Disable 1: Enable</td>
</tr>
<tr>
<td>5</td>
<td>WO xxh</td>
<td>Enable Alpha Blending for Render Target 1</td>
<td>0: Disable 1: Enable</td>
</tr>
<tr>
<td>4</td>
<td>WO xxh</td>
<td>Enable Alpha Blending for Render Target 0</td>
<td>0: Disable 1: Enable</td>
</tr>
<tr>
<td>3</td>
<td>WO xxh</td>
<td>Enable Dither for Render Target 3</td>
<td>0: Disable 1: Enable</td>
</tr>
<tr>
<td>2</td>
<td>WO xxh</td>
<td>Enable Dither for Render Target 2</td>
<td>0: Disable 1: Enable</td>
</tr>
<tr>
<td>1</td>
<td>WO xxh</td>
<td>Enable Dither for Render Target 1</td>
<td>0: Disable 1: Enable</td>
</tr>
<tr>
<td>0</td>
<td>WO xxh</td>
<td>Enable Dither for Render Target 0</td>
<td>0: Disable 1: Enable</td>
</tr>
</tbody>
</table>
### 3D Registers

**HParaType = 01h, Sub-Address = 01h**

#### Enable Setting 2

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 23          | WO        | xxh     | Enable Line Drawing from Up/Left to Down/Right  
0: Draw line from vertex a to vertex b.  
1: For vertical line, draw from up vertex to down vertex. For horizontal line, draw from left vertex to right vertex. |
| 22          | WO        | xxh     | Enable Diamond Rule for Line Drawing  
0: Disable  
1: Enable |
| 21          | WO        | xxh     | Enable Point Sprite  
0: Disable  
1: Enable  
This setting is only available for PMType "point" and "triangle point". All Points have sizes (default is 1.0), and Point Sprite only affects the texture coordinate.  
**If non-PointSprite points:***All the texture coordinates of point 4 vertexes are all those from FVF.**  
**If PointSprite points:**  
Texture coordinate of the upper-left corner is (0, 0, 0, 1).  
Texture coordinate of the upper-right corner is (1, 0, 0, 1).  
Texture coordinate of the lower-left corner is (0, 1, 0, 1).  
Texture coordinate of the lower-right corner is (1, 1, 0, 1). |
| 20          | WO        | xxh     | Enable Clipping Coordinate to Screen Coordinate Transformation  
0: Disable  
1: Enable |
| 19          | WO        | xxh     | Enable Fog Perspective Correction  
0: Disable  
1: Enable |
| 18          | WO        | xxh     | Enable Spectra Color Perspective Correction  
0: Disable  
1: Enable |
| 17          | WO        | xxh     | Enable Diffuse Color Perspective Correction  
0: Disable  
1: Enable |
| 16:14       | WO        | xxh     | Number of Render Target  
000: Only RT0  
001: RT0 & RT1  
010: RT0, RT1 and RT2  
011: RT0, RT1, RT2 and RT3  
1xx: Reserved |
| 13          | WO        | xxh     | Enable of Coarse Z Test  
0: Disable  
1: Enable  
Note that Coarse Z Test is only available for triangles, not the lines. |
| 12          | WO        | xxh     | Enable Vertex Cache  
0: Disable  
1: Enable |
| 11          | WO        | xxh     | Enable Clipping Engine  
0: Disable  
1: Enable |
| 10          | WO        | xxh     | Enable Pixel Shader  
0: Disable (Texture map is also disabled)  
1: Enable |
| 9           | WO        | xxh     | Enable Writing Coarse Z Buffer  
0: Do not update the Coarse Z Buffer  
1: Enable |
| 8           | WO        | xxh     | Enable Texture Cache  
0: Disable Texture Cache and Clear Texture Cache  
1: Enable |
| 7           | WO        | xxh     | Enable Back Face Culling  
0: Disable  
1: Enable  
**<HenBFCull>** |
| 6           | WO        | xxh     | Enable Color Write  
0: Disable  
1: Enable |
| 5           | WO        | xxh     | Enable Anti-Aliasing  
0: Disable  
1: Enable |
| 4           | WO        | xxh     | Enable Stencil Test  
0: Disable (Always pass)  
1: Enable (Depth buffer must contain stencil bits) |
| 3           | WO        | xxh     | Enable Z Test  
0: Disable (Always pass)  
1: Enable |
| 2           | WO        | xxh     | Enable Z Write  
0: Disable  
1: Enable |
| 1           | WO        | xxh     | Enable Stipple Pattern  
0: Disable  
1: Enable |
| 0           | WO        | xxh     | Enable Line Pattern  
0: Disable  
1: Enable |
HParaType = 01h, Sub-Address = 02h
Enable Setting 3

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:2</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>1</td>
<td>WO</td>
<td>xxh</td>
<td>Clear Read-Color Cache (RC Cache)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>RC Cache will be cleared while this bit is set to 1.</td>
</tr>
<tr>
<td>0</td>
<td>WO</td>
<td>xxh</td>
<td>Enable Read-Color Cache</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable</td>
</tr>
</tbody>
</table>

HParaType = 01h, Sub-Address = 03-0Fh: Reserved (for Enable Setting)

HParaType = 01h, Sub-Address = 10h
Z Setting 1

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:0</td>
<td>WO</td>
<td>xxh</td>
<td>ZW Buffer Base Address</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>In unit of 256 bytes.</td>
</tr>
</tbody>
</table>

HParaType = 01h, Sub-Address = 11h
Z Setting 2

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>22:13</td>
<td>WO</td>
<td>xxh</td>
<td>ZW Buffer Pitch &lt;HZWBPitch&gt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>In unit of 32 bytes for linear mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>In unit of tile (256 bytes) for tile mode.</td>
</tr>
<tr>
<td>12</td>
<td>WO</td>
<td>xxh</td>
<td>Enable Reading-Z Cache</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td>11</td>
<td>WO</td>
<td>xxh</td>
<td>Clear Reading-Z Cache</td>
</tr>
<tr>
<td>10</td>
<td>WO</td>
<td>xxh</td>
<td>Mode of Reading-Z Cache</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: 128-bit mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: 256-bit mode</td>
</tr>
<tr>
<td>9</td>
<td>WO</td>
<td>xxh</td>
<td>Z and Stencil Value are written through to BE directly</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Fully data path from PERZ through PS and RC, and then to BE</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Short data path from PERZ to BE directly</td>
</tr>
<tr>
<td>8:2</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>1:0</td>
<td>WO</td>
<td>xxh</td>
<td>Location Setting of Z Buffer</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: System Local Frame Buffer (S.L.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: System Dynamic Frame Buffer (S.F.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: Reserved (System Memory)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: Reserved</td>
</tr>
</tbody>
</table>
### HParaType = 01h, Sub-Address = 12h

#### Z Setting 3

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23</td>
<td>WO</td>
<td>xxh</td>
<td>ZW Buffer Type</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: ZW buffer stores Z value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: ZW buffer stores W value (PP replaces Z by W)</td>
</tr>
<tr>
<td>22</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>21</td>
<td>WO</td>
<td>xxh</td>
<td>Force the Z Value from 1.0 to 1.0- (from 1.00000000h to 0.FFFFFFFFh)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Keep the original 1.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Force to 1.0- whenever Z equals to 1.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This register is only useful for fixed-point format.</td>
</tr>
<tr>
<td>20</td>
<td>WO</td>
<td>xxh</td>
<td>Clamp the Z Value is over 1.0 to 1.0- (from 1.00000000h to 0.FFFFFFFFh)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Keep the original value over 1.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Clamp to 1.0- whenever Z is over 1.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This register is only useful for fixed-point format.</td>
</tr>
<tr>
<td>19</td>
<td>WO</td>
<td>xxh</td>
<td>Clamp the Z Value is Negative to Zero- (from –x.00000000h to 0.00000000h)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Keep the original negative value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Clamp to 0.0- whenever Z is negative</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Note: These clamping registers do not affect the test of nearby or distant plane. The test of the nearby or distant plane is by the original biased and un-clamped Z value with floating format.</td>
</tr>
<tr>
<td>18:16</td>
<td>WO</td>
<td>xxh</td>
<td>ZW Buffer Format</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>For Z Buffer</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>000: 16-bit fixed-point format, 0.0 ≤ Z &lt; 1.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>001: 16-bit floating format s[5].10 from +2^31<em>1.FFFF to –2^31</em>1.FFFF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>010: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>011: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100: 32-bit fixed-point format, 0.0 ≤ Z &lt; 1.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>101: 32-bit fixed-point format s[8].23</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>110: 24-bit fixed-point format Z, 0.0 ≤ Z &lt; 1.0, and Stencil</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Z is located in bit [31:8], Stencil is located in bit [7:0]</td>
</tr>
<tr>
<td>15:7</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>6:5</td>
<td>WO</td>
<td>xxh</td>
<td>Location Setting of Separated Stencil Buffer</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: System Local Frame Buffer (S.L.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: System Dynamic Frame Buffer (S.F.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: Reserved (System Memory)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: Reserved</td>
</tr>
<tr>
<td>4</td>
<td>WO</td>
<td>xxh</td>
<td>Write Stencil Value of the Separated Stencil Buffer to the Z Buffer</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Normal</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Force “STVALID” as true and stencil operation as “Keep”, so the stencil value in the separated buffer can be filled into Z buffer.</td>
</tr>
<tr>
<td>3</td>
<td>WO</td>
<td>xxh</td>
<td>Synchronized with the Separated Stencil Value in Z Buffer</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Indicate whether the stencil value in the separated stencil buffer is synchronized with the stencil value in Z buffer.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: No synchronization. Hardware just updates the stencil value in the separated stencil buffer, which may not be synchronized to the stencil value in Z buffer.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: The stencil value in the separated stencil buffer is synchronized to the stencil value in Z buffer. Hardware would update the separated stencil buffer and Z buffer.</td>
</tr>
<tr>
<td>2</td>
<td>WO</td>
<td>xxh</td>
<td>Existence of Separated Stencil Buffer</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: No separated stencil buffer</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: There is a separated stencil buffer</td>
</tr>
<tr>
<td>1</td>
<td>WO</td>
<td>xxh</td>
<td>Extend for Z Format Transformation</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Do nothing. For Z with 32-bit floating s[8],23 and mantissa as 1.Z[22:0],it will be extended to 1.{Z[22:0], 8’h00} and transformed to fixed-format.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Extend mantissa to 32 bits before format transformation. Consider Z with 32-bit floating s[8],23 and mantissa as 1.Z[22:0], it will be extended to 1.Z[22:0], 1'b1, Z[22:16] and transformed to fixed format.</td>
</tr>
<tr>
<td>0</td>
<td>WO</td>
<td>xxh</td>
<td>Memory Mode of ZW Buffer</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Linear mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Tile mode</td>
</tr>
</tbody>
</table>
### HParaType = 01h, Sub-Address = 13h

#### Z Setting 4

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 23          | WO        | xxh     | Source Z is Generated by Pixel Shader Instead of Shading \( \langle HZSrcPS \rangle \)  
1: Source Z is generated in PS, RZ module should pipe the Zdst to PE. The Zdst and Zsrc for depth test come from BE. |
| 22:19       | WO        | xxh     | ZW Test Mode \( \langle HZWTMOD \rangle \)  
000: Z or W test never pass  
001: Z or W test pass if Znew < Zdst  
010: Z or W test pass if Znew = Zdst  
011: Z or W test pass if Znew ≤ Zdst  
100: Z or W test pass if Znew > Zdst  
101: Z or W test pass if Znew ≠ Zdst  
110: Z or W test pass if Znew ≥ Zdst  
111: Z or W test always pass  
Where Znew is the calculated Z value and Zdst is the Z stored in the Z buffer. |
| 15:8        | WO        | xxh     | Reserved |
| 7:0         | WO        | xxh     | Z Normalization Factor  
The range is from 0 to 255. By definition, Z can be divided by a value of power of 2. Thus, it allows the input Z free from the constrain of Z < 1.  
Z Normalization is Z = Zin / 2^{HZNF} |

### HParaType = 01h, Sub-Address = 14h

#### Z Setting 5

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:0</td>
<td>WO</td>
<td>xxh</td>
<td>Lower 3 Bytes of ZW Clear Data</td>
</tr>
</tbody>
</table>

### HParaType = 01h, Sub-Address = 15h

#### Z Setting 6

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 23:8        | WO        | xxh     | Negative of Mask to the Zsrc’s Last 16-bit Mantissa  
Note that this mask is just implemented to the rendered Z value for format transformation, then a Z test is conducted and wrote-back to Z buffer.  
Consider the generated Z value “Zsrc[31:0]” with floating s[8:23]:  
Step1: Zsrc[15:0] = Zsrc[15:0] & ~HZWMMSK_N[15:0]  
Step2: Format transform Zsrc according to HZWFM  
Step3: Z test  
Step4: Updated Z buffer with the format transformed Zsrc if Z test is passed |
| 7:0         | WO        | xxh     | Highest Byte of ZW Clear Data |

### HParaType = 01h, Sub-Address = 16h

#### Z Setting 7

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 23:0        | WO        | xxh     | Lower 3 Bytes of Z Bias Offset  
With 32-bit floating format, since Z format transformation is between fixed and floating, and HZBiasOffset description is suggested to be modified as below:  
If (HZWBFM == 32-bit fixed)  
\[ HZBiasOffset = HZBiasOffset * (2^{32} - 1) / 2^{32} \]  
Else if (HZWBFM == 24-bit fixed)  
\[ HZBiasOffset = HZBiasOffset * (2^{24} - 1) / 2^{24} \]  
Else if (HZWBFM == 16-bit fixed)  
\[ HZBiasOffset = HZBiasOffset * (2^{16} - 1) / 2^{16} \]
**HParaType = 01h, Sub-Address = 17h**

**Z Setting 8**

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[23:0]</td>
<td>WO</td>
<td>xxh</td>
<td><strong>Bias Scale with 32-bit Floating Format</strong></td>
</tr>
<tr>
<td>23:16</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>15:8</td>
<td></td>
<td></td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>7:0</td>
<td>WO</td>
<td>xxh</td>
<td><strong>Highest Byte of Z Bias Offset</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$SEZbias = \max(Zdx, Zdy) \times HZBiasScale + HZBias Offset$</td>
</tr>
</tbody>
</table>

**HParaType = 01h, Sub-Address = 18h**

**Z Setting 9**

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[23:0]</td>
<td>WO</td>
<td>xxh</td>
<td><strong>Z Bias Scale With 32-bit Floating Format</strong></td>
</tr>
<tr>
<td>23:0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**HParaType = 01h, Sub-Address = 19h**

**Z Setting 10**

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[23:0]</td>
<td>WO</td>
<td>xxh</td>
<td><strong>Low 23 Bits of Low Boundary to Clamp the Z Bias</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>With format of 32-bit floating.</td>
</tr>
<tr>
<td>23:0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**HParaType = 01h, Sub-Address = 1Ah**

**Z Setting 11**

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[23:0]</td>
<td>WO</td>
<td>xxh</td>
<td><strong>Low 23 Bits of High Boundary to Clamp the Z Bias</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>With format of 32-bit floating.</td>
</tr>
<tr>
<td>23:0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**HParaType = 01h, Sub-Address = 1Bh**

**Z Setting 12**

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[23:0]</td>
<td>WO</td>
<td>xxh</td>
<td><strong>Enhance Z’s Precision During PE Rendering</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td>23:16</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>22:16</td>
<td>WO</td>
<td>xxh</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>15:8</td>
<td>WO</td>
<td>xxh</td>
<td><strong>High 8 Bits of High Boundary to Clamp the Z Bias</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>With format of 32-bit floating.</td>
</tr>
<tr>
<td>7:0</td>
<td>WO</td>
<td>xxh</td>
<td><strong>High 8 Bits of Low Boundary to Clamp the Z Bias</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>With format of 32-bit floating.</td>
</tr>
</tbody>
</table>

**HParaType = 01h, Sub-Address = 1Ch**

**Z Setting 13**

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[23:0]</td>
<td>WO</td>
<td>xxh</td>
<td><strong>Low 24 Bits Occlusion Count of both Z Test and Stencil Test Result</strong></td>
</tr>
<tr>
<td>23:0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**HParaType = 01h, Sub-Address = 1Dh**

**Z Setting 14**

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[23:0]</td>
<td>WO</td>
<td>xxh</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>23:8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7:0</td>
<td>WO</td>
<td>xxh</td>
<td><strong>High 8 Bits Occlusion Count of Both Z Test and Stencil Test Result</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### HParaType = 01h, Sub-Address = 1Eh

#### Z Setting 15

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[23:0]</td>
<td>WO</td>
<td>xxh</td>
<td>Lower 24 Bits of Clip Plane’s Far Value</td>
</tr>
</tbody>
</table>

### HParaType = 01h, Sub-Address = 1Fh

#### Z Setting 16

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[23:0]</td>
<td>WO</td>
<td>xxh</td>
<td>Lower 24 Bits of Clip Plane’s Near Value</td>
</tr>
</tbody>
</table>

### HParaType = 01h, Sub-Address = 20h

#### Z Setting 17

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[23:16]</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>15:8</td>
<td>WO</td>
<td>xxh</td>
<td>Higher 8 Bits of Clip Plane’s Far Value With format of 32-bit floating.</td>
</tr>
<tr>
<td>7:0</td>
<td>WO</td>
<td>xxh</td>
<td>Higher 8 Bits of Clip Plane’s Near Value With format of 32-bit floating. Check each pixel’s Z value before depth testing, and remove this pixel if it’s out of the range. If ( Z &gt; ) HZClipFar</td>
</tr>
</tbody>
</table>

### HParaType = 01h, Sub-Address = 21h

#### Z Setting 18

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[23:0]</td>
<td>WO</td>
<td>xxh</td>
<td>Low 24 Bits of Video Memory Address to Address to Write the “HZOcclusionCNT” (&lt;HZOcclusionAdrL&gt;) in a unit of 4 bytes. Note for Driver: Whenever a non-zero value is set to this register, the “HZOcclusionCNT” would be written back to the video memory with the address of “HZOcclusionAdr”. Since the address is separated into 2 sub-addresses, please set driver “HZOcclusionAdrL” and then “HZOcclusionAdrH” in order. Whenever decoding the “HZOcclusionAdrH”, hardware would check if the address (HZOcclusionAdrH and HZOcclusionAdrL cascaded) is zero or not.</td>
</tr>
</tbody>
</table>

### HParaType = 01h, Sub-Address = 22h

#### Z Setting 19

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[23:22]</td>
<td>WO</td>
<td>xxh</td>
<td>Location Setting of Z Occlusion Counter (HZOcclusionCNT) 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: Reserved (System Memory) 11: Reserved</td>
</tr>
<tr>
<td>21:8</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>7:0</td>
<td>WO</td>
<td>xxh</td>
<td>High 8 Bits of Video Memory Address to Address (&lt;HZOcclusionAdrH&gt;) For writing the “HZOcclusionCNT”, in the unit of 4 bytes.</td>
</tr>
</tbody>
</table>
### HPARA = 01h, Sub-Address = 23h

#### Stencil Setting 1

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 23:16       | WO        | xxh    | Stencil Test Reference Value for Clock-Wise Face \(<HSTCWREF>\)  
This value is a positive 8-bit fixed point number with range from 0 to 255, which is used for Stencil Test as the comparison result between Stencil and HSTCWREF. |
| 15:8        | WO        | xxh    | Stencil Test Operation Mask for Clock-Wise Face \(<HSTCWOPMSK>\)  
Indicates the comparison result between (Stencil & HSTCWOPMSK) and (HSTCWREF & HSTCWBMKS). |
| 7:0         | WO        | xxh    | Stencil Buffer Bit Mask for Clock-Wise Face \(<HSTCWBMKS>\)  
If this bit = 0, the corresponding bit in the stencil buffer cannot be changed. Otherwise, it can be changed. |

### HPARA = 01h, Sub-Address = 24h

#### Stencil Setting 2

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:19</td>
<td>WO</td>
<td>x</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 18:16       | WO        | xxh    | Stencil Test Mode for Clock-Wise Face  
000: Stencil Test never pass  
001: Stencil Test pass if (HSTCWREF & HSTCWOPMSK) < (Stencil & HSTCWOPMSK)  
010: Stencil Test pass if (HSTCWREF & HSTCWOPMSK) = (Stencil & HSTCWOPMSK)  
011: Stencil Test pass if (HSTCWREF & HSTCWOPMSK) ≤ (Stencil & HSTCWOPMSK)  
100: Stencil Test pass if (HSTCWREF & HSTCWOPMSK) > (Stencil & HSTCWOPMSK)  
101: Stencil Test pass if (HSTCWREF & HSTCWOPMSK) ≠ (Stencil & HSTCWOPMSK)  
110: Stencil Test pass if (HSTCWREF & HSTCWOPMSK) ≥ (Stencil & HSTCWOPMSK)  
111: Stencil Test always pass |
| 8:6         | WO        | xxh    | Reserved |
| 5:3         | WO        | xxh    | Stencil Operation for Stencil Test Fail for Clock-Wise Face  
000: KEEP  
001: ZERO  
010: REPLACE  
011: INCRSAT  
100: DECRSAT  
101: INVERT  
110: INCR  
111: DECR |
| 2:0         | WO        | xxh    | Stencil Operation for Stencil Test Pass and Z Test Fail for Clock-Wise Face  
000: KEEP  
001: ZERO  
010: REPLACE  
011: INCRSAT  
100: DECRSAT  
101: INVERT  
110: INCR  
111: DECR |
### HParaType = 01h, Sub-Address = 25h

#### Stencil Setting 3

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 23:16       | WO        | xxh     | **Stencil Test Reference Value for Counter-Clock-Wise Face** \(<\text{HSTCCWREF}>\)  
This value is a positive 8-bit fixed point number with range from 0 to 255, which is used for Stencil Test as the comparison result between Stencil and HSTCCWREF. |
| 15:8        | WO        | xxh     | **Stencil Test Operation Mask for Counter-Clock-Wise Face** \(<\text{HSTCCWOPMSK}>\)  
Indicates the comparison result between (Stencil \& HSTCCWOPMSK) and (HSTCCWREF \& HSTCCWBMSK). |
| 7:0         | WO        | xxh     | **Stencil Buffer Bit Mask for Counter-Clock-Wise Face** \(<\text{HSTCCWBMSK}>\)  
If this bit = 0, the corresponding bit in the stencil buffer cannot be changed. Otherwise, it can be changed. |

---

### HParaType = 01h, Sub-Address = 26h

#### Stencil Setting 4

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:19</td>
<td>WO</td>
<td>xxh</td>
<td><strong>Reserved</strong></td>
</tr>
</tbody>
</table>
| 18:16       | WO        | xxh     | **Stencil Test Mode for Counter-Clock-Wise Face**  
000: Stencil Test never pass  
001: Stencil Test pass if (HSTCCWREF \& HSTCCWOPMSK) < (Stencil \& HSTCCWOPMSK)  
010: Stencil Test pass if (HSTCCWREF \& HSTCCWOPMSK) = (Stencil \& HSTCCWOPMSK)  
011: Stencil Test pass if (HSTCCWREF \& HSTCCWOPMSK) \(\leq\) (Stencil \& HSTCCWOPMSK)  
100: Stencil Test pass if (HSTCCWREF \& HSTCCWOPMSK) > (Stencil \& HSTCCWOPMSK)  
101: Stencil Test pass if (HSTCCWREF \& HSTCCWOPMSK) \(\neq\) (Stencil \& HSTCCWOPMSK)  
110: Stencil Test pass if (HSTCCWREF \& HSTCCWOPMSK) \(\geq\) (Stencil \& HSTCCWOPMSK)  
111: Stencil Test always pass |
| 15:9        | WO        | xxh     | **Reserved** |
| 8:6         | WO        | xxh     | **Stencil Operation for Stencil Test Fail for Counter-Clock-Wise Face**  
000: KEEP  
001: ZERO  
010: REPLACE  
011: INCRSAT  
100: DECRSAT  
101: INVERT  
110: INCR  
111: DECR |
| 5:3         | WO        | xxh     | **Stencil Operation for Stencil Test Pass and Z Test Fail for Counter-Clock-Wise Face**  
000: KEEP  
001: ZERO  
010: REPLACE  
011: INCRSAT  
100: DECRSAT  
101: INVERT  
110: INCR  
111: DECR |
| 2:0         | WO        | xxh     | **Stencil Operation for Stencil Test Pass and Z Test Pass for Counter-Clock-Wise Face**  
000: KEEP  
001: ZERO  
010: REPLACE  
011: INCRSAT  
100: DECRSAT  
101: INVERT  
110: INCR  
111: DECR |
**HParaType = 01h, Sub-Address = 27h**

**Setting for Fast-Z-Clear 1**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:16</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>15:8</td>
<td>WO</td>
<td>xxh</td>
<td>Index of ZW Buffer for Current Scene</td>
</tr>
<tr>
<td>11:8</td>
<td>WO</td>
<td>xxh</td>
<td>Length of HZWBIdx in Unit of Bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0000: Disable ZW buffer index</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0001: Use the LSB 1 bit as ZW buffer index</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0010: Use the LSB 2 bits as ZW buffer index</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0011: Use the LSB 3 bits as ZW buffer index</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0100: Use the LSB 4 bits as ZW buffer index</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1111 ~ 0101: Reserved</td>
</tr>
<tr>
<td>7:1</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>0</td>
<td>WO</td>
<td>xxh</td>
<td>Enable Fast-Z-Clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable</td>
</tr>
</tbody>
</table>

**HParaType = 01h, Sub-Address = 28h**

**Setting for Fast-Z-Clear 2**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:0</td>
<td>WO</td>
<td>xxh</td>
<td>Stencil Buffer’s Base Address &lt;HSTBas&gt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>In unit of 256 bytes. The pitch of the separated stencil buffer is just the setting of the Z buffer pitch. Since there is only Z24S8 format for the stencil value, the Z must be 32 bpp wen separated stencil buffer is enabled. No matter Z buffer is in linear or tile mode, the HZWBPit is just (W+7) &gt;&gt; 3, where W is the screen coordinate. E3R(W)STADR = HSTBas*256 + Y[10:3]<em>HZWBPit</em>64 + X[10:3]*64 + Y[2:1]*16</td>
</tr>
</tbody>
</table>

**HParaType = 01h, Sub-Address = 29h**

**Setting for Coarse Z Test Function 1**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23</td>
<td>WO</td>
<td>xxh</td>
<td>Force CZ Retest If Original Is “Reject” and the Related Primitive Is Clock-Wise</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Force the CZ result as “ReTEST” if original is “REJECT” and the related primitive is Clock-Wise.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Normal CZ test</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Never reject</td>
</tr>
<tr>
<td>22</td>
<td>WO</td>
<td>xxh</td>
<td>Force CZ Retest If Original Is “Pass” and the Related Primitive Is Clock-Wise</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Force the CZ result as “ReTEST” if original is “Pass” and the related primitive is Clock-Wise.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Normal CZ test</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Never pass</td>
</tr>
<tr>
<td>21:20</td>
<td>WO</td>
<td>xxh</td>
<td>Coarse Z Buffer Location Setting</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: System Local Frame Buffer (S.L.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: System Dynamic Frame Buffer (S.F.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: Reserved (System Memory)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: Reserved</td>
</tr>
<tr>
<td>19:18</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>17</td>
<td>WO</td>
<td>xxh</td>
<td>Inverse Mode for CZ Test</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Smaller Z value as nearer and larger Z value as farer, for HZWTMD is LESS or LESSEQUAL</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Larger Z value as nearer and smaller Z value as farer, for HZWTMD is GREATER or GREATEREQUAL</td>
</tr>
<tr>
<td>16</td>
<td>WO</td>
<td>xxh</td>
<td>Coarse Z Write Back Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Whenever the CZTAG_CNT is “0” and CZTAG.UPDATED, write the CZ in cache back to video memory</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Whenever the cell is selected for new CZ value and CZTAG.UPDATED, write the old CZ in cache back to video memory, and then read the new CZ value.</td>
</tr>
<tr>
<td>15</td>
<td>WO</td>
<td>xxh</td>
<td>Reset of CZ Cache’s TAG</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Instead of having software to clear this setting, it would be auto-cleared by hardware.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Normal</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Rest</td>
</tr>
<tr>
<td>14</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>13:12</td>
<td>WO</td>
<td>xxh</td>
<td>Coarse Z Test by Using Conservative Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: Use optimized merging rule</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: Use Conservative Merging Rule and only update both “MIN” value and “MAX” value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: Use Conservative Merging Rule and only update “MIN” value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: Reserved</td>
</tr>
<tr>
<td>WO xxh</td>
<td>11</td>
<td>Force CZ Retest If Original Is “Reject” and the Related Primitive Is Counter-Clock-Wise</td>
<td></td>
</tr>
<tr>
<td>--------</td>
<td>----</td>
<td>--------------------------------------------------------------------------------</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Force the CZ result as “ReTEST” if original is “REJECT” and the related primitive is Counter-Clock-Wise.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: Normal CZ test</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Never reject</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>WO xxh</th>
<th>10</th>
<th>Force CZ Retest If Original Is “Pass” and the Related Primitive Is Counter-Clock-Wise</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Force the CZ result as “ReTEST” if original is “REJECT” and the related primitive is Counter-Clock-Wise.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: Normal CZ test</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Never reject</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>WO xxh</th>
<th>9</th>
<th>Force ReTest as the Result of HZ Test</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>0: Normal</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Force</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>WO xxh</th>
<th>8:0</th>
<th>Coarse Z Buffer’s Pitch</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>In unit of 32 bytes.</td>
</tr>
</tbody>
</table>

### HPareType = 01h, Sub-Address = 2Ah

Setting for Coarse Z Test Function 2

<table>
<thead>
<tr>
<th>Bits [23:0] Attribute Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:0 WO xxh</td>
<td>Coarse Z Buffer’s Base Address</td>
</tr>
<tr>
<td></td>
<td>In unit of 256 bytes.</td>
</tr>
<tr>
<td></td>
<td>E3R(W)CZADR = HCZBas<em>256 + Y</em>HCZPit<em>32 + (2</em>X)*16</td>
</tr>
</tbody>
</table>

### HPareType = 01h, Sub-Address = 33h

Alpha Setting 1

<table>
<thead>
<tr>
<th>Bits [23:0] Attribute Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:15 WO xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>14:12 WO xxh</td>
<td>Alpha Test Mode</td>
</tr>
<tr>
<td></td>
<td>000: Alpha test never pass</td>
</tr>
<tr>
<td></td>
<td>001: Alpha test pass if Anew &lt; HATREF (bits [10:0])</td>
</tr>
<tr>
<td></td>
<td>010: Alpha test pass if Anew = HATREF</td>
</tr>
<tr>
<td></td>
<td>011: Alpha test pass if Anew ≤ HATREF</td>
</tr>
<tr>
<td></td>
<td>100: Alpha test pass if Anew &gt; HATREF</td>
</tr>
<tr>
<td></td>
<td>101: Alpha test pass if Anew ≠ HATREF</td>
</tr>
<tr>
<td></td>
<td>110: Alpha test pass if Anew ≥ HATREF</td>
</tr>
<tr>
<td></td>
<td>111: Alpha test always pass</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>WO xxh</th>
<th>11</th>
<th>Reserved</th>
</tr>
</thead>
<tbody>
<tr>
<td>10:0   WO xxh</td>
<td>Alpha Test Reference Value &lt;HATREF&gt;</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Positive fixed-point from 0.0 to 1.0.</td>
</tr>
</tbody>
</table>
**HPaType = 01h, Sub-Address = 34h**

**Alpha Setting 2**

*Alpha Blending Equation of RGB:*

Equation of RGB: \(\text{Cout} = ((\text{AB}_{\text{FCa}} \times \text{AB}_{\text{Ca}}) \text{AB}_{\text{Cop}} (\text{AB}_{\text{FCb}} \times \text{AB}_{\text{Cb}}))\)

If (HABLCsat = false) Clamp Cout to 1.0 to 0.0

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:17</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 16          | WO        | xxh     | RGB Saturation Control of Alpha Blending Calculation \(\text{<HABLCsat>}\)

0: Cout will be clamp to 0.0 ~ 1.0
1: Cout will not be clamp to 0.0 ~ 1.0

<table>
<thead>
<tr>
<th>15:10</th>
<th>WO</th>
<th>xxh</th>
<th>Ca of Alpha Blending Equation (\text{&lt;HABLCA&gt;})</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bits [9:4]</td>
<td>Attribute</td>
<td>Default</td>
<td>Description</td>
</tr>
<tr>
<td>9:4</td>
<td>WO</td>
<td>xxh</td>
<td>FCa of Alpha Blending Equation (\text{&lt;HABLFCa&gt;})</td>
</tr>
<tr>
<td>Bits [3:0]</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

**Table:**

<table>
<thead>
<tr>
<th>Bits [3:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3:0</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
### Alpha Setting 3

**HParaType = 01h, Sub-Address = 35h**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:16</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>15:14</td>
<td>WO</td>
<td>xxh</td>
<td>Cop of Alpha Blending Equation &lt;HABL Cop&gt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>HABL Cop</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Cop</td>
</tr>
<tr>
<td></td>
<td></td>
<td>00</td>
<td>+</td>
</tr>
<tr>
<td></td>
<td></td>
<td>01</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10</td>
<td>Max</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11</td>
<td>Min</td>
</tr>
<tr>
<td>13:8</td>
<td>WO</td>
<td>xxh</td>
<td>Cb of Alpha Blending Equation &lt;HABL Cb&gt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>HABL Cb[3:0]</td>
</tr>
<tr>
<td></td>
<td></td>
<td>R of OP Cb</td>
<td>G of OP Cb</td>
</tr>
<tr>
<td>0000</td>
<td>Rsrc</td>
<td>Gsrc</td>
<td>Bsrc</td>
</tr>
<tr>
<td>0001</td>
<td>Rdst</td>
<td>Gdst</td>
<td>Bdst</td>
</tr>
<tr>
<td>0101</td>
<td>R of HABL R Cb</td>
<td>G of HABL R Cb</td>
<td>B of HABL R Cb</td>
</tr>
<tr>
<td>7:2</td>
<td>WO</td>
<td>xxh</td>
<td>Fcb of Alpha Blending Equation &lt;HABL FCb&gt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>HABL FCb[5:4]</td>
</tr>
<tr>
<td></td>
<td></td>
<td>R of AB FCb</td>
<td>G of AB FCb</td>
</tr>
<tr>
<td>00</td>
<td>R of OPF Cb</td>
<td>G of OPF Cb</td>
<td>B of OPF Cb</td>
</tr>
<tr>
<td>01</td>
<td>1.0 - (R of OPF Cb)</td>
<td>1.0 - (G of OPF Cb)</td>
<td>1.0 - (B of OPF Cb)</td>
</tr>
<tr>
<td>0000</td>
<td>Rsrc</td>
<td>Gsrc</td>
<td>Bsrc</td>
</tr>
<tr>
<td>0001</td>
<td>Rdst</td>
<td>Gdst</td>
<td>Bdst</td>
</tr>
<tr>
<td>0010</td>
<td>Asrc</td>
<td>Asrc</td>
<td>Asrc</td>
</tr>
<tr>
<td>0011</td>
<td>Adst</td>
<td>Adst</td>
<td>Adst</td>
</tr>
<tr>
<td>0101</td>
<td>R of HABL RF Cb</td>
<td>G of HABL RF Cb</td>
<td>B of HABL RF Cb</td>
</tr>
<tr>
<td>1000</td>
<td>min (Asrc, 1-Adst)</td>
<td>min (Asrc, 1-Adst)</td>
<td>min (Asrc, 1-Adst)</td>
</tr>
<tr>
<td>1:0</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
HParaType = 01h, Sub-Address = 36h

### Alpha Setting 4

**Equation of A:**
\[ \text{Aout} = ((\text{AB\_FAa} \times \text{AB\_Aa}) \text{AB\_Aop} (\text{AB\_FAb} \times \text{AB\_Ab})) \]

If (HABLAsat = false) Clamp Aout to 1.0 to 0.0

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:17</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 16          | WO        | xxh     | Alpha Saturation Control of Alpha Blending Calculation \(<HABLAsat>\)  
0: Aout will be clamped to 0.0 ~ 1.0  
1: Aout will not be clamped to 0.0 ~ 1.0 |
| 15:10       | WO        | xxh     | Aa of Alpha Blending Equation \(<HABLAAa>\)  
HABLAa[5:4] AB Aa  
xx Reserved |
| 9:4         | WO        | xxh     | FAa of Alpha Blending Equation \(<HABLFAa>\)  
HABLFAa[5:4] AB FAa  
0 OPFAa  
1 \(1 - \text{OPFAa}\)  
11 Reserved |
| 3:0         | WO        | xxh     | Reserved    |
### HParaType = 01h, Sub-Address = 37h
#### Alpha Setting 5

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[23:0]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>23:16</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>15:14</td>
<td>WO</td>
<td>xxh</td>
<td><strong>Aop of Alpha Blending Equation</strong> &lt;HABL_Aop&gt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><strong>HABL_Aop</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><strong>AB_Aop</strong></td>
</tr>
<tr>
<td>00</td>
<td>+</td>
<td></td>
<td></td>
</tr>
<tr>
<td>01</td>
<td>-</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>Max</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>Min</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| 13:8  | WO        | xxh     | **Ab of Alpha Blending Equation** <HABL_Ab> |
|       |           |         |                              |
|       |           |         | **HABL_Ab**                   |
|       |           |         | **AB_Ab**                     |
| [5:4] | Reserved  |         |                              |

| 7:2   | WO        | xxh     | **Fab of Alpha Blending Equation** <HABL_Fab> |
|       |           |         |                              |
|       |           |         | **HABL_Fab**                  |
| [5:4] | OPFab     |         |                              |
| 00    | OPFab     |         |                              |
| 01    | 1 – OPFab |         |                              |

| 1:0   | WO        | xxh     | Reserved                     |

### HParaType = 01h, Sub-Address = 38h
#### Alpha Setting 6

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[23:0]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>22:12</td>
<td>WO</td>
<td>xxh</td>
<td><strong>G of HABLRCa</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This is an 11-bit positive fixed-point number from 0.0 to 1.0.</td>
</tr>
<tr>
<td>11</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>10:0</td>
<td>WO</td>
<td>xxh</td>
<td><strong>B of HABLRCa</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This is an 11-bit positive fixed-point number from 0.0 to 1.0.</td>
</tr>
</tbody>
</table>

### HParaType = 01h, Sub-Address = 39h
#### Alpha Setting 7

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[23:0]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>22:12</td>
<td>WO</td>
<td>xxh</td>
<td><strong>R of HABLRFca</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This is an 11-bit positive fixed-point number from 0.0 to 1.0.</td>
</tr>
<tr>
<td>11</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>10:0</td>
<td>WO</td>
<td>xxh</td>
<td><strong>R of HABLRCa</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This is an 11-bit positive fixed-point number from 0.0 to 1.0.</td>
</tr>
</tbody>
</table>
### HParaType = 01h, Sub-Address = 3Ah
#### Alpha Setting 8

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 22:12       | WO        | xxh     | G of HABLRFCa  
This is an 11-bit positive fixed-point number from 0.0 to 1.0. |
| 11          | WO        | xxh     | Reserved    |
| 10:0        | WO        | xxh     | B of HABLRFCa  
This is an 11-bit positive fixed-point number from 0.0 to 1.0. |

### HParaType = 01h, Sub-Address = 3Bh
#### Alpha Setting 9

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 22:12       | WO        | xxh     | G of HABLRCb  
This is an 11-bit positive fixed-point number from 0.0 to 1.0. |
| 11          | WO        | xxh     | Reserved    |
| 10:0        | WO        | xxh     | B of HABLRCb  
This is an 11-bit positive fixed-point number from 0.0 to 1.0. |

### HParaType = 01h, Sub-Address = 3Ch
#### Alpha Setting 10

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 22:12       | WO        | xxh     | R of HABLRFb  
This is an 11-bit positive fixed-point number from 0.0 to 1.0. |
| 11          | WO        | xxh     | Reserved    |
| 10:0        | WO        | xxh     | R of HABLRCb  
This is an 11-bit positive fixed-point number from 0.0 to 1.0. |

### HParaType = 01h, Sub-Address = 3Dh
#### Alpha Setting 11

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 22:12       | WO        | xxh     | G of HABLRFb  
This is an 11-bit positive fixed-point number from 0.0 to 1.0. |
| 11          | WO        | xxh     | Reserved    |
| 10:0        | WO        | xxh     | B of HABLRFb  
This is an 11-bit positive fixed-point number from 0.0 to 1.0. |

### HParaType = 01h, Sub-Address = 3Eh
#### Alpha Setting 12

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 22:12       | WO        | xxh     | Constant Register of Aa  
This is an 11-bit positive fixed-point number from 0.0 to 1.0. |
| 11          | WO        | xxh     | Reserved    |
| 10:0        | WO        | xxh     | Constant Register of FAa  
<\text{HABLRF}Aa>  
This is an 11-bit positive fixed-point number from 0.0 to 1.0. |
### HParaType = 01h, Sub-Address = 3Fh
#### Alpha Setting 13

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[23:0]</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>22:12</td>
<td>WO</td>
<td>xxh</td>
<td>Constant Register of Ab &lt;HABLRAb&gt; This is an 11-bit positive fixed-point number from 0.0 to 1.0.</td>
</tr>
<tr>
<td>11</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>10:0</td>
<td>WO</td>
<td>xxh</td>
<td>Constant Register of FAb &lt;HABLRFAb&gt; This is an 11-bit positive fixed-point number from 0.0 to 1.0.</td>
</tr>
</tbody>
</table>

### HParaType = 01h, Sub-Address 40–4Fh: Reserved (for Alpha Setting)

### HParaType = 01h, Sub-Address = 50h
#### Destination Setting – Render Target 0 – Setting 1

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:0</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target0's Base Address In unit of 256 bytes.</td>
</tr>
</tbody>
</table>

### HParaType = 01h, Sub-Address = 51h
#### Destination Setting – Render Target 0 – Setting 2

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23</td>
<td>WO</td>
<td>xxh</td>
<td>Memory Mode of Render Target 0 0: Linear mode 1: Tile mode</td>
</tr>
<tr>
<td>22</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target0's Tile Is 16-pixel High &lt;HMRT0TileH16&gt; 0: Normal 8-pixel high 1: 16-pixel high</td>
</tr>
<tr>
<td>21:20</td>
<td>WO</td>
<td>xxh</td>
<td>Location Setting of Render Target 0 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: Reserved (System Memory) 11: Reserved</td>
</tr>
<tr>
<td>19:0</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
### Destination Setting – Render Target 0 – Setting 3

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:16</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target 0’s Format</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><strong>For Bit [23:19]:</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00000: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00001: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00010: Luminance format</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00011: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00100: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00101: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00110: YUV (Video Texture) format</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00111-10000: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10001: ARGB 16bpp format</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10010: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10011: ARGB 32bpp format</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10100: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10101: ABGR 16bpp format</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10110: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10111: ABGR 32bpp format</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11000: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11001: RGBA 16bpp format</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11010: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11011: RGBA 32bpp format</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11100: BGRA 16bpp format</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11101: BGRA 32bpp format</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11110: Floating Color format</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11111: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><strong>If there is NO Alpha channel in the defined format, fill 1.0 as Alpha value.</strong></td>
</tr>
</tbody>
</table>

**For Bit [18:16]:**

**For Luminance Format:**

000-100: Reserved
101: AL88 (Bits [15:8] = A, Bits [7:0] = L)
110: L16 (Bits [15:0] = L) For L16 format, post-rendering must be disabled.
111: Reserved

**For YUV Format (Video Texture):**

Others: Reserved

**For reading color,** consider the 8-bit Y as positive 8-bit G, 8-bit U as positive 8-bit R, and 8-bit V as positive 8-bit B. Then extend them to s1.10 according to setting of **Color Extending Mode** (see bit 15).

**For writing color,** the adjacent 2 pixels are combined into 32 bits and share same 8-bit U and V. Consider an even pixel with R0, G0 & B0 (dithered 8-bit color), and the next odd pixel with R1, G1 & B1 (dithered 8-bit color), the packed result is \((B0 + B1)/2, G1, (R0+R1)/2, G0\). Note the \((B0+B1)/2\) and \((R0+R1)/2\) are the result of rounding.

**For ARGB 16bpp Format:**

100: Reserved
11x: Reserved

**For ARGB 32bpp Format:**

011-1xx: Reserved

**For ABGR 16bpp Format:**

11x: Reserved

For ABGR 32bpp Format:
1xx: Reserved

For RGBA 16bpp Format:
100: Reserved
11x: Reserved

For RGBA 32bpp Format:
011-1xx: Reserved

For BGRA 16bpp Format:
100: Reserved
11x: Reserved

For BGRA 32bpp Format:
011-1xx: Reserved

For Floating Color Format:
000: R16F (Bits [15:0] = R)
101: R32F (Bits [31:0] = R)
For floating color format, post-rendering must be disabled.
Color Extending Mode (Excluding Alpha)

0: Extending with high color bit
Translate to 1.10 format.

10 => 11
\[ C_{11} = C_{10} \times \frac{1024}{1023} = C_{10} + \frac{1}{1023} \times C_{10} \]
\[ C_{10} < 1023, \quad C_{11} = 0.xxxxxxxxxx(C_{10}) \]
\[ C_{10} = 1023, \quad C_{11} = 1.0000000000 \]

8 => 11
\[ C_{11} = C_{8} \times \frac{1024}{255} = 4\times C_{8} + \frac{4}{255}\times C_{8} \]
\[ C_{8} < 64, \quad C_{11} = 0.C_{8}00 \]
\[ 64 \leq C_{8} < 128, \quad C_{11} = 0.C_{8}01 \]
\[ 128 \leq C_{8} < 192, \quad C_{11} = 0.C_{8}10 \]
\[ 192 \leq C_{8} < 255, \quad C_{11} = 0.C_{8}11 \]
\[ C_{8} = 255, \quad C_{11} = 1.0000000000 \]

6 => 11
\[ C_{11} = C_{6} \times \frac{1024}{63} = 16\times C_{6} + \frac{16}{63}\times C_{6} \]
\[ C_{6} < 4, \quad C_{11} = 0.C_{6}0000 \]
\[ 4 \leq C_{6} < 8, \quad C_{11} = 0.C_{6}0001 \]
\[ 8 \leq C_{6} < 12, \quad C_{11} = 0.C_{6}0010 \]
\[ 12 \leq C_{6} < 16, \quad C_{11} = 0.C_{6}0011 \]
\[ 16 \leq C_{6} < 20, \quad C_{11} = 0.C_{6}0100 \]
\[ 20 \leq C_{6} < 24, \quad C_{11} = 0.C_{6}0101 \]
\[ 24 \leq C_{6} < 28, \quad C_{11} = 0.C_{6}0110 \]
\[ 28 \leq C_{6} < 32, \quad C_{11} = 0.C_{6}0111 \]
\[ 32 \leq C_{6} < 36, \quad C_{11} = 0.C_{6}1000 \]
\[ 36 \leq C_{6} < 40, \quad C_{11} = 0.C_{6}1001 \]
\[ 40 \leq C_{6} < 44, \quad C_{11} = 0.C_{6}1010 \]
\[ 44 \leq C_{6} < 48, \quad C_{11} = 0.C_{6}1011 \]
\[ 48 \leq C_{6} < 52, \quad C_{11} = 0.C_{6}1100 \]
\[ 52 \leq C_{6} < 56, \quad C_{11} = 0.C_{6}1101 \]
\[ 56 \leq C_{6} < 60, \quad C_{11} = 0.C_{6}1110 \]
\[ 60 \leq C_{6} < 63, \quad C_{11} = 0.C_{6}1111 \]
\[ C_{6} = 63, \quad C_{11} = 1.0000000000 \]

5 => 11
\[ C_{11} = C_{5} \times \frac{1024}{31} = 33\times C_{5} + \frac{32}{31}\times C_{5} \]
\[ C_{5} < 31, \quad C_{11} = 0.C_{5}C_{5} \]
\[ C_{5} = 31, \quad C_{11} = 1.0000000000 \]

4 => 11
\[ C_{11} = C_{4} \times \frac{1024}{15} = 68\times C_{4} + \frac{4}{15}\times C_{4} \]
\[ C_{4} < 4, \quad C_{11} = 0.C_{4}00 \]
\[ 4 \leq C_{4} < 8, \quad C_{11} = 0.C_{4}01 \]
\[ 8 \leq C_{4} < 12, \quad C_{11} = 0.C_{4}10 \]
\[ 12 \leq C_{4} < 15, \quad C_{11} = 0.C_{4}11 \]
\[ C_{4} = 15, \quad C_{11} = 1.0000000000 \]

1: Extending with zero
Considering 6=>11 as example: C11 = 0. C0000

Saturation of PS’s Output for Render Target “M”

0: Clamp PS’s output color oCm to related render tager format’s range
For format ARGB and Luminance: MINVALUE = 0.0, MAXVALUE = 1.0.
For 16-bit floating color format: MINVALUE = 16’hFBFF, MAXVALUE = 16’h7BFF.
For 32-bit floating color format: MINVALUE = 32’h7F7FFFFF, MAXVALUE = 32’hFF7FFFFF.
Clamped Value = min(MAXVALUE, max(oCm, MINVALUE))
Note if oCm is “Nan”, clamped value is MINVALUE.
1: oCm doesn’t clamp
### HParaType = 01h, Sub-Address = 53h
#### Destination Setting – Render Target 0 – Setting 4

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target0’s Y Inverse for Dither</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Not inverse</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Inverse</td>
</tr>
<tr>
<td>22:21</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target0’s Y Bias for Dither</td>
</tr>
<tr>
<td>20</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target0’s X Inverse for Dither</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Not inverse</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Inverse</td>
</tr>
<tr>
<td>19:18</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target0’s X Bias for Dither</td>
</tr>
<tr>
<td>17</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>16:15</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target0’s Dither Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: Dither Table with multiplied by (2^n – 1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: Rounding with multiplied by (2^n – 1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: Dither Table without multiplied by (2^n – 1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: Rounding without multiplied by (2^n – 1)</td>
</tr>
<tr>
<td>14:12</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>11:8</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target0’s Raster Operation</td>
</tr>
<tr>
<td>10:9</td>
<td>WO</td>
<td>xxh</td>
<td>DeGamma for Render Target0’s Reading Color</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable. Use one-by-one mapping to deGamma the readen color from 2.2 to 1.0 color field before alpha blending operation.</td>
</tr>
<tr>
<td>5:4</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target0 is SRGB</td>
</tr>
<tr>
<td>3</td>
<td>WO</td>
<td>xxh</td>
<td>Mask of Render Target0’s Alpha Channel</td>
</tr>
<tr>
<td>2</td>
<td>WO</td>
<td>xxh</td>
<td>Mask of Render Target0’s Red Channel</td>
</tr>
<tr>
<td>1</td>
<td>WO</td>
<td>xxh</td>
<td>Mask of Render Target0’s Green Channel</td>
</tr>
<tr>
<td>0</td>
<td>WO</td>
<td>xxh</td>
<td>Mask of Render Target0’s Blue Channel</td>
</tr>
</tbody>
</table>

### HParaType = 01h, Sub-Address = 54 – 57h: Reserved (for Destination Setting – Render Target 0)
### HParaType = 01h, Sub-Address = 58h
**Destination Setting – Render Target 1 – Setting 1**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:0</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target 1’s Base Address</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>In unit of 256 bytes.</td>
</tr>
</tbody>
</table>

### HParaType = 01h, Sub-Address = 59h
**Destination Setting – Render Target 1 – Setting 2**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23</td>
<td>WO</td>
<td>xxh</td>
<td>Memory Mode of Render Target 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Linear mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Tile mode</td>
</tr>
<tr>
<td>22</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target 1’s Tile is 16-Pixel high</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>&lt;HMRT1TileH16&gt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Normal 8-pixel high</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: 16-pixel high</td>
</tr>
<tr>
<td>21:20</td>
<td>WO</td>
<td>xxh</td>
<td>Location Setting of Render Target 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: System Local Frame Buffer (S.L.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: System Dynamic Frame Buffer (S.F.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: Reserved (System Memory)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: Reserved</td>
</tr>
<tr>
<td>19:0</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

### HParaType = 01h, Sub-Address = 5Ah
**Destination Setting – Render Target 1 – Setting 3**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:16</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target 1’s Format</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The definition is same as Render Target0’s Format.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Please refer to HParaType 01h, Sub-Address 52h bits [23:16] for details.</td>
</tr>
<tr>
<td>15</td>
<td>WO</td>
<td>xxh</td>
<td>Color Extending Mode (Excluding Alpha)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Extending with high color bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Extending with zero</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Please refer to HParaType 01h, Sub-Address 52h bit [15] for details.</td>
</tr>
<tr>
<td>14:13</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>12</td>
<td>WO</td>
<td>xxh</td>
<td>Saturation of PS’s Output for Render Target “M”</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Clamp PS’s output color oCm to related render tager format’s range</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>For format ARGB and Luminance: MINVALUE = 0.0, MAXVALUE = 1.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>For 16-bit floating color format: MINVALUE = 16’hFBFF, MAXVALUE = 16’h7BFF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>For 32-bit floating color format: MINVALUE = 32’h7F7FFFFFF, MAXVALUE =32’hFF7FFFFFF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Clamped Value = min(MAXVALUE, max(oCm, MINVALUE))</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Note if oCm is “NAN”, clamped value is MINVALUE</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: oCm doesn’t clamp</td>
</tr>
<tr>
<td>11:10</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>9:0</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target 1’s Pitch</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>In unit of 32 bytes for linear mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>In unit of tile (256 bytes or 512 bytes depend on HMRT1TileH16) for tile mode.</td>
</tr>
</tbody>
</table>
### HParaType = 01h, Sub-Address = 5Bh

#### Destination Setting – Render Target 1 – Setting 4

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target1’s Y Inverse for Dither</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Not inverse</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Inverse</td>
</tr>
<tr>
<td>22:21</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target1’s Y Bias for Dither</td>
</tr>
<tr>
<td>20</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target1’s X Inverse for Dither</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Not inverse</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Inverse</td>
</tr>
<tr>
<td>19:18</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target1’s X Bias for Dither</td>
</tr>
<tr>
<td>17</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>16:15</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target1’s Dither Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: Dither Table with multiplied by ((2^n – 1))</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: Rounding with multiplied by ((2^n – 1))</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: Dither Table without multiplied by ((2^n – 1))</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: Rounding without multiplied by ((2^n – 1))</td>
</tr>
<tr>
<td>14:12</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>11:8</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target1’s Raster Operation</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0000: BLACK 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0001: NOT_MERGE_PEN DPon</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0010: MASK_NOT_PEN DPna</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0011: NOT_COPY_PEN Pn</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0100: MASK_PEN_NOT PDna</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0101: NOT Dn</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0110: XOR_PEN DPx</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0111: NOT_MASK_PEN DPan</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1000: MASK_PEN DPa</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1001: NOT_XOR_PEN DPxn</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1010: NOP D</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1011: MERGE_NOT_PEN DPno</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1100: COPY_PEN P</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1101: MERGE_PEN_NOT PDno</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1110: MERGE_PEN DPo</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1111: WHITE 1</td>
</tr>
<tr>
<td>7</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>6</td>
<td>WO</td>
<td>xxh</td>
<td>DeGamma for Render Target1’s Reading Color</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable. Use one-by-one mapping to deGamma the readen color from 2.2 to 1.0 color field before alpha blending operation.</td>
</tr>
<tr>
<td>5:4</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target Is SRGB</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: Gamma 1.0 field. Disable Gamma correction of writing back color</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: Gamma correction enabled. Use one-by-one mapping to transform the color to gamma 2.2 field before written back to color buffer</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: Gamma correction enabled. Use Gamma Table “HGTWC” to transform each color channel to a specific color field before written back to color buffer</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: Reserved</td>
</tr>
<tr>
<td>3</td>
<td>WO</td>
<td>xxh</td>
<td>Mask of Render Target1’s Alpha Channel</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: The relative data bit will remain the same in Frame Buffer</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: The relative data bit will be updated by a new calculated number</td>
</tr>
<tr>
<td>2</td>
<td>WO</td>
<td>xxh</td>
<td>Mask of Render Target1’s Red Channel</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: The relative data bit will remain the same in Frame Buffer</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: The relative data bit will be updated by a new calculated number</td>
</tr>
<tr>
<td>1</td>
<td>WO</td>
<td>xxh</td>
<td>Mask of Render Target1’s Green Channel</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: The relative data bit will remain the same in Frame Buffer</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: The relative data bit will be updated by a new calculated number</td>
</tr>
<tr>
<td>0</td>
<td>WO</td>
<td>xxh</td>
<td>Mask of Render Target1’s Blue Channel</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: The relative data bit will remain the same in Frame Buffer</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: The relative data bit will be updated by a new calculated number</td>
</tr>
</tbody>
</table>

**HParaType = 01h, Sub-Address = 5C-5Fh: Reserved** (for Destination Setting – Render Target 1)
### HParaType = 01h, Sub-Address = 60h
**Destination Setting – Render Target 2 – Setting 1**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:0</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target2’s Base Address</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>In unit of 256 bytes.</td>
</tr>
</tbody>
</table>

### HParaType = 01h, Sub-Address = 61h
**Destination Setting – Render Target 2 – Setting 2**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23</td>
<td>WO</td>
<td>xxh</td>
<td>Memory Mode of Render Target 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Linear mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Tile mode</td>
</tr>
<tr>
<td>22</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target2’s Tile is 16-pixel high</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Normal 8-pixel high</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: 16-pixel high</td>
</tr>
<tr>
<td>21:20</td>
<td>WO</td>
<td>xxh</td>
<td>Location Setting of Render Target 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: System Local Frame Buffer (S.L.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: System Dynamic Frame Buffer (S.F.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: Reserved (System Memory)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: Reserved</td>
</tr>
<tr>
<td>19:0</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

### HParaType = 01h, Sub-Address = 62h
**Destination Setting – Render Target 2 – Setting 3**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:16</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target2’s Format</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The definition is same as Render Target0’s Format.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Please refer to HParaType 01h, Sub-Address 52h bits [23:16] for details.</td>
</tr>
<tr>
<td>15</td>
<td>WO</td>
<td>xxh</td>
<td>Color Extending Mode (Excluding Alpha)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Extending with high color bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Extending with zero</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Please refer to HParaType 01h, Sub-Address 52h bit [15] for details.</td>
</tr>
<tr>
<td>14:13</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>12</td>
<td>WO</td>
<td>xxh</td>
<td>Saturation of PS’s Output for Render Target “M”</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Clamp PS’s output color oCm to related render target format’s range</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>For format ARGB and Luminance: MINVALUE = 0.0, MAXVALUE = 1.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>For 16-bit floating color format: MINVALUE = 16’hFBFF, MAXVALUE = 16’h7BFF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>For 32-bit floating color format: MINVALUE = 32’h7F7FFFFFF, MAXVALUE =32’hFF7FFFFFF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Clamped Value = min(MAXVALUE, max(oCm, MINVALUE))</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Note if oCm is “NAN”, clamped value is MINVALUE</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: oCm doesn’t clamp</td>
</tr>
<tr>
<td>11:10</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>9:0</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target2’s Pitch</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>In unit of 32 bytes for linear mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>In unit of tile (256 bytes or 512 byte depend on HMRT2TileH16) for tile mode.</td>
</tr>
</tbody>
</table>
### HParaType = 01h, Sub-Address = 63h

**Destination Setting – Render Target 2 – Setting 4**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target2’s Y Inverse for Dither</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Not inverse</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Inverse</td>
</tr>
<tr>
<td>22:21</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target2’s Y Bias for Dither</td>
</tr>
<tr>
<td>20</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target2’s X Inverse for Dither</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Not inverse</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Inverse</td>
</tr>
<tr>
<td>19:18</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target2’s X Bias for Dither</td>
</tr>
<tr>
<td>17</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>16:15</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target2’s Dither Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: Dither Table with multiplied by (2^n - 1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: Rounding with multiplied by (2^n - 1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: Dither Table without multiplied by (2^n - 1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: Rounding without multiplied by (2^n - 1)</td>
</tr>
<tr>
<td>14:12</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>11:8</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target2’s Raster Operation</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0000: BLACK 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0001: NOT MERGE PEN DPon</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0010: MASK NOT PEN DPna</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0011: NOT COPY PEN Pn</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0100: MASK PEN NOT PDna</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0101: NOT Dn</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0110: XOR PEN DPx</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0111: NOT MASK PEN DPan</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1000: MASK PEN DPa</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1001: NOT XOR PEN DPxn</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1010: NOP D</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1011: MERGE NOT PEN DPno</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1100: COPY PEN P</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1101: MERGE PEN NOT PDno</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1110: MERGE PEN PDp</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1111: WHITE 1</td>
</tr>
<tr>
<td>7</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>6</td>
<td>WO</td>
<td>xxh</td>
<td>DeGamma for Render Target2’s Reading Color</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable. Use one-by-one mapping to deGamma the readen color from 2.2 to 1.0 color field before alpha blending operation</td>
</tr>
<tr>
<td>5:4</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target2 is SRGB</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: Gamma 1.0 field. Disable Gamma correction of writing back color</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: Gamma correction enabled. Use one-by-one mapping to transform the color to gamma 2.2 field before written back to color buffer</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: Gamma correction enabled. Use Gamma Table “HGTWC” to transform each color channel to a specific color field before written back to color buffer</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: Reserved</td>
</tr>
<tr>
<td>3</td>
<td>WO</td>
<td>xxh</td>
<td>Mask of Render Target2’s Alpha Channel</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: The relative data bit will remain the same in Frame Buffer</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: The relative data bit will be updated by a new calculated number</td>
</tr>
<tr>
<td>2</td>
<td>WO</td>
<td>xxh</td>
<td>Mask of Render Target2’s Red Channel</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: The relative data bit will remain the same in Frame Buffer</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: The relative data bit will be updated by a new calculated number</td>
</tr>
<tr>
<td>1</td>
<td>WO</td>
<td>xxh</td>
<td>Mask of Render Target2’s Green Channel</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: The relative data bit will remain the same in Frame Buffer</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: The relative data bit will be updated by a new calculated number</td>
</tr>
<tr>
<td>0</td>
<td>WO</td>
<td>xxh</td>
<td>Mask of Render Target2’s Blue Channel</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: The relative data bit will remain the same in Frame Buffer</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: The relative data bit will be updated by a new calculated number</td>
</tr>
</tbody>
</table>

**HParaType = 01h, Sub-Address = 64-67h: Reserved** (for Destination Setting – Render Target 2)
### HParaType = 01h, Sub-Address = 68h

#### Destination Setting – Render Target 3 – Setting 1

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:0</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target3’s Base Address</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>In unit of 256 bytes.</td>
</tr>
</tbody>
</table>

### HParaType = 01h, Sub-Address = 69h

#### Destination Setting – Render Target 3 – Setting 2

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23</td>
<td>WO</td>
<td>xxh</td>
<td>Memory Mode of Render Target 3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Linear mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Tile mode</td>
</tr>
<tr>
<td>22</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target3’s Tile is 16-pixel high</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>&lt;HMRT3TileH16&gt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Normal 8-pixel high</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: 16-pixel high</td>
</tr>
<tr>
<td>21:20</td>
<td>WO</td>
<td>xxh</td>
<td>Location Setting of Render Target 3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: System Local Frame Buffer (S.L.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: System Dynamic Frame Buffer (S.F.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: Reserved (System Memory)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: Reserved</td>
</tr>
<tr>
<td>19:0</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

### HParaType = 01h, Sub-Address = 6Ah

#### Destination Setting – Render Target 3 – Setting 3

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:16</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target3’s Format</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The definition is same as Render Target0’s Format.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Please refer to HParaType 01h, Sub-Address 52h bits [23:16] for details.</td>
</tr>
<tr>
<td>15</td>
<td>WO</td>
<td>xxh</td>
<td>Color Extending Mode (Excluding Alpha)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Extending with high color bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Extending with zero</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Please refer to HParaType 01h, Sub-Address 52h bit [15] for details.</td>
</tr>
<tr>
<td>14:13</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>12</td>
<td>WO</td>
<td>xxh</td>
<td>Saturation of PS’s Output for Render Target “M”</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Clamp PS’s output color oCm to related render tager format’s range.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>For format ARGB and Luminance: MINVALUE = 0.0, MAXVALUE = 1.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>For 16-bit floating color format: MINVALUE = 16’hFBFF, MAXVALUE = 16’h7BFF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>For 32-bit floating color format: MINVALUE = 32’h7F7FFFFF, MAXVALUE = 32’hFF7FFFFFF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Clamped Value = min(MAXVALUE, max(oCm, MINVALUE))</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Note if oCm is “NAN”, clamped value is MINVALUE</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: oCm doesn’t clamp</td>
</tr>
<tr>
<td>11:10</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>9:0</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target3’s Pitch</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>In unit of 32 bytes for linear mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>In unit of tile (256 bytes or 512 bytes depend on HMRT3TileH16) for tile mode.</td>
</tr>
</tbody>
</table>
### HParaType = 01h, Sub-Address = 6Bh
#### Destination Setting – Render Target 3 – Setting 4

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
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<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target3’s Y Inverse for Dither</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Not inverse</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Inverse</td>
</tr>
<tr>
<td>22:21</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target3’s Y Bias for Dither</td>
</tr>
<tr>
<td>20</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target3’s X Inverse for Dither</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Not inverse</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Inverse</td>
</tr>
<tr>
<td>19:18</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target3’s X Bias for Dither</td>
</tr>
<tr>
<td>17</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>16:15</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target3’s Dither Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: Dither Table with multiplied by (2^n – 1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: Rounding with multiplied by (2^n – 1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: Dither Table without multiplied by (2^n – 1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: Rounding without multiplied by (2^n – 1)</td>
</tr>
<tr>
<td>14:12</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>11:8</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target3’s Raster Operation</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0000: BLACK</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0001: NOT_MERGE_PEN  D_Pon</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0010: MASK_NOT_PEN  D_Pna</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0011: NOT_COPY_PEN  Pn</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0100: MASK_PEN_NOT  P_Dna</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0101: NOT  Dn</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0110: XOR_PEN  D_Px</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0111: NOT_MASK_PEN  D_Pan</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1000: MASK_PEN  D_Pa</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1001: NOT_XOR_PEN  D_Pxn</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1010: NOP  Dn</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1011: MERGE_NOT_PEN  D_Pno</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1100: COPY_PEN  P</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1101: MERGE_PEN_NOT  P_Dno</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1110: MERGE_PEN  P_Dp</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1111: WHITE  1</td>
</tr>
<tr>
<td>7</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>6</td>
<td>WO</td>
<td>xxh</td>
<td>DeGamma for Render Target3’s Reading Color</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable. Use one-by-one mapping to deGamma the readen color from 2.2 to 1.0 color field before alpha blending operation.</td>
</tr>
<tr>
<td>5:4</td>
<td>WO</td>
<td>xxh</td>
<td>Render Target3 is SRGB</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: Gamma 1.0 field. Disable Gamma correction of writing back color</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: Gamma correction enabled. Use one-by-one mapping to transform the color to gamma 2.2 field before written back to color buffer</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: Gamma correction enabled. Use Gamma Table “HGTWC” to transform each color channel to a specific color field before written back to color buffer</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: Reserved</td>
</tr>
<tr>
<td>3</td>
<td>WO</td>
<td>xxh</td>
<td>Mask of Render Target3’s Alpha Channel</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: The relative data bit will remain the same in Frame Buffer</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: The relative data bit will be updated by a new calculated number</td>
</tr>
<tr>
<td>2</td>
<td>WO</td>
<td>xxh</td>
<td>Mask of Render Target3’s Red Channel</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: The relative data bit will remain the same in Frame Buffer</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: The relative data bit will be updated by a new calculated number</td>
</tr>
<tr>
<td>1</td>
<td>WO</td>
<td>xxh</td>
<td>Mask of Render Target3’s Green Channel</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: The relative data bit will remain the same in Frame Buffer</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: The relative data bit will be updated by a new calculated number</td>
</tr>
<tr>
<td>0</td>
<td>WO</td>
<td>xxh</td>
<td>Mask of Render Target3’s Blue Channel</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: The relative data bit will remain the same in Frame Buffer</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: The relative data bit will be updated by a new calculated number</td>
</tr>
</tbody>
</table>

**HParaType = 01h, Sub-Address = 6C-6Fh: Reserved** (for Destination Setting – Render Target 3)
### HPaRTYpe = 01h, Sub-Address = 70h

#### Fog Setting 1

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:8</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>7</td>
<td>WO</td>
<td>xxh</td>
<td>Fog Factor Source From PS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Fog factor is generated in PE (Including vertex, linear or exponential Fog)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Fog factor and Fog operation is dealt by the PS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Instead of 8-bit fixed Fog factor, PE sends “Fog coordinate” with format floating s[7].10 to PS.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Note: When this bit is set, HenFOGRT0, HenFOGRT1, HenFOGMRT2 and HenFOGMRT3 should be disabled.</td>
</tr>
<tr>
<td>6</td>
<td>WO</td>
<td>xxh</td>
<td>Linear Fog Calculation Factor Setting 2 &lt;HFogLF2&gt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Use W or Z to calculate linear Fog by setting of bit 4</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Use attribute “Fog” as fog coordinate to calculate linear Fog</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>If (HFogLF2 == 1) // this bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Use Fog attribute to calculate linear fog or exponential fog (fog per pixel)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Else if (HFogLF == 0) // bit 4</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Use Z attribute to calculate linear fog or exponential fog (fog per pixel)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Else Use W attribute to calculate linear fog or exponential fog (fog per pixel)</td>
</tr>
<tr>
<td>5</td>
<td>WO</td>
<td>xxh</td>
<td>Fog Factor from Spectra Color’s Alpha</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Individual Fog attribute</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Use Spectral (Color 2) Alpha as Fog factor</td>
</tr>
<tr>
<td>4</td>
<td>WO</td>
<td>xxh</td>
<td>Linear Fog Calculation Factor Setting &lt;HFogLF&gt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Use W to calculate linear Fog</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Use Z to calculate linear Fog</td>
</tr>
<tr>
<td>3</td>
<td>WO</td>
<td>xxh</td>
<td>Fog Equation</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Use Fog equation 0: Cout = f * ( Cin + Cspec ) + (1-f) * HCFog</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Use Fog equation 1: Cout = (1-f) * ( Cin + Cspec ) + f * HCFog</td>
</tr>
<tr>
<td>2:0</td>
<td>WO</td>
<td>xxh</td>
<td>Fog Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When substituting for vertex Z, Z is calculated in PS (HZSrcPS = 1), linear or non-linear Fog from Z is not allowed.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>000: Local Fog</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>001: Reserved (Global Fog)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>010: Linear Fog</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>011: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100: Exponential Fog</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>101: Exponential_2 Fog</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11x: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Note: Setting of 1xx: is for Non-linear Fog (Use Fog Table).</td>
</tr>
</tbody>
</table>

### HPaRTYpe = 01h, Sub-Address = 71h

#### Fog Setting 2

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>22:12</td>
<td>WO</td>
<td>xxh</td>
<td>G of HCFOgCL</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Positive fixed-point from 0 to 1.0</td>
</tr>
<tr>
<td>11</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>10:0</td>
<td>WO</td>
<td>xxh</td>
<td>G of HCFOgCL</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Positive fixed-point from 0 to 1.0</td>
</tr>
</tbody>
</table>

### HPaRTYpe = 01h, Sub-Address = 72h

#### Fog Setting 3

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:11</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>10:0</td>
<td>WO</td>
<td>xxh</td>
<td>R of Fog Color</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Positive fixed-point from 0 to 1.0</td>
</tr>
</tbody>
</table>
### HP araType = 01h, Sub-Address = 73h
#### Fog Setting 4

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:15</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 14:0        | WO        | xxh     | Fog Start   
Floating-point is used to calculate Fog factor. The format is floating-point [8].7.

### HP araType = 01h, Sub-Address = 74h
#### Fog Setting 5

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:0</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

### HP araType = 01h, Sub-Address = 75h
#### Fog Setting 6

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:4</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 3:0         | WO        | xxh     | Mantissa Part of the One Over (Fog End - Fog Start) <HFogOOdMF>  
Note: The leading one is not included.

### HP araType = 01h, Sub-Address = 76h
#### Fog Setting 7

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:8</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 7:0         | WO        | xxh     | Exponential Part of the One Over (Fog End - Fog Start) <HFogOOdEF>  
Format is IEEE’s floating presentation.  
The value of 1/(Fog End – Fog Start) is ( 1.HfogOOdMF[1:0] * 2^(HfogOOdEF – 127) ) .

### HP araType = 01h, Sub-Address = 77h
#### Fog Setting 8

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:15</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 14:0        | WO        | xxh     | Lower 3 Bytes of Fog End <HFogEnd>  
The format of HFogEnd is floating-point [8].7.

### HP araType = 01h, Sub-Address = 78h
#### Fog Setting 9

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:21</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>7:0</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

### HP araType = 01h, Sub-Address = 79-7Fh: Reserved (for Fog Setting)
### HPType = 01h, Sub-Address = 80h
#### Miscellaneous Setting 1

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:12</td>
<td>WO</td>
<td>xxh</td>
<td>Color Window Top Clipping Value in the Range of 0 to 2048</td>
</tr>
<tr>
<td>11:0</td>
<td>WO</td>
<td>xxh</td>
<td>Color Window Bottom Clipping Value in the Range of 0 to 2048</td>
</tr>
</tbody>
</table>

### HPType = 01h, Sub-Address = 81h
#### Miscellaneous Setting 2

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:12</td>
<td>WO</td>
<td>xxh</td>
<td>Color Window Left Clipping Value in the Range of 0 to 2048</td>
</tr>
<tr>
<td>11:0</td>
<td>WO</td>
<td>xxh</td>
<td>Color Window Right Clipping Value in the Range of 0 to 2048</td>
</tr>
</tbody>
</table>

### HPType = 01h, Sub-Address = 82h
#### Miscellaneous Setting 3

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:12</td>
<td>WO</td>
<td>xxh</td>
<td>Scissor Window Top Clipping Value in the Range of 0 to 2048</td>
</tr>
<tr>
<td>11:0</td>
<td>WO</td>
<td>xxh</td>
<td>Scissor Window Bottom Clipping Value in the Range of 0 to 2048</td>
</tr>
</tbody>
</table>

### HPType = 01h, Sub-Address = 83h
#### Miscellaneous Setting 4

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:12</td>
<td>WO</td>
<td>xxh</td>
<td>Scissor Window Left Clipping Value in the Range of 0 to 2048</td>
</tr>
<tr>
<td>11:0</td>
<td>WO</td>
<td>xxh</td>
<td>Scissor Window Right Clipping Value in the Range of 0 to 2048</td>
</tr>
</tbody>
</table>

### HPType = 01h, Sub-Address = 84h
#### Miscellaneous Setting 5

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:16</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>15:0</td>
<td>WO</td>
<td>xxh</td>
<td>Line Pattern</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The Line Pattern bit starts from the LSB.</td>
</tr>
</tbody>
</table>

### HPType = 01h, Sub-Address = 85h
#### Miscellaneous Setting 6

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23</td>
<td>WO</td>
<td>xxh</td>
<td>Line Pattern Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Hardware would reset related repeat counter automatically whenever this register is set to “1”. It is NOT necessary for driver to clear this bit. Hardware would clear it after the counter reset.</td>
</tr>
<tr>
<td>22:16</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>15:0</td>
<td>WO</td>
<td>xxh</td>
<td>Line Pattern Repeat Factor</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This number denotes how many times that a line pattern bit will be used for several line pixels.</td>
</tr>
</tbody>
</table>
### HParaType = 01h, Sub-Address = 86h
**Miscellaneous Setting 7 - Lower 3 Bytes of Solid Shading Color**  \(<HSolidCL>\)

<table>
<thead>
<tr>
<th>Bits 23:0</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:16</td>
<td>WO</td>
<td>xxh</td>
<td>R of Solid Shading Color</td>
</tr>
<tr>
<td>15:8</td>
<td>WO</td>
<td>xxh</td>
<td>G of Solid Shading Color</td>
</tr>
<tr>
<td>7:0</td>
<td>WO</td>
<td>xxh</td>
<td>B of Solid Shading Color</td>
</tr>
</tbody>
</table>

### HParaType = 01h, Sub-Address = 87h
**Miscellaneous Setting 8 - Highest Byte of Solid Shading Color**  \(<HSolidCH>\)

<table>
<thead>
<tr>
<th>Bits 23:0</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:8</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>7:0</td>
<td>WO</td>
<td>xxh</td>
<td>Alpha of Solid Shading Color</td>
</tr>
</tbody>
</table>

### HParaType = 01h, Sub-Address = 88h
**Miscellaneous Setting 9**

<table>
<thead>
<tr>
<th>Bits 23:0</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:13</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>12:0</td>
<td>WO</td>
<td>xxh</td>
<td>Guard Band Window Left Clipping Value Format as s12 2’s complement</td>
</tr>
</tbody>
</table>

### HParaType = 01h, Sub-Address = 89h
**Miscellaneous Setting 10**

<table>
<thead>
<tr>
<th>Bits 23:0</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:13</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>12:0</td>
<td>WO</td>
<td>xxh</td>
<td>Guard Band Window Right Clipping Value Format as s12 2’s complement</td>
</tr>
</tbody>
</table>

### HParaType = 01h, Sub-Address = 8Ah
**Miscellaneous Setting 11**

<table>
<thead>
<tr>
<th>Bits 23:0</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23</td>
<td>WO</td>
<td>xxh</td>
<td>Enhance TX’s Precision During PE’s Rendering 0: Disable 1: Enable</td>
</tr>
<tr>
<td>22:17</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>16</td>
<td>WO</td>
<td>xxh</td>
<td>Zero Round Mode for the Texture Coordinate from PE to PS 0: Round to zero 1: Round to 0’</td>
</tr>
<tr>
<td>15:4</td>
<td>WO</td>
<td>xxh</td>
<td>Bottom Y Value for PS’s Location Register (&lt;HYB4LocationReg&gt;) As 12 positive integer</td>
</tr>
<tr>
<td>3</td>
<td>WO</td>
<td>xxh</td>
<td>Enable HYB4LocationReg  HYB4LocationReg is defined in bits [15:4]. 0: Disable 1: Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>If ( HPSLocationReg == true ) // T01A90[19] and this bit is set ) LocationReg.Y = floating(HYB4LocationReg – PEY) Else LocationReg.Y = floating(PEY)</td>
</tr>
<tr>
<td>2</td>
<td>WO</td>
<td>xxh</td>
<td>PreModulate Color 0 (Diffuse Color) with Ws 0: Not pre-modulated; multiply C0 and Ws in SE 1: Pre-modulated; don’t multiply C0 and Ws in WS</td>
</tr>
<tr>
<td>1</td>
<td>WO</td>
<td>xxh</td>
<td>PreModulate Color 1 (Specula Color) with Ws 0: Not pre-modulated; multiply C1 and Ws in SE 1: Pre-modulated; don’t multiply C1 and Ws in WS</td>
</tr>
</tbody>
</table>
**W0 xxh**  
**PreModulate Fog with Ws**  
0: Not pre-modulated; multiply Fog and Ws in SE  
1: Pre-modulated; don’t multiply Fog and Ws in WS

**23:0 W0 xxh**  
**Reserved**

**HPaParaType = 01h, Sub-Address = 8B-8Fh: Reserved** (for Miscellaneous Setting)

**HPaParaType = 01h, Sub-Address = 90h**

### Pixel Shader Setting 1

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 23          | W0        | xxh     | Disable the Function of Detecting “ALUOut” by Hardware PS  
0: PS would detect the “ALUOut” automatically  
1: “ALUOut” set by software PS code |
| 22          | W0        | xxh     | Software Sets the HPSDPNTPAU_N  
0: Hardware judges dependant TAU instruction by  
(HPSINAtoT[127:0] != 128’h0) |  
1: Software sets HPSDPNTPAU_N (bit 21) and hardware followed |
| 21          | W0        | xxh     | TAU Execute Dependant Instruction Control <HPSDPNTPAU_N>  
0: There is dependant TAU instruction  
1: No dependant TAU instruction |
| 20          | W0        | xxh     | TAU Executes Dependant TXKILL Instruction Control  
0: TAU would execute dependant TXKILL instruction  
1: TAU would not execute dependant TXKILL instruction  
Example of “dependant TXKILL”  
Example 1  
```plaintext  
txld r0, t0, s0 ← load texture for CV ALID | STV ALID  
mad t1, r0, xx, xx  
txkill t1 ← effect both CVALID and STVALID  
```
| 19          | W0        | xxh     | Pixel Shader Gets Location Register (X, Y, Z, 1/W) from PE <HPSLocationReg>  
0: No location Register used in PS  
1: Location Register used in PS |
| 18          | W0        | 0       | Pixel Shader Fired by ALU Instruction Initially <HPSFireALU>  
0: Disable (Default)  
1: Enable |
| 17          | W0        | xxh     | The Contents of PS’s Constant Registers with Index 32 to 54 Are the Same as the Contents in Index from 0 to 22  
0: Filled independently  
1: Fill the same value to n and (n+32) |
| 16:15       | W0        | xxh     | Pixel Shader Configure  
00: Normal configure. There are 16 texture registers and 12 temporary registers used for each pixel.  
01: Double configure. There are 8 texture registers and 6 temporary registers used for each pixel.  
10: Triple configure. There are 5 texture registers and 4 temporary registers used for each pixel.  
11: 4-Time configure. There are 4 texture registers and 3 temporary registers used for each pixel. |
| 14          | W0        | xxh     | Texture Register 14(t14) As the Input to ALU  
0: None  
1: For ALU (Arithmetic unit) |
| 13          | W0        | xxh     | Texture Register 13(t13) As the Input to ALU  
0: None  
1: For ALU (Arithmetic unit) |
| 12          | W0        | xxh     | Texture Register 12(t12) As the Input to ALU  
0: None  
1: For ALU (Arithmetic unit) |
| 11          | W0        | xxh     | Texture Register 11(t11) As the Input to ALU  
0: None  
1: For ALU (Arithmetic unit) |
| 10          | W0        | xxh     | Texture Register 10(t10) As the Input to ALU  
0: None  
1: For ALU (Arithmetic unit) |
| 9           | W0        | xxh     | Texture Register 9(t9) As the Input to ALU  
0: None  
1: For ALU (Arithmetic unit) |
| 8           | W0        | xxh     | Texture Register 8(t8) As the Input to ALU  
0: None  
1: For ALU (Arithmetic unit) |
### HParaType = 01h, Sub-Address = 91h

**Pixel Shader Setting 2**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 23 | WO | xxh | Texture Register 15(t15) As the Input to ALU  
0: None  
1: For ALU (Arithmetic unit) |
| 22:16 | WO | xxh | Reserved |
| 15 | WO | xxh | Texture Register 15(t15) As the Input to TAU  
0: None  
1: For TAU (Texture address unit) |
| 14 | WO | xxh | Texture Register 14(t14) As the Input to TAU  
0: None  
1: For TAU (Texture address unit) |
| 13 | WO | xxh | Texture Register 13(t13) As the Input to TAU  
0: None  
1: For TAU (Texture address unit) |
| 12 | WO | xxh | Texture Register 12(t12) As the Input to TAU  
0: None  
1: For TAU (Texture address unit) |
| 11 | WO | xxh | Texture Register 11(t11) As the Input to TAU  
0: None  
1: For TAU (Texture address unit) |
| 10 | WO | xxh | Texture Register 10(t10) As the Input to TAU  
0: None  
1: For TAU (Texture address unit) |
| 9 | WO | xxh | Texture Register 9(t9) As the Input to TAU  
0: None  
1: For TAU (Texture address unit) |
| 8 | WO | xxh | Texture Register 8(t8) As the Input to TAU  
0: None  
1: For TAU (Texture address unit) |
| 7 | WO | xxh | Texture Register 7(t7) As the Input to TAU  
0: None  
1: For TAU (Texture address unit) |
| 6 | WO | xxh | Texture Register 6(t6) As the Input to TAU  
0: None  
1: For TAU (Texture address unit) |
| 5 | WO | xxh | Texture Register 5(t5) As the Input to TAU  
0: None  
1: For TAU (Texture address unit) |
| 4 | WO | xxh | Texture Register 4(t4) As the Input to TAU  
0: None  
1: For TAU (Texture address unit) |
### Pixel Shader Setting 3

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23</td>
<td>WO</td>
<td>xxh</td>
<td>The Result of SOP’s Special Case Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: The result of SOP’s special case such as 1/0 or 1/(\sqrt{0}) is “MAX”</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: The result of SOP’s special case such as 1/0 or 1/(\sqrt{0}) is “INFINITE”</td>
</tr>
<tr>
<td>22</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>21:16</td>
<td>WO</td>
<td>xxh</td>
<td>Length of TAU Instruction</td>
</tr>
<tr>
<td>15</td>
<td>WO</td>
<td>xxh</td>
<td>Enable Texture Register 12-15 Swapping to Internal Register 0-3 whenever TAU-to-ALU Switches</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td>14</td>
<td>WO</td>
<td>xxh</td>
<td>Enable Internal Register 0-3 Swapping to Texture Register 12-15 whenever ALU-to-TAU Switches</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td>13:9</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>8:0</td>
<td>WO</td>
<td>xxh</td>
<td>Length of ALU Instruction</td>
</tr>
</tbody>
</table>

### Pixel Shader Setting 4

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from TAU to ALU after the 23(^{rd}) TAU Instruction</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Operate next TAU instruction</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Switch to operate ALU instruction</td>
</tr>
<tr>
<td>22</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from TAU to ALU after the 22(^{nd}) TAU Instruction</td>
</tr>
<tr>
<td>21</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from TAU to ALU after the 21(^{st}) TAU Instruction</td>
</tr>
<tr>
<td>20</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from TAU to ALU after the 20(^{th}) TAU Instruction</td>
</tr>
<tr>
<td>19</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from TAU to ALU after the 19(^{th}) TAU Instruction</td>
</tr>
<tr>
<td>18</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from TAU to ALU after the 18(^{th}) TAU Instruction</td>
</tr>
<tr>
<td>17</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from TAU to ALU after the 17(^{th}) TAU Instruction</td>
</tr>
<tr>
<td>16</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from TAU to ALU after the 16(^{th}) TAU Instruction</td>
</tr>
<tr>
<td>15</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from TAU to ALU after the 15(^{th}) TAU Instruction</td>
</tr>
<tr>
<td>14</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from TAU to ALU after the 14(^{th}) TAU Instruction</td>
</tr>
<tr>
<td>13</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from TAU to ALU after the 13(^{th}) TAU Instruction</td>
</tr>
<tr>
<td>12</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from TAU to ALU after the 12(^{th}) TAU Instruction</td>
</tr>
<tr>
<td>11</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from TAU to ALU after the 11(^{th}) TAU Instruction</td>
</tr>
<tr>
<td>10</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from TAU to ALU after the 10(^{th}) TAU Instruction</td>
</tr>
<tr>
<td>9</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from TAU to ALU after the 9(^{th}) TAU Instruction</td>
</tr>
<tr>
<td>8</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from TAU to ALU after the 8(^{th}) TAU Instruction</td>
</tr>
<tr>
<td>7</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from TAU to ALU after the 7(^{th}) TAU Instruction</td>
</tr>
<tr>
<td>6</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from TAU to ALU after the 6(^{th}) TAU Instruction</td>
</tr>
<tr>
<td>5</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from TAU to ALU after the 5(^{th}) TAU Instruction</td>
</tr>
<tr>
<td>4</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from TAU to ALU after the 4(^{th}) TAU Instruction</td>
</tr>
<tr>
<td>3</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from TAU to ALU after the 3(^{rd}) TAU Instruction</td>
</tr>
<tr>
<td>2</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from TAU to ALU after the 2(^{nd}) TAU Instruction</td>
</tr>
<tr>
<td>1</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from TAU to ALU after the 1(^{st}) TAU Instruction</td>
</tr>
<tr>
<td>0</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from TAU to ALU after the 0(^{th}) TAU Instruction</td>
</tr>
</tbody>
</table>
### HParaType = 01h, Sub-Address = 94h

**Pixel Shader Setting 5**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:8</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>7</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from TAU to ALU after the 31st TAU Instruction</td>
</tr>
<tr>
<td>6</td>
<td>WO</td>
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<td>Instruction Switch from TAU to ALU after the 30th TAU Instruction</td>
</tr>
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<td>5</td>
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<td>Instruction Switch from TAU to ALU after the 29th TAU Instruction</td>
</tr>
<tr>
<td>4</td>
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<td>Instruction Switch from TAU to ALU after the 28th TAU Instruction</td>
</tr>
<tr>
<td>3</td>
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<td>Instruction Switch from TAU to ALU after the 27th TAU Instruction</td>
</tr>
<tr>
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<td>Instruction Switch from TAU to ALU after the 26th TAU Instruction</td>
</tr>
<tr>
<td>1</td>
<td>WO</td>
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<td>Instruction Switch from TAU to ALU after the 25th TAU Instruction</td>
</tr>
<tr>
<td>0</td>
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<td>xxh</td>
<td>Instruction Switch from TAU to ALU after the 24th TAU Instruction</td>
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### HParaType = 01h, Sub-Address = 95h

**Pixel Shader Setting 6**

<table>
<thead>
<tr>
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<tr>
<td>23</td>
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<td>Instruction Switch from ALU to TAU after the 23rd ALU Instruction</td>
</tr>
<tr>
<td>22</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 22nd ALU Instruction</td>
</tr>
<tr>
<td>21</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 21st ALU Instruction</td>
</tr>
<tr>
<td>20</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 20th ALU Instruction</td>
</tr>
<tr>
<td>19</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 19th ALU Instruction</td>
</tr>
<tr>
<td>18</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 18th ALU Instruction</td>
</tr>
<tr>
<td>17</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 17th ALU Instruction</td>
</tr>
<tr>
<td>16</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 16th ALU Instruction</td>
</tr>
<tr>
<td>15</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 15th ALU Instruction</td>
</tr>
<tr>
<td>14</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 14th ALU Instruction</td>
</tr>
<tr>
<td>13</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 13th ALU Instruction</td>
</tr>
<tr>
<td>12</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 12th ALU Instruction</td>
</tr>
<tr>
<td>11</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 11th ALU Instruction</td>
</tr>
<tr>
<td>10</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 10th ALU Instruction</td>
</tr>
<tr>
<td>9</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 9th ALU Instruction</td>
</tr>
<tr>
<td>8</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 8th ALU Instruction</td>
</tr>
<tr>
<td>7</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 7th ALU Instruction</td>
</tr>
<tr>
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<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 6th ALU Instruction</td>
</tr>
<tr>
<td>5</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 5th ALU Instruction</td>
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<tr>
<td>4</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 4th ALU Instruction</td>
</tr>
<tr>
<td>3</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 3rd ALU Instruction</td>
</tr>
<tr>
<td>2</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 2nd ALU Instruction</td>
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<tr>
<td>1</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 1st ALU Instruction</td>
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<tr>
<td>0</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 0th ALU Instruction</td>
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### Pixel Shader Setting 7

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 23          | WO        | xxh     | Instruction Switch from ALU to TAU after the 47th ALU Instruction  
0: Operate next ALU instruction  
1: Switch to operate TAU instruction |
| 22          | WO        | xxh     | Instruction Switch from ALU to TAU after the 46th ALU Instruction |
| 21          | WO        | xxh     | Instruction Switch from ALU to TAU after the 45th ALU Instruction |
| 20          | WO        | xxh     | Instruction Switch from ALU to TAU after the 44th ALU Instruction |
| 19          | WO        | xxh     | Instruction Switch from ALU to TAU after the 43rd ALU Instruction |
| 18          | WO        | xxh     | Instruction Switch from ALU to TAU after the 42nd ALU Instruction |
| 17          | WO        | xxh     | Instruction Switch from ALU to TAU after the 41st ALU Instruction |
| 16          | WO        | xxh     | Instruction Switch from ALU to TAU after the 40th ALU Instruction |
| 15          | WO        | xxh     | Instruction Switch from ALU to TAU after the 39th ALU Instruction |
| 14          | WO        | xxh     | Instruction Switch from ALU to TAU after the 38th ALU Instruction |
| 13          | WO        | xxh     | Instruction Switch from ALU to TAU after the 37th ALU Instruction |
| 12          | WO        | xxh     | Instruction Switch from ALU to TAU after the 36th ALU Instruction |
| 11          | WO        | xxh     | Instruction Switch from ALU to TAU after the 35th ALU Instruction |
| 10          | WO        | xxh     | Instruction Switch from ALU to TAU after the 34th ALU Instruction |
| 9           | WO        | xxh     | Instruction Switch from ALU to TAU after the 33rd ALU Instruction |
| 8           | WO        | xxh     | Instruction Switch from ALU to TAU after the 32nd ALU Instruction |
| 7           | WO        | xxh     | Instruction Switch from ALU to TAU after the 31st ALU Instruction |
| 6           | WO        | xxh     | Instruction Switch from ALU to TAU after the 30th ALU Instruction |
| 5           | WO        | xxh     | Instruction Switch from ALU to TAU after the 29th ALU Instruction |
| 4           | WO        | xxh     | Instruction Switch from ALU to TAU after the 28th ALU Instruction |
| 3           | WO        | xxh     | Instruction Switch from ALU to TAU after the 27th ALU Instruction |
| 2           | WO        | xxh     | Instruction Switch from ALU to TAU after the 26th ALU Instruction |
| 1           | WO        | xxh     | Instruction Switch from ALU to TAU after the 25th ALU Instruction |
| 0           | WO        | xxh     | Instruction Switch from ALU to TAU after the 24th ALU Instruction |

### Pixel Shader Setting 8

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 23          | WO        | xxh     | Instruction Switch from ALU to TAU after the 71st ALU Instruction  
0: Operate next ALU instruction  
1: Switch to operate TAU instruction |
| 22          | WO        | xxh     | Instruction Switch from ALU to TAU after the 70th ALU Instruction |
| 21          | WO        | xxh     | Instruction Switch from ALU to TAU after the 69th ALU Instruction |
| 20          | WO        | xxh     | Instruction Switch from ALU to TAU after the 68th ALU Instruction |
| 19          | WO        | xxh     | Instruction Switch from ALU to TAU after the 67th ALU Instruction |
| 18          | WO        | xxh     | Instruction Switch from ALU to TAU after the 66th ALU Instruction |
| 17          | WO        | xxh     | Instruction Switch from ALU to TAU after the 65th ALU Instruction |
| 16          | WO        | xxh     | Instruction Switch from ALU to TAU after the 64th ALU Instruction |
| 15          | WO        | xxh     | Instruction Switch from ALU to TAU after the 63rd ALU Instruction |
| 14          | WO        | xxh     | Instruction Switch from ALU to TAU after the 62nd ALU Instruction |
| 13          | WO        | xxh     | Instruction Switch from ALU to TAU after the 61st ALU Instruction |
| 12          | WO        | xxh     | Instruction Switch from ALU to TAU after the 60th ALU Instruction |
| 11          | WO        | xxh     | Instruction Switch from ALU to TAU after the 59th ALU Instruction |
| 10          | WO        | xxh     | Instruction Switch from ALU to TAU after the 58th ALU Instruction |
| 9           | WO        | xxh     | Instruction Switch from ALU to TAU after the 57th ALU Instruction |
| 8           | WO        | xxh     | Instruction Switch from ALU to TAU after the 56th ALU Instruction |
| 7           | WO        | xxh     | Instruction Switch from ALU to TAU after the 55th ALU Instruction |
| 6           | WO        | xxh     | Instruction Switch from ALU to TAU after the 54th ALU Instruction |
| 5           | WO        | xxh     | Instruction Switch from ALU to TAU after the 53rd ALU Instruction |
| 4           | WO        | xxh     | Instruction Switch from ALU to TAU after the 52nd ALU Instruction |
| 3           | WO        | xxh     | Instruction Switch from ALU to TAU after the 51st ALU Instruction |
| 2           | WO        | xxh     | Instruction Switch from ALU to TAU after the 50th ALU Instruction |
| 1           | WO        | xxh     | Instruction Switch from ALU to TAU after the 49th ALU Instruction |
| 0           | WO        | xxh     | Instruction Switch from ALU to TAU after the 48th ALU Instruction |
### Pixel Shader Setting 9

<table>
<thead>
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<td></td>
<td>0: Operate next ALU instruction</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Switch to operate TAU instruction</td>
</tr>
<tr>
<td>23</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 94th ALU Instruction</td>
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<tr>
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<td>Instruction Switch from ALU to TAU after the 93rd ALU Instruction</td>
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<td>Instruction Switch from ALU to TAU after the 92nd ALU Instruction</td>
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<td>Instruction Switch from ALU to TAU after the 91st ALU Instruction</td>
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<tr>
<td>19</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 90th ALU Instruction</td>
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<tr>
<td>18</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 89th ALU Instruction</td>
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<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 88th ALU Instruction</td>
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<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 87th ALU Instruction</td>
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<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 86th ALU Instruction</td>
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<td>Instruction Switch from ALU to TAU after the 85th ALU Instruction</td>
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<td>Instruction Switch from ALU to TAU after the 84th ALU Instruction</td>
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<td>Instruction Switch from ALU to TAU after the 83rd ALU Instruction</td>
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<td>Instruction Switch from ALU to TAU after the 82nd ALU Instruction</td>
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<td>Instruction Switch from ALU to TAU after the 81st ALU Instruction</td>
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<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 80th ALU Instruction</td>
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<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 79th ALU Instruction</td>
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<td>Instruction Switch from ALU to TAU after the 78th ALU Instruction</td>
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<td>Instruction Switch from ALU to TAU after the 77th ALU Instruction</td>
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<td>Instruction Switch from ALU to TAU after the 76th ALU Instruction</td>
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<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 75th ALU Instruction</td>
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<td>Instruction Switch from ALU to TAU after the 74th ALU Instruction</td>
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<td>Instruction Switch from ALU to TAU after the 73rd ALU Instruction</td>
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<td>Instruction Switch from ALU to TAU after the 72nd ALU Instruction</td>
</tr>
<tr>
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### Pixel Shader Setting 10

<table>
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<td>Instruction Switch from ALU to TAU after the 119th ALU Instruction</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Operate next ALU instruction</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Switch to operate TAU instruction</td>
</tr>
<tr>
<td>23</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 118th ALU Instruction</td>
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<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 117th ALU Instruction</td>
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<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 116th ALU Instruction</td>
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<td>Instruction Switch from ALU to TAU after the 115th ALU Instruction</td>
</tr>
<tr>
<td>19</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 114th ALU Instruction</td>
</tr>
<tr>
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<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 113th ALU Instruction</td>
</tr>
<tr>
<td>17</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 112th ALU Instruction</td>
</tr>
<tr>
<td>16</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 111th ALU Instruction</td>
</tr>
<tr>
<td>15</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 110th ALU Instruction</td>
</tr>
<tr>
<td>14</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 109th ALU Instruction</td>
</tr>
<tr>
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<td>Instruction Switch from ALU to TAU after the 108th ALU Instruction</td>
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<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 107th ALU Instruction</td>
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<tr>
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<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 106th ALU Instruction</td>
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<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 105th ALU Instruction</td>
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<tr>
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<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 104th ALU Instruction</td>
</tr>
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<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 103rd ALU Instruction</td>
</tr>
<tr>
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<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 102nd ALU Instruction</td>
</tr>
<tr>
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<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 101st ALU Instruction</td>
</tr>
<tr>
<td>5</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 100th ALU Instruction</td>
</tr>
<tr>
<td>4</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 99th ALU Instruction</td>
</tr>
<tr>
<td>3</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 98th ALU Instruction</td>
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<tr>
<td>2</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 97th ALU Instruction</td>
</tr>
<tr>
<td>1</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 96th ALU Instruction</td>
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<tr>
<td>0</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 95th ALU Instruction</td>
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### HParaType = 01h, Sub-Address = 9Ah

#### Pixel Shader Setting 11

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
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<th>Description</th>
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<tr>
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<td>Temporary Register 15(r15)'s Initial Setting for Destination Check Bit</td>
</tr>
<tr>
<td>22</td>
<td>WO</td>
<td>xxh</td>
<td>Temporary Register 14(r14)'s Initial Setting for Destination Check Bit</td>
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<td>Temporary Register 13(r13)'s Initial Setting for Destination Check Bit</td>
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<td>Temporary Register 12(r12)'s Initial Setting for Destination Check Bit</td>
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<td>Temporary Register 11(r11)'s Initial Setting for Destination Check Bit</td>
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<td>xxh</td>
<td>Temporary Register 10(r10)'s Initial Setting for Destination Check Bit</td>
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<td>WO</td>
<td>xxh</td>
<td>Temporary Register 9(r9)'s Initial Setting for Destination Check Bit</td>
</tr>
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<td>WO</td>
<td>xxh</td>
<td>Temporary Register 8(r8)'s Initial Setting for Destination Check Bit</td>
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<td>WO</td>
<td>xxh</td>
<td>Temporary Register 7(r7)'s Initial Setting for Destination Check Bit</td>
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<td>14</td>
<td>WO</td>
<td>xxh</td>
<td>Temporary Register 6(r6)'s Initial Setting for Destination Check Bit</td>
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<td>13</td>
<td>WO</td>
<td>xxh</td>
<td>Temporary Register 5(r5)'s Initial Setting for Destination Check Bit</td>
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<td>WO</td>
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<td>Temporary Register 4(r4)'s Initial Setting for Destination Check Bit</td>
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<td>WO</td>
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<td>Temporary Register 3(r3)'s Initial Setting for Destination Check Bit</td>
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<td>WO</td>
<td>xxh</td>
<td>Temporary Register 2(r2)'s Initial Setting for Destination Check Bit</td>
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<td>WO</td>
<td>xxh</td>
<td>Temporary Register 1(r1)'s Initial Setting for Destination Check Bit</td>
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<tr>
<td>8</td>
<td>WO</td>
<td>xxh</td>
<td>Temporary Register 0(r0)'s Initial Setting for Destination Check Bit</td>
</tr>
</tbody>
</table>

0: It is not necessary to check r0's valid bit whenever used as ALU’s destination at the 1st time.  
1: It is necessary to check r0’s valid bit whenever used as ALU’s destination at the 1st time.

**Note to Driver:** Define HPSRnDstChk for PS’s temporary register n. The default value is “0”. If some temporary register is as both TAU and ALU’s destination when 1st used, the HPSRnDstChk must be set as “1”. Hardware would check r#’s valid bit to see if data from “txld” is valid or not before the ALU instruction which uses r# as “partial” destination. Here are some examples:

```
txld r0, t0;  
mov r0.a c0.a;  
........
```

or

```
txld r0, t0;  
txld r1, t1;  
mov r2, r1  
mov r0.a, c0.a;  
........
```

The HPSR0DstChk must be set as “1” by driver. It is very, very important, wrong setting would lead to wrong result.

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 127th ALU Instruction</td>
</tr>
<tr>
<td>6</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 126th ALU Instruction</td>
</tr>
<tr>
<td>5</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 125th ALU Instruction</td>
</tr>
<tr>
<td>4</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 124th ALU Instruction</td>
</tr>
<tr>
<td>3</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 123rd ALU Instruction</td>
</tr>
<tr>
<td>2</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 122nd ALU Instruction</td>
</tr>
<tr>
<td>1</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 121st ALU Instruction</td>
</tr>
<tr>
<td>0</td>
<td>WO</td>
<td>xxh</td>
<td>Instruction Switch from ALU to TAU after the 120th ALU Instruction</td>
</tr>
</tbody>
</table>

### HParaType = 01h, Sub-Address = AAh

#### Software Inspection

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:16</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>13:0</td>
<td>WO</td>
<td>xxh</td>
<td>Flag Number for Software Inspection</td>
</tr>
</tbody>
</table>
HPaParaType 02h: Attribute of Texture Stage N (HPaParaSubType: 00-0Fh)

The register table in this section is used for following HPaParaSubTypes (from 00h to 0Fh).

- **HPaParaSubType = 0000 0000 (00h) -- For Texture 0**
- **HPaParaSubType = 0000 0001 (01h) -- For Texture 1**
- **HPaParaSubType = 0000 0010 (02h) -- For Texture 2**
- **HPaParaSubType = 0000 0011 (03h) -- For Texture 3**
- **HPaParaSubType = 0000 0100 (04h) -- For Texture 4**
- **HPaParaSubType = 0000 0101 (05h) -- For Texture 5**
- **HPaParaSubType = 0000 0110 (06h) -- For Texture 6**
- **HPaParaSubType = 0000 0111 (07h) -- For Texture 7**
- **HPaParaSubType = 0000 1000 (08h) -- For Texture 8**
- **HPaParaSubType = 0000 1001 (09h) -- For Texture 9**
- **HPaParaSubType = 0000 1010 (0Ah) -- For Texture A**
- **HPaParaSubType = 0000 1011 (0Bh) -- For Texture B**
- **HPaParaSubType = 0000 1100 (0Ch) -- For Texture C**
- **HPaParaSubType = 0000 1101 (0Dh) -- For Texture D**
- **HPaParaSubType = 0000 1110 (0Eh) -- For Texture E**
- **HPaParaSubType = 0000 1111 (0Fh) -- For Texture F**

**Sub-Address (Bits [31:24]): 00-51h**

**HPaParaType = 02h (HPaParaSubType = 00h-0Fh), Sub-Address = 00h**

**Face 0 Level 0 Base Address**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 23:0        | WO        | xxh     | Face 0’s Level 0 Base Address  
This is A31 to A8 in unit of 256 bytes. |

**HPaParaType = 02h (HPaParaSubType = 00h-0Fh), Sub-Address = 01h**

**Face 1 Level 0 Base Address**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 23:0        | WO        | xxh     | Face 1’s Level 0 Base Address  
This is A31 to A8 in unit of 256 bytes. |

**HPaParaType = 02h (HPaParaSubType = 00h-0Fh), Sub-Address = 02h**

**Face 2 Level 0 Base Address**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 23:0        | WO        | xxh     | Face 2’s Level 0 Base Address  
This is A31 to A8 in unit of 256 bytes. Program it back to 0. |

**HPaParaType = 02h (HPaParaSubType = 00h-0Fh), Sub-Address = 03h**

**Face 3 Level 0 Base Address**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 23:0        | WO        | xxh     | Face 3’s Level 0 Base Address  
This is A31 to A8 in unit of 256 bytes. |

**HPaParaType = 02h (HPaParaSubType = 00h-0Fh), Sub-Address = 04h**

**Face 4 Level 0 Base Address**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 23:0        | WO        | xxh     | Face 4’s Level 0 Base Address  
This is A31 to A8 in unit of 256 bytes. |
# HParaType = 02h (HParaSubType = 00h-0Fh), Sub-Address = 05h

## Face 5 Level 0 Base Address

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:0</td>
<td>WO</td>
<td>xxh</td>
<td>Face 5's Level 0 Base Address in unit of 256 bytes. This is A31 to A8.</td>
</tr>
</tbody>
</table>

## HParaType = 02h (HParaSubType = 00h-0Fh), Sub-Address = 06-17h: Reserved

## HParaType = 02h (HParaSubType = 00h-0Fh), Sub-Address = 18h

### Texture Control 1

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23</td>
<td>WO</td>
<td>xxh</td>
<td>Force Miss for Texture n’s Texture Cache Hit Detection</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Detect hit or miss normally</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Always force to miss</td>
</tr>
<tr>
<td>22:18</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>17:16</td>
<td>WO</td>
<td>xxh</td>
<td>Texture Location of Face0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: System Local Frame Buffer (S.L.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: System Dynamic Frame Buffer (S.F.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: Reserved (System Memory)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: Reserved</td>
</tr>
<tr>
<td>15:14</td>
<td>WO</td>
<td>xxh</td>
<td>Texture Location of Face0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: System Local Frame Buffer (S.L.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: System Dynamic Frame Buffer (S.F.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: Reserved (System Memory)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: Reserved</td>
</tr>
<tr>
<td>13</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>12</td>
<td>WO</td>
<td>xxh</td>
<td>Base Address Mode for Texture Sample N</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: HTXnLOmOffset is not offset related to Level 0, but an independent Base Address of Level m.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: This mode is for cubic texture and planner mode texture Base Address of Level m = HTXnFL0Bas + HTXnLOmOffset</td>
</tr>
<tr>
<td>11:8</td>
<td>WO</td>
<td>xxh</td>
<td>Mode of Texture N</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0000: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0001: 2 Dimension, both S and T coordinates.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0011: Cube texture</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1xxx: Projection texture</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Others: Reserved</td>
</tr>
<tr>
<td>7:6</td>
<td>WO</td>
<td>xxh</td>
<td>Texture Location of Face0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: System Local Frame Buffer (S.L.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: System Dynamic Frame Buffer (S.F.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: Reserved (System Memory)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: Reserved</td>
</tr>
<tr>
<td>5:4</td>
<td>WO</td>
<td>xxh</td>
<td>Texture Location of Face2 or Cr Buffer for Y-Cb-Cr Format</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: System Local Frame Buffer (S.L.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: System Dynamic Frame Buffer (S.F.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: Reserved (System Memory)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: Reserved</td>
</tr>
<tr>
<td>3:2</td>
<td>WO</td>
<td>xxh</td>
<td>Texture Location of Face1, Cb Buffer for Y-Cb-Cr Format, or Crb Buffer for Y-Crb Format</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: System Local Frame Buffer (S.L.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: System Dynamic Frame Buffer (S.F.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: Reserved (System Memory)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: Reserved</td>
</tr>
<tr>
<td>1:0</td>
<td>WO</td>
<td>xxh</td>
<td>Texture Location of Face0 or Y Buffer for Y-Cb-Cr or Y-Crb Format</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: System Local Frame Buffer (S.L.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: System Dynamic Frame Buffer (S.F.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: Reserved (System Memory)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: Reserved</td>
</tr>
</tbody>
</table>

**The procedure to determine the location of accessed texture:**

Consider fetch the texture with level "l" of texture stage "n"’s face "f"

\[
\text{LOC} = \begin{cases} 
\text{HTXnFL0LOC} & \text{if } \text{HTXnBaseMode} == 1 \text{ and } \text{HTXnPower2} == 1 \\
\text{HTXnF0LOC} & \text{else}
\end{cases}
\]

**3D Registers**
HParaType = 02h (HParaSubType = 00h-0Fh), Sub-Address = 19-1Fh: Reserved (Texture Control)

HParaType = 02h (HParaSubType = 00h-0Fh), Sub-Address = 20h
Texture Control 2

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:12</td>
<td>WO xxh</td>
<td>Height of Texture Level 0</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>The height of each level is calculated from HTXSnL0H Height at Level “l” = HTXSnL0H &gt;&gt; l. Maximum is 2048.</td>
<td></td>
</tr>
<tr>
<td>11:0</td>
<td>WO xxh</td>
<td>Width of Texture Level 0</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>The Width of each level is calculated from HTXSnL0W Width at Level “l” = HTXSnL0W &gt;&gt; l. Maximum is 2048.</td>
<td></td>
</tr>
</tbody>
</table>

HParaType = 02h (HParaSubType = 00h-0Fh), Sub-Address = 21h
Texture Control 3

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:12</td>
<td>WO xxh</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>11:0</td>
<td>WO xxh</td>
<td>Length of Texture Level 0, Maximum to 2048 (for 3D Volume Texture's R Axis)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>The Length of each level is calculated from HTXSnL0L Length at Level “l” = HTXSnL0L &gt;&gt; l, but NO MIP for 3D volume texture.</td>
<td></td>
</tr>
</tbody>
</table>

HParaType = 02h (HParaSubType = 00h-0Fh), Sub-Address = 22h
Texture Control 4

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:18</td>
<td>WO xxh</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>WO xxh</td>
<td>Memory Mode of Texture N</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: Linear mode</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Tile mode</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>WO xxh</td>
<td>Texture N’s Tile Is 16-texel High</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: Normal 8-texel high</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: 16-texel high</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>WO xxh</td>
<td>Texture N’s Width and Height Are Both Power of 2</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: Non-power of 2 texture</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Power of 2 texture</td>
<td></td>
</tr>
<tr>
<td>14:12</td>
<td>WO xxh</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>11:8</td>
<td>WO xxh</td>
<td>Exponential of Length of Texture N Level 0</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Maximum is up to 11(2^11).</td>
<td></td>
</tr>
<tr>
<td>7:4</td>
<td>WO xxh</td>
<td>Exponential of Height of Texture N Level 0</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Maximum is up to 11(2^11).</td>
<td></td>
</tr>
<tr>
<td>3:0</td>
<td>WO xxh</td>
<td>Exponential of Width of Texture N Level 0</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Maximum is up to 11(2^11).</td>
<td></td>
</tr>
</tbody>
</table>

HParaType = 02h (HParaSubType = 00h-0Fh), Sub-Address = 23-2Fh: Reserved (Texture Control)
### Texture Control 5

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:16</td>
<td>WO</td>
<td>xxh</td>
<td>Texture Format</td>
</tr>
</tbody>
</table>

**Bit [23:19]:**

- 00000: Reserved
- 00001: Intensity format
  - R, G, B ≤ I
  - A ≤ 1.0
- 00010: Luminance format
  - R, G, B ≤ L
  - A ≤ 1.0 or A
- 00011: Alpha format
  - R, G, B ≤ 0.0
  - A ≤ A
- 00100: Reserved
- 00101: Compressed texture
- 00110: YUV (Video texture) format
- 00111: Format for BumpMapping
- 11111-01000: Reserved
- 10000: Reserved
- 10001: ARGB_16bpp format
- 10010: Reserved
- 10011: ARGB_32bpp format
- 10100: Reserved
- 10101: ABGR_16bpp format
- 10110: Reserved
- 10111: ABGR_32bpp format
- 11000: Reserved
- 11001: RGBA_16bpp format
- 11010: Reserved
- 11011: RGBA_32bpp format
- 11100: BGRA_16bpp format
- 11101: BGRA_32bpp format
- 11110: Floating Color format
- 11111: Scale ( Said Z format or only one component)  
  *If there is NO Alpha channel in the defined format, fill 1.0 as Alpha value.*

**Bit [18:16]:**

**For Intensity Format:**

- 000: Reserved
- 001: Reserved
- 010: T4 (Bits [3:0] = T)
- 011: T8 (Bits [7:0] = T)
- 1xx: Reserved

**For Luminance Format:**

- 000: Reserved
- 001: Reserved
- 010: L4 (Bits [3:0] = L)
- 011: L8 (Bits [7:0] = L)
- 110: L16 (Bits [15:0] = L)
  
  **For L16 Format:**
  
  - A = 1.0f
  - R = G = B = float (L/65536)
  - // if (L = FFFFh) R = G = B = 1.0
  - // else
  - // fill “0” into mantissa
  - 111: Reserved

**For Alpha Format:**

- 000: Reserved
- 001: Reserved
- 010: A4 (Bits [3:0] = A)
- 011: A8 (Bits [7:0] = A)
- R = G = B = 0.0
- 1xx: Reserved
For Compressed Format:
000: Reserved
001: DXT1, 16-bpp format
010: DXT2, DXT3, 4-bit Alpha format
011: DXT4, DXT5, 3-bit Alpha format
100-101: Reserved
The G8R8, G8B8 can be defined by set as YUV format’s package mode and set HTXnYUV2RGBmode to RGB mode

For YUV format (Video Texture):
010: IA44 (Bits [7:4] = I as a 16 entries index to get a Y(R)8U(G)8V(B)8 texel, Bits [3:0] = A. A does not come from palette)
011: AI44 (Bits [7:4] = A. A does not come from palette, Bits [3:0] = I as a 16 entries index to get a Y(R)8U(G)8V(B)8 texel)
100-101: Reserved

For BumpMapping Format (Reserved):
000: VU88 (Bits [15:8] = dV, Bits [7:0] = dU)
100: VU16 (Bits [31:16] = dV, Bits [15:0] = dU)
110: CVUx88 Reserved
111: Reserved

For ARGB_16bpp Format:
100: Reserved
11x: Reserved

For ARGB_32bpp Format:
011: G16R16 (Bits [31:16] = G, Bits [15:0] = R) for this format, A = B = 1.0f, G and R are transformed to s[7].16
1xx: Reserved

For ABGR_16bpp Format:
100: Reserved
11x: Reserved

For ABGR_32bpp Format:
011-111: Reserved

For RGBA_16bpp Format:
100: Reserved
11x: Reserved

For RGBA_32bpp Format:
### 3D Registers

<table>
<thead>
<tr>
<th>Code</th>
<th>Description</th>
</tr>
</thead>
</table>

- **011-111**: Reserved

**For ABGR_16bpp Format:**
- **100**: Reserved
- **11x**: Reserved

**For BGRA_32bpp Format:**
- **011-11**: Reserved

**For Floating Color Format (Filter not supported):**
- **000**: R16F (Bits [15:0] = R) s[5].10
  - A = G = B = 1.0f, and R is extended to s[7].16 with “0”.
  - A = B = 1.0f, R and G are extended to s[7].16 with “0”.
- **101**: R32F (Bits [31:0] = R) s[8].23
  - A = G = B = 1.0f, and R is clamped to s[7].16 (saturation)
- **111**: Reserved

**For Z Format:**
- **000**: 16-bit fixed-point format, 0.0 ≤ Z < 1.0
  - **001**: 16-bit floating format s[5].10 from +2^63*1.FFFF to –2^63*1.FFFF. <*>Only Nearest>
- **010-011**: Reserved
- **100**: 32-bit fixed-point format, 0.0 ≤ Z < 1.0. <*>Only Nearest>
- **101**: 32-bit floating format s[8].23. <*>Only Nearest>
- **110**: 24-bit fixed-point format Z, 0.0 ≤ Z < 1.0, and Stencil. <*>Only Nearest>
  - Z is located in D[31:8], Stencil is located in D[7:0]
- **111**: Reserved

### Texture Color Extending Mode (Excluding Alpha)

- **0**: Extending with high color bit.
- **1**: For Alpha channel, always extend it with high color bit.
- For YUV format (video texture) and when HTxYUV2RGBmode set as 0, always extend it with zero.
- 0: Extending with high color bit.

### Inverse the Texel Order in One Byte for Those Texture with 1bpp, 2bpp or 3bpp

- **0**: Normal
  - Consider Index 1:
  - Consider Index 2:
  - Consider Index 4:
- **1**: Inverse
  - Consider Index 1:
  - Consider Index 2:
  - Consider Index 4:
### Mode for Z (Depth) Format Texture

#### 000: D3D Mode
- \( R = 0.0 \)
- \( G = Z \)
- \( B = 0.0 \)
- \( A = 1.0 \)

#### 010: Luminance mode
- \( R = Z \)
- \( G = Z \)
- \( B = Z \)
- \( A = 1.0 \)

#### 100: Intensity mode
- \( R = Z \)
- \( G = Z \)
- \( B = Z \)
- \( A = Z \)

#### 110: Alpha mode
- \( R = 0.0 \)
- \( G = 0.0 \)
- \( B = 0.0 \)
- \( A = Z \)

Note to OpenGL Driver: For Depth texture’s border color, please set the \( R, G, B, A \) component to HTXSnTBR, HTXSnTBG, HTXSnTBB and HTXSnTBA separately. Although ICD defines the 1st component of texture border color as the “Depth” value, HW would just adopts HTXSnTBR, HTXSnTBG, HTXSnTBB and HTXSnTBA, not matter what the HTXnMode’s setting is.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>10:9</td>
<td>WO xxh</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>WO xxh</td>
<td>Texture Is as sRGB (Non-gamma 1.0)</td>
<td></td>
</tr>
<tr>
<td>7:2</td>
<td>WO xxh</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>1:0</td>
<td>WO xxh</td>
<td>Video Texture Is as BT601(SDTV), BT709(HDTV) or Just RGB</td>
<td></td>
</tr>
</tbody>
</table>

#### Texture Is as sRGB (Non-gamma 1.0)

The DeGamma correction is necessary for DeGamma table “HDGTRTX”. DeGamma correction is only used to \( R, G \) and \( B \) component. Any color format could be DeGammaed just after the filtering (& color space conversion).

- 0: Disable DeGamma
- 1: Enable DeGamma

#### Video Texture Is as BT601(SDTV), BT709(HDTV) or Just RGB

- 00: RGB
  - For this format, consider the 8-bit \( Y \) as positive 8-bit \( G \), 8-bit \( U \) as positive 8-bit \( R \), and 8-bit \( V \) as positive 8-bit \( B \). Then extend them to s1.10 according to setting of HTXnCExtend. Then filter the texels.
  - For this setting, YUV2RGB transform is not done in format decoder module or YUV2RGB transformed implemented by PS.

- 01: BT601(SDTV)
  - \( R = \text{clip} \left( \text{round} \left( (Y - 16) \times 1.164383 + (U - 128) \times 1.596027 \times 256/255 \right) \right) \)
  - \( G = \text{clip} \left( \text{round} \left( (Y - 16) \times 1.164383 - (U - 128) \times 0.391762 - (V - 128) \times 0.812968 \times 256/255 \right) \right) \)
  - \( B = \text{clip} \left( \text{round} \left( (Y - 16) \times 1.164383 + (U - 128) \times 2.017232 \times 256/255 \right) \right) \)

- 10: BT709(HDTV)
  - \( R = \text{clip} \left( \text{round} \left( (Y - 16) \times 1.164383 - (U - 128) \times 0.0002 \times 256/255 \right) \right) \)
  - \( G = \text{clip} \left( \text{round} \left( (Y - 16) \times 1.164383 - (U - 128) \times 0.2132 \times 256/255 \right) \right) \)
  - \( B = \text{clip} \left( \text{round} \left( (Y - 16) \times 1.164383 + (U - 128) \times 0.5329 \times 256/255 \right) \right) \)

For 8-bit YUV

- \( R = \text{clip} \left( \text{round} \left( (Y \times A + U \times B1 + V \times C1 + D) \times 256/255 \right) \right) \)
- \( G = \text{clip} \left( \text{round} \left( (Y \times A + U \times B2 + V \times C2 + D) \times 256/255 \right) \right) \)
- \( B = \text{clip} \left( \text{round} \left( (Y \times A + U \times B3 + V \times C3 + D) \times 256/255 \right) \right) \)

For 10-bit YUV

- \( R = \text{clip} \left( \text{round} \left( (Y \times A + U \times B1 + V \times C1 + D) \times 1024/1023 \right) \right) \)
- \( G = \text{clip} \left( \text{round} \left( (Y \times A + U \times B2 + V \times C2 + D) \times 1024/1023 \right) \right) \)
- \( B = \text{clip} \left( \text{round} \left( (Y \times A + U \times B3 + V \times C3 + D) \times 1024/1023 \right) \right) \)

### Software Inspection for Texture N – 1st Flag Number

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[23:0]</td>
<td>Attribute</td>
<td>Default</td>
<td>Description</td>
</tr>
<tr>
<td>23:16</td>
<td>WO xxh</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>15:0</td>
<td>WO xxh</td>
<td>Texture N's 1st Flag Number for SW inspection</td>
<td></td>
</tr>
</tbody>
</table>
HParaType = 02h (HParaSubType = 00h-0Fh), Sub-Address = 51h
Software Inspection for Texture N – 2nd Flag Number

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[23:0]</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>23:16</td>
<td>WO</td>
<td>xxh</td>
<td>Texture n’s 2nd Flag Number for SW inspection</td>
</tr>
</tbody>
</table>
HParaType 02h: Attribute of Texture Sample Stage N (HParaSubType: 20-2Fh)

The register table in this section is used for the following HParaSubTypes (from 20h to 2Fh).

- HParaSubType = 0010 0000 (20h) For Texture Sample 0
- HParaSubType = 0010 0001 (21h) For Texture Sample 1
- HParaSubType = 0010 0010 (22h) For Texture Sample 2
- HParaSubType = 0010 0011 (23h) For Texture Sample 3
- HParaSubType = 0010 0100 (24h) For Texture Sample 4
- HParaSubType = 0010 0101 (25h) For Texture Sample 5
- HParaSubType = 0010 0110 (26h) For Texture Sample 6
- HParaSubType = 0010 0111 (27h) For Texture Sample 7
- HParaSubType = 0010 1000 (28h) For Texture Sample 8
- HParaSubType = 0010 1001 (29h) For Texture Sample 9
- HParaSubType = 0010 1010 (2Ah) For Texture Sample A
- HParaSubType = 0010 1011 (2Bh) For Texture Sample B
- HParaSubType = 0010 1100 (2Ch) For Texture Sample C
- HParaSubType = 0010 1101 (2Dh) For Texture Sample D
- HParaSubType = 0010 1110 (2Eh) For Texture Sample E
- HParaSubType = 0010 1111 (2Fh) For Texture Sample F

Sub-Address (Bits [31:24]): 00-51h

HParaType = 02h (HParaSubType = 20h-2Fh), Sub-Address = 00h-2Fh: Reserved

---

### Texture Level Control 1

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:22</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>21:12</td>
<td>WO</td>
<td>xxh</td>
<td>Texture Level 0 Offset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Format: 2's Complement fixed-point number with 5-bit integer and 5-bit fraction. The real Level 0 is (Texture Minimum Level + HTNxL0OS).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Bit [21:17]: 5-bit integer of Texture n Level 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Bit [16:12]: 5-bit fraction of Texture n Level 0</td>
</tr>
<tr>
<td>11:6</td>
<td>WO</td>
<td>xxh</td>
<td>Maximum Texture Level</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>000000: Texture n Maximum Level = 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>000001: Texture n Maximum Level = 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>000010: Texture n Maximum Level = 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>000011: Texture n Maximum Level = 3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>000100: Texture n Maximum Level = 4</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>000101: Texture n Maximum Level = 5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>000110: Texture n Maximum Level = 6</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>000111: Texture n Maximum Level = 7</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>001000: Texture n Maximum Level = 8</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>001001: Texture n Maximum Level = 9</td>
</tr>
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<td></td>
<td></td>
<td>001010: Texture n Maximum Level = A</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>001011: Texture n Maximum Level = B</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Others: Reserved</td>
</tr>
<tr>
<td>5:0</td>
<td>WO</td>
<td>xxh</td>
<td>Minimum Texture Level</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>000000: Texture n Minimum Level = 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>000001: Texture n Minimum Level = 1</td>
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<td>000010: Texture n Minimum Level = 2</td>
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<td>000011: Texture n Minimum Level = 3</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>000100: Texture n Minimum Level = 4</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>000101: Texture n Minimum Level = 5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>000110: Texture n Minimum Level = 6</td>
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<td>000111: Texture n Minimum Level = 7</td>
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<td>001000: Texture n Minimum Level = 8</td>
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<td>001001: Texture n Minimum Level = 9</td>
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<td>001010: Texture n Minimum Level = A</td>
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<td>001011: Texture n Minimum Level = B</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Others: Reserved</td>
</tr>
</tbody>
</table>
HParaType = 02h (HParaSubType = 20h-2Fh), Sub-Address = 31h
Texture Filter Control 1

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>[23:0]</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>20:16</td>
<td>WO</td>
<td>xxh</td>
<td>Maximum Ratio for Anisotropy (Maximum up to 16)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00000: Max ratio to 0 (no anisotropy)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00001: Max ratio to 1 (no anisotropy)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00010: Max ratio to 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00011: Max ratio to 3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00100: Max ratio to 4</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00101: Max ratio to 5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00110: Max ratio to 6</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00111: Max ratio to 7</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01000: Max ratio to 8</td>
</tr>
<tr>
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<td></td>
<td></td>
<td>01001: Max ratio to 9</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01010: Max ratio to 10</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01011: Max ratio to 11</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>01100: Max ratio to 12</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01101: Max ratio to 13</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01110: Max ratio to 14</td>
</tr>
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<td></td>
<td></td>
<td>01111: Max ratio to 15</td>
</tr>
<tr>
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<td></td>
<td></td>
<td>Others: Reserved</td>
</tr>
<tr>
<td>15:13</td>
<td>WO</td>
<td>xxh</td>
<td>Texture Filter Setting in S Direction for Texture Enlargement</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>000: Nearest</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>001: Linear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>010: Linear Anisotropy</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>011: 4x4 filter</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Others: Reserved</td>
</tr>
<tr>
<td>12:10</td>
<td>WO</td>
<td>xxh</td>
<td>Texture Filter Setting in S Direction for Texture Shrinking</td>
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<tr>
<td></td>
<td></td>
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<td>000: Nearest</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>001: Linear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>010: Linear Anisotropy</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>011: 4x4 filter</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Others: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>000: Nearest</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>001: Linear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>010: Linear Anisotropy</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>011: 4x4 filter</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Others: Reserved</td>
</tr>
</tbody>
</table>
* HTXSnFLTe & HTXSnFLSe must be the same when Linear Anisotropy is set. |
| 6:4           | WO        | xxh     | Texture Filter Setting in T Direction ForTexture Shrinking       |
|               |           |         | 000: Nearest                                                     |
|               |           |         | 001: Linear                                                      |
|               |           |         | 010: Linear Anisotropy                                           |
|               |           |         | 011: 4x4 filter                                                  |
|               |           |         | Others: Reserved                                                 |
* HTXSnFLTs & HTXSnFLSs must be the same when Linear Anisotropy is set. |
| 3:0           | WO        | xxh     | Texture Filter Setting in D Direction For Texture Shrinking      |
|               |           |         | 0000: Always uses Texture Level 0                                |
|               |           |         | 0001: Nearest                                                    |
|               |           |         | 0010: Linear                                                    |
|               |           |         | 0011: Reserved                                                   |
|               |           |         | 0100: Dither                                                     |
|               |           |         | Others: Reserved                                                 |

Preliminary Revision 1.0, July 29, 2009
### Texture Filter Control 2 & Texture Mapping Control

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:22</td>
<td>WO xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>21:19</td>
<td>WO xxh</td>
<td>Texture Filter Setting in R Direction for Texture Enlargement (Only for 3D Volume Texture)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>000: Nearest</td>
</tr>
<tr>
<td></td>
<td></td>
<td>001: Linear</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Others: Reserved</td>
</tr>
<tr>
<td>18:16</td>
<td>WO xxh</td>
<td>Texture Filter Setting in R Direction For Texture Shrinking (Only for 3D Volume Texture)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>000: Nearest</td>
</tr>
<tr>
<td></td>
<td></td>
<td>001: Linear</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Others: Reserved</td>
</tr>
<tr>
<td>15:12</td>
<td>WO xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>11:0</td>
<td>WO xxh</td>
<td>Texture Mapping Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bits [11:9]: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bits [8:6]: R Axis Setting (for 3D Volume texture)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>000: Border Color</td>
</tr>
<tr>
<td></td>
<td></td>
<td>001: Clamp</td>
</tr>
<tr>
<td></td>
<td></td>
<td>010: Repeat</td>
</tr>
<tr>
<td></td>
<td></td>
<td>011: Mirror</td>
</tr>
<tr>
<td></td>
<td></td>
<td>110-100: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td>111: Mirror Once</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bits [5:3]: T Axis Setting</td>
</tr>
<tr>
<td></td>
<td></td>
<td>000: Border Color</td>
</tr>
<tr>
<td></td>
<td></td>
<td>001: Clamp</td>
</tr>
<tr>
<td></td>
<td></td>
<td>010: Repeat</td>
</tr>
<tr>
<td></td>
<td></td>
<td>011: Mirror</td>
</tr>
<tr>
<td></td>
<td></td>
<td>110-100: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td>111: Mirror Once</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bits [2:0]: S Axis Setting</td>
</tr>
<tr>
<td></td>
<td></td>
<td>000: Border Color</td>
</tr>
<tr>
<td></td>
<td></td>
<td>001: Clamp</td>
</tr>
<tr>
<td></td>
<td></td>
<td>010: Repeat</td>
</tr>
<tr>
<td></td>
<td></td>
<td>011: Mirror</td>
</tr>
<tr>
<td></td>
<td></td>
<td>110-100: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td>111: Mirror Once</td>
</tr>
</tbody>
</table>

### Texture Border Control 1

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:12</td>
<td>WO xxh</td>
<td>Red Color or U Component of Texture Border</td>
</tr>
<tr>
<td></td>
<td></td>
<td>As s1.10 from –1.0 to 1.0</td>
</tr>
<tr>
<td>11:0</td>
<td>WO xxh</td>
<td>Green Color or Y Component of Texture Border</td>
</tr>
<tr>
<td></td>
<td></td>
<td>As s1.10 from –1.0 to 1.0</td>
</tr>
</tbody>
</table>
### Texture Border Control 2

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:12</td>
<td>WO</td>
<td>xxh</td>
<td>Blue Color or V Component of Texture Border (&lt;HTXSnTBB&gt;)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>As s1.10 from –1.0 to 1.0</td>
</tr>
<tr>
<td>11:0</td>
<td>WO</td>
<td>xxh</td>
<td>Texture Border Alpha (&lt;HTXSnTBA&gt;)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>As s1.10 from –1.0 to 1.0</td>
</tr>
</tbody>
</table>

**Note for texture border color’s usage:**
If any filtered texel is border color:
- A channel of filter output = HTXSnTBA
- R channel of filter output = HTXSnTBR
- G channel of filter output = HTXSnTBG
- B channel of filter output = HTXSnTBB
else if texel is border color:
- Use \([HTXSnTBR][11:0], HTXSnTBG[11:0]\) as border value with format .24
else:
- If (the texel is border color):
  - A channel of filter input of the texel = HTXSnTBA
  - R channel of filter input of the texel = HTXSnTBR
  - G channel of filter input of the texel = HTXSnTBG
  - B channel of filter input of the texel = HTXSnTBB
- else
  - A channel of filter input of the texel = A after “color extending”
  - R channel of filter input of the texel = R after “color extending”
  - G channel of filter input of the texel = G after “color extending”
  - B channel of filter input of the texel = B after “color extending”

**Note for YUV format and HTXnYUV2RGBmode is SDTV or HDTV, the border color is not in RGB space any more. It must be inverse transformed to YUV space as HTXSnTBG <= Y, HTXSnTBR <= U & HTXSnTBB <= V. And the HTXSnTBG[1:0], HTXSnTBG[1:0] & HTXSnTBR[1:0] are all zero.**

---

### HParaType = 02h (HParaSubType = 20h-2Fh), Sub-Address = 37-40h: Reserved

### HParaType = 02h (HParaSubType = 20h-2Fh), Sub-Address = 50h
**Software Inspection for Texture Sample N – 1st Flag Number**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:16</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>15:0</td>
<td>WO</td>
<td>xxh</td>
<td>Texture Sample n’s 1st Flag Number for SW Inspection</td>
</tr>
</tbody>
</table>

### HParaType = 02h (HParaSubType = 20h-2Fh), Sub-Address = 51h
**Software Inspection for Texture Sample N – 2nd Flag Number**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>10:0</td>
<td>WO</td>
<td>xxh</td>
<td>Texture Sample N’s 2nd Flag Number for SW Inspection</td>
</tr>
</tbody>
</table>
HParaType 02h: Attribute of Texture Stage N (HParaSubType: FEh)

The register tables in this section are used for HParaSubType (FEh).

Sub-Address (Bits [31:24]): 00-13h

HParaType = 02h (HParaSubType = FEh), Sub-Address = 00h

General Texture Attribute Control

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:8</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>7:4</td>
<td>WO</td>
<td>xxh</td>
<td>Number of Texture</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>n: n Texture, max up to 8</td>
</tr>
<tr>
<td>3:2</td>
<td>WO</td>
<td>xxh</td>
<td>Configuration of Data FIFO for Reading Texture</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: DFIFO1 is assigned to System memory’s 1st T-Arbitrator (SL)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>DFIFO2 is assigned to System memory’s 2nd T-Arbitrator (SF)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>DFIFO3 is assigned to Local Memory’s T-Arbitrator</td>
</tr>
<tr>
<td>1</td>
<td>WO</td>
<td>xxh</td>
<td>Fetch Texture 2 QWs (256 bits) or 4 QWs (512 bits) for Each Request</td>
</tr>
<tr>
<td>0</td>
<td>WO</td>
<td>xxh</td>
<td>Clear Texture Cache</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Don’t care</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Clear texture cache</td>
</tr>
</tbody>
</table>

HParaType = 02h (HParaSubType = FEh), Sub-Address = 01h

Attribute of Texture 0/1/2

Texture 0 to Texture 7 are defined for Primitive Engine.

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>22:21</td>
<td>WO</td>
<td>xxh</td>
<td>Perspective Mode of Texture 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: Enable perspective correction</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: Enable projection and be implemented to UVD module</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: Reserved</td>
</tr>
<tr>
<td>20:18</td>
<td>WO</td>
<td>xxh</td>
<td>Source of Texture 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>000: Texture comes from Texture A</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>001: Texture comes from Texture B</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>010: Texture comes from Texture C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>011: Texture comes from Texture D</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100: Texture comes from Texture E</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>101: Texture comes from Texture F</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>110: Texture comes from Texture G</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>111: Texture comes from Texture H</td>
</tr>
<tr>
<td>17:16</td>
<td>WO</td>
<td>xxh</td>
<td>Dimension of Texture 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: 1 dimension; only S coordinate</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: 2 dimensions; both S and T coordinates</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: 3 dimensions; volume texture; S, T, R coordinates</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: 4 dimensions; S, T, R, Q coordinates</td>
</tr>
<tr>
<td>14:13</td>
<td>WO</td>
<td>xxh</td>
<td>Perspective Mode of Texture 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: Enable perspective correction</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: Enable projection and be implemented to UVD module</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: Reserved</td>
</tr>
</tbody>
</table>
### Source of Texture 1
- 000: Texture comes from Texture A
- 001: Texture comes from Texture B
- 010: Texture comes from Texture C
- 011: Texture comes from Texture D
- 100: Texture comes from Texture E
- 101: Texture comes from Texture F
- 110: Texture comes from Texture G
- 111: Texture comes from Texture H

### Dimension of Texture 1
- 00: 1 dimension; only S coordinate
- 01: 2 dimensions; both S and T coordinates
- 10: 3 dimensions; volume texture; S, T, R coordinates
- 11: 4 dimensions; S, T, R, Q coordinates

### Perspective Mode of Texture 0
- 00: Disable
- 01: Enable perspective correction
- 10: Enable projection and be implemented to UVD module
- 11: Reserved

### Source of Texture 0
- 000: Texture comes from Texture A
- 001: Texture comes from Texture B
- 010: Texture comes from Texture C
- 011: Texture comes from Texture D
- 100: Texture comes from Texture E
- 101: Texture comes from Texture F
- 110: Texture comes from Texture G
- 111: Texture comes from Texture H

### Dimension of Texture 0
- 00: 1 dimension; only S coordinate
- 01: 2 dimensions; both S and T coordinates
- 10: 3 dimensions; volume texture; S, T, R coordinates
- 11: 4 dimensions; S, T, R, Q coordinates

### Perspective Mode of Texture 4
- 00: Disable
- 01: Enable perspective correction
- 10: Enable projection and be implemented to UVD module
- 11: Reserved

### Source of Texture 5
- 000: Texture comes from Texture A
- 001: Texture comes from Texture B
- 010: Texture comes from Texture C
- 011: Texture comes from Texture D
- 100: Texture comes from Texture E
- 101: Texture comes from Texture F
- 110: Texture comes from Texture G
- 111: Texture comes from Texture H

### Dimension of Texture 5
- 00: 1 dimension; only S coordinate
- 01: 2 dimensions; both S and T coordinates
- 10: 3 dimensions; volume texture; S, T, R coordinates
- 11: 4 dimensions; S, T, R, Q coordinates

### Perspective Mode of Texture 5
- 00: Disable
- 01: Enable perspective correction
- 10: Enable projection and be implemented to UVD module
- 11: Reserved

---

**HPaParaType = 02h (HPaParaSubType = FEh), Sub-Address = 02h**

### Attribute of Texture 3/4/5

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23</td>
<td>WO xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 22:21       | WO xxh            | Perspective Mode of Texture 5  
- 00: Disable  
- 01: Enable perspective correction  
- 10: Enable projection and be implemented to UVD module  
- 11: Reserved |
| 20:18       | WO xxh            | Source of Texture 5  
- 000: Texture comes from Texture A  
- 001: Texture comes from Texture B  
- 010: Texture comes from Texture C  
- 011: Texture comes from Texture D  
- 100: Texture comes from Texture E  
- 101: Texture comes from Texture F  
- 110: Texture comes from Texture G  
- 111: Texture comes from Texture H |
| 17:16       | WO xxh            | Dimension of Texture 5  
- 00: 1 dimension; only S coordinate  
- 01: 2 dimensions; both S and T coordinates  
- 10: 3 dimensions; volume texture; S, T, R coordinates  
- 11: 4 dimensions; S, T, R, Q coordinates |
| 15          | WO xxh            | Reserved    |
| 14:13       | WO xxh            | Perspective Mode of Texture 4  
- 00: Disable  
- 01: Enable perspective correction  
- 10: Enable projection and be implemented to UVD module  
- 11: Reserved |
<table>
<thead>
<tr>
<th>12:10 WO xxh</th>
<th>Source of Texture 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>000: Texture comes from Texture A</td>
<td></td>
</tr>
<tr>
<td>001: Texture comes from Texture B</td>
<td></td>
</tr>
<tr>
<td>010: Texture comes from Texture C</td>
<td></td>
</tr>
<tr>
<td>011: Texture comes from Texture D</td>
<td></td>
</tr>
<tr>
<td>100: Texture comes from Texture E</td>
<td></td>
</tr>
<tr>
<td>101: Texture comes from Texture F</td>
<td></td>
</tr>
<tr>
<td>110: Texture comes from Texture G</td>
<td></td>
</tr>
<tr>
<td>111: Texture comes from Texture H</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>9:8 WO xxh</th>
<th>Dimension of Texture 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>00: 1 dimension; only S coordinate</td>
<td></td>
</tr>
<tr>
<td>01: 2 dimensions; both S and T coordinates</td>
<td></td>
</tr>
<tr>
<td>10: 3 dimensions; volume texture; S, T, R coordinates</td>
<td></td>
</tr>
<tr>
<td>11: 4 dimensions; S, T, R, Q coordinates</td>
<td></td>
</tr>
</tbody>
</table>

| 7 WO xxh | Reserved |

<table>
<thead>
<tr>
<th>6:5 WO xxh</th>
<th>Perspective Mode of Texture 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>00: Disable</td>
<td></td>
</tr>
<tr>
<td>01: Enable perspective correction</td>
<td></td>
</tr>
<tr>
<td>10: Enable projection and be implemented to UVD module</td>
<td></td>
</tr>
<tr>
<td>11: Reserved</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>4:2 WO xxh</th>
<th>Source of Texture 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>000: Texture comes from Texture A</td>
<td></td>
</tr>
<tr>
<td>001: Texture comes from Texture B</td>
<td></td>
</tr>
<tr>
<td>010: Texture comes from Texture C</td>
<td></td>
</tr>
<tr>
<td>011: Texture comes from Texture D</td>
<td></td>
</tr>
<tr>
<td>100: Texture comes from Texture E</td>
<td></td>
</tr>
<tr>
<td>101: Texture comes from Texture F</td>
<td></td>
</tr>
<tr>
<td>110: Texture comes from Texture G</td>
<td></td>
</tr>
<tr>
<td>111: Texture comes from Texture H</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>1:0 WO xxh</th>
<th>Dimension of Texture 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>00: 1 dimension; only S coordinate</td>
<td></td>
</tr>
<tr>
<td>01: 2 dimensions; both S and T coordinates</td>
<td></td>
</tr>
<tr>
<td>10: 3 dimensions; volume texture; S, T, R coordinates</td>
<td></td>
</tr>
<tr>
<td>11: 4 dimensions; S, T, R, Q coordinates</td>
<td></td>
</tr>
</tbody>
</table>

HParaType = 02h (HParaSubType = FEh), Sub-Address = 03h

### Attribute of Texture 6/7

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:19 WO xxh</td>
<td>Threshold Value for Mip-map Linear Mode</td>
<td></td>
<td></td>
</tr>
<tr>
<td>18:15 WO xxh</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>14:13 WO xxh</td>
<td>Perspective Mode of Texture 7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12:10 WO xxh</td>
<td>Source of Texture 7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9:8 WO xxh</td>
<td>Dimension of Texture 7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7 WO xxh</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6:5 WO xxh</td>
<td>Perspective Mode of Texture 6</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### 4:2 WO xxh Source of Texture 6

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>Texture comes from Texture A</td>
</tr>
<tr>
<td>001</td>
<td>Texture comes from Texture B</td>
</tr>
<tr>
<td>010</td>
<td>Texture comes from Texture C</td>
</tr>
<tr>
<td>011</td>
<td>Texture comes from Texture D</td>
</tr>
<tr>
<td>100</td>
<td>Texture comes from Texture E</td>
</tr>
<tr>
<td>101</td>
<td>Texture comes from Texture F</td>
</tr>
<tr>
<td>110</td>
<td>Texture comes from Texture G</td>
</tr>
<tr>
<td>111</td>
<td>Texture comes from Texture H</td>
</tr>
</tbody>
</table>

### 1:0 WO xxh Dimension of Texture 6

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1 dimension; only S coordinate</td>
</tr>
<tr>
<td>1</td>
<td>2 dimensions; both S and T coordinates</td>
</tr>
<tr>
<td>10</td>
<td>3 dimensions; volume texture; S, T, R coordinates</td>
</tr>
<tr>
<td>11</td>
<td>4 dimensions; S, T, R, Q coordinates</td>
</tr>
</tbody>
</table>

---

### HParaType = 02h (HParaSubType = FEh), Sub-Address = 04h

#### Texture Coordinate Control

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:20</td>
<td>WO xxh</td>
<td></td>
<td>Exponential of Width for the Texture Coordinate Replaced by (x, y) ( s = x / 2^ HTXXYrpSTWE )</td>
</tr>
<tr>
<td>19:16</td>
<td>WO xxh</td>
<td></td>
<td>Exponential of High for the Texture Coordinate Replaced by (x, y) ( t = y / 2^ HTXXYrpSTHE )</td>
</tr>
<tr>
<td>15:8</td>
<td>WO xxh</td>
<td>Reserved</td>
<td></td>
</tr>
</tbody>
</table>
| 7:0         | WO xxh    |         | Use Screen Coordinates \((x, y)\) to Replace \((s, t)\) 
The value of bit[n] is used to control the setting of corresponding Texture[n]. (ex. bit[0] for Texture 0, bit[1] for Texture 1) 
0: Normal \((s,t)\) for Texture n 
1: Use \((x,y)\) to replace \((s,t)\) for Texture n |

---

### HParaType = 02h (HParaSubType = FEh), Sub-Address = 05h

#### User Defined Clipping Planes Control - 1st/2nd Groups

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:16</td>
<td>WO xxh</td>
<td>Reserved</td>
<td></td>
</tr>
</tbody>
</table>
| 15          | WO xxh    |         | Enable of 2nd Group of User Defined Clipping Planes \(<HTXUCP1Enable>\) 
0: Disable. No user defined clipping plane or only 1 texture is used for “User defined Clipping Plane”. 
1: Enable. A 2nd texture is used for “User defined Clipping Plane”. |
| 14          | WO xxh    |         | Perspective Mode of the Texture for 2nd Group of User Defined Clipping Planes 
0: Disable 
1: Enable perspective correction |
| 13:10       | WO xxh    |         | Source of the Texture for 2nd Group of User Defined Clipping Planes 
0000: Texture comes from Texture A 
0001: Texture comes from Texture B 
0010: Texture comes from Texture C 
0011: Texture comes from Texture D 
0100: Texture comes from Texture E 
0101: Texture comes from Texture F 
0110: Texture comes from Texture G 
0111: Texture comes from Texture H 
1000: Texture comes from Texture I 
1001: Texture comes from Texture J 
Others: Reserved |
| 9:8         | WO xxh    |         | Dimension of the Texture for 2nd Group of User Defined Clipping Planes 
00: 1 dimension; only S coordinate 
01: 2 dimensions; both S and T coordinates 
10: 3 dimensions; volume texture; S, T, R coordinates 
11: 4 dimensions; S, T, R, Q coordinates |
| 7           | WO xxh    |         | Enable of 1st Group of User Defined Clipping Planes \(<HTXUCP0Enable>\) 
0: Disable. No user defined clipping plane. 
1: Enable. A texture is used for “User defined Clipping Plane”. |
| 6           | WO xxh    |         | Perspective Mode of the Texture for 1st Group of User Defined Clipping Planes 
0: Disable 
1: Enable perspective correction |
### 5:2 WO xxh: Source of the Texture for 1st Group of User Defined Clipping Planes

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<td>Texture come from Texture B</td>
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<tr>
<td>0010</td>
<td>Texture come from Texture C</td>
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<tr>
<td>0011</td>
<td>Texture come from Texture D</td>
</tr>
<tr>
<td>0100</td>
<td>Texture come from Texture E</td>
</tr>
<tr>
<td>0101</td>
<td>Texture come from Texture F</td>
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<td>Texture come from Texture G</td>
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<td>0111</td>
<td>Texture come from Texture H</td>
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### 1:0 WO xxh: Dimension of the Texture for 1st Group of User Defined Clipping Planes

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<td>2 dimensions; both S and T coordinate</td>
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<td>3 dimensions; volume texture; S, T, R coordinates</td>
</tr>
<tr>
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<td>4 dimensions; S, T, R, Q coordinates</td>
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*Note to Driver: It is forbidden to enable HTXUCP1Enable but disable HTXUCP0Enable.*

### HParaType = 02h (HParaSubType = FEh), Sub-Address = 06-07h: Reserved

### HParaType = 02h (HParaSubType = FEh), Sub-Address = 08h: Texture A-H Control 1
Texture A to Texture H is defined in Vertex Buffer.

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| 20          | WO        | xxh     | Texture T Coordinate Input Mode – for Texture E  
|             |           |         | 0: Un-normalized  
|             |           |         | 1: Normalized     |
| 19          | WO        | xxh     | Texture R Coordinate Input Mode – for Texture E  
|             |           |         | 0: Un-normalized  
|             |           |         | 1: Normalized     |
| 18          | WO        | xxh     | Texture Q Coordinate Input Mode – for Texture E  
|             |           |         | 0: Un-normalized  
|             |           |         | 1: Normalized     |
| 17:16       | WO        | xxh     | Dimension of Texture E  
|             |           |         | 00: 1 dimension; only S coordinate  
|             |           |         | 01: 2 dimensions; both S and T coordinates  
|             |           |         | 10: 3 dimensions; volume texture; S, T, R coordinates  
|             |           |         | 11: 4 dimensions; S, T, R, Q coordinates     |
| 15:14       | WO        | xxh     | Reserved    |
| 13          | WO        | xxh     | Texture S Coordinate Input Mode – for Texture D  
|             |           |         | 0: Un-normalized  
|             |           |         | 1: Normalized     |
| 12          | WO        | xxh     | Texture T Coordinate Input Mode – for Texture D  
|             |           |         | 0: Un-normalized  
|             |           |         | 1: Normalized     |
| 11          | WO        | xxh     | Texture R Coordinate Input Mode – for Texture D  
|             |           |         | 0: Un-normalized  
|             |           |         | 1: Normalized     |
| 10          | WO        | xxh     | Texture Q Coordinate Input Mode – for Texture D  
|             |           |         | 0: Un-normalized  
|             |           |         | 1: Normalized     |
| 9:8         | WO        | xxh     | Dimension of Texture D  
|             |           |         | 00: 1 dimension; only S coordinate  
|             |           |         | 01: 2 dimensions; both S and T coordinates  
|             |           |         | 10: 3 dimensions; volume texture; S, T, R coordinates  
|             |           |         | 11: 4 dimensions; S, T, R, Q coordinates     |
| 7:6         | WO        | xxh     | Reserved    |
| 5           | WO        | xxh     | Texture S Coordinate Input Mode – for Texture C  
|             |           |         | 0: Un-normalized  
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| 4           | WO        | xxh     | Texture T Coordinate Input Mode – for Texture C  
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| 3           | WO        | xxh     | Texture R Coordinate Input Mode – for Texture C  
|             |           |         | 0: Un-normalized  
|             |           |         | 1: Normalized     |
| 2           | WO        | xxh     | Texture Q Coordinate Input Mode – for Texture C  
|             |           |         | 0: Un-normalized  
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| 1:0         | WO        | xxh     | Dimension of Texture C  
|             |           |         | 00: 1 dimension; only S coordinate  
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|             |           |         | 10: 3 dimensions; volume texture; S, T, R coordinates  
|             |           |         | 11: 4 dimensions; S, T, R, Q coordinates     |
### HParaType = 02h (HParaSubType = FEh), Sub-Address = 0Ah

#### Texture A-H Control 3

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<td>Texture F Wrap Correction along S Coordinate 0: No wrap 1: Wrap</td>
</tr>
<tr>
<td>6</td>
<td>WO</td>
<td>xxh</td>
<td>Texture F Wrap Correction along T Coordinate 0: No wrap 1: Wrap</td>
</tr>
<tr>
<td>5:4</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>3</td>
<td>WO</td>
<td>xxh</td>
<td>Texture E Wrap Correction along S Coordinate 0: No wrap 1: Wrap</td>
</tr>
<tr>
<td>2</td>
<td>WO</td>
<td>xxh</td>
<td>Texture E Wrap Correction along T Coordinate 0: No wrap 1: Wrap</td>
</tr>
<tr>
<td>1:0</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
**HParaType = 02h (HParaSubType = FEh), Sub-Address = 0Dh**

### Texture A-H Control 6

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
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<tbody>
<tr>
<td>23:16</td>
<td>WO</td>
<td>xxh</td>
<td>Exponential of Modulus</td>
</tr>
<tr>
<td>15:8</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>7</td>
<td>WO</td>
<td>xxh</td>
<td>Do “Modulus of 2^HTXMODE” with Texture H’s Coordinate</td>
</tr>
<tr>
<td>6</td>
<td>WO</td>
<td>xxh</td>
<td>Do “Modulus of 2^HTXMODE” with Texture G’s Coordinate</td>
</tr>
<tr>
<td>5</td>
<td>WO</td>
<td>xxh</td>
<td>Do “Modulus of 2^HTXMODE” with Texture F’s Coordinate</td>
</tr>
<tr>
<td>4</td>
<td>WO</td>
<td>xxh</td>
<td>Do “Modulus of 2^HTXMODE” with Texture E’s Coordinate</td>
</tr>
<tr>
<td>3</td>
<td>WO</td>
<td>xxh</td>
<td>Do “Modulus of 2^HTXMODE” with Texture D’s Coordinate</td>
</tr>
<tr>
<td>2</td>
<td>WO</td>
<td>xxh</td>
<td>Do “Modulus of 2^HTXMODE” with Texture C’s Coordinate</td>
</tr>
<tr>
<td>1</td>
<td>WO</td>
<td>xxh</td>
<td>Do “Modulus of 2^HTXMODE” with Texture B’s Coordinate</td>
</tr>
<tr>
<td>0</td>
<td>WO</td>
<td>xxh</td>
<td>Do “Modulus of 2^HTXMODE” with Texture A’s Coordinate</td>
</tr>
</tbody>
</table>

**HParaType = 02h (HParaSubType = FEh), Sub-Address = 0Eh**

### Texture I/J Control

<table>
<thead>
<tr>
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<th>Attribute</th>
<th>Default</th>
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<tbody>
<tr>
<td>23:14</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>13</td>
<td>WO</td>
<td>xxh</td>
<td>Texture S Coordinate Input Mode – for Texture J</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Un-normalized</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Normalized</td>
</tr>
<tr>
<td>12</td>
<td>WO</td>
<td>xxh</td>
<td>Texture T Coordinate Input Mode – for Texture J</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Un-normalized</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Normalized</td>
</tr>
<tr>
<td>11</td>
<td>WO</td>
<td>xxh</td>
<td>Texture R Coordinate Input Mode – for Texture J</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Un-normalized</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Normalized</td>
</tr>
<tr>
<td>10</td>
<td>WO</td>
<td>xxh</td>
<td>Texture Q Coordinate Input Mode – for Texture J</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Un-normalized</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Normalized</td>
</tr>
<tr>
<td>9:8</td>
<td>WO</td>
<td>xxh</td>
<td>Dimension of Texture J</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: 1 dimension; only S coordinate</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: 2 dimensions; both S and T coordinates</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: 3 dimensions; volume texture. S, T, R coordinates</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: 4 dimensions; S, T, R, Q coordinates</td>
</tr>
<tr>
<td>7:6</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>5</td>
<td>WO</td>
<td>xxh</td>
<td>Texture S Coordinate Input Mode – for Texture I</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Un-normalized</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Normalized</td>
</tr>
<tr>
<td>4</td>
<td>WO</td>
<td>xxh</td>
<td>Texture T Coordinate Input Mode – for Texture I</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Un-normalized</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Normalized</td>
</tr>
<tr>
<td>3</td>
<td>WO</td>
<td>xxh</td>
<td>Texture R Coordinate Input Mode – for Texture I</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Un-normalized</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Normalized</td>
</tr>
<tr>
<td>2</td>
<td>WO</td>
<td>xxh</td>
<td>Texture Q Coordinate Input Mode – for Texture I</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Un-normalized</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Normalized</td>
</tr>
<tr>
<td>1:0</td>
<td>WO</td>
<td>xxh</td>
<td>Dimension of Texture I</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: 1 dimension, only S coordinate</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: 2 dimensions; both S and T coordinates</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: 3 dimensions; volume texture. S, T, R coordinates</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: 4 dimensions; S, T, R, Q coordinates</td>
</tr>
</tbody>
</table>

**HParaType = 02h (HParaSubType = FEh), Sub-Address = 0Fh: Reserved**
### HParaType = 02h (HParaSubType = FEh), Sub-Address = 10h

**Coefficient Setting 1**

<table>
<thead>
<tr>
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<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23</td>
<td>WO xxh</td>
<td></td>
<td>YUV422 (Packet Mode) Texture Decode Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Even texel in S direction (Ye, Ue, Ve)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Odd texel in S direction (Yo, Uo, Vo)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Even texel in S direction (Ye, Ue, Ve)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Odd texel in S direction (Yo, (Ue + Ue+1)/2, (Ve + Ve+1)/2)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Note:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>If (HTXYUV422DM == true &amp; HTXnFM == 00110 000b</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>&amp; (HTXSnFLSe == nearest for enlarge</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>&amp; (odd texel in S direction) &amp; (not the rightest texel of texture)) {</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Y = Yo</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>U = (Ue + Ue+1)/2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>V = (Ve + Ve+1)/2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>} else {</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Y = Y</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>U = Ue</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>V = Ve</td>
</tr>
</tbody>
</table>

22:12 WO xxh Coefficient D of YUV to RGB Conversion
Format as 2’s complement s.2.8

11 WO xxh Reserved

10:0 WO xxh Coefficient A of YUV to RGB Conversion
Format as 2’s complement s.2.8

### HParaType = 02h (HParaSubType = FEh), Sub-Address = 11h

**Coefficient Setting 2**

<table>
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<th>Description</th>
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</thead>
<tbody>
<tr>
<td>23</td>
<td>WO xxh</td>
<td></td>
<td>Reserved</td>
</tr>
<tr>
<td>22:12</td>
<td>WO xxh</td>
<td></td>
<td>Coefficient C1 of YUV to RGB Conversion</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Format as 2’s complement s.2.8</td>
</tr>
<tr>
<td>11</td>
<td>WO xxh</td>
<td></td>
<td>Reserved</td>
</tr>
<tr>
<td>10:0</td>
<td>WO xxh</td>
<td></td>
<td>Coefficient B1 of YUV to RGB Conversion</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Format as 2’s complement s.2.8</td>
</tr>
</tbody>
</table>

### HParaType = 02h (HParaSubType = FEh), Sub-Address = 12h

**Coefficient Setting 3**

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</thead>
<tbody>
<tr>
<td>23</td>
<td>WO xxh</td>
<td></td>
<td>Reserved</td>
</tr>
<tr>
<td>22:12</td>
<td>WO xxh</td>
<td></td>
<td>Coefficient C2 of YUV to RGB Conversion</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Format as 2’s complement s.2.8</td>
</tr>
<tr>
<td>11</td>
<td>WO xxh</td>
<td></td>
<td>Reserved</td>
</tr>
<tr>
<td>10:0</td>
<td>WO xxh</td>
<td></td>
<td>Coefficient B2 of YUV to RGB Conversion</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Format as 2’s complement s.2.8</td>
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### HParaType = 02h (HParaSubType = FEh), Sub-Address = 13h

**Coefficient Setting 4**

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<tbody>
<tr>
<td>23</td>
<td>WO xxh</td>
<td></td>
<td>Reserved</td>
</tr>
<tr>
<td>22:12</td>
<td>WO xxh</td>
<td></td>
<td>Coefficient C3 of YUV to RGB Conversion</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Format as 2’s complement s.2.8</td>
</tr>
<tr>
<td>11</td>
<td>WO xxh</td>
<td></td>
<td>Reserved</td>
</tr>
<tr>
<td>10:0</td>
<td>WO xxh</td>
<td></td>
<td>Coefficient B3 of YUV to RGB Conversion</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Format as 2’s complement s.2.8</td>
</tr>
</tbody>
</table>
**HParaType 03h: Palette (HParaSubType: 00-22h)**

**HParaType = 03h (HParaSubType = 00h)**
Texture Palette 0

<table>
<thead>
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<th>Attribute</th>
<th>Default</th>
<th>Description</th>
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<tbody>
<tr>
<td>31:24</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>23:16</td>
<td>WO</td>
<td>xxh</td>
<td>Y of Texture Palette N Data</td>
</tr>
<tr>
<td>15:8</td>
<td>WO</td>
<td>xxh</td>
<td>U of Texture Palette N Data</td>
</tr>
<tr>
<td>7:0</td>
<td>WO</td>
<td>xxh</td>
<td>V of Texture Palette N Data</td>
</tr>
</tbody>
</table>

**HParaType = 03h (HParaSubType = 01h): Reserved (Texture Palette1 1)**

**HParaType = 03h (HParaSubType = 02h): Reserved (Texture Palette1 2)**

**HParaType = 03h (HParaSubType = 03h): Reserved (Texture Palette1 3)**

**HParaType = 03h (HParaSubType = 04h): Reserved (Texture Palette1 4)**

**HParaType = 03h (HParaSubType = 05h): Reserved (Texture Palette1 5)**

**HParaType = 03h (HParaSubType = 06h): Reserved (Texture Palette1 6)**

**HParaType = 03h (HParaSubType = 07h): Reserved (Texture Palette1 7)**

**HParaType = 03h (HParaSubType = 08-0Fh): Reserved**
## HParaType = 03h (HParaSubType = 10h)

### Offset or Base Address of Texture from Level 1 to Level 8 for the 16 Texture Samples

There are 16 texture samples and each sample can be up to 8 levels, so there should be 16x8 = 128 entries.

- HParaAddr 0 → HTXS0L1Offset
- HParaAddr 1 → HTXS0L2Offset
- ...........
- HParaAddr 7 → HTXS0L8Offset
- HParaAddr 8 → HTXS1L1Offset
- HParaAddr 9 → HTXS1L2Offset
- ...........
- HParaAddr 15 → HTXS1L8Offset
- HParaAddr 16 → HTXS2L1Offset
- HParaAddr 17 → HTXS2L2Offset
- ...........
- HParaAddr 23 → HTXS2L8Offset
- ............
- HParaAddr 118 → HTXSFL1Offset
- HParaAddr 119 → HTXSFL2Offset
- ............
- HParaAddr 127 → HTXSFL8Offset

To sum up, consider HTXS\textsubscript{nm}BasOffset, its entry is \((n*8 + m)\), where \(n\) is from 0 to Fh, and \(m\) is from 1 to 8h.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
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<tbody>
<tr>
<td>31:30</td>
<td>WO</td>
<td>xxh</td>
<td>Location of Texture Sample n’s Level m</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: System Local Frame Buffer (S.L.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: System Dynamic Frame Buffer (S.F.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: Reserved (System Memory)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: Reserved</td>
</tr>
<tr>
<td>29:24</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>23:0</td>
<td>WO</td>
<td>xxh</td>
<td>Offset Related to Texture Sample n’s Level 0 for Level m Base Address</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>In unit of byte.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This must be 256-byte boundary (in unit of 256 bytes or [31:8]).</td>
</tr>
</tbody>
</table>

## HParaType = 03h (HParaSubType = 11h)

### Texture 4x4 Filter Coefficient Table

There are 2^5 = 32 entries. The 5-bit fraction of “sf” or “tf” is the index.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:22</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>21:16</td>
<td>WO</td>
<td>xxh</td>
<td>Coefficient Cm for 4x4 Filter</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Format as 1.5 positive fixed-point; maximum is 1.0.</td>
</tr>
<tr>
<td>15</td>
<td>WO</td>
<td>xxh</td>
<td>Double the Coefficient Cr</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Crd = HTX4X4FltCrd</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Crd = HTX4X4FltCrd &lt;&lt; 1</td>
</tr>
<tr>
<td>14:8</td>
<td>WO</td>
<td>xxh</td>
<td>Coefficient C2 for 4x4 Filter</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Format as s1.5’s complement fixed-point; maximum is 1.0 and minimum is –0.5.</td>
</tr>
<tr>
<td>7</td>
<td>WO</td>
<td>xxh</td>
<td>Double the Coefficient Clu</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Clu = HTX4X4FltClu</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Clu = HTX4X4FltClu &lt;&lt; 1</td>
</tr>
<tr>
<td>6:0</td>
<td>WO</td>
<td>xxh</td>
<td>Coefficient Clu for 4x4 Filter</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Format as s1.5 2’s complement fixed-point; maximum is 1.0 and minimum is –0.5.</td>
</tr>
</tbody>
</table>
Cl = HTX4X4Clu(sf) * 2^HTX4X4CluE(sf)
Cr = HTX4X4Crd(sf) * 2^HTX4X4CrdE(sf)
Csm = HTX4X4Cm(sf)
Cu = HTX4X4Clu(tf) * 2^HTX4X4CluE(tf)
Cd = HTX4X4Crd(tf) * 2^HTX4X4CrdE(tf)
Ctm = HTX4X4Cm(tf)

Cp1 = (1 – Csm)*(1 – Ctm)
Cp2 = Csm*(1 – Ctm)
Cp3 = (1 – Csm)*Ctm
Cp4 = Csm*Ctm

T1 = (1 – Cl)*(1 – Cu)*T1ul + Cl*(1 – Cu)*T1ur + (1 – Cl)*Cu*T1dl + Cl*Cu*T1dr
T2 = (1 – Cr)*(1 – Cu)*T2ul + Cr*(1 – Cu)*T2ur + (1 – Cr)*Cu*T2dl + Cr*Cu*T2dr
T3 = (1 – Cl)*(1 – Cd)*T3ul + Cl*(1 – Cd)*T3ur + (1 – Cl)*Cd*T3dl + Cl*Cd*T3dr
T4 = (1 – Cr)*(1 – Cd)*T4ul + Cr*(1 – Cd)*T4ur + (1 – Cr)*Cd*T4dl + Cr*Cd*T4dr
P = T1*Cp1 + T2*Cp2 + T3*Cp3 + T4*Cp4
### HParaType = 03h (HParaSubType = 14h)
#### Stipple Palette

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>WO</td>
<td>xxh</td>
<td>32-Bit Stipple Palette Data</td>
</tr>
</tbody>
</table>

### HParaType = 03h (HParaSubType = 15h), HParaAdr = 00h
#### De-Gamma Table for Reading Texture

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
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| 31:30| WO        | xxh     | Rounding Mode  
00: Truncate  
01: Rounding  
1x: Reserved |
| 29:20| WO        | xxh     | De-Gamma Table Value for Reading Texture at C = 10'h0C0 |
| 19:10| WO        | xxh     | De-Gamma Table Value for Reading Texture at C = 10'h080 |
| 9:0  | WO        | xxh     | De-Gamma Table Value for Reading Texture at C = 10'h040 |

### HParaType = 03h (HParaSubType = 15h), HParaAdr = 01h
#### De-Gamma Table for Reading Texture

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#### De-Gamma Table for Reading Texture

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#### De-Gamma Table for Reading Texture

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### HParaType = 03h (HParaSubType = 17h), HParaAdr = 11h
#### Gamma-de-Gamma Table for Writing Color

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<tr>
<td>19:10</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing G Channel at $G = 10'h0C0$</td>
</tr>
<tr>
<td>9:0</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing B Channel at $B = 10'h0C0$</td>
</tr>
</tbody>
</table>

### HParaType = 03h (HParaSubType = 17h), HParaAdr = 12h
#### Gamma-de-Gamma Table for Writing Color

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:30</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>29:20</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing R Channel at $R = 10'h0E0$</td>
</tr>
<tr>
<td>19:10</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing G Channel at $G = 10'h0E0$</td>
</tr>
<tr>
<td>9:0</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing B Channel at $B = 10'h0E0$</td>
</tr>
</tbody>
</table>

### HParaType = 03h (HParaSubType = 17h), HParaAdr = 13h
#### Gamma-de-Gamma Table for Writing Color

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:30</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>29:20</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing R Channel at $R = 10'h100$</td>
</tr>
<tr>
<td>19:10</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing G Channel at $G = 10'h100$</td>
</tr>
<tr>
<td>9:0</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing B Channel at $B = 10'h100$</td>
</tr>
</tbody>
</table>

### HParaType = 03h (HParaSubType = 17h), HParaAdr = 14h
#### Gamma-de-Gamma Table for Writing Color

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:30</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>29:20</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing R Channel at $R = 10'h140$</td>
</tr>
<tr>
<td>19:10</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing G Channel at $G = 10'h140$</td>
</tr>
<tr>
<td>9:0</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing B Channel at $B = 10'h140$</td>
</tr>
</tbody>
</table>

### HParaType = 03h (HParaSubType = 17h), HParaAdr = 15h
#### Gamma-de-Gamma Table for Writing Color

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:30</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>29:20</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing R Channel at $R = 10'h180$</td>
</tr>
<tr>
<td>19:10</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing G Channel at $G = 10'h180$</td>
</tr>
<tr>
<td>9:0</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing B Channel at $B = 10'h180$</td>
</tr>
</tbody>
</table>

### HParaType = 03h (HParaSubType = 17h), HParaAdr = 16h
#### Gamma-de-Gamma Table for Writing Color

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:30</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>29:20</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing R Channel at $R = 10'h1C0$</td>
</tr>
<tr>
<td>19:10</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing G Channel at $G = 10'h1C0$</td>
</tr>
<tr>
<td>9:0</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing B Channel at $B = 10'h1C0$</td>
</tr>
</tbody>
</table>
### HParaType = 03h (HParaSubType = 17h), HParaAdr = 17h
#### Gamma-de-Gamma Table for Writing Color

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:30</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>29:20</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing R Channel at R = 10'h200</td>
</tr>
<tr>
<td>19:10</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing G Channel at G = 10'h200</td>
</tr>
<tr>
<td>9:0</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing B Channel at B = 10'h200</td>
</tr>
</tbody>
</table>

### HParaType = 03h (HParaSubType = 17h), HParaAdr = 18h
#### Gamma-de-Gamma Table for Writing Color

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:30</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>29:20</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing R Channel at R = 10'h240</td>
</tr>
<tr>
<td>19:10</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing G Channel at G = 10'h240</td>
</tr>
<tr>
<td>9:0</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing B Channel at B = 10'h240</td>
</tr>
</tbody>
</table>

### HParaType = 03h (HParaSubType = 17h), HParaAdr = 19h
#### Gamma-de-Gamma Table for Writing Color

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:30</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>29:20</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing R Channel at R = 10'h280</td>
</tr>
<tr>
<td>19:10</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing G Channel at G = 10'h280</td>
</tr>
<tr>
<td>9:0</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing B Channel at B = 10'h280</td>
</tr>
</tbody>
</table>

### HParaType = 03h (HParaSubType = 17h), HParaAdr = 1Ah
#### Gamma-de-Gamma Table for Writing Color

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:30</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>29:20</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing R Channel at R = 10'h300</td>
</tr>
<tr>
<td>19:10</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing G Channel at G = 10'h300</td>
</tr>
<tr>
<td>9:0</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing B Channel at B = 10'h300</td>
</tr>
</tbody>
</table>

### HParaType = 03h (HParaSubType = 17h), HParaAdr = 1Bh
#### Gamma-de-Gamma Table for Writing Color

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:30</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>29:20</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing R Channel at R = 10'h340</td>
</tr>
<tr>
<td>19:10</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing G Channel at G = 10'h340</td>
</tr>
<tr>
<td>9:0</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing B Channel at B = 10'h340</td>
</tr>
</tbody>
</table>

### HParaType = 03h (HParaSubType = 17h), HParaAdr = 1Ch
#### Gamma-de-Gamma Table for Writing Color

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:30</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>29:20</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing R Channel at R = 10'h340</td>
</tr>
<tr>
<td>19:10</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing G Channel at G = 10'h340</td>
</tr>
<tr>
<td>9:0</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing B Channel at B = 10'h340</td>
</tr>
</tbody>
</table>
HParaType = 03h (HParaSubType = 17h), HParaAdr = 1Dh
Gamma-de-Gamma Table for Writing Color

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:30</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>29:20</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing R Channel at R = 10'h380</td>
</tr>
<tr>
<td>19:10</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing G Channel at G = 10'h380</td>
</tr>
<tr>
<td>9:0</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing B Channel at B = 10'h380</td>
</tr>
</tbody>
</table>

HParaType = 03h (HParaSubType = 17h), HParaAdr = 1Eh
Gamma-de-Gamma Table for Writing Color

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:30</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>29:20</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing R Channel at R = 10'h3C0</td>
</tr>
<tr>
<td>19:10</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing G Channel at G = 10'h3C0</td>
</tr>
<tr>
<td>9:0</td>
<td>WO</td>
<td>xxh</td>
<td>Gamma Table Value for Writing B Channel at B = 10'h3C0</td>
</tr>
</tbody>
</table>

HParaType = 03h (HParaSubType = 20h)
Pixel Shader ALU Instruction
Each instruction contains 4 double words. HParaAdr (4n+3) to (4n) are as the n-th instruction. Because of total 96 instructions, there are up to 96*4 (=384) entries.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>WO</td>
<td>xxh</td>
<td>Pixel Shader ALU Instruction</td>
</tr>
</tbody>
</table>

HParaType = 03h (HParaSubType = 21h)
Pixel Shader TAU Instruction
There are totally 32 32-bit TAU instructions.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>WO</td>
<td>xxh</td>
<td>Pixel Shader TAU Instruction</td>
</tr>
</tbody>
</table>

HParaType = 03h (HParaSubType = 22h)
Pixel Shader Constant Registers
Each constant register contains 4 32-bit components.
HParaAdr (4n) is as the 1st component of the n-th constant register.
HParaAdr (4n+1) is as the 2nd component of the n-th constant register.
HParaAdr (4n+2) is as the 3rd component of the n-th constant register.
HParaAdr (4n+3) is as the 4th component of the n-th constant register.
Where n is from 0 to 22, and 32 to 54.
If HPSSDbCnstR is set, the n from 32 to 54 is the same as the n from 0 to 22. And HW would fill n from 32 to 54 automtly.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>WO</td>
<td>xxh</td>
<td>Pixel Shader’s Constant Register as Floating s[8].23</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Hardware would automatically transform the 32-bit floating to 24-bit floating format.</td>
</tr>
</tbody>
</table>
**HParaType 04h: Vertex and Primitive Setting**

**Sub-Address (Bits [31:24]): 00-AAh**

**Flexible Vertex Format 1**

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:22</td>
<td>WO</td>
<td>xxh</td>
<td><strong>Flexibility Vertex Format's (X, Y) Test Mode</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: If (X or Y is “Not-a-Number) then ignore corresponded <strong>primitive</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1x: If (X or Y is “Not-a-Number) then ignore corresponded <strong>primitive list</strong></td>
</tr>
<tr>
<td>21:20</td>
<td>WO</td>
<td>xxh</td>
<td><strong>Flexibility Vertex Format's Z Test Mode</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: If (Z is “Not-a-Number) then ignore corresponded <strong>primitive</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1x: If (Z is “Not-a-Number) then ignore corresponded <strong>primitive list</strong></td>
</tr>
<tr>
<td>19:18</td>
<td>WO</td>
<td>xxh</td>
<td><strong>Flexibility Vertex Format's W Test Mode</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: If (W is “Not-a-Number) then ignore corresponded <strong>primitive</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1x: If (W is “Not-a-Number) then ignore corresponded <strong>primitive list</strong></td>
</tr>
<tr>
<td>17</td>
<td>WO</td>
<td>xxh</td>
<td><strong>Switch the Flexibility Vertex Format's X to Y, and Y to X</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Keep</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Switch</td>
</tr>
<tr>
<td>16:15</td>
<td>WO</td>
<td>xxh</td>
<td><strong>Location of Vertex Buffer</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: System Local Frame Buffer (S.L.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: System Dynamic Frame Buffer (S.F.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: Reserved (System Memory)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Note to Driver and HW: All vertex buffers are located in LL, SF, or all in LL,</td>
</tr>
<tr>
<td>14:6</td>
<td>WO</td>
<td>xxh</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>5:0</td>
<td>WO</td>
<td>xxh</td>
<td><strong>Length of FVF Vertex Length</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>In unit of 32 bits</td>
</tr>
</tbody>
</table>
### HParaType = 04h, Sub-Address = 01h

#### Flexible Vertex Format 2

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[23:0]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>23:22</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>21:16</td>
<td>WO</td>
<td>xxh</td>
<td>The 3rd FVF Attribute Number (X, Y, ... QJ, BFCdiff, BFCspec)</td>
</tr>
<tr>
<td>15:14</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>13:8</td>
<td>WO</td>
<td>xxh</td>
<td>The 2nd FVF Attribute Number (X, Y, ... QJ, BFCdiff, BFCspec)</td>
</tr>
<tr>
<td>7:6</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>5:0</td>
<td>WO</td>
<td>xxh</td>
<td>The 1st FVF Attribute Number (X, Y, ... QJ, BFCdiff, BFCspec)</td>
</tr>
<tr>
<td></td>
<td>00h: X</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>01h: Y</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>02h: Z</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>03h: W</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>04h: Point Size</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>05h: Color 0: Diffuse</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>06h: Color 1: Specula</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>07h: Fog Factor</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>08h: S of TextureA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>09h: T of TextureA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0Ah: R of TextureA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0Bh: Q of TextureA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0Ch: S of TextureB</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0Dh: T of TextureB</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 Eh: R of TextureB</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0Fh: Q of TextureB</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>10h: S of TextureC</td>
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<td>13:8</td>
<td>WO</td>
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<td>The 5th FVF Attribute Number (X, Y, …, QJ, BFCdiff, BFCspec)</td>
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<td>The 4th FVF Attribute Number (X, Y, …, QJ, BFCdiff, BFCspec)</td>
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### Flexible Vertex Format 4

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<tr>
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<td>The 8th FVF Attribute Number (X, Y, …, QJ, BFCdiff, BFCspec)</td>
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<td>The 7th FVF Attribute Number (X, Y, …, QJ, BFCdiff, BFCspec)</td>
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### Flexible Vertex Format 5

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<td>The 12th FVF Attribute Number (X, Y, …, QJ, BFCdiff, BFCspec)</td>
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<tr>
<td>13:8</td>
<td>WO</td>
<td>xxh</td>
<td>The 11th FVF Attribute Number (X, Y, …, QJ, BFCdiff, BFCspec)</td>
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### Flexible Vertex Format 6

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<td>xxh</td>
<td>The 15th FVF Attribute Number (X, Y, …, QJ, BFCdiff, BFCspec)</td>
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<td>Reserved</td>
</tr>
<tr>
<td>13:8</td>
<td>WO</td>
<td>xxh</td>
<td>The 14th FVF Attribute Number (X, Y, …, QJ, BFCdiff, BFCspec)</td>
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<td>The 13th FVF Attribute Number (X, Y, …, QJ, BFCdiff, BFCspec)</td>
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### Flexible Vertex Format 7

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<td>The 18th FVF Attribute Number (X, Y, …, QJ, BFCdiff, BFCspec)</td>
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<td>Reserved</td>
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<tr>
<td>13:8</td>
<td>WO</td>
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<td>The 17th FVF Attribute Number (X, Y, …, J, BFCdiff, BFCspec)</td>
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<td>The 16th FVF Attribute Number (X, Y, …, QJ, BFCdiff, BFCspec)</td>
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### HPaParaType = 04h, Sub-Address = 07h

#### Flexible Vertex Format 8

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<td>The 21st FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)</td>
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<td>Reserved</td>
</tr>
<tr>
<td>13:8</td>
<td>WO</td>
<td>xxh</td>
<td>The 20th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)</td>
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<td>5:0</td>
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<td>xxh</td>
<td>The 19th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)</td>
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### HPaParaType = 04h, Sub-Address = 08h

#### Flexible Vertex Format 9

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### HPaParaType = 04h, Sub-Address = 09h

#### Flexible Vertex Format 10

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<td>The 27th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)</td>
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<td>Reserved</td>
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<tr>
<td>13:8</td>
<td>WO</td>
<td>xxh</td>
<td>The 26th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)</td>
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<td>5:0</td>
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<td>The 25th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)</td>
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### HPaParaType = 04h, Sub-Address = 0Ah

#### Flexible Vertex Format 11

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<td>The 30th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)</td>
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<td>Reserved</td>
</tr>
<tr>
<td>13:8</td>
<td>WO</td>
<td>xxh</td>
<td>The 29th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)</td>
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<td>xxh</td>
<td>The 28th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)</td>
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### HPaParaType = 04h, Sub-Address 0Bh

#### Flexible Vertex Format 12

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<tr>
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<td>WO</td>
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<td>The 32th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)</td>
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### HPareType = 04h, Sub-Address = 0Ch
**Flexible Vertex Format 13**

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<tr>
<td>21:16</td>
<td>WO</td>
<td>xxh</td>
<td>The 36th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)</td>
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<td>15:14</td>
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<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>13:8</td>
<td>WO</td>
<td>xxh</td>
<td>The 35th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)</td>
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<td>5:0</td>
<td>WO</td>
<td>xxh</td>
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### HPareType = 04h, Sub-Address = 0Dh
**Flexible Vertex Format 14**

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<tr>
<td>21:16</td>
<td>WO</td>
<td>xxh</td>
<td>The 39th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)</td>
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<td>Reserved</td>
</tr>
<tr>
<td>13:8</td>
<td>WO</td>
<td>xxh</td>
<td>The 38th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)</td>
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<td>xxh</td>
<td>The 37th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)</td>
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### HPareType = 04h, Sub-Address = 0Eh
**Flexible Vertex Format 15**

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<td>WO</td>
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<td>The 41st FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)</td>
</tr>
<tr>
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<td>xxh</td>
<td>The 40th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)</td>
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### HPareType = 04h, Sub-Address = 0Fh
**Flexible Vertex Format 16**

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<td>The 47th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)</td>
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### HPareType = 04h, Sub-Address = 10h
**Flexible Vertex Format 17**

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<td>WO</td>
<td>xxh</td>
<td>Flexible Vertex Format Mask</td>
</tr>
<tr>
<td>Bit [23]: BFCdiff Parameter Mask</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0: Primitive Vertex Parameter does not have Back Face Color0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1: Primitive Vertex Parameter has Back Face Color0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bit [22]: BFCspec Parameter Mask</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0: Primitive Vertex Parameter does not have Back Face Color1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1: Primitive Vertex Parameter has Back Face Color1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>21:18</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>17:12</td>
<td>WO</td>
<td>xxh</td>
<td>The 50th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)</td>
</tr>
<tr>
<td>11:6</td>
<td>WO</td>
<td>xxh</td>
<td>The 49th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)</td>
</tr>
<tr>
<td>5:0</td>
<td>WO</td>
<td>xxh</td>
<td>The 48th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)</td>
</tr>
</tbody>
</table>
HParaType = 04h, Sub-Address = 11-1Fh: Reserved  (For Flexible Vertex Format)

HParaType = 04h, Sub-Address = 20h
Vertex Buffer & Primitive Setting 1

There are totally 32 32-bit TAU instructions.

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23</td>
<td>WO</td>
<td>xxh</td>
<td>Disable Clipping for Triangle Point (Just Near Plane)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Note to Driver: This register is only for triangle with fill mode “point”. When this register enabled, there might be 2 new points resulted from near plane clipping, and their attributes (such as point size, color, texture and so on) are interpolated from the original 3 vertices. When disabled (HenCL4TriPoint N = 1), HW just renders the vertices inside the view volumn.</td>
</tr>
<tr>
<td>22:21</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>21:16</td>
<td>WO</td>
<td>xxh</td>
<td>The Setting of Second or Even One-vertex Triangle &lt;H2nd1VT&gt;</td>
</tr>
</tbody>
</table>

  **Bit [21:20]: Setting of Vertex A**
  This setting is used for both triangle and line rendering.
  00: Vertex a is a new input
  01: The Vertex a will be replaced by previous Vertex a.
  10: The Vertex a will be replaced by previous Vertex b.
  11: The Vertex a will be replaced by previous Vertex c.

  **Bit [19:18]: Setting of Vertex B**
  This setting is used for both triangle and line rendering.
  00: Vertex b is a new input
  01: The Vertex b will be replaced by previous Vertex a.
  10: The Vertex b will be replaced by previous Vertex b.
  11: The Vertex b will be replaced by previous Vertex c.

  **Bit [17:16]: Setting of Vertex C**
  This setting is used for both triangle and line rendering.
  00: Vertex c is a new input
  01: The Vertex c will be replaced by previous Vertex a.
  10: The Vertex c will be replaced by previous Vertex b.
  11: The Vertex c will be replaced by previous Vertex c.
15:8 WO xxh | Primitive Render Mode
---|---
00000000: Full Vertex Cycle
For Triangle Rendering, this is the 3 vertexes cycle.
For Line Rendering, this is the 2 vertexes cycle.
10xxxxxx: Reserved
x1xxxxxx: Automatic Fast Primitive Vertex Cycle
For Triangle Rendering, this is a fast way to render 3111 Mode
For Line Rendering, this is a fast way to render 2111 Mode
The first or odd single vertex cycle will use the setting of bit [5:0].
The second or even single vertex cycle will use the setting of H2nd1VT.

<table>
<thead>
<tr>
<th>Bit [13:12] Setting of Vertex A</th>
</tr>
</thead>
<tbody>
<tr>
<td>This setting is used for both triangle and line rendering.</td>
</tr>
<tr>
<td>00: Vertex a is a new input</td>
</tr>
<tr>
<td>01: The Vertex a will be replaced by previous Vertex a.</td>
</tr>
<tr>
<td>10: The Vertex a will be replaced by previous Vertex b.</td>
</tr>
<tr>
<td>11: The Vertex a will be replaced by previous Vertex c.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit [11:10] Setting of Vertex B</th>
</tr>
</thead>
<tbody>
<tr>
<td>This setting is used for both triangle and line rendering.</td>
</tr>
<tr>
<td>00: Vertex b is a new input</td>
</tr>
<tr>
<td>01: The Vertex b will be replaced by previous Vertex a.</td>
</tr>
<tr>
<td>10: The Vertex b will be replaced by previous Vertex b.</td>
</tr>
<tr>
<td>11: The Vertex b will be replaced by previous Vertex c.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit [9:8] Setting of Vertex C</th>
</tr>
</thead>
<tbody>
<tr>
<td>This setting is used for both triangle and line rendering.</td>
</tr>
<tr>
<td>00: Vertex c is a new input</td>
</tr>
<tr>
<td>01: The Vertex c will be replaced by previous Vertex a.</td>
</tr>
<tr>
<td>10: The Vertex c will be replaced by previous Vertex b.</td>
</tr>
<tr>
<td>11: The Vertex c will be replaced by previous Vertex c.</td>
</tr>
</tbody>
</table>

7:2 WO xxh | Reserved
---|---
1 WO xxh | Vertex Buffer Index Mode
0: 16-bit index
1: 32-bit index
0 WO xxh | Vertex Mode
0: Command mode Vertex
1: Index mode Vertex

HParaType = 04h, Sub-Address = 21h
Vertex Buffer & Primitive Setting 2

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:0</td>
<td>WO xxh</td>
<td>Lower 3 Bytes of Vertex Buffer Base Address</td>
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</tr>
</tbody>
</table>

HParaType = 04h, Sub-Address = 22h
Vertex Buffer & Primitive Setting 3

<table>
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<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:16</td>
<td>WO xxh</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>15:8</td>
<td>WO xxh</td>
<td>Pitch of Each Vertex in Vertex Buffer</td>
<td></td>
</tr>
<tr>
<td>7:0</td>
<td>WO xxh</td>
<td>Higher Byte of Vertex Buffer Base Address</td>
<td></td>
</tr>
</tbody>
</table>
### Vertex Buffer & Primitive Setting 4

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:16</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 15          | WO        | xxh     | Last Pixel Control for Drawing Line  
0: Discard the last pixel of each line  
1: Draw the last pixel of each line |
| 14:12       | WO        | xxh     | Shading Setting  
000: Solid shading  
001: Flat shading via Vertex a  
010: Flat shading via Vertex b  
011: Flat shading via Vertex c  
100: Gouraud shading |
| 11:9        | WO        | xxh     | Edge Flag  
Assume the vertex transmission sequence of a triangle is a, b, then c.  
000: Render NO Edge for triangle wire-frame or antialiasing  
1xx: Render Edge (a, b) for triangle wire-frame or antialiasing  
x1x: Render Edge (b, c) for triangle wire-frame or antialiasing  
xx1: Render Edge (c, a) for triangle wire-frame or antialiasing |
| 8           | WO        | xxh     | Back Face Mode for “Culling”  
0: If the vertex input is in the order of clockwise, it would be “culled”  
1: If the vertex input is in the order of counterclockwise, it would be “culled” |
| 7           | WO        | xxh     | Back Face Mode for VS’s Output “oBFD#”  
0: If the vertex input is in the order of clockwise, “oBFD#” would be selected as the vertex color  
1: If the vertex input is in the order of counterclockwise, “oBFD#” would be selected as the vertex color |
| 6:5         | WO        | xxh     | Primitive Type for Clockwise Triangle  
00: Triangle Rendering for Hen2FRender enabled and clockwise primitive  
01: Reserved  
10: Triangle Wire-frame Rendering for Hen2FRender enabled and clockwise primitive  
11: Triangle Point Rendering for Hen2FRender enabled and clockwise primitive |
| 4           | WO        | xxh     | Render Mode (PMType) Is Different for Front-Face and Back-Face Primitive <Hen2FRender>  
The related PMType is “Triangle”, “Triangle Wire-Frame” and “Triangle Point”.  
0: The PMTypes for both front-face and back-face are the same, or only one kind of face is rendered.  
1: The PMType is different for front-face and back-face primitive. |
| 3:0         | WO        | xxh     | Primitive Type  
0000: Point Rendering  
0001: Line Rendering  
0010: Triangle Rendering for “Hen2Frender” is false, or Hen2Frender enabled and counter-clockwise primitive  
0011: Reserved  
0100: Rectangle  
0101: Reserved  
0110: Triangle Wire-frame Rendering for “Hen2Frender” is false, or Hen2Frender enabled and counter-clockwise primitive  
0111: Triangle Point Rendering for “Hen2Frender” is false, or Hen2Frender enabled and counter-clock-wise primitive  
xxxx: Reserved |

### Vertex Buffer & Primitive Setting 5

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 23:0        | WO        | xxh     | Vertices Number  
\(n\): There are \(n\) vertexes in current primitive list. |
### HParaType = 04h, Sub-Address = 25h
#### Vertex Buffer & Primitive Setting 6

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
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<th>Description</th>
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</thead>
<tbody>
<tr>
<td>23:0</td>
<td>WO</td>
<td>xxh</td>
<td>Vertexes Number</td>
</tr>
</tbody>
</table>

**Bit [23]: X Parameter Mask**
- 0: Primitive Vertex Parameter does not have X
- 1: Primitive Vertex Parameter has X

**Bit [22]: Y Parameter Mask**
- 0: Primitive Vertex Parameter does not have Y
- 1: Primitive Vertex Parameter has Y

**Bit [21]: Z Parameter Mask**
- 0: Primitive Vertex Parameter does not have Z
- 1: Primitive Vertex Parameter has Z

**Bit [20]: W Parameter Mask**
- 0: Primitive Vertex Parameter does not have W
- 1: Primitive Vertex Parameter has W

**Bit [19]: Point-Size Parameter Mask**
- 0: Primitive Vertex Parameter does not have Point-Size
  - If the primitive type is point, use HVPointSize.
- 1: Primitive Vertex Parameter has Point-Size
  - If the primitive type is point, use the value from Vertex Data.

**Bit [18]: Cd(C0) Parameter Mask**
- 0: Primitive Vertex Parameter does not have Diffuse Color, ARGB
- 1: Primitive Vertex Parameter has Diffuse Color, ARGB

**Bit [17]: Cs(C1) Parameter Mask**
- 0: Primitive Vertex Parameter does not have Specula Color, SR SG SB, and SA
- 1: Primitive Vertex Parameter has Specula Color, SR SG SB, and SA

**Bit [16]: Fog-Factor Parameter Mask**
- 0: Primitive Vertex Parameter does not have Fog Factor
- 1: Primitive Vertex Parameter has Fog Factor

**Bit [15]: Texture A’s S Parameter Mask**
- 0: Primitive Vertex Parameter does not have Texture Coordinate S
- 1: Primitive Vertex Parameter has Texture Coordinate S

**Bit [14]: Texture A’s T Parameter Mask**
- 0: Primitive Vertex Parameter does not have Texture Coordinate T
- 1: Primitive Vertex Parameter has Texture Coordinate T

**Bit [13]: Texture A’s R Parameter Mask**
- 0: Primitive Vertex Parameter does not have Texture Coordinate R
- 1: Primitive Vertex Parameter has Texture Coordinate R

**Bit [12]: Texture A’s Q Parameter Mask**
- 0: Primitive Vertex Parameter does not have Texture Coordinate Q
- 1: Primitive Vertex Parameter has Texture Coordinate Q

**Bit [11]: Texture B’s S Parameter Mask**
- 0: Primitive Vertex Parameter does not have Texture Coordinate S
- 1: Primitive Vertex Parameter has Texture Coordinate S

**Bit [10]: Texture B’s T Parameter Mask**
- 0: Primitive Vertex Parameter does not have Texture Coordinate T
- 1: Primitive Vertex Parameter has Texture Coordinate T

**Bit [9]: Texture B’s R Parameter Mask**
- 0: Primitive Vertex Parameter does not have Texture Coordinate R
- 1: Primitive Vertex Parameter has Texture Coordinate R

**Bit [8]: Texture B’s Q Parameter Mask**
<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Mask</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Texture C's S Parameter Mask</td>
<td>0: No texture</td>
<td>0: No texture coordinate S</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Texture</td>
<td>1: Texture coordinate S</td>
</tr>
<tr>
<td>6</td>
<td>Texture C’s T Parameter Mask</td>
<td>0: No texture</td>
<td>0: No texture coordinate T</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Texture</td>
<td>1: Texture coordinate T</td>
</tr>
<tr>
<td>5</td>
<td>Texture C’s R Parameter Mask</td>
<td>0: No texture</td>
<td>0: No texture coordinate R</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Texture</td>
<td>1: Texture coordinate R</td>
</tr>
<tr>
<td>4</td>
<td>Texture C’s Q Parameter Mask</td>
<td>0: No texture</td>
<td>0: No texture coordinate Q</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Texture</td>
<td>1: Texture coordinate Q</td>
</tr>
<tr>
<td>3</td>
<td>Texture D’s S Parameter Mask</td>
<td>0: No texture</td>
<td>0: No texture coordinate S</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Texture</td>
<td>1: Texture coordinate S</td>
</tr>
<tr>
<td>2</td>
<td>Texture D’s T Parameter Mask</td>
<td>0: No texture</td>
<td>0: No texture coordinate T</td>
</tr>
<tr>
<td></td>
<td></td>
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<td>1: Texture coordinate T</td>
</tr>
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<td>Texture D’s R Parameter Mask</td>
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<td>0: No texture coordinate R</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Texture</td>
<td>1: Texture coordinate R</td>
</tr>
<tr>
<td>0</td>
<td>Texture D’s Q Parameter Mask</td>
<td>0: No texture</td>
<td>0: No texture coordinate Q</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Texture</td>
<td>1: Texture coordinate Q</td>
</tr>
</tbody>
</table>
**Vertex Buffer & Primitive Setting 7**

- **HParaType = 04h, Sub-Address = 26h**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:16</td>
<td>WO</td>
<td>xxh</td>
<td>Flexible Vertex Format Mask</td>
</tr>
<tr>
<td>Bit [23]: Texture I's S Parameter Mask</td>
<td>0: Primitive Vertex Parameter does not have Texture Coordinate S</td>
<td>1: Primitive Vertex Parameter has Texture Coordinate S</td>
<td></td>
</tr>
<tr>
<td>Bit [22]: Texture I's T Parameter Mask</td>
<td>0: Primitive Vertex Parameter does not have Texture Coordinate T</td>
<td>1: Primitive Vertex Parameter has Texture Coordinate T</td>
<td></td>
</tr>
<tr>
<td>Bit [21]: Texture I's R Parameter Mask</td>
<td>0: Primitive Vertex Parameter does not have Texture Coordinate R</td>
<td>1: Primitive Vertex Parameter has Texture Coordinate R</td>
<td></td>
</tr>
<tr>
<td>Bit [20]: Texture I's Q Parameter Mask</td>
<td>0: Primitive Vertex Parameter does not have Texture Coordinate Q</td>
<td>1: Primitive Vertex Parameter has Texture Coordinate Q</td>
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</tr>
<tr>
<td>Bit [19]: Texture J's S Parameter Mask</td>
<td>0: Primitive Vertex Parameter does not have Texture Coordinate S</td>
<td>1: Primitive Vertex Parameter has Texture Coordinate S</td>
<td></td>
</tr>
<tr>
<td>Bit [18]: Texture J's T Parameter Mask</td>
<td>0: Primitive Vertex Parameter does not have Texture Coordinate T</td>
<td>1: Primitive Vertex Parameter has Texture Coordinate T</td>
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<tr>
<td>Bit [17]: Texture J's R Parameter Mask</td>
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<tr>
<td>Bit</td>
<td>Description</td>
<td>Mask Value</td>
<td>Vertex Parameter Description</td>
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<td>------------</td>
<td>------------------------------------------------------------------</td>
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<tr>
<td>15</td>
<td>Texture E’s S Parameter Mask</td>
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<td>1</td>
<td>Primitive Vertex Parameter has Texture Coordinate S</td>
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</tr>
<tr>
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<td>Primitive Vertex Parameter has Texture Coordinate S</td>
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<tr>
<td>3</td>
<td>Texture H’s S Parameter Mask</td>
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<td>2</td>
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<td></td>
<td></td>
<td>1</td>
<td>Primitive Vertex Parameter has Texture Coordinate T</td>
</tr>
<tr>
<td>1</td>
<td>Texture H’s R Parameter Mask</td>
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<td>Primitive Vertex Parameter does not have Texture Coordinate R</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>Primitive Vertex Parameter has Texture Coordinate R</td>
</tr>
<tr>
<td>0</td>
<td>Texture H’s Q Parameter Mask</td>
<td>0</td>
<td>Primitive Vertex Parameter does not have Texture Coordinate Q</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>Primitive Vertex Parameter has Texture Coordinate Q</td>
</tr>
</tbody>
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HPaParaType = 04h, Sub-Address = 27h
Vertex Buffer & Primitive Setting 8

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
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<tbody>
<tr>
<td>23:0</td>
<td>WO</td>
<td>xxh</td>
<td>Starting Primitive Count</td>
</tr>
</tbody>
</table>

HPaParaType = 04h, Sub-Address = 28h
Vertex Buffer & Primitive Setting 9

<table>
<thead>
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<th>Attribute</th>
<th>Default</th>
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<tbody>
<tr>
<td>23:0</td>
<td>WO</td>
<td>xxh</td>
<td>Vertex Parameter Mask</td>
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<tr>
<td></td>
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<td></td>
<td><em>Note that the &quot;(**)&quot; is controlled by HVPDV_XX's Setting</em></td>
</tr>
<tr>
<td></td>
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<td><strong>Bit [23]: X Parameter Mask</strong></td>
</tr>
<tr>
<td></td>
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<td>0: Primitive Vertex Parameter does not have X thus use default value 0.0</td>
</tr>
<tr>
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<td></td>
<td>1: Primitive Vertex Parameter has X</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><strong>Bit [22]: Y Parameter Mask</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Primitive Vertex Parameter does not have Y thus use default value 0.0</td>
</tr>
<tr>
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<td></td>
<td></td>
<td>1: Primitive Vertex Parameter has Y</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><strong>Bit [21]: Z Parameter Mask</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Primitive Vertex Parameter does not have Z thus use default value (***)</td>
</tr>
<tr>
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<td>1: Primitive Vertex Parameter has Z</td>
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<td></td>
<td><strong>Bit [20]: W Parameter Mask</strong></td>
</tr>
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<td></td>
<td></td>
<td></td>
<td>0: Primitive Vertex Parameter does not have W thus use default value (***)</td>
</tr>
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<td></td>
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<td>1: Primitive Vertex Parameter has W</td>
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<tr>
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<td></td>
<td><strong>Bit [19]: Reserved</strong></td>
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<tr>
<td></td>
<td></td>
<td></td>
<td><strong>Bit [18]: Cd (C0) Parameter Mask</strong></td>
</tr>
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<td></td>
<td>0: Primitive Vertex Parameter does not have Diffuse Color, ARGB thus use default value (***)</td>
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<td></td>
<td>1: Primitive Vertex Parameter has Diffuse Color, ARGB</td>
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<tr>
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<td></td>
<td></td>
<td><strong>Bit [17]: Cs (C1) Parameter Mask</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Primitive Vertex Parameter does not have Specula Color, SR SG SB, and SA thus use default value (***)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Primitive Vertex Parameter has Specula Color, SR SG SB, and SA</td>
</tr>
<tr>
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<td></td>
<td></td>
<td><strong>Bit [16]: Fog-Factor Parameter Mask</strong></td>
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<td>0: Primitive Vertex Parameter does not have Fog Factor thus use default value (***)</td>
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<td></td>
<td></td>
<td>1: Primitive Vertex Parameter has Fog Factor</td>
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<tr>
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<td></td>
<td></td>
<td><strong>Bit [15]: Texture 0’s S Parameter Mask</strong></td>
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<td></td>
<td>0: Primitive Vertex Parameter does not have Texture Coordinate S thus use default value (***)</td>
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<td></td>
<td></td>
<td>1: Primitive Vertex Parameter has Texture Coordinate S</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><strong>Bit [14]: Texture 0’s T Parameter Mask</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Primitive Vertex Parameter does not have Texture Coordinate T thus use default value (***)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Primitive Vertex Parameter has Texture Coordinate T</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><strong>Bit [13]: Texture 0’s R Parameter Mask</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Primitive Vertex Parameter does not have Texture Coordinate R thus use default value (***)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Primitive Vertex Parameter has Texture Coordinate R</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><strong>Bit [12]: Texture 0’s Q Parameter Mask</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Primitive Vertex Parameter does not have Texture Coordinate Q thus use default value (***)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Primitive Vertex Parameter has Texture Coordinate Q</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><strong>Bit [11]: Texture 1’s S Parameter Mask</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Primitive Vertex Parameter does not have Texture Coordinate S thus use default value (***)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Primitive Vertex Parameter has Texture Coordinate S</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><strong>Bit [10]: Texture 1’s T Parameter Mask</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Primitive Vertex Parameter does not have Texture Coordinate T thus use default value (***)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Primitive Vertex Parameter has Texture Coordinate T</td>
</tr>
</tbody>
</table>
Bit [9]: Texture 1’s R Parameter Mask
0: Primitive Vertex Parameter does not have Texture Coordinate R thus use default value (**)
1: Primitive Vertex Parameter has Texture Coordinate R

Bit [8]: Texture 1’s Q Parameter Mask
0: Primitive Vertex Parameter does not have Texture Coordinate Q thus use default value (**)
1: Primitive Vertex Parameter has Texture Coordinate Q

Bit [7]: Texture 2’s S Parameter Mask
0: Primitive Vertex Parameter does not have Texture Coordinate S thus use default value (**)
1: Primitive Vertex Parameter has Texture Coordinate S

Bit [6]: Texture 2’s T Parameter Mask
0: Primitive Vertex Parameter does not have Texture Coordinate T thus use default value (**)
1: Primitive Vertex Parameter has Texture Coordinate T

Bit [5]: Texture 2’s R Parameter Mask
0: Primitive Vertex Parameter does not have Texture Coordinate R thus use default value (**)
1: Primitive Vertex Parameter has Texture Coordinate R

Bit [4]: Texture 2’s Q Parameter Mask
0: Primitive Vertex Parameter does not have Texture Coordinate Q thus use default value (**)
1: Primitive Vertex Parameter has Texture Coordinate Q

Bit [3]: Texture 3’s S Parameter Mask
0: Primitive Vertex Parameter does not have Texture Coordinate S thus use default value (**)
1: Primitive Vertex Parameter has Texture Coordinate S

Bit [2]: Texture 3’s T Parameter Mask
0: Primitive Vertex Parameter does not have Texture Coordinate T thus use default value (**)
1: Primitive Vertex Parameter has Texture Coordinate T

Bit [1]: Texture 3’s R Parameter Mask
0: Primitive Vertex Parameter does not have Texture Coordinate R thus use default value (**)
1: Primitive Vertex Parameter has Texture Coordinate R

Bit [0]: Texture 3’s Q Parameter Mask
0: Primitive Vertex Parameter does not have Texture Coordinate Q thus use default value (**)
1: Primitive Vertex Parameter has Texture Coordinate Q

HParaType = 04h, Sub-Address = 29h
Vertex Buffer & Primitive Setting 10

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:16</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 15:0        | WO        | xxh     | Vertex Parameter Mask  
|              |           |         | Note that the "(**)" is controlled by HVPDF_XX’s Setting |

Bit [15]: Texture 4’s S Parameter Mask
0: Primitive Vertex Parameter does not have Texture Coordinate S thus use default value (**)
1: Primitive Vertex Parameter has Texture Coordinate S

Bit [14]: Texture 4’s T Parameter Mask
0: Primitive Vertex Parameter does not have Texture Coordinate T thus use default value (**)
1: Primitive Vertex Parameter has Texture Coordinate T

Bit [13]: Texture 4’s R Parameter Mask
0: Primitive Vertex Parameter does not have Texture Coordinate R thus use default value (**)
1: Primitive Vertex Parameter has Texture Coordinate R

Bit [12]: Texture 4’s Q Parameter Mask
0: Primitive Vertex Parameter does not have Texture Coordinate Q thus use default value (**)
1: Primitive Vertex Parameter has Texture Coordinate Q

Bit [11]: Texture 5’s S Parameter Mask
0: Primitive Vertex Parameter does not have Texture Coordinate S thus use default value (**)
1: Primitive Vertex Parameter has Texture Coordinate S

Bit [10]: Texture 5’s T Parameter Mask
### 0: Primitive Vertex Parameter does not have Texture Coordinate T thus use default value (**)  
1: Primitive Vertex Parameter has Texture Coordinate T

**Bit [9]: Texture 5’s R Parameter Mask**  
0: Primitive Vertex Parameter does not have Texture Coordinate R thus use default value (**)  
1: Primitive Vertex Parameter has Texture Coordinate R

**Bit [8]: Texture 5’s Q Parameter Mask**  
0: Primitive Vertex Parameter does not have Texture Coordinate Q thus use default value (**)  
1: Primitive Vertex Parameter has Texture Coordinate Q

**Bit [7]: Texture 6’s S Parameter Mask**  
0: Primitive Vertex Parameter does not have Texture Coordinate S thus use default value (**)  
1: Primitive Vertex Parameter has Texture Coordinate S

**Bit [6]: Texture 6’s T Parameter Mask**  
0: Primitive Vertex Parameter does not have Texture Coordinate T thus use default value (**)  
1: Primitive Vertex Parameter has Texture Coordinate T

**Bit [5]: Texture 6’s R Parameter Mask**  
0: Primitive Vertex Parameter does not have Texture Coordinate R thus use default value (**)  
1: Primitive Vertex Parameter has Texture Coordinate R

**Bit [4]: Texture 6’s Q Parameter Mask**  
0: Primitive Vertex Parameter does not have Texture Coordinate Q thus use default value (**)  
1: Primitive Vertex Parameter has Texture Coordinate Q

**Bit [3]: Texture 7’s S Parameter Mask**  
0: Primitive Vertex Parameter does not have Texture Coordinate S thus use default value (**)  
1: Primitive Vertex Parameter has Texture Coordinate S

**Bit [2]: Texture 7’s T Parameter Mask**  
0: Primitive Vertex Parameter does not have Texture Coordinate T thus use default value (**)  
1: Primitive Vertex Parameter has Texture Coordinate T

**Bit [1]: Texture 7’s R Parameter Mask**  
0: Primitive Vertex Parameter does not have Texture Coordinate R thus use default value (**)  
1: Primitive Vertex Parameter has Texture Coordinate R

**Bit [0]: Texture 7’s Q Parameter Mask**  
0: Primitive Vertex Parameter does not have Texture Coordinate Q thus use default value (**)  
1: Primitive Vertex Parameter has Texture Coordinate Q

---

**HParaType = 04h, Sub-Address = 2Ah**  
Vertex Buffer & Primitive Setting 11

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 23:0        | WO        | xxh     | Point’s Default Width as Floating s[8].15  
When point size comes from FVF, this setting is as the maximum value of point size.  
Point Sprite is not only useful for 3D AP, but also for 2D and video AP. This can be considered as just filled a rectangle and make use of all those 3D features at the same time.  
The maximum value is 2048.0. The minimum value is 1.0.  
If (HFVFMask of “point size” is “0”, and primitive type is point)  
Point_width = HVPointW  
Else  
Point_width = max(HVPointH, min(HVPointW, value from Primitive Vertex data’s “point_size”)) |

**HParaType = 04h, Sub-Address = 2Bh**  
Vertex Buffer & Primitive Setting 12

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 23:0        | WO        | xxh     | Point’s Default Hight as Floating s[8].15  
When point size comes from FVF, this setting is as the minimum value of point size.  
The maximum value is 2048.0. The minimum value is 1.0. |
### HParaType = 04h, Sub-Address = 2Ch
**Vertex Buffer & Primitive Setting 13**

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:0</td>
<td>WO</td>
<td>xxh</td>
<td>Lower 24 Bits for Maximum Value of Vertex Buffer’s Index</td>
</tr>
</tbody>
</table>

### HParaType = 04h, Sub-Address = 2Dh
**Vertex Buffer & Primitive Setting 14**

<table>
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<th>Attribute</th>
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<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:0</td>
<td>WO</td>
<td>xxh</td>
<td>Lower 24 Bits for Minimum Value of Vertex Buffer’s Index</td>
</tr>
</tbody>
</table>

### HParaType = 04h, Sub-Address = 2Eh
**Vertex Buffer & Primitive Setting 15**

<table>
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<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:16</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>15:8</td>
<td>WO</td>
<td>xxh</td>
<td>Higher 8 Bits for Maximum Value of Vertex Buffer’s Index</td>
</tr>
<tr>
<td>7:0</td>
<td>WO</td>
<td>xxh</td>
<td>Higher 8 Bits for Minimum Value of Vertex Buffer’s Index</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>If (index of vertex &gt; HVBIndexMax</td>
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</table>

### HParaType = 04h, Sub-Address = 2Fh
**Vertex Buffer & Primitive Setting 16**

<table>
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<th>Attribute</th>
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<th>Description</th>
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<tbody>
<tr>
<td>23</td>
<td>WO</td>
<td>xxh</td>
<td>Default Value for Vertex Parameter Z</td>
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<td>0: Default value is 0.0</td>
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<tr>
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<td>1: Default value is 1.0</td>
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<tr>
<td>22</td>
<td>WO</td>
<td>xxh</td>
<td>Default Value for Vertex Parameter W</td>
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<td>0: Default value is 0.0</td>
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<td></td>
<td></td>
<td></td>
<td>1: Default value is 1.0</td>
</tr>
<tr>
<td>21</td>
<td>WO</td>
<td>xxh</td>
<td>Default Value for Vertex Parameter Fog</td>
</tr>
<tr>
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<td></td>
<td></td>
<td>0: Default value is 0.0</td>
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<tr>
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<td></td>
<td></td>
<td>1: Default value is 1.0</td>
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<tr>
<td>20</td>
<td>WO</td>
<td>xxh</td>
<td>Default Value for Vertex Parameter Color 0</td>
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<td>1: Default value is 1.0</td>
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<tr>
<td>19</td>
<td>WO</td>
<td>xxh</td>
<td>Default Value for Vertex Parameter Alpha 0</td>
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<td>1: Default value is 1.0</td>
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<td>18</td>
<td>WO</td>
<td>xxh</td>
<td>Default Value for Vertex Parameter Color 1</td>
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<td>0: Default value is 0.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Default value is 1.0</td>
</tr>
<tr>
<td>17</td>
<td>WO</td>
<td>xxh</td>
<td>Default Value for Vertex Parameter Alpha 1</td>
</tr>
<tr>
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<td></td>
<td></td>
<td>0: Default value is 0.0</td>
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<td></td>
<td></td>
<td></td>
<td>1: Default value is 1.0</td>
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<tr>
<td>16</td>
<td>WO</td>
<td>xxh</td>
<td>Default Value for Vertex Parameter Texture Coordinate S</td>
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<td></td>
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<td>1: Default value is 1.0</td>
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<td>15</td>
<td>WO</td>
<td>xxh</td>
<td>Default Value for Vertex Parameter Texture Coordinate T</td>
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<td></td>
<td></td>
<td>1: Default value is 1.0</td>
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<tr>
<td>14</td>
<td>WO</td>
<td>xxh</td>
<td>Default Value for Vertex Parameter Texture Coordinate R</td>
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<td></td>
<td>1: Default value is 1.0</td>
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<td>13</td>
<td>WO</td>
<td>xxh</td>
<td>Default Value for Vertex Parameter Texture Coordinate Q</td>
</tr>
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<td>0: Default value is 0.0</td>
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</tr>
<tr>
<td>12:10</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
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### 3D Registers

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<th>Description</th>
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</thead>
<tbody>
<tr>
<td>23:0</td>
<td>WO xxh</td>
<td></td>
<td>Lower 3 Bytes of Scaling for X Transform</td>
</tr>
</tbody>
</table>

**HParaType = 04h, Sub-Address = 40h**

Clipping Window to Screen Window Transformation Setting 2

<table>
<thead>
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<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:0</td>
<td>WO xxh</td>
<td></td>
<td>Lower 3 Bytes of Offset for X Transform</td>
</tr>
</tbody>
</table>

**HParaType = 04h, Sub-Address = 41h**

Clipping Window to Screen Window Transformation Setting 3

<table>
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<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:16</td>
<td>WO xxh</td>
<td></td>
<td>Reserved</td>
</tr>
<tr>
<td>15:8</td>
<td>WO xxh</td>
<td></td>
<td>Higher Byte of Offset for X Transform</td>
</tr>
<tr>
<td>7:0</td>
<td>WO xxh</td>
<td></td>
<td>Higher Byte of Scaling for X Transform</td>
</tr>
</tbody>
</table>

Note to Driver: There are 2 enable settings for Point Sprite, “HenPSprite” and “HVPenPSpriteTXn”, where n is from A to J. For OpenGL, the “HVPenPSpriteTXn” are used to set point sprite for each texture. But for D3D, “HenPSprite” is used to set point sprite for ALL textures. HW would do point sprite if any one of the 2 registers is true. That is

For (n = A to J):

If ((PMType is “point or “triangle point”) & (HenPSprite | HVPenPSpriteTXn))

Texture n is setup as “Point Sprite”

**HParaType = 04h, Sub-Address = 30-3Fh: Reserved** (for Vertex Buffer & Primitive Setting)
### Clipping Window to Screen Window Transformation Setting 4

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:0</td>
<td>WO</td>
<td>xxh</td>
<td>Lower 3 Bytes of Scaling for Y Transform</td>
</tr>
</tbody>
</table>

### Clipping Window to Screen Window Transformation Setting 5

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:0</td>
<td>WO</td>
<td>xxh</td>
<td>Lower 3 Bytes of Offset for Y Transform</td>
</tr>
</tbody>
</table>

### Clipping Window to Screen Window Transformation Setting 6

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:16</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>15:8</td>
<td>WO</td>
<td>xxh</td>
<td>Higher Byte of Offset for Y Transform</td>
</tr>
<tr>
<td>7:0</td>
<td>WO</td>
<td>xxh</td>
<td>Higher Byte of Scaling for Y Transform</td>
</tr>
</tbody>
</table>

### Clipping Window to Screen Window Transformation Setting 7

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:0</td>
<td>WO</td>
<td>xxh</td>
<td>Lower 3 Bytes of Scaling for Z Transform</td>
</tr>
</tbody>
</table>

### Clipping Window to Screen Window Transformation Setting 8

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:0</td>
<td>WO</td>
<td>xxh</td>
<td>Lower 3 Bytes of Offset for Z Transform</td>
</tr>
</tbody>
</table>

### Clipping Window to Screen Window Transformation Setting 9

<table>
<thead>
<tr>
<th>Bits [23:0]</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:16</td>
<td>WO</td>
<td>xxh</td>
<td>A Threshold Value For More Accurate Area Calculating &lt;HC2SXYEmax4Area&gt;</td>
</tr>
</tbody>
</table>

A threshold value of screen coordinate’s Exponential part for more accurate area calculation.

If any screen coordinate’s exponential is over “HC2SXYEmax4Area”, the area calculating equation would be

\[ XbYc – XbYa – XaYc – XcYb + XcYa + XaYb \]

And add each term in the order from absolute largest to the absolute smallest.

Note to HW: The minimum value of HC2SXYEmax4Area is 19+127 (that is 2^19). HW has to check and makes adjustment as

Used HC2SXYEmax4Area = max(146, decoded HC2SXYEmax4Area). Thus the original patterns won’t be re-generated.

| 15:8        | WO        | xxh     | Higher Byte of Offset for Z Transform |
| 7:0         | WO        | xxh     | Higher Byte of Scaling for Z Transform |

### Clipping Window to Screen Window Transformation Setting 49-4Fh: Reserved

(for Clipping Window to Screen Window Transformation Setting)
### HParaType = 04h, Sub-Address = 50h
Clipping Window to Screen Window Transformation Setting 10

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[23:0]</td>
<td>WO</td>
<td>xxh</td>
<td>Lower 3 Bytes of Upper Clamping Value for Screen Coordinate</td>
</tr>
</tbody>
</table>

### HParaType = 04h, Sub-Address = 51h
Clipping Window to Screen Window Transformation Setting 11

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[23:0]</td>
<td>WO</td>
<td>xxh</td>
<td>Lower 3 Bytes of Down Clamping Value for Screen Coordinate</td>
</tr>
</tbody>
</table>

### HParaType = 04h, Sub-Address = 52h
Clipping Window to Screen Window Transformation Setting 12

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[23:16]</td>
<td>WO</td>
<td>xxh</td>
<td>Maximum Exponential Value Clipped Screen Coordinate &lt;HC2SXYEmax4CL&gt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>If the clipped new vertex’s screen coordinate is over ±2^{HC2SXYEmax4CL}, re-generate this clipped vertex to a smaller screen coordinate.</td>
</tr>
<tr>
<td>[7:0]</td>
<td>WO</td>
<td>xxh</td>
<td>Higher Byte of Down Clamping Value for Screen Coordinate</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>If (Xs &gt;= HC2SXYUClamp) Xs = HC2SXYUClamp Else if (Xs &lt;= HC2SXYDClamp) Xs = *HC2SXYDClamp</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>If (Ys &gt;= HC2SXYUClamp) Ys = HC2SXYUClamp Else if (Ys &lt;= HC2SXYDClamp) Ys = HC2SXYDClamp</td>
</tr>
</tbody>
</table>

### HParaType = 04h, Sub-Address AAh
Software Inspection

<table>
<thead>
<tr>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[23:16]</td>
<td>WO</td>
<td>xxh</td>
<td>Reserved</td>
</tr>
<tr>
<td>[15:0]</td>
<td>WO</td>
<td>xxh</td>
<td>Flag Number for SW Inspection</td>
</tr>
</tbody>
</table>

### HParaType 10h: Commands for Command Regulator

Refer to CR Chapter’s “HParaType 10h: Commands for Command Regulator” for more details.

### HParaType 11h: Commands for Frame Buffer Swapping and CR’s Miscellaneous Setting

Refer to CR Chapter’s “HParaType 11h: Commands for Frame Buffer Swapping and CR’s Miscellaneous Setting” for more details.