Open Graphics Programming Manual

Chrome9 HD Graphics Processor

VX900 Series System Processor

Part I: Graphics Core / 2D

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INTRODUCTION

This document contains detailed graphics registers descriptions and other general information for the Chrome9 HD graphics engine. The graphics registers for the Chrome9 HD main features and its underlying subsystems are described explicitly in the following chapters.

About This Programming Guide

The programming manual is organized into 2 volumes (Part I & Part II). A brief description of each chapter is given below:

Part I:

Introduction.

An overview of the Chrome9 HD design features is given in this chapter, along with block diagram and product model.

Register Overview

Register specifications for register addressing and I/O space division are shown in this chapter.

AGP Graphics Control Register Descriptions

This chapter provides detailed AGP graphics control register descriptions. Those registers locate in PCI configuration space Device 0 Function 1.

VGA I/O Register Descriptions

This chapter provides detailed VGA-related register descriptions. The various video modes supported by the Chrome9 HD controller are also included in the configuration section.

2D Engine Register Descriptions

This chapter provides detailed 2D Engine register summary and descriptions.

DMA Register Descriptions

This chapter provides detailed DMA register summary and descriptions.

CBU Rotation Register Descriptions

This chapter provides detailed CBU rotation register summary and descriptions.

LVDS and DVI Register Descriptions

This chapter provides detailed LVDS and DVI register descriptions.

Display Port Register Descriptions

This chapter provides detailed Display Port register descriptions.

Part II:

Video Register Descriptions

This chapter provides both detailed video display engine register and video capture engine register summary and descriptions.

HQV Register Descriptions

This chapter provides detailed HQV register summary and descriptions.

Command Regulator (CR) Register Descriptions

This chapter provides detailed CR register descriptions.

3D Engine Register Descriptions

This chapter provides detailed 3D Engine register descriptions.

REGISTER OVERVIEW

In the register descriptions, column “Default” indicates the default value of register bit, while column “Attribute” indicates access type of register bit.

Abbreviation

Basic Attributes: *indicate common read-write operations.*

RO:	Read Only.
WO:	Write Only. (register value can not be read by the software)
RW:	Read / Write.
RW1:	Write Once then Read Only after that.
RW1C:	Read / Write of “1” clears bit to zero.

Sticky Attributes**:** adding an “S” in tail to indicate a sticky register, which means that register will not be set or altered by hot reset.

ROS:	Sticky-Read-Only.
WOS:	Sticky-Write-Only.
RWS:	Sticky-Read/Write.
RW1S:	Sticky-Write-Once.
RW1CS:	Sticky-Write-1-to-Clear.

Default Value Definitions

Dip: Means the default value is set by dip switch or strapping.
HwInit: Hardware initialized; bit default value is set by hardware to reflect related status.
ROMSIP: The default will be overwritten by the value defined in ROMSIP after system reset.

I/O Address Space

The I/O space of the Chrome9 HD processor is divided into the following subspaces for various functions of the processor:

- PCI Interface: PCI/AGP/Power Management configuration space
- VGA space
- Extended I/O space
- Secondary Display Engine / LCD Display
- 2D engine space
- 3D engine space
- Command regulator space
- Video Playback / Blending / Video Capture / HQV engines space
- LVDS / DVI space
- Display port space
- PCI Interface
- HQV space
- DMA engine space
- CBU engine space

Table 1 lists the various I/O space categories and their corresponding I/O addresses for the Chrome9 HD processor. Please note that in the monochrome mode, the "X" contained within the I/O addresses stands for **"B",** and in the color mode the "X" stands for **"D".**

Table 1. Chrome9 HD Processor I/O Space

Categories	I/O Address
PCI Interface	PCI Configuration Space
VGA Space	Standard VGA Space
Extended I/O Space	3C5.10 ~ 3C5.FF / 3CF.20 ~ 3CF.2F / 3X5.30 ~ 3X5.4F
Secondary Display Engine / LCD Display	3X5.50 ~ 3X5.FD

Memory Address Space

Memory Mapped I/O Register Address Spaces for Graphics Control

There are three memory spaces implemented in the Chrome9 HD graphics processor:

1. Starting from GFX Memory Base 0, **MB0**, there is a **512MB** memory space reserved for MMIO of AES.
2. Starting from GFX Memory Base 1**, MB1**, there is a **16MB** memory space reserved for **memory-mapped I/O**, 2D Host BitBLT space and burst **command area**.
3. Starting from GFX Memory Base 2, **MB2**, there is a **512MB** memory space reserved as the graphics and video playback buffer.(Named as **S.L.** – System Local Frame Buffer), for the lower 32bit for 32bit BAR.
4. Starting from GFX Memory Base 2, **MB2**, there is a **512MB** memory space reserved as the graphics and video playback buffer. (Named as **L.L.** – Local Memory Local Frame Buffer, and dedicated for Graphics), for the 64 Bits BAR.

MB0 is declared in the register with offset address 10h~13h in the D1F0 PCI configuration space.

MB1 is declared in the register with offset address 14h~17h in the D1F0 PCI configuration space.

MB2 is declared in the register with offset address 18h~1Bh in the D1F0 PCI configuration space.

Table 2. MMIO Address Space Partition Table for MB0

Memory Range (Note)	Usage
0 ~ 2M-1:	
0x00000000 ~ 0x000001FF	2D Engine Register Space
0x00000200 ~ 0x000003FF	Video Related Engines Register Space 1
0x00000400 ~ 0x000007FF	3D Engine Register Space
0x00000800 ~ 0x00000BFF	Burst Command Area
0x00000C00 ~ 0x00000DFF	Reserved
0x00000E00 ~ 0x00000FFF	DMA(AGP) Register Space
0x00001200 ~ 0x000013FF	Video Related Engines Register Space 2
0x00001C00 ~ 0x00001DFF	WMV MC Register Space
0x00001E00 ~ 0x00001FFF	CBU Rotate Related
0x00002200 ~ 0x000023FF	Extended Video Engines Register Space 1
0x00002E00 ~ 0x00002FFF	DMA(AGP) Register Space 2
0x00003200 ~ 0x000033FF	Extended Video Engines Register Space 2
0x000083CX ~ 0x000083DX	VGA memory mapped IO Space
0x0000C000 ~ 0x0000C1FF	Reserved
0x0000C200 ~ 0x0000C5FF	Reserved
2M ~ 4M-1	**2D Host BitBLT Space**
4M ~ 8M-1	**Burst Command Area**
8M ~ 16M-1	**Reserved**

AGP GRAPHICS CONTROL REGISTER: DEVICE 1 FUNCTION 0 (D1F0)

PCI Configuration Space

This section provides a complete overview for AGP graphics control registers. Those registers are located in PCI configuration space and should be programmed using PCI configuration mechanism through I/O registers CF8 / CFC with bus number 0, device number 1 and function number 0.

Supported PCI Commands

Table 3 shows the PCI commands supported by the Chrome9 HD graphic processor. The Chrome9 HD processor complies with the PCI bus interface protocol, Rev. 2.2. The design clock rate is 66 MHz and both of master and slave modes are supported.

Table 3. PCI Command

Command Code	Command
0000	**Interrupt Acknowledge**
0001	**Special**
0010	I/O Read
0011	I/O Write
0100	**Reserved**
0101	**Reserved**
0110	Memory Read
0111	Memory Write
1000	**Reserved**
1001	**Reserved**
1010	Configuration Read
1011	Configuration Write
1100	Memory Read Multiple; treated as 0110 memory read
1101	**Dual Address**
1110	Memory Read Line; treated as 0110 memory read
1111	Memory Write and Invalid; treated as 0111 memory write

Note: The command codes in **bold** are not supported in Chrome9 HD.

PCI Register Summary

The following table summarizes the Device 1 Function 0 PCI configuration registers of this chip. This table also documents the power-on default value ("Default") and attribute ("Attribute") for each register. Access type definitions used are RW (Read/Write), RO (Read/Only) and RW1C (Read / Write of "1" clears bit to zero). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RW1C may have some read-only or read write bits (see individual register descriptions for details). All default values are shown in hexadecimal unless otherwise indicated.

Table 4. PCI Configuration Registers

Offset Address	Normal PCI Configuration Area	Default Value	Attribute
01-00h	VIA Technology ID	1106h	RO
03-02h	Device ID	7122h	RO
05-04h	PCI Command	0000h	RW
07-06h	PCI Status	0010h	RW
08h	Revision ID	00h	RO
0B-09h	Class Code	03 0000h	RO
13-10h	Memory Base 0 Address (MMIO) for AES/Video IP	0000 0000 0000 0004h	RW
17-14h	Memory Base 1 Address (MMIO) for GFXCTL	0000 0000 0000 0000h	RW
1B-18h	Memory Base 2 Address (S.L.) Lower 32-bit for 32 Bits BAR	0000 0000 0000 000Ch	RW
1F-1Ch	Memory Base 2 Address (S.L.) Upper 32-bit for 64 Bits BAR	0000 0000 0000 0000h	RW
2D-2Ch	Subsystem Vendor ID	1106h	RO
2F-2Eh	Subsystem ID	7122h	RO
33-30h	ROM Base Address	0000 0000h	RW
34h	Capabilities Pointer	60h	RO
3Ch	Interrupt Line	00h	RW
3Dh	Interrupt Pin	01h	RO

Offset Address	Power Management Configuration Area	Default Value	Attribute
60h	Capability ID (01h)	01h	RO
61h	Next Item Pointer	90h	RO
63-62h	Power Management Capability	0622h	RO
65-64h	Power Management Control / Status	0000h	RO / RW
67-66h	Data + PMCSR_BSE	0000h	RO

Offset Address	PCI Express Configuration Area	Default Value	Attribute
70h	PCI Express Cap ID	10h	RO
71h	Next Cap Pointer	00h	RO
73-72h	PCI Express Capabilities	0091h	RO
77-74h	Device Capabilities	0000 0000h	RO
79-78h	Device Control	0000h	RW
7B-7Ah	Device Status	0000h	RO

Offset Address	MSI Configuration Area	Default Value	Attribute	Bit
90h	MSI Capability ID	05h	RO	7:0
91h	Next Cap Pointer	00h	RO	7:0
93-92h	Message Control	0000h	RW	15:0
9B~94h	Message Address	0	RW	63:0
9D~9Ch	Message Data	0000h	RW	15:0

Offset Address	VIA GFX Configuration Area	Default Value	Attribute	Bit
B0h	Memory Base Control Register	00h	RW	7:0
B1h	Reserved	00h	RW	7:0
B2h	Memory Base 2 Size (S.L.)	00h	RW	7:0

Header Registers (00-3Fh)

Offset Address: 01-00h (D1F0)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technology ID**

Offset Address: 03-02h (D1F0)

Device ID **Default Value: 7122h**

Bit	Attribute	Default	Description
15:0	RO	7122h	**Device ID**

Offset Address: 05-04h (D1F0)

PCI Command **Default Value: 0000h**

Bit	Attribut	Default	Description
15:11	RO	0	**Reserved**
10	RW	0	**Interrupt Disable** 0: Disable 1: Enable
9	RW	0	**Fast Back-to-Back Enable** 0: Disable 1: Enable
8	RW	0	**SERR# Enable** 0: Disable 1: Enable
7	RW	0	**Wait Cycle Control** 0: Disable 1: Enable
6	RW	0	**Parity Error Response** 0: Disable 1: Enable
5	RW	0	**VGA Palette Snoop** 0: Disable 1: Enable
4	RW	0	**Memory Write and Invalidate Enable** 0: Disable 1: Enable
3	RW	0	**Special Cycle** 0: Disable 1: Enable
2	RW	0	**Bus Master** 0: Disable 1: Enable
1	RW	0	**Memory Space** 0: Disable 1: Enable
0	RW	0	**IO Space** 0: Disable 1: Enable

Offset Address: 07-06h (D1F0)

PCI Status **Default Value: 0010h**

Bit	Attribut	Default	Description
15	RW1C	0	**Detected Parity Error** Assert 1 whenever a parity error is detected.
14	RO	0	**Signaled System Error**
13	RW1C	0	**Received Master Abort** Assert 0 when a master abort is detected.
12	RW1C	0	**Received Target Abort** Assert 0 when a target abort is detected.
11	RW	0	**Signaled Target Abort**
10:9	RO	00b	**DEVSEL# Timing** 00: Fast 01: Medium 10: Slow 11: Reserved
8	RO	0	**Master Data Parity Error**
7	RO	0	**Fast Back-to-back Capable**
6	RO	0	**Reserved**
5	RO	0	**66MHz Capable**
4	RO	1b	**Capabilities List** Presence the extended capability list.
3	RW	0	**Interrupt Status** 1: Assert an interrupt at the INTA#.
2:0	RO	0	**Reserved**

Offset Address: 08h (D1F0)

Revision ID **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**Revision ID**

Offset Address: 0B-09h (D1F0)

Class Code **Default Value: 03 0000h**

Bit	Attribute	Default	Description
23:0	RO	03 0000h	**Class Code**

Offset Address: 13-10h (D1F0)

Memory Base 0 Address (MMIO) for AES / Video IP **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0000 0000h	**Memory Base 0 Address (MMIO) for AES / Video IP**

Offset Address: 17-14h (D1F0)

Memory Base 1 Address (MMIO) for GFXCTL **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0000 0000h	**Memory Base 1 Address (MMIO) for GFXCTL**

Offset Address: 1B-18h (D1F0)

Memory Base 2 Address (S.L.) Lower 32-Bit for 32 Bits BAR **Default Value: 0000 0008h**

Bit	Attribute	Default	Description
31:0	RW	0000 0008h	**Memory Base 2 Address (S.L.) Lower 32 Bits**

Offset Address: 1F-1Ch (D1F0)

Memory Base 2 Address (S.L.) Upper 32-Bit for 64 Bits BAR **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0000 0000h	**Memory Base 2 Address (S.L.) Upper 32 Bits**

Offset Address: 2D-2Ch (D1F0)

Subsystem Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D1F0)

Subsystem ID **Default Value: 1122h**

Bit	Attribute	Default	Description
15:0	RO	1122h	**Subsystem ID**

Offset Address: 33-30h (D1F0)

ROM Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**ROM Base Address**

Offset Address: 34h (D1F0)

Capabilities Pointer **Default Value: 60h**

Bit	Attribute	Default	Description
7:0	RO	60h	**Capabilities Pointer**

Offset Address: 35-3Bh (D1F0) – Reserved

Offset Address: 3Ch (D1F0)

Interrupt Line **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Interrupt Line**

Offset Address: 3Dh (D1F0)

Interrupt Pin **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Interrupt Pin**

Offset Address: 3E-3Fh (D1F0) – Reserved

Reserved Registers (40-5Fh)

Offset Address: 40-5Fh (D1F0) – Reserved

Power Management Configuration Area (60-6Fh)

Offset Address: 60h (D1F0)

Capability ID **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Capability ID**

Offset Address: 61h (D1F0)

Next Item Pointer **Default Value: 90h**

Bit	Attribute	Default	Description
7:0	RO	90h	**Next Item Pointer** Point to MSI capability list

Offset Address: 63-62h (D1F0)

Power Management Capability **Default Value: 0622h**

Bit	Attribut	Default	Description
15:11	RO	0	**Power Management Event (PME) Support**
10	RO	1b	**D2 Support**
9	RO	1b	**D1 Support**
8:6	RO	0	**3.3 Vaux Auxiliary Current**
5	RO	1b	**DSI Device Specific Initialization**
4	RO	0	**Reserved**
3	RO	0	**Power Management Event (PME) Clock**
2:0	RO	010b	**Version** Complies with version 1.1

Offset Address: 65-64h (D1F0)

Power Management Control / Status **Default Value: 0000h**

Bit	Attribut	Default	Description
15	RO	0	**Power Management Event (PME) Status**
14:13	RO	0	**Data Scale**
12:10	RO	0	**Reserved**
9	RO	0	**D1 Select**
8	RO	0	**PME Enable** 0: Disable 1: Enable
7:2	RO	0	**Reserved**
1:0	RW	00b	**Power State** 00: D0 State 01: D1 State 10: D2 State 11: D3 State

Offset Address: 67-66h (D1F0)

Data + PMCSR_BSE **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0	**Data + PMCSR_BSE** Please refer to "partial pages of PCI Power Management Interface Specification v1.2" for detail of PMCSR_BSE .

Offset Address: 68-6Fh (D1F0) – Reserved

PCI Express Configuration Area (70-8Fh)

Offset Address: 71-70h (D1F0)

PCI Express Capability List **Default Value: 0010h**

Bit	Attribute	Default	Description
15:8	RO	00h	**Next Capability Pointer** Point to MSI capability list.
7:0	RO	10h	**Capability ID**

Offset Address: 73-72h (D1F0)

PCI Express Capabilities **Default Value: 0091h**

Bit	Attribute	Default	Description
15:14	RO	0	**Reserved**
13:9	RO	0	**Interrupt Message Number**
8	RO	0	**Slot Implemented**
7:4	RO	1001b	**Device / Port Type** PCI Express Legacy Endpoint
3:0	RO	0001b	**Capability Version**

Offset Address: 77-74h (D1F0)

Device Capabilities **Default Value: 0000 0000h**

Bit	Attribut	Default	Description
31:28	RO	0	**Reserved**
27:26	RO	0	**Captured Slot Power Limit Scale**
25:18	RO	0	**Captured Slot Power Limit Value**
17:15	RO	0	**Reserved**
14	RO	0	**Power Indicator Present**
13	RO	0	**Attention Indicator Present**
12	RO	0	**Attention Button Present**
11:9	RO	0	**Endpoint L1 Acceptable Latency** Less than 1μs
8:6	RO	0	**Endpoint L0s Acceptable Latency** Less than 64ns
5	RO	0	**Extended Tag Field Supported** 5-bit tag field supported
4:3	RO	0	**Phantom Functions Supported** No phantom function
2:0	RO	0	**Max_Payload_Size Supported**

Offset Address: 79-78h (D1F0)

Device Control **Default Value: 0000h**

Bit	Attribut	Default	Description
15	RO	0	**Reserved**
14:12	RW	0	**Max_Read_Request_Size** Max. 128 Bytes read request
11	RW	0	**Enable No Snoop**
10	RW	0	**Auxiliary (AUX) Power PM Enable** 0: Disable 1: Enable
9	RW	0	**Phantom Functions Enable** 0: Disable 1: Enable
8	RW	0	**Extended Tag Field Enable** 0: Disable 1: Enable
7:5	RW	0	**Max_Payload_Size**
4	RW	0	**Enable Relaxed Ordering** 0: Disable 1: Enable
3	RW	0	**Unsupported Request Reporting Enable** 0: Disable 1: Enable
2	RW	0	**Fatal Error Reporting Enable** 0: Disable 1: Enable
1	RW	0	**Non-Fatal Error Reporting Enable** 0: Disable 1: Enable
0	RW	0	**Correctable Error Reporting Enable** 0: Disable 1: Enable

Offset Address: 7B-7Ah (D1F0)

Device Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:6	RO	0	**Reserved**
5	RO	0	**Transitions Pending**
4	RO	0	**Auxiliary (AUX) Power Detected**
3	RO	0	**Unsupported Request Detected**
2	RO	0	**Fatal Error Detected**
1	RO	0	**Non-Fatal Error Detected**
0	RO	0	**Correctable Error Detected**

Offset Address: 7C-8Fh (D1F0) – Reserved

MSI Configuration Area (90-9Fh)

Offset Address: 91-90h (D1F0)

MSI Capability List **Default Value: 0005h**

Bit	Attribute	Default	Description
15:8	RO	0	**Next Capability Pointer**
7:0	RO	05h	**Capability ID**

Offset Address: 93-92h (D1F0)

Message Control **Default Value: 0080h**

Bit	Attribute	Default	Description
15:8	RO	0	**Reserved**
7	RW	1b	**64 Bits Address Capable**
6:4	RW	000b	**Multiple Message Enable**
3:1	RW	000b	**Multiple Message Capable** A message request
0	RW	0	**MSI Enable** 0: Disable 1: Enable

Offset Address: 9B-94h (D1F0)

Message Address **Default Value: 0**

Bit	Attribute	Default	Description
63:2	RW	0	**Message Address** System specified data.
1:0	RO	0	**Reserved**

Offset Address: 9D-9Ch (D1F0)

Message Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Message Data** System specified data.

Offset Address: 9E-9Fh (D1F0) – Reserved

Reserved Registers (A0-AFh)

Offset Address: A0-AFh (D1F0) – Reserved

VIA GFX Configuration Area (B0-FFh)

Offset Address: B0h (D1F0)

Memory Base Control Register **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**64-bit SL Support** 0: Disable 1: Enable
6	RW	0	**Disable AES/Video IP PCI command Path (DS to AES/Video IP)** 0: Disable 1: Disable
5	RW	0	**Reserved**
4	RO	0	**Reserved**
3	RW	0	**UNLOCK**
2	RW	0	**S.L. Disable** 0: Reserved 1: Disable
1	RW	0	**L.L. Disable** 0: Reserved 1: Disable
0	RW	0	**VGA Memory Selection** 0: Reserved (VGA in L.L) 1: VGA in S.L.

Offset Address: B1h (D1F0) – Reserved

Offset Address: B2h (D1F0)

Memory Base 2 Size (S.L.) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:0	RW	000 0000b	**Memory Base 2 Size** 000 0000: 512MB 100 0000: 256MB 110 0000: 128MB 111 0000: 64MB 111 1000: 32MB 111 1100: 16MB 111 1110: 8MB 111 1111: 4MB

Offset Address: B3-F2h (D1F0) – Reserved

Offset Address: F1-FFh (D1F0) – Reserved

VGA REGISTERS

This chapter provides VGA I/O register summary table, extended IO register summary table, secondary display IO register summary table, IGA1 Display Engine MMIO registers and ther detailed register descriptions are provided in the subsequent sections.

VGA I/O Register Descriptions

These VGA register tables document the I/O port, I/O index, register function and register attribute for each register.

Table 5. VGA I/O Registers

I/O Port (Hex)	I/O Index (Hex)	Attribute Control Register	Attribute
3C0	-	Address	RW
3C1	00 – 0F	Palette	RW
3C1	10	Mode Control	RW
3C1	11	Overscan Color	RW
3C1	12	Color Plane Enable	RW
3C1	13	Horizontal Pixel Panning	RW
3C1	14	Color Select	RW

I/O Port (Hex)	I/O Index (Hex)	General Register	Attribute
3C2	-	Miscellaneous Output	WO
3CC	-	Miscellaneous Output	RO
3C2	-	Input Status 0	RO
3XA	-	Input Status 1	RO
3C3	-	Video Subsystem Enable	RW
46E8	-	Video Adapter Enable	RW

I/O Port (Hex)	I/O Index (Hex)	Sequencer Register	Attribute
3C4	-	Address	RW
3C5	00	Reset	RW
3C5	01	Clocking Mode	RW
3C5	02	Map Mask	RW
3C5	03	Character Map Select	RW
3C5	04	Memory Mode	RW

I/O Port (Hex)	I/O Index (Hex)	Graphic Controller Register	Attribute
3CE	-	Address	RW
3CF	00	Set / Reset	RW
3CF	01	Enable Set / Reset	RW
3CF	02	Color Compare	RW
3CF	03	Data Rotate	RW
3CF	04	Read Map Select	RW
3CF	05	Mode	RW
3CF	06	Miscellaneous	RW
3CF	07	Color Don’t Care	RW
3CF	08	Bit Mask	RW

I/O Port (Hex)	I/O Index (Hex)	CRTC Controller Register	Attribute
3X4	-	Address	RW
3X5	00	Horizontal Total	RW
3X5	01	Horizontal Dipslay End	RW
3X5	02	Horizontal Blank Start	RW
3X5	03	Horizontal Blank End	RW
3X5	04	Horizontal Retrace Start	RW
3X5	05	Horizontal Retrace End	RW
3X5	06	Vertical Total	RW
3X5	07	Overflow	RW
3X5	08	Preset Row Scan	RW
3X5	09	Max Scan Line	RW
3X5	0A	Cursor Start	RW
3X5	0B	Cursor End	RW
3X5	0C	Start Address High	RW
3X5	0D	Start Address Low	RW
3X5	0E	Cursor Location High	RW
3X5	0F	Cursor Location Low	RW
3X5	10	Vertical Retrace Start	RW
3X5	11	Vertical Retrace End	RW
3X5	12	Vertical Display End	RW
3X5	13	Offset	RW
3X5	14	Underline Location	RW
3X5	15	Vertical Blank Start	RW
3X5	16	Vertical Blank End	RW
3X5	17	CRTC Mode Control	RW
3X5	18	Line Compare	RW

Table 6. Extended I/O Registers

I/O Port (Hex)	I/O Index (Hex)	Sequencer Extended Register	Attribute
3C5	10	Extended Register Unlock	RW
3C5	11	Configuration Register 0	RO
3C5	12	Configuration Register 1	RO
3C5	13	Configuration Register 2	RO
3C5	14	Frame Buffer Size Control	RO
3C5	15	Display Mode Control	RW
3C5	16	Display FIFO Threshold Control	RW
3C5	17	Display FIFO Control	RW
3C5	18	Display Arbiter Control 0	RW
3C5	19	Power Management	RW
3C5	1A	PCI Bus Control	RW
3C5	1B	Power Management Control 0	RW
3C5	1C	Horizontal Display Fetch Count Data	RW
3C5	1D	Horizontal Display Fetch Count Control	RW
3C5	1E	Power Management Control	RW
3C5	20	Typical Arbiter Control 0	RW
3C5	21	Typical Arbiter Control 1	RW
3C5	22	Display Arbiter Control 1	RW
3C5	26	IIC Serial Port Control 0	RW
3C5	2A	Power Management Control 5	RW
3C5	2B	DVI and LVDS Interrupt Control	RW
3C5	2C	General Purpose I/O Port	RW
3C5	2D	Power Management Control 1	RW
3C5	2E	Power Management Control 2	RW
3C5	31	IIC Serial Port Control 1	RW
3C5	34-32	Reserved	RO
3C5	36-35	Subsystem Vender ID	RW
3C5	38-37	Subsystem ID	RW
3C5	3A-39	BIOS Reserved Register 1-0	RW
3C5	3B	PCI Revision ID Back Door	RW
3C5	3C	Miscellaneous	RW
3C5	3D	General Purpose I/O Port	RW
3C5	3E	Miscellaneous Register for AGP Mux	RW
3C5	3F	Power Management Control 2	RW
3C5	40	PLL Control	RW
3C5	41	Typical Arbiter Control 1	RW
3C5	42	Typical Arbiter Control 2	RW
3C5	43	Graphics Bonding Option	RO

I/O Port (Hex)	I/O Index (Hex)	Clock Synthesizer Register	Attribute
3C5	44	VCK Clock Synthesizer Value 0	RW
3C5	45	VCK Clock Synthesizer Value 1	RW
3C5	46	VCK Clock Synthesizer Value 2	RW
3C5	47	ECK Clock Synthesizer Value 0	RW
3C5	48	ECK Clock Synthesizer Value 1	RW
3C5	49	ECK Clock Synthesizer Value 2	RW
3C5	4A	Secondary Display (LCDCK) Clock Synthesizer Value 0	RW
3C5	4B	Secondary Display (LCDCK) Clock Synthesizer Value 1	RW
3C5	4C	Secondary Display (LCDCK) Clock Synthesizer Value 2	RW
3C5	4D	Preemptive Arbiter Control	RW
3C5	4E	Software Reset Control	RW
3C5	4F	CR Gating Clock Control	RW
3C5	50	AGP Control Register	RW
3C5	51	Display FIFO Control 1	RW
3C5	52	Integrated TV Shadow Register Control	RW
3C5	53	DAC Sense Control Register 1	RW
3C5	54	DAC Sense Control Register 2	RW
3C5	55	DAC Sense Control Register 3	RW
3C5	56	DAC Sense Control Register 4	RW
3C5	57	Display FIFO Control 2	RW
3C5	58	GFX Power Control Register 1	RW
3C5	59	GFX Power Control Register 2	RW
3C5	5A	PCI Bus Control 2	RW
3C5	5B	Device Used Status 0	RO
3C5	5C	Device Used Status 1	RO
3C5	5D	Timer Control Register	RW
3C5	5E	DAC Control Register 2	RW
3C5	60	I2C Mode Control	RW
3C5	61	I2C Host Address	RW
3C5	62	I2C Host Data	RW
3C5	63	I2C Host Control	RW
3C5	64	I2C Status	RW
3C5	65	Power Management Control 6	RW
3C5	66	GTI Control 0	RW
3C5	67	GTI Control 1	RW
3C5	68	GTI Control 2	RW
3C5	69	GTI Control 3	RW
3C5	6A	GTI Control 4	RW
3C5	6B	GTI Control 5	RW
3C5	6C	GTI Control 6	RW
3C5	6D	GTI Control 7	RW
3C5	6E	GTI Control 8	RW
3C5	6F	GTI Control 9	RW
3C5	70	GARB Control 0	RW
3C5	71	Typical Arbiter Control 2	RW
3C5	72	Typical Arbiter Control 3	RW
3C5	73	Typical Arbiter Control 4	RW
3C5	74	Typical Arbiter Control 5	RW
3C5	75	Typical Arbiter Control 6	RW
3C5	76	Backlight Control 1	RW
3C5	77	Backlight Control 2	RW

I/O Port (Hex)	I/O Index (Hex)	Clock Synthesizer Register	Attribute
3C5	78	Backlight Control 3	RW
3C5	79	GTI Control 10	RW
3C5	7A	GTI Control 11	RW
3C5	7B	GTI Control 12	RW
3C5	7C	GTI Control 13	RW
3C5	7D	Transmitter Power Control 0	RW
3C5	7E ~ A7	Reserved	RO
3C5	A8	V1 Power Mode Control 0	RW
3C5	A9	V1 Power Mode Control 1	RW
3C5	AA	V1 Power Mode Control 2	RW
3C5	AB	V1 Power Mode Control 3	RW
3C5	AC	V1 Power Mode Control 4	RW
3C5	AD	V1 Power Mode Control 5	RW
3C5	AE	V1 Power Mode Control 6	RW
3C5	AF	V1 Power Mode Control 7	RW

I/O Port (Hex)	I/O Index (Hex)	Graphics Controller Extended Register	Attribute
3CF	20	Offset Register Control	RW
3CF	21	Offset Register A	RW
3CF	22	Offset Register B	RW

I/O Port (Hex)	I/O Index (Hex)	CRT Controller Extended Register	Attribute
3X5	30	Display Fetch Blocking Control	RW
3X5	31	Half Line Position	RW
3X5	32	Mode Control	RW
3X5	33	HSYNC Adjuster	RW
3X5	34	Starting Address Overflow	RW
3X5	35	Extended Overflow	RW
3X5	36	Power Management Control 3 (Monitor Control)	RW
3X5	37	DAC Control Register	RW
3X5	38	Signature Data B0	RW
3X5	39	Signature Data B1	RW
3X5	3A	Signature Data B2	RW
3C5	3F-3B	Scratch Pad Register 6-2	RW
3X5	40	Test Mode Control 0	RW
3X5	43	IGA1 Display Control	RW
3X5	44	DAC Sense Data	RW
3X5	45	Extended Horizontal Timing Control	RW
3X5	46	Test Mode Control 1	RW
3X5	47	Test Mode Control 2	RW
3X5	48	Starting Address Overflow	RW
3X5	49-4F	Reserved	RW

Note: In monochrome mode, the “X” in the above table stands for **“B”**
In color mode, the “X” in the above table stands for **“D”.**

Table 7. Secondary Display I/O Registers

I/O Port (Hex)	I/O Index (Hex)	Sequencer Extended Registers	Attribute
3X5	50	Second CRTC Horizontal Total Period	RW
3X5	51	Second CRTC Horizontal Active Data Period	RW
3X5	52	Second CRTC Horizontal Blanking Start	RW
3X5	53	Second CRTC Horizontal Blanking End	RW
3X5	54	Second CRTC Horizontal Blanking Overflow	RW
3X5	55	Second CRTC Horizontal Period Overflow	RW
3X5	56	Second CRTC Horizontal Retrace Start	RW
3X5	57	Second CRTC Horizontal Retrace End	RW
3X5	58	Second CRTC Vertical Total Period	RW
3X5	59	Second CRTC Vertical Active Data Period	RW
3X5	5A	Second CRTC Vertical Blanking Start	RW
3X5	5B	Second CRTC Vertical Blanking End	RW
3X5	5C	Second CRTC Vertical Blanking Overflow	RW
3X5	5D	Second CRTC Vertical Period Overflow	RW
3X5	5E	Second CRTC Vertical Retrace Start	RW
3X5	5F	Second CRTC Vertical Retrace End	RW
3X5	60	Second CRTC Vertical Status 1	RO
3X5	61	Second CRTC Vertical Status 2	RO
3X5	62	Second Display Starting Address Low	RW
3X5	63	Second Display Starting Address Middle	RW
3X5	64	Second Display Starting Address High	RW
3X5	65	Second Display Horizontal Quadword Count Data	RW
3X5	66	Second Display Horizontal Offset	RW
3X5	67	Second Display Color Depth and Horizontal Overflow	RW
3X5	68	Second Display Queue Depth and Read Threshold	RW
3X5	69	Second Display Interrupt Enable and Status	RW
3X5	6A	Second Display Channel and LCD Enable	RW
3X5	6B	Channel 1 and 2 Clock Mode Selection	RW
3X5	6C	TV Clock Control	RW
3X5	6D	Horizontal Total Shadow	RW
3X5	6E	End Horizontal Blanking Shadow	RW
3X5	6F	Vertical Total Shadow	RW
3X5	70	Vertical Display Enable End Shadow	RW
3X5	71	Vertical Display Overflow Shadow	RW
3X5	72	Start Vertical Blank Shadow	RW
3X5	73	End Vertical Blank Shadow	RW
3X5	74	Vertical Blank Overflow Shadow	RW
3X5	75	Vertical Retrace Start Shadow	RW
3X5	76	Vertical Retrace End Shadow	RW
3X5	77	LCD Horizontal Scaling Factor	RW
3X5	78	LCD Vertical Scaling Factor	RW
3X5	79	LCD Scaling Control	RW
3X5	7A	LCD Scaling Parameter 1	RW
3X5	7B	LCD Scaling Parameter 2	RW
3X5	7C	LCD Scaling Parameter 3	RW
3X5	7D	LCD Scaling Parameter 4	RW
3X5	7E	LCD Scaling Parameter 5	RW
3X5	7F	LCD Scaling Parameter 6	RW
3X5	80	LCD Scaling Parameter 7	RW
3X5	81	LCD Scaling Parameter 8	RW

I/O Port (Hex)	I/O Index (Hex)	Sequencer Extended Registers	Attribute
3X5	82	LCD Scaling Parameter 9	RW
3X5	83	LCD Scaling Parameter 10	RW
3X5	84	LCD Scaling Parameter 11	RW
3X5	85	LCD Scaling Parameter 12	RW
3X5	86	LCD Scaling Parameter 13	RW
3X5	87	LCD Scaling Parameter 14	RW
3X5	88	LCD Panel Type (See LVDS/DVI Chapter)	RW
3X5	89	Reserved	RO
3X5	8A	LCD Timing Control 1	RW
3X5	8B	LCD Power Sequence Control 0	RW
3X5	8C	LCD Power Sequence Control 1	RW
3X5	8D	LCD Power Sequence Control 2	RW
3X5	8E	LCD Power Sequence Control 3	RW
3X5	8F	LCD Power Sequence Control 4	RW
3X5	90	LCD Power Sequence Control 5	RW
3X5	91	Software Control Power Sequence	RW
3X5	92	Read Threshold 2	RW
3X5	93	Reserved	RO
3X5	94	Expire Number and Display Queue Extend Bit	RW
3X5	95	Extend Threshold Bit	RW
3X5	97	LVDS Channel 1 Function Select 0 (See LVDS/DVI Chapter)	RW
3X5	98	LVDS Channel 1 Function Select 1 (See LVDS/DVI Chapter)	RW
3X5	99	LVDS Channel 0 Function Select 0 (See LVDS/DVI Chapter)	RW
3X5	9A	Reserved	RO
3X5	9B	Digital Video Port 1 Function Select 0	RW
3X5	9C	Reserved	RO
3X5	9D	Power Now Control 2	RW
3X5	9E	Power Now Control 3	RW
3X5	9F	Power Now Control 4	RW
3X5	A0	Horizontal Scaling Initial Value	RW
3X5	A1	Vertical Scaling Initial Value	RW
3X5	A2	Horizontal and Vertical Scaling Enable Bit	RW
3X5	A3	Second Display Starting Address Extended	RW
3X5	A4	Reserved	RO
3X5	A5	Second LCD Vertical Scaling Factor	RW
3X5	A6	Second LCD Vertical Scaling Factor	RW
3X5	A7	Expected IGA1 Vertical Display End	RW
3X5	A8	Expected IGA1 Vertical Display End	RW
3X5	A9	Hardware Gamma Control Register	RW
3X5	AA	FIFO Depth & Threshold Overflow bit	RW
3X5	AB	IGA2 Interlace Half Line Register	RW
3X5	AC	IGA2 Interlace Half Line Register	RW
3X5	AF	P-Arbiter Write Expired Number Register	RW
3X5	B0 ~ CF	Reserved	RO
3X5	D0	LVDS PLL Control Register (See LVDS/DVI Chapter)	RW
3X5	D1	DVI PLL Control Register (See LVDS/DVI Chapter)	RW
3X5	D2	LVDS / DVI Control Register (See LVDS/DVI Chapter)	RW

I/O Port (Hex)	I/O Index (Hex)	Sequencer Extended Registers	Attribute
3X5	D3	Second Power sequence Control Register 0 (See LVDS/DVI Chapter)	RW
3X5	D4	Second Power sequence Control Register 1 (See LVDS/DVI Chapter)	RW
3X5	D5	LVDS Settting Mode Control Register (See LVDS/DVI Chapter)	RW
3X5	D6	DCVI Control Register 0	RW
3X5	D7	DCVI Control Register 1	RW
3X5	D8	PLL control register	RW
3X5	D9	Scaling Down Source Data Offset Control	RW
3X5	DA	Scaling Down Source Data Offset Control	RW
3X5	DB	Scaling Down Source Data Offset Control	RW
3X5	DC	Scaling Down Horizontal Scale Control	RW
3X5	DD	Scaling Down Horizontal Scale Control	RW
3X5	DE	Scaling Down Vertical Scale Control	RW
3X5	DF	Scaling Down Vertical Scale Control	RW
3X5	E0	Scaling Down Destination Frame Buffer Starting Address 0	RW
3X5	E1	Scaling Down Destination Frame Buffer Starting Address 0	RW
3X5	E2	Scaling Down Destination Frame Buffer Starting Address 0	RW
3X5	E3	Scaling Down Destination Frame Buffer Starting Address 0	RW
3X5	E4	Scaling Down SW Source Frame Buffer Stride	RW
3X5	E5	Scaling Down Destination Frame Buffer Starting Address 1	RW
3X5	E6	Scaling Down Destination Frame Buffer Starting Address 1	RW
3X5	E7	Scaling Down Destination Frame Buffer Starting Address 1	RW
3X5	E8	Scaling Down Destination Frame Buffer Starting Address 1	RW
3X5	E9	Scaling Down Destination Frame Buffer Starting Address 2	RW
3X5	EA	Scaling Down Destination Frame Buffer Starting Address 2	RW
3X5	EB	Scaling Down Destination Frame Buffer Starting Address 2	RW
3X5	EC	IGA1 Down Scaling Destination Control Register	RW
3X5	F0	SNAPSHOP Mode – Starting Address of Display Data	RW
3X5	F1	SNAPSHOP Mode – Starting Address of Display Data	RW
3X5	F2	SNAPSHOP Mode – Starting Address of Display Data	RW
3X5	F3	SNAPSHOP Mode Control	RW
3X5	F4	SNAPSHOP Mode Control	RW
3X5	F5	SNAPSHOP Mode Control	RW
3X5	F6	SNAPSHOP Mode Control	RW
3X5	F7	Internal Spread Spectrum Control CH0	RW
3X5	F8	Reserved (Internal SSCG CH1 for dual channel)	RW
3X5	F9	V1 Power Control 0	RW
3X5	FA	V1 Power Control 1	RW
3X5	FB	IGA2 Interlace Vsync Timing register	RW
3X5	FC	IGA2 Interlace Vsync Timing register	RW
3X5	FD	IGA1 Scaling Up Control	RW

Table 8. IGA1 Display Engine MMIO Registers

Offset	Register Name	Attribute
IGA1 Display Engine MMIO Engines Register Space 1 (0x00008400 ~ 0x0000843F)		
840F-840C	IGA1 Scaling Function Control	RW
8413-8410	Scaling Parameter Setting 1-4	RW
8417-8414	Scaling Parameter Setting 8-5	RW
841B-8418	Scaling Parameter Setting C-9	RW
841F-841C	Scaling Parameter Setting D/E	RW
8433-8430	Power Management IDEL Control	RW

Extended I/O Space Register Descriptions

Sequencer Extended Registers

IO Port / Index: 3C5.10
Extended Register Unlock **Default Value: 01h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	1b	**Unlock Accessing of I/O Space** 0: Disable 1: Enable

IO Port / Index: 3C5.11
Configuration Register 0 **Default Value: 58h**

Bit	Attribute	Default	Description
7	RO	0	**VGA Port Select** 0: 3C3 1: 46E8
6	RO	1b	**PC AT Space Disable** 0: Disable VGA & memory space: A0000h-BFFFFh 1: IBM VGA standard space
5	RO	0	**Reserved** Always reads 0.
4:3	RO	11b	**Bus Type** 00: Reserved 01: Reserved 10: Reserved 11: 1x, 2x, 4x (8x) side band AGP bus
2:0	RO	0	**Reserved**

IO Port / Index: 3C5.12
Configuration Register 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RO	0	**Reerved**
5:4	RO	0	**Reserved**
3:0	RO	0	**Panel Type ID (H/W Strapping)** 0h~8h: VIA generic type 9h~Fh: Customers' request

IO Port / Index: 3C5.13
Configuration Register 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RO	0	**DVP1 Output Select (Reflects strapping from signal VCPD13)** See bits [2:1] for bit value description detail.
5	RO	0	**Reserved**
4	RO	0	**Reserved**
3	RO	0	**Reserved**
2:1	RO	0	**DVP1 Output Select (Reflects strapping from signal VCPD12 / VCPD11)** **Bit [6, 2, 1]** / **Description** 00x: DVP-TV output 01x: DVP with alpha output 100: DCVI 10-bit data output 101: DCVI 8-bit data output 110: DCVI 20-bit data output 111: DCVI 16-bit data output
0	RO	0	**Reserved**

IO Port / Index: 3C5.12
Shadow Configuration Register 1 (3C5.5A[0]=1) **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0000b	**Video Capture Port 1 Type Select (Reflects strapping from signals DVP1D7/6/5/4)** 0000: CAP 8 bit CCIR656 0001: CAP 8 bit CCIR601 0010: CAP 8 bit VIP 1.1 0011: CAP 8 bit VIP 2.0 0100: CAP 16 bit CCIR656 0101: CAP 16 bit CCIR601 0110: CAP 16 bit VIP 1.1 0111: CAP 16 bit VIP 2.0 1xxx: TS 8 bit
3:0	RO	0000b	**Video Capture Port 0 Type Select (Reflects strapping from singals DVP1D3/2/1/0)** 0000: CAP 8 bit CCIR656 0001: CAP 8 bit CCIR601 0010: CAP 8 bit VIP 1.1 0011: CAP 8 bit VIP 2.0 0100: CAP 16 bit CCIR656 0101: CAP 16 bit CCIR601 0110: CAP 16 bit VIP 1.1 0111: CAP 16 bit VIP 2.0 1xxx: TS 8 bit

IO Port / Index: 3C5.13
Configuration Register 2 (3C5.5A[0]=1) **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	00b	**Integrated LVDS / DVI Mode Select (Reflects strapping from signal DVP1D15/14) - *Refer to LVDS / DVI chapter for details***
5:3	RO	000b	**Second DAC (TV/CRT) Output Mode Select (Reflects strapping from signal DVP1D13/12/11)** 1xx: DAC D/E/F = R/G/B for CRT 000: DAC D/E/F = C/Y/CVBS for TV 001: DAC D/E/F = C/Y/C for TV 010: DAC D/E/F = R/G/B for TV 011: DAC D/E/F = Pr/Y/Pb for TV
2:0	RO	000b	**First DAC (CRT/TV) Output Mode Select (Reflects strapping from signal DVP1D10/09/08)** 0xx: DAC A/B/C = R/G/B for CRT 100: DAC A/B/C = C/Y/CVBS for TV 101: DAC A/B/C = C/Y/Y for TV 110: DAC A/B/C = R/G/B for TV 111: DAC A/B/C = Pr/Y/Pb for TV

IO Port / Index: 3C5.14
Frame Buffer Size Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Frame Buffer Size Control** 00h: 512MB 80h: 256MB C0h: 128MB E0h: 64MB F0h: 32MB F8h: 16MB The minimum frame buffer size is 16MB.

IO Port / Index: 3C5.15
Display Mode Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**8/6 Bits LUT** 0: 6-bit 1: 8-bit
6	RW	0	**Text Column Control** 0: 80 column 1: 132 column
5	RW	0	**Wrap Around Disable** 0: Disable (For Mode 0-13) 1: Enable
4	RW	0	**Hi Color Mode Select** 0: 555 1: 565
3:2	RW	00b	**Display Color Depth Select** 00: 8bpp 01: 16bpp 10: 30bpp 11: 32bpp
1	RW	0	**Extended Display Mode Enable** 0: Disable 1: Enable
0	RW	0	**For Refresh Circuit**

IO Port / Index: 3C5.16
Display FIFO Threshold Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Display FIFO Normal Threshold[6]**
6	RW	0	**DAC Source Select** 0: IGA1 1: IGA2
5:0	RW	0	**Display FIFO Normal Threshold**

IO Port / Index: 3C5.17
Display FIFO Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Display FIFO Depth Select** See also Rx3C5.51[2].

IO Port / Index: 3C5.18
Display Arbiter Control 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Display FIFO Hight Regiseter Threshold [6]**
6	RW	0	**Force Preepmty Arbitor Request Always High Than Typical Request** 0: Disable 1: Enable
5:0	RW	0	**Display FIFO High Register Threshold [5:0]**

IO Port / Index: 3C5.19

Power Management **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**MIU/AGP Interface Clock Control** 0: Clocks always on 1: Enable clock gating
5	RW	0	**P-Arbiter Interface Clock Control** 0: Clocks always on 1: Enable clock gating
4	RW	0	**AGP Interface Clock Control** 0: Clocks always on 1: Enable clock gating
3	RW	0	**Typical Arbiter Interface Clock Control** 0: Clocks always on 1: Enable clock gating
2	RW	0	**MC Interface Clock Control** 0: Clocks always on 1: Enable clock gating
1	RW	0	**Display Interface Clock Control** 0: Clocks always on 1: Enable clock gating
0	RW	0	**CPU Interface Clock Control** 0: Clocks always on 1: Enable clock gating

IO Port / Index: 3C5.1A

PCI Bus Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Read Cache Enable** 0: Disable 1: Enable
6	RW	0	**Software Reset** 0: Default value 1: Reset
5	RW	0	**DVI Sense - *Refer to LVDS / DVI chapter for details***
4	RW	0	**Second DVI Sense - *Refer to LVDS / DVI chapter for details***
3	RW	0	**Extended Mode Memory Access Enable** 0: Disable 1: Enable
2	RW	0	**PCI Burst Write Wait State Select** 0: 0 Wait state 1: 1 Wait state
1	RO	0	**Reserved**
0	RW	0	**LUT Shadow Access** 0: 3C6/3C7/3C8/3C9 addresses map to Primary Display's LUT 1: 3C6/3C7/3C8/3C9 addresses map to Secondary Display's LUT

IO Port / Index: 3C5.1B

Power Management Control 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**Secondary Display Engine (Gated Clock <LCK>)** 0x: Clock always off 10: Clock always on 11: Clock on/off according to the Power Management Status (PMS)
5:4	RW	00b	**Primary Display Engine (Gated Clock <VCK>)** 0x: Clock always off 10: Clock always on 11: Clock on/off according to the PMS
3:2	RO	0	**Reserved**
1	RW	0	**Reserved**
0	RW	0	**Primary Display's LUT On/Off** 0: On 1: Off

IO Port / Index: 3C5.1C

Horizontal Display Fetch Count Data **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Horizontal Display Fetch Count Data [7:0]** Unit: 16 bytes

IO Port / Index: 3C5.1D
Horizontal Display Fetch Count Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**For REFRESH Circuit** 0: REFRESH off 1: REFRESH on
6:5	RO	0	**Reserved**
4:2	RW	0	**For REFRESH Circuit**
1:0	RW	0	**Horizontal Display Fetch Count Data Bit [9:8]** Used in conjunction with Rx3C5.1C register.

IO Port / Index: 3C5.1E
Power Management Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**Video Capture Port Power Control** 0x: Pad always off 10: Depend on the other control signal 11: Pad on/off according to the PMS
5:4	RW	00b	**Digital Video Port 1 Power Control** 0x: Pad always off 10: Depend on the other control signal 11: Pad on/off according to the PMS
3	RW	0	**Spread Spectrum On/Off** 0: Off 1: On
2	RW	0	**Reserved**
1	RW	0	**Replace ECK by MCK** For BIST purpose.
0	RW	0	**On/Off ROC ECK** 0: Off 1: On

IO Port / Index: 3C5.20
Typical Arbiter Control 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Typical Request Max. Queuing Number for Channel 0** Min: 0 Max: 62 (The recommended value is 4.)

IO Port / Index: 3C5.21
Typical Arbiter Control 1 **Default Value: 0Eh**

Bit	Attribute	Default	Description
7:0	RW	0	**Typical Request Track FIFO Number for Channel 0**

IO Port / Index: 3C5.22
Display Arbiter Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Display Queue Request Expire Number** Hardware multiples this register value by 4 to handle the FIFO control.

IO Port / Index: 3C5.26
IIC Serial Port Control 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	0	**CRTSPCLK Pin Control** 0: Driven low 1: Tri-Stated
4	RW	0	**CRTSPD Pin Control** 0: Driven low 1: Tri-Stated
3	RO	0	**CRTSPCLK Pin Status**
2	RO	0	**CRTSPD Pin Status**
1	RW	0	**CRTSPCLK Wait State Enable** 0: Disable 1: Enable (Drive DDCSCL low upon receipt of serial port start)
0	RW	0	**Serial Port Enable** 0: Disable 1: Enable

IO Port / Index: 3C5.2A
Power Management Control 5 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Spread Spectrum Type Control** 0: Original Type 1: FIFO Type
5	RW	0	**Reserved**
4	RW	0	**Reserved**
3:2	RW	00b	**LVDS Channel 1 I/O Pad Control** 0x: Pad always off 10: Depend on the other control signal 11: Pad on/off according to the PMS
1:0	RW	00b	**LVDS Channel 0 and DVI I/O Pad Control** 0x: Pad always off 10: Depend on the other control signal 11: Pad on/off according to the PMS

IO Port / Index: 3C5.2B

DVI and LVDS Interrupt Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DVI Sense Interrupt Enable** - ***Refer to LVDS / DVI chapter for details***
6	RW1C	0	**DVI Sense Interrupt Status** - ***Refer to LVDS / DVI chapter for details***
5	RW	0	**LVDS Sense Interrupt Enable** - ***Refer to LVDS / DVI chapter for details***
4	RW1C	0	**LVDS Sense Interrupt Status** - ***Refer to LVDS / DVI chapter for details***
3	RW	0	**CRT Sense Interrupt Enable** 0: Disable 1: Enable
2	RW1C	0	**CRT Sense Interrupt Status**
1	RW	0	**CRT Hot Plug Detection Function Enable** 0: Disable 1: Enable Please wait at least 2 frames to enable interrupt, when this function is enabled.
0	RW1C	0	**MSI Pending Interrupt Re-trigger Bit** When SW wants to exit interrupt service, please clear the bit. HW may send out interrupt again if pending interrupt exists. The funciton is enabled when MSI Enable = 1'b1.

IO Port / Index: 3C5.2C

General Purpose I/O Port **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**GPIO_2 Output Enable** 0: Disable 1: Enable
6	RW	0	**GPIO_3 Output Enable** 0: Disable 1: Enable
5	RW	0	**GPIO_2 Output Data**
4	RW	0	**GPIO_3 Output Data**
3	RO	0	**GPIO_2 Pin Status**
2	RO	0	**GPIO_3 Pin Status**
1	RW	0	**GPIO Port Enable** 0: HW controlled 1: SW controlled
0	RW	0	**Spectrum IO Selected** 0: GPIO port 1: GPIO_2 as DISPCLKI0 and GPIO_3 as DISPCLKO0

IO Port / Index: 3C5.2D

Power Management Control 1 **Default Value: 2Ah**

Bit	Attribute	Default	Description
7:6	RW	00b	**E3_ECK_N Selection** 00: E3_ECK_N 01: E3_ECK 10: Delayed E3_ECK_N 11: Delayed E3_ECK
5:4	RW	10b	**VCK (Primary Display Clock) PLL Power Control** 0x: PLL power-off 10: PLL always on 11: PLL on/off according to the PMS
3:2	RW	10b	**LCK (Secondary Display Clock) PLL Power Control** 0x: PLL power-off 10: PLL always on 11: PLL on/off according to the PMS
1:0	RW	10b	**ECK (Engine Clock) PLL Power Control** 0x: PLL power-off 10: PLL always on 11: PLL on/off according to the PMS

IO Port / Index: 3C5.2E

Power Management Control 2 **Default Value: AAh**

Bit	Attribute	Default	Description
7:6	RO	10b	**Capturer (Gated Clock <ECK>)** 0x: Clock off 10: Clock always on 11: Clock on/off according to the engine IDLE status
5:4	RW	10b	**Video Processor (Gated Clock <ECK>)** 0x: Clock off 10: Clock always on 11: Clock on/off according to the engine IDLE status
3:2	RW	10b	**PCI Master/DMA (Gated Clock <ECK/CPUCK>)** 0x: Clock off 10: Clock always on 11: Clock on/off according to the engine IDLE status
1:0	RW	10b	**Video Playback Engine (V3/V4 Gated Clock <VCK>)** 0x: Clock off 10: Clock always on 11: Clock on/off according to the engine IDLE status

IO Port / Index: 3C5.31

IIC Serial Port Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	0	**DVP1SPCLK Pin Control** 0: DVP1SPLCK driven low 1: DVP1SPLCK tri-stated
4	RW	0	**DVP1SPD Pin Control** 0: DVP1SPD driven low 1: DVP1SPD tri-stated
3	RO	0	**DVP1SPCLK Pin Status** 0: DVP1SPCLK driven low 1: DVP1SPCLK tri-stated
2	RO	0	**DVP1SPD Pin Status** 0: DVP1SPD driven low 1: SDATA tri-stated
1	RW	0	**DVP1SPCLK Wait State Enable** 0: Disable 1: Enable (Drive DVP1SPCLK low upon receipt of serial port start)
0	RW	0	**Serial Port Enable** 0: Disable 1: Enable

IO Port / Index: 3C5.35

Subsystem Vendor ID 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Subsystem Vendor ID [7:0]**

IO Port / Index: 3C5.36

Subsystem Vendor ID 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Subsystem Vendor ID [15:8]**

IO Port / Index: 3C5.37
Subsystem ID 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Subsystem ID [7:0]**

IO Port / Index: 3C5.38
Subsystem ID 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Subsystem ID [15:8]**

IO Port / Index: 3C5.39
BIOS Reserved Register 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**BIOS Reserved Register 0**

IO Port / Index: 3C5.3A
BIOS Reserved Register 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**BIOS Reserved Register 1**

IO Port / Index: 3C5.3B
PCI Revision ID Back Door **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**PCI Revision ID Back Door**

IO Port / Index: 3C5.3C
Miscellaneous **Default Value: 01h**

Bit	Attribute	Default	Description
7	RW	0	**IGA1 HCNT Control** 0: IGA2 HSYNC will not affect 1: IGA2 HSYNC will affect
6:5	RW	00b	**PLL Frequency Division Select for Testing** 00: Original 01: 1/2 10: 1/4 11: 1/8
4	RO	0	**ECK PLL Locked Detect** 0: Unlocked 1: Locked
3	RO	0	**VCK PLL Locked Detect** 0: Unlocked 1: Locked
2	RO	0	**LCDCK PLL Locked Detect** 0: Unlocked 1: Locked
1	RW	0	**Switch 3 PLLs to Prime Output** 0: Disable 1: Enable
0	RW	1b	**AGP Bus Back Door** 0: ACP2.0 Spec 1: ACP3.0 Spec

IO Port / Index: 3C5.3D

General Purpose I/O Port **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**GPIO_4 Output Enable** 0: Disable 1: Enable
6	RW	0	**GPIO_5 Output Enable** 0: Disable 1: Enable
5	RW	0	**GPIO_4 Output Data**
4	RW	0	**GPIO_5 Output Data**
3	RO	0	**GPIO_4 Pin Status**
2	RO	0	**GPIO_5 Pin Status**
1	RO	0	**Reserved**
0	RW	0	**Spectrum IO Selected** 0: GPIO Port 1: GPIO_4 as DISPCLKI1 and GPIO_5 as DISPCLKO1

IO Port / Index: 3C5.3E

Miscellaneous Register for AGP Mux **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DVI Sense Interrupt Enable** - ***Refer to LVDS / DVI chapter for details***
6	RW1C	0	**DVI Sense Interrupt Status** - ***Refer to LVDS / DVI chapter for details***
5	RW	0	**Inside DVI Sense** - ***Refer to LVDS / DVI chapter for details***
4	RO	0	**Reserved**
3	RW	0	**PCIe Capability Control Back Door** - ***Refer to LVDS / DVI chapter for details***
2	RO	0	**Reserved**
1	RW	0	**Multi-function Selection** - ***Refer to LVDS / DVI chapter for detail***
0	RW	0	**Second DVIDET Sense Signal Source** - ***Refer to LVDS / DVI chapter for details***

IO Port / Index: 3C5.3F

Power Management Control 2 **Default Value: AAh**

Bit	Attribute	Default	Description
7:6	RW	10b	**CR Clock Control (Gated Clock <ECK>)** 0x: Clock off 10: Clock always on 11: Clock on/off according to the engine IDLE status
5:4	RW	10b	**3D Clock Control (Gated Clock <ECK>)** 0x: Clock off 10: Clock always on 11: Clock on/off according to the engine IDLE status
3:2	RW	10b	**2D Clock Control (Gated Clock <ECK/CPUCK>)** 0x: Clock off 10: Clock always on 11: Clock on/off according to the engine IDLE status
1:0	RW	10b	**DVD Clock Control (Gated Clock <ECK>)** 0x: Clock off 10: Clock always on 11: Clock on/off according to each engine IDLE status

IO Port / Index: 3C5.40
PLL Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**CRT Sense Enable** Hardware sends constant value to DAC for sense. 0: Disable 1: Enable. When enabled, send pattern 24'h555555 to DAC.
6	RW	0	**Reserved**
5:4	RW	00b	**Free Run ECK Frequency Within the Idle Mode** 00: No change 01: 1/2 ECK 10: 1/4 ECK 11: 1/8 ECK
3	RW	0	**LVDS and DVI Interrupt Method** - ***Refer to LVDS / DVI chapter for details***
2	RW	0	**Reset LCDCK PLL**
1	RW	0	**Reset VCK PLL**
0	RW	0	**Reset ECK PLL**

IO Port / Index: 3C5.41
Typical Arbiter Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Typical Request T-Hold**
3:0	RO	0	**Typical Request Pre-T-Hold**

IO Port / Index: 3C5.42
Typical Arbiter Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Linear Addressing Mode Enable** 0: Force all engine use linear addressing mode 1: The addressing mode is decided by engine itself
6	RO	0	**Pre-empty Arbitor Request Attribute** 1: Supports Fetch Cycle With Length (2) Capability
5	RO	0	**Pre-empyt Arbitor Arbitration Type** 0: Run-robin Like 1: Fix
4:0	RO	0	**Typical Request Maximum Queuing Number**

IO Port / Index: 3C5.43
Graphics Bonding Option **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Advance Video Enable Flag** 0: Disable 1: Enable
6	RO	0	**Windows Media Video Enable Flag** 0: Disable 1: Enable
5	RW1C	0	**IGA2 Display FIFO Underflow Flag**
4	RW1C	0	**IGA1 Display FIFO Underflow Flag**
3	RW1C	0	**Typical Channel 0 Arbiter Read Back Data Overwrite Flag**
2	RW1C	0	**Typical Channel 1 Arbiter Read Back Data Overwrite Flag**
1	RO	0	**Reserved**
0	RO	0	**Notebook Used Flag** 0: Desktop 1: Notebook

Clock Synthesizer Registers

IO Port / Index: 3C5.44
Primary Display (VCK) Clock Synthesizer Value 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**DM[7:0]**

IO Port / Index: 3C5.45
Primary Display (VCK) Clock Synthesizer Value 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**{DTZ[0], 2'b00, DR[2:0], DM[9:8]}**

IO Port / Index: 3C5.46
Primary Display (VCK) Clock Synthesizer Value 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**{DTZ[1], DN[6:0]}**

IO Port / Index: 3C5.47
ECK Clock Synthesizer Value 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**DM[7:0]**

IO Port / Index: 3C5.48
ECK Clock Synthesizer Value 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**{DTZ[0], 2'b00, DR[2:0], DM[9:8]}**

IO Port / Index: 3C5.49
ECK Clock Synthesizer Value 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**{DTZ[1], DN[6:0]}**

IO Port / Index: 3C5.4A
Secondary Display (LCDCK) Clock Synthesizer Value 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**DM[7:0]**

IO Port / Index: 3C5.4B
Secondary Display (LCDCK) Clock Synthesizer Value 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**{DTZ[0], 2'b00, DR[2:0], DM[9:8]}**

IO Port / Index: 3C5.4C
Secondary Display (LCDCK) Clock Synthesizer Value 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**{DTZ[1], DN[6:0]}**

Note:
1. DTZ[1:0]: Select charge-pump current. Default value = 00b.
2. DGAIN[1:0] is for testing purpose and must be 00b in normal mode.
3. Frequency equations: the following two equations must be asserted

Internal Working Frequency

Fvco = Fref * (DM) / (DN) and 300MHz <= Fvco <= 600MHz

True Output Frequency

Fout = Fref * (DM) / [(DN) (2^{DR})]

IO Port / Index: 3C5.4D
Preemptive Arbiter Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Ypical Arbiter Tracking FIFO Type** 0: 64 level 1: 128 level (only single channel can use)
6	RO	0	**Reserved**
5:4	RW	00b	**P Arbiter Length Control** 0x: 2 quad words 10: 4 quad words 11: 8 quad words
3:0	RO	0	**Reserved**

IO Port / Index: 3C5.4E
Software Reset Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	00b	**CR Reset Control** 01: Engine reset (high active) 10: Register reset (high active)
5:4	RW	00b	**3D Reset Control** 01: Engine reset (high active) 10: Register reset (high active)
3:2	RW	00b	**2D Reset Control** 01: Engine reset (high active) 10: Register reset (high active)
1:0	RW	00b	**HQV/DVD/Capture Reset Control** 01: Engine reset (high active) 10: Register reset (high active)

IO Port / Index: 3C5.4F
CR Gating Clock Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	0	**DMA Write Cycle with Length Control** 0: Enable length (2/4/8QW alignment with address) 1: Disable length (always 2QW cycle)
4:0	RW	0	**Threshold Value of Engine Idle for Gating Engine Clock**

IO Port / Index: 3C5.50

AGP Control Register **Default Value: 1Bh**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**AGP Request Attribute** 0: Only support length 1 1: Support length 2
5:0	RW	63h	**AGP Track FIFO Number** The default value is 63h.

IO Port / Index: 3C5.51

Display FIFO Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**NB FIFO Clock Control** 0: Disable 1: Enable
6:5	RW	0	**Reserved**
4	RO	0	**Reserved**
3	RW	0	**Typical Arbiter Software Reset** 1: Reset (high active)
2	RW	0	**Reserved**
1	RW	0	**Pre-empty Arbiter and NB FIFO Software Reset** 1: Reset (high active)
0	RW	0	**Reserved**

IO Port / Index: 3C5.52

Integrated MMIO Shadow Register Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RW	0b	**Integrated MMIO Shadow Register Enable to B000** 0: Disable 1: Enable
0	RW	0	**Integrated MMIO Shadow Register Enable to A000** 0: Disable 1: Enable

IO Port / Index: 3C5.53

DAC Sense Control Register 1 **Default Value: 00h**

Bit	Attribut	Default	Description
7:0	RW	0	**Vertical Line Count for Sense Bits [7:0]** Programming which line that HW can assert HW_SENSE

IO Port / Index: 3C5.54

DAC Sense Control Register 2 **Default Value: 00h**

Bit	Attribut	Default	Description
7:0	RW	0	**Horizontal Pixel Count for Sense Start Bits [7:0]** Programming which pixel that HW asserts HW_SENSE

IO Port / Index: 3C5.55

DAC Sense Control Register 3 **Default Value: 00h**

Bit	Attribut	Default	Description
7:0	RW	0	**Horizontal Pixel Count for Sense End Bits [7:0]** Programming which pixel that HW asserts HW_SENSE

IO Port / Index: 3C5.56

DAC Sense Control Register 4 **Default Value: 00h**

Bit	Attribut	Default	Description
7:5	RO	0	**Reserved**
4	RW	0	**Horizontal Pixel Count for Sense End Bit [8]** Programming which pixel that HW asserts HW_SENSE
3	RW	0	**Horizontal Pixel Count for Sense Start Bit [8]** Programming which pixel that HW asserts HW_SENSE
2:0	RW	0	**Vertical Line Count for Sense Bits [10:8]** Programming which line that HW can assert HW_SENSE

IO Port / Index: 3C5.57
Display FIFO Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Display Queue Request Expire Number Bit [5]**
5	RW	0	**NB FIFO Delay Mode** 0: Original 1: Delay 1 cycle
4	RW	0	**Display FIFO Threshold Select Bit [7]**
3	RW	0	**Display FIFO Depth Select Bit [8]**
2	RW	0	**Display FIFO Threshold High Select Bit [7]**
1	RW	0	**NB FIFO Extended Source Select** 0: IGA1 1: IGA2
0	RW	0	**NB FIFO Length Extended Control** 0: Disable 1: Enable

IO Port / Index: 3C5.58
GFX Power Control Register 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Display FIFO Low Threshold Select** HW will multiples the value by 4 to handle.

IO Port / Index: 3C5.59
GFX Power Control Register 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**IGA1 Enable** When IGA1 engine is active, this bit needs to be set to 1.
6	RO	0	**Reserved**
5	RW	0	**IGA Low Threshold Enable** 0: Disable 1: Enable
4	RW	0	**GFX-NM IGA Vertical Blanking Enable** 0: Disable 1: Enable
3	RW	0	**GFX-NM PCIC Dynamic Clock Enable** 0: Disable 1: Enable
2	RW	0	**GFX-NM GMINT Channel 1 Dynamic Clock Enable** 0: Disable 1: Enable
1	RW	0	**GFX-NM GMINT Channel 0 Dynamic Clock Enable** 0: Disable 1: Enable
0	RW	0	**GFX-NM AGP Dynamic Clock Enable** 0: Disable 1: Enable

IO Port / Index: 3C5.5A

PCI Bus Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**Scratch Pad Register Shadow Access** 0: This bit controls Rx3X5.49-4F, Rx3C5.39/3A and Rx3X5.3B-3F (total 14) addresses map to original registers. 1: This bit controls Rx3X5.49-4F, Rx3C5.39/3A and Rx3X5.3B-3F (total 14) addresses map to secondary registers.

IO Port / Index: 3C5.5B

Device Used Status 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**DCVI Source Selection Flag** 0:Graphic 1:TV
6	RO	0	**DAC0 User Flag** 0: Graphic 1: TV
5	RO	0	**DAC0 Used IGA1 Source Flag** 0: No use 1: Use
4	RO	0	**DAC0 Used IGA2 Source Flag** 0: No use 1: Use
3	RO	0	**LVDS0 Used IGA1 Source Flag** - ***Refer to LVDS / DVI chapter for details***
2	RO	0	**LVDS0 Used IGA2 Source Flag** - ***Refer to LVDS / DVI chapter for detail***
1	RO	0	**LVDS1 Used IGA1 Source Flag** - ***Refer to LVDS / DVI chapter for details***
0	RO	0	**LVDS1 Used IGA2 Source Flag**- ***Refer to LVDS / DVI chapter for details***

IO Port / Index: 3C5.5C

Device Used Status 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RO	0	**DAC1 User Flag** 0: Graphic 1: TV
5	RO	0	**DAC1 Used IGA1 Source Flag** 0: No use 1: Use
4	RO	0	**DAC1 Used IGA2 Source Flag** 0: No use 1: Use
3	RO	0	**Reserved**
2	RO	0	**Reserved**
1	RO	0	**DVP1 Used IGA1 Source Flag** 0: No use 1: Use
0	RO	0	**DVP1 Used IGA2 Source Flag** 0: No use 1: Use

IO Port / Index: 3C5.5D

Timer Control Register **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Timer Status** When the bit is asserted, it means the timer is reached.
6:0	RW	0	**Timer Step Setting** Countdown step value for timer. (one step is about 10us (8.9us))

IO Port / Index: 3C5.5E

DAC Control Register 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**CRT DACOFF Setting** When this bit is 1, CRT DACOFF signal will be controlled by screen off register (Rx3C5.01[5]).

IO Port / Index: 3C5.60

I2C Mode Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**I2C Byte Count** This field is programmed with the data transfer count (a value between 0 and 15).
3	RW	0	**Internal Timer Count Using Clock Divided By 2** 0: Counter using original clock 1: Counter using clock divided by 2
2	RW	0	**NO STOP Command Generation** When this bit is enabled, master controller finishes the transaction without STOP.
1	RW	0	**I2C Mode** 0: Standard mode 1: Fast mode
0	RW	0	**I2C Master Interrupt Enable** 0: Disable interrupt generation 1: Enable generation of interrupts on completion of the current transaction

IO Port / Index: 3C5.61

I2C Host Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RW	0	**I2C Host Address** This field contains the 7 bit address of the targeted slave device.
0	RW	0	**I2C Write or Read** 0: Write 1: Read

IO Port / Index: 3C5.62

I2C Host Data **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**I2C Host Data** Hardware supports the queue of 2-byte data. Reads and writes to this register are used to access the 2-byte data queue. An internal index pointer is used to address the queue. It is reset to 0 by reads of the I2C Host Control register and incremented automatically by each access to this register.

IO Port / Index: 3C5.63

I2C Host Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Software Reset** 0: Normal function 1: Reset I2C master controller
6	RW	0	**No Active Driving to High before Release the Bus** 0: Driving to high 1: No driving to high
5	RO	0	**Reserved**
4	RW	0	**I2C Master Clock Control** 0: Disable 1: Enable
3:2	RW	00b	**Which Port I2C Master Process** 00: 31h 01: 2Ch 10: 26h 11: 25h
1	RW	0	**Kill Transaction in Progress** 0: Normal master controller operation 1: Stop transaction currently in progress
0	RW	0	**Fire** 0: No effect 1: Writing one to this bit causes master controller to start transaction

IO Port / Index: 3C5.64

I2C Status **Default Value: 40h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	1b	**Queue Empty Status** When this bit is one, it means hardware queue is empty.
4	RW1C	0	**I2C Data Transferred Status**
3	RW1C	0	**I2C Transaction Done Status**
2	RW1C	0	**I2C Abnormal Status**
1	RW	0	**Queue Full Status** When this bit is one, it means hardware queue is full.
0	RW	0	**Master Busy Status** When this bit is one, it means master controller is busy processing a command.

IO Port / Index: 3C5.65

Power Management Control 6 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:2	RW	00b	**DVP1 Clock Pads Driving Select** 00 (Low) ←→ 11 (High)
1:0	RW	00b	**DVP1 Data Pads Driving Select** 00 (Low) ←→ 11 (High)

IO Port / Index: 3C5.66

GTI Control 0 **Default Value: C8h**

Bit	Attribute	Default	Description
7:0	RW	C8h	**Typical Request Kill Number for Channel 0**

IO Port / Index: 3C5.67

GTI Control 1 **Default Value: C8h**

Bit	Attribute	Default	Description
7:0	RW	C8h	**3D Request Kill Number for Channel 0**

IO Port / Index: 3C5.68

GTI Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**SLSZ** 00h: 512MB 80h: 256MB C0h: 128MB E0h: 64MB F0h: 32MB F8h: 16MB FCh: 8MB FEh: 4MB FFh: 2MB

IO Port / Index: 3C5.69

GTI Control 3 **Default Value: C8h**

Bit	Attribute	Default	Description
7:0	RW	C8h	**GTI Request Kill Number for Channel 0**

IO Port / Index: 3C5.6A
GTI Control 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Base Address [19:12] of RTSF in SL**

IO Port / Index: 3C5.6B
GTI Control 5 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Base Address [27:20] of RTSF in SL**

IO Port / Index: 3C5.6C
GTI Control 6 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**GART Table Write Protect Enable** Enable to avoid hardware write. 0: Disable 1: Enable
6	RW	0	**GARB SAMPLE_GFX1DATA**
5	RW	0	**GTI SAMPLE_GFX0DATA**
4:2	RO	0	**Reserved**
1	RO	0	**Reserved**
0	RW	0	**Base Address [28] of RTSF in SL**

IO Port / Index: 3C5.6D
GTI Control 7 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Base Address [28:21] of SL in System Memory**

IO Port / Index: 3C5.6E
GTI Control 8 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Base Address [36:29] of SL in System Memory**

IO Port / Index: 3C5.6F
GTI Control 9 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**GTI Cache Flush** Set by SW and reset by GTI.
6:0	RW	0	**Base Address [43:37] of SL in System Memory**

IO Port / Index: 3C5.6F - Reserved

IO Port / Index: 3C5.71
Typical Arbiter Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Typical Request Max. Queuing Number for Channel 1** Min: 0 Max: 62 (The recommended value is 4.)

IO Port / Index: 3C5.72
Typical Arbiter Control 3 **Default Value: 1Dh**

Bit	Attribute	Default	Description
7:0	RW	0	**Typical Request Track FIFO Number for Channel 1**

IO Port / Index: 3C5.73
Typical Arbiter Control 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5:4	RW	00b	**Typical Request Max. Burst Length to GTI for Channel 1** 00: 1 01: 2 11: 4
3:2	RO	0	**Reserved**
1:0	RW	00b	**Typical Request Max. Burst Length to GTI for Channel 0** 00: 1 01: 2 11: 4

IO Port / Index: 3C5.74
Typical Arbiter Control 5 **Default Value: 1Fh**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5:0	RW	1Fh	**Typical Request Maximum ACK Number Minus One for Channel 1** 00h: Disable the function

IO Port / Index: 3C5.75
Typical Arbiter Control 6 **Default Value: 1Fh**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5:0	RW	1Fh	**Typical Request Maximum ACK Number Minus One for Channel 0** 00h: Disable the function

IO Port / Index: 3C5.76
Backlight Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Debug Port Group Selection**
3	RW	0	**Debug Port Group0/Group1 Selection**
2:1	RW	0	**Reserved**
0	RW	0	**Backlight Control Enable** 0: Disable 1: Enable

IO Port / Index: 3C5.77
Backlight Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**PWM Level Indicator** Total 256 level from 0% ~ 100%.

IO Port / Index: 3C5.78
Backlight Control 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**South Module Pad Share Enable** 0: Disable 1: Enable
6	RW	0	**Inverse IGA2 HSYNC to LVDS** - ***Refer to LVDS / DVI chapter for details***
5	RW	0	**Inverse IGA2 VSYNC to LVDS** - ***Refer to LVDS / DVI chapter for details***
4	RW	0	**Inverse IGA1 HSYNC to LVDS** - ***Refer to LVDS / DVI chapter for details***
3	RW	0	**Inverse IGA1 VSYNC to LVDS** - ***Refer to LVDS / DVI chapter for details***
2:1	RW	00b	**Clock Source Selection** 00: 14.318 MHz / 2 01: 14.318 MHz / 4 10: 14.318 MHz /128 11: 14.318 MHz / 16384
0	RW	0	**Backlight Control Fire** 1: Fire (3C5.76[0] must be 1

IO Port / Index: 3C5.79
GTI Control 10 SL/SF Request Kill Number 0 **Default Value: C8h**

Bit	Attribute	Default	Description
7:0	RW	C8h	**SL/SF Request Kill Number 0** Kill number setting by SW. Used if there is high P-ARB request.

IO Port / Index: 3C5.7A
GTI Control 11 SL/SF Request Kill Number 1 **Default Value: C8h**

Bit	Attribute	Default	Description
7:0	RW	C8h	**SL/SF Request Kill Number 1** Kill number setting by SW. Used if there is not high P-ARB request.

Note: the kill number0 can be set small value for servicing display ASAP, and kill number1 can be set larger value to service SL/SF request much time.

IO Port / Index: 3C5.7B
SNAPSHOT Mode Control & GTI Control 12 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0	**Reserved**

IO Port / Index: 3C5.7C
GTI Control 13 CBU Request Kill Number **Default Value: C8h**

Bit	Attribute	Default	Description
7:0	RW	C8h	**CBU Request Kill Number** Kill number setting by SW.

IO Port / Index: 3C5.7D
Transmitter Power Control 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**SSCG Selection of FIFO Type** 0: External SSCG 1: Internal SSCG
6	RW	0	**The Source Clock Selection of External SSCG (For Original Type)** 0: VCKSRC 1: LCDCK_SRC0
5	RW	0	**SSCG Selection of Original Type** 0: External SSCG 1: Internal SSCG
4	RW	0	**The Source Clock Selection of Internal SSCG** 0: FIFO type 1: Original type
3	RW	0	**Add a Protect Flag to Prevent All Snapshot State Failure**
2	RW	0	**Real PD3 Polatiry** - ***Refer to LVDS / DVI chapter for details***
1	RW	0	**Real PD2 Polatiry** - ***Refer to LVDS / DVI chapter for details***
0	RW	0	**Real PD1 Polatiry** - ***Refer to LVDS / DVI chapter for details***

IO Port / Index: 3C5.7E
GTI Control 14 CR Request Kill Number **Default Value: C8h**

Bit	Attribute	Default	Description
7:0	RW	C8h	**Command Regulao(CR) Request Kill Number for Channel 0**

IO Port / Index: 3C5.7F~A7 – Reserved

IO Port / Index: 3C5.A8
Number of Idle Cycles for Gating ECK **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Number[7:0] of Idle Cycles for Gating ECK** If the period of GFX idle equal this number gate off ECK. Unit: Engine clock cycle * 8.

IO Port / Index: 3C5.A9
Gating ECK Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Number[8] of Idle Cycles for Gating ECK** If the period of GFX idle equal this number gate off ECK. Unit: Engine clock cycle * 8.
6	RW	0	**Enable IGA2 Vertical Blank for C4P** 0: Disable, vertical Blank =0 1: Enable
5	RW	0	**Enable IGA1 Vertical Blank for C4P** 0: Disable, vertical Blank =0 1: Enable
4	RW	0	**Enable G2N_ENGIDLE.** 0: G2N_ENGIDLE = 0 1: Output G2N_ENGIDLE for C4P
3:2	RW	0	**ECK Gating Selection** 0x: Shut down the root ECK gating function 10: When engine all idle in C3/C4 state gate ECK 11: When engine all idle gate ECK regardless of power state of NB
1	RW	0	**Enable IGA2 Turning on ECK Function** 0: IGA2 can't turn on ECK 1: IGA2 turn on ECK at first and last line every frame
0	RW	0	**Enable IGA1 Turning on ECK Function.** 0: IGA1 can't turn on ECK 1: IGA1 turn on ECK at first and last line every frame

IO Port / Index: 3C5.AA
Number of Idle Cycles for Gating ECK **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable IGA2 Screen off for C4P** 0: Disable, screen off for C4P is 0 1: Enable
6:4	RW	0	**IGA1 Vertical Blank End Offset for C4P - Bits [10:8]**
3	RW	0	**Enable IGA1 Screen off for C4P** 0: Disable, screen off for C4P is 0 1: Enable
2:0	RW	0	**IGA1 Vertical Blank Start Offset for C4P - Bits [10:8]**

IO Port / Index: 3C5.AB
IGA1 Vertical Blank Start for C4P **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**IGA1 Vertical Blank Start Offset for C4P - Bits [7:0]**

IO Port / Index: 3C5.AC
IGA1 Vertical Blank End for C4P **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**IGA1 Vertical Blank End Offset for C4P - Bits [7:0]**

IO Port / Index: 3C5.AD
IGA1 Vertical Blank Start for C4P **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**IGA2 Vertical Blank Start Offset for C4P - Bits [7:0]**

IO Port / Index: 3C5.AE
IGA1 Vertical Blank End for C4P **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**IGA2 Vertical Blank End Offset for C4P - Bits [7:0]**

IO Port / Index: 3C5.AF
Number of Idle Cycles for Gating ECK **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable Turn Off LVDS when GFX Leaves D0** 0: Disable 1: Enable
6	RW	0	**Select GFX_VBLANK=G2N_VB_C4P for DRAM Self-refresh** 0: Normal 1: GFX_VBLANK = G2N_VB_C4P
5:4	RW	0	**IGA2 Vertical Blank End Offset for C4P - Bits [9:8] and Bit [10] = 0b**
3	RW	0	**IGA1 Vertical Blank Control** 0: Normal 1: IGA1 Vertical blank for C4P ==1
2	RW	0	**IGA2 Vertical Blank Control** 0: Normal 1: IGA2 Vertical blank for C4P ==1
1:0	RW	0	**IGA2 Vertical Blank Start Offset for C4P - Bits [9:8] and Bit [10] = 0b**

IO Port / Index: 3C5.B0
GTI Control 15 Enable GTI Mapping Address More Than 4GByte to MMIO Address Range **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**Enable GTI Mapping Address More Than 4GByte to MMIO Address Range** 0: Disable 1: Enable

IO Port / Index: 3C5.B1
GTI Control 16 Mapping Base Address[35:28] **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Mapping Base Address[35:28]** GTI will map address more than 4GByte to this base address.

IO Port / Index: 3C5.B2
GTI Control 17 Mapping Base Address[27:20] **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Mapping Base Address[27:20]** GTI will map address more than 4GByte to this base address.

IO Port / Index: 3C5.B3

GTI Control 18 Mapping Base Address[19:12] **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Mapping Base Address[19:12]** GTI will map address more than 4GByte to this base address.

IO Port / Index: 3C5.B4

GTI Control 19 Mapping Base Address[11:4] **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Mapping Base Address[11:4]** GTI will map address more than 4GByte to this base address.

IO Port / Index: 3C5.B5

GTI Control 20 Mapping Threshold Address[35:28] **Default Value: 10h**

Bit	Attribute	Default	Description
7:0	RW	10h	**Mapping Threshold Address[35:28]** GTI will map address more than this threshold (default = 4GByte) to this base address.

IO Port / Index: 3C5.B6

GTI Control 21 Mapping Threshold Address[27:20] **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Mapping Threshold Address[27:20]** GTI will map address more than this threshold (default = 4GByte) to this base address.

IO Port / Index: 3C5.B7

GTI Control 22 Mapping Threshold Address[19:12] **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Mapping Threshold Address[19:12]** GTI will map address more than this threshold (default = 4GByte) to this base address.

IO Port / Index: 3C5.B8

GTI Control 23 Mapping Threshold Address[11:4] **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Mapping Threshold Address[11:4]** GTI will map address more than this threshold (default = 4GByte) to this base address.

IO Port / Index: 3C5.C0
Video IP Clock (VDCK) Synthesizer Value 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**DM[7:0]**

IO Port / Index: 3C5.C1
Video IP Clock (VDCK) Synthesizer Value 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**{DTZ[0],2'b00,DR[2:0],DM[9:8]}**

IO Port / Index: 3C5.C2
Video IP Clock (VDCK) Synthesizer Value 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**{DTZ[1],DN[6:0]}**

IO Port / Index: 3C5.C3
Video IP Clock (VDCK) Synthesizer Control Register **Default Value: 08h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:2	RW	10b	**VDCK (Video IP Clock) PLL Power Control** 0x: PLL power-off 10: PLL always on (default) 11: PLL on/off according to the PMS
1	RW	0	**Reset VDCK PLL**
0	RW	0	**VDCK PLL Locked Detect (RO)** 0: Unlock 1: Locked

IO Port / Index: 3C5.C4
Video IP Debug Register 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**VDREG[7:0]**

IO Port / Index: 3C5.C5
Video IP Debug Register 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**VDREG[15:8]**

IO Port / Index: 3C5.C6
Video IP Debug Register 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**VDREG[23:16]**

IO Port / Index: 3C5.C7
Video IP Debug Register 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**VDREG[31:24]**

IO Port / Index: 3C5.C8

Back Light Clock Divider Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**The Clock Selected by 3C5.78[2:1]/[2*(reg+1)]**

IO Port / Index: 3C5.C9

Dynamic ECK Switching Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RW	0	**Reserved**
0	RW	0	**Selecting the Source of GFX Engine Clock** 0: GFX engine clock ECK comes from the output clock of GFX ECK PLL 1: GFX engine clock ECK comes from the output clock of PCIe PLL (200MHz)

Graphics Controller Extended Register

This section describes the graphics controller extended register definitions in detail.

IO Port / Index: 3CF.20

Offset Register Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Offset Register A Overflow Bit 9**
5	RW	0	**Offset Register A Overflow Bit 8**
4	RW	0	**Offset Register B Overflow Bit 8**
3:2	RO	0	**Reserved**
1	RW	0	**Offset Read/Write Control** 0: Offset A (Rx3CF.21) and B (Rx3CF.22) as read/write 1: Offset A as write and offset B as read
0	RW	0	**Offset Configuration** 0: Offset A and B configured as 64KB 1: Offset A and B configured as 16KB

IO Port / Index: 3CF.21

Offset Register A **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Offset A**

IO Port / Index: 3CF.22

Offset Register B **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Offset B**

CRT Controller Standard Registers

This section provides detail CRT controller standard register bit definitions. The "X" contained within the I/O port address stands for **"B"** during monochrome mode and is changed to **"D"** in color mode. For example, the I/O index for Mode Control register will be **Rx3B5.12** in monochrome mode and **Rx3D5.12** in color mode.

IO Port / Index: 3X5.00
Horizontal Total Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**HT Horizontal Total** It determines the horizontal scan time. It includes the boarder, active display time, and horizontal retrace time. VGA HT = The horizontal total -5

IO Port / Index: 3X5.01
Horizontal Display End Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**HDE Horizontal Display Enable** It determines the horizontal the number of displayed characters or character positions on a horizontal line. VGA HDE = The number of displayed characters.

IO Port / Index: 3X5.02
Horizontal Blanking Start Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**SHB Horizontal Blanking Start** The value of the character counter at the time the horizontal blanking period should begin.

IO Port / Index: 3X5.03
Horizontal Blanking End Register **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:5	RW	0	**DES Display Enable Skew** The number of character clocks to skew the position of the horizontal timing to achieve proper synchronization. The 2-bit binary value in this register represents the number of character clocks used to delay the timing.
4:0	RW	0	**EHB Horizontal Blanking End** This field is used to determine the end of the horizontal blanking period. In the VGA, a sixth bit is found in the EHB field of the End Horizontal Retrace Period.

IO Port / Index: 3X5.04
Horizontal Retrace Start Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**SHR Horizontal Retrace Start** The value used to determine the start of the horiz ontal retrace period.

IO Port / Index: 3X5.05
Horizontal Retrace End Register **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**EHB Horizontal Blanking End** The sixth bit of the EHB field found in the END Horizontal Blanking Register.
6:5	RW	0	**HRD Horizontal Retrace Delay** The skew of the horizontal retrace signal used to synchronize the display adapter with the monitor. The high-resolution advanced EGA modes require retrace delays. The binary number in this 2-bit field determines the number of character clocks to skew the system.
4:0	RW	0	**EHR End Horizontal Retrace** The 5-bit value used to determine the end of the horizontal retrace period.

IO Port / Index: 3X5.06
Vertical Total Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**VT Vertical Total** It determines the low-order 8bit of scan lines, including both displayed and non-displayed lines. It determines the frequency at which the vertical sync pulses will be generated. The high-order 3bit is defined by 3X5.35[0], 3X5.07[5], 3X507[0]

IO Port / Index: 3X5.07
Overflow Register **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**VRS Vertical Retrace Start Bit [9]** The ninth bit of the vertical retrace start value. The low-order eight bits are found in the Vertical Retrace Start Register.
6	RW	0	**VDE Vertical Display Enable End Bit [9]** The ninth bit of the vertical display start value. The low-order eight bits are found in the Vertical Display Enable End Register.
5	RW	0	**VT Vertical Total Bit [9]** The tenth bit of the vertical total value. The low-order eight bits are found in the Vertical Total Register. The ninth bit is found in the VT field of this register.
4	RW	0	**LC Line Compare** The ninth bit of the line compare value. The low-order eight bits are found in the Line Compare Register.
3	RW	0	**VBS Vertical Blanking Start Bit [8]** The ninth bit of the start vertical blanking value. The low-order eight bits are found in the Start Vertical Blanking Register.
2	RW	0	**VRS Vertical Display Enable End Bit [8]** The ninth bit of the start vertical display end value. The low-order eight bits are found in the Vertical Retrace Start Register.
1	RW	0	**VDE Vertical Display Enable End Bit [8]** The ninth bit of the start vertical display end value. The low-order eight bits are found in the Vertical Display Register.
0	RW	0	**VT Vertical Total Bit [8]** The ninth bit of the start vertical total value. The low-order eight bits are found in the Vertical Total Register. For the VGA, the tenth bit is found in the VT1 field of this register.

IO Port / Index: 3X5.08
Preset Row Scan Register **Default Value: 00h**

Bit	Attribute	Default	Description
6:5	RW	0	**BP Byte Panning** This field controls the number of bytes to pan during a panning operation. The Horizontal Panning Register determines the number of pixels to pan, and this field determines the number of bytes to pan. Together, these fields allow up to three characters to panned.
4:0	RW	0	**PRS Preset Row Scan** The starting row of a character box displayed on the top row of characters on a screen. Normally, the value in this register is 0, which displays the entire vertical extent of the top row of characters.

IO Port / Index: 3X5.09
Maximum Scan Line Register **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**2T4 200-to-400-line Conversion** Allows a 200-line mode to be displayed on 400 display scan lines. This permits the 200-line display modes to fill the entire screen. Each line is duplicated twice by dividing the clock to the row scan counter by 2. 0: Normal operation. 1: Display 200 lines on the full display.
6	RW	0	**LC Line Compare Bit [9]** The tenth bit of the Line Compare value. The low-order eight bits are found in the Line Compare Register, and the ninth bit is in the LC field of the Overflow Register.
5	RW	0	**VBS Vertical Blanking Start Bit [9]** The tenth bit of the start vertical blanking value. The lower eight bits are in the Start Vertical Blanking Register, and the ninth bit is in the VBS field of the Overflow Register.
4:0	RW	0	**MSL Maximum Scan Line** The number of scan lines in a character row minus 1.

IO Port / Index: 3X5.0A
Cursor Start Register **Default Value: 00h**

Bit	Attribute	Default	Description
5	RW	0	**COO Cursor On/Off** Allows the cursor to be turned on or off. 0: Turn the cursor off. 1: Turn the cursor on.
4:0	RW	0	**CS Cursor Start** The number of the scan line within a character box that will be the first scan line displayed for the cursor. Because the maximum character size is 32 scan lines, this value may range from 0 to 31.

IO Port / Index: 3X5.0B
Cursor End Register **Default Value: 00h**

Bit	Attribute	Default	Description
6:5	RW	0	**CSK Cursor Skew** The number of character to delay the cursor data to achieve proper synchronization. The binary amount in this field to the number of character to skew.
4:0	RW	0	**CE Cursor End** The bottom scan line to display per character row for the cursor.

IO Port / Index: 3X5.0C
Start Address High Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**SAH Start Address High** The high-order eight bits to the starting address that will determine the first data to be displayed after a vertical refresh. The low-order eight bits of the starting address are found in the Start Address Low Register. The extended 4 bits are difined by 3X5.48[3:0]

IO Port / Index: 3X5.0D
Start Address High Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**SAL Start Address Low** The low-order eight bits to the starting address that will determine the first data to be displayed after a vertical refresh. The low-order eight bits of the starting address are found in the Start Address High Register.

IO Port / Index: 3X5.0E
Cursor Location High Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**CLH Cursor Location High** The eight high-order bits of the 16-bit address that determines where the cursor will be located.

IO Port / Index: 3X5.0F
Cursor Location Low Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**CLH Cursor Location Low** The eight low-order bits of the 16-bit address that determines where the cursor will be located.

IO Port / Index: 3X5.10
Vertical Retrace Start Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**VRS Vertical Retrace Start** The eight low-order bits of the value that determines when a vertical retrace pulse begins. The scan line counter is compared to this register at each horizontal retrace time. When the scan-line counter equals this value, the vertical retrace period begins.

IO Port / Index: 3X5.11
Vertical Retrace End Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	0	**DVI Disable Vertical Interrupts** 0: Enable vertical interrupts. 1: Disable vertical interrupts.
4	RW	0	**CVI Clear Vertical Interrupts** 0: Clear the vertical interrupt. 1: No effect.
3:0	RW	0	**ERV Vertical Retrace End** The low-order five bits of the value that will cause the vertical retrace period to end. The horizontal scan line count is compared to the Vertical Retrace Start Register. When the values are equal, a vertical retrace period is started. After this time, the low-order five bits of the scan line count are compared to the five bits in the ERV field. When they are equal, the vertical retrace period ends.

IO Port / Index: 3X5.12
Vertical Display End Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**VDE Vertical Display End Enable** The low-order eight bits of the value in the Vertical Display Enable End Register. This determines the last horizontal line to be displayed on the bottom of the monitor, including the overscan region.

IO Port / Index: 3X5.13
Offset Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Offset** This register specifies the pitch of the display data address.

IO Port / Index: 3X5.14
Underline Location Register **Default Value: 00h**

Bit	Attribute	Default	Description
6	RW	0	**DW Double Word Mode** Allows normal addressing or double-word addressing. 0: Normal word addressing. 1: Double word addressing.
5	RO	0	**Reserved**
4:0	RW	0	**UL Underline Location** The value in this field minus 1 determines the horizontal scan line within a character box on which the underline will occur.

IO Port / Index: 3X5.15
Vertical Blank Start Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**VBS Vertical Blank Start** The low-order eight bits of the value that is compared to the horizontal san line counter. When these two values are equal, the vertical blanking period begins. The high-order 3bit is defined by 3X5.35[3], 3X5.09[5], 3X5.07[3]

IO Port / Index: 3X5.16
Vertical Blank End Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**VBE Vertical Blanking End** The value that determines when the vertical blanking interval should end. This value is compared to the low-order seven bits of the horizontal scan line counter.

IO Port / Index: 3X5.17

Mode Control Register **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**HR Hardware Reset** 0: Places all horizontal and vertical control timings into a hold state, thereby forcing a reset condition. 1: Enables the occurrence of the horizontal and vertical control signals.
6	RW	0	**W/B Word/Byte Mode** 0: The word mode is selected, causing the addresses bits to be shifted left one position before being output to the display memory. A more significant address bit is output on the least significant memory address line. This bit is either bit 13 or bit 15 depending on the value in the AW field in this register. 1: The byte mode is selected, causing the addresses to be output to the display memory without being shifted,
5	RW	0	**AW Address Wrap** 0: Selects address bit-13 to be sent to the least significant address bit to the display memory. This should be used when 64K bytes of memory is installed on the EGA/VGA board. 1: Select address bit-15 to be sent to the least significant address bit to the display memory. This should be used when greater than 64K bytes of memory is installed on the EGA boarder.
4:3	RO	0	**Reserved**
2	RW	0	**HRS Horizontal Retrace Select** 0: Clock the scan-line counter with every horizontal retrace. 1: Clock the scan-line counter with every horizontal retrace divided by 2 allowing up to 2,048 horizontal scan lines for the VGA.
1	RW	0	**SRS Select Row Scan Counter** 0: Row scan counter bit 1 is placed on the memory address bus bit 14 during active display time. Bit 1, placed on memory address bit 14, has the effect of quartering the memory. 1: Memory addresses are output sequentially.
0	RW	0	**CMS Compatibility Mode Support** 0: Substitutes row scan address bit 0 for memory address bit 13, causing the memory of the EGA/VGA during the graphics modes to be compatible with the CGA's 6845 controller chip. 1: Performs no substitution, causing the EGA to access memory sequentially.

IO Port / Index: 3X5.18

Line Compare Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**LC Line Compare** When the line counter is equal to the 11-bit line-compare vale, the refresh address will be cleared, causing the horizontal display lines beneath the line compare value to be refreshed from display memory address 0. The effect is a dual-screen operation. This register contains the low-order eight bits of the line-compare value. The high-order 3bit is defined by3X5.35[4] ,3X509[6], 3X5.07[4]

CRT Controller Extended Registers

This section provides detail CRT controller extended register bit definitions. The "X" contained within the I/O port address stands for **"B"** during monochrome mode and is changed to **"D"** in color mode. For example, the I/O index for Mode Control register will be **Rx3B5.32** in monochrome mode and **Rx3D5.32** in color mode.

IO Port / Index: 3X5.30

Display Fetch Blocking Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**IGA1 Digital Interface Test Enable** 0: Disable 1: Enable
6	RW	0	**Convert Primary Display Data From RGB TO YCbCr** 0: Disable 1: Enable
5	RO	0	**Reserved**
4:3	RW	00b	**DR. DAC Speed Enhancement**
2	RW	0	**On / Off Power Now Signals in Primary Path** 0: Disable 1: Enable
1:0	RW	00b	**Block T_REQ Path** 0x: Disable 10: Block request within the vertical & horizontal display area 11: Block request within the vertical display area

IO Port / Index: 3X5.31

Half Line Position **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Horizontal Half Line Count**

IO Port / Index: 3X5.32

Mode Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	000b	**HSYNC Delay Number by VCLK** 000: No delay 001: Delay + 4 VCKs 010: Delay + 8 VCKs 011: Delay + 12 VCKs 100: Delay + 16 VCKs 101: Delay + 20 VCKs Others: Undefined
4	RO	0	**Reserved**
3	RW	0	**CRT SYNC Driving Selection** 0: Low 1: High
2	RW	0	**Display End Blanking Enable** 0: Disable 1: Enable
1	RW	0	**Digital Video Port (DVP) Gamma Correction** If the gamma correction of primary display is turned on, the gamma correction in DVP can be enabled/disabled by this bit. 0: Disable 1: Enable
0	RW	0	**Real-Time Flipping** 0: Flip by the frame 1: Flip by each scan line

IO Port / Index: 3X5.33

HSYNCH Adjuster **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Primary Display Gamma Correction** 0: Disable 1: Enable
6	RW	0	**Primary Display Interlace Mode**
5	RW	0	**Horizontal Blanking End Bit [6]**
4	RW	0	**HSYNC Start Bit [8]**
3	RW	0	**Prefetch Mode** 0: Disable 1: Enable
2:0	RW	000b	**The Value will Shift the HSYNC to be Early than Planned** 000: Shift to early time by 3 character (VGA mode sugested value; default value) 001: Shift to early time by 4 character 010: Shift to early time by 5 character 011: Shift to early time by 6 character 100: Shift to early time by 7 character 101: Shift to early time by 0 character (Non-VGA mode sugested value) 110: Shift to early time by 1 character 111: Shift to early time by 2 character

IO Port / Index: 3X5.34

Starting Address Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Starting Address Overflow Bits [23:16]**

IO Port / Index: 3X5.35

Extended Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Offset Bits [10:8]**
4	RW	0	**Line Compare Bit [10]**
3	RW	0	**Vertical Blanking Start Bit [10]**
2	RW	0	**Vertical Display End Bit [10]**
1	RW	0	**Vertical Retrace Start Bit [10]**
0	RW	0	**Vertical Total Bit [10]**

IO Port / Index: 3X5.36

Power Management 3 (Monitor Control) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DPMS VSYNC Output**
6	RW	0	**DPMS HSYNC Output**
5:4	RW	00b	**DPMS Control** 00: On 01: Stand-by 10: Suspend 11: Off When the DPMS state is off, both HSYNC and VSYNC are grounded, saving monitor power consumption.
3	RW	0	**Horizontal Total Bit [8]**
2:1	RO	0	**Reserved**
0	RW	0	**PCI Power Management Control** 0: Disable 1: Enable

IO Port / Index: 3X5.37

DAC Control Register **Default Value: 04h**

Bit	Attribute	Default	Description
7	RW	0	**DAC Power Save Control 1** 0: Depend on Rx3X5.37[5:4] setting 1: DAC always goes into power save mode
6	RW	0	**DAC Power Down Control** 0: Depend on Rx3X5.47[2] setting 1: DAC never goes to power down mode
5:4	RW	00b	**DAC Power Save Control 2** 00: DAC never goes to power save mode 01: DAC goes to power save mode by line 10: DAC goes to power save mode by frame 11: DAC goes to power save mode by line and frame
3	RW	0	**DAC Current Control** 0: Not set. 1: Set a minimum level during none blanking period to increase Iout.
2:0	RW	100b	**DAC Factor** Adjusts DAC output curret, the default setting is 100b.

IO Port / Index: 3X5.38

Signature Data Register B0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Signature Data Register B0**

IO Port / Index: 3X5.39

Signature Data Register B1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Signature Data Register B1**

IO Port / Index: 3X5.3A
Signature Data Register B2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Signature Data Register B2**

IO Port / Index: 3X5.3B
Scratch Pad Register 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Scratch Pad Register 2**

IO Port / Index: 3X5.3C
Scratch Pad Register 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Scratch Pad Register 3**

IO Port / Index: 3X5.3D
Scratch Pad Register 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Scratch Pad Register 4**

IO Port / Index: 3X5.3E
Scratch Pad Register 5 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Scratch Pad Register 5**

IO Port / Index: 3X5.3F
Scratch Pad Register 6 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Scratch Pad Register 6**

IO Port / Index: 3X5.40
Test Mode Control 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Test Group Select**
3	RW	0	**Test Mode Control** 0: Disable 1: Enable
2	RW	0	**Signature Test Source** 0: Primary display 1: Secondary display
1	RW	0	**Signature Test Enable** 0: Disable 1: Enable
0	RW	0	**DAC Test Mode Control Enable** 0: Disable 1: Enable Data come from MDI[23:0].

IO Port / Index: 3X5.41~42 — Reserved

IO Port / Index: 3X5.43
IGA1 Display Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**DAC Sense Pattern [9:8]**
5:4	RW	00b	**DAC Reference Level Select** 00: 1/4 Vbg 01: 2/4 Vbg 10: 3/4 Vbg 11: 4/4 Vbg
3	RW	0	**IGA1 10 Bit Gamma Algorithm LUT256 Index 0 for Color 0** 0: Color 0 always output 10'b0 1: Color 0 output value from index 0' data
2	RW	0	**IGA1 Address Mode Selection** 0: Linear 1: Tile
1	RW	0	**IGA1 Hardware 10 Bit Gamma Enable** 0: Disable 1: Enable
0	RW	0	**IGA1 Extend 10 Bit Mode LSB Selection** 0: Always 00b 1: MSB bits

IO Port / Index: 3X5.44
DAC Sense Data **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**DAC Sense Data [7:0]**

IO Port / Index: 3X5.45
Extended Horizontal Timing Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	0	**IGA1 Screen Off Method Select** This bit is used to choose original screen off method or new method 0: Use original method 1: Use new method that only in vertical blank period that can turn off screen for no garbage
4	RW	0	**IGA1 Internal Shadow Register Select** This bit is used to select shadow or normal registers in IGA1. When it is set to 1, all operations are intended to write/read shadow registers. 0: Select normal registers 1: Select shadow registers
3	RW	0	**IGA1 Internal Shadow Register Enable** This bit is used to control using shadow 3X5.33[2:0] for standard VGA text mode or not. 0: Disable 1: Enbale
2	RW	0	**Horizontal Display Enable End Bit [9]** The ninth of the horizontal display end value. The low-order eight bits are found in the Horizontal Display Enable End Register.
1	RW	0	**Horizontal Blank Enable Start Bit [9]** The ninth of the horizontal blank start value. The low-order eight bits are found in the Horizontal Blank Enable Start Register.
0	RW	0	**Reserved**

IO Port / Index: 3X5.46
Test Mode Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
10:0	RW	0	**Load a Value to the Vertical Counter**

IO Port / Index: 3X5.47

Test Mode Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**IGA1 Timing Plus 2 VCK**
6	RW	0	**IGA1 Timing Plus 4 VCK**
5	RW	0	**Peep at the PCI Bus** 0: Disable 1: Enable
4	RW	0	**CRTC Timing Register Protect**
3	RW	0	**IGA1 Timing Plus 6 VCK**
2	RW	0	**DACOFF Backdoor Register**
1	RW	0	**LCD Simultaneous Mode Backdoor Register for 8/9 Dot Clocks**
0	RW	0	**LCD Simultaneous Mode Backdoor Register for Clock Select**

IO Port / Index: 3X5.48

Starting Address Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**IGA1 Channel Selection** 00: S.L 01: S.F. 1x: Reserved
5	RO	0	**Reserved**
4:0	RW	0	**Starting Address Overflow Bits[28:24]**

Secondary Display Register Descriptions

This section describes the secondary display I/O register bit definitions. The "X" contained within the I/O port address stands for **"B"** during monochrome mode and is changed to **"D"** in color mode. For example, the I/O index for the Second CRTC horizontal Total Period register will be **Rx3B5.50** in monochrome mode and **Rx3D5.50** in color mode.

IO Port / Index: 3X5.50
Second CRTC Horizontal Total Period **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Horizontal Total Period Bit [7:0]** ***Selected by EXCR89[1]:*** 0: For second CRTC 1: For scaling down CRTC ***When EXCR89[1]=1, selected by EXCRFD[7]:*** 0: For IGA2 scaling down CRTC 1: For IGA1 scaling down CRTC

IO Port / Index: 3X5.51
Second CRTC Horizontal Active Data Period **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Horizontal Active Data Period Bit [7:0]** ***Selected by EXCR89[1]:*** 0: For second CRTC 1: For scaling down CRTC ***When EXCR89[1]=1, selected by EXCRFD[7]:*** 0: For IGA2 scaling down CRTC 1: For IGA1 scaling down CRTC

IO Port / Index: 3X5.52
Second CRTC Horizontal Blanking Start **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Second CRTC Horizontal Blanking Start Bit [7:0]** ***Selected by EXCR89[1]:*** 0: For second CRTC 1: For scaling down CRTC ***When EXCR89[1]=1, selected by EXCRFD[7]:*** 0: For IGA2 scaling down CRTC 1: For IGA1 scaling down CRTC

IO Port / Index: 3X5.53
Second CRTC Horizontal Blanking End **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Second CRTC Horizontal Blanking End Bit [7:0]** ***Selected by EXCR89[1]:*** 0: For second CRTC 1: For scaling down CRTC ***When EXCR89[1]=1, selected by EXCRFD[7]:*** 0: For IGA2 scaling down CRTC 1: For IGA1 scaling down CRTC

IO Port / Index: 3X5.54

Second CRTC Horizontal Blanking Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Horizontal Retrace Start Bit [9:8]** ***Selected by EXCR89[1]:*** 0: For second CRTC 1: For scaling down CRTC ***When EXCR89[1]=1, selected by EXCRFD[7]:*** 0: For IGA2 scaling down CRTC 1: For IGA1 scaling down CRTC
5:3	RW	0	**Horizontal Blanking End Bit [10:8]** ***Selected by EXCR89[1]:*** 0: For second CRTC 1: For scaling down CRTC ***When EXCR89[1]=1, selected by EXCRFD[7]:*** 0: For IGA2 scaling down CRTC 1: For IGA1 scaling down CRTC
2:0	RW	0	**Horizontal Blanking Start Bit [10:8]** ***Selected by EXCR89[1]:*** 0: For second CRTC 1: For scaling down CRTC ***When EXCR89[1]=1, selected by EXCRFD[7]:*** 0: For IGA2 scaling down CRTC 1: For IGA1 scaling down CRTC

IO Port / Index: 3X5.55

Second CRTC Horizontal Period Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Horizontal Active Data Period Bit [11:8]** ***Selected by EXCR89[1]:*** 0: For second CRTC 1: For scaling down CRTC ***When EXCR89[1]=1, selected by EXCRFD[7]:*** 0: For IGA2 scaling down CRTC 1: For IGA1 scaling down CRTC
3:0	RW	0	**Horizontal Total Period Bit [11:8]** ***Selected by EXCR89[1]:*** 0: For second CRTC 1: For scaling down CRTC ***When EXCR89[1]=1, selected by EXCRFD[7]:*** 0: For IGA2 scaling down CRTC 1: For IGA1 scaling down CRTC

IO Port / Index: 3X5.56

Second CRTC Horizontal Retrace Start **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Horizontal Retrace Start Bit [7:0]** ***Selected by EXCR89[1]:*** 0: For second CRTC 1: For scaling down CRTC ***When EXCR89[1]=1, selected by EXCRFD[7]:*** 0: For IGA2 scaling down CRTC 1: For IGA1 scaling down CRTC

IO Port / Index: 3X5.57
Second CRTC Horizontal Retrace End **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Horizontal Retrace End** ***Selected by EXCR89[1]:*** 0: For second CRTC 1: For scaling down CRTC ***When EXCR89[1]=1, selected by EXCRFD[7]:*** 0: For IGA2 scaling down CRTC 1: For IGA1 scaling down CRTC

IO Port / Index: 3X5.58
Second CRTC Vertical Total Period **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Vertical Total Period [7:0]** ***Selected by EXCR89[1]:*** 0: For second CRTC 1: For scaling down CRTC ***When EXCR89[1]=1, selected by EXCRFD[7]:*** 0: For IGA2 scaling down CRTC 1: For IGA1 scaling down CRTC

IO Port / Index: 3X5.59
Second CRTC Vertical Active Data Period **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Vertical Active Data Period Bit [7:0]** ***Selected by EXCR89[1]:*** 0: For second CRTC 1: For scaling down CRTC ***When EXCR89[1]=1, selected by EXCRFD[7]:*** 0: For IGA2 scaling down CRTC 1: For IGA1 scaling down CRTC

IO Port / Index: 3X5.5A
Second CRTC Vertical Blanking Start **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Vertical Blanking Start Bit [7:0]** ***Selected by EXCR89[1]:*** 0: For second CRTC 1: For scaling down CRTC ***When EXCR89[1]=1, selected by EXCRFD[7]:*** 0: For IGA2 scaling down CRTC 1: For IGA1 scaling down CRTC

IO Port / Index: 3X5.5B

Second CRTC Vertical Blanking End **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Vertical Blanking End Bit [7:0]** ***Selected by EXCR89[1]:*** 0: For second CRTC 1: For scaling down CRTC ***When EXCR89[1]=1, selected by EXCRFD[7]:*** 0: For IGA2 scaling down CRTC 1: For IGA1 scaling down CRTC

IO Port / Index: 3X5.5C

Second CRTC Vertical Blanking Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Horizontal Retrace Bit [10]** ***Selected by EXCR89[1]:*** 0: For second CRTC 1: For scaling down CRTC ***When EXCR89[1]=1, selected by EXCRFD[7]:*** 0: For IGA2 scaling down CRTC 1: For IGA1 scaling down CRTC
6	RW	0	**Horizontal Retrace End Bit [8]** ***Selected by EXCR89[1]:*** 0: For second CRTC 1: For scaling down CRTC ***When EXCR89[1]=1, selected by EXCRFD[7]:*** 0: For IGA2 scaling down CRTC 1: For IGA1 scaling down CRTC
5:3	RW	0	**Vertical Blanking End Bit [10:8** ***Selected by EXCR89[1]:*** 0: For second CRTC 1: For scaling down CRTC ***When EXCR89[1]=1, selected by EXCRFD[7]:*** 0: For IGA2 scaling down CRTC 1: For IGA1 scaling down CRTC**]**
2:0	RW	0	**Vertical Blanking Start Bit [10:8]** ***Selected by EXCR89[1]:*** 0: For second CRTC 1: For scaling down CRTC ***When EXCR89[1]=1, selected by EXCRFD[7]:*** 0: For IGA2 scaling down CRTC 1: For IGA1 scaling down CRTC

IO Port / Index: 3X5.5D

Second CRTC Vertical Period Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Horizontal Retrace Start Bit [11]** ***Selected by EXCR89[1]:*** 0: For second CRTC 1: For scaling down CRTC ***When EXCR89[1]=1, selected by EXCRFD[7]:*** 0: For IGA2 scaling down CRTC 1: For IGA1 scaling down CRTC
6	RW	0	**Horizontal Blanking End Bit [11]** ***Selected by EXCR89[1]:*** 0: For second CRTC 1: For scaling down CRTC ***When EXCR89[1]=1, selected by EXCRFD[7]:*** 0: For IGA2 scaling down CRTC 1: For IGA1 scaling down CRTC
5:3	RW	0	**Vertical Active Data Period Bit [10:8]** ***Selected by EXCR89[1]:*** 0: For second CRTC 1: For scaling down CRTC ***When EXCR89[1]=1, selected by EXCRFD[7]:*** 0: For IGA2 scaling down CRTC 1: For IGA1 scaling down CRTC
2:0	RW	0	**Vertical Total Period Bit [10:8]** ***Selected by EXCR89[1]:*** 0: For second CRTC 1: For scaling down CRTC ***When EXCR89[1]=1, selected by EXCRFD[7]:*** 0: For IGA2 scaling down CRTC 1: For IGA1 scaling down CRTC

IO Port / Index: 3X5.5E

Second CRTC Vertical Retrace Start **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Vertical Retrace Start Bit [7:0]** ***Selected by EXCR89[1]:*** 0: For second CRTC 1: For scaling down CRTC ***When EXCR89[1]=1, selected by EXCRFD[7]:*** 0: For IGA2 scaling down CRTC 1: For IGA1 scaling down CRTC

IO Port / Index: 3X5.5F

Second CRTC Vertical Retrace End **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Vertical Retrace Start Bit [10:8]** ***Selected by EXCR89[1]:*** 0: For second CRTC 1: For scaling down CRTC ***When EXCR89[1]=1, selected by EXCRFD[7]:*** 0: For IGA2 scaling down CRTC 1: For IGA1 scaling down CRTC
4:0	RW	0	**Vertical Retrace End** ***Selected by EXCR89[1]:*** 0: For second CRTC 1: For scaling down CRTC ***When EXCR89[1]=1, selected by EXCRFD[7]:*** 0: For IGA2 scaling down CRTC 1: For IGA1 scaling down CRTC

IO Port / Index: 3X5.60

Second CRTC Vertical Status 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Vertical Count Number [7:0]**

IO Port / Index: 3X5.61

Second CRTC Vertical Status 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Vertical Retrace Status** 1: Retrace period
6	RO	0	**Vertical Active Data Status** 1: Active data period
5	RO	0	**Second Display start address change/Flip Flag**
4	RO	0	**(LVDS0) Power Sequence Flag 0** 0: Invalid 1: Valid
3	RO	0	**(LVDS1) Power Sequence Flag 1** 0: Invalid 1: Valid
2:0	RO	0	**Vertical Count Number [10:8]**

IO Port / Index: 3X5.62

Second Display Starting Address Low **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RW	0	**Second Display Starting Address Bits [9:3]** This is 1-quadword boundary.
0	RW	0	**Second Display Address Mode Selection** 0: Linear mode 1: Tile mode

IO Port / Index: 3X5.63

Second Display Starting Address Middle **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Second Display Starting Address Bits [17:10]**

IO Port / Index: 3X5.64

Second Display Starting Address High **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Second Display Starting Address Bits [25:18]**

IO Port / Index: 3X5.65

Second Display Horizontal Quadword Count Data **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Second Display Horizontal 2-Quadword Count Data Bits [7:0]**

IO Port / Index: 3X5.66

Second Display Horizontal Offset **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Second Display Horizontal Offset Bits [10:3] or Horizontal Synchronous Point**

IO Port / Index: 3X5.67

Second Display Color Depth and Horizontal Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**Color Depth** 00: 8bpp 01: 16bpp 10: 30bpp 11: 32bpp
5	RW	0	**Second Display Interlace Mode**
4	RW	0	**IGA2 Extend 10 Bit Mode LSB Selection** 0: 00b 1: MSB[7:6]
3:2	RW	0	**Second Display Horizontal 2-Quadword Count Data Bits [9:8]**
1:0	RW	0	**Second Display Horizontal Offset Bits [12:11]**

IO Port / Index: 3X5.68

Second Display Queue Depth and Read Threshold **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Display Queue Depth [3:0]** Unit 8 level ([5:4] on Rx3X5..95[7] and Rx3X5..94[7])
3:0	RW	0	**Display Queue Read Threshold 1** Unit 4 level ([6:4] on Rx3X5.95[6:4])

IO Port / Index: 3X5.69

Second Display Interrupt Enable and Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	***For Write:*** **Interrupt Clear** 1: Clear ***For Read:*** **Interrupt Status** 0: No interrupt 1: Interrupt period
6	RW	0	**Interrupt Enable** 0: Disable 1: Enable
5:0	RO	0	**Reserved**

IO Port / Index: 3X5.6A

Second Display Channel and LCD Enable **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Second Display Channel Enable** 0: Disable 1: Enable
6	RW	0	**Second Display Channel Reset** 0: Reset
5	RW	0	**Second Display 8/6 Bits LUT** 0: 6-bits 1: 8-bits
4	RW	0	**Second Display Channel Clock Mode Selection. Same with 3X5.6B[5]** 0: Normal 1: Division by 2
3	RW	0	**First Hardware Power Sequence** - ***Refer to LVDS / DVI chapter for details***
2	RW	0	**Second Display Channel Vertical Clear** 1: Clear
1	RW	0	**LCD Gamma Enable** 0: Disable 1: Enable
0	RW	0	**LCD Pre-fetch Mode Enable** 0: Disable 1: Enable

IO Port / Index: 3X5.6B

Channel 1 and 2 Clock Mode Selection **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**First Display Channel Clock Mode Selection** 0x: Normal 1x: Division by 2
5:4	RW	00b	**Second Display Channel Clock Mode Selection** 0x: Normal 1x: Division by 2
3	RW	0	**Simultaneous Display Enable** 0: Disable 1: Enable
2	RW	0	**IGA2 Screen Off** 0: Normal 1: Screen off
1	RW	0	**IGA2 Screen Off Selection Method** 0: Use 3X5.6B[2] to control IGA2 Screen off 1: Use 3C5.01[5] to control IGA2 Screen off
0	RW	0	**Horizontal Blanking Start Bit [11]** ***Selected by EXCR89[1]:*** 0: For Second CRTC 1: For Scaling Down CRTC ***When EXCR89[1]=1, selected by EXCRFD[7]:*** 0: For IGA2 Scaling Down CRTC 1: For IGA1 Scaling Down CRTC

IO Port / Index: 3X5.6C

TV CLK Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	000b	**VCK PLL Reference Clock Source Selection** 000: From XI pin 001: From TVXI 01x: From TVPLL 100: Reserved 101: DVP1TVCLKR 110: CAP0 Clock 111: CAP1 Clock
4	RW	0	**VCK Source Selection** 0: VCK PLL output clock 1: VCK PLL reference clock
3:1	RW	000b	**LCDCK PLL Reference Clock Source Selection** 000: From XI pin 001: From TVXI 01x: From TVPLL 100: Reserved 101: DVP1TVCLKR 110: CAP0 Clock 111: CAP1 Clock
0	RW	0	**LCDCK Source Selection** 0: LCDCK PLL output clock 1: LCDCK PLL reference clock

VCK Example:

IO Port / Index: 3X5.6D

Horizontal Total Shadow **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Horizontal Total Bit [7:0]**

IO Port / Index: 3X5.6E

End Horizontal Blanking Shadow **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**End Horizontal Blanking Bit [7:0]**

IO Port / Index: 3X5.6F
Vertical Total Shadow **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Vertical Total Bit [7:0]**

IO Port / Index: 3X5.70
Vertical Display Enable End Shadow **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Vertical Display Enable End Bit [7:0]**

IO Port / Index: 3X5.71
Vertical Display Overflow Shadow **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Second Display Horizontal Offset Bit [13]**
6:4	RW	0	**Vertical Display Enable End Bit [10:8]**
3	RW	0	**Horizontal Total Bit [8]**
2:0	RW	0	**Vertical Total Bit [10:8]**

IO Port / Index: 3X5.72
Start Vertical Blank Shadow **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Start Vertical Blanking Bit [7:0]**

IO Port / Index: 3X5.73
End Vertical Blank Shadow **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**End Vertical Blanking Bit [7:0]**

IO Port / Index: 3X5.74
Vertical Blank Overflow Shadow **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**For 6 Bit-LUT** 0: Send back original 8 bits data 1: Send back transformed 8 bits data
6:4	RW	0	**Start Vertical Blanking Bit [10:8]**
3	RO	0	**Reserved**
2:0	RW	0	**End Vertical Blanking Bit [10:8]**

IO Port / Index: 3X5.75
Vertical Retrace Start Shadow **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Vertical Retrace Start Bit [7:0]**

IO Port / Index: 3X5.76
Vertical Retrace End Shadow **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	0	**Vertical Retrace Start Bit [10:8]**
3:0	RW	0	**Vertical Retrace End**

IO Port / Index: 3X5.77

LCD Horizontal Scaling Factor **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**IGA1/IGA2 Horizontal Scaling Factor Bit [9:2]** ***Selected by EXCRFD[7]:*** 0: For IGA2 1: For IGA1

IO Port / Index: 3X5.78

LCD Vertical Scaling Factor **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Vertical Scaling Factor Bit [8:1]** ***Selected by EXCRFD[7]:*** 0: For IGA2 1: For IGA1

IO Port / Index: 3X5.79

LCD Scaling Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Vertical Scaling Factor Bit [10:9]** ***Selected by EXCRFD[7]:*** 0: For IGA2 1: For IGA1
5:4	RW	0	**Horizontal Scaling Factor Bit [11:10]** ***Selected by EXCRFD[7]:*** 0: For IGA1 1: For IGA2
3	RW	0	**Vertical Scaling Factor Bit [0]** ***Selected by EXCRFD[7]:*** 0: For IGA2 1: For IGA1
2	RW	0	**Vertical Scaling Selection** 0: Duplication 1: Interpolation ***Selected by EXCRFD[7]:*** 0: For IGA1 1: For IGA2
1	RW	0	**Horizontal Scaling Selection** 0: Duplication 1: Interpolation ***Selected by EXCRFD[7]:*** 0: For IGA2 1: For IGA1
0	RW	0	**LCD Scaling Enable** 0: Disable 1: Enable ***Selected by EXCRFD[7]:*** 0: For IGA2 1: For IGA1

IO Port / Index: 3X5.7A

LCD Scaling Parameter 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 1** ***Selected by EXCRFD[7]:*** 0: For IGA2 1: For IGA1

IO Port / Index: 3X5.7B

LCD Scaling Parameter 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 2** ***Selected by EXCRFD[7]:*** 0: For IGA2 1: For IGA1

IO Port / Index: 3X5.7C

LCD Scaling Parameter 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 3** ***Selected by EXCRFD[7]:*** 0: For IGA2 1: For IGA1

IO Port / Index: 3X5.7D

LCD Scaling Parameter 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 4** ***Selected by EXCRFD[7]:*** 0: For IGA2 1: For IGA1

IO Port / Index: 3X5.7E
LCD Scaling Parameter 5 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 5** ***Selected by EXCRFD[7]:*** 0: For IGA2 1: For IGA1

IO Port / Index: 3X5.7F
LCD Scaling Parameter 6 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 6** ***Selected by EXCRFD[7]:*** 0: For IGA2 1: For IGA1

IO Port / Index: 3X5.80
LCD Scaling Parameter 7 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 7** ***Selected by EXCRFD[7]:*** 0: For IGA2 1: For IGA1

IO Port / Index: 3X5.81
LCD Scaling Parameter 8 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 8** ***Selected by EXCRFD[7]:*** 0: For IGA2 1: For IGA1

IO Port / Index: 3X5.82
LCD Scaling Parameter 9 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 9** ***Selected by EXCRFD[7]:*** 0: For IGA2 1: For IGA1

IO Port / Index: 3X5.83
LCD Scaling Parameter 10 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 10** ***Selected by EXCRFD[7]:*** 0: For IGA2 1: For IGA1

IO Port / Index: 3X5.84
LCD Scaling Parameter 11 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 11** ***Selected by EXCRFD[7]:*** 0: For IGA2 1: For IGA1

IO Port / Index: 3X5.85
LCD Scaling Parameter 12 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 12** ***Selected by EXCRFD[7]:*** 0: For IGA2 1: For IGA1

IO Port / Index: 3X5.86
LCD Scaling Parameter 13 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 13** ***Selected by EXCRFD[7]:*** 0: For IGA2 1: For IGA1

IO Port / Index: 3X5.87
LCD Scaling Parameter 14 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 14** ***Selected by EXCRFD[7]:*** 0: For IGA2 1: For IGA1

IO Port / Index: 3X5.88
LCD Panel Type **Default Value: 00h**
Refer to LVDS / DVI chapter for more details

IO Port / Index: 3X5.89
LCD Timing Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**IGA1/IGA2 Buffer Sharing Enable** 0: Disable 1: Enable ***Selected by EXCRFD[7]:*** 0: For IGA2 1: For IGA1
6:1	RO	0	**Reserved**
0	RW	0	**LCD Scaling Down Function Enable** 0: Disable 1: Enable ***Selected by EXCRFD[7]:*** 0: For IGA2 1: For IGA1

IO Port / Index: 3X5.8A
LCD Timing Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	0	**Adjust FLM**
3	RO	0	**Reserved**
2:0	RW	0	**Adjust LP**

IO Port / Index: 3X5.8B
LCD Power Sequence Control 0 **Default Value: CAh**

Bit	Attribute	Default	Description
7:0	RW	CAh	**TD0 Timer Bit [7:0] (Default 32ms)**

IO Port / Index: 3X5.8C
LCD Power Sequence Control 1 **Default Value: CAh**

Bit	Attribute	Default	Description
7:0	RW	CAh	**TD1 Timer Bit [7:0] (Default 32ms)**

IO Port / Index: 3X5.8D
LCD Power Sequence Control 2 **Default Value: CAh**

Bit	Attribute	Default	Description
7:0	RW	CAh	**TD2 Timer Bit [7:0] (Default 32ms)**

IO Port / Index: 3X5.8E
LCD Power Sequence Control 3 **Default Value: CAh**

Bit	Attribute	Default	Description
7:0	RW	CAh	**TD3 Timer Bit [7:0] (Default 32ms)**

IO Port / Index: 3X5.8F

LCD Power Sequence Control 4 **Default Value: 11h**

Bit	Attribute	Default	Description
7:4	RW	1	**TD1 Timer [11:8]**
3:0	RW	1	**TD0 Timer [11:8]**

IO Port / Index: 3X5.90

LCD Power Sequence Control 5 **Default Value: 11h**

Bit	Attribute	Default	Description
7:4	RW	1	**TD3 Timer [11:8]**
3:0	RW	1	**TD2 Timer [11:8]**

IO Port / Index: 3X5.91

Software Control Power Sequence **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Software Direct On / Off Display Period in the Panel Path** 0: On 1: Off
6	RW	0	**Software On / Off Back Light Directly** 0: On 1: Off
5	RW	0	**Software Direct On / Off Display Period in the Secondary Display Path** 0: On 1: Off
4	RW	0	**Software VDD On**
3	RW	0	**Software Data On**
2	RW	0	**Software VEE On**
1	RW	0	**Software Back Light On**
0	RW	0	**Hardware or Software Control Power Sequence** 1: Software Control

IO Port / Index: 3X5.92

Read Threshold 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	1b	**IGA2 LUT Off** 0: LUT on 1: LUT off
6:4	RO	0	**Reserved**
3:0	RW	0	**Read Threshold 2**

IO Port / Index: 3X5.94

Expire Number and Display Queue Extend Bit **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Display Queue Depth Bit [4]**
6:0	RW	0	**Display2 Expire Number Bits [6:0]**

IO Port / Index: 3X5.95

Extend Threshold Bit **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Display Queue Depth Bit[5]**
6:4	RW	0	**Read Threshold 1 Bits [6:4]**
3	RO	0	**Reserved**
2:0	RW	0	**Read Threshold 2 Bits [6:4]**

IO Port / Index: 3X5.96 – Reserved

IO Port / Index: 3X5.97
LVDS Channel 1 Function Select 0 **Default Value: 00h**
Refer to LVDS / DVI chapter for more details

IO Port / Index: 3X5.98
LVDS Channel 1 Function Select 1 **Default Value: 00h**
Refer to LVDS / DVI chapter for more details

IO Port / Index: 3X5.99
LVDS Channel 0 Function Select 0 **Default Value: 00h**
Refer to LVDS / DVI chapter for more details

IO Port / Index: 3X5.9B
Digital Video Port 1 Function Select 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DVP1 ALPHA Enable** 0: Disable 1: Enable
6	RW	0	**DVP1 VSYNC Polarity** 0: Positive 1: Negative
5	RW	0	**DVP1 HSYNC Polarity** 0: Positive 1: Negative
4	RW	0	**DVP1 Data Source Selection 0** 0: Primary display 1: Secondary display
3	RW	0	**DVP1 Clock Polarity**
2:0	RW	0	**DVP1 Clock Adjust**

IO Port / Index: 3X5.9D[7]
Power Now Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Specifies the Indicator Ending Reference Point in the Vertical Blanking Period** 0: Use vertical retrace starting position 1: Use bits [6:0] of this register

IO Port / Index: 3X5.9E
Power Now Control 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Use Which Condition As The Power Now Indicator** 0: Active in the vertical blanking area 1: Active while display FIFO is almost full (refer bit[6:0])or vertical blanking period
6:0	RW	0	**Display FIFO Threshold for Power Now Indicator** The value must be divided by 4.

IO Port / Index: 3X5.9F
Power Now Control 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable the Power Now Indicator** 0: Disable 1: Enable
6:2	RO	0	**Reserved**
1:0	RW	0	**IGA1/IGA2 Horizontal Scaling Factor Bit [1:0]** ***Selected by EXCRFD[7]:*** 0: For IGA2 1: For IGA1

IO Port / Index: 3X5.A0
Horizontal Scaling Initial Value **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Horizontal Scaling Initial Value** Add on scaling factor high 8 bits.

IO Port / Index: 3X5.A1
Vertical Scaling Initial Value **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Vertical Scaling Initial Value** Add on scaling factor high 8 bits.

IO Port / Index: 3X5.A2
Scaling Enable Bit **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**IGA1/IGA2 Horizontal Scaling Enable Bit** ***Selected by EXCRFD[7]:*** 0: For IGA2 1: For IGA1
6	RW	0	**IGA1/IGA2 Horizontal Scaling Factor Selection** 0: Original 1: Linear Mode ***Selected by EXCRFD[7]:*** 0: For IGA2 1: For IGA1
5:4	RO	0	**Reserved**
3	RW	0	**IGA1/IGA2 Vertical; Scaling Enable Bit.** ***Selected by EXCRFD[7]:*** 0: For IGA2 1: For IGA1
2:0	RO	0	**Reserved**

IO Port / Index: 3X5.A3
Second Display Starting Address Extended **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5:4	RW	0	**IGA2 Frame Buffer Selection** 1x: Reserved 00: S.L 01: S.F.
3	RO	0	**Reserved**
2:0	RW	0	**Second Display Starting Address Bit [28:26]**

IO Port / Index: 3X5.A57
Second LCD Vertical Scaling Factor **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Second LCD Vertical Scaling Factor Bits [8:1]**

IO Port / Index: 3X5.A6
Second LCD Vertical Scaling Factor **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2	RW	0	**Second Vertical Scaling Factor Bit [0]**
1:0	RW	0	**Second Vertical Scaling Factor Bits [10:9]**

IO Port / Index: 3X5.A7
Expected IGA1 Vertical Display End **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Expected IGA1 Vertical Display End Bits [7:0]**

IO Port / Index: 3X5.A8
Expected IGA1 Vertical Display End **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RW	0	**Expected IGA1 Vertical Display End Bits [10:8]**

IO Port / Index: 3X5.A9
Hardware Gamma Control Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RW	0	**Hardware 10 bit Gamma Enable**
0	RW	0	**10 Bit Gamma Algorithm LUT256 Index 0 for Color 0** 0: Color 0 always output 10'b0

IO Port / Index: 3X5.AA
FIFO Depth & Threshold Overflow Bit **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Reserved**

IO Port / Index: 3X5.AB
IGA2 Interlace Half Line Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**IGA2 Interlace Half Line RegisterBits [7:0]**

IO Port / Index: 3X5.AC
IGA2 Interlace Half Line Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RW	0	**IGA2 Interlace Half Line Register Bits [10:8]**

IO Port / Index: 3X5.AF
P-Arbiter Write Expired Number Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**P-Arbiter Write Expired NumberBits [4:0]**

IO Port / Index: 3X5.D0
LVDS PLL Control Register **Default Value: 00h**
Refer to LVDS / DVI chapter for more details

IO Port / Index: 3X5.D1
DVI PLL Control Register **Default Value: 00h**
Refer to LVDS / DVI chapter for more details

IO Port / Index: 3X5.D2
LVDS / DVI Control Register **Default Value: 00h**
Refer to LVDS / DVI chapter for more details

IO Port / Index: 3X5.D3
Second Power Sequence Control Register 0 **Default Value: 00h**
Refer to LVDS / DVI chapter for more details

IO Port / Index: 3X5.D4
Second Power Sequence Control Register 1 **Default Value: 00h**
Refer to LVDS / DVI chapter for more details

IO Port / Index: 3X5.D5
LVDS Testing Mode Control Register **Default Value: 00h**
Refer to LVDS / DVI chapter for more details

IO Port / Index: 3X5.D6
DCVI Control Register 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DCVI Data Testing Mode** 0: Disable 1: Enable
6	RW	0	**DCVI Format Selection** 0: 656 or 601 output 1: 20 bit output
5	RW	0	**DVCI Format Source Selection High Bit** 0: Reference Rx3X5.9B[4] 1: P2I mode
4	RO	0	**Reserved**
3	RW	0	**DCVI Output Format Selection** 0: Original 1: TV5 mode
2	RW	0	**DCVI Dither Enable**
1	RW	0	**DCVI Color Space Convert Enable**
0	RW	0	**DCVI Enable** 0: Off 1: On

IO Port / Index: 3X5.D7
DCVI Control Register 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**DCVI Output Field Polarity** 0: Original 1: Invert
2:0	RW	0	**DCVI Field Delay Lines After Vertical Blank Start**

IO Port / Index: 3X5.D8
PLL Control Register **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**VCOMODE3 (INTLCDCK)** PLL Output Frequency Select: 1X or 2X 0: 1X 1: 2X
6	RW	0	**VCOMODE2 (INTECK)** PLL Output Frequency Select: 1X or 2X 0: 1X 1: 2X
5	RW	0	**VCOMODE1 (INTVCK)** PLL Output Frequency Select: 1X or 2X 0: 1X 1: 2X
4:0	RO	0	**Reserved**

IO Port / Index: 3X5.D9
Scaling Down Source Data Offset Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Scaling Down Source Data Horizontal Offset Bits [7:0]** Unit: pixel (2P)

IO Port / Index: 3X5.DA
Scaling Down Source Data Offset Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Scaling Down Source Data Vertical Offset Bits [7:0]** Unit: pixel (2P)

IO Port / Index: 3X5.DB
Scaling Down Source Data Offset Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5:3	RW	0	**Scaling Down Source Data Vertical Offset Bits [10:8]** Unit : pixel (2P)
2:0	RW	0	**Scaling Down Source Data Horizontal Offset Bits [10:8]** Unit : pixel (2P)

IO Port / Index: 3X5.DC
Scaling Down Horizontal Scale Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Horizontal Scale Factor Bits [7:0]**

IO Port / Index: 3X5.DD
Scaling Down Horizontal Scale Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DN Flip Select**
6	RW	0	**Horizontal Scale Down Enable** 0: Disable 1: Enable
5:0	RW	0	**Horizontal Scale Factor Bits [13:8]**

IO Port / Index: 3X5.DE
Scaling Down Vertical Scale Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Vertical Scale Factor Bits [7:0]**

IO Port / Index: 3X5.DF
Scaling Down Vertical Scale Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Vertical Scale Down Enable** 0: Disable 1: Enable
5:0	RW	0	**Vertical Scale Factor Bits [13:8]**

IO Port / Index: 3X5.E0
Scaling Down Destination Frame Buffer Starting Address 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Destination Frame Buffer Starting Address 0 Bits [10:3]**

IO Port / Index: 3X5.E1
Scaling Down Destination Frame Buffer Starting Address 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Destination Frame Buffer Starting Address 0 Bits [18:11]**

IO Port / Index: 3X5.E2

Scaling Down Destination Frame Buffer Starting Address 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Destination Frame Buffer Starting Address 0 Bits [26:19]**

IO Port / Index: 3X5.E3

Scaling Down Destination Frame Buffer Starting Address 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Scaling Down Function RGB Setting** 00: RGB32 01: RGB8 10: RGB565 11: RGB10
5:4	RW	0	**SW Source Frame Buffer Stride Bits [9:8]**
3:2	RW	0	**Reserved**
1:0	RW	0	**Destination Frame Buffer Starting Address 0 Bits [28:27]**

IO Port / Index: 3X5.E4

Scaling Down SW Source Frame Buffer Stride **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**SW source Frame Buffer Stride Bits [7:0]** Unit: 16 bytes

IO Port / Index: 3X5.E5

Scaling Down Destination Frame Buffer Starting Address 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Destination Frame Buffer Starting Address 1 Bits [10:3]**

IO Port / Index: 3X5.E6

Scaling Down Destination Frame Buffer Starting Address 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Destination Frame Buffer Starting Address 1 Bits [18:11]**

IO Port / Index: 3X5.E7

Scaling Down Destination Frame Buffer Starting Address 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Destination Frame Buffer Starting Address 1 Bits [26:19]**

IO Port / Index: 3X5.E8

Scaling Down Destination Frame Buffer Starting Address 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Which IGA Run Scaling Down** 0:IGA1 1:IGA2
6	RW	0	**Line Flip Enable** 0: Disable 1: Enable
5	RW	0	**Flip** IGA2 can start to get next frame
4	RW	0	**Scaling Down Enable** 0: Disable 1: Enable
3:2	RW	0	**Destination Frame Buffer Starting Address 2 Bits [28:27]**
1:0	RW	0	**Destination Frame Buffer Starting Address 1 Bits [28:27]**

IO Port / Index: 3X5.E9

Scaling Down Destination Frame Buffer Starting Address 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Destination Frame Buffer Starting Address 2 Bits [10:3]**

IO Port / Index: 3X5.EA

Scaling Down Destination Frame Buffer Starting Address 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Destination Frame Buffer Starting Address 2 Bits [18:11]**

IO Port / Index: 3X5.EB

Scaling Down Destination Frame Buffer Starting Address 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Destination Frame Buffer Starting Address 2 Bits [26:19]**

IO Port / Index: 3X5.EC

IGA1 Down Scaling Destination Control Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2	RW	0	**IGA1 Down Scalar Line Flip**
1	RW	0	**IGA1 Down Scalar Flip**
0	RW	0	**IGA1 Down Scalar Enable**

IO Port / Index: 3X5.F0

SNAPSHOT Mode – Starting Address of Display Data **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Snapshot Mode TVPK_SRC Bits [11:4]**

IO Port / Index: 3X5.F1

SNAPSHOT Mode – Starting Address of Display Data **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Snapshot Mode TVPK_SRC Bits [19:12]**

IO Port / Index: 3X5.F2

SNAPSHOT Mode – Starting Address of Display Data **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Snapshot Mode TVPK_SRC Bits [27:20]**

IO Port / Index: 3X5.F3
SNAPSHOT Mode Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**For 18 bits TTL_LCD**
6	RW	0	**Snapshot Mode TVPK_SRC Bit [28]**
5	RW	0	**SW Set NM and GFX Entering Snapshot in C0 State** 0: Disable 1: Enable
4	RW	0	**Snapshot Mode** 0 : Mode 0 1 : Mode 1
3	RO	0	**Snapshot PLL Wakeup Setting** 0: Counter (2ms) 1: PLL_OK
2	RW	0	**Snapshot Mode Enable** 0: Disable 1: Enable GFX support Snapshot mode.
1	RW	0	**Enable GFX PLL Power Off When In Snapshot Mode** 0: Disable 1: Enable
0	RO	0	**The VSYNC and HSYNC of DAC0 Are Tied** 0: VSYNC and HSYNC are normal 1: Tied

IO Port / Index: 3X5.F4
SNAPSHOT Mode Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**PK_HREQ_THD Bits [2:0]**
4:0	RW	0	**PK_REQ_THD Bits [4:0]**

IO Port / Index: 3X5.F5
SNAPSHOT Mode Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**The VSYNC and HSYNC of DAC1 Are Tied** 0: VSYNC and HSYNC are normal 1: Tied
6:5	RW	0	**PK_HREQ_THD Bits [4:3]**
4:0	RW	0	**PK_EXPIR_NUM Bits [4:0]**

IO Port / Index: 3X5.F6
SNAPSHOT Mode Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**The VSYNC Count While Engine Is Idle and SW Enables Snapshot (G2N_SW_VIDLE_CNT)** In C0 state, the idle VSYNC count to disable the G2N_SW_SNAPSHOT_EN.

IO Port / Index: 3X5.F7

Internal Spread Spectrum Control CH0 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Select Internal/External Clock Source** 0: External 1: Internal
6	RW	0	**Power Down Control** 0: Disable 1: Enable
5:4	RW	0	**Frequency Selection (FREQ_SEL[1:0])** Digital logic input used to select Input Clock Frequency Range. See Input Clock Frequency Selection Table below.
3:2	RW	0	**Spreading Range Selection (SR_SEL[1:0])** Digital logic input used to select Spreading Range. See Modulation Selection Table below.
1	RW	0	**FM Selection (FM_SEL)** Digital logic input used to select modulation rate. See Modulation Selection Table below.
0	RW	0	**Spread Spectrum Enable (S_EN)** Digital logic input used to enable Spread Spectrum function. 0: Disable 1: Enable (3C5.7D[7] or [5] must be 1)

Modulation Selection Table

FM_SEL	SR_SEL[1:0]	Spreading Range	Modulation Rate (KHz)
0	00	± 1.0%	Fin/1152
0	01	± 1.5%	Fin/1152
0	10	± 2.0%	Fin/1152
0	11	± 2.5%	Fin/1152
1	00	Reserved	Reserved
1	01	Reserved	Reserved
1	10	± 2.0%	Fin/1920
1	11	± 2.5%	Fin/1920

Input Clock Selection Table

Input Clock Range	FREQ_SEL[1:0]
25~40MHz	00
40~65MHz	01
65~110MHz	10
110~135MHz	11

IO Port / Index: 3X5.F9

V1 Power Control 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**The Period Between NB Trigger GFX to Exit V1 Power Mode** The period between NB trigger GFX to exit V1 power mode and GFX really exit V1 power mode. (Unit: frame)

IO Port / Index: 3X5.FA

V1 Power Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**The Status of GFX V1 Mode to SB** This bit is sent to SB when GFX is in V1 power mode. This bit is set to 1'b1 by HW and reset to 1'b0 by SW.

IO Port / Index: 3X5.FB

IGA2 Interlace VSYNC Timing Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**The Offset Cycle of VSYNC[7:0]**

IO Port / Index: 3X5.FC

IGA2 Interlace VSYNC Timing Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RW	0	**The Offset Cycle of VSYNC[10:8]**

IO Port / Index: 3X5.FD

IGA1 Scaling Up and Timing Control

Bit	Attribute	Default	Description
7	RW	0	**Scaling Up Parameter Destination Select** 0: for IGA2 1: for IGA1
6	RO	0	**Reserved**
5	RW	0	**IGA1 Scaling Up Parameter Source Select** 0 : All parameters configured by IO (Shared registers with IGA2) 1 : All parameters configured by MMIO (Start from +840C)
4:3	RO	0	**Reserved**
2	RW	0	**Power Sequence PAD Select** 0: Share PAD for LVDS0 power sequence signals. 1: Share PAD for LVDS1 power sequence signals.
1	RW	0	**IGA2 Color Space Conversion Enable** 0: CSC Disable 1: CSC Enable
0	RW	0	**CRTC Programing Selection** 0: Program Second CRTC. 1: Program Scaling Down CRTC.

IO Port / Index: 3X5.FF

V1 Power Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**Reserved**
2	RW	0	**HDTV1 Source Select**
1	RW	0	**HDTV0 Source Select**
0	RW	0	**Reserved**

IGA1 Display Engine MMIO Registers

Register Space 0x00008400-0x0000843F is assigned to VGA. All offset and default values are shown in hexadecimal unless otherwise indicated.

Offset Address: 840F-840Ch

IGA1 Scaling Function Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**IGA1 Scaling Up Enable**
30	RW	0	**Vertical Scaling Enable** 0: Disable 1: Enable
29	RW	0	**Vertical Interpolation Enable** 0: Disable 1: Enable
28:27	RO	0	**Reserved**
26:16	RW	0	**Scaling Vertical Factor**
15	RW	0	**Horizontal Scaling Enable** 0: Disable 1: Enable
14	RW	0	**Horizontal Interpolation Enable** 0: Disable 1: Enable
13	RW	0	**Scaling MUX disable** 0: Enable 1: Disable
12	RO	0	**Reserved**
11:0	RW	0	**Horizontal Scaling Factor**

Offset Address: 8413-8410h

Scaling Parameter Setting 1-4 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:24	RW	0	**Scaling Parameter 4**
23:21	RO	0	**Reserved**
20:16	RW	0	**Scaling Parameter 3**
15:13	RO	0	**Reserved**
12:8	RW	0	**Scaling Parameter 2**
7:5	RO	0	**Reserved**
4:0	RW	0	**Scaling Parameter 1**

Offset Address: 8417-8414h

Scaling Parameter Setting 5-8 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:24	RW	0	**Scaling Parameter 8**
23:21	RO	0	**Reserved**
20:16	RW	0	**Scaling Parameter 7**
15:13	RO	0	**Reserved**
12:8	RW	0	**Scaling Parameter 6**
7:5	RO	0	**Reserved**
4:0	RW	0	**Scaling Parameter 5**

Offset Address: 841B-8418h

Scaling Parameter Setting 9-C **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:24	RW	0	**Scaling Parameter C**
23:21	RO	0	**Reserved**
20:16	RW	0	**Scaling Parameter B**
15:13	RO	0	**Reserved**
12:8	RW	0	**Scaling Parameter A**
7:5	RO	0	**Reserved**
4:0	RW	0	**Scaling Parameter 9**

Offset Address: 841F-841Ch

Scaling Parameter Setting D/E **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:13	RO	0	**Reserved**
12:8	RW	0	**Scaling Parameter E**
7:5	RO	0	**Reserved**
4:0	RW	0	**Scaling Parameter D**

Offset Address: 8433-8430h

Power Management IDLE Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**PMU IDLE Control**

2D ENGINE REGISTERS

This chapter provides 2D register summary table and detailed graphics engine register descriptions.

2D Engine Register Summary

These 2D engine register table documents the MMIO offset , register function and register attribute for each register.

Please note that the actual address equals to MB1 (MMIO Base Address) + Offset Address. MB1 is declared in the register with offset address 17h-14h in the PCI configuration space.

Table 9. Graphics Engine Registers

Offset (Hex.)	2D Engine Registers	Attribute
03-00	GE Command	RW
07-04	GE Mode and Status	RW
0B-08	Pitch & FB Location	RW
0F-0C	Destination Dimension	RW
13-10	BitBLT Destination Address	RW
17-14	Destination Map Base Address	RW
1B-18	BitBLT Source Address	RW
1F-1C	Source Map Base Address	RW
23-20	Pattern Address	RW
27-24	Mono Pattern Data Port 0 or Style Line	RW
2B-28	Mono Pattern Data Port 1	RW
2F-2C	Error Term of Line Draw	RW
33-30	Color format conversion (CFC)	RW
43-40	Clipping Window Top and Left Limit	RW
47-44	Clipping Window Bottom and Right Limit	RW
4B-48	Color Key and Chroma Key Control	RW
4F-4C	Foreground Color or Destination Color Key or Line Color or Rectangle Fill Color	RW
53-50	Background Color or Source Color key	RW
5B-58	Foreground Color of Pattern	RW
5F-5C	Background Color of Pattern	RW
60-9F	Reserved	RO
1FF-100	Color Pattern RAM Port 0 – 63	WO

Graphics Engine Register Descriptions

This section provides detailed register descriptions for the 2D graphics engine.

Offset Address: 03-00h

GE Command **Default Value: 0000 0000h**

Bit	Attribut	Default	Description
31:24	RW	0	**Raster Operation Code (ROP code)**
23	RW	0	**Quick Start Enable** 0: Disable 1: Enable When enabled, a command will be kicked off when a command writes to register 10h, saving one command write instruction.
22	RW	0	**Pattern Keep** 0: Must get somewhere (bitmap pattern register or frame buffer) to pattern RAM. 1: Current pattern RAM (directly use pattern RAM data without filling it again).
21	RW	0	**Line Draws Major** 0: X major 1: Y major
20	RW	0	**Line Draw Last Pixel Turn On Disable** 0: Enable, draw the last pixel or not. 1: Disable, do not draw the last pixel.
19:18	RW	0	**Monochrome Data Next Line Alignment Type (if Alignments Enable)** 00: Byte 01: Reserved 10: Dword 11: Reserved
17	RW	0	**Monochrome Data Alignment Enable** 0: Disable 1: Enable
16	RW	0	**Monochrome Pattern Transparency Enable** 0: Opaque 1: Transparency
15	RW	0	**Destination X-Direction Select** 0: Increment 1: Decrement
14	RW	0	**Destination Y-Direction Select** 0: Increment 1: Decrement
13	RW	0	**Fix Color Pattern** 0: Normal 1: Fix Color
12	RW	0	**Clipping Enable** 0: Disable 1: Enable
11	RW	0	**Pattern Source Select** 0: Pattern from frame buffer 1: Pattern from pattern register
10	RW	0	**Monochrome Source Transparency Enable** 0: Opaque 1: Transparency
9	RW	0	**Pattern Data Format** 0: Color 1: Monochrome
8	RW	0	**Source Data Format** 0: Color 1: Monochrome
7	RO	0	**Reserved**
6	RW	0	**Source Select** 0: On-screen frame buffer 1: From host
5:4	RW	0	**Reserved**
3:0	RW	0000b	**GE Command Select** 0000: No operation 0001: Bit BLT 0010: Text (mono, ROP == CC) 0011: AlphaBLT(ROP == CC) 0101: Bresenham line draw 1001: Bitblt then rotate 1010: Text (mono, ROP == CC) then rotate Others: Reserved

Offset Address: 07-04h

GE Mode and Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:10	RO	0	**Reserved**
20	RW	0	**Alpha Value Select** 0: Set per pixel alpha value 1: Set constant alpha value
19:12	RW	0	**Constant Alpha Value**
9:8	RW	00b	**Destination Color Depth Select** 00: 8 bpp 01: 16 bpp 10: Reserved 11: 32 bpp
7:2	RO	0	**Reserved**
1:0	RW	00b	**Rotation Angle (Hardware: 90=270, diff. X/YDIR)** 00: Rotate 0 degree 01: Rotate anticlockwise 90 degree 10: Rotate anticlockwise 180 degree 11: Rotate anticlockwise 270 degree

Offset Address: 0B-08h

Pitch and FB Location **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RW	00b	**Destination FB Location** 00: S.L. 01: S.F. 10: Reserved 11: L.L.
29:27	RO	0	**Reserved**
26:16	RW	0	**Destination Pitch; 64-bit Address (128 Bit Alignment)**
15:14	RW	00b	**Pattern FB Location** 00: S.L. 01: S.F. 10: Reserved 11: L.L.
13:12	RW	00b	**Source FB Location** 00: S.L. 01: S.F. 10: Reserved 11: L.L.
11	RO	0	**Reserved**
10:0	RW	0	**Source Pitch** 64-bit address (128-bit alignment).

Offset Address: 0F-0Ch

Destination Dimension **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:16	RW	0	**BitBLT Destination Rectangle Height** These bits specify the destination rectangle height (value = height – 1) for the BitBLT operation.
15:12	RO	0	**Reserved**
11:0	RW	0	**BitBLT Destination Rectangle Width** These bits specify the destination rectangle width (value = width – 1) for the BitBLT operation.

Offset Address: 13-10h

BitBLT Destination Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Destination Tile Add Control** 0: Normal 1: Tile
30:28	RO	0	**Reserved**
27:16	RW	0	**BitBILT Destination Address** For BitBLT, bits [27:16] specify the destination y-position.
15:12	RW	0	**Reserved**
11:0	RW	0	**BitBILT Destination Address** For BitBLT, bits [11:0] specify the destination x-position operation.

Offset Address: 17-14h

Destination Map Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RO	0	**Reserved**
25:0	RW	0	**Destination Map Base Address** 64-bit address (128-bit alignment).

Offset Address: 1B-18h

BitBLT Source Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Source Tile Add Control** 0: Normal 1: Tile
30	RO	0	**Reserved**
29:16	RW	0	**BitBILT Source Address** These bits are used for three different commands: 1. For color or mono BitBLT, bits [27:16] specify the source y-position (XY based). 2. For line draw, bits [29:16] specify the axial step (K1 term of Bresenham line draw).
15:0	RW	0	**BitBILT Source Address** These bits are used for four different commands: 1. For color BitBLT, bits [11:0] specify the source x-position (XY based). 2. For mono BitBLT, bits [14:0] specify the source x-position. 3. For line draw, bits [13:0] specify the diagonal step (K2 term of Bresenham line draw).

Offset Address: 1F-1Ch

Source Map Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RO	0	**Reserved**
25:0	RW	0	**Source Base Address; 64-bit address (128 bit alignment).**

Offset Address: 23-20h

Pattern Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RW	0	**Pattern Offset** Bits [31:29]: Start line(Y) location (0~7) Bits [28:26]: 1. Pattern from frame buffer : Start location(X) in a line (0~7) 2. Pattern from frame host : Dest. start location(X) in a line (0~7)
25:0	RW	0	**Pattern Base Address** These bits are used for the following different purposes: For 8x8 pattern, bits [25:0] specify the 8x8 pattern address stored in the off-screen frame buffer, 64-bit address (128 bit alignment).

Offset Address: 27-24h

Mono Pattern Data Port 0 / Style Line **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Pattern 0**

Offset Address: 2B-28h

Mono Pattern Data Port 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Pattern 1**

Offset Address: 2F-2Ch

Error Term of Line Draw **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RW	0	**Error Term for Textured Line** The error term for textured line.
15:14	RO	0	**Reserved**
13:0	RW	0	**Error Term** The error term for line.

Offset Address: 33-30h

Color format conversion (CFC) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Color Format Conversion Enable** If Disable : HW ignore Source Color depth (Bits[7:6]). Set Source Color depth = Dest. Color depth & set Source Color format = Dest. Color format
30	RW	0	**CFC Extending Mode(Excluding Alpha)** For Alpha channel, always extended with high color bit. 0 : Extending with high color bit 1 : Extending with zero
29	RW	0	**CFC Dither Mode** 0: Dither Table 1: Rounding
28:10	RO	0	**Reserved**
9:8	RW	0	**Destination Color Format** ***16BPP:*** 00: RGB555 (Bits[14:10] = R, Bits[9:5] = G, Bits[4:0] = B) 01: RGB565 (Bits[15:11] = R, Bits[10:5] = G, Bits[4:0] = B) 1x: Reserved ***32BPP:*** 00:ARGB8888 (Bits[31:24] = A, Bits[23:16] = R, Bits[15:8] = G, Bits[7:0] = B) 01: ARGB2_10_10_10 (Bits[31:30] = A, Bits[29:20] = R, Bits[19:10] = G, Bits[9:0] = B) 1x: Reserved
7:6	RW	0	**Source Color Depth Select** 00: 8 bpp 01: 16 bpp 10: Reserved 11: 32 bpp
5:2	RO	0	**Reserved**
1:0	RW	0	**Source Color Format** ***16BPP:*** 00: RGB555 (Bits[14:10] = R, Bits[9:5] = G, Bits[4:0] = B) 01: RGB565 (Bits[15:11] = R, Bits[10:5] = G, Bits[4:0] = B) 1x: Reserved ***32BPP:*** 00:ARGB8888 (Bits[31:24] = A, Bits[23:16] = R, Bits[15:8] = G, Bits[7:0] = B) 01: ARGB2_10_10_10 (Bits[31:30] = A, Bits[29:20] = R, Bits[19:10] = G, Bits[9:0] = B) 1x: Reserved

Offset Address: 43-40h

Clipping Window Top and Left Limit **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:16	RW	0	**Top Limit for Clipping Operation** For clipping operation, these bits specify the top limit.
15:12	RO	0	**Reserved**
11:0	RW	0	**Left Limit for Clipping Operation** For clipping operation, these bits specify the left limit.

Offset Address: 47-44h

Clipping Window Bottom and Right Limit **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:16	RW	0	**Bottom Limit for Clipping Operation** For clipping operation, these bits specify the bottom limit.
15:12	RO	0	**Reserved**
11:0	RW	0	**Right Limit for Clipping Operation** For clipping operation, these bits specify the right limit.

Offset Address: 4B-48h

Color Key and Chroma Key Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RW	0	**The Byte Mask of 32 bpp in Rectangle Fill Mode** 0: Write 1: Not write (mask)
27:16	RO	0	**Reserved**
15	RW	0	**Destination Key Select** 0: Disable 1: Enable
14	RW	0	**Source Key Select** 0: Disable 1: Enable
13	RW	0	**Key Type** 0: Write if same / match 1: Write if diff / not match
12:0	RO	0	**Reserved**

Offset Address: 4F-4Ch

Foreground Color or Destination Color Key or Line Color or Rectangle Fill Color **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	For each bpp mode, bits [bpp-1:0] specify foreground color or destination color key.

Offset Address: 53-50h

Background Color or Source Color Key or Chroma Key Upper Bound **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	For each bpp mode, bits [bpp-1:0] specify background color or source color key or chroma key upper bound.

Offset Address: 54-57h – Reserved

Offset Address: 5B-58h

Foreground Color of Pattern **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Foreground Color of Mono Pattern**

Offset Address: 5F-5Ch

Background Color of Pattern **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Background Color of Mono Pattern**

3D / 2D Control Registers (60-1FFh)

Offset Address: 60-9Fh – Reserved

Offset Address: 1FF-100h

Color Pattern RAM Port 0 –Port 63 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	WO	0	**Color Pattern Data**

DMA REGISTERS

This chapter provides detailed DMA register summary table and register descriptions are followed in the sequent section.

DMA Register Summary

These DMA register tables document the MMIO offset , register function and register attribute for each register.

Table 10. DMA Controller Operation Registers

Offset	DMA Controller Operation Registers	Attribute
03-00h	Channel 0 Mode (MR0)	RW
07-04h	Channel 0 Command / Status (CSR0)	RW
0B-08h	Channel 1 Mode (MR1)	RW
0F-0Ch	Channel 1 Command / Status (CSR1)	RW
13-10h	Channel 2 Mode (MR2)	RW
17-14h	Channel 2 Command / Status (CSR2)	RW
1B-18h	Channel 3 Mode (MR3)	RW
1F-1Ch	Channel 3 Command / Status (CSR3)	RW
23-20h	Memory Address Low Register of Channel 0 (MARL0)	RW
27-24h	Memory Address High Register of Channel 0 (MARH0)	RW
2B-28h	Channel 0 Device Address (DAR0)	RW
2F-2Ch	Double Quad-Word Count Register of Channel 0 (DQWCR0)	RW
33-30h	Tile Mode Register of Channel 0 (TMR0)	RW
37-34h	Descriptor Pointer Low Register of Channel 0 (DPRL0)	RW
3B-38h	Descriptor Pointer High Register of Channel 0 (DPRH0)	RW
43-40h	Memory Address Low Register of Channel 1 (MARL1)	RW
47-44h	Memory Address High Register of Channel 1 (MARH1)	RW
4B-48h	Channel 1 Device Address (DAR1)	RW
4F-4Ch	Double Quad-Word Count Register of Channel 1 (DQWCR1)	RW
53-50h	Tile Mode Register of Channel 1 (TMR1)	RW
57-54h	Descriptor Pointer Low Register of Channel 1 (DPRL1)	RW
5B-58h	Descriptor Pointer High Register of Channel 1 (DPRH1)	RW
63-60h	Memory Address Low Register of Channel 2 (MARL2)	RW
67-64h	Memory Address High Register of Channel 2 (MARH2)	RW
6B-68h	Device Address Register of Channel 2 (DAR2)	RW
6F-6Ch	Double Quad-Word Count Register of Channel 2 (DQWCR2)	RW
73-70h	Tile Mode Register of Channel 2 (TMR2)	RW
77-74h	Descriptor Pointer Low Register of Channel 2 (DPRL2)	RW
7B-78h	Descriptor Pointer High Register of Channel 2 (DPRH2)	RW
83-80h	Memory Address Low Register of Channel 3 (MARL3)	RW
87-84h	Memory Address High Register of Channel 3 (MARH3)	RW
8B-88h	Channel 3 Device Address (DAR3)	RW
8F-8Ch	Double Quad-Word Count Register of Channel 3 (DQWCR3)	RW
93-90h	Tile Mode Register of Channel 3 (TMR3)	RW
97-94h	Descriptor Pointer Low Register of Channel 3 (DPRL3)	RW
9B-98h	Descriptor Pointer High Register of Channel 3 (DPRH3)	RW
123-120h	Byte Enable Register of Channel 0 (BER0)	RW
127-124h	Destination Dimension Register of Channel 0 (DDR0)	RW
12B-128h	Pitch Memory Address Low Register of Channel 0 (PMARL0)	RW
12F-12Ch	Pitch Memory Address High Register of Channel 0 (PMARH0)	RW
133-130h	Pitch Device Address Register of Channel 0 (PDAR0)	RW

Offset	DMA Controller Operation Registers	Attribute
137-134h	Pitch Mode Register of Channel 0 (PMR0)	RW
143-140h	Byte Enable Register of Channel 1 (BER1)	RW
147-144h	Destination Dimension Register of Channel 1 (DDR1)	RW
14B-148h	Pitch Memory Address Low Register of Channel 1 (PMARL1)	RW
14F-14Ch	Pitch Memory Address High Register of Channel 1 (PMARH1)	RW
153-150h	Pitch Device Address Register of Channel 1 (PDAR1)	RW
157-154h	Pitch Mode Register of Channel 1 (PMR1)	RW
163-160h	Byte Enable Register of Channel 2 (BER2)	RW
167-164h	Destination Dimension Register of Channel 2 (DDR2)	RW
16B-168h	Pitch Memory Address Low Register of Channel 2 (PMARL2)	RW
16F-16Ch	Pitch Memory Address High Register of Channel 2 (PMARH2)	RW
173-170h	Pitch Device Address Register of Channel 2 (PDAR2)	RW
177-174h	Pitch Mode Register of Channel 2 (PMR2)	RW
183-180h	Byte Enable Register of Channel 3 (BER3)	RW
187-184h	Destination Dimension Register of Channel 3 (DDR3)	RW
18B-188h	Pitch Memory Address Low Register of Channel 3 (PMARL3)	RW
18F-18Ch	Pitch Memory Address High Register of Channel 3 (PMARH3)	RW
193-190h	Pitch Device Address Register of Channel 3 (PDAR3)	RW
197-194h	Pitch Mode Register of Channel 3 (PMR3)	RW

Note: 1. The offset address for all registers is MB1 + 0x0E00 and these registers can be re-allocated by changing the base address registers MB1.

Table 11. DMA Controller Operation Registers (by Channel)

Register Name	Channel 0		Channel 1		Channel 2		Channel 3	
	Offset	Register	Offset	Register	Offset	Register	Offset	Register
MRn: Channel n Mode	03-00	MR0	0B-08	MR1	13-10	MR2	1B-18	MR3
CSRn: Channel n Command / Status	07-04	CSR0	0F-0C	CSR1	17-14	CSR2	1F-1C	CSR3
MARLn: Memory Address Low Register of Channel n	23-20	MARL0	43-40	MARL1	63-60	MARL2	83-80	MARL3
MARHn: Memory Address High Register of Channel n	27-24	MARH0	47-44	MARH1	67-64	MARH2	87-84	MARH3
DARn: Channel n Device Address	2B-28	DAR0	4B-48	DAR1	6B-68	DAR2	8B-88	DAR3
DQWCRn: Double Quad-Word Count Register of Channel n	2F-2C	DQWCR0	4F-4C	DQWCR1	6F-6C	DQWCR2	8F-8C	DQWCR3
TMRn: Tile Mode Register of Channel n	33-30	TMR0	53-50	TMR1	73-70	TMR2	93-90	TMR3
DPRLn: Descriptor Pointer Low Register of Channel n	37-34	DPRL0	57-54	DPRL1	77-74	DPRL2	97-94	DPRL3
DPRHn: Descriptor Pointer High Register of Channel n	3B-38	DPRH0	5B-58	DPRH1	7B-78	DPRH2	9B-98	DPRH3
Byte Enable Register	123-120	BER0	143-140	BER1	163-160	BER2	183-180	BER3
Destination Dimension Register	127-124	DDR0	147-144	DDR1	167-164	DDR2	187-184	DDR3
Pitch Memory Address Low Register	12B-128	PMARL0	14B-148	PMARL1	16B-168	PMARL2	18B-188	PMARL3
Pitch Memory Address High Register	12F-12C	PMARH0	14F-14C	PMARH1	16F-16C	PMARH2	18F-18C	PMARH3
Pitch Device Address Register	133-130	PDAR0	153-150	PDAR1	173-170	PDAR2	193-190	PDAR3
Pitch Mode Register	137-134	PMR0	157-154	PMR1	177-174	PMR2	197-194	PMR3

DMA Operation Register Descriptions

Following registers are the DMA Operation registers used to control the operation of the DMA controller. Address space mentioned in the following registers (except MAR) is frame buffer address space.

Mode Register (MRn)

Offset Address: {MR0 = 0x00, MR1 = 0x08, MR2 = 0x10, MR3 = 0x18} **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RO	0	**Reserved**
1	RW	0	**Transfer Done Interrupt Enable** A value of 1 enables the interrupt to be generated when transfer is done.
0	RW	0	**Chaining Mode** A value of 1 causes the DMA controller to operate in chaining mode.

Command/ /Status Register (CSRn)

Offset Address: {CSR0 = 0x04, CSR1 = 0x0C, CSR2 = 0x14, CSR3 = 0x1C} **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	0	**Reserved**
3	RWC	0	**Transfer Done** A value of 1 indicates that the transfer of this channel is complete. Writing a 1 will clear this bit and the interrupt due to this event when TDIE is set to 1. This field can ONLY be written from CBU path.
2	RW	0	**Transfer Abort** Writing a 1 to this bit causes the channel to abort the current transfer. This channel transfer done bit is set when the abort is complete. Reading this bit always gets 0. This field can ONLY be written from CBU path.
1	RW	0	**Transfer Start** Writing 1 to this bit causes the channel to start transferring data if the channel is enabled. Reading this bit always gets 0.
0	RW	0	**DMA Enable** A value of 1 enables this DMA channel.

Low 28 Bits Register (MARLn)

Offset Address: {MARL0 = 0x20, MARL1 = 0x40, MARL2 = 0x60, MARL3 = 0x80} **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RW	0	**Memory Address Lower 28 Bits** This field indicates the starting memory address (lower 28 bits) of a DMA transfer. The unit is 128-bit.
3:0	RO	0	**Reserved**

High 12 Bits Register (MARHn)

Offset Address: {MARH0 = 0x24, MARH1 = 0x44, MARH2 = 0x64, MARH3 = 0x84} **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RO	0	**Reserved**
11:0	RW	0	**Memory Address Higher 12 Bits** This field indicates the starting memory address (higher 12 bits) of a DMA transfer. The unit is byte.

Device Address Register (DARn)

Offset Address: {DAR0 = 0x28, DAR1 = 0x48, DAR2 = 0x68, DAR3 = 0x88} **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RW	0	**Device Addressing Type** This field indicates the memory translation type of the starting device address of a DMA transfer. 0x0: System Local Frame Buffer (SL) 0x1: System Dynamic Frame Buffer (SF) 0x2: Reserved, do not use. 0x3: Local Memory / Local Frame Buffer (LL)
29	RO	0	**Reserved**
28:4	RW	0	**Device Address** This field indicates the starting device address of a DMA transfer. In the Tile Mode transfer, this filed must point to the starting address of memory tile.
3:0	RO	0	**Reserved**

Double Quad-word Count Register(DQWCRn)

Offset Address: {DQWCR0 = 0x2C, DQWCR1 = 0x4C, DQWCR2 = 0x6C, DQWCR3 = 0x8C}

Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:25	RO	0	**Reserved**
24:0	RW	0	**Double Quad-Word Count** This field indicates the number of 16-byte count to be transferred during a DMA transfer. It will be cleared when the transfer is done by hardware.

Tile Mode Register (TMRn)

Offset Address: {TMR0 = 0x30, TMR1 = 0x50, TMR2 = 0x70, TMR3 = 0x90} **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Tile Mode Enable** A value of 1 enables tile mode memory mapping for the coming device memory transfer.
30:28	RO	0	**Reserved**
27:24	RW	0	**Tile Mode Index** This field indicates the starting location of the current tile for the current transfer descriptor. It will be cleared when the transfer is done by hardware. This filed is used ONLY in the tile mode, otherwise this field is reserved.
23:16	RW	0	**Tile Mode Pitch Count** This field indicates the pitch count for the tile mode transfer. A value of 00h indicates the maximum pitch count, 256. This filed is used only in the tile mode.
15:8	RO	0	**Reserved**
7:0	RW	0	**Tile Mode Horizontal Tile Index** This field indicates the horizontal tile index for the tile mode transfer. This filed is used only in the tile mode.

Low 32 Bit Register (DPRLn)

Offset Address: {DPRL0 = 0x34, DPRL1 = 0x54, DPRL2 = 0x74, DPRL3 = 0x94} **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RW	0	**Next Descriptor Address Lower 28 Bits** This field indicates the lower 28 bits of the double quad-word aligned address of the next descriptor.
3	RW	0	**Direction of Transfer** A value of 1 indicates transfers from memory to PCI device. A value of 0 indicates transfers from PCI device to memory.
2	RO	0	**Reserved**
1	RW	0	**End of Chain** A value of 1 indicates the end of chain.
0	RO	0	**Reserved**

High 12 Bit Register (DPRHn)

Offset Address: {DPRH0 = 0x38, DPRH1 = 0x58, DPRH2 = 0x78, DPRH3 = 0x98} **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RO	0	**Reserved**
11:0	RW	0	**Next Descriptor Address Higher 12 Bits** This field indicates the higher 12 bits of the double quad-word aligned address of the next descriptor.

Byte Enable Register (BERn)

Offset Address: {BER0 = 0x120, BER1 = 0x140, BER2 = 0x160, BER3 = 0x180} **Default Value: 0000 0F0Fh**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:12	RW	0	**DMA Transaction Starting Memory Address Lower 4 Bits** This field indicates the starting memory address (lower 4 bits) of a DMA destination transfer. In unit of byte. This filed is used only in the pitch mode.
11:8	RW	F	**DMA Transaction Ending Memory Address Lower 4 Bits** This field indicates the ending memory address (lower 4 bits) of a DMA destination transfer. In unit of byte. This filed is used only in the pitch mode.
7:4	RW	0	**DMA Transaction Starting Memory Address Lower Bits** This field indicates the starting memory address (lower 4 bits) of a DMA source transfer. In unit of byte. This filed is used only in the pitch mode.
3:0	RW	F	**DMA Transaction Ending Memory Address Lower 4 Bits** This field indicates the ending memory address (lower 4 bits) of a DMA source transfer. In unit of byte. This filed is used only in the pitch mode.

Destination Dimension Register (DDRn)

Offset Address: {DDR0 = 0x124, DDR1 = 0x144, DDR2 = 0x164, DDR3 = 0x184} **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Direction of Moving** A value of 1 indicates transfers from system memory to frame buffer. A value of 0 indicates transfers from frame buffer to system memory.
30:28	RO	0	**Reserved**
27:16	RW	0	**Destination Rectangle Height** The destination rectangle height equals the value. In unit of line. When setup this field ,BERn must be set first.
15:9	RO	0	**Reserved**
8:0	RW	0	**Destination Rectangle Width** The destination rectangle width equals the value. In unit of 128-bit. When setup this field, BERn must be set first.

Low 28 Bit Register (PMARLn)

Offset Address: {PMARL0 = 0x128, PMARL1 = 0x148, PMARL2 = 0x168, PMARL3 = 0x188}

Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:4	RW	0	**Pitch Memory Address Lower 28 Bits** This field indicates the starting pitch memory address (lower 28 bits) of a DMA transfer. In unit of 128-bit.
3:0	RO	0	**Reserved**

High 12 Bit Register (PMARHn)

Offset Address: {PMARH0 = 0x12C, PMARH1 = 0x14C, PMARH2 = 0x16C, PMARH3 = 0x18C} **Attribute: RW**

Bit	Attribute	Default	Description
31:12	RO	0	**Reserved**
11:0	RW	0	**Pitch Memory Address Higher 12 Bits** This field indicates the starting pitch memory address (higher 12 bits) of a DMA transfer. In unit of 128-bit.

Pitch Device Address Register (PDARn)

Offset Address: {PDAR0 = 0x130, PDAR1 = 0x150, PDAR2 = 0x170, PDAR3 = 0x190} **Attribute: RW**

Bit	Attribute	Default	Description
31:30	RW	0	**Pitch Device Addressing Type** This field indicates the memory translation type of the starting pitch device address of a DMA transfer. 0x0: System Local Frame Buffer (SL) 0x1: System Dynamic Frame Buffer (SF) 0x2: Reserved, do NOT use 0x3: Local Memory / Local Frame Buffer (LL)
29	RO	0	**Reserved**
28:4	RW	0	**Pitch Device Address** This field indicates the starting pitch device address of a DMA transfer. In unit of 128-bit.
3:0	RO	0	**Reserved**

Pitch Mode Register (PMRn)

Offset Address: {PMR0 = 0x134, PMR1 = 0x154, PMR2 = 0x174, PMR3 = 0x194} **Attribute: RW**

Bit	Attribute	Default	Description
31	RW	0	**Pitch Mode Enable** A value of 1 enables pitch mode memory mapping for the coming device memory transfer.
30	RW	0	**Pitch Support Tile Address Mode Enable** A value of 1 enables pitch mode memory support tile address mapping for the coming device memory transfer.
29	RO	0	**Reserved**
28	RW	0	**Tile Mode Index of Pitch Destination** This field indicates the starting location of the current tile for the current transfer descriptor. It will be cleared when the transfer is done by hardware. This filed is used only in the tile mode and move data from system memory to frame buffer, otherwise this field is reserved.
27	RO	0	**Reserved**
26	RW	0	**Tile Mode Index of Pitch Destination** This field indicates the starting location of the current tile for the current transfer descriptor. It will be cleared when the transfer is done by hardware. This filed is used only in the tile mode and move data from frame buffer to system memory, otherwise this field is reserved.
25	RO	0	**Reserved**
24:16	RW	0	**Destination Pitch Mode Pitch Count** This field indicates the pitch count for the pitch mode transfer. This filed is used only in the pitch mode.
15	RO	0	**Reserved**
14:11	RW	0	**Frame Buffer Tile Index** This field indicates the index of starting position with frame buffer tile mode.
10:9	RO	0	**Reserved**
8:0	RW	0	**Source Pitch Mode Pitch Count** This field indicates the pitch count for the pitch mode transfer. This filed is used only in the pitch mode.

CBU ROTATION REGISTERS

This chapter provides detailed CBU register summary table and its detailed register descriptions are followed in the sequent sections.

CBU Register Summary

The CBU Rotation Function Register Table documents the offset range, register name and register attribute for each Rotate Window Register.

Table 12. CBU Rotation Function Registers

Offset	CDMA Controller Operation Registers	Attribute
1E1C-1E00	Rotate Window Register 0	RW
1E3C-1E20	Rotate Window Register 1	RW
1E5C-1E40	Rotate Window Register 2	RW
1E7C-1E60	Rotate Window Register 3	RW
1E9C-1E80	Rotate Window Register 4	RW
1EBC-1EA0	Rotate Window Register 5	RW
1EDC-1EC0	Rotate Window Register 6	RW
1EFC-1EE0	Rotate Window Register 7	RW
1F1C-1F00	Rotate Window Register 8	RW
1F3C-1F20	Rotate Window Register 9	RW
1F5C-1F40	Rotate Window Register 10	RW
1F7C-1F60	Rotate Window Register 11	RW
1F9C-1F80	Rotate Window Register 12	RW
1FBC-1FA0	Rotate Window Register 13	RW
1FDC-1FC0	Rotate Window Register 14	RW
1FFC-1FE0	Rotate Window Register 15	RW

Note: Rotation Base Address[28:16], Rotation End Address[28:16] and Rotation Source Pitch[21:0] are write-only. Reading these bits always gets 0.

CBU Rotation Register Descriptions

There are 16 Rotate Window Registers, ranging from Rotate Window Register 0 to Rotate Window Register 15. The table below specifies the standard structure of each Rotate Window Register.

Offset	CDMA Controller Operation Registers	Attribute
03h-00h	Rotate Control 0	RW
07h-04h	Rotate Base Address 0	RW
0Bh-08h	Rotate End Address 0	RW
0Fh-0Ch	Rotate Source Pitch 1 0	RW
13h-10h	Rotate Pitch 0	RW
17h-14h	Rotate Height and Width 0	RW
1Ch-18h	Reserved	RW

Offset Address: Rotate Window Register Address + (03h-00h)

Rotate Control **Default Value: 0000 0000h**

Bit	Attribut	Default	Description
31:8	RO	0	**Reserved**
7	RW	0	**Tile Mapping Mode Select** When this bit is set to 1 and bit 6 (Rotate function with tile) is set to 0, 16 x 256 tile mapping mode is used to translate linear address to tiling address. 0: 8 x 256 tile mapping mode 1: 16 x 256 tile mapping mode
6	RW	0	**Rotate Function with Tile** When this bit is set to 1, translated linear address to tiling address within rotation mode is supported.
5	RW	0	**Tile Function Flag** When bit 0 (Rotate Function Enable) is set to 1, this bit shows the function which is supported. 0: Rotate function 1: Tile function
4:3	RW	00b	**Rotate Type** 00: No support 01: 90 degrees 10: 180 degrees 11: 270 degrees
2:1	RW	00b	**Rotate Bpp** 00: 8 bpp 01: 16 bpp 1x: 32 bpp
0	RW	0	**Rotate Function Enable** 0: Disable 1: Enable

Offset Address: Rotate Window Register Address + (07h-04h)

Rotate Base Address **Default Value: 0000 0000h**

Bit	Attribut	Default	Description
31:29	RO	0	**Reserved**
28:0	RW	0	**Rotate Base Address [28:0]** Bits [3:0] are read only. Unit: byte

Offset Address: Rotate Window Register Address + (0Bh-08h)

Rotate Window Size **Default Value: 0000 0000h**

Bit	Attribut	Default	Description
31:30	RO	0	**Reserved**
29:0	RW	0	**Rotate End Address [29:0]** Bits [3:0] are read only. Unit: byte

Offset Address: Rotate Window Register Address + (0Fh-0Ch)

Rotate Source Pitch 1 **Default Value: 0000 0000h**

Bit	Attribut	Default	Description
31:0	RW	0	**Rotate Source Pitch Reciprocal** 32 bits (1/source pitch, source pitch unit: pixel) (1/sp = 0.x, for example, Source pitch = 256 d, x = 1000000h)

Offset Address: Rotate Window Register Address + (13h-10h)

Rotate Pitch **Default Value: 0000 0000h**

Bit	Attribut	Default	Description
31:16	RW	0	**Rotate Destination Pitch** Unit: pixel Scope: 1 ~ 65536
15:0	RW	0	**Rotate Source Pitch** Unit: pixel Scope: 1 ~ 65536

Offset Address: Rotate Window Register Address + (17h-14h)

Rotate Height and Width **Default Value: 0000 0000h**

Bit	Attribut	Default	Description
31:16	RW	0	**Rotate Window Height** Unit: pixel Scope: 1 ~ 65536
15:0	RW	0	**Rotate Window Width** Unit: pixel Scope: 1 ~ 65536

LVDS / DVI REGISTERS

This chapter is dedicated for detailed LVDS and DVI register descriptions.

IO Port / Index: 3C5.13 [7:6]
Configuration Register 2 (3C5.5A[0]=1) **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	00b	**Integrated LVDS / DVI Mode Select** Reflects strapping from signal DVP1D15/14. 00: LVDS1 01: Reserved 10: No effect 11: No effect

IO Port / Index: 3C5.1A [5:4]
PCI Bus Control **Default Value: 00h**

Bit	Attribute	Default	Description
5	RW	0	**Reserevd**
4	RW	0	**Reserved**

IO Port / Index: 3C5.2B [7:4]
LVDS Interrupt Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW1C	0	**Reserved**
5	RW	0	**LVDS Sense Interrupt Enable** 0: Disable 1: Enable
4	RW1C	0	**LVDS Sense Interrupt Status**

IO Port / Index: 3C5.3E

Miscellaneous Register for AGP Mux **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW1C	0	**Reserved**
5	RW	0	**Reserved**
3	RW	0	**PCIe Capability Control Back Door** 0: Capability = 00h 1: Capability = 70h
1	RW	0	**Multi-function Selection** 0: Emulate I^2C and DDC Bus by GPIO2/3/4 1: Direct ENPVDD/ ENPVEE / ENBLT signals through AGP Bus
0	RW	0	**Second DVIDET Sense Signal Source** 0: Reserved 1: From DVP1

IO Port / Index: 3C5.40 [3]

PLL Control **Default Value: 00h**

Bit	Attribute	Default	Description
3	RW	0	**LVDS and DVI Interrupt Method** 0: New method (bypass and low active) 1: Old method

IO Port / Index: 3C5.5B [3:0]

Device Used Status 0 **Default Value: 00h**

Bit	Attribute	Default	Description
3	RO	0	**LVDS0 Used IGA1 Source Flag** 0: No use 1: Use
2	RO	0	**LVDS0 Used IGA2 Source Flag** 0: No use 1: Use
1	RO	0	**LVDS1 Used IGA1 Source Flag** 0: No use 1: Use
0	RO	0	**LVDS1 Used IGA2 Source Flag** 0: No use 1: Use

IO Port / Index: 3C5.78 [6:3]

Backlight Control 3 **Default Value: 00h**

Bit	Attribute	Default	Description
6	RW	0	**Inverse IGA2 HSYNC to LVDS**
5	RW	0	**Inverse IGA2 VSYNC to LVDS**
4	RW	0	**Inverse IGA1 HSYNC to LVDS**
3	RW	0	**Inverse IGA1 VSYNC to LVDS**

IO Port / Index: 3C5.7D [2:0]

Power Down Output Pad Polarity **Default Value: 00h**

Bit	Attribute	Default	Description
2	RW	0	**The LVDSENVDD Pad Output Polarity** 0: Inversed 1: Normal
1	RW	0	**Reserved**
0	RO	0	**LVDS Channel 0 Power Down Output Polarity** 0: Inversed 1: Normal

IO Port / Index: 3X5.6A [3]

Second Display Channel and LCD Enable **Default Value: 00h**

Bit	Attribute	Default	Description
3	RW	0	**First Hardware Power Sequence** 0: Off 1: On

IO Port / Index: 3X5.88

LCD Panel Type **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Spread Spectrum FIFO Reset** 0: Reset 1: Normal
6	RW	0	**LVDS First Channel 0 (LVDS0) Output Format** 0: Rotation 1: Sequential
5	RW	0	**Flip Strategy** 0: By frame 1: By line
4:1	RO	0	**Reserved**
0	RW	0	**LVDS Second Channel 0 Output Bits (LVDS0 dither enable)** 0: 24 bits 1: 18 bits

IO Port / Index: 3X5.97

LVDS Channel 1 Function Select 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Reserved**
5	RW	0	**Reserved**
4	RW	0	**LVDS Channel 1 Data Source Selection** 0: Primary Display 1: Secondary Display
3:0	RO	0	**Reserved**

IO Port / Index: 3X5.98

LVDS Channel 1 Function Select 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6:4	RW	0	**Reserved**
3:0	RO	0	**Reserved**

IO Port / Index: 3X5.99

LVDS Channel 0 Function Select 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**LVDS Channel 0 VSYNC Polarity** 0: Positive 1: Negative
5	RW	0	**LVDS Channel 0 HSYNC Polarity** 0: Positive 1: Negative
4	RW	0	**LVDS Channel 0 Data Source Selection** 0: Primary Display 1: Secondary Display
3:0	RO	0	**Reserved**

IO Port / Index: 3X5.9A

LVDS Channel 0 Function Select 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**LVDS Channel 0 DE Mask to Zero Enable**
6	RW	0	**LVDS Channel 0 VSYNC Mask to Zero Enable**
5	RW	0	**LVDS Channel 0 HSYNC Mask to Zero Enable**
4	RW	0	**Reserved**
3:0	RO	0	**Reserved**

IO Port / Index: 3X5.D0

LVDS PLL Control Register **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**PLL1 Reference Clock Edge Select Bit** 0: PLLCK lock to rising edge of reference clock 1: PLLCK lock to falling edge of reference clock
6:5	RW	0	**PLL1 Charge Pump Current Set Bits** 00: ICH = 12.5 uA 01: ICH = 25.0 uA 10: ICH = 37.5 uA 11: ICH = 50.0 uA
4	RW	0	**Choose LVDS Driver Power Down Attribute** 0: Tri-state (Hi-Z) 1: Drive low
3	RO	0	**Reserved**
2:0	RW	0	**PLL1 Output Clock (PLLCK) Delay Select Bits** 000: T_{DLY} = 0.82 nS 001: T_{DLY} = 0.1T + 0.82 nS 010: T_{DLY} = 0.2T + 0.82 nS 011: T_{DLY} = 0.3T + 0.82 nS 100: T_{DLY} = 0.4T + 0.82 nS

IO Port / Index: 3X5.D1

DVI PLL Control Register **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6:5	RW	0	**Reserved**
4:3	RW	0	**Reserved**
2	RO	0	**Reserved**
1	RO	0	**TX PLL1 Ready** 0: Not ready 1: Ready
0	RW	0	**Reserved**

IO Port / Index: 3X5.D2

LVDS / DVI Control Register **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Power Down (Active High) for Channel 01 LVDS** The output polarity is controlled by VGA register 3C5.7D[7]. 0: Disable 1: Enable
6	RW	0	**Reserevd**
5:4	RW	0	**Display Channel Select** 00: LVDS Channel 0 Others: Reserved
3	RW	0	**Enable LVDSENVDD Pad Output** 0: Disable 1: Enable
2	RO	0	**Reserved**
1	RW	0	**LVDS Channel 0 Format Selection** 0: SPWG Mode 1: OPENLDI Mode
0	RW	0	**Reserved**

IO Port / Index: 3X5.D3

Second Power Sequence Control Register 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Software Direct On / Off Display Period in the Panel Path** 0: On 1: Off
6	RW	0	**Software On / Off Back Light Directly** 0: On 1: Off
5	RW	0	**Software Direct On / Off Display Period on DVP1 Port** 0: On 1: Off
4	RW	0	**Software VDD On**
3	RW	0	**Software Data On**
2	RW	0	**Software VEE On**
1	RW	0	**Software Back Light On**
0	RW	0	**Hardware or Software Control Power Sequence** 1: Software Control

IO Port / Index: 3X5.D4

Second Power Sequence Control Register 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**Reserved**
5:2	RO	0	**Reserved**
1	RW	0	**Secondary Power Hardware Power Sequence Enable** 0: Off 1: On
0	RW	0	**Power Sequence Timer Selection** 0: First (LVDS0) 1: Second (LVDS1)

IO Port / Index: 3X5.D5

LVDS Testing Mode Control Register **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**PD1 Enable Selection** 0: Select by register 1: Select by power flag
6	RW	0	**PD2 Enable Selection** 0: Select by register 1: Select by power flag
5	RW	0	**Reserved**
4	RW	0	**Reserved**
3	RO	0	**Reserved**
2	RW	0	**LVDS Testing Mode Enable**
1:0	RW	0	**LVDS Testing Format Selection** 00: Always 0 01: Always 1 1x: 0, 1 toggle

IO Port / Index: 3X5.F3 [7]

18 Bits TTL LCD **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved** Must set to 1 for normal function.

DISPLAY PORT REGISTERS

This chapter provides detailed Display Port register and its detailed register descriptions are followed in the sequent sections. Please note that there are no default values in Display Port, unless otherwise indicated. Please note that the actual address equals to MB1 (MMIO Base Address) + Offset Address. **MB1** is declared in the register with offset address 14h~17h in the Device 1 Function 0 PCI configuration space.

Integrated Display Port Register Descriptions

Offset Address: C613h-C610h (DISPLAY PORT-MMIO)

Display Port 1 Attribute Data Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RW	0	**Miscellaneous Main Stream Attribute Data** ***Bits[31:27]***: Reserved, set to 0 ***Bits[26:25]***: Stereo video attribute ***Bit 24***: Interlaced vertical total even
23:0	RW	0	**N for Stream Clock Recovery**

Offset Address: C617-C614h (DISPLAY PORT-MMIO)

Display Port 1 Link Training Control Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**DP1 Link Training Done** 0: Not done 1: Done. When SW starts HW link training, need to poll this bit. If this bit is set to 1, check C640[29:28] also to see if LT success or not. Software write 0 to clear this bit.
30	RW	0	**Clock Recovery Sequence Fail** 0: Not take action 1: SW set Link training fail. If AUX_CH reads that Not all LANEX_CR_DONE bits are 1, then set this bit (refer 1.1 spec fig 2-36, when this bit set link training state transfer to not enabled state, SW need to do HW or SW link training.
29:28	RW	0	**Software Lane 3 Pre-emphasis**
27:26	RW	0	**Software Lane 3 Swing**
25:24	RW	0	**Software Lane 2 Pre-emphasis**
23:22	RW	0	**Software Lane 2 Swing**
21:20	RW	0	**Software Lane 1 Pre-emphasis**
19:18	RW	0	**Software Lane 1 Swing**
17:16	RW	0	**Software Lane 0 Pre-emphasis**
15:14	RW	0	**Software Lane 0 Swing**
13	RW	0	**Software Bit Rate** 0: 1.62G bit rate 1: 2.7G bit rate
12:11	RW	00b	**Software Link Training State** 00: Not enabled 01: Clcok recovery state 10: Channel EQ state 11: Normal state
10	RW	0	**Software Link Training Enable** 0: Disable 1: Enable
9:7	RW	0	**Number of Lanes** 001: 1 lane 010: 2 lanes 100: 4 lanes Other values are not allowed
6	RW	0	**SW hpd Asserted** Enable display port spec. V1.1 fig 2-32 AUX CH Source state change from S1 to S2.
5:4	RW	0	**MAX Pre-emphasis in HW Link Training Mode** Must be 10b or 11b.
3:2	RW	0	**MAX Voltage Swing in HW Link Training Mode** Must be 10b or 11b.
1	RW	0	**Start Link Rate** 0: 1.62G bit rate 1: 2.7G bit rate

0	RW	0	**Start Link Training** 0: Not start HW Link training 1: Start HW Link training. This bit should be cleared to 0 immediately after set to 1 by SW.

Offset Address: C61B-C618h (DISPLAY PORT-MMIO)

Display Port 1 General Controller Register **Default Value: n038 0000h**

Bit	Attribute	Default	Description
31	RW	-	**Reserved**
30	RW	0	**Video Input Selection** 0: HDTV0 1: HDTV1
29:24	RW	20h	**HDEN / VDEN / VSYN Delay Control** The min delay number is 0 stream clock period. The max delay number is 63 stream clock period.
23:18	RW	0Eh	**Ddefine the SYNC Data Pulse in AUX lphy's Manchester II Decoder** 09h~0Eh is suggested.
17	RO	0	**Hardware Link Training AUX Fail** 0: Aux is ok. 1: If HW link training AUX_READ or AUX_WR meets 7 consecutive not ACK reply (DEFFER or NACK or invalid reply), then set this bit, and HW link training failed , need driver to perform SW link training or other thing. Software write 0 to clear this bit.
16	RW	0	**Audio Stream Selection** Not decoded in DP module 0: Audio Codec 1 1: Audio Codec 2
15:11	RO	0	**AUX Length**
10:2	RO	0	**IDLE Pattern Counter**
1	RW	0	**Switch Mode of IDLE Pattern to Video** 0: Audio Sample does not send immediately after C640[3]=1. 1: Audio Sample continue sending after C640[3]=1
0	RW	0	**Enable Main Link Lane Scrambler** 0: Disable main link lane scrambler 1: Enable main link lane scrambler

Offset Address: C61F-C61Ch (DISPLAY PORT-MMIO)

Display Port 1 Extension Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**DP Clock Selection** (for debug only) 0: Select EPHY MPLL clock as DP clock 1: Select DCLK1 as DP clock
30	RW	0	**Horizontal Width bit 11** Bits[10:0] are at C644[10:0].
29:24	RW	0	**Reserved**
23:0	RW	0	**The Header of Extension Packet**

Offset Address: C623-C620h (DISPLAY PORT-MMIO)
Display Port 1 MMIO FIFO Register 0 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Display Port 1 MMIO FIFO 0**

Offset Address: C627-C624h (DISPLAY PORT-MMIO)
Display Port 1 MMIO FIFO Register 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Display Port 1 MMIO FIFO 1**

Offset Address: C62B-C628h (DISPLAY PORT-MMIO)
Display Port 1 MMIO FIFO Register 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Display Port 1 MMIO FIFO 2**

Offset Address: C62F-C62Ch (DISPLAY PORT-MMIO)
Display Port 1 MMIO FIFO Register 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Display Port 1 MMIO FIFO 3**

Offset Address: C633-C630h (DISPLAY PORT-MMIO)
Display Port 1 MMIO FIFO Register 4 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Display Port 1 MMIO FIFO 4**

Offset Address: C637-C634h (DISPLAY PORT-MMIO)
Display Port 1 MMIO FIFO Register 5 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Display Port 1 MMIO FIFO 5**

Offset Address: C63B-C638h (DISPLAY PORT-MMIO)
Display Port 1 MMIO FIFO Register 6 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Display Port 1 MMIO FIFO 6**

Offset Address: C63F-C63Ch (DISPLAY PORT-MMIO)
Display Port 1 MMIO FIFO Register 7 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Display Port 1 MMIO FIFO 7**

Offset Address: C643-C640h (DISPLAY PORT-MMIO)

Display Port 1 General Control Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RW	00b	**Test Pattern Select Signal** 00: Link quality test pattern not transmitted 01: D10.2 test pattern transmitted 10: Symbol error rate measurement pattern transmitted 11: PRBS7 transmitted
29:28	RO	00b	**Mainlink Status** 00: Main link is disabled 01: Clock recovery pattern transmitted 10: Channel EQ pattern transmitted 11: Normal operation
27:26	RW	0	**Reserved**
25	RW	0	**Generate MVID in Asynchronous Mode**
24	RW	0	**Enable Audio** 0: Disable 1: Enable
23	RW	0	**Enable Extension Packet** 0: Disable 1: Enable
22:19	RW	0	**InfoFrame FIFO 2 Length**
18:15	RW	0	**InfoFrame FIFO 1 Length**
14:11	RW	0	**InfoFrame FIFO 2 Start Address**
10:7	RW	0	**InfoFrame FIFO 1 Start Address**
6	RW	0	**InfoFrame FIFO Select** 0: Take InfoFrame Packet from FIFO 1 1: Take InfoFrame Packet from FIFO 2
5	RW	0	**InfoFrame FIFO 2 Ready**
4	RW	0	**InfoFrame FIFO 2 Ready**
3	RW	0	**Video Enable** 0: Idle Pattern transmitted 1: Video transmitted
2	RW	0	**Enhanced Framing Mode** 0: Default framing mode 1: Enhanced framing mode
1	RW	0	**Field Invert** 0: The FieldID_Flag in VBID is same as HDTV module output 1: The FieldID_Flag in VBID is the inverter of HDTV module output
0	RW	0	**Display Port 1 Enable** 0: DP1 disable 1: DP1 enable

Offset Address: C647-C644h (DISPLAY PORT-MMIO)

Display Port 1 General Control Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:17	RW	0	**TU_Ratio**
16:11	RW	0	**DP Required TU Size** DP require TU size is 32~64 Programme this register to (TU size -1)
10:0	RW	0	**Horizontal Width is 12 Bits** The MSB is at C61C[30]. The value = (the number of horizontal active pixel/lane number) -1

Offset Address: C64B-C648h (DISPLAY PORT-MMIO)

Display Port 1 General Control Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Extension Packet Valid Signal** Software writes 1 to this bit to indicate hardware to transmit extension packet. Hardware clears this bit after the extension packet is sent.
30:27	RW	0	**Byte Number of Extensioin Packet**
26:15	RW	0	**Number of LS_CLK in Horizontal Blank** The value = (HBLANK_time * Link_symbol_clock_frequency) -15
14:0	RW	0	**Number of LS_CLK in One Line** The value = (Link_symbol_clock_frequency/horizontal_frequency) -15

Offset Address: C64F-C64Ch (DISPLAY PORT-MMIO)

Display Port 1 Attribute Data Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RW	0	**Miscellaneous Main Stream Attribute Data** ***Bits[31:29]***: Bit depth per color/component ***Bit 28***: YCbCr Colorimetry 0: ITU-R BT601-5 1: ITU-R BT709-5 ***Bit 27***: Dynamic range 0: VESA range 1: CEA range ***Bits [26:25]***: Component format 00: RGB 01: YCbCr 4:2:2 10: YCbCr 4:4:4 ***Bit 24*** 0: Asynchronous Clock 1: Synchronous Clock
23:0	RW	0	**M for Stream Clock Recovery**

Offset Address: C653-C650h (DISPLAY PORT-MMIO)

Display Port 1 Attribute Data Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RW	0	**Vertical Totals of the Transmitted Main Video Stream in Line Counts**
15:0	RW	0	**Horizontal Totals of the Transmitted Main Video Stream in Pixel Counts**

Offset Address: C657-C654h (DISPLAY PORT-MMIO)

Display Port 1 Attribute Data Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RW	0	**Vertical Active Start from the Leading Edges of Vsync in Line**
15:0	RW	0	**Horizontal Active Start from the Leading Edges of Hsync in Pixel**

Offset Address: C65B-C658h (DISPLAY PORT-MMIO)

Display Port 1 Attribute Data Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RW	0	**Vsync Polarity / Vsync Width in Line**
15:0	RW	0	**Hsync Polarity / Hsync Width in Pixel**

Offset Address: C65F-C65Ch (DISPLAY PORT-MMIO)

Display Port 1 Attribute Data Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RW	0	**Active Video Height in Line**
15:0	RW	0	**Active Video Width in Pixel**

Offset Address: C663-C660h (DISPLAY PORT-MMIO)

Display Port 1 InfoFrame FIFO Control Register **Default Value: nnnn n0nnh**

Bit	Attribute	Default	Description
31:12	RW	-	**Reserved**
11:8	RW	0	**Info Frame Start Address**
7:2	RW	-	**Reserved**
1	RW	0	**Info Frame Read Fire** 1: Info Frame Read Fire Set to 0 when read data is ready
0	RW	0	**Info Frame Write Fire** 1: Info Frame Write Fire Set to 0 when info frame data has been written to FIFO.

Offset Address: C673-C670h (DISPLAY PORT-MMIO)

Display Port 1 Extension Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Extension Packet Payload Byte 3~0**

Offset Address: C677-C674h (DISPLAY PORT-MMIO)

Display Port 1 Extension Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Extension Packet Payload Byte 7~4**

Offset Address: C67B-C678h (DISPLAY PORT-MMIO)

Display Port 1 Extension Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Extension Packet Payload Byte 11~8**

Offset Address: C67F-C67Ch (DISPLAY PORT-MMIO)

Display Port 1 Extension Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Extension Packet Payload Byte 15~12**

Offset Address: C713-C710h (DISPLAY PORT-MMIO)

Display Port 1 AUX Write Data Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Software AUX Write Data Byte 3~0**

Offset Address: C717-C714h (DISPLAY PORT-MMIO)

Display Port 1 AUX Write Data Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Software AUX Write Data Byte 7~4**

Offset Address: C71B-C718h (DISPLAY PORT-MMIO)

Display Port 1 AUX Write Data Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Software AUX Write Data Byte 11~8**

Offset Address: C71F-C71Ch (DISPLAY PORT-MMIO)

Display Port 1 AUX Write Data Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Software AUX Write Data Byte 15~12**

Offset Address: C723-C720h (DISPLAY PORT-MMIO)

Display Port 1 AUX Read Data Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Software AUX Read Data Byte 3~0**

Offset Address: C727-C724h (DISPLAY PORT-MMIO)

Display Port 1 AUX Read Data Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Software AUX Read Data Byte 7~4**

Offset Address: C72B-C728h (DISPLAY PORT-MMIO)

Display Port 1 AUX Read Data Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Software AUX Read Data Byte 11~8**

Offset Address: C72F-C72Ch (DISPLAY PORT-MMIO)

Display Port 1 AUX Read Data Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Software AUX Read Data Byte 15~12**

Offset Address: C733-C730h (DISPLAY PORT-MMIO)

Display Port 1 General Control Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RO	00b	**Hot Plug Interrupt Status** 00: No interrupt 01: Hot plug 10: Hot Unplug 11: Hot IRQ
29:26	RO	0	**AUX Command**
25:6	RO	0	**Software Timer Counter**
5	RW	0	**Software Timer Enable** 0: Disable 1: Enable
4	RW	0	**Software Timer Clear**
3	RO	0	**Timeout Signal out from Aux_Source_Arbiter When Driver Uses AUX Channel** When timeout, HW will automatically set this bit. Software write 0 to clear this bit
2	RO	0	**Data Ready Signal out from Aux_Source_Arbiter When Driver Uses AUX Channel** When data ready, HW will automatically set this bit. Software write 0 to clear this bit.
1	RW	0	**Request Signal to Aux_Source_Arbiter When Driver Uses AUX Channel** Hardware clear this bit after the AUX command send.
0	RW	0	**The Enable Signal When Driver Needs to Use AUX Channel** 0: HW uses AUX channel 1: SW uses AUX channel, when finished must set to 0.

Offset Address: C737-C734h (DISPLAY PORT-MMIO)

Display Port 1 General Control Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RW	0	**Software AUX Address**
11:4	RW	0	**Software AUX Length**
3:0	RW	0	**Software AUX Command**

Offset Address: C73B-C738h (DISPLAY PORT-MMIO)

Display Port 1 AUX Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Link Training Software Reset**
30	RW	0	**AUX Software Reset** 0: Not reset AUX decoder, encoder, source_arbiter logic 1: Reset the AUX decoder, encoder, source_arbiter logic, need to set C614[6] after clearing this bit to 0.
29	RW	0	**Generate Audio M for SSC** The mode of generate MAUD in Asynchronous mode, suggest use mode 0. 0: 24bit 1: 15bit
28	RW	0	**Generate MAUD in Asynchronous Mode**
27	RW	0	**Mute Mode** 0: Reserved 1: Mute from register C738[26]
26	RW	0	**Reserved**
25	RW	0	**Audio Output Enable**
24	RW	0	**Reserved**
23:0	RW	0	**The NAUD in Audio Time Stamp Packet**

Offset Address: C73F-C73Ch (DISPLAY PORT-MMIO)

Display Port 1 General Control Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Secondary-data Packet ID**
23:0	RW	0	**The MAUD in Audio Time Stamp Packet**

Offset Address: C743-C740h (DISPLAY PORT-MMIO)

Display Port 1 EPHY Control Register **Default Value: 38C4 BEE8h**

Bit	Attribute	Default	Description
31:30	RW	00b	**TPLL N2, N3 and N4 Divider Settings** 00: 135MHz<=LP_REFCLKIN <= 270MHz 01: 67.5MHz<=LP_REFCLKIN<135MHz 10: 33.75MHz<=LP_REFCLKIN<67.5MHz 11: 25MHz<=LP_REFCLKIN <33.75MHz
29:27	RW	111b	**TPLL Charge Pump Current Setting** 000: 0uA 001: 6.9uA 010: 13.8uA 011: 20.6uA 100: 27.4uA 101: 34.3uA 110: 41.1uA 111: 48uA
26	RW	0	**TPLL Power Down** 0: Power down 1: Enable
25	RW	0	**TPLL Voltage Regulator Power Down** 0: Power down 1: Enable
24:23	RW	01b	**SSC Frequency Spread Magnitude Peak-to-Peak Control** 00: 0.25% 01: 0.5 10: 1% 11: 2%
22	RW	1b	**Modulating Signal Profile** 0:Symmetrical triangular 1: Asymmetric triangular
21	RW	0	**Dither Control** 0: Dither off 1: Dither enable
20	RW	0	**SSC Frequency Spread** 0: Down spread 1: Center spread
19	RW	0	**SSC Enable** 0: SSC off 1: SSC enable
18:17	RW	2h	**MPLL Output Divider P** 00: Divide by 4 (not used) 01: Divide by 8 for DP_HBR mode 1x: Divide by 16 for DP_RBR mode
16	RW	0	**MPLL Reference Divider R** 0: Divide by 2 (default) 1: Divide by 8
15:8	RW	BEh	**MPLL Main Divider N** Divider number N= M+2 Div 192 =>M=10111110 for DP_RBR mode Div 160 =>M=10011110 for DP_HBR mode
7:5	RW	111b	**MPLL CP Current Setting** 000: 0uA 001: 6.9uA 010: 13.8uA 011: 20.6uA 100: 27.4uA 101: 34.3uA 110: 41.1uA 111: 48uA
4:3	RW	01b	**MPLL PTAT Current Setting** 00: 12.5 uA 01: 25uA 10: 25uA 11: 37.5uA
2	RW	0	**MPLL Power Down** 0: Power down 1: Enable
1	RW	0	**MPLL Regulator Power Down** 0: Power down 1: Enable
0	RW	0	**Bandgap Power Down** 0 : Power down 1: Enable

Offset Address: C747-C744h (DISPLAY PORT-MMIO)

Display Port 1 EPHY Control Register **Default Value: FF00 0082h**

Bit	Attribute	Default	Description
31:30	RW	11b	**TX Power Control Mode – Lane 3** 00: All functions are on. 01: The driver is in idle mode; the PISO is off 10: The driver CMOP is on, the PISO and driver are off. 11: TX power down mode
29:28	RW	11b	**TX Power Control Mode – Lane 2** 00: All functions are on. 01: The driver is in idle mode; the PISO is off. 10: The driver CMOP is on, the PISO and driver are off. 11: TX power down mode
27:26	RW	11b	**TX Power Control Mode – Lane 1** 00: All functions are on. 01: The driver is in idle mode; the PISO is off. 10: The driver CMOP is on, the PISO and driver are off. 11: TX power down mode
25:24	RW	11b	**TX Power Control Mode – Lane 0** 00: All functions are on. 01: The driver is in idle mode; the PISO is off. 10: The driver CMOP is on, the PISO and driver are off. 11: TX power down mode
23:22	RW	00b	**Reserved**
21:20	RW	00b	**Reserved**
19:18	RW	00b	**Reserved**
17:16	RW	00b	**Reserved**
15	RW	0	**Driver On / Off Control – Lane 3** Current mirrors are on. This control signal is applied to Lane 3. 0: Driver idle 1: Driver awakened
14	RW	0	**Driver On / Off Control – Lane 2** Current mirrors are on. This control signal is applied to Lane 2. 0: Driver idle 1: Driver awakened
13	RW	0	**Driver On / Off Control – Lane 1** Current mirrors are on. This control signal is applied to Lane 1. 0: Driver idle 1: Driver awakened
12	RW	0	**Driver On / Off Control – Lane 0** Current mirrors are on. This control signal is applied to Lane 0. 0: Driver idle 1: Driver awakened
11	RW	0	**TX Driver Regulator Power Down – Lane 3** 0: Disable regulator 1: Enable regulator
10	RW	0	**TX Driver Regulator Power Down – Lane 2** 0: Disable regulator 1: Enable regulator
9	RW	0	**TX Driver Regulator Power Down – Lane 1** 0: Disable regulator 1: Enable regulator
8	RW	0	**TX Driver Regulator Power Down – Lane 0** 0: Disable regulator 1: Enable regulator
7:4	RW	1000b	**TX Resistance Value Settings** 0000: 73.5 0001: 69.4 0010: 65.8 0011: 62.5 0100: 59.5 0101: 56.8 0110: 54.3 0111: 52.1 1000: 50.0 1001: 48.1 1010: 46.3 1011: 44.6 1100: 43.1 1101: 41.7 1110: 40.3 1111: 39.1
3	RW	0	**TX Resistance Set Enable** 0: Hold the auto-calibrated result 1: Enable resistance
2	RW	0	**Resistance Tuning Enable** 1: Enable resistance auto calibration mode
1	RW	1	**Resistance Tuning Reset** 0: Reset
0	RW	0	**Resistance Tuning Power Down** 0: Power Down 1: Enable

Offset Address: C74B-C748h (DISPLAY PORT-MMIO)

Display Port 1 EPHY Control Register **Default Value: 0010 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**TX Resistance Output**
27:24	RO	0	**MPLL SSC Output**
23	RO	0	**MPLL Lock Indicator** 0: Unlock 1: Lock
22	RO	0	**TPLL Lock Indicator** 0: Unlock 1: Lock
21	RO	0	**TPLL Reset Signal**
20	RW	1b	**Hot-Plug Detect Power Down Control** 0: Power down 1: Enable
19	RW	0	**TX High Impedance – Lane 3** 0: N nominal 50Ohm 1: High impedance
18	RW	0	**TX High Impedance – Lane 2** 0: Nominal 50Ohm 1: High impedance
17	RW	0	**TX High Impedance – Lane 1** 0: Nominal 50Ohm 1: High impedance
16	RW	0	**TX High Impedance – Lane 0** 0: Nominal 50Ohm 1: High impedance
15:14	RW	00b	**Operation Mode for the AUX Channel** 00: AUX power off 01: The CMOP is on; the TX and RX are off (The timing relation of 00->01 pls refer EPHY spec.) 10: Operation mode is controlled by HW. When output, the driver is on, the RX is off. When input, the driver is idle (or off); the RX is on. 11: Reserved
13:9	RW	0	**Pre-emphasis Current Setting Overwrites Value** Tuning step is 0.25mA. 00000: Minimum 0mA 01111: Max 8mA
8:4	RW	0	**Driver Current Setting Overwrites Value** Tuning step is 0.5mA. 00000: Minimum 0mA 11111: Max 12.5mA
3:2	RW	00b	**Used for Analog Circuit Functionalities Verification** 00: BIST disable 01: BIST up 10: BIST down 11: BIST free running
1	RW	0	**Decide the Current Setting if They Can Be Overwritten** 0: Not overwrite 1: Overwrite current setting
0	RW	0	**Reserved** Must set to 1 for normal operation in DisplayPort mode

Offset Address: C74F-C74Ch (DISPLAY PORT-MMIO)

Display Port 1 EPHY Control Register **Default Value: nnnn nnn0h**

Bit	Attribute	Default	Description
31:6	RW	-	**Reserved**
5	RW	0	**Display Port 1 Interrupt Mode** 0: DP interrupt mode 1: Reserved
4:3	RW	0	**Pre-pp Setting for All Lanes** Works when C74C[0] is enabled.
2:1	RW	0	**Swing Level Setting for All Lanes** Works when C74C[0] is enabled.
0	RW	0	**Software Directly Control FIR Swing and Pre-pp** 0: Disable 1: Enable

Offset Address: C693-C690h (DISPLAY PORT-MMIO)

Display Port 2 Attribute Data Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RW	0	**Miscellaneous Main Stream Attribute Data** ***Bits[31:27]***: Reserved, set to 0 ***Bits[26:25]***: Stereo video attribute ***Bit 24***: Interlaced vertical total even
23:0	RW	0	**N Value for Stream Clock Recovery in Main Stream Attribute Data**

Offset Address: C697-C694h (DISPLAY PORT-MMIO)

Display Port 2 Link Training Control Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**DP2 Link Training Done** 0: Not done 1: Done. When SW start HW link training, need to polling this bit. If this bit is set 1b, will also read C6C0bit [29:28] to see if LT success or not. Software write 0 to clear this bit.
30	RW	0	**DP2 Clock Recovery Sequence Fail** 0: Not take action 1: SW set Link training fail. If AUX_CH read not all LANEX_CR_DONE bit is 1, then set this bit (refer 1.1 spec fig 2-36, when this bit set link training state transfer to not enabled state, SW need to do HW or SW link training.
29:28	RW	0	**Software Lane 3 Pre-emphasis**
27:26	RW	0	**Software Lane 3 Swing**
25:24	RW	0	**Software Lane 2 Pre-emphasis**
23:22	RW	0	**Software Lane 2 Swing**
21:20	RW	0	**Software Lane 1 Pre-emphasis**
19:18	RW	0	**Software Lane 1 Swing**
17:16	RW	0	**Software Lane 0 Pre-emphasis**
15:14	RW	0	**Software Lane 0 Swing**
13	RW	0	**Software Bit Rate** 0: 1.62G bit rate 1: 2.7G bit rate
12:11	RW	00b	**Software Link Training State** 00: Not enabled 01: Clcok recovery state 10: Channel EQ state 11: Normal state
10	RW	0	**Software Link Training Enable** 0: Disable 1: Enable
9:7	RW	000	**Number of Lane** 001: 1 Lane 010: 2 lanes 100: 4 lanes Other values are not allowed
6	RW	0	**SW hpd Asserted** Enable display port spec. V1.1 fig 2-32 AUX CH Source state change from S1 to S2.
5:4	RW	0	**MAX Pre-emphasis in HW Link Training Mode** Must be 10b or 11b.
3:2	RW	0	**MAX Voltage Swing in HW Link Training Mode** Must be 10b or 11b.
1	RW	0	**Start Link Rate** 0: 1.62G bit rate 1: 2.7G bit rate
0	RW	0	**Start Link Training** 0: Not start HW Link training 1: Start HW Link training. This bit should be cleared to 0 immediately after set to 1 by SW.

Offset Address: C69B-C698h (DISPLAY PORT-MMIO)

Display Port 2 General Controller Register **Default Value: n038 0000h**

Bit	Attribute	Default	Description
31	RW	-	**Reserved**
30	RW	0	**Video Input Selection** 0: HDTV0 1: HDTV1
29:24	RW	20h	**HDEN / VDEN / VSYN Delay Control** The min delay number is 0 stream clock period. The max delay number is 63 stream clock period.
23:18	RW	0Eh	**Ddefine the SYNC Data Pulse In AUX lphy's Manchester II Decoder**
17	RO	0	**Hardware Link Training AUX Fail** 0: Aux is ok 1: If HW Link training, AUX_READ or AUX_WR meet 7 consecutive not ACK reply (DEFFER or NACK or invalid reply) then set this bit, and hw link training failed , need driver to perform SW link training or other thing. Software write 0 to clear this bit.
16	RW	0	**Audio Stream Selection** Not decoded in DP module. 0: Audio Codec 1 1: Audio Codec 2
15:11	RO	0	**AUX Length**
10:2	RO	0	**IDLE Pattern Counter**
1	RW	0	**Switch Mode of IDLE Pattern to Video** 0: Audio Sample does not send immediately after C6C0[3]=1. 1: Audio Sample continues sending after C6C0[3]=1
0	RW	0	**Enable Main Link Lane Scrambler** 0: Disable main link lane's scrambler 1: Enable main link lane's scrambler

Offset Address: C69F-C69Ch (DISPLAY PORT-MMIO)

Display Port 2 Extension Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**DP Clock Selection** For debug only. 0: Select EPHY MPLL clock as DP clock 1: Select DCLK1 as DP clock
30	RW	0	**Horizontal Width Bit 11** Bits[10:0] are at C6C4[10:0].
29:24	RW	0	**Reserved**
23:0	RW	0	**Header of Extension Packet**

Offset Address: C6A3-C6A0h (DISPLAY PORT-MMIO)

Display Port 2 MMIO FIFO Register 0 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Display Port 2 MMIO FIFO 0**

Offset Address: C6A7-C6A4h (DISPLAY PORT-MMIO)

Display Port 2 MMIO FIFO Register 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Display Port 2 MMIO FIFO 1**

Offset Address: C6AB-C6A8h (DISPLAY PORT-MMIO)

Display Port 2 MMIO FIFO Register 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Display Port 2 MMIO FIFO 2**

Offset Address: C6AF-C6ACh (DISPLAY PORT-MMIO)

Display Port 2 MMIO FIFO Register 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Display Port 2 MMIO FIFO 3**

Offset Address: C6B3-C6B0h (DISPLAY PORT-MMIO)

Display Port 2 MMIO FIFO Register 4 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Display Port 2 MMIO FIFO 4**

Offset Address: C6B7-C6B4h (DISPLAY PORT-MMIO)

Display Port 2 MMIO FIFO Register 5 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Display Port 2 MMIO FIFO 5**

Offset Address: C6BB-C6B8h (DISPLAY PORT-MMIO)

Display Port 2 MMIO FIFO Register 6 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Display Port 2 MMIO FIFO 6**

Offset Address: C6BF-C6BCh (DISPLAY PORT-MMIO)

Display Port 2 MMIO FIFO Register 7 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Display Port 2 MMIO FIFO 7**

Offset Address: C6C3-C6C0h (DISPLAY PORT-MMIO)

Display Port 2 General Control Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RW	0	**Test Pattern Select Signal** 00: Link quality test pattern not transmitted 01: D10.2 test pattern transmitted 10: Symbol Error Rate measurement pattern transmitted 11: PRBS7 transmitted
29:28	RO	0	**Mainlink Status** 00: Main link disabled. 01: Clock recovery pattern transmitted. 10: Channel EQ pattern transmitted. 11: Normal operation
27:26	RW	0	**Reserved**
25	RW	0	**Generate MVID in Asynchronous Mode**
24	RW	0	**Enable Audio** 0: Disable 1: Enable
23	RW	0	**Enable Extension Packet** 0: Disable 1: Enable
22:19	RW	0	**InfoFrame FIFO 2 Length**
18:15	RW	0	**InfoFrame FIFO 1 Length**
14:11	RW	0	**InfoFrame FIFO 2 Start Address**
10:7	RW	0	**InfoFrame FIFO 1 Start Address**
6	RW	0	**InfoFrame FIFO Select** 0: Take InfoFrame Packet From FIFO 1 1: Take InfoFrame Packet From FIFO 2
5	RW	0	**InfoFrame FIFO 2 Ready**
4	RW	0	**InfoFrame FIFO 2 Ready**
3	RW	0	**Video Enable** 0: Idle Pattern transmitted 1: Video transmitted
2	RW	0	**Enhanced Framing Mode** 0: Default framing mode 1: Enhanced framing mode
1	RW	0	**Field Invert** 0: The FieldID_Flag in VBID is same as HDTV module output 1: The FieldID_Flag in VBID is the inverter of HDTV module output
0	RW	0	**Enable Display Port 2** 0: Disable DP2 1: Enable DP2

Offset Address: C6C7-C6C4h (DISPLAY PORT-MMIO)

Display Port 2 General Control Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:17	RW	0	**TU_Ratio**
16:11	RW	0	**DP Require TU Size** DP require TU size is 32~64. Programme this register to (TU size -1)
10:0	RW	0	**Horizontal Width** Horizontal width is 12 bit. The MSB is at C69C[30]. The value = (the number of horizontal active pixel/lane number) -1

Offset Address: C6CB-C6C8h (DISPLAY PORT-MMIO)

Display Port 2 General Control Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Extension Packet Valid Signal** Software writes 1 to this bit to indicate hardware to transmit extension packet. Hardware clear this bit after the extension packet sended.
30:27	RW	0	**Byte Number of Extensioin Packet**
26:15	RW	0	**Number of LS_CLK in Horizontal Blank** The value = (HBLANK_time * Link_symbol_clock_frequency) -15
14:0	RW	0	**Number of LS_CLK in One Line** The value = (Link_symbol_clock_frequency/horizontal_frequency) -15

Offset Address: C6CF-C6CCh (DISPLAY PORT-MMIO)

Display Port 2 Attribute Data Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RW	0	**Miscellaneous Main Stream Attribute Data** ***Bits[31:29]***: Bit depth per color/component ***Bit 28***: YCbCr Colorimetry 0: ITU-R BT601-5 1: ITU-R BT709-5 ***Bit 27***: Dynamic range 0: VESA range 1: CEA range ***Bits [26:25]***: Component format 00: RGB 01: YCbCr 4:2:2 10: YCbCr 4:4:4 ***Bit 24*** 0: Asynchronous Clock 1: Synchronous Clock
23:0	RW	0	**M for Stream Clock Recovery**

Offset Address: C6D3-C6D0h (DISPLAY PORT-MMIO)

Display Port 2 Attribute Data Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RW	0	**Vertical Totals of the Transmitted Main Video Stream in Line Counts**
15:0	RW	0	**Horizontal Totals of the Transmitted Main Video Stream in Pixel Counts**

Offset Address: C6D7-C6D4h (DISPLAY PORT-MMIO)

Display Port 2 Attribute Data Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RW	0	**Vertical Active Start from the Leading Edges of Vsync in Line**
15:0	RW	0	**Horizontal Active Start from the Leading Edges of Hsync in Pixel**

Offset Address: C6DB-C6D8h (DISPLAY PORT-MMIO)

Display Port 2 Attribute Data Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RW	0	**Vsync Polarity / Vsync Width in Line**
15:0	RW	0	**Hsync Polarity / Hsync Width in Pixel**

Offset Address: C6DF-C6DCh (DISPLAY PORT-MMIO)

Display Port 2 Attribute Data Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RW	0	**Active Video Height in Line**
15:0	RW	0	**Active Video Width in Pixel**

Offset Address: C6E3-C6E0h (DISPLAY PORT-MMIO)

Display Port 2 InfoFrame FIFO Control Register **Default Value: nnnn n0nnh**

Bit	Attribute	Default	Description
31:12	RW	-	**Reserved**
11:8	RW	0	**Infor Frame Start Address**
7:2	RW	-	**Reserved**
1	RW	0	**Info Frame Read Fire** 1: Info frame read fire Set to 0 when read data is ready.
0	RW	0	**Info Frame Write Fire** 1: Info frame write fire Set to 0 when info frame data has been written to FIFO.

Offset Address: C6F3-C6F0h (DISPLAY PORT-MMIO)

Display Port 2 Extension Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Extension Packet Payload Byte 3~0**

Offset Address: C6F7-C6F4h (DISPLAY PORT-MMIO)

Display Port 2 Extension Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Extension Packet Payload Byte 7~4**

Offset Address: C6FB-C6F8h (DISPLAY PORT-MMIO)

Display Port 2 Extension Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Extension Packet Payload Byte 11~8**

Offset Address: C6FF-C6FCh (DISPLAY PORT-MMIO)

Display Port 2 Extension Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Extension Packet Payload Byte 15~12**

Offset Address: C793-C790h (DISPLAY PORT-MMIO)

Display Port 2 AUX Write Data Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Software AUX Write Data Byte 3~0**

Offset Address: C797-C794h (DISPLAY PORT-MMIO)

Display Port 2 AUX Write Data Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Software AUX Write Data Byte 7~4**

Offset Address: C79B-C798h (DISPLAY PORT-MMIO)

Display Port 2 AUX Write Data Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Software AUX Write Data Byte 11~8**

Offset Address: C79F-C79Ch (DISPLAY PORT-MMIO)

Display Port 2 AUX Write Data Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Software AUX Write Data Byte 15~12**

Offset Address: C7A3-C7A0h (DISPLAY PORT-MMIO)

Display Port 2 AUX Read Data Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Software AUX Read Data Byte 3~0**

Offset Address: C7A7-C7A4h (DISPLAY PORT-MMIO)

Display Port 2 AUX Read Data Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Software AUX Read Data Byte 7~4**

Offset Address: C7AB-C7A8h (DISPLAY PORT-MMIO)

Display Port 2 AUX Read Data Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Software AUX Read Data Byte 11~8**

Offset Address: C7AF-C7ACh (DISPLAY PORT-MMIO)

Display Port 2 AUX Read Data Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Software AUX Read Data Byte 15~12**

Offset Address: C7B3-C7B0h (DISPLAY PORT-MMIO)

Display Port 2 General Control Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RO	00b	**DP2 Hot Plug Detect Interrupt Status** 00: No interrupt 01: Hot Plug 10: Hot Unplug 11: Hot IRQ
29:26	RO	0	**AUX Command**
25:6	RO	0	**Software Timer Counter**
5	RW	0	**Software Timer Enable** 0: Disable 1: Enable
4	RW	0	**Software Timer Clear**
3	RO	0	**Timeout Signal out from Aux_Source_Arbiter When Driver Uses AUX Channel** When timeout, HW will automatically set this bit. Software write 0 to clear this bit.
2	RO	0	**Data Ready Signal out from Aux_Source_Arbiter When Driver Uses AUX Channel** When data ready, HW will automatically set this bit. Software write 0 to clear this bit.
1	RW	0	**Request Signal to Aux_Source_Arbiter When Driver Uses AUX Channel** Hardware clear this bit after the AUX command send.
0	RW	0	**The Enable Signal When Driver Needs to Use AUX Channel** 0: HW use AUX channel 1: SW use AUX channel, when finished must set to 0

Offset Address: C7B7-C7B4h (DISPLAY PORT-MMIO)

Display Port 2 General Control Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RW	0	**Software AUX Address**
11:4	RW	0	**Software AUX Length**
3:0	RW	0	**Software AUX Command**

Offset Address: C7BB-C7B8h (DISPLAY PORT-MMIO)

Display Port 2 AUX Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Link Training Software Reset**
30	RW	0	**AUX Software Reset** 0: Not reset AUX decoder, encoder, source_arbiter logic 1: Reset the AUX decoder, encoder, source_arbiter logic, need to set C614[6] after clear this bit to 0.
29	RW	0	**R_DP2_MODE** The mode of generate MAUD in Asynchronous mode, suggest use mode 0.
28	RW	0	**Generate MAUD in Asynchronous Mode**
27	RW	0	**Mute Mode** 0: Reserved 1: Mute from register C738[26]
26	RW	0	**MUTE**
25	RW	0	**Audio Output Enable**
24	RW	0	**Reserved**
23:0	RW	0	**The NAUD in Audio Time Stamp Packet**

Offset Address: C7BF-C7BCh (DISPLAY PORT-MMIO)

Display Port 2 General Control Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Secondary-data Packet ID**
23:0	RW	0	**The MAUD in Audio Time Stamp Packet**

Offset Address: C7C3-C7C0h (DISPLAY PORT-MMIO)

Display Port 2 EPHY Control Register **Default Value: n380 AAnnh**

Bit	Attribute	Default	Description
31:28	RW	-	**Reserved**
27	RW	0	**Low Priority SSC Enable** It works only when C7CF[1] is disabled. 0: SSC off 1: SSC enable
26:24	RW	3h	**TPLL Charge Pump Current Setting** The signal comes from the setting register. 000: 0A 001: 6.9uA 010: 13.8uA 011: 20.6uA 100: 27.4uA 101: 34.3uA 110: 41.1uA 111: 48.0uA
23:20	RW	8h	**TX Resistance Set Value** 0000: 73.5 0001: 69.4 0010: 65.8 0011: 62.5 0100: 59.5 0101: 56.8 0110: 54.3 0111: 52.1 1000: 50.0 1001: 48.1 1010: 46.3 1011: 44.6 1100: 43.1 1101: 41.7 1110: 40.3
19	RW	0	**TX Power Status Set Enable -- Lane 3** 0: Disable 1: Enable
18	RW	0	**TX Power Status Set Enable -- Lane 2** 0: Disable 1: Enable
17	RW	0	**TX Power Status Set Enable -- Lane 1** 0: Disable 1: Enable
16	RW	0	**TX Power Status Set Enable -- Lane 0** 0: Disable 1: Enable
15:14	RW	2h	**TX Power Status Set -- Lane 3**
13:12	RW	2h	**TX Power Status Set -- Lane 2**
11:10	RW	2h	**TX Power Status Set -- Lane 1**
9:8	RW	2h	**TX Power Status Set -- Lane 0**
7:0	RW	-	**Reserved**

Offset Address: C7C7-C7C4h (DISPLAY PORT-MMIO)

Display Port 2 EPHY Control Register **Default Value: nn00 2402h**

Bit	Attribute	Default	Description
31:30	RW	0	**Used for Analog Circuit Functionalities Verification** The purpose of this register is to verify analog circuit functionalities. The signal comes from the setting register. 00: BIST disable 01: BIST down 10: BIST up 11: BIST free running
29:25	RW	-	**Reserved**
24:20	RW	0	**DP Pre-emphasis Current Settings Overwrite Value** The signal comes from the setting register. 00000: Minimum 0mA 01111: Mx 7mA Tuning step: 0.25mA
19	RW	0	**TX Electrical Idle Control -- Lane 3** 0: Electrical idle 1: Transmit data
18	RW	0	**TX Electrical Idle Control -- Lane 2** 0: Electrical idle 1: Transmit data
17	RW	0	**TX Electrical Idle Control -- Lane 1** 0: Electrical idle 1: Transmit data
16	RW	0	**TX Electrical Idle Control -- Lane 0** 0: Electrical idle 1: Transmit data
15	RW	0	**TX Resistance Set Enable** 0: Hold the auto-calibrated result 1: Enable resistance overwrite manually mode
14	RW	0	**TX Margining, Swing and De-emphasis Manual Set Enable**
13:11	RW	4h	**MPLL1 CP Current Setting** The signal comes from the setting register. 000: 0uA 001: 5uA 010: 10uA 011: 15uA 100: 20uA 101: 25uA 110: 30uA 111: 35uA
10:8	RW	4h	**SSCGPLL CP Current Setting** The signal comes from the setting register. 000: 0uA 001: 5uA 010: 10uA 011: 15uA 100: 20uA 101: 25uA 110: 30uA 111: 35uA
7:6	RW	0	**Near-end TX Swing and De-emphasis Manual Set**
5:4	RW	0	**Far-end TX Swing and De-emphasis Manual Set**
3	RW	0	**SSC Frequency Spread** 0: Down spread 1: Center spread
2	RW	0	**Dither Control** 0: Dither off 1: Dither enable
1	RW	1b	**Modulating Signal Profile** 0: Symmetrical triangular 1: Asymmetric triangular
0	RW	0	**AUX Manual Set Enable** 0: Disable 1: Enable

Offset Address: C7CB-C7C8h (DISPLAY PORT-MMIO)

Display Port 2 EPHY Control Register **Default Value: 4000 0000h**

Bit	Attribute	Default	Description
31:30	RW	01b	**SSC Frequency Spread Magnitude Peak-to-Peak Control** 00: 0.25% 01: 0.5% 10: 1% 11: 2%
29:28	RW	0	**Operation Mode for the AUX Channel** 00: AUX power off 01: The CMOP is on; the TX and RX are off 10: The driver is idle (or off); the RX is on 11: The driver is on; the RX is off
27:25	RW	0	**DP TX Level Select** Set according to lane 0 swing level and pre_emphasis level. It work when bit 24 is enabled and C74C bit 2 is 1. ***Level 1: (Vp-p=400mV)*** 000: 0dB 001: 3.5dB 010: 6dB ***Level 2: (Vp-p=600mV)*** 011: 0dB 100: 3.5dB 101: 6dB ***Level 3: (Vp-p=800mV)*** 110: 0dBL 111:3.5dB
24	RW	0	**TX Swing and Pre-emphasis Manual Set Enable** 0: Disable 1: Enable
23	RW	0	**Speed Manual Set Enable -- Lane 3** 0: Disable 1: Enable
22	RW	0	**Speed Manual Set Enable -- Lane 2** 0: Disable 1: Enable
21	RW	0	**Speed Manual Set Enable -- Lane 1** 0: Disable 1: Enable
20	RW	0	**Speed Manual Set Enable -- Lane 0** 0: Disable 1: Enable
19	RW	0	**Speed Manual Set -- Lane 3**
18	RW	0	**Speed Manual Set -- Lane 2**
17	RW	0	**Speed manual set -- Lane 1**
16	RW	0	**Speed Manual Set -- Lane 0**
15:14	RW	00b	**DP Port Tx Output Peak-to-Peak Voltage Swing Setting for DP Port - Lane 3** 00: 400mVdiff-pp 01: 600mVdiff-pp 10: 800mVdiff-pp 11: 1200mVdiff-pp (reserved)
13:12	RW	00b	**DP Port Tx Output Peak-to-Peak Voltage Swing Setting for DP Port - Lane 2** 00: 400mVdiff-pp 01: 600mVdiff-pp 10: 800mVdiff-pp 11: 1200mVdiff-pp (reserved)
11:10	RW	00b	**DP Port Tx Output Peak-to-Peak Voltage Swing Setting for DP Port - Lane 1** 00: 400mVdiff-pp 01: 600mVdiff-pp 10: 800mVdiff-pp 11: 1200mVdiff-pp (reserved)
9:8	RW	00b	**DP Port Tx Output Peak-to-Peak Voltage Swing Setting for DP Port - Lane 0** 00: 400mVdiff-pp 01: 600mVdiff-pp 10: 800mVdiff-pp 11: 1200mVdiff-pp (reserved)
7:6	RW	00b	**TX Power Control Mode for DP Lanes** 00: All functions are on. 01: The driver is in idle mode; the PISO is off. 10: The driver CMOP is on; the PISO and driver are off. 11: TX power down mode
5:4	RW	00b	**TX PowerControl Mode for DP Lanes** 00: All functions are on. 01: The driver is in idle mode; the PISO is off. 10: The driver CMOP is on; the PISO and driver are off. 11: TX power down mode
3:2	RW	00b	**TX Power Control Mode for DP Lanes** 00: All functions are on. 01: The driver is in idle mode; the PISO is off. 10: The driver CMOP is on; the PISO and driver are off. 11: TX power down mode

1:0	RW	00b	**TX Power Control Mode for DP Lanes** 00: All functions are on. 01: The driver is in idle mode; the PISO is off. 10: The driver CMOP is on; the PISO and driver are off. 11: TX power down mode

Offset Address: C7CF-C7CCh (DISPLAY PORT-MMIO)

Display Port 2 EPHY Control Register **Default Value: 0102 BEnnh**

Bit	Attribute	Default	Description
31	RW	0	**Driver On / Off Control – Lane 3** Current mirrors are on. This control signal is applied to Lane 3. 0: Driver idle 1: Driver awakened
30	RW	0	**Driver On / Off Control – Lane 2** Current mirrors are on. This control signal is applied to Lane 2. 0: Driver idle 1: Driver awakened
29	RW	0	**Driver On / Off Control – Lane 1** Current mirrors are on. This control signal is applied to Lane 1. 0: Driver idle 1: Driver awakened
28	RW	0	**Driver On / Off Control – Lane 0** Current mirrors are on. This control signal is applied to Lane 0. 0: Driver idle 1: Driver awakened
27:26	RW	00b	**MPLL1 Current Setting** 00: 12.5uA 01/10: 25uA 11: 37.5uA
25	RW	0	**Disable SSC/MPLL/TPLL** 0: Enable SSC/MPLL/TPLL 1: Disable SSC/MPLL/TPLL
24	RW	1b	**DP Operation Mode** 0: TEST mode 1: Normal function mode
23	RO	0	**PCIe-DP EPHY Work Mode** 0: PCIe mode 1: DP mode
22:20	RW	0	**Near-end TX Manual Set**
19:18	RW	00b	**Operation Mode for the AUX Channel** 00: AUX power off 01: The CMOP is on; the TX and RX are off. 10: Operation mode is controlled by HW. When output, the driver is on, the RX is off ; when input, the driver is idle (or off); the RX is on. 11: Reserved
17:16	RW	10b	**MPLL Output Divider P** 00: Divide by 4 (not used) 01: Divide by 8 for DP_HBR mode 1x: Divide by 16 for DP_RBR mode
15:8	RW	BEh	**MPLL Main Divider N** Divider number N= M+2 Div 192 =>M=10111110 for DP_RBR mode Div 160 =>M=10011110 for DP_HBR mode
7:5	RW	0	**Speed Manual Set Enable of Lane 0** 0: Disable 1: Enable
4:2	RW	-	**Reserved**
1	RW	0	**Force to Turn on All Functions in Master Block When EPHY Testing** 0: Normal mode 1: Test mode enable
0	RW	1	**Hot-plug Detect Power-down Control** 0: Power down 1: Enable

Offset Address: C7D3-C7D0h (DISPLAY PORT-MMIO)

Display Port 2 EPHY Read Back Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**MPLL Lock Indicator** 0: Unlock 1: Lock
30:27	RO	0	**TX Resistance Output**
26	RO	0	**Driver On / Off Control from Link Training – Lane 0** Current mirrors are on. This control signal is applied to Lane 0. 0: Driver idle 1: Driver awakened
25	RO	0	**Driver On / Off Control from Link Training – Lane 1** Current mirrors are on. This control signal is applied to Lane 1. 0: Driver idle 1: Driver awakened
24	RO	0	**Driver On / Off Control from Link Training – Lane 2** Current mirrors are on. This control signal is applied to Lane 2. 0: Driver idle 1: Driver awakened
23	RO	0	**Driver On / Off Control from Link Training – Lane 3** Current mirrors are on. This control signal is applied to Lane 3. 0: Driver idle 1: Driver awakened
22	RO	0	**TX High Impedance – Lane 0** 0: N nominal 50Ohm 1: High impedance
21	RO	0	**TX High Impedance – Lane 1** 0: N nominal 50Ohm 1: High impedance
20	RO	0	**TX High Impedance – Lane 2** 0: N nominal 50Ohm 1: High impedance
19	RO	0	**TX High Impedance – Lane 3** 0: N nominal 50Ohm 1: High impedance
18	RO	0	**Read from Register C694[1] Start Link Rate – Lane 0** 0: 1.62G bit rate 1: 2.7G bit rate
17	RO	0	**Read from Register C694[1] Start Link Rate – Lane 1** 0: 1.62G bit rate 1: 2.7G bit rate
16	RO	0	**Read from Register C694[1] Start Link Rate – Lane 2** 0: 1.62G bit rate 1: 2.7G bit rate
15	RO	0	**Read from Register C694[1] Start Link Rate – Lane 3** 0: 1.62G bit rate 1: 2.7G bit rate
14:12	RO	0	**Near-end TX Manual Set – Lane 0** All set to 000.
11:9	RO	0	**Near-end TX Manual Set – Lane 1** All set to 000.
8:6	RO	0	**Near-end TX Manual Set – Lane 2** All set to 000.
5:3	RO	0	**Near-end TX Manual Set – Lane 3** All set to 000.
2:1	RO	00b	**Read back the Operation Mode for the AUX Channel** 00: AUX power off 01: The CMOP is on; the TX and RX are off. 10: Operation mode is controlled by HW. When output, the driver is on, the RX is off. When input, the driver is idle (or off); the RX is on. 11: Reserved
0	RO	0	**Hot Plug Detected Active Signal from EPHY**

Offset Address: C7D7-C7D4h (DISPLAY PORT-MMIO)

Display Port 2 EPHY Read Back Register **Default Value: nnnn 0000h**

Bit	Attribute	Default	Description
31:18	RO	-	**Reserved**
17	RO	0	**Bandgap Power Down** 0: Power down 1: Enable
16	RO	0	**DP2 MPLL Reference Clock Power Down** 0: Power down 1: Enable
15	RO	0	**DP2 MPLL Power Down** 0: Power down 1: Enable
14	RO	0	**DP2 TPLL Power Down** 0: Power down 1: Enable
13	RO	0	**DP2 SSC Power Down** 0: Power down 1: Enable
12	RO	0	**SSC Enable** 0: SSC off 1: SSC enable
11	RO	0	**SSC Clock Select** It is determined by DP operation mode.
10	RO	0	**Resistance Tuning Power Down** 0: Power Down 1: Enable
9	RO	0	**Resistance Tuning Reset** 0: Reset
8	RO	0	**Enable Resistance Tuning** 1: Enable resistance auto calibration mode
7:6	RO	0	**TX Power Control Mode – Lane 0** 00: All functions are on. 01: The driver is in idle mode; the PISO is off. 10: The driver CMOP is on, the PISO and driver are off. 11: TX power down mode
5:4	RO	0	**TX Power Control Mode – Lane 1** 00: All functions are on. 01: The driver is in idle mode; the PISO is off. 10: The driver CMOP is on, the PISO and driver are off. 11: TX power down mode
3:2	RO	0	**TX Power Control Mode – Lane 2** 00: All functions are on. 01: The driver is in idle mode; the PISO is off. 10: The driver CMOP is on, the PISO and driver are off. 11: TX power down mode
1:0	RO	0	**TX Power Control Mode – Lane 3** 00: All functions are on. 01: The driver is in idle mode; the PISO is off. 10: The driver CMOP is on, the PISO and driver are off. 11: TX power down mode