OML Sync Control

- What is it
- How can it be tested
- How is it implemented
- What can we do about that?
What is it?

- OML: OpenML
- Like EXT Swap Control, but better
- Can schedule buffer swaps and get feedback
- Use case: Neuroscience
UST, MSC, and SBC

UST: Common time base
MSC: Number of vsyncs
SBC: Number of buffer swaps
Functions

- glXGetSyncValuesOML
- glXGetMscRateOML
- glXSwapBuffersMscOML(target, div, rem)
- glXWaitForMscOML(target, div, rem)
- glXWaitForSbcOML(target)
Things you will get wrong

- Divisor 0
- INT64 wrap
- Returning 0 values
- GetSyncValues scheduling
- Externally meaningless values
- Timestamps from the future!
Assertions to test

SBC starts at 0
Counters don’t go backwards after glxWaitFor*
SwapBuffers schedules correct SBC
Requested target MSC/SBC was hit
Divisor and remainder respected
Spurious SBC increments
Statistics

Suspicious:
\[ \text{stddev} \left( \frac{\Delta \text{UST}}{\Delta \text{MSC}} \right) > 100 \text{UST?} \]

Broken:
\[ \text{stddev} \left( \frac{\Delta t}{\Delta \text{MSC}} \right) > 1 \text{ms?} \]

\[ | \text{avg} \left( \frac{\Delta t}{\Delta \text{MSC}} \right) - 1 \text{s} / \text{GetMSCRate} | > 50 \text{us?} \]
if (__builtin_constant_p(frame) || (__builtin_constant_p(tv_sec) && __builtin_constant_p(tv_usec))) {
    static int _already_warned;
    if (!_already_warned) {
        _already_warned = 1;
        _DRI2WarnConstantUSTOrMSC(__FILE__, __LINE__, __func__, pDraw, frame, tv_sec, tv_usec);
    }
}
intel_dri.c: In function 'I830DRI2ScheduleFlip':
intel_dri.c:956:273: warning: call to '_DRI2WarnConstantUSTOrMSC' declared with attribute warning: 
UST and MSC can't be constants. Please fix this driver's DRI2 support for OML_sync_control.
intel_dri.c: In function 'I830DRI2ScheduleWaitMSC':
intel_dri.c:1554:282: warning: call to '_DRI2WarnConstantUSTOrMSC' declared with attribute warning: 
UST and MSC can't be constants. Please fix this driver's DRI2 support for OML_sync_control.
intel_dri.c: In function 'I830DRI2ScheduleSwap':
intel_dri.c:1369:273: warning: call to '_DRI2WarnConstantUSTOrMSC' declared with attribute warning: 
UST and MSC can't be constants. Please fix this driver's DRI2 support for OML_sync_control.
Performance in the wild

Until xf86-video-intel commit 2.99.912~134:

sna_dri2.c: In function 'sna_dri2_schedule_wait_msc':

sna_dri2.c:2478:282: warning: call to '_DRI2WarnConstantUSTOrMSC' declared with attribute warning: UST and MSC can't be constants. Please fix this driver's DRI2 support for OML_sync_control.

sna_dri2.c: In function 'sna_dri2_immediate_blit':

sna_dri2.c:1548:277: warning: call to '_DRI2WarnConstantUSTOrMSC' declared with attribute warning: UST and MSC can't be constants. Please fix this driver's DRI2 support for OML_sync_control.

sna_dri2.c:1564:275: warning: call to '_DRI2WarnConstantUSTOrMSC' declared with attribute warning: UST and MSC can't be constants. Please fix this driver's DRI2 support for OML_sync_control.

sna_dri2.c: In function 'chain_flip':

sna_dri2.c:1731:281: warning: call to '_DRI2WarnConstantUSTOrMSC' declared with attribute warning: UST and MSC can't be constants. Please fix this driver's DRI2 support for OML_sync_control.

In function 'sna_dri2_schedule_flip',

   inlined from 'sna_dri2_schedule_swap' at sna_dri2.c:2214:6:

sna_dri2.c:2034:276: warning: call to '_DRI2WarnConstantUSTOrMSC' declared with attribute warning: UST and MSC can't be constants. Please fix this driver's DRI2 support for OML_sync_control.

sna_dri2.c: In function 'sna_dri2_schedule_swap':

sna_dri2.c:2324:273: warning: call to '_DRI2WarnConstantUSTOrMSC' declared with attribute warning: UST and MSC can't be constants. Please fix this driver's DRI2 support for OML_sync_control.
Piglit results
Where to go from here?

Driver patches

Glamor-EGL? video-modesetting?
Questions, Discussion?

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