## **Framebuffer Modifiers**

### Supporting end-to-end graphics compression

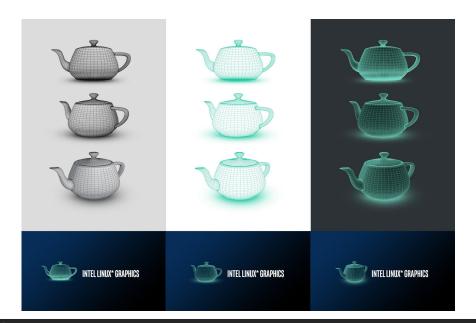
#### **Ben Widawsky**





#### About Me

- Worked on all parts of graphics and other driver stacks
- Avid Buffer Modifier
- Motivated by disparity with closed implementations
  - If they can do it; damn it, we can too.







#### Summarizing the Work

	Linux DRM <ul> <li>blobifier</li> <li>AddFB2</li> <li>multi-plane</li> </ul>	Linux i915 • blobifier • AddFB2	Mesa DRI EGL ANV RADV other	Protocol • DRI3.1 o X.org o xcb • Wayland o Mutter o Weston	<pre>Khronos     image_dma_buf_import_mod     ifiers     VK_EXT_external_*</pre>
Intel	~	~	~	~	<b>v</b>
Collabora	V	~	V	V	<i>v</i>
Google	V		~		<i>v</i>
Others	V		V	V	





#### Status

- Many years in the making: almost there!
- Early modifier support already released: Mesa 17.2, Kernel 4.14
- Full compression support soon:
  - Modesetting
  - Wayland/Mutter?
  - X.org/DRI3
    - Mesa DRI3 support
    - Mesa Wayland support





#### Mountains out of Molehills?

- Each EU needs 1GB/s bandwidth
  - Texturing (trilinear, anisotropic) 0
  - Transparency/Blending 0
  - Antialiasing 0
- Display
  - 3840 px \* 2160 rows \* 4 Bpp \* 60 Hz = 1.85GB/s
  - It keeps getting worse 0
    - Increasing resolutions (5K, 8K)
    - Increasing refresh rates (120Hz, 240 Hz)
- Workloads are already memory bandwidth limited
  - Can't scale up compute without more bandwidth 0
  - Reduce visual effects  $\bigcirc$
  - Decrease resolution Ο

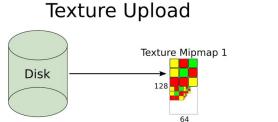


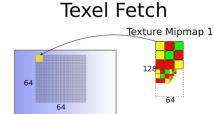
Salt

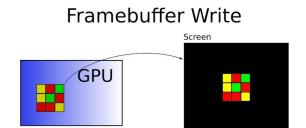


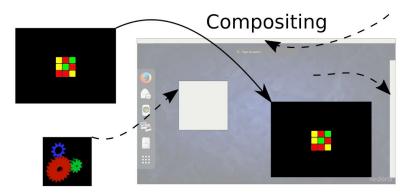


#### Admiring the Problem

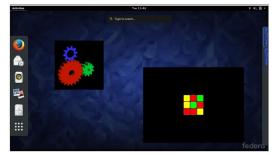








#### **Display Scanout**

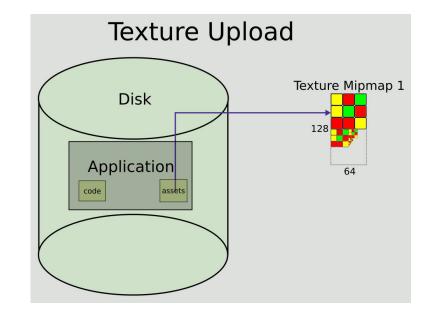






#### **Texture Upload**

The application needs to get its assets (geometry data, texture data, precompiled shaders, etc.) into memory from storage.

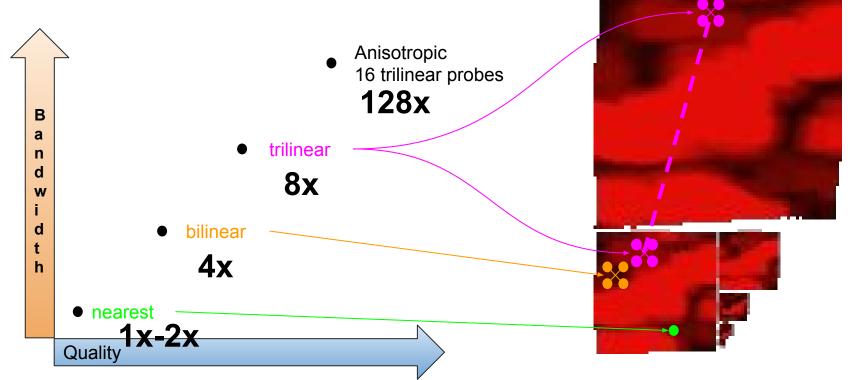






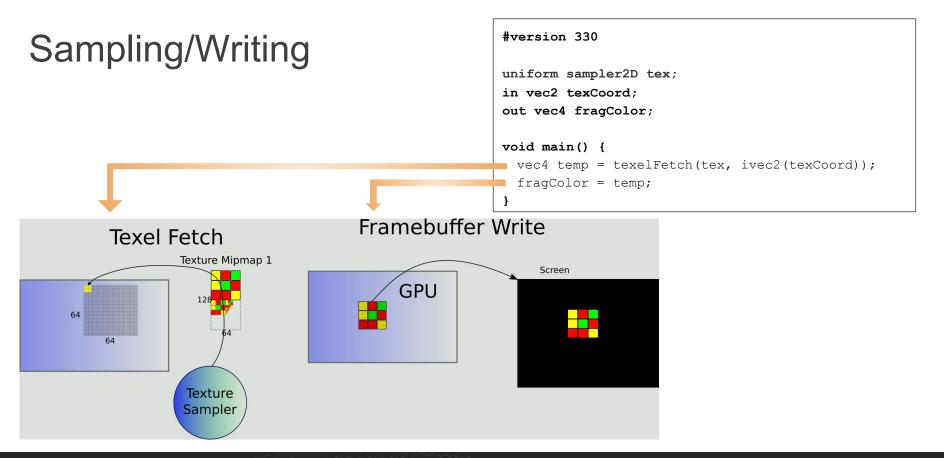
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#### **Texturing Fetch/Filtering**











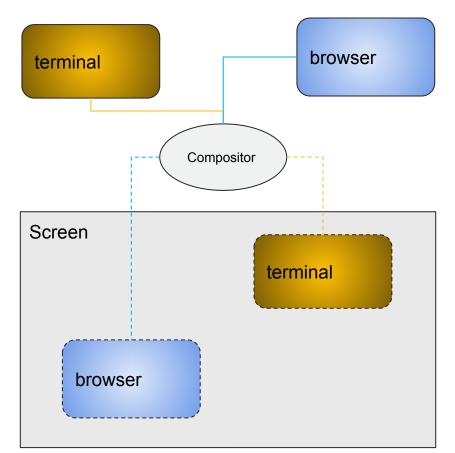


### Compositing

Compositor is responsible for taking client application's window contents and amalgamates into a single image for display.

Like a window manager, but with offscreen buffers

• Needs to read from application's rendered data, and write to the screen

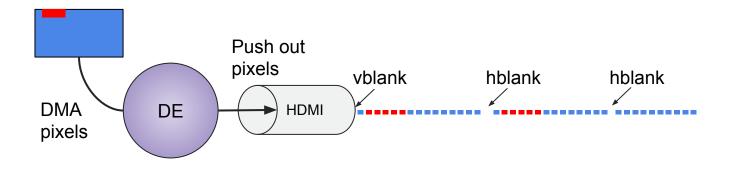






### **Display Engine**

Specialized, fixed function hardware which sources pixel data and pushes it out over some display protocol; possibly blending, and scaling the pixels along the way.







# Bandwidth Costs Bytes Per

Bytes Per Component

Operation	Color Depth	Desc.	Bandwidth	R/W
Texture Upload	1Bpc (RGBX8)	File to DRAM	16KB (64 * 64 * 4)	W
Texel Fetch	1Bpc (RGBX8)	DRAM to Sampler	16KB (64 * 64 * 4)	R
FB Write	1Bpc (RGBX8)	GPU to DRAM	16KB (64 * 64 * 4)	W
Compositing	1Bpc (RGBX8)	DRAM to DRAM	32KB (64 * 64 * 4 * 2)	R+W
Display Scanout	1Bpc (RGBX8)	DRAM to PHY	16KB (64 * 64 * 4)	R





#### At Least it Looks Better

Filter Mode	Multiplier (texel fetch stage)	Total Bandwidth
Nearest	1x	5.625 MB/s
Bilinear	4x	11.25 MB/s
Trilinear	8x	18.75 MB/s
Aniso 4x	32x	63.75 MB/s*
Aniso 16x	128x	<b>243.75</b> MB/s*

\* Oblique angle + implementation details would reduce further





#### **Proposed Solution: Increase Headroom**

Color Depth	Operation	Bandwidth		
1Врс	Texture Upload	16KB (64 * 64 * 4)		
1Врс	Texel Fetch	16KB (64 * 64 * 4)		
1Врс	FB Write	16KB (64 * 64 * 4)		
1Врс	Composite	32KB (64 * 64 * 4 * 2)		
1Врс	Scanout	16KB (64 * 64 * 4)		
Total Bandwidth = 5.625 MB/s				

Technology (~2013)	Technology (~2016)	Improvement
DDR3-2133 34GB/s (dual channel)	DDR4-3200 51.2 GB/s (dual channel)	50%
GTX 780 (Kepler) GDDR5 288 GB/s	GTX1080 (Pascal) GDDR5X 352 GB/s	22%
Radeon R9 290X (Hawaii) GDDR5 (320GB/s)	Radeon R9 Fury⁻(Fiji) HBM1 512GB/s	60%
LPDDR3-1600 12.8 GB/s (single channel)	LPDDR4-3200 25.6 GB/s (single channel)	100%

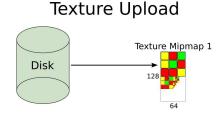




#### **Proposed Solution: Hardware Composition**

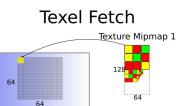
Hardware is capable of having multiple hardware planes. Use them.

Color Depth	Operation	Bandwidth		
1Bpc (RGBA8)	Texture Upload	16KB (64 * 64 * 4)		
1Bpc (RGBA8)	Texel Fetch	16KB (64 * 64 * 4)		
1Bpc (RGBA8)	FB Write	16KB (64 * 64 * 4)		
1Bpc (RGBA8)	Composite	<del>32KB (64 * 64 * 4 * 2)</del>		
1Bpc (RGBA8) Scanout		16KB (64 * 64 * 4)		
Total Bandwidth = 3.75 MB/s (33% savings)				

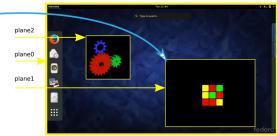


Framebuffer Write

GPU



#### **Display Scanout**



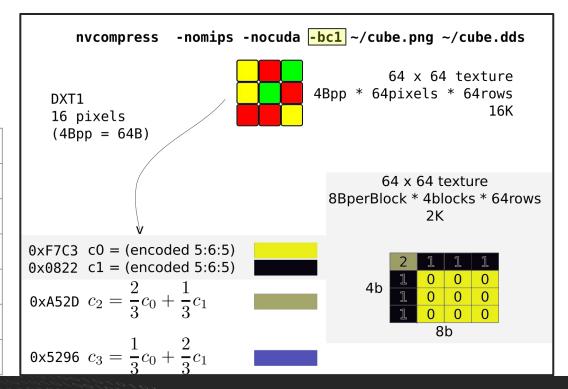




#### Proposed Solution: Texture Compression

- DXT1 (8:1)
- ETC1/2 (4:1)
- ASTC (variable, 6:1)

Color Depth	Operation	Bandwidth		
DXT1	Texture Upload	16KB / 8		
DXT1	Texel Fetch	<mark>16KB /8</mark>		
1Врс	FB Write	16KB (64 * 64 * 4)		
1Врс	Composite	32KB (64 * 64 * 4 * 2)		
1Врс	Scanout	16KB (64 * 64 * 4)		
Total Bandwidth = 3.925 MB/s (30%)				





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#### Problems (Increase Bandwidth)

- 1. Limited by process and design
- 2. Costly for manufacturing
  - a. New memory modules

Rating: Sure. Won't hold my breath

- b. New boards
- c. Utilizes new fabrication process
- 3. May be power hungry







#### Problems (More Planes)



- 1. Hardware specific
  - a. Not all hardware can composite the same number of planes
- 2. Max planes is small
  - a. Increasing this significantly isn't feasible (die size)
- 3. Only helps compositing step

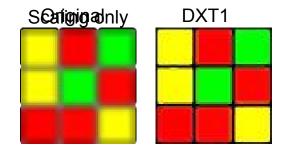
Rating: Great, doesn't scale





#### Problems (Texture Compression)

- 1. May be lossy
- 2. Hardware compatibility
  - a. Better formats require new hardware
  - b. Increased gate counts
- 3. Patents or proprietary
- 4. Misses display improvement
- 5. Doesn't play nicely with all filtering methods (aniso)



Rating: Great, but lacking





### Introducing E2E Lossless Compression

- Supplement other bandwidth saving techniques
  - Doesn't reduce size (in fact internally things get larger).
- Internal hardware blocks compress/decompress on the fly.
  - Display
  - Media
  - Texture units

#### <u>Pros</u>

- Lossless
- Transparent to applications/tools
  - Easier development
  - Hardware improvements automatically help
- No offline compression necessary
- Compression benefits through display
- Can be huge when texturing is small amount of bandwidth consumption

#### <u>Cons</u>

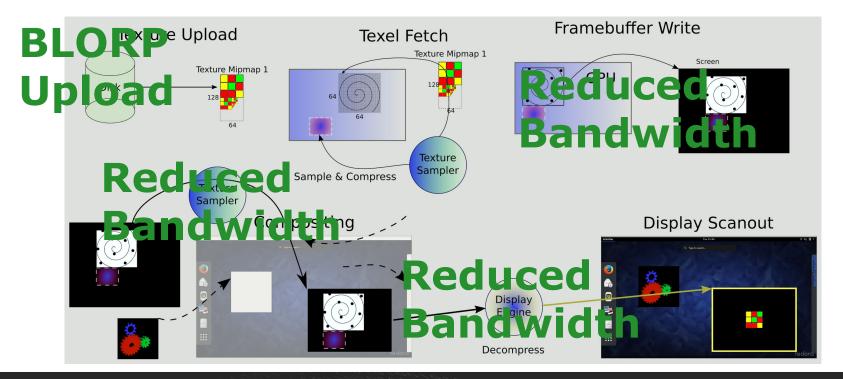
- Relatively low compression
  - 2:1 max on current Intel
  - 4:1 max seems to be industry standard
  - Not everything will be compressible
    - Will never get max.
- Limited by hardware
  - However, many GPUs getting this
    - UBWC (Qualcomm), AFBC (ARM), DCC (AMD), DCC (Nvidia), PVRIC (Imagination)





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#### Several Opportunities for Savings



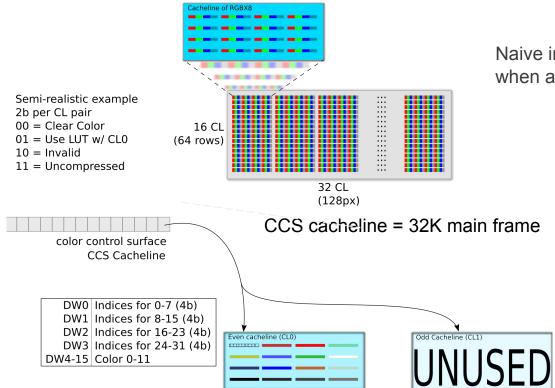




010

#### **Dumb Example**

Naive implementation will get 2:1 compression when a pair of cachelines has 12 or less colors



Software





#### E2E Bandwidth Savings (2:1 compression)

Operation	Color Depth	Desc.	Bandwidth	R/W	
Texture Upload	1Bpc (RGBX8)	File to DRAM	16KB (64 * 64 * 4)	W	
Texel Fetch	1Bpc (RGBX8)	DRAM to Sampler	16KB (64 * 64 * 4)	R	
FB Write	Compressed (2:1)	GPU to DRAM	16KB (64 * 64 * 4) <mark>/ 2</mark>	W	
Compositing	Compressed (2:1)	DRAM to DRAM	32KB (64 * 64 * 4 * 2) <mark>/ 2</mark>	R+W	
Display Scanout	Compressed (2:1)	DRAM to PHY	16KB (64 * 64 * 4) <mark>/2</mark>	R	
<i>Total Bandwidth</i> = (16 + 16 + 8 + 16 + 8) * 60Hz = <b>3.75 MB/s (33%)</b>					



#### Molehills out of Mountains!

Technique	Bandwidth	BW Savings	Disk Savings
Base	5.625 MB/s 16 + 16 + 16 + 32 + 16	-	-
+ HW compositing	<b>3.75 MB/s</b> 16 + 16 + 16 + <del>32</del> + 16	33%	0%
+ DXT1 Compression	<b>2.11 MB/s</b> 2 + 2 + 16 + <del>32</del> + 16	62%	30%
+ E2E Compression	<b>1.17 MB/s</b> 2+2+8+ <del>32</del> +8	79%	30%



#### Intermission

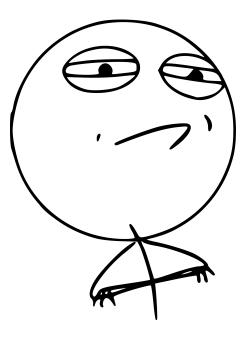






### **Implementation Challenges**

- 1. Currently, everything treats a framebuffer as a buffer of pixels.
  - a. The main buffer is no longer just pixel data.
  - b. There's another buffer! (similar to planar formats)
- 2. Buffer allocation, buffer import/export, and display server protocol need to be made aware of this.
- 3. Applications and compositors cannot rely on compression working everywhere.
  - a. Ex. Skylake doesn't allow compression on pipe C







#### **Several Solutions**

- 1. Encode "modifiers" in fource format
  - a. V4L does this (include/uapi/linux/videodev2.h)
  - b. Works well for entirely proprietary formats
  - c. Concern about amount of bits for modifiers in DRM
    - i. Graphics formats combinatorially explode faster [apparently]
    - ii. Even 64b modifier was questioned
  - d. Never really considered (not sure why)
- 2. Intel specific plane property (<u>original proposal</u>)
  - a. Many other drivers shared similar problem.
  - b. KMS clients wanted a hardware agnostic mechanism
  - c. Protocol still required anyway
- 3. dma-buf metadata
  - a. Just a get/set IOCTL for adding modifiers to a dma-buf





#### The Result - Modifiers

- Some support already landed
- Describes modifications to a buffer's layout
- Easy to add new modifiers to support different tiling formats
- Missing some key pieces
  - Query interface
  - Protocol
  - Driver implementation
- Compression somewhat muddles the definition

commit e3eb3250d84ef97b766312345774367b6a310db8
Author: Rob Clark <robdclark@gmail.com>
Date: Thu Feb 5 14:41:52 2015 +0000

drm: add support for tiled/compressed/etc modifier in addfb2

		<pre>32 pixel_format; /* fource code from drm_fource.h */ 32 flags; /* see above flags */ In case of planar formats, this ioctl allows up to 4</pre>		
	*	utfer objects with offsets and pitches per plane. The pitch and offset order is dictated by the <u>fource</u> , e.g. <u>W12</u> ( <u>http://fource.org/ynv.php# W12</u> ) is described		
		YUV 4:2:0 image with a plane of 8 bit Y samples followed by an interleaved U/V plane containing 8 bit 2 <u>x2 subsampled</u> colour difference samples.		
		So it would consist of Y as offsets[0] and UV as offsets[1]. Note that offsets[0] will generally be 0 (but this is not required).		
	* * * * * *	To accommodate tiled, compressed, etc formats, a modifier can be specified. The default value of zero indicates "native" format as specified by the <u>fource</u> . Vendor specific modifier token. Note that even though it looks like we have a modifier per-plane, we in fact do not. The modifier for each plane must be identical. Thus all combinations of different data layouts for multi plane formats must be enumerated as separate		
	*/ u: u: u:	modifiers. 32 handles[4]; 32 pitches[4]; /* pitch for each plane */ 32 offsets[4]; /* offset of each plane */ 54 modifier[4]; /* ig, tiling, compress */		
}; <drm drn<="" td=""><td>1_mo</td><td>de.h [Git(drm-intel-next-queued)][Cpp]</td><td>(449,1)</td><td>58</td></drm>	1_mo	de.h [Git(drm-intel-next-queued)][Cpp]	(449,1)	58

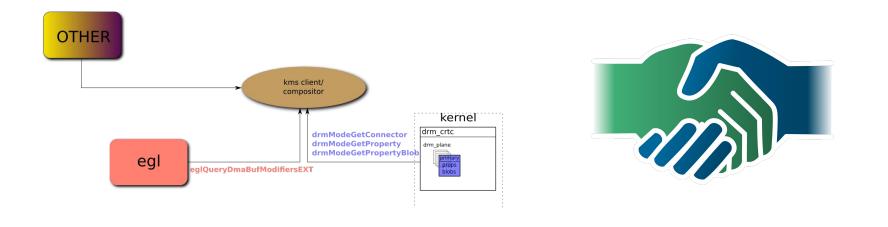




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#### **Step 1: Compositor Negotiation**

Query all "sink" APIs to find out what modifiers are supported for the given format, and hardware.







#### Queries

- Blobifier (KMS blob property for drm\_plane)
  - What modifiers does the plane support?
- EGL extensions
  - EXT\_image\_dma\_buf\_import\_modifiers
    - eglQueryDmaBufModifiersEXT
      - What modifiers does my format support?
      - "is used to query the dma\_buf format modifiers supported by <dpy> for the given format."
- Vulkan/WSI (WIP)
  - VK\_MESAX\_external\_image\_dma\_buf.

Plumbers: Collabora (funded by Intel and Google), Google, Intel



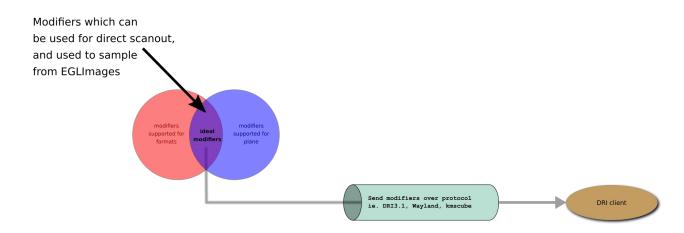


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#### Step 2: Take That and Shove It

down your protocol pipe

With the optimal modifiers in hand, some protocol will tell the client which modifiers it might want to use.







#### Protocols

- Wayland
  - "zwp\_linux\_buffer\_params\_v1" version="3"
- DRI3.1
  - Multi-plane support
  - xDRI3GetSupportedModifiers

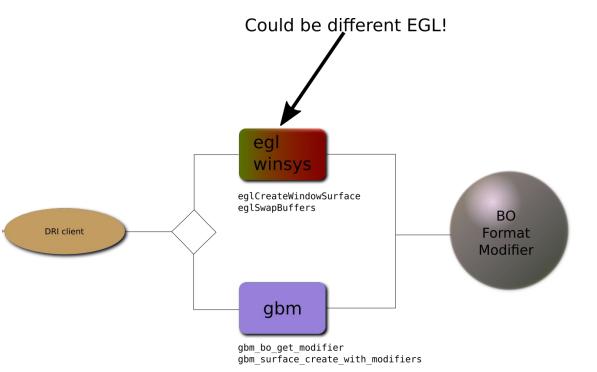
Plumbers: Collabora (paid for by Intel)





#### Step 3: Making BOs

Next, the client creates the buffer either directly, or indirectly with the formats and modifiers it desires.







#### **Buffer Creation**

#### • EGL

- eglCreateWindowSurface
  - Wayland
  - X11
    - (Mesa) Ask over DRI3.1 what's supported
    - (Mesa) Call into DRI driver to create an image

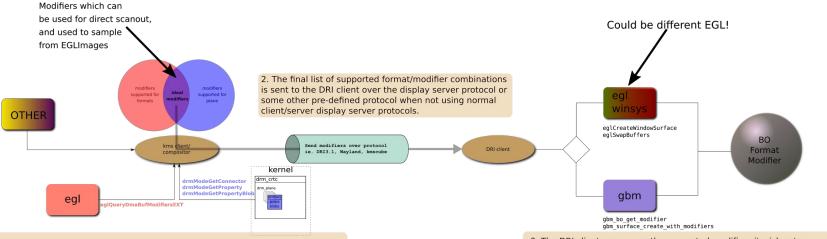
- GBM
  - gbm\_\*\_create\_with\_modifiers
- DRIImage
  - createImageWithModifiers (made for GBM)
  - createImageFromDmaBufs2 (made for DRI 3.1)
- Vulkan/WSI (WIP)

Plumbers: Collabora, Google, Intel





#### The Whole Story Thus Far



1. The KMS client AKA the compositor will query the kernel via KMS APIs to find out what modifiers are supported for the formats it wishes to use on the sinks it wishes to use. To do this, first the KMS client will use the connector found via drmModeGetConnector(), and get a random CRTC from the connector. Next, the primary plane can be found with drmModeGetProperty, and finally, the modifiers comes in as a blob drmModeGetPropertyBlob().

1b. The compositor also queries other sink APIs, eg EGL for texturing from buffer or encoder for screen capture.

3. The DRI client may query the supported modifiers it wishes to use based on the format it wants to render to and creates the buffer. With EGL, this will normally be handled by the EGL winsys layer. It could also be done explicitly via GBM which a compositor or very low level application may do. If it doesn't do this, no modifiers will be used.





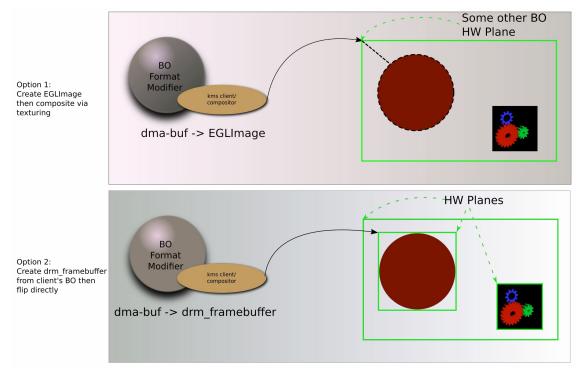
### Display it

- 1. Software Compositing (Option)
  - a. EGL\_EXT\_image\_dma\_buf\_import\_modifiers
  - b. Much work required
- 2. Hardware compositing (Option)
  - a. drmModeAddFB2WithModifiers
  - b. Relatively minor changes required. AddFB2 already supported modifiers
    - i. Add new modifiers to drm\_fourcc.h
    - ii. Added error checking when modifiers change plane count.
    - iii. Driver specific handling of modifiers.





#### He'll Flip You (for real)







#### **Preliminary Results**

"Benchmark"	Original	CCS	%improved
kmscube	1.22 GB/s	600 MB/s	51 (2x)
glxgears	1775 FPS	3900 FPS	54 (2.2x)
TRex			2.3 (.02x)





#### Takeaways

- Memory bandwidth requirements for graphics workloads can be astronomical.
- Don't assume texture compression is the end of the bandwidth story.
- Modifiers "modify" the framebuffer's pixel layout.
- Lossless compression reduces bandwidth, not size
  - Many GPUs support this transparently
- Hardware compositing is great.
- Getting features like this plumbed through can easily be a multi-year effort.
- Haiku isn't supported :/







#### Thank Yous

<u>Platinum Level</u> Kristian Høgsberg, Google Daniel Stone, Collabora

<u>Gold Level</u> Rob Clark, Red Hat Jason Ekstrand, Intel Ville Syrjälä, Intel Daniel Vetter, Intel Liviu Dudau, Arm Ltd Eric Engestrom, Imagination Technologies Varad Gautam, Collabora Topi Pohjolainen, Intel Lucas Stach, Pengutronix Emil Velikov, Collabora Chad Versace, Google Tomeu Vizoso, Collabora





## Q&A (not about EGLStreams)

