# Intel® Open Source HD Graphics Programmers' Reference Manual (PRM)

## Volume 4: Configurations

For the 2014 Intel Atom™ Processors, Celeron™ Processors, and Pentium™ Processors based on the "BayTrail" Platform (ValleyView graphics)

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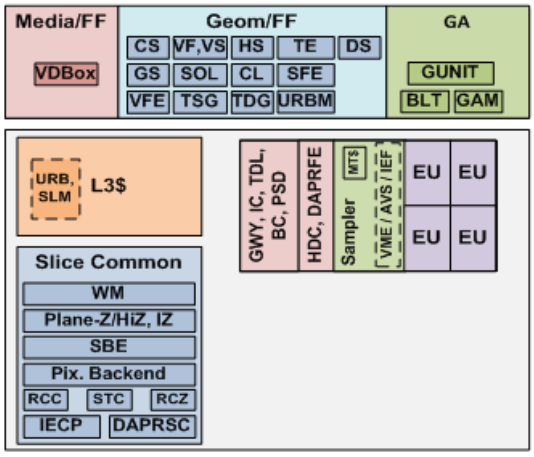
# Table of Contents

# Configurations Overview

The Gen Graphics Architecture was first introduced to the market in 2004. Since that time, the architecture and its implementation have evolved to include many new features while achieving higher performance levels and increasing power efficiencies. This chapter tracks that evolution and provides generational information as to many basic architectural attributes. Further, for each generation, several variants of feature-set and/or performance may be released to the market, to which this chapter acts as a guide.

## Top Level Block Diagram




Above is an organizational block diagram of a Valleyview (VLV) configuration, consisting of the following functional partitions:

(a) Geometry Fixed Functions (Geom/FF)

(b) Media Fixed Functions (Media/FF)

(c) Global Assets (GA)

(d) A Subslice

(e) A Slice-Common block

(f) An L3 Cache (L3$) block.

Note that the combination of (a), (b), and (c) is typically referred to as the “unslice”, while a combination of (d), (e), and (f) is referred to as a compute “slice”.

The functionality in each of these groupings is further broken down as follows:

- Unslice – Fixed function pipelines for 3D, GPGPU, and Media operations, and interface to the outside world.
    - The 3D Geometry / Fixed Function (Geom/FF) block consisting of:
        - 3D fixed function pipeline (CS, VFVS, HS, TE, DS, GS, SOL, SL, SFE)
        - Video Front-End unit (VFE)
        - Thread Spawner unit (TSG) and the global Thread Dispatcher unit (TDG)

        - Unified Return Buffer Manager (URBM)
    - Media fixed function assets including Video Decode (VD) Box
    - The Global Assets (GA) block as the primary interface and memory stream gateway to the outside world, consisting of:
        - GUNIT
        - Blitter (BLT)
        - Graphics Arbiter (GAM)
- Subslice (one instance shown) – A compute unit with supporting fixed- or shared-function assets sufficient for the EU capability.
    - A bank of four Execution Units (EUs)
    - Sampler, supporting both media and 3D functions
    - Gateway (GWY)
    - Instruction cache (IC)
    - Local Thread Dispatcher (TDL)
    - Barycentric Calculator (BC)
    - Pixel Shader Dispatcher (PSD)
    - Data Cluster (HDC) and Dataport Render (DAPRFE)
- Slice Common – Scalable fixed function assets which support the compute horsepower provided two or more subslices.
    - 3D Fixed Function:
        - Windower/Mask unit (WM)
        - Plane-Z, Hi-Z (HZ) and Intermediate Z (IZ)
        - Setup Backend (SBE)
        - Pixel backend units
        - 3D stream caches (RCC, STC, RCZ)
    - Media Fixed Function:
        - DAPRSC
- L3 Cache – backing L3 cache for certain memory streams emanating from subslices.
    - L3 Data cache with support for data, URB, and shared local memory (SLM)

## Device Attributes

| Product Configuration Attribute Table | VLV |
|---|---|
| | 1x4 |
| **Global Attributes** | |
| Slice count | 1 |
| Subslice Count | 1 |
| EU/Subslice | 4 |
| EU count (total) | 4 |
| Thread Count | 8 |
| Thread Count (Total) | 32 |
| FLOPs/Clk - Half Precision, MAD (peak) | N/A |
| FLOPs/Clk - Single Precision, MAD (peak) | 64 |
| FLOPs/Clk - Double Precision, MAD (peak) | 8 |
| **Caches & Dedicated Memories** | |
| L3 Cache, total size (bytes) | 192K |
| URB Size (kbytes) | |
| SLM Size (kbytes) | 0, 64K |
| LLC/L4 size (bytes) | N/A |
| **3D Attributes** | |
| Geometry pipes | 1 |
| Samplers (3D) | 1 |
| Texel Rate, point, 32b (tex/clk) | 4 |
| Texel Rate, bilinear, 32b (tex/clk) | 4 |
| Texel Rate, trilinear, 32b (tex/clk) | 4 |
| Texel Rate, aniso 2x, 32b (tex/clk) | 2 |
| Pixel Rate, fill, 32bpp (pix/clk, RCC hit) | 2 |
| **Media Attributes** | |
| Samplers (media) | 1 |
| VDBox Instances | 1 |